TECHNICAL MANUAL
Volume 2

PBC 1002 Revision 1

pb Packard Bell Computer

A SUBSIDIARY OF PACKARD BELL ELECTRONICS
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PREFACE

This manual is provided for the use of technical personnel engaged in PB250 Computer installation, operation, checkout, and maintenance. It is assumed that such technical personnel are familiar with basic computer technology.

CONTENTS

CONTENTS (Continued)

FIGURES

FIGURES (Continued)

TABLES

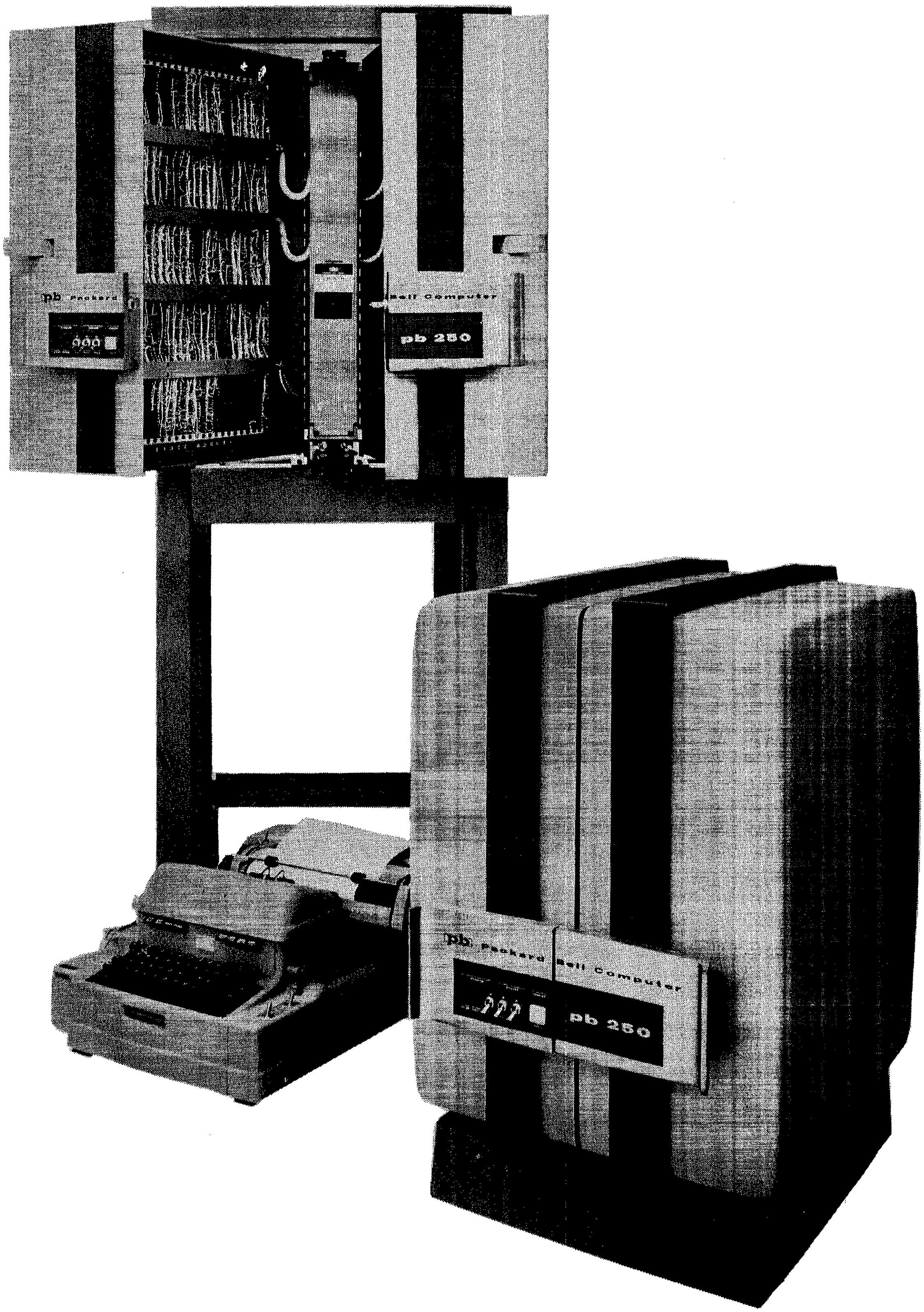


Figure 1-1. PB250 Computer Rack and Desk Mounted

I. DESCRIPTION

A. GENERAL (Figure 1-1)

This publication comprises operating and maintenance instructions for the PB250 Computer manufactured by Packard Bell Computer, Los Angeles, California.

Detailed description and applicable leading particulars are contained in Volume I of this manual.

B. CONTROLS AND INDICATORS

The controls and indicators on the front panel of the PB250 are shown in Figure 1-2 and the applicable functions are described in Table 1-1. The controls and indicators on the front panel of the PS-7 Power Supply are shown in Figure 1-3 and the applicable functions are described in Table 1-2. The Flexowriter manual controls and indicators are shown in Figure 1-4 and the applicable functions are described in Table 1-3. For further information on the Flexowriter switches and keys refer to the vendor's manual, shipped with the Flexowriter.

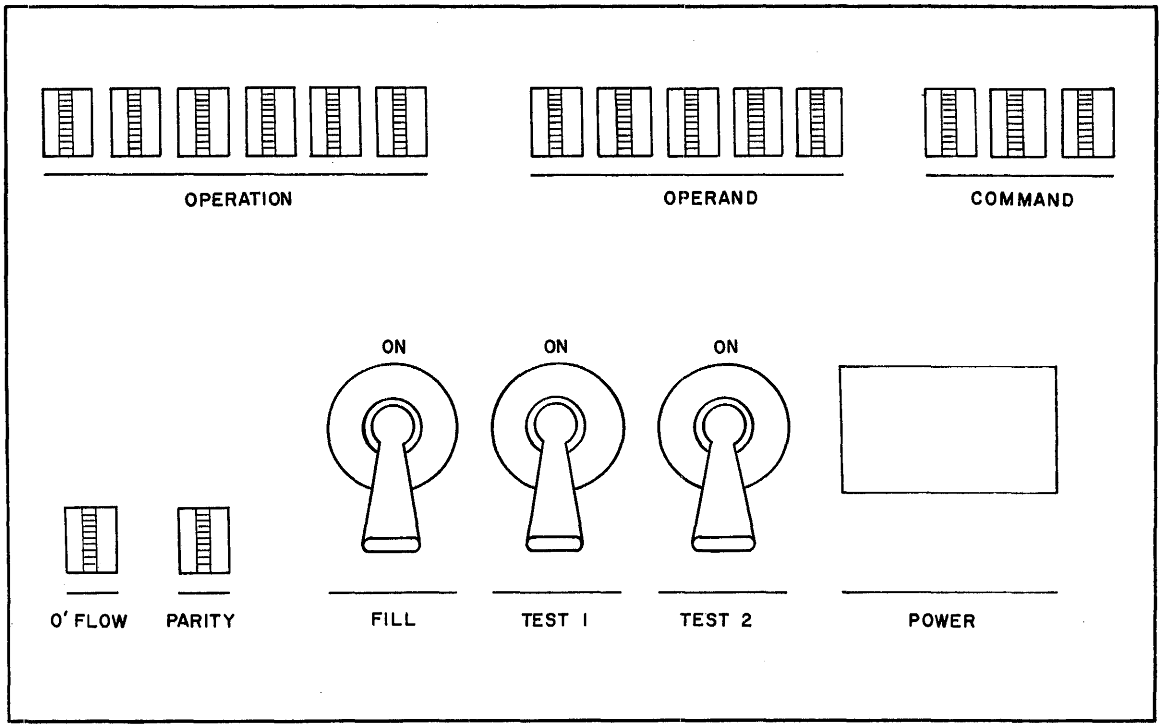


Figure 1-2. **PB250** Control Panel

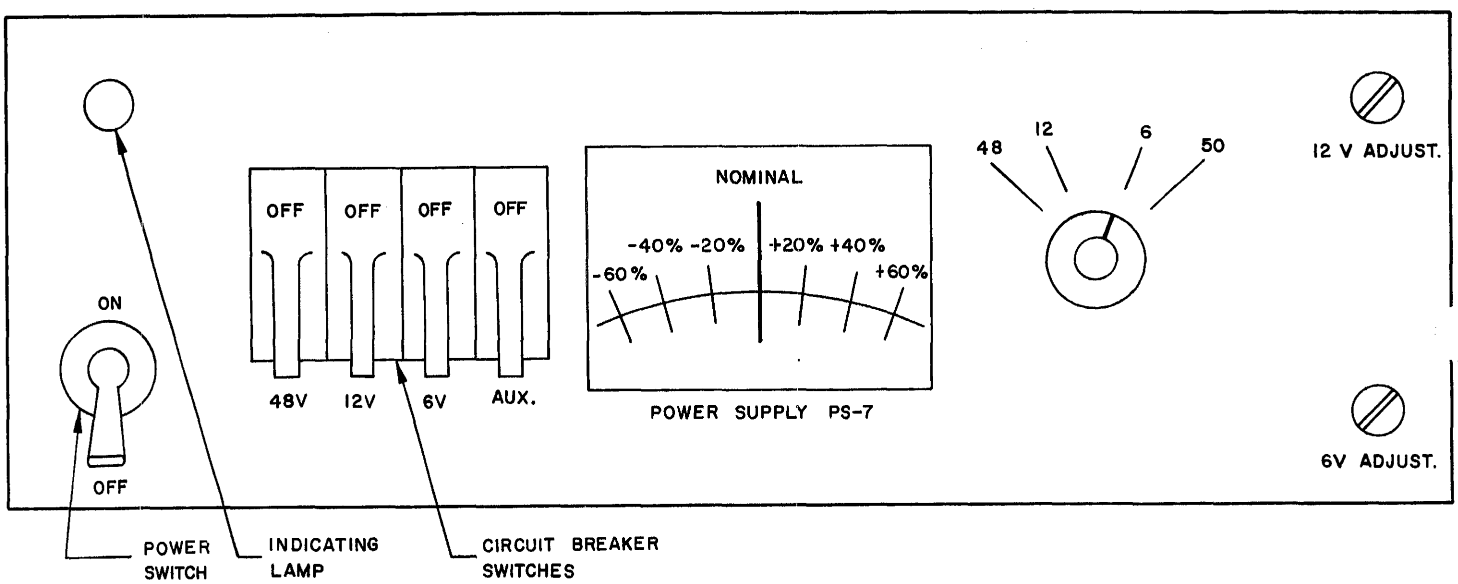


Figure 1-3. **PB250 Power** Supply Control Panel

Table 1-1. (Sheet 1 of 2)

PB250 CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
OPERATION	Green	Within certain limitations, these six indicators specify which op code has been executed, i.e. ADD (command 14 in octal), LOAD A (command 05 in octal) etc. Using a light on to indicate 1 and a light off to indicate 0, the pattern 001100 represents the command ADD in binary format.
OPERAND	Green	These five indicators specify the line number portion of the address.
COMMAND	Green	These three indicators specify from which command line the commands are being executed.
O'FLOW	Green	This indicator is on when an overflow has occurred.
PARITY	Green	This indicator is on when a parity check error is present, or a halt occurs.

Table 1-1. (Sheet 2 of 2)

PB250 CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
FILL		This switch is used to load the bootstrap routine. When this switch is in the ON position, it sets up certain conditions which command the computer to read and store the bootstrap information into memory line one.
TEST 1		This switch is used in marginal testing of the computer circuitry (see Section IV).
TEST 2		This switch is also used in marginal testing of the computer circuitry (see Section IV).
POWER	White	This backlighted indicator switch is used to apply power to the computer, and remains lit as long as power is applied to the computer.

Table 1-2. (Sheet 1 of 2)

PS-7 POWER SUPPLY CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
Power Switch		This toggle switch is used to apply ac power to the computer POWER switch.
Indicating Lamp	Amber	The indicating lamp is lit when the PS-7 power switch is in the ON position.
Circuit Breaker Switches		The four magnetic circuit breaker switches provide circuit protection against overload of voltage supplies within the PS-7.
Output Voltage Meter		This meter is used in conjunction with the Voltage Selection Switch to check indicated voltages. The meter also is used in calibration of the +6 and -12-volt dc output voltages. When these voltages have been correctly adjusted, the needle will be in NOMINAL position. Other indications are plus or minus percentages of the nominal output voltage.

Table 1-2. (Sheet 2 of 2)

PS-7 POWER SUPPLY CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
Voltage Selection Switch		This four-position rotary switch allows selection of a particular voltage as shown on the switch.
12 V ADJUST 6 V ADJUST		These potentiometers are used to adjust the +6 or -12-volt output voltages to the required reading on the Output Voltage Meter.*

*For correct adjustment procedures, refer to Section II of PS-7G Power Supply Technical Manual PBC 3006.

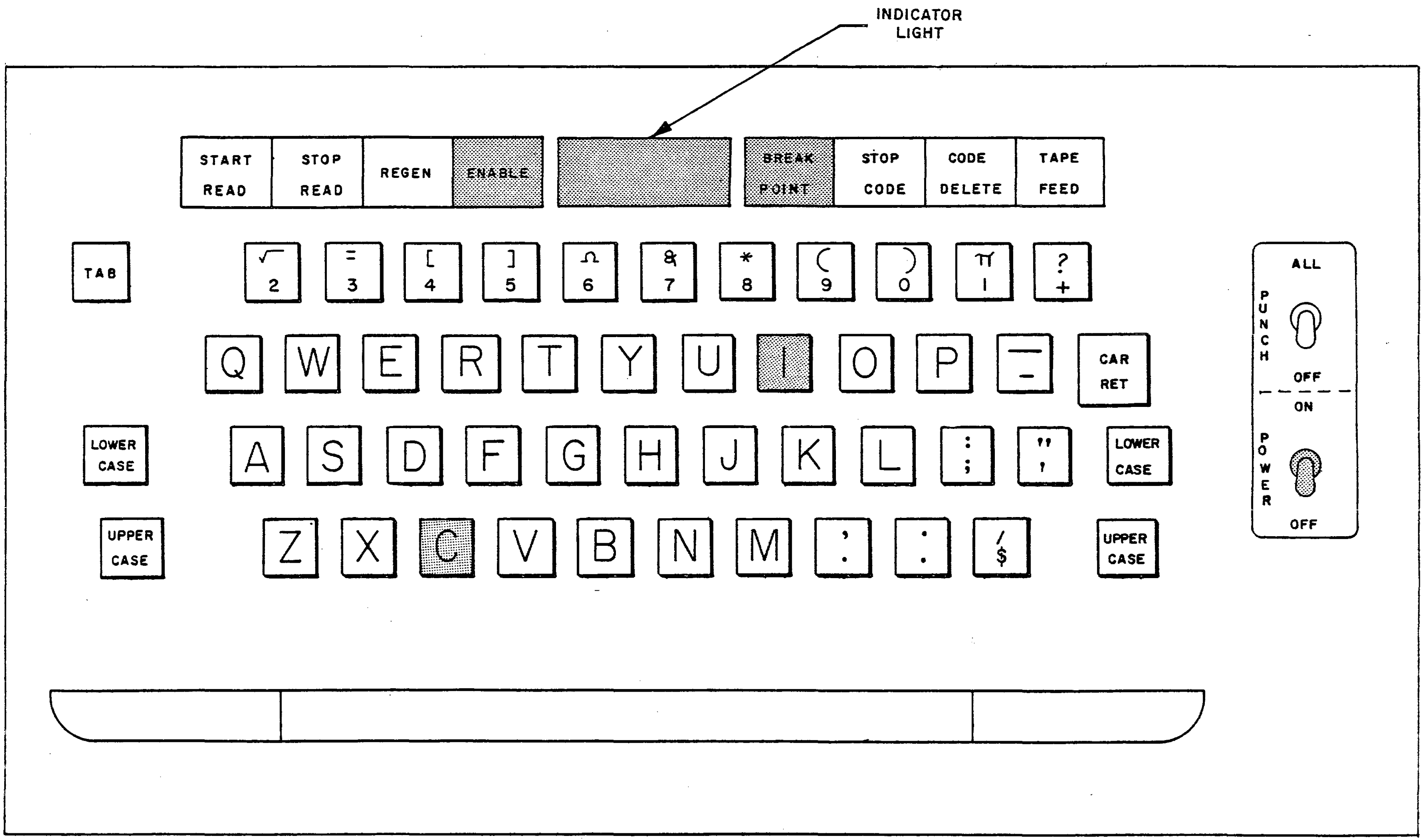


Figure 1-4. Flexowriter Keyboard

Table 1-3. (Sheet 1 of 2)

FLEXOWRITER CONTROLS AND INDICATORS

Control or Indicator	Color	Function and/or Indication
ENABLE Switch		This switch is used to interrupt the PB250 computation process, and condition for use switches and keys of the Flexowriter.
BREAKPOINT Switch		This switch causes signals to be sent to the PB250 which may be tested by TES (Transfer on External Signal) command, and together with the ENABLE switch in down position will clear the parity flip-flop (PARITY indicator light lit, see Figure 1-2).
"I" Key		When the "I" key is operated with the ENABLE switch in down position, the PB250 will be set to execute the command in memory location 00001.
"C" Key		When the "C" key is operated with the ENABLE switch in down position, the PB250 will read and execute the next desired command,

Table 1-3. (Sheet 2 of 2)

FLEXOWRITER CONTROLS AND INDICATORS

Control or Indicator	Color	
"C" Key (Continued)		and then halt. The "C" key is referred to as the "single-cycle key."
Indicating Light	White	When the indicating light is lit, it indicates that the PB250 is ready to receive information.

B-1. ELAPSED TIME INDICATOR

The five digit elapsed time indicator is mounted above the computer master circuit breaker on the spine inside the computer. The indicator employs a synchronous motor for 50-60 cycles per second operation, and accuracy of the unit is determined by the regulation of the line frequency. Power consumption of this unit is approximately 3 watts at 115-volts ac and it will operate reliably within a voltage variation of ±10%. Temperature rise of the motor is less than 45°C at rated voltage and frequency; tolerance on the reading, at 50-60 cycles per second, is ±1 digit.

B-2. MASTER CIRCUIT BREAKER

The computer master circuit breaker is mounted below the elapsed time indicator on the spine inside the computer. The single pole circuit breaker has an electrical rating of 125-volts ac, 60 cycles per second, 0.020 amp to 50 amps. Circuit interruption may occur at 1% but must occur at 25% over the rated load.

II. INSTALLATION

A. GENERAL

This section of the manual covers the basic considerations pertinent to installation procedures for the PB250 Computer or computer system. The initial installation of the PB250 Computer is made by a customer service representative of Packard Bell Computer Corporation.

B. INSTALLATION REQUIREMENTS

The following paragraphs discuss the preinstallation, installation, and preoperational requirements for the PB250 Computer.

B-1. SPACE

The PB250 Computer has been constructed to occupy a minimum space, whether table or rack mounted. Figure 2-1 shows the typical space requirements of the PB250R. Both equipments require identical extension areas, but differ in height requirements.

Prior to the installation of computer or computer system, consideration must be given to the space required for storage of tapes, spare parts, tools, test equipment, and other miscellaneous equipment.

B-2. PREINSTALLATION

Before a decision is made on the precise location of the PB250 in the selected area, the following points should be observed.

a) Ensure that computer programmer will have unobstructed view of the PB250 Computer and Flexowriter, and other associated equipment, from a given position.

b) Ensure the existence of ample good lighting in the data processing area.

c) Ensure isolation of the PB250 Computer from noisy machinery of manufacturing areas. Noise may distract the computer programmer and lead to possible errors.

d) Ensure that the data processing area is restricted to authorized, qualified personnel. Ideal facilities are such that the computer programmer may work while completely free of any interruption or diverting influence.

B-3. TEST AND MAINTENANCE EQUIPMENT

In addition to the requirements contained in paragraph B-1, consideration must be given to the space required for test and maintenance equipment.

The following equipment is recommended for proper test and maintenance of the PB250 Computer.

a) Oscilloscope. Tektronix Type 545A with 53C and CA Plug-In Units.

b) Module Tester. Packard Bell, Type MT-I, for testing all modules and delay lines.

c) Work Bench. To facilitate working on modules or units.

d) Electrical Outlets. A sufficient number for connection of test equipment and soldering irons.

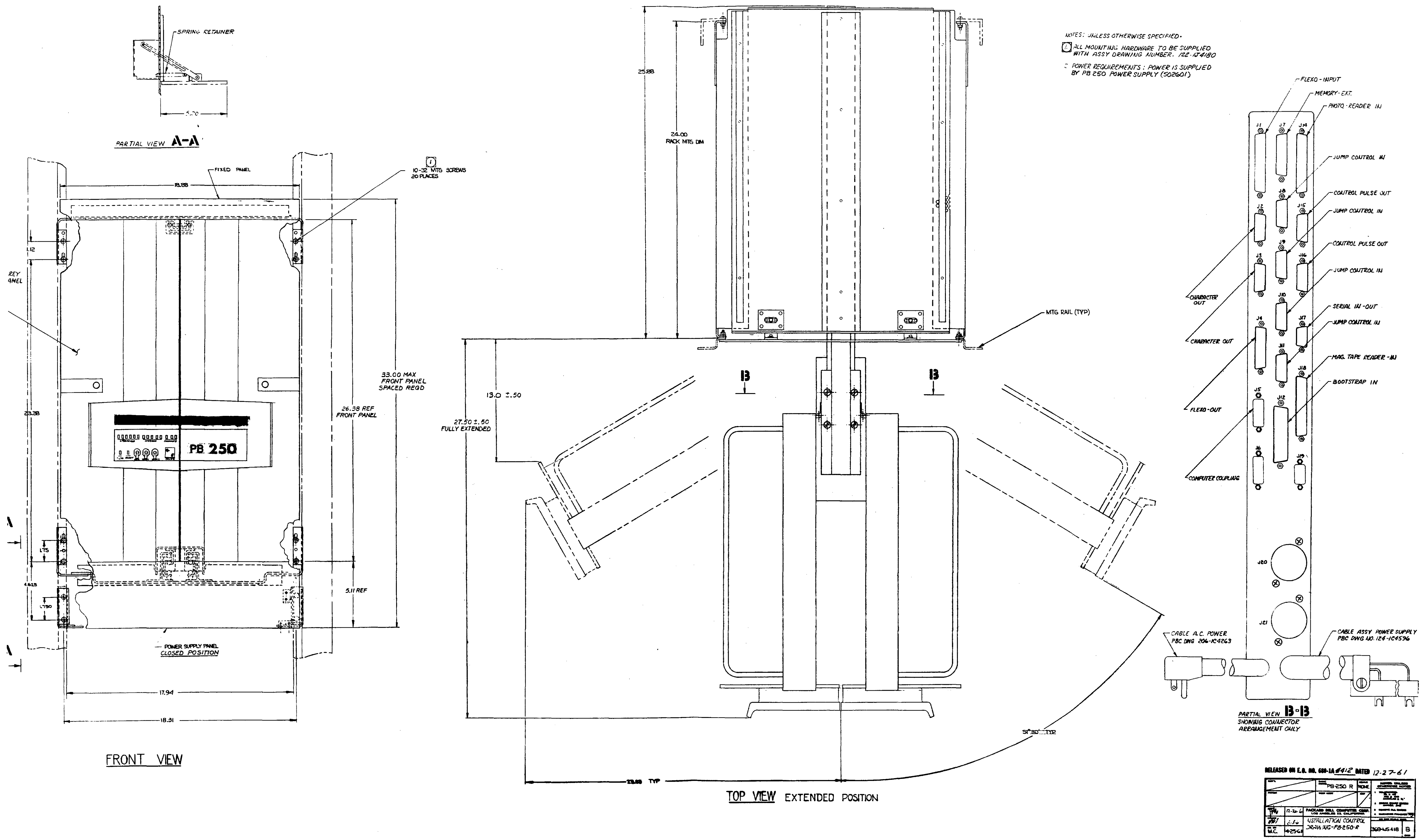


Figure 2-1. PB250 Computer Space Requirements

e) Filing System. The initiation of a filing system will greatly assist the recording of modifications, changes or malfunctions of equipment. Reference to this record may help to establish a failure rate of the computer or computer system and provide data useful in troubleshooting.

Up-to-date schematics of the equipment should be readily available in the immediate vicinity of the computer. A system may be established in the field service group to cover modifications and changes which can be helpful to other field service engineers. A documentary paper detailing the latest changes should be published periodically and made available to all personnel concerned with the equipment.

B-4. ENVIRONMENT

For proper PB250 Computer operation, the ambient temperature in the data processing area must be between the limits 41°F and 113°F (5°C and 45°C). Most data processing areas are air-conditioned to maintain a stable temperature for the equipment.

B-5. POWER

Operating power for the PB250 Computer is a 115-volt, 60-cycle, single-phase input which should be free of transients and have reasonably good regulation. The computer operates satisfactorily between the parameters with line voltage variations between 100-volts ac and 125-volts ac (115-volts ac optimum) and under normal conditions, draws approximately 110 watts.

B-6. CABLING

Installation of the cables from the PB250 Computer and the Flexowriter has been simplified by keying of the connectors. The cables consist of one input, one output, and two ac line cords. During installation of the computer or computer system, it is preferable that interconnecting cables be run in channels beneath the floor level. This method ensures a neat system layout and eliminates possible hazards to personnel.

C. PRECAUTIONS

The following precautions must be observed when installing or operating the PB250 Computer.

1) If the unit is to be uncrated by other than a Packard Bell Computer representative, caution must be exercised when removing the base of the shipping crate. The large Phillips-head bolts must be removed one at a time and similarly replaced by the bolts supplied in the attached plastic bag. The one-by-one sequence is important because these bolts support the power supply.

2) Do not attempt to remove the balance weight from the base of the PB250R (rack-mounted) computer unless the computer has been securely bolted down.

3) Use caution in extending the PB250R Computer or Flexowriter from the rack frame.

4) Do not attempt to unlatch or open the sides of the computer until the unit has been fully extended.

5) Do not attempt to move the computer until the sides are closed and the front handles latched.

III. OPERATION

A. GENERAL

The PB250 Computer is designed to function efficiently as a systems component to connect directly with various items of peripheral equipment. These devices are fully described in Packard Bell Computer Technical Manuals as listed below.

1)	MTU-1	Magnetic Tape Unit	PBC 1014
2)	MTC-1	Magnetic Tape Control Unit	PBC 1015
3)	HSB-N	High-Speed Buffer Register	PBC 1007
4)	HSR-1	High-Speed Reader	PBC 1010
5)	HSP-1	High-Speed Punch	PBC 1009
6)	MX-1	Memory Extension	PBC 1011
7)	PS-7G	Power Supply	PBC 3006
8)	PS-8	Power Supply	PBC 1013
9)		Flexowriter	PBC 1016
10)		Interface	PBC 1005

B. OPERATING PROCEDURE

The sequential operating procedure for the PB250 Computer is as follows:

1) Preoperational Setup
2) Operational Procedures

B-1. PREOPERATIONAL SETUP

The following procedures are to be followed for preoperational setup:

1) Make certain that cabling between computer and Flexowriter are properly secured.

2) Check that all switches on computer and Flexowriter are off or in normal position.

3) Check that ac cables from computer and Flexowriter are connected to proper external source of 115-volt ac power.

4) Open computer and set circuit breaker switch to ON position. (Breaker switch is located on spine of computer.)

5) On front panel of power supply set all breaker switches to ON.

6) On front panel of power supply turn power switch to ON.

7) On computer front panel press POWER switch to ON. After pushbutton release make certain that switch remains back-lighted.

8) On Flexowriter set POWER switch to ON.

B-2. OPERATIONAL PROCEDURES

The following step-by-step procedures are followed, a) check the Flexowriter, and b) load the computer, and c) check computer operation.

1) On Flexowriter insert bootstrap tape into reader mechanism.

2) On front panel of computer set FILL switch to ON.

3) On Flexowriter press ENABLE switch, then press and release BREAKPOINT switch. (BREAKPOINT switch will reset parity flip-flop.) The computer begins to read tape. The computer will stop after the first stop code has been read.

4) When tape stops turn FILL switch to OFF.

5) To start computer operation under computer control, press ENABLE switch on Flexowriter to down position.

6) On Flexowriter strike "I" key.

7) On Flexowriter press BREAKPOINT switch to down position.

8) On Flexowriter release BREAKPOINT switch.

9) On Flexowriter release ENABLE switch. Computer operation will begin.

IV. MAINTENANCE AND TROUBLESHOOTING

A. GENERAL

The PB250 Computer is designed to function with a comparatively trouble-free life and the necessary maintenance is at a minimum. However, the computer should be regularly tested under marginal conditions. If the computer fails to meet these marginal requirements, the probable cause may be a weak module card.

The following paragraphs are intended as a guide in performing marginal checks on the ability of the computer memory and of all the commands to function properly under marginal conditions.

B. MARGINAL CHECKING

To find the margin of safety between the condition of a system and the point of failure, use is made of marginal checking. In the PB250, this procedure is normally followed in routine maintenance to locate deteriorating components before they cause system failure, although in many instances, routine marginal checking may not be necessary due to the comparatively long life of modern transistors. Marginal checking of the PB250 is accomplished by use of:

1) PROBE I Diagnostic Routine.

2) TEST 1 and TEST 2 switches on the computer control panel (Figure 1-2).

3) Varying the +6 and -12 voltage levels on the PS-7 Power Supply between ±5% limits (Figure 1-3).

B-1. CHECKING PROCEDURE

The marginal checking procedural steps are as follows:

a) Load and start operation of PROBE I (see paragraph C, below).

b) Set TEST 1 switch to ON position.

c) Wait two minutes then set TEST 1 switch to OFF position. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

d) Set TEST 2 switch to ON position.

e) Wait two minutes then set TEST 2 switch to OFF position. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

NOTE

Both TEST switches must not be in ON position at the same time or an illegal indication may result.

f) Set Voltage Selector switch to 6.

g) Allow PROBE I to run, and decrease the +6-volt supply by 5% by means of the adjustable control on the power supply front panel (Figure 1-3). Adjust meter indication to NOMINAL, if no failure is apparent, proceed to step h . If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

h) Allow PROBE I to run, and increase +6-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

i) Set Voltage Selector switch to 12.

j) Allow PROBE I to run, and rotate voltage selection switch on the power supply front panel to 12. Decrease -12-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if no failure is apparent, proceed to step k. If failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

k) Allow PROBE I to run, and increase -12-volts by 5% as explained in step g. Adjust meter indication to NOMINAL, if failure exists the diagnostic routine type-out will indicate where the marginal command or commands are located. Refer to Bootstrap Diagnostic Routines to check commands and identify marginal components.

C. PROBE I DIAGNOSTIC ROUTINE (CAT. # 9003)

A description of the PROBE I diagnostic routine is provided in Table 4-1, followed by the program listing in Table 4-2 and the flow diagrams in Figure 4-1.

Table 4-1. (Sheet 1 of 10)

PROBE I DIAGNOSTIC ROUTINE

Purpose:	To test the read-write circuitry of the PB250 memory under operator control. To check all commands in the PB250 under marginal operation. To check the punching and reading phases of the Flexowriter. In addition, the program may link test routines for various peripheral equipments by changing one of the commands (see Use).
Restrictions:	Lines 00 through 07 must be in the machine. Line 00 must be a medium line. If more than minimal operation is desired, an external switch bank must be connected to the computer.
Storage:	All sectors of lines 02 and 03 are used by the program. Sectors 000 through 051, and sector 377 of line 01 are used by the bootstrap loader. The contents of these sectors may be destroyed once the program is loaded. All line 00 sectors are used for temporary storage.
Timing:	When checking memory, the program requires approximately three seconds to write and read one line (optimized). When checking commands, the program requires about one second to test all commands in one line.

PROBE I DIAGNOSTIC ROUTINE

Timing: (Continued)	When checking the punch-read phase of the Flexowriter, the program proceeds at the Flexowriter speed of 15 characters per second.
Use:	1. Loading Two tapes are available; one has its own bootstrap loader, and the other may be loaded by the Octal Utility Package. Total time required to load the program is (depending on the tape used) 3-1/2 - 4 minutes. a. Bootstrap Loading This tape may be loaded by bootstrap control through conventional use of the FILL switch on the console. Upon completion of loading, if there is no checksum error, control is transferred to sector 000 of line 02. A TRU command to 00002 will be placed in sector 000 of line 01 by the bootstrap so that control may be returned to the beginning of the program at any time by using the ENABLE switch and I key. If there has been a checksum error, the machine will halt and display a line number of $37)_8$ on the OPERAND lights. b. Octal Utility Package Loading This tape may be loaded by the Octal Utility Package by inserting the tape in the mechanical reader and striking the F key. Be sure the BREAKPOINT switch is raised, or loading will halt half way through. Should this happen, the remainder of the tape may be loaded by re-striking the F key. On completion of successful loading, the keyboard light will come back on and control may be transferred to the program by striking the T key. If there has been a checksum error, the machine will halt and display a line number of $37)_8$.

Sector 000 of line 02 is the beginning of the program and contains a HALT with a line number of $30)_8$. The HALT instruction indicates the beginning of the program and allows the operator to set up the desired switch configuration. Once everything is in order, the program may be started by clearing parity and raising the ENABLE switch.

2. Modes of Operation

There are two basic modes of operation in the program; Memory and Command. The mode is determined by the position of the BREAKPOINT switch as follows: with BREAKPOINT in the raised position the program operates in Memory Mode (Write-Read II); with BREAKPOINT in the depressed position the program operates in Command Mode. In Memory Mode all lines may be checked except lines 00, 01, 02, and 03. In Command Mode, all commands are checked except DVR, RTK, PTU, and BSO. With no external switch bank connected, the program will check lines 04 through 07 in Memory Mode and lines 03 through 07 in Command Mode. For more specific or extended uses, an external switch bank must be connected to the computer.

3. Switch Bank

For more effective operator control, the program has been set up to scan a switch bank and limit or extend its operation according to the switch settings. The switch bank should be connected so as to be addressable by TES commands on lines 10 through 17. The switches should be wired such that transfer of control will be effected when a switch is in a raised position. Wiring instructions and lists are in Section VI, Logic Diagrams.

PROBE I DIAGNOSTIC ROUTINE

The switch bank is divided into two sections of four switches each. The four left-hand switches define an instruction, and the four right-hand switches define an address. All address designations are in octal.

a. Memory Mode

The following sub-table shows the switch controls for operation in the Memory Mode.

MEMORY MODE

Switch Line	Raised	Lowered
10	Program halts after checking specified lines.	Program continues after checking specified lines. Switches are rescanned for new instructions.
11	Program will only WRITE random numbers into specified lines.	Program write-reads continuously through all specified lines.
12	Program checks only that line indicated on ADDRESS SWITCHES	Program checks all lines from 04 up to line indicated on address switches.
13	Program write-reads lines 04 through 17.	Program write-reads lines 04 through 07.

When the program is instructed to halt (switch 10), it will halt and display a line number of $30)_8$ which indicates the beginning of the program. Clearing parity at this point will resume computation. Where possible ambiguities occur, lower numbered switches have priority over higher numbered ones. Thus, if switches 12 and 13 are both raised, switch 13 is ignored. With switch 11 raised, random numbers are stored continuously throughout memory but no checking is done. When it is desired to return to Write-Read (by lowering switch 11), the ENABLE switch must be depressed and the I key struck to return control to the beginning. Failure to do this will cause the program to go directly to the Read phase of the Write-Read program and an apparent error will occur due to the fact that the original random number is no longer correct. No complications will result other than the usual error punch-out which may be interrupted by pressing the ENABLE switch.

If an error is detected during a Write-Read phase, the Flexowriter will punch out the sector and line where the error occurred, followed by the number that should have been found and the number that was found. If the error is one of parity, the machine will halt and display an 05 code in the OPERATION lights and the line number where the error occurred in the OPERAND lights. Clearing parity will resume punch-out. Whenever five consecutive errors are noted, the entire line is assumed to be bad and the program will continue with no further punch-out for that line. Switches may be altered during any phase, but their states will not be determined until the current phase is complete. This is a cardinal rule for all operations in the program.

NOTE

> No new phase will be initiated, regardless of switch positions, until the current phase is complete. In some cases, this may be 30 or 40 seconds.

PROBE I DIAGNOSTIC ROUTINE

Switches 14 through 17 indicate a line address associated with the operation indicated in switches 10 through 13. Thus, 1001 on the switch bank specifies line $11)_8$. A line configuration of 0000 will indicate lines 04 through 07/17 are to be checked, depending upon the state of switch 13. In this case, switch 12 is ignored. Line configuration 0001, 0010, and 0011 are unused in this mode and will be rejected. In the event unused codes are encountered, the program will loop and rescan the switch bank until a legitimate combination is indicated. Sector 073 of line 02 contains a TAN command which notes if an illegal combination is present and returns control to rescan the switches. If so desired, these unused positions may be used to transfer out of PROBE I to other test programs by changing the TAN command to transfer to the desired location. When returning from an external test program, a transfer to sector 000 of line 02 will halt computation at the beginning of PROBE I. If it is desired to return to PROBE I without halting, transfer should be made to sector 001 of line 02.

b. Command Mode

The following sub-table shows the switch controls for operation in Command Mode.

COMMAND MODE

Switch Line	Raised	Lowered
10	Program halts after each Block check	Program continues after each block is checked.

10 Raised: Program halts after each block checked   Lowered: Program continues after each block is checked

Table 4-1. (Sheet 7 of 10)

PROBE I DIAGNOSTIC ROUTINE

COMMAND MODE (Continued) Breakpoint [illegible]

Switch Line	Raised	Lowered
11	Program repeats current block using same number only if error occurs.	Program halts if error in current block and displays block number in OPERAND lights.
12	Program repeats current block using different numbers unless error.	Program continues to next block in sequence with a different number unless error.
13	Program executes commands in all lines, 03 through 17.	Program executes commands in all lines, 03 through 07.

There are $20)_8$ command blocks in this mode which operate with random numbers where applicable. Command blocks are numbered $01)_8$ through $20)_8$, consecutively and the commands checked in each block are listed below. When one block is complete, if no error is noted, the next block in sequence is checked, and so on. When the last block has been checked, the program is moved to the next higher line and the process repeats. When the last line has been checked, the program returns to scan the switches and proceeds from there. The time required to check the entire $16)_{10}$ blocks is about one second and the progress of the program through the lines may be noted by observing the K flip-flops on the computer console.

Whenever the program executes a halt in this mode, the block number where the halt occurred will be displayed on the OPERAND lights except when the last block is reached and the program returns to the beginning, at which time the line number displayed will be $30)_8$. If switch 10 is raised, the program will halt unconditionally after each block. Thus, if it is desired to repeat block 06 continuously, switch 10 should be raised and the program cycled by means of the ENABLE switch until 06 appears on the OPERAND lights. Then switch 12 should be raised, switch 10 lowered, and the program allowed to run. In this manner, block 06 will be checked continuously with different numbers until an error is detected or the switch configuration is changed.

Switches 14 through 17 define an address to be used in reference to the other switches. A switch configuration of 0000 will automatically check lines 03 through 07/17 depending on the setting of switch 13. An address of 0010 will initiate a punch-read phase. In this phase, five inches of leader are punched, followed by a marker character of 8 "ones" and 64 frames of random digits. When the last frame has been punched, another five inches of trailer is punched and the frames punched are read back into the machine and checked. During punch-out, there will be sufficient time for the operator to insert the tape in the mechanical reader so that reading may be started immediately on completion of punching. When an error is detected, the reader halts momentarily (about three seconds) and the light on the Flexowriter flashes. If the ENABLE switch is pressed while this light is on, the character just read may be viewed in the OPERATION and OPERAND lights on the console. By comparing the state of the lights against the frame just read, the operator may determine which read channel has failed. If the frame and display agree, then the error occurred during the punch phase. Raising the ENABLE switch will allow resumption of the test. When the test is complete, the program returns to the beginning and halts with a line display of $30)_8$.

All other configurations of the address switches indicate which line is to be tested. Only the particular line indicated will be tested. Line 01 may be tested, but if the Octal Utility Package is in this line, it will be destroyed. When the program is loaded by bootstrap, a TRU command to 00002 is stored in sector 000 of line 01 so that control may be returned to the beginning of the program at any time by use of the I key. This TRU command is also in sector 000 of line 03 and, when line 01 is tested, this command will be moved to 00001 so that the operator may still return to sector 000 of line 02 even after destroying the former contents of line 01 by checking that line.

The following sub-table lists the command blocks by number (in octal) and the commands checked in that block. Commands which are not listed in this sub-table are considered to have been checked elsewhere, i.e., LAI, CIB, etc.

COMMAND BLOCK NUMBERS

Block Diagram	Commands Checked
01	IAC, IBC, ROT
02	LDC, CLA, ADD, SUB
03	MUP, DIV
04	MAC, AMC, EXF, AOC
05	LDP, STD, DPA, DPS, TOF
06	TAN, TBN, TCN, TRU, CLB
07	LDB, STB, EBP, IAM
10	LDA, CLC, STC, NAD, SAI
11	RSI, CAM
12	MLX, LST (26 [illegible]) SLT

Table 4-1. (Sheet 10 of 10)

PROBE I DIAGNOSTIC ROUTINE

COMMAND BLOCK NUMBERS (Continued)

Block Diagram	Commands Checked
13	RFU, DIU, TES (36)
14	LRS, GTB
15	NOP
16	SBR, LSD
17	BSI, STA
20	SQR

Table 4-2. (Sheet 1 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
000	000 0030;	HLT	= Start of program
001	002S0702;	LDP	
002	000S0000;	CONST	Clear A and put marker bit in B
003	000 0000;	CONST	
004	020S7100;	MCL	Initialize
005	[050 7710;]	TES	
006	047S1400;	ADD	Add 1 if switch lowered
007	000 00001	CONST	
010	052 2110;	LST	1
011	047 3602;	TBN	Exit if B negative
012	112S0100;	IAC	
013	125 0500;	LDA	
014	135S1400;	ADD	Increment line
015	000 0001;	CONST	
016	145 1100;	STA	
017	044S0100;	IAC	Return to next switch
020	045S3700;	TRU	Read switches
021			
022	023S0402;	LDC	Begin memory mode
023	000 0002;	CONST	
024	015 1000;	STC	Set first line = 04
025	034 2210;	RST	6
026	032 3602;	TBN	Switch 13
027	030S0402;	LDC	
030	000 0043;	CONST	$\overline{\text{S13}}$; last line = 07
031	034S1000;	STC	
032	033S0402;	LDC	
033	000 0047;	CONST	S13; last line = 17
034	014 1000;	STC	
035	037 2200;	RSI	1

Table 4-2. (Sheet 2 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
036	042 3602;	TBN	Switch 12
037	040S0402;	LDC	
040	076 3502;	TAN	$\overline{S12}$; Disable setting of last line
041	044S3702;	TRU	
042	043S0402;	LDC	
043	015 1100;	STA	S12; Enable setting of last line
044	075 1002;	STC	
045	050 2210;	RST	2
046	056S3702;	TRU	
047	000 1100;	STA	Save scanned word
050	051S0502;	LDA	
051	000 0377;	CONST	Take one's complement
052	000 1500;	SUB	
053	100 7735;	TES	B.P.
054	022S3702;	TRU	
055			
056	062 3602;	TBN	Switch 10
057	060S0402;	LDC	
060	001S3702;	TRU	$\overline{S10}$; Set return for no halt
061	064S3702;	TRU	
062	063S0402;	LDC	
063	000S3702;	TRU	S10; Set return for halt
064	264 1003;	STC	
065	072 2110;	LST	4
066	000 4500;	CLA	
067	075 2110;	LST	Save address only
070	003 5602;	CAM	If address = 0000, exit
071	077 7502;	TOF	to Write-Read II
072	023 1502;	SUB	Subtract 4,
073	001 3502;	TAN	If negative, return to rescan

Table 4-2. (Sheet 3 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
074	023 1402;	ADD	Not negative, restore address
075	015 1100;	STA TAN	Address = first line if S12
076	014 1100;	STA	Address = last line
077	124S4400;	CLC	Set read mode and exit
100	101S0402;	LDC	Begin command mode
101	000 0041;	CONST	Set index = 03
102	103 1037;	STC	
103	104S4002;	EBP	For switch 13
104	377S7720;	CONST	
105	110 3502;	TAN	
106	030 0402;	LDC	$\overline{S13}$; set last line = 07
107	111S3702;	TRU	
110	033 0402;	LDC	S13; set last line = 17
111	012 1000;	STC	
112	000 0100;	IAC	
113	033 4202;	AMC	Extract off address
114	000 0300;	ROT	
115	003 5602;	CAM	Exit if address = 0000
116	372 7503;	TOF	
117	120S5602;	CAM	
120	000 0001;	CONST	Exit to punch-read if address = 0010
121	265 7503;	TOF	
122	123 1137;	STA	Otherwise address to index
123	012 1100;	STA	And last line
124	372S3703;	TRU	Exit to command mode
125	160 1002;	STC	Store phase constant
126	127S0502;	LDA	
127	047 2646;	CONST	Prestore first random number
130	004 1100;	STA	
131	005 1100;	STA	

Table 4-2. (Sheet 4 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
132	141 3402;	TCN	Test phase constant
133	135 2100;	LSD	Was read, set write
134	160 1002;	STC	
135	005 0500;	LDA	Ki ⟶ Ko
136	004 1100;	STA	
137	155 0600;	LDB	First line to index
140	143S1237;	STB	
141	143 2200;	RSI	
142	160 1002;	STC	Was write, set read
143	171S3702;	TRU	
144	152 3402;	TCN	Test phase constant
145	146S0702;	LDP	= read
146	000 0000;	CONST	
147	200 5600I	$\boxed{\text{CAM}}$	Reset error counter (Ce)
150	007 1200;	STB	and prestore CAM
151	154S3702;	TRU	
152	153S0502;	LDA	
153	200 1100I	$\boxed{\text{STA}}$	Prestore STA
154	156 1102;	STA	
155	164S7100;	MCL	Put store-check sequence in line 00
156	$\boxed{200\ 1100I}$	CAM STA	
157	240S0400;	LDC	
160	377S7777I	CONST	Store and check sequence
161	244 7502;	TOF	
162	250 3402;	TCN	
163	266S3702;	TRU	
164	165S0600;	LDB	With Ki
165	355S65671	CONST	
166	167S0402;	LDC	
167	046 2233I	CONST	= +2304555

Table 4-2. (Sheet 5 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
170	220S3200;	MUP	Generate Ki + 1
171	004 0500;	LDA	
172	005 1100;	STA	Ko $\longrightarrow$ Ki
173	137S3702;	TRU	
174	007 1000;	STC	(From 276) Ce + 1 = Ce
175	176S1102;	STA	Save Nr = read phase number
176		CONST	
177	016 0500;	LDA	
200	201S1502;	SUB	Prepare to pick up
201	000 5100;	CONST	Nw = write phase number
202	203 1102;	STA	
203	$\boxed{\text{204 0500}}$	LDA	Pick up Nw
204	165 1102;	STA	
205	016 0600;	LDB	With CAM in check sequence
206	000 4500;	CLA	
207	221 2110;	LST	
210	000 0100;	IAC	Save SSS in C
211	212 0637;	LDB	With index for LL
212	233 2110;	LST	16
213	000 0100;	IAC	Merge with SSS
214	227 2210;	RST	10
215	006 1200;	STB	Save for punch out
216	376 0706;	LDP	Save 37606 and 37706
217	220S4400;	CLC	
220	225S1200;	STB	Save B for next random number
221	010 1300;	STD	
222	012 1000;	STC	To reset space counter
223	306 0702;	LDP	Set space punch mode and
224	263 1302;	STD	limit = 5
225	226S0600;	LDB	

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
226	236S3700;	TRU	Exit to store-check sequence
227	000 4500;	CLA	
230	234 2110;	LST	3, to extract one digit
231	006 1200;.	STB	Save rest for later punching
232	000 4300;	CLB	
233	000 4400;	CLC	Copy digit to C
234	235 0000;	MAC	
235	003 5602;	CAM	Is digit = 0?
236	000 4100;	GTB	To check parity
237	000 0100;	IAC	Return original digit to A
240	243 3402;	TCN	Parity odd or even?
241	245 1402;	ADD	Was even, add 1 At 17
242	241 7502;	TOF	Digit was zero, add again
243	251S1402;	ADD	Add into WOC
244	245S4500;	CLA	No error, reset Ce
245	000 0004;	CONST	= 1 at 17
246	247S1100;	STA	In Ce
247	313S3702;	$\boxed{\text{TRU}}$	Punch return
250	256S0500;	LDA	With CAM/STA
251	000 1400;	CONST	WOC skeleton and delay number
252	277 2210;	RST	Put command in B
253	247 0502;	LDA	With punch return
254	376 1306;	STD	
255	251 0402;	LDC	To line 06 for punch-out
256	376S3706;	TRU	
257	260S1402;	ADD	
260	001 0000;	CONST	Increment sector
261	276S1100;	STA	
262	000 6116;	WOC	Carriage return
263	000 0000;	CONST	For punch limit

Table 4-2. (Sheet 7 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
264	000 6116;	WOC	Space or carriage return
265	321S3702;	TRU	Return
266	267S0400;	LDC	With Ce
267	377S77361	CONST	Limit = 8
270	271S0100;	IAC	Save A in C
271	010 0000;	CONST	N = 1, for command mode
272	273S5602;	CAM	
273	000 0042;	CONST	If Ce = 5, no further punching
274	250 7502;	TOF	
275	337 1402;	ADD	Ce ≠ 5, exit to
276	173S0100;	IAC	punch-out sequence
277	301 7502;	TOF	(From 261) overflow if last sector
300	165S0600;	LDB	Not last sector, return to begin
301	302S4500;	CLA	To reset Ce
302	303S1137;	STA	(From 377) restore index
303	304S0437;	LDC	With index
304	004S37001	TRU	Return to begin of command mode
305	307S1100;	STA	In Ce
306	377S77761	CONST	Limit = 5,
307	000 6020;	WOC	Space punch
310	311S4202;	AMC	Extract off line number
311	000 0047;	CONST	From index register
312	331S0300;	ROT	
313	263 0402;	LDC	
314	316 2200;	RSI	Increment digit counter
315	263 1002;	STC	
316	225 3402;	TCN	Return to punch if not through
317	264 0702;	LDP	Word done; punch space or
320	254S3702;	TRU	carriage return and go to 321
321	264 0502;	LDA	With termination character

Table 4-2. (Sheet 8 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
322	262 5602;	CAM	If carriage return, line done
323	360 7502;	TOF	
324	267 0602;	LDB	Line not done, set punch
325	263 1202;	STB	Limit = 8
326	012 0500;	LDA	Test space counter
327	365 3502;	TAN	
330	267 1402;	ADD	
331	012 1100;	STA	Space counter +; make -
332	341S3702;	TRU	
333	334S5600;	CAM	(From 312) compare
334			index with last line
335	357 7502;	TOF	
336	337S1402;	ADD	Not last line, increment
337	000 0040;	CONST	index and return to begin
340	163S1137;	STA	
341	165 0602;	LDB	Since space counter +,
342	165 0402;	LDC	Pick up Nw
343	345 2110;	LST	Extract sign
344	006 1200;	STB	
345	352 3402;	TCN	Check sign of Nw/Nr
346	347S0702;	LDP	
347	000 6036;	[WOC]	Sign positive, punch +
350	225S3702;	[TRU]	
351	254S3702;	TRU	
352	353S0702;	LDP	
353	000 6037;	[WOC]	Sign negative, punch -
354	225S3702;	[TRU]	
355	254S3702;	TRU	
356			
357	360S0400;	LDC	Pick up phase constant

Table 4-2. (Sheet 9 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
360	370S0700;	LDP	(From 323) restore 37606 & 37706
361	137 7711;	TES	Stay in write phase & return if S11
362	363S3702;	TRU	Proceed if $\overline{S11}$
363	141 3402;	TCN	Test phase constant
364	262S3703;	TRU	Exit from memory mode
365	262 0502;	LDA	(From 327) space counter
366	264 1102;	STA	-, prestore C/R punch
367	176 0602;	LDB	
370	176 0402;	LDC	Pick up Nr
371	343S3702;	TRU	
372	376 1306;	STD	Restore 37606 & 37706
373	250S3702;	TRU	
374	011 0500;	LDA	(Command mode) pick up N
375	016 2210;	RST	
376	000 2537;	IAM	N $\rightarrow$ index, save index
377	302S00001	HLT	Halt & display N

Table 4-2. (Sheet 10 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
00003$	000S3702;	TRU	Return to beginning
001	011 1100;	STA	(From 37303)set first block(N = 1)
002	127 0502;	LDA	Prestore first random number
003	006 1100;	STA	
004	005S71001	MCL	Move test to indexed line and transfer there
005	006S37001	TRU	
006	167 0602;	LDB	Generate random number
007	006 0400;	LDC	
010	040 3200;	MUP	
011	006 1200;	STB	
012	010 1100;	STA	
013	011 0500;	LDA	Assemble jump command for transferring to block N
014	15S14001	ADD	
015	051S37001	$\boxed{\text{TRU}}$	
016	020 11001	STA	
017	010 0500;	LDA	Pick up random number
020	$\boxed{\text{251S37001}}$	TRU	Transfer to block N
021	010 5600;	CAM	Transfer to 032 if no error — ERROR SEQUENCE
022	032 75001	TOF	
023	017 7711;	TES	Switch 11: repeat if error; halt & display N if error
024	025S37001	TRU	
025	011 0500;	LDA	Pick up block number
026	047 2210;	RST	
027	031 2537;	IAM	Save index
030	000 00001	HLT	Halt and display N
031	033 2537;	IAM	Restore index
032	011 0500;	LDA	Pick up N
033	034S56001	CAM	Test for maximum N
034	200 0000;	CONST	
035	254 75001	TOF	Transfer to 254 if through

Table 4-2. (Sheet 11 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
036	041 7712;	TES	S12: Do not increment N
037	271 1402;	ADD	$\overline{S12}$: Increment N
040	011 1100;	STA	
041	043 7710;	TES	S10: Halt and display N
042	004S3703;	TRU	$\overline{S10}$: Continue in Sequence
043	374S3702;	TRU	
044	045 0437;	LDC	Pick up index
045	033 4202;	AMC	Extract off line number
046	000 0300;	ROT	
047	012 5600;	CAM	Is this last line?
050	001 7502;	TOF	Transfer to 00102 if last line
051	337 1402;	ADD	Not last line; increment index
052	053 1137;	STA	
053	271 0502;	LDA	Set N = 1
054	011 1100;	STA	
055	041S3703;	TRU	Return to test S10
056	060 7710;	TES	(From 256LL)
057	044S37001	TRU	Halt and display N if S10
060	056S0030;	HLT	

Table 4-2. (Sheet 12 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
254	006 0500;	LDA	(From 035LL) Change original random number
255	127 1102;	STA	
256	056S37001	TRU	
257	253S6000;	WOC	(From 371LL) Flash light and display Input character
260	174 0402;	LDC	
261	256S5100;	RTK	
262	005 0500;	LDA	Change random number and return to scan switches
263	127 1102;	STA	
264	000S3702;	TRU	
265	127 0502;	LDA	Begin punch-read: initialize First random number
266	007 1100;	STA	
267	000 4500;	CLA	Set punch phase
270	010 1100;	STA	
271	104 0602;	LDB	Set limit = 64
272	006 1200;	STB	
273	274S0703;	LDP	To punch leader
274	000 6000;	[WOC]	
275	301S3703;	[TRU]	
276	074 0402;	LDC	With large delay number
277	376 1306;	STD	
300	376S3706;	TRU	Punch 5 inches of leader
301	010 0400;	LDC	Transfer to 31303 if read phase
302	313 3403;	TCN	
303	007 0500;	LDA	Pick up first random number
304	011 1100;	STA	
305	306S0703;	LDP	Punch 8-channel marker and go to 33603
306	000 6737;	[WOC]	
307	336S3703;	[TRU]	
310	311S0403;	LDC	Delay
311	000 2000;	CONST	= +0004000

Table 4-2. (Sheet 13 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
312	277S3703;	TRU	
313	011 0500;	LDA	Initiate read phase
314	007 1100;	STA	
315	316S0503;	LDA	Turn read switch off
316	327S5503;	[LAI]	(To remain off until marker is read)
317	321 1103;	STA	
320	322S4500;	CLA	Enter read sequence
321	364S5503;	LAI	
322	320S5200;	RPT	
323	324 5200;	RPT	Read one frame
324	323 7736;	TES	
325	322 7736;	TES	
326	324S5700;	CIB	
327	000 01771	CONST	LAI mask
330	327 5603;	CAM	Transfer to 33303 when
331	333 7503;	TOF	marker frame is read
332	322S4500;	CLA	Return to read sequence
333	334S0503;	LDA	Marker has been read;
334	364S5503;	[LAI]	Turn read switch on
335	321 1103;	STA	
336	007 0600;	LDB	
337	167 0402;	LDC	Generate next random digit
340	370 3200;	MUP	
341	007 1200;	STB	Save LSH for next number
342	000 0100;	IAC	Extract off eight bits
343	327 4203;	AMC	
344	010 0400;	LDC	Transfer to 36203 if read phase
345	362 3403;	TCN	
346	375 2110;	LST	Assemble into WOC command
347	251 1402;	ADD	

Table 4-2. (Sheet 14 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
350	375 2210;	RST	
351	352S0503;	LDA	Set return address
352	355S3703;	TRU	
353	251 0402;	LDC	With delay
354	277S3703;	TRU	Out to punch digit
355	006 0500;	LDA	Return from digit punchout
356	007 1402;	ADD	
357	006 1100;	STA	Increment frame counter
360	336 3503;	TAN	Return to 33603 if not done
361	270S1000;	STC	Through; restore counter
362	012 1200;	STB	(From 34405) Save random
363	322S4500;	CLA	digit and return to read
364	000 01771	CONST	LAI mask
365	012 5600;	CAM	Enter here after marker frame
366	374 7503;	TOF	read; go to 37403 if no error
367	372 2110;	LST	Error: assemble input character
370	250 1403;	ADD	into WOC command & go to 26003
371	257S1103;	STA	
372	271 0502;	LDA	(From 12402) pick up N = 1
373	001S3703;	TRU	Go to beginning of command mode
374	006 0500;	LDA	Pick up frame counter
375	007 1402;	ADD	Increment
376	006 1100;	STA	Restore counter
377	336 3503;	TAN	Return if not last frame

Table 4-2. (Sheet 15 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
06103	062S0100;	IAC	BLOCK 01
063	064S0200;	IBC	
065	017S0300;	ROT	
07103	010 0400;	LDC	BLOCK 02 Put number in C
072	073S4500;	CLA	Zeros to C
074	075S0100;	IAC	Number to A
076	023 3400I	TCN	If C negative, error
077	020 1400I	ADD	Test ADD and SUB
100	020S1500I	SUB	
10103	074S0100;	IAC	BLOCK 03
075	102S4200I	AMC	Number to C, copy to B
102	-7777777	CONST	
103	132 3200;	MUP	Check MUP, DIV
104	133 3100;	DIV	
105	107 3600I	TBN	If negative, correct quotient
106	017S0300;	ROT	Return to check
107	030 1600I	DPA	DIV correction
110	017S0300;	ROT	Return to check
030	+0000001	CONST	
11103	000 4400;	CLC	BLOCK 04 Copy number to C
112	113 0000;	MAC	
113	114S4200I	AMC	Copy number to B
114	-7776000	CONST	
115	000 0200;	IBC	
116	114 4700I	EXF	Check AMC, EXF, AOC
117	114 4600I	AOC	
120	017S0300;	ROT	Return to check

Table 4-2. (Sheet 16 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
12103	114 06001	LDB	Negative number to B — BLOCK 05
122	124 36001	TBN	
123	023S37001	TRU	If TBN fails, error
124	017 16001	DPA	Check DPA, STD
125	000 1300;	STD	
126	061S4500;	CLA	
062	063S4300;	CLB	
064	066S56001	CAM	Check for zero after CLA
066	+0000000	CONST	
067	127 75001	TOF	
070	023S37001	TRU	Error if TOF fails
127	000 0700;	LDP	Check LDP, DPS
130	017S17001	DPS	
13103	072S4300;	CLB	Zero to C — BLOCK 06
073	131S0200;	IBC	
132	133 0000;	MAC	Copy A to C
133	102 42001	AMC	Copy C to B
134	157 35001	TAN	If A positive then B and C must be also If not, error
135	023 36001	TBN	
136	023 34001	TCN	
137	032S37001	TRU	Continue to next block
157	167 36001	TBN	A was negative, B must be or else error
160	023S37001	TRU	
167	032 34001	TCN	A and B negative, C must be or else error
170	023S37001	TRU	

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
14103	127 0600I	LDB	With 7 at 14 — BLOCK 07
142	004 1200;	STB	Save in F04
143	145 2500;	IAM	Interchange random number & F04
144	114 4000I	EBP	Extend bit 12 to sign bit
145	147 3500I	TAN	A must now be negative,
146	023S3700I	TRU	other wise error
147	004 0500;	LDA	Pick up original number
150	021S3700I	TRU	and return to check
			BLOCK 10
15103	000 4400;	CLC	Set C = 0
152	226 2000;	NAD	Normalize then rescale
153	227 2300;	SAI	(C) should = 0
154	000 0100;	IAC	Number to C, then to F00
155	000 1000;	STC	
156	020S0500;	LDA	Pick up number & return to check
			BLOCK 11
16103	000 4400;	CLC	Set C = 0
162	203 2200;	RSI	Right shift 16 places
163	000 0100;	IAC	(C) should now be +0000020
164	245 5602;	CAM	Check to see if it is
165	032 7500I	TOF	
166	023S3700I	TRU	To error sequence
24502	+0000020	CONST	
			BLOCK 13
20103	000 5300;	RFU	sRf, sTf
202	023 7736;	TES	Should not transfer
203	000 5000;	DIU	rRf, rTf
204	032 7736;	TES	Should now transfer

Table 4-2. (Sheet 18 of 19)

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
17103	177S26001	MLX	BLOCK 12 Move block to 07
177	172S3707;	TRU	
172	010 0400;	LDC	With random number
173	245 0602;	LDB	With 1 at 17
174	223 3200;	MUP	Should shift right 17 places
175	217 2110;	LST	Back 17 places
176	021S37001	TRU	Out to check
21103	200 05001	LDA	BLOCK 14 Constant to A
200	+0222222	CONST	
212	215 3320;	LRS	Parity is even therefore
213	023 35001	TAN	A should be positive
214	000 4100;	GTB	Check GTB
215	216S56001	CAM	
216	-7707070	CONST	
217	022S37001	TRU	
22103	140S2400;	NOP	BLOCK 15 Check NOP and Oc
140	220S2400;	NOP	
220	021S2400;	NOP	
23103	221S4400;	CLC	BLOCK 16 Set C = 0
222	226 3300;	SBR	Should clear A
223	066 56001	CAM	Check for A = 0
224	226 75001	TOF	
225	023S37001	TRU	A not equal to zero; error
226	233 2100;	LSD	See if C decrements; since
227	032 34001	TCN	C was zero, should now be neg.
230	023S37001	TRU	Error exit if C not negative
066	+0000000	CONST	

PROBE I DIAGNOSTIC ROUTINE, PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
24103	245 11001	STA	Put number in 245 — BLOCK 17
242	102 04001	LDC	Put all 1's in F05
243	005 1000;	STC	
244	246S7300;	BSI	If no external buffer, 245 ⟶ F05
245	+0000000	CONST	BSI mask
246	005 0500;	LDA	Pick up BSI'ed word
247	021S37001	TRU	Out to error check
102	-7777777	CONST	
25103	032 35001	TAN	Reject if number neg. — BLOCK 20
252	204S0100;	IAC	Square number
205	010 0600;	LDB	
206	235 3200;	MUP	
207	235 3000;	SQR	Take square root
210	230S1700;	DPS	Subtract original number ⟶A: difference should be no more than 2^{-21}
232	000 0300;	ROT	
233	030 56001	CAM	Check for + 2^{-21}
234	032 75001	TOF	
235	066 56001	CAM	Check for zero
236	032 75001	TOF	
237	102 56001	CAM	Check for - 2^{-21}
240	022S37001	TRU	

Table 4-3.

ABBREVIATIONS USED IN PROBE I FLOW DIAGRAM

RETN	Return
STRT	Start
PR	Punch Read
MEM	Memory
COM	Command
ES	Error Sequence
CAM/STA	Compare A and M/Store A
TOF	Transfer on Overflow
OF	Overflow
BP	Breakpoint
SSS	Three digit symbol to indicate sector number
LL	Two digit symbol to indicate line number

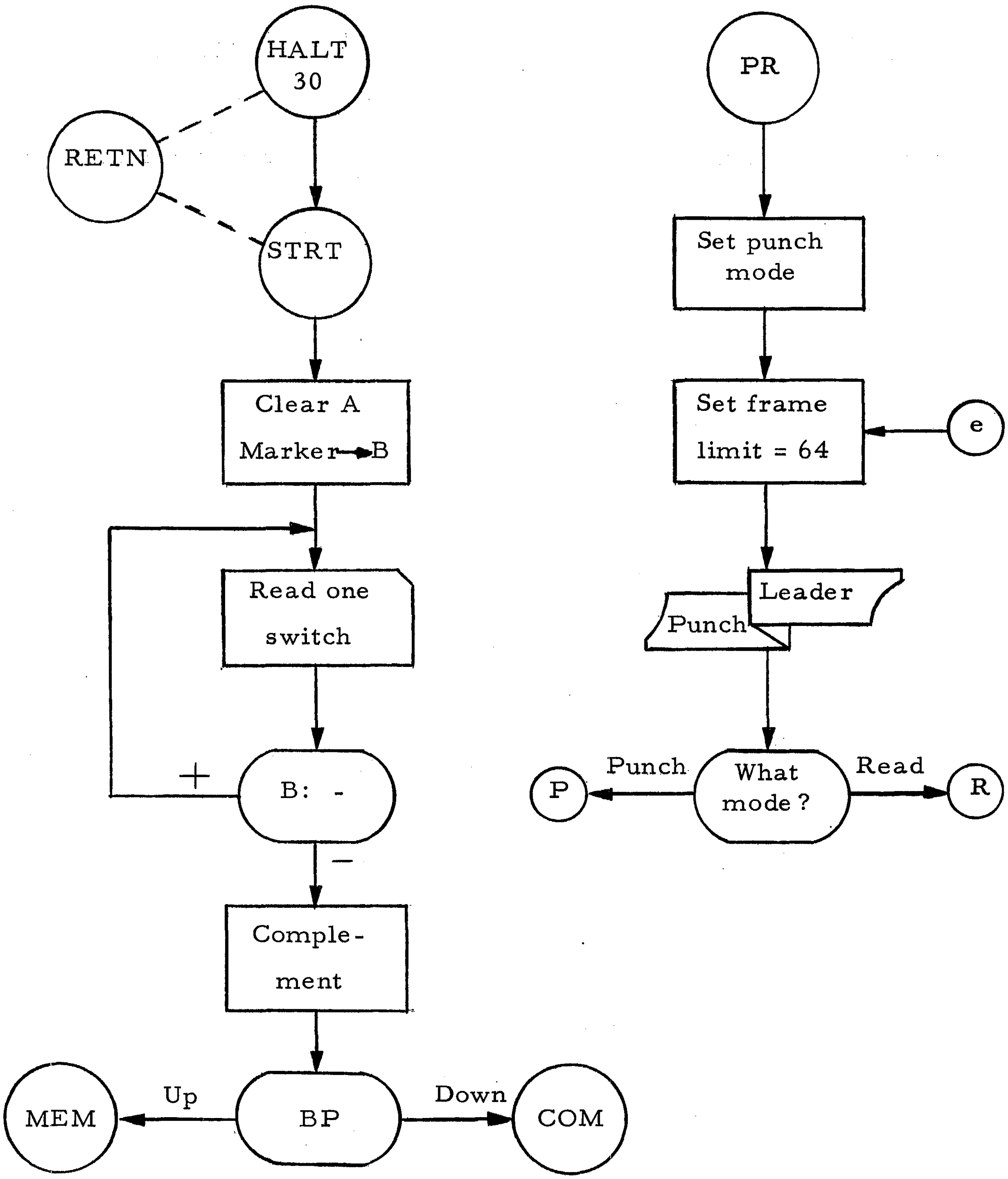


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 1 of 8)

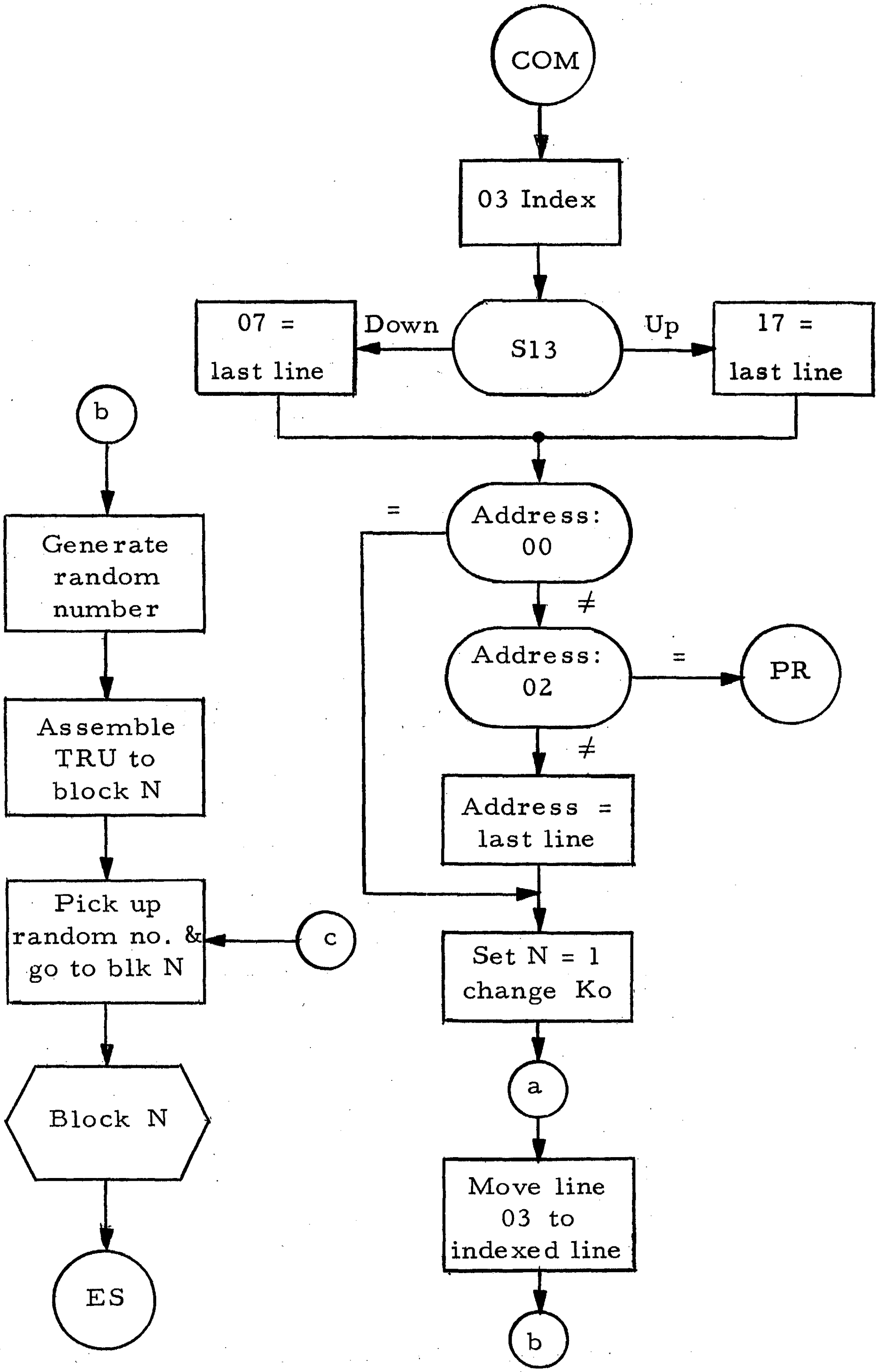


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 2 of 8)

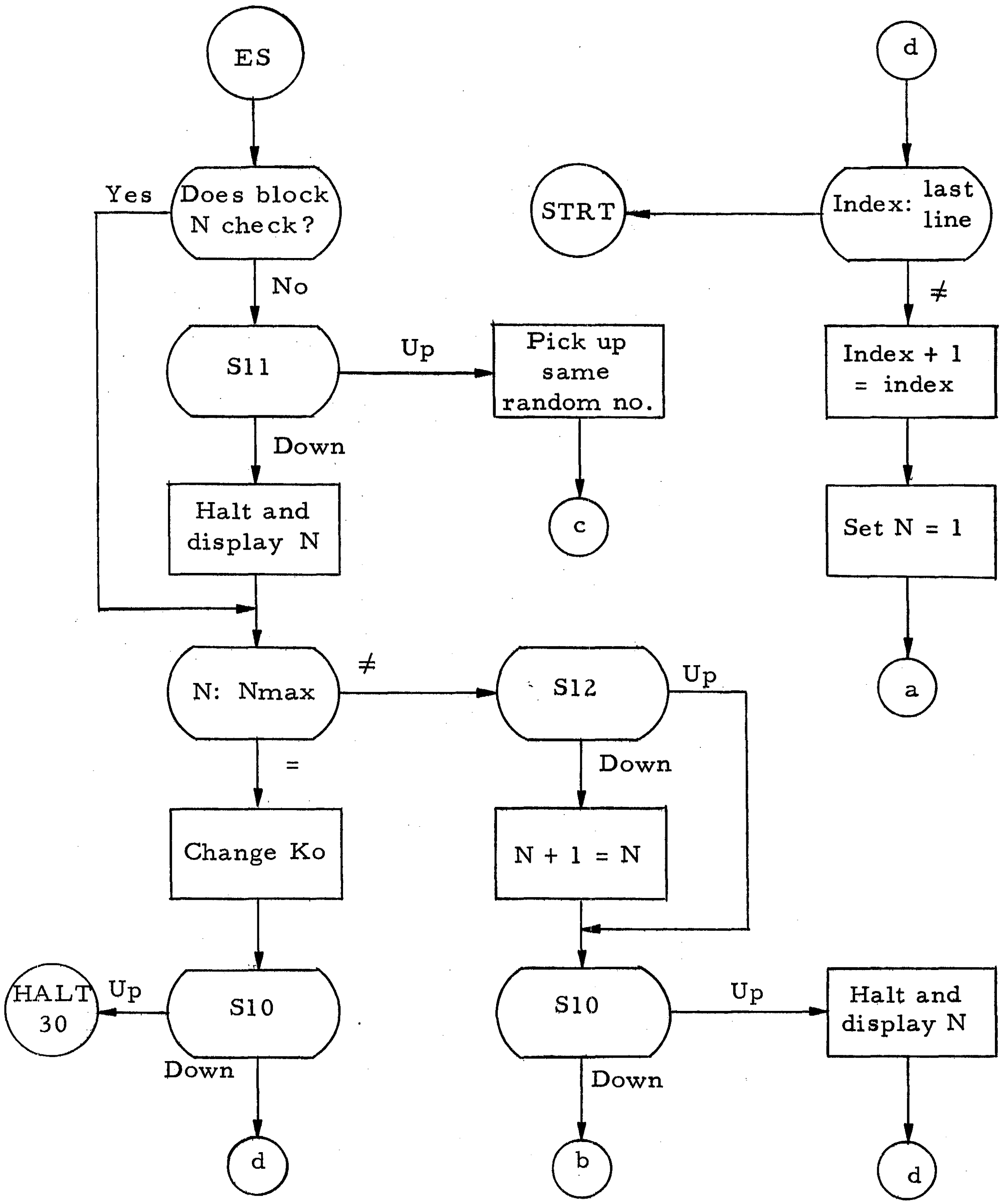


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 3 of 8)

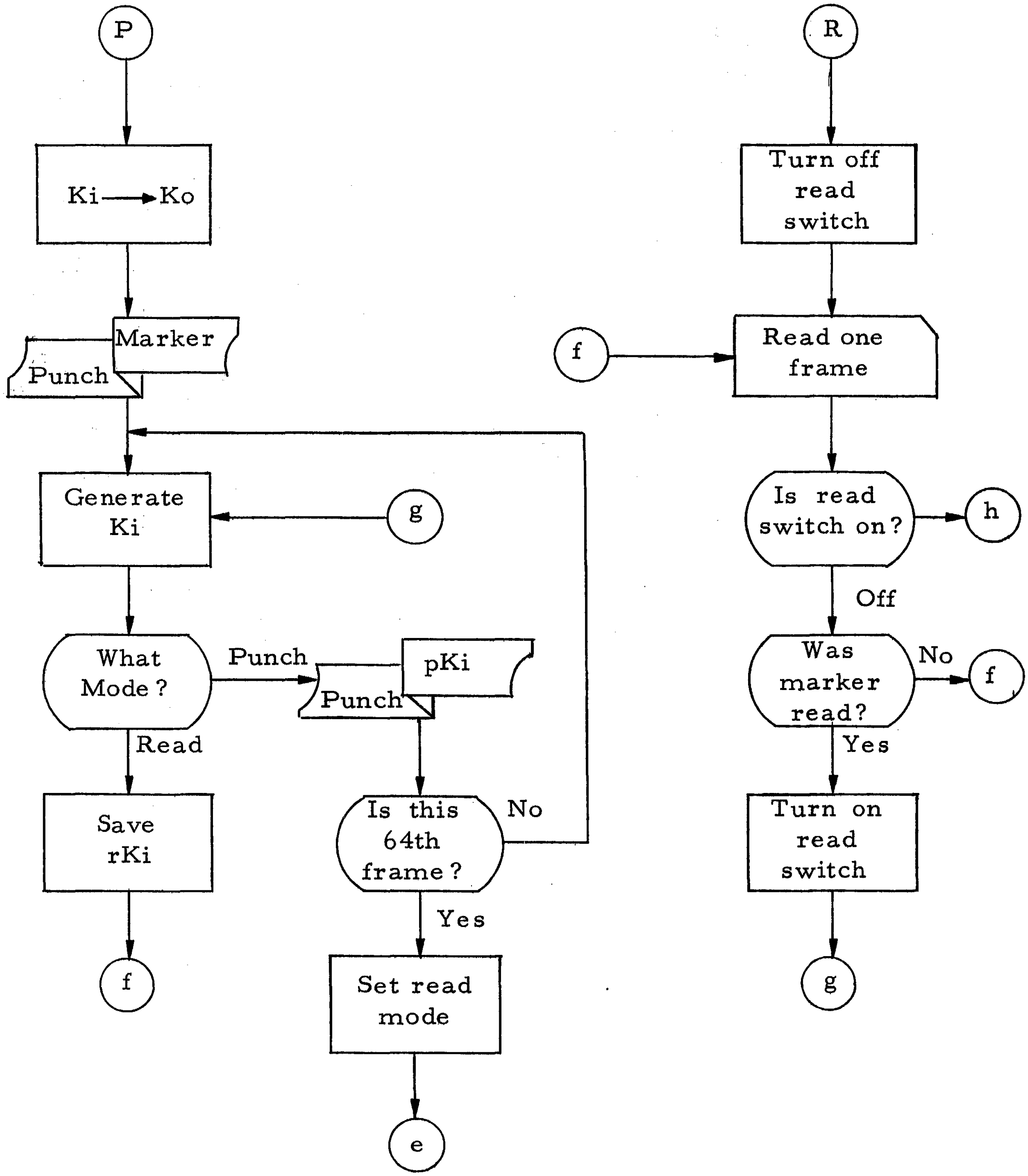


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 4 of 8)

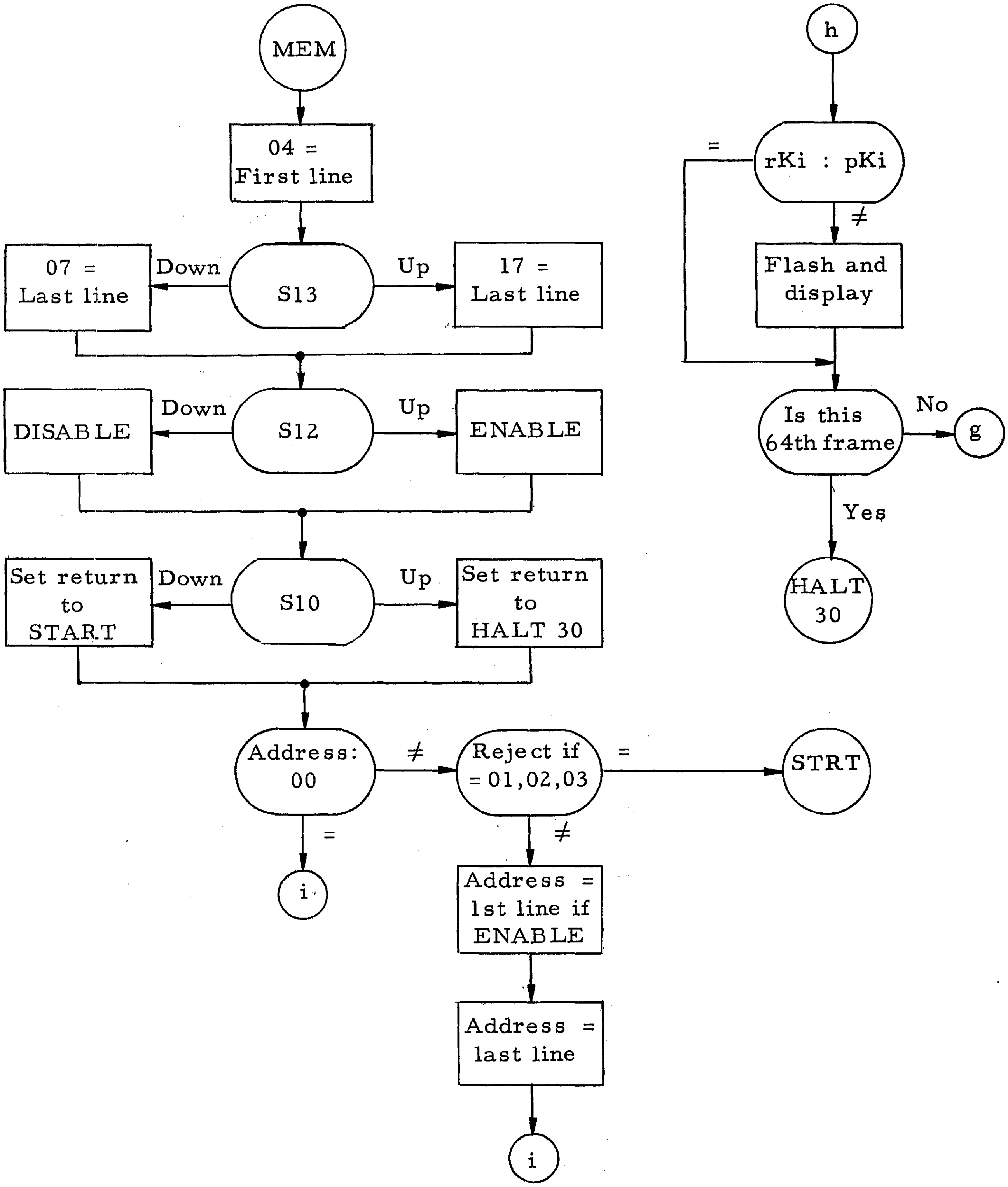


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 5 of 8)

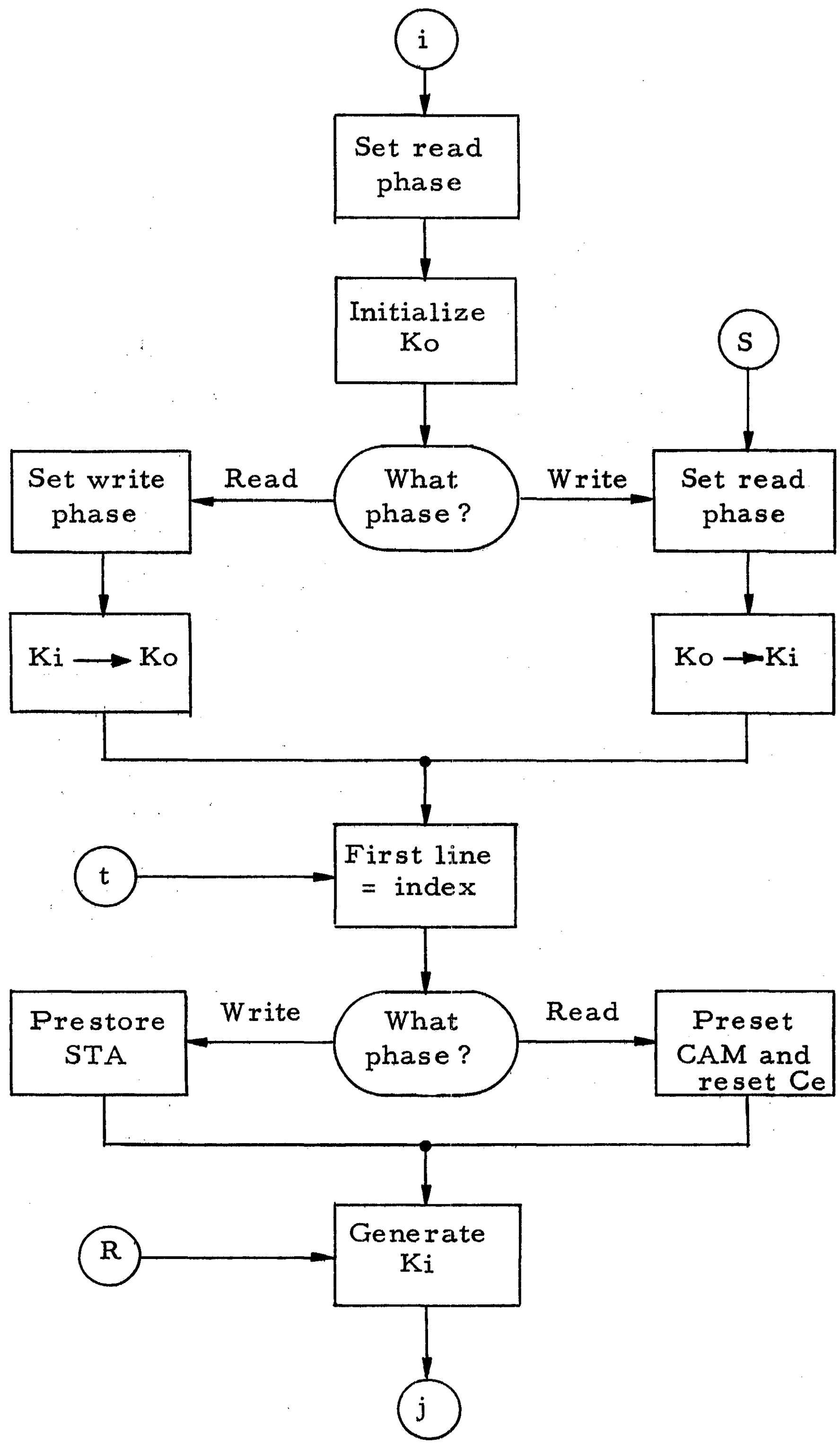


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 6 of 8)

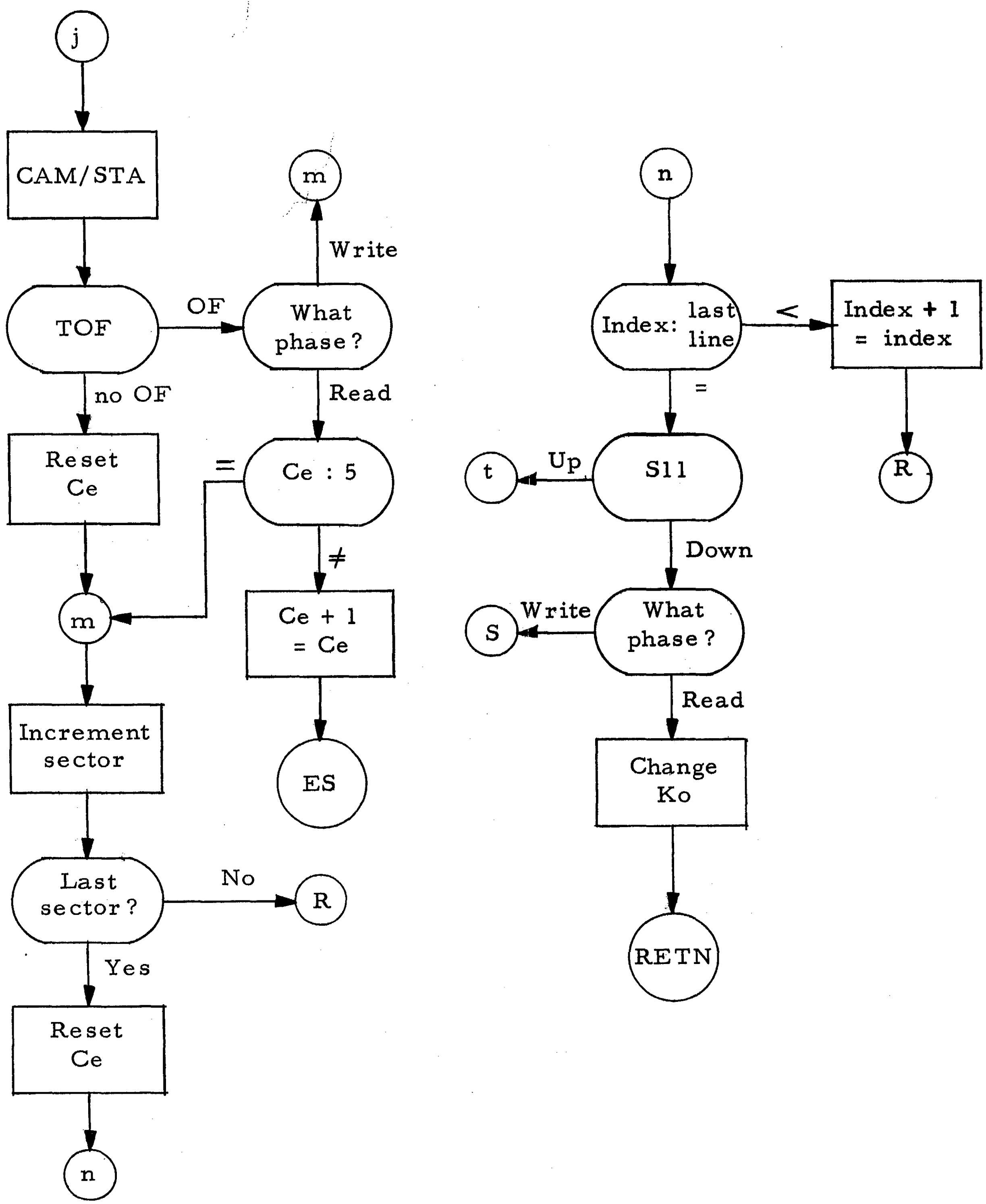


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 7 of 8)

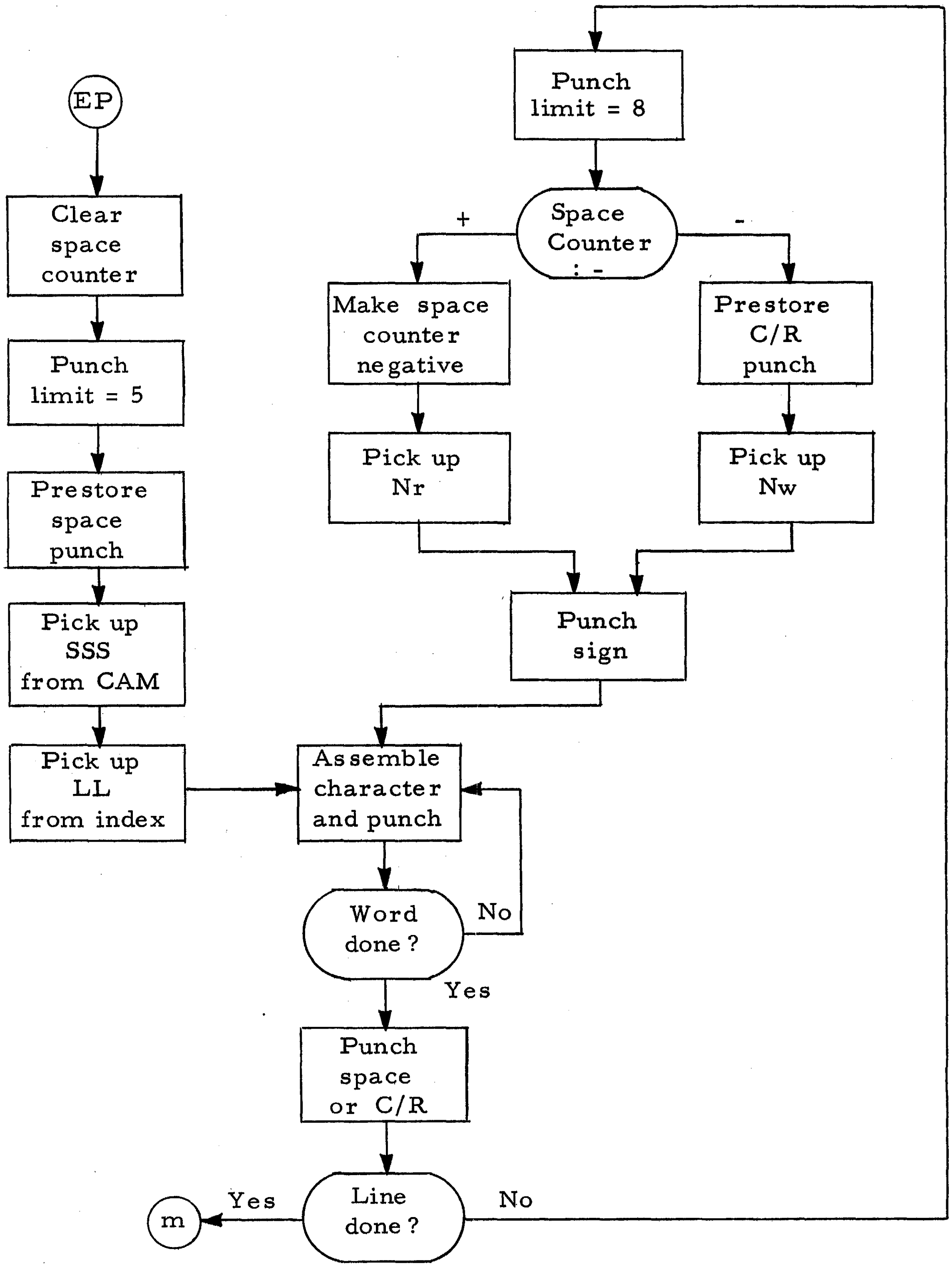


Figure 4-1. Probe I Diagnostic Routine, Flow Diagram (Sheet 8 of 8)

D. BOOTSTRAP DIAGNOSTIC ROUTINES

After the particular failure area has been defined by the PROBE I diagnostic routine, it is desirable to use a bootstrap test routine together with an oscilloscope and the applicable logic diagrams to further identify the marginal components. The applicable bootstrap diagnostic routines are described in this paragraph. These routines are given in listable octal format and their bootstrap serial binary format. Tapes supplied with standard technical literature kits are punched in bootstrap binary format, and punched at the end of each tape is an extra filler bit (zero) and a stop code.

To check the commands, it is necessary to enter simple programs, such as those shown on the following pages, in the basic bootstrap format. The steps for entering a program are as follows:

1) Insert the tape in the reader.

2) Turn computer power on.

3) Turn Flexowriter power on.

4) Turn FILL switch on the front of computer to the ON position.

5) Press ENABLE switch then BREAKPOINT switch to reset the parity flip-flop, then release the BREAKPOINT switch. The computer will now read the tape.

6) When the tape stops, turn the FILL switch to off position.

7) To start computer operation under computer control, press ENABLE switch on Flexowriter to down position.

8) On Flexowriter strike "I" key, then depress BREAKPOINT switch.

9) Release BREAKPOINT switch.

10) Release ENABLE switch. Computer operation will begin.

A command list showing operations, mnemonic and numeric codes, and descriptions is provided in Table 4-4.

Table 4-4.

COMMAND LIST OF OPERATIONS AND CODES

Operation	Mnemonic Code	Numeric Code	Description
Arithmetic	ADD	14	Add
	SUB	15	Subtract
	DPA	16	Double Precision Add
	DPS	17	Double Precision Subtract
	SQR	30	Square Root
	DIV	31	Divide
	DVR	31	Divide Remainder
	MUP	32	Multiply
	CLA	45	Clear A
	CLB	43	Clear B
	CLC	44	Clear C
	GTB	41	Gray to Binary
	CAM	56	Compare A and M
Transfer	TAN	35	Transfer if A Negative
	TBN	36	Transfer if B Negative
	TCN	34	Transfer if C Negative
	TRU	37	Transfer Unconditionally
	TOF	75	Transfer on Overflow
	TES	77	Transfer on External Signal
Loading & Storing	LDA	05	Load A
	LDB	06	Load B
	LDC	04	Load C
	LDP	07	Load Double Precision
	IAC	01	Interchange A & C
	IBC	02	Interchange B & C
	ROT	03	Rotate
	IAM	25	Interchange A & M
	STA	11	Store A
	STB	12	Store B
	STC	10	Store C
	STD	13	Store Double Precision
	MCL	71	Move Command Line Block
	MLX	26	Move Line X to Line 7
Logical & Shifting	EBP	40	Extend Bit Pattern
	AMC	42	AND M & C
	MAC	00	Merge A into C
	AOC	46	AND OR Combined
	EXF	47	Extract Field
	NAD	20	Normalize and Decrement
	LSD	21	Left Shift and Decrement
	RSI	22	Right Shift and Increment
	SAI	23	Scale Right and Increment
	SBR	33	Shift B Right
Control	NOP	24	No Operation
	HLT	00	Halt
Input-Output	DIU	50	Disconnect Input Unit
	RTK	51	Read Typewriter Keyboard
	RPT	52	Read Paper Tape
	RFU	53	Read Fast Unit
	LAI	55	Load A From Input Buffer
	CIB	57	Clear Input Buffer
	WOC	6X	Write Output Character
	PTU	70	Pulse to Specified Unit
	BSO	72	Block Serial Output
	BSI	73	Block Serial Input

D-1. LOAD, STORE AND CLEAR REGISTERS

The A, B, and C Registers are successively loaded, stored and cleared. Each is loaded with a different pattern of bits. The A Register is stored in sector 006, the B in 010 and the C in 012.

Location	Instruction	Symbolic Op Code	Remarks
377	000S0501;	LDA	
0	012S4552;	[CLA]	(A) 100001010110010101010 10
1	002S0601;	LDB	
2	+6314631		(B) 101100110011001100110 01
3	004S0401;	LDC	
4	+3434343		(C) 100111000111000111000 11
5	006S1101;	STA	
6	-7777777		
7	010S1201;	STB	
10	+0000000		
11	012S1001;	STC	
12	-7777777		
13	014S4500;	CLA	
14	+0000000		
15	016S4300;	CLB	
16	+0000000		
17	376S4400;	CLC	

D-2. LOAD AND STORE DOUBLE PRECISION

The A and B Registers are first loaded double precision and then stored.

Location	Instruction	Symbolic Op Code	Remarks
377	+0000000		
0	001S0701;	LDP	
1	-2525252		
2	+6314631		
3	376S1301;	STD	

D-3. INTERCHANGES

The A, B, and C Registers are loaded and then interchanged, first with a ROT, then with an IAC and IBC. The net result of these is that after one complete memory recirculation, each register should contain its original pattern.

Location	Instruction	Symbolic Op Code	Remarks
377	000S0100;	IAC	
0	002S0701;	LDP	
1	005S0200;	IBC	
2	-2525252	CONST	(A) 110101010101010101010101
3	+6314631	CONST	(B) 101100110011001100110011
4	005S0401;	LDC	
5	+3434343	CONST	(C) 100111000111000111000111
6	375S0300;	ROT	

D-4. ADD AND SUBTRACT IN SINGLE AND DOUBLE PRECISION

The A and B Registers are first loaded with constants. A constant is added to A. A double precision constant is added to A and B, and another constant subtracted from A and B. Finally, a constant is subtracted from A alone and the cycle repeats.

Location	Instruction	Symbolic Op Code	Remarks
377	+1010102	D_4	
0	001S0701;	LDP	D_0
1	-5454540	D_0	
2	+4646460	D_0'	
3	004S1401;	ADD	D_1
4	+0202022	D_1	
5	006S1601;	DPA	D_2
6	-0404042	D_2	
7	+1010100	D_2'	
10	011S1701;	DPS	D_3
11	-1414141	D_3	
12	+1414140	D_3'	
13	377S1501;	SUB	D_4

This chart shows contents of A and B Registers after each of the five operations.

D-4

	S	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
LDP	1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	1	1	0	0	0	0	0	(B) D_0
	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	0	0	0	(A) D_0'
ADD	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	D_1
	1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	1	1	0	0	0	0	0	(B)
	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	0	(A)
DPA	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	D_2
	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	D_2'
	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	(B)
	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	(A)
DPS	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	D_3
	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	D_3'
	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	(B)
	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0	(A)
SUB	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	D_4
	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	(B)
	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	(A)

D-5. TRANSFERS

The C Register is loaded with a negative number and the A Register is cleared. A negative constant is added to A and the sign of C tested. Since it is negative, a transfer is made to a TES Breakpoint which, if on, will transfer back to the CLA and start again. If the Breakpoint is off, the overflow is tested, and since it is now off, the negative constant is again added to A. The program cycles in this loop with a TCN (34) command displayed on the console until A overflows and goes positive.

The TOF will cause a transfer to a ROT which moves the negative constant to B and the positive constant to C. The program starts again with the CLA and ADD except that this time the C Register is positive so control passes through the TCN to a TBN (36) which will appear on the console until A overflows.

When A overflows this time, the positive constant from C is rotated to B and the constant from A to C. The CLA and ADD begin again, and now control passes through both the TCN and TBN to a TAN which appears as a 35 on the console. This time, control does not pass through the TES or TOF before adding, so when A overflows and becomes positive, the TAN does not transfer; instead, a TRU carries control back to the start of the routine in sector 000.

D-5

Location	Instruction	Symbolic Op Code	Remarks
377	000S0300;	ROT	002
0	001S0401;	LDC	-N
1	-2525252	-N	
2	004S4500;	CLA	005
3	002 7735;	TES	B.P. 002
4	377 7501;	TOF	377
5	066S1401;	ADD	
6	-7770000	-77	
7	003 3401;	TCU	003
10	003 3601;	TBN	003
11	005 3501;	TAN	005
12	000S3701;	TRU	000

D-6. LOGICAL COMMANDS

The A Register is loaded with a constant which is modified by an EBP command and then moved to C. From C, part of the pattern is modified and moved to B with an AMC. Additional bits from C are moved to B with an AOC. The result in B is partially cleared with an EXF command and the process begins again in A.

Location	Instruction	Symbolic Op Code	Remarks
377	-6564040	S	
0	001S0501;	LDA	N
1	-0202026	N	
2	003S4001;	EBP	M
3	-1414146	M	
4	005S0100;	IAC	
5	+0000000		
6	007S4201;	AMC	Q
7	+1414147	Q	
10	011S4601;	AOC	R
11	+0706077	R	
12	377S4701;	EXF	S

This chart shows the contents of the A and B Registers after each of the five operations.

D-6

	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
LDA	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	N
	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	(A)
EBP	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	M
	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(A)
IAC	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(C)
AMC	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1	Q
	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	(B)
AOC	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	R
	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	(B)
EXF	1	1	1	0	1	0	1	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	S
	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	(B)

D-7. SHIFTING (UNCONDITIONAL)

The A and C Registers are cleared and B is loaded with a pattern of bits. If the Breakpoint is up, a left shift and decrement is executed for two sectors and the sign of B tested. The B Register will be negative so control goes back to the TES Breakpoint and another shift is executed. This continues until B is positive, and then a right shift and increment moves the pattern two bit positions into B. This should make B negative, so control will go back to the right shift until a zero is shifted into the sign of B. When B is positive, control goes back to the left shift. If the Breakpoint is down the shifts will be without incrementing or decrementing C and will only execute for one sector.

Location	Instruction	Symbolic Op Code	Remarks
377	004S0601;	LDB	-B 005
0	010S4500;	CLA	011
1	003 7735;	TES	B.P.
2	005S2100;	LSD	2
3	005S2110;	LSO	1
4	-7355143	-B	-B
5	001 3601;	TBN	
6	010 7735;	TES	B.P.
7	012S2200;	RSI	2
10	012S2210;	RSO	1
11	376S4400;	CLC	377
12	006 3601;	TBN	
13	001S3701;	TRU	001 0

D-8 SHIFTING (CONDITIONAL)

This routine operates similar to D-7 in that it shifts back and forth from A and B. First, a negative number is loaded into B, and A and C are cleared. A normalize and decrement of three is executed and the sign of B tested, if negative, another NAD is executed. Going in steps of three, it will take seven full shifts plus a one-bit shift to normalize the number. In this way, both the normal shifting feature plus the conditional terminating feature of the NAD are tested. The B Register should be positive when the number is normalized.

During normalization, the C Register will have been decremented to the negative of the number of normalizing shifts required. It should be possible by now, executing scale right and increment commands in steps of three, to move the number back to its original condition with A and C equal to zero.

When C is scaled to zero, control will go back to the NAD loop. If the BREAKPOINT is pressed, computation will hang up in a TES loop after either normalizing or scaling.

D-8

Location	Instruction	Symbolic Op Code	Remarks
377	003S2000;	NAD	003
0	000S4500;	CLA	001
1	011S0601;	LDB	-N 012
2	006S2300;	SRI	006
3	377 3601;	TBN	377
4	004 7735;	TES	B. P. 004
5	022S3701;	TRU	
6	002 3601;	TBN	
7	007 7735;	TES	B. P. 007
10	377S3701;	TRU	377
11	-7153514	-N	-N
12	376S4400;	CLC	377

D-9. CAM AND GTB

A number is loaded in A and compared with itself. If overflow occurs, the number is converted from Gray code to binary and compared to the correct result. If overflow occurs, control goes to a Breakpoint test. If Breakpoint is up, the routine starts again; if Breakpoint is down, the binary number is compared with the original number and overflow should not occur.

When comparing the converted number with the correct result, if overflow does not occur the sign of A is tested, and if negative, a transfer is made to 000 with a TAN (35). if not negative, the transfer will be a TBN (36).

Location	Instruction	Symbolic Op Code	Remarks
377	002 7735;	TES	B. P. 002
0	001S0501;	LDA	N_G
1	+5252525	N_G	N_G
2	003S5601;	CAM	N_G
3	+5252525	N_G	N_G
4	006 7501;	TOF	
5	002S3701;	TRU	002
6	007S4100;	GTB	
7	+0000000		
10	011S5601;	CAM	N_B
11	-1463146	N_B	N_B
12	377 7501;	TOF	377
13	000 3501;	TAN	000
14	000S3601;	TBN	000 S

D-10. TO TEST INDEX REGISTER, HLT, MAC, AND NOP

The A and C Registers are cleared and A stored in the Index Register. A and C are OR gated into C and computation halts, displaying the contents of the Index Register in the OPERAND lights. When parity is cleared, a NOP is executed and the contents of the Index Register picked up, incremented by one and restored. Then another MAC and halt are executed.

This process continues each time the parity is cleared. The Ar will show a count, and the Cr a buildup from the right.

Location	Instruction	Symbolic Op Code	Remarks
377	000S1401;	ADD	001
0	001S4540;	CLA	002
1	002S1137;	STA	I. R. 003
2	000S4400I	CLC	001
3	004S0000I	MAC	005
4	006S2400I	NOP	006
5	004S0000I	HLT	004
6	376S0537;	LDA	I. R. 377

D-11. MOVE LINE AND IAM

The Index Register is cleared to zero and line 01 is moved to 00. Then the Index Register is incremented by one and another MCL is executed. This continues through line 36, and then the MCL is changed to a MLX by means of an IAM. Using the Index Register, each line from 00 through 36 is moved to line 07 and the routine then repeats.

If the Breakpoint is down, the program halts after each move and displays the line moved.

Location	Instruction	Symbolic Op Code	Remarks	
377	000S0100;	IAC		
000	002S0501;	LDA	X	
1	004S1401;	ADD	N	
2	010S7100I	X	(MCL) I	
3	005S4400;	CLC		
4	+0200002	N	N	+.020 0002
5	006S0100;	IAC		
6	010S2501;	IAM		
7	010S2600I	MLX	I	
010	003 7501;	TOF		
1	013 7735;	TES	35	
2	376S1037;	STC	37	377
3	012S0000I	HLT		

D-12. MULTIPLY, DIVIDE AND SQUARE ROOT

This routine executes in line 00, therefore it is not possible to single step and always obtain the correct answer. However, all pertinent operations occur in the first $073)_8$ sector times.

The same number is loaded into the B and C Registers and garbage into A. A multiply for 22-word times is executed, and the result in A compared to the correct result. The overflow is not tested, but it may be observed on the console. After the multiply, if the Breakpoint is up, a divide for 22-word times is executed and the remainder in A compared with +0000000. If the Breakpoint is down, a square root for 21-word times is executed and the remainder in A compared to +0000000. When executing the divide, the comparison is true and the overflow occurs. The square root has a remainder of $-7777777)_8$ and will not compare.

By observing sector time $073)_8$, the results of both the divide and square root may be seen.

Location	Instruction	Symbolic Op Code	Remarks
377	+5252525	X_B	X_B
0	014S7100;	X_A	MCL
1	030S3200;	MUL	S = 22 030
2	+3434343	Y_1	Y_1
3	045 7735;	TES	B.P. 045
4	073S3100;	DIV	S = 22 073 R: (A) = +0000000
5	073S3000;	SQR	S = 21 073 R: (A) = -7777777
6	+0000000	Y_2	Y_2
7	111S0400;	LDC	X_C
010	042S5600;	CAM	Y_1 043
1	+5252525	X_C	X_C
2	377S0701;	LDP	$X_{A \& B}$ 001
3	106S5600;	CAM	Y_2 107
4	107S7500;	TOF	

D-13. RTK, RPT, LAI, WOC AND CIB

After pressing the "I" key and raising the ENABLE switch, the Flexowriter light will come on and a character may be typed. This character will be loaded into the A Register, added to a WOC, and the WOC used to display it on the console for about two seconds. After the WOC, a HLT with a line number of $13)_8$ will occur.

When parity is cleared, another character may be entered. The character will come from the tape reader if the Breakpoint is down, and from the keyboard if the Breakpoint is up.

Location	Instruction	Symbolic Op Code	Remarks
377	010 0013;	D	HLT
000	000S4500;	CLA	
1	001S5700;	CIB	
2	004 7735;	TES	B. P.
3	006S5100;	RTK	
4	006S5200;	RPT	
5	+0000377	M	M
6	010 7736;	TES	36
7	005S5501;	LAI	M
010	010S4300;	CLB	
1	014 2110;	LSO	2
2	013S1401;	ADD	
3	377S6000;	WOC	0 377
4	377 0401;	LDC	D
5	016 1101;	STA	$ + 1

D-14. FLEXOWRITER TYPING AND PUNCHING.

Both lines 05 and 06 must be present for this test. Every possible character from 000 through $377)_8$ will be typed, then punched. Some of these are not valid keyboard characters and will not print, but all should be punched.

Location	Instruction	Symbolic Op Code	Remarks
377	001S3706;	TRU	06
0	017S7106;	MCL	06 017 moves 00101 → 01601 to 00106 - 01606 next command 01701
1	002S0406;	LDC	D_2
2	+0002424	D_2	D_2
3	000 6000;	WOC	000
4	005S1406;	ADD	C
5	+0000004	C	C
6	007S5606;	CAM	E
7	000 7000;	E	E
010	000 7501;	TOF	I
1	003 1106;	STA	06
2	376 1105;	STA	05
3	014S0406;	LDC	D_1
4	+0003232	D_1	D_1
5	015 7737;	TES	37
6	376S3705;	TRU	05 376
7	003 0501;	LDA	WOC 0
020	012S7105	MCL	05 012 thru 01101 → line 5 go to 01201

D-15. DIV, RFU AND RfTf TEST

A DIV is given, followed by a TES $36)_8$ which sould be true. Then an RFU and a TES $36)_8$ which should now be false. If the TES $36)_8$ is false, after the DIV, a halt will occur with 50-37 displayed. This means that the RFU did not set either Rf or Tf. When the program runs correctly, a 53-00 is displayed.

Location	Instruction	Symbolic Op Code	Remarks
377	001 7736;	TES	36
000	001S5000;	DIU	
1	376S5336;	RFU	ERROR HLT
2	004 7736;	TES	36
3	001S5036;	DIU	ERROR HLT
4	376S5300;	RFU	

D-16. PTU

Two PTU's are executed, each for approximately 3 ms. One has a line number of $37)_8$, the other 00.

Location	Instruction	Symbolic Op Code	Remarks
377	000S7037;	PTU	37
0	377S7000;	PTU	0

D-17. BSO, BSI

After pressing the "I" key, a BSO from line 01 is executed for 3 ms, and as long as the Breakpoint is up, Block Serial Inputs will continue. If the Breakpoint is down, after the first BSO, then BSI's will be executed until it is raised.

Location	Instruction	Symbolic Op Code	Remarks
377	001 7735;	TES	35
0	377S7201;	BSO	
1	377S7301;	BSI	

D-18. FLEXOWRITER FORMAT

If the tapes which are punched in bootstrap binary format are reproduced on a Flexowriter they will appear in serial binary Flexowriter format as shown in Figure 4-2. The type-outs D-1 through D-17 relate directly to paragraphs D-1 through D-17. In this format, H = binary one and 0 = binary zero.

D-1

OHHHHHHHOHHOOHOOOOOOOOO
OOOOOOOOOOOOOOOOOOOOOOO
HOOOOHHHOHHOOOHHOOOOOOO
OOOOOOOOOOOOOOOOOOOOOOO
OOOOOHHOOHHOOHOHOOOOOOO
OHHHHHHHHHHHHHHHHHHHHHH
HOOOOHOHOHOOHOOOOOOOHOO
OOOOOOOOOOOOOOOOOOOOOOO
HOOOOHOOOHOOHOHOOOOOHOO
OHHHHHHHHHHHHHHHHHHHHHH
OOOOOOHHOHOOHOOHOOOOHOO
HOOHHHOOOHHHOOOHHHOOOHH
OOOOOOHOOHOOOHOOOOOOHOO
HOHHOOHHOOHHOOHHOOHHOOH
HOOOOOOHOHOOOHHOOOOOHOO
HOOOOHOHOHHOOHOHOHOHOHO
OOOOOOOOOHOOOHOHOOOOHOO
O

D-2

OHHHHHHHOHOOHOHHOOOOHOO
HOHHOOHHOOHHOOHHOOHHOOH
HHOHOHOHOHOHOHOHOHOHOHO
OOOOOOOOHHOOOHHHOOOOHOO
OOOOOOOOOOOOOOOOOOOOOOO
O

D-3

OHHHHHHOHHOOOOHHOOOOOOO
OHOHHHOOOHHHOOOHHHOOOHH
HOOOOOHOHHOOOHOOOOOOHOO
HOHHOOHHOOHHOOHHOOHHOOH
HHOHOHOHOHOHOHOHOHOHOHO
OOOOOOHOHHOOOOHOOOOOOOO
OOOOOOOHOHOOOHHOOOOHOO
OOOOOOOOOHOOOOOHOOOOOOO
O

D-4

HHHHHHHHHHOOHHOHOOOOHOO
OOOOHHOOOOHHOOOOHHOOOOO
OHOOHHOOOOHHOOOOHHOOOOH
OOOOOHOOHHOOHHHOOOOHOO
HOOOHOOOOOHOOOOOHOOOOOO
HHOOOHOOOOOHOOOOOHOOOHO
HOOOOOHHOHOOHHHOOOOOHOO
OOOOOOHOOOOOHOOOOOHOOHO
HOOOOOHOOHOOHHOOOOOOHOO
HOHOOHHOHOOHHOHOOHHOOOO
OHHOHHOOHOHHOOHOHHOOOOO
OOOOOOOOHHOOOHHHOOOOHOO
OOOOHOOOOOHOOOOOHOOOOHO
O

D-5

HOOOOOOOOHOHHHHHOOOOHOO
HOOOOOHOHOOHHHOHOOOOHOO
HOOOOOOHHOOHHHHOOOOOHOO
OOOOOOOHHOOHHHOOOOOOHOO
OHHHHHHHHHHOOOOOOOOOOOO
OOOOOOHHOHOOHHOOOOOOHOO
OHHHHHHHHOHHHHOHOOOOHOO
HOOOOOOHOOHHHHHHHHHOHOO
HOOOOOHOOHHOOHOHOOOOOOO
HHOHOHOHOHOHOHOHOHOHOHO
OOOOOOOOHHOOOHOOOOOOHOO
HOOOOOOOOHOOOOHHOOOOOOO
O

D-6

OHHHHHHHHHHOOHHHOOOOHOO
HOOOOHHHOOOHHOOOOHHHHHH
HOOOOHOOHHHOOHHOOOOOHOO
HOOOHHOOOOHHOOOOHHOOHHH
HOOOOOHHHHHOOOHOOOOOHOO
OOOOOOOOOOOOOOOOOOOOOOO
OOOOOOHOHHOOOOOHOOOOOOO
HHOOHHOOOOHHOOOOHHOOHHO
HOOOOOOHHHHOOOOOOOOOHOO
OHOOOOHOOOOOHOOOOOHOHHO
HOOOOOOOHHOOOHOHOOOOHOO
HHHHOHOHHHOHOOOOOHOOOOO
O

D-7

OOOOOOOOHHOHHHHHOOOOHOO
HOOOOOHHOOOHHHHOOOOOHOO
OHHHHHHOHHOOHOOOOOOOOOO
OOOOOHOHOHOHOOHOOHOOOOOO
HOOOOHOHOHOHOOHOOOOOOOO
HOOOOHOOOOHHHHHHHHHOHOO
OOOOOOOOHOOHHHHOOOOOHOO
OHHHOHHHOHHOHOOHHOOOHH
OOOOOOHOHHOHOOOHOHOOOOO
HOOOOOHOHHOHOOOHOOOOOOO
OOOOOOOHHOHHHHHHHHHOHOO
HOOOOHOOOHHOOHOHOOOOOOO
HOOOOOHOOHOOOHHOOOOOHOO
O

D-8

OHHHHHHHOHHOOHOOOOOOOOO
HHHHHOOHHOHOHHHOHOOHHOO
HHHHHHHHHHOHHHHHOOOOHOO
HOOOOOHHHOHHHHHHHHHOHOO
HOOOOOOHOOOHHHOOOOOOHOO
OOOOOOOHOHOHHHHHOOOOHOO
HOOOOOHOOOHHHHHHHHHOHOO
HHHHHHHHHOOHHHHOOOOOHOO
OOOOOOHHOHOHOOHHOOOOOOO
OOOOOHOOHHOOOHHOOOOOHOO
OOOOOOOOOHHOOHOHOOOOOOO
OOOOOOOHHHOHOOOOOOOOOOO
O

D-9

OOOOOOOOOHOHHHHOOOOOHOO
HOOOOOOOOOOHHHOHOOOOHOO
OHHHHHHHHOHHHHOHOOOOHOO
HHOOHHOOHHOOHHOOHHOOHHO
OOOOOHOOHHHOHHHOOOOOHOO
OOOOOOOOOOOOOOOOOOOOOOO
OOOOOOHHHHHOOOOHOOOOOOO
OOOOOOOHOHOHHHHHOOOOHOO
OOOOOOHHOOHHHHOHOOOOHOO
HOHOHOHOHOHOHOHOHOHOHOH
OOOOOOOHHHHOHHHOOOOOHOO
HOHOHOHOHOHOHOHOHOHOHOH
HOOOOOOOHHOOOHOHOOOOHOO
HOOOOOOHOOHHHHHHHHHOHOO
O

D-10

HHHHHHHHOHOOOHOHHHHHHOO
HOOOOOHOOHOOOOOOOOOOOOH
OOOOOOHHOHOHOHOOOOOOOOH
HOOOOOHOOHOOOOOOOOOOOOH
OOOOOOOOOHHOOHOOOOOOOOH
HOOOOOOHOHOOHOOHHHHHHOO
OOOOOOOOHHHOOHOHOOOOOHO
OOOOOOOOOHOOHHOOOOOOHOO
O

D-11

OOOOOHOHOHOOOOOOOOOOOOH
OHHHHHHHOHOOHOOOHHHHHOO
HOOOHOHHOHHHHHHHHHHOHOO
OOOOOOOHHOHHHHOHOOOOHOO
OOOOOHOOOHOHOHHOOOOOOOH
OOOOOHOOOHOHOHOHOOOOHOO
OOOOOOHHOHOOOOOHOOOOOOO
OOOOOOHOOOOOOOOOOOOOOHO
HOOOOOHOHHHOOHOOOOOOOOO
HOOOHOOOHHHHOOHOOOOOOH
HOOOOOHOOHOOHHOOOOOOHOO
HOOOOOOHOHOOOHOHOOOOHOO
OOOOOOOOOHOOOOOHOOOOOOO
O

D-12

OOHOOOHHHHHHHHOHOOOOOOO
OOHOOOHHOHHOHHHOOOOOOOO
HHHHHHHHHHOOOHHHOOOOHOO
HOHOHOHOHOHOHOHOHOHOHOH
HOOHOOOHOHHOHHHOOOOOOOO
HOHOOHOOHHOOOHOOOOOOOOO
OOOOOOOOOOOOOOOOOOOOOOO
OOOHHOHHHOHHOOOOOOOOOOO
HOOHHHOHHHOHHOOHOOOOOOO
HOOHOOHOHOHHHHHHHHHOHOO
HOOHHHOOOHHHOOOHHHOOOHH
OOOOHHOOOHOHHOHOOOOOOOO
HOOOOHHOOHHHOOHOOOOOOOO
HOHOHOHOHOHOHOHOHOHOHOH
O

D-13

OOOOOHHHOOOOHOOHOOOOHOO
OHHHHHHHHOOOOHOOOOOOHOO
HHHHHHHHHHHHOOOOOOOOOOO
HOOOOHOHHOOHHOOOOOOHOO
HOOOOHHOOOOHOOOHOHOOOOO
HOOOOHOOOHHOOOHHOOOOOOO
OOOOOOHOHHOHHOHOOOOHOO
HOOOOHOOOOHHHHHHHHHHOOO
OOOOOOOOOOOOOOOOHHHHHHH
OOOOOOHHOHHOHOHOOOOOOOO
OOOOOOHHOHHOHOOHOOOOOOO
HOOOOOHOOOHHHHHHHHHOHOO
HOOOOOOOHHOHHHHOOOOOOO
OOOOOOOOOHHOOHOHOOOOOOO
OOOOOHOOOOOOOOOOOHOHHOO
O

D-14

HOOOOHOHOHHHHOOHOOHOHOO
HOOOOOOHHOOOOHOHOOOOHOO
HHHHHHHHOHOHHHHHOOHOHOO
OOOOOHHOHOHHHHHHHHHHHOO
OOOOOOOOOOOOHHOHOOHHOHO
OOOOOHHOOHOOOHOOOOHHOOO
HHHHHHHHOOOOHOOHOOHOHOO
OOOOOOOHHOOOHOOHOOHHOOO
OOOOOOOOOOHHHHOHOOOOHOO
HOOOOOOOOOHHHOOOOOOOOOO
OOOOOOHHHHHOHHHOOOHHOOO
HOOOOOOOOOOOOOOOOOOOHOO
HOOOOOHOHHOOHHOOOOHHOOO
OOOOOOOOOOHHOOOOOOOOOOO
OOOOOOOOOOOOHOHOOOHOHOO
HOOOOOOHOHOOOHOOOOHHOOO
HOOOOHHHHHHHHOOHOOHHOOO
HOOOOOOOHHOHHHHHOOHHOOO
O

D-15

OHHHHHHHOHHOHOHHOOOOOOO
OOOOOOOOHHHOHOOOHHHHHOO
HOOOOOHOOOHHHHHHHHHHOOO
OHHHHHHHOHHOHOHHHHHHHOO
OOOOOOOOHHHOHOOOOOOOOOO
HOOOOOOOHOHHHHHHHHHHOOO
O

D-16

OHHHHHHHHHHHOOOOOOOOOOO
HOOOOOOOOHHHOOOHHHHHOO
O

D-17

HHHHHHHHHHHHHOHHOOOOHOO
OHHHHHHHHHHHOHOOOOOOHOO
HOOOOOOOHOHHHHHHHHHOHOO
O

Figure 4-2 Serial Binary Flexowriter Format
(Bootstrap Diagnostic Routines)

E. TROUBLESHOOTING

A general guide to the troubleshooting sequence for the PB250 Computer is provided in Figure 4-3. Further information regarding the numbered blocks, is given in the following paragraphs.

E-1. VOLTAGES (BLOCK 1)

Proceed as follows:

a) Turn on power supply and check meter for NOMINAL voltage reading.

b) Using a voltmeter take voltage readings on the power busses. If the readings are within 5%, no adjustments should be made. The indicator lamps on the front panel should be lit. If the readings are in excess of 5%, reference must be made to the PS-7G Power Supply Technical Manual, PBC 3006, or the PS-8 Power Supply Technical Manual, PBC 1013, before making adjustments.

E-2. SA-100 (BLOCK 2)

This is an optional module card which is not used in all PB250 Computers. Paragraph H contains full details of this module.

E-3. CLOCK DISTRUBUTION (BLOCK 3)

For pin connections refer to the applicable logic diagram in Section VI and use a Tektronix Type 545A Oscilloscope with 53C and CA Plug-In Units for all waveform analyses. Refer to Figure 4-4A and proceed as follows:

a) Check the waveform on the CD-100 and one output of the GD-100 module for distributing the general computer clock.

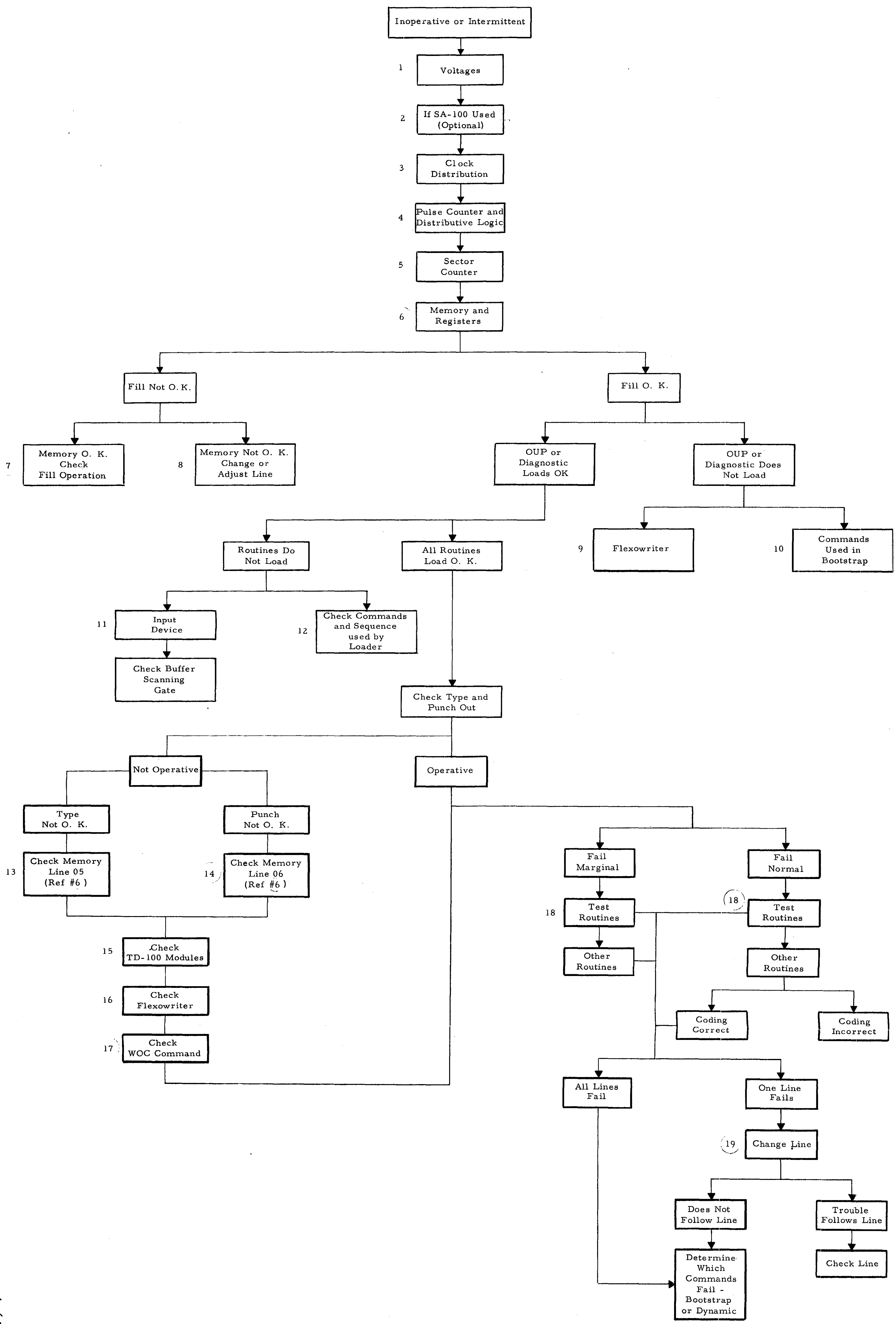


Figure 4-3. Troubleshooting Sequence Block Diagram

b) Check the waveform on the three outputs of the GD-100 module for the distribution of the memory clock.

c) Watch for overloaded outputs.

NOTE

There are two marginal test switches on the front of the computer which are used for changing the width of the computer clock and the memory clock. When the TEST 1 switch is in the ON position, it lengthens the memory clock from 0.155μsec ±10% to 0.170μsec ±10%. See Figure 4-4B.

When the TEST 2 switch is in the ON position, it shortens the computer clock width from 0.27μsec ±5% to 0.24μsec ±10%, and shortens the memory clock from 0.155μsec ±10% to 0.140μsec ±10%. See Figure 4-4C.

E-4. PULSE COUNTER AND DISTRIBUTIVE LOGIC (BLOCK 4)

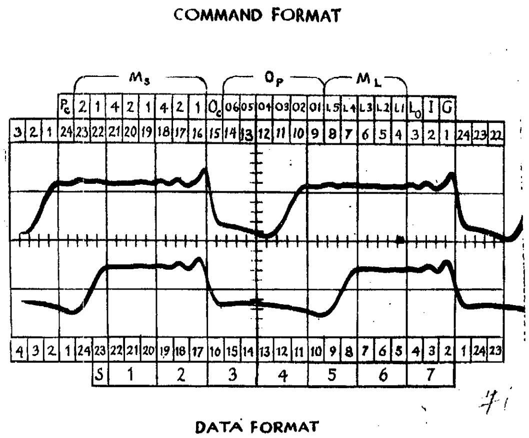
Proceed as follows:

a) Check the operation of the pulse counter by following the procedures shown below Figure 4-4, waveforms D through H.

b) Check the output signals of the following pulses and their time relationship to the pulse counter as follows:

P1, $\overline{P1}$, P2, $\overline{P2}$, P3, $\overline{P3}$, P23, $\overline{P23}$, P24, $\overline{P24}$

(P8-P15), (P16-P23) and (P24-P7)

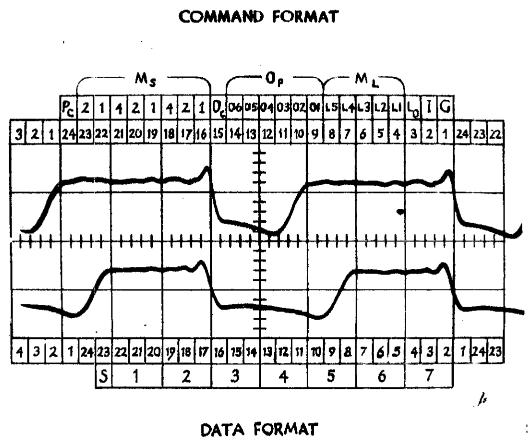


Oscilloscope Settings:

SWEEP	A
TIME/CM	0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	Memory Clock. 25B24
CHANNEL B Trace	Computer Clock. 25B14

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

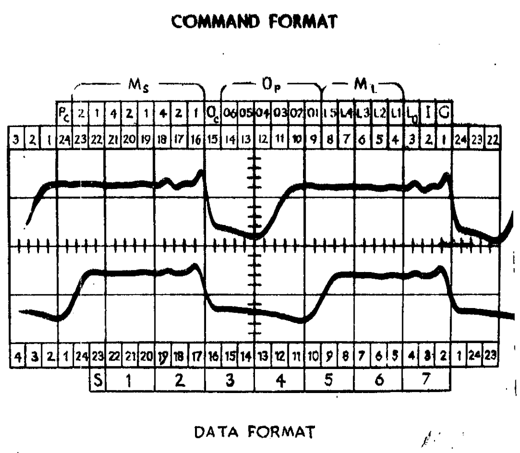


Oscilloscope Settings:

SWEEP	A
TIME/CM	0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	Memory Clock. 25B24
CHANNEL B Trace	Computer Clock. 25B14

Computer Front Panel Settings:

TEST switch 1	ON
TEST switch 2	off

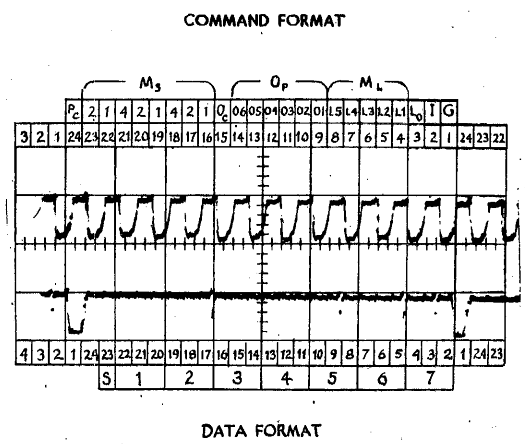


Oscilloscope Settings:

SWEEP	A
TIME/CM	0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	Memory Clock. 25B24
CHANNEL B Trace	Computer Clock. 25B14

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	ON



Oscilloscope Settings:

SWEEP	A
TIME/CM	*0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	F1, 2A14
CHANNEL B Trace	P24, 3E4

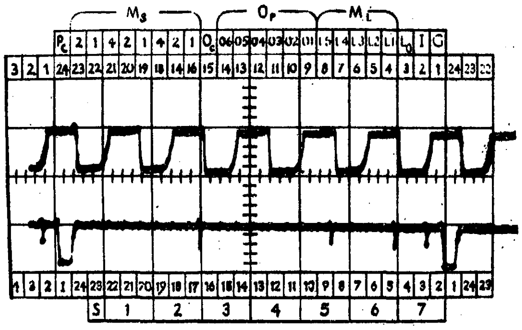
Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

* Calibrated to one word time.

Figure 4-4. Clocks and Pulse Counter Waveforms (Sheet 1 of 2)

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:

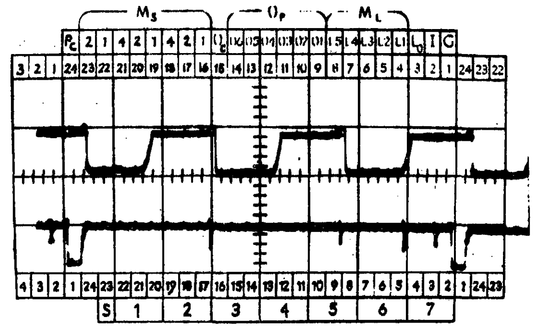
SWEEP	A
TIME/CM	*0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	F2, 2A22
CHANNEL B Trace	P24, 3E4

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

* Calibrated to one word time.

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:

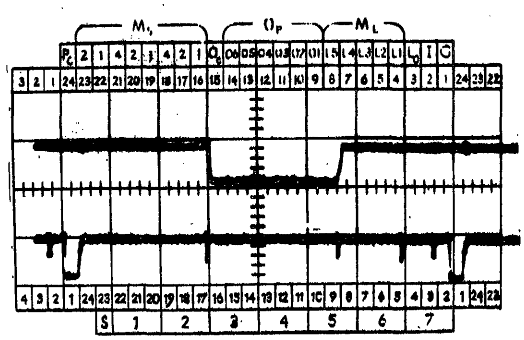
SWEEP	A
TIME/CM	*0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	F3, 3A14
CHANNEL B Trace	P24, 3E4

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

* Calibrated to one word time.

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:

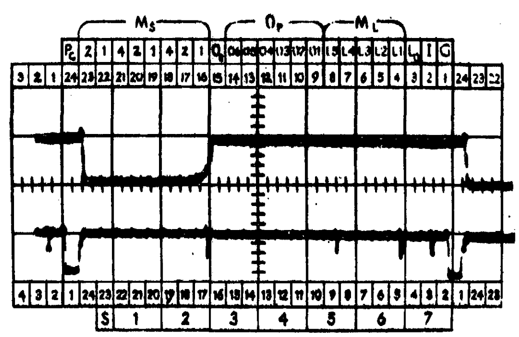
SWEEP	A
TIME/CM	*0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	F4, 3A22
CHANNEL B Trace	P24, 3E4

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

* Calibrated to one word time.

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:

SWEEP	A
TIME/CM	*0. 1μ sec
TRIGGER	P24
VOLTS/CM	10 volts
CHANNEL A Trace	F5, 5A14
CHANNEL B Trace	P24, 3E4

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

* Calibrated to one word time.

Figure 4-4. Clocks and Pulse Counter Waveforms (Sheet 2 of 2)

Sc = sector counter
Cs c register ?,
Qg = sector counter clear term

E-5. CHECKING sSc GATE (BLOCK 5)

Without the sector counter plugged in, check the waveform of sSc. It should be true during P7 and P15. Replace the sector counter and check its counting ability by observing the Sr output and triggering the oscilloscope from the Cs gate. The Cs gate outputs should be 3.072 milliseconds apart. After satisfactory locking on one machine cycle, expand the waveform and check the counting, sector by sector.

E-6. MEMORY AND REGISTERS (BLOCK 6)

Full details of changing or adjusting delay lines are given in paragraph F, below.

E-7. MEMORY OK, CHECK FILL OPERATION (BLOCK 7)

Proceed as follows:

a) Turn the FILL switch (Figure 1-2) to ON position and check that Fi blocks computation by locking the machine in Phase I ($\bar{E}c\bar{R}c$).

b) Check the sector counter to see if Fi is synchronizing via Qg, the two sector numbers P23 - P16.

c) Check the 06 flip-flop. It should be on for (P16-P23) once per machine cycle. 5C14

E-8. MEMORY NOT OK (BLOCK 8)

Change or adjust delay line. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

E-9. FLEXOWRITER (BLOCK 9)

For complete details of the Flexowriter, refer to the Flexowriter Technical Manual, PBC 1016.

E-10. COMMANDS USED IN BOOTSTRAP (BLOCK 10)

Use the individual bootstrap diagnostic routines described in paragraph D, above. These routines may be correlated using the oscilloscope and the particular logic diagram provided in Section VI.

E-11. INPUT DEVICE (BLOCK 11)

Refer to the applicable technical manuals for the Flexowriter, PBC 1016, High-Speed Reader, PBC 1010, Magnetic Tape Unit, PBC 1014, or the High-Speed Buffer Register, PBC 1007.

E-12. CHECK COMMANDS AND SEQUENCE USED BY LOADER (BLOCK 12)

If the input devices have been ascertained as operative, use the individual bootstrap diagnostic routines described in paragraph D, above.

E-12. CHECK MEMORY LINE 05 (BLOCK 13)

Change or adjust memory line 05. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

E-14. CHECK MEMORY LINE 06 (BLOCK 14)

Change or adjust memory line 06. Refer to paragraph F, below, for details on changing or adjusting magnetostrictive delay lines.

E-15. CHECK TD-100 MODULES (BLOCK 15)

These modules are the output cards used to operate the Flexowriter. Refer to Table 6-1 for the locations of TD-100 module cards and the applicable logic diagram for test points.

E-16. CHECK FLEXOWRITER (BLOCK 16)

For complete details of the Flexowriter, refer to the Flexowriter Technical Manual, PBC 1016.

E-17. CHECK WOC COMMAND (BLOCK 17)

To check this command, refer to the bootstrap diagnostic routine described in paragraph IV D; above.

E-18. TEST ROUTINE (BLOCK 18)

Refer to the individual bootstrap diagnostic routines in paragraph IV D above, and eliminate the marginal components.

E-19. CHANGE LINE (BLOCK 19)

Change or adjust delay line. Refer to paragraph F, below for details on changing or adjusting magnetostrictive delay lines.

F. ADJUSTMENT OF MAGNETOSTRICTIVE DELAY LINES

The magnetostrictive delay lines are pre-adjusted at the manufacturer's facility and will not normally require adjustment in the field. However, should adjustment appear necessary, it is advisable to contact the Packard Bell Computer representative. The basic procedure for setting amplifier gain, dc level, and magnetostrictive delay time, is as follows.

F-1. READ AMPLIFIER, DC LEVEL ADJUSTMENT

a) Temporarily connect test point TP 2 to ground, to clear the memory lines.

b) Calibrate the gain on the plug-in vertical amplifier of the oscilloscope.

c) The dc level present at test point TP 1 should be -1. 3 volts.

d) For means of adjustment, refer to Figure 4-5.

1.3v

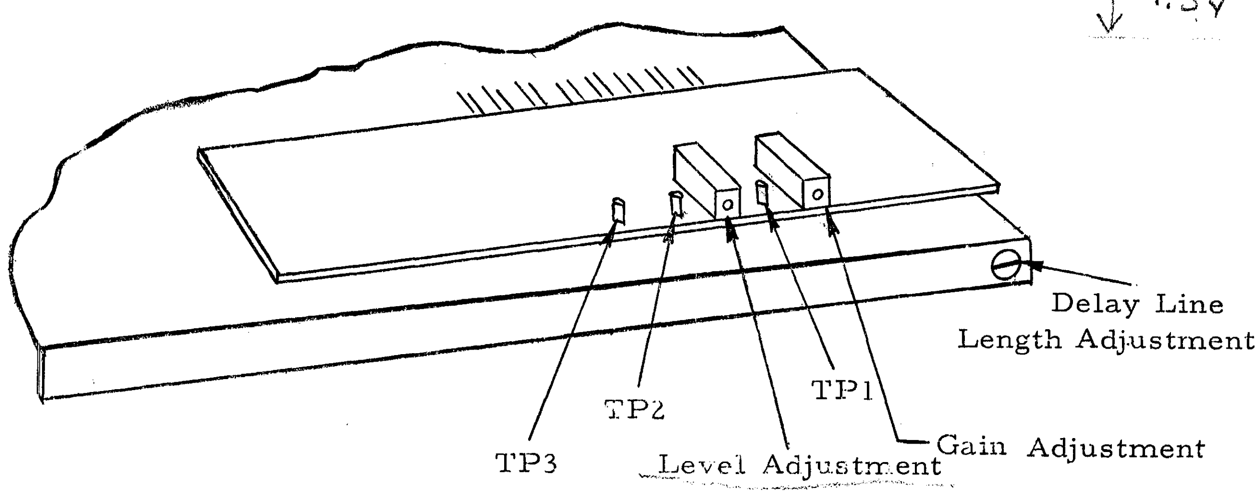


Figure 4-5. Adjustment of Read Amplifier

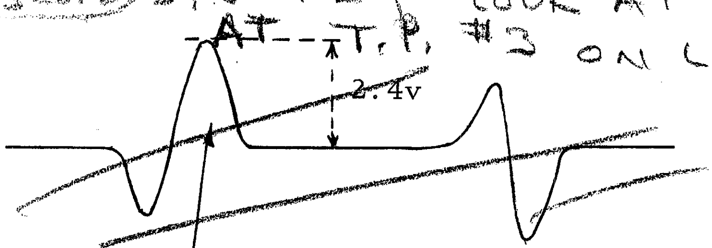
F-2. READ AMPLIFIER, GAIN ADJUSTMENT

a) Fill the line with information by temporarily connecting test point TP 2 to the output of the pulse counter (pin number 3E6, (F-5) Figure 4-8).

b) The displayed information at test point TP 1 should be as shown in Figure 4-6. The information signal should be at an amplitude of 2.4 volts. For means of adjustment, refer to Figure 4-5. INSERT P24 ON TEST POINT 1

2

SCOPE SYN P24 LOOK AT P24 → THEN LOOK AT T.P. #3 ON LINE.



PICTURE ON SCOPE ~~Trailing dipole in positive voltage.~~

Figure 4-6. Read Amplifier Gain Adjustment (Waveform)

F-3. DELAY LINE LENGTH ADJUSTMENT

a) Fill the line with information by temporarily connecting test point TP 2 to the output of the sector counter (pin number 3E1, Figure 4-8).

b) Use a dual trace oscilloscope input with alternate sweep and trigger. Trigger the sweep from the computer clock.

c) With channel B of the vertical amplifier of the oscilloscope, observe the memory clock signal.

LENGTH Of LINE

LINES SET UP

1 SCOPE SET UP

A SYN EXT. - NEG ON P24

B LOOK AT P24 WITH TRACE A

1 .5 VOLTS (~.2 ms/cm)

C LOOK AT DESIRED LINE WITH TRACE B

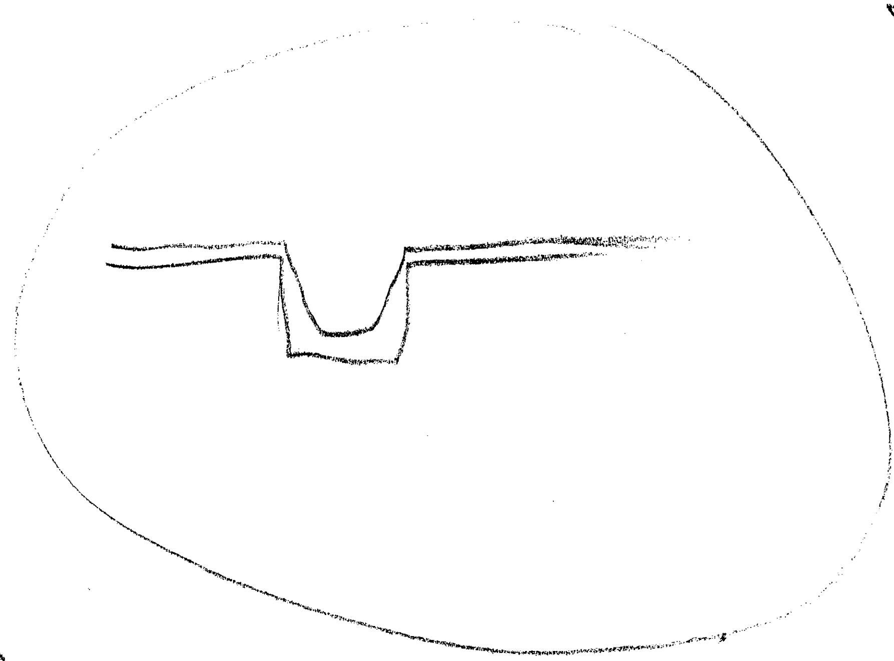
1 .5 VOLTS (x10 PROBE)

D INSERT P24 ON T.P # 1

E WITH TRACE B LOOK AT T.P. #3

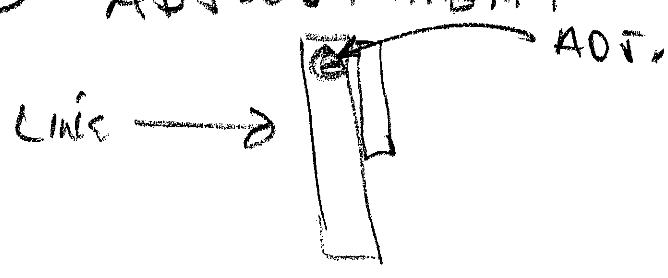
PICTURE ON SCOPE

Sweep .1 u sec.



NOTE: TP 2 INVERTS PULSE

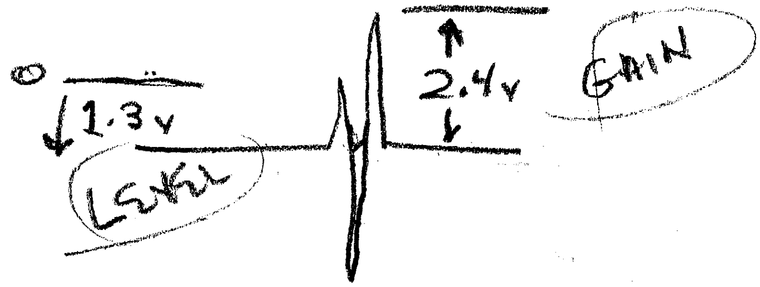
F ADJUSTMENT IS MADE



GAIN & LEVEL

A ONLY ONE TRACE B

SCOPE SET UP. .2 VOLT 2M SEC



.00330

1512.8.1 | 50000

45384

PACKARD BELL COMPUTER CORPORATION

CUSTOMER SERVICE CHARGE ORDER

C.S.C.O. No. 32

Company Name

Company Address

Serial Numbers Affected All

Previous C.S.C.O. Necessary None

Subject: Delay lines adjustment

Purpose: To standardize delay line adjustment procedure

Change Made By

Date Completed

Delay Line Adjustment Procedure

Read Amplifier, dc level and gain adjustment: B

1. Calibrate the gain on the plug-in vertical amplifier of the oscilloscope.
2. To clear an individual line, temporarily connect TP2 of the line to ground. To clear all lines of the machine, turn power on the PB 250 on and off.
3. The dc level at TP1should be -1.3 volts.
4. For means of adjustment, refer to Figure 4-5 in Technical Manual, Volume 2.
5. Fill the line with information by temporarily connecting TP3 to P24 (3E4)*.
6. Displaying TP1 on the scope, a pulse with two positive peaks and one negative peak should be present. The second positive peak (peak furthest from the trigger), should have an amplitude of 2.4 volts.
7. To adjust the gain, refer to Figure 4-5 in Technical Manual, Volume 2.

*CAUTION: Do not allow the jumper to be grounded while it is connected to P24, or damage to P24 circuitry may result.

Delay Line length adjustment: A

1. Use a dual trace oscilloscope input with alternate sweep and trigger. Trigger the sweep with Cycle Sync ~~(0)~~ F5
2. Place one scope probe on TP3 of line to be checked and the other on the memory clock (19E6).
3. Fill the line with information by wiping your finger across the terminals, on the delay line can, that have the co-ax leads on them.
4. Increase the time base to something between 20 usec/cm and .5 msce/cm. With the scope properly synced, the clocks will be stationary and the line information will drift. If the line is out of adjustment. Adjust the delay line length until drift stops. (Refer to Figure 4-5 for means of adjustment) The line is now coarse tuned.

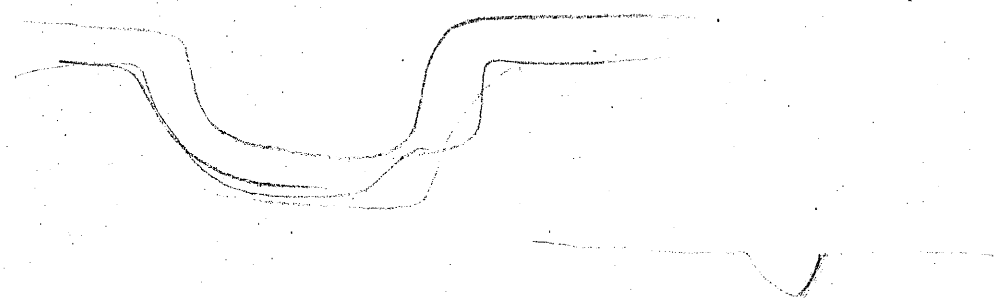
Delay line length adjustment: (cont.)

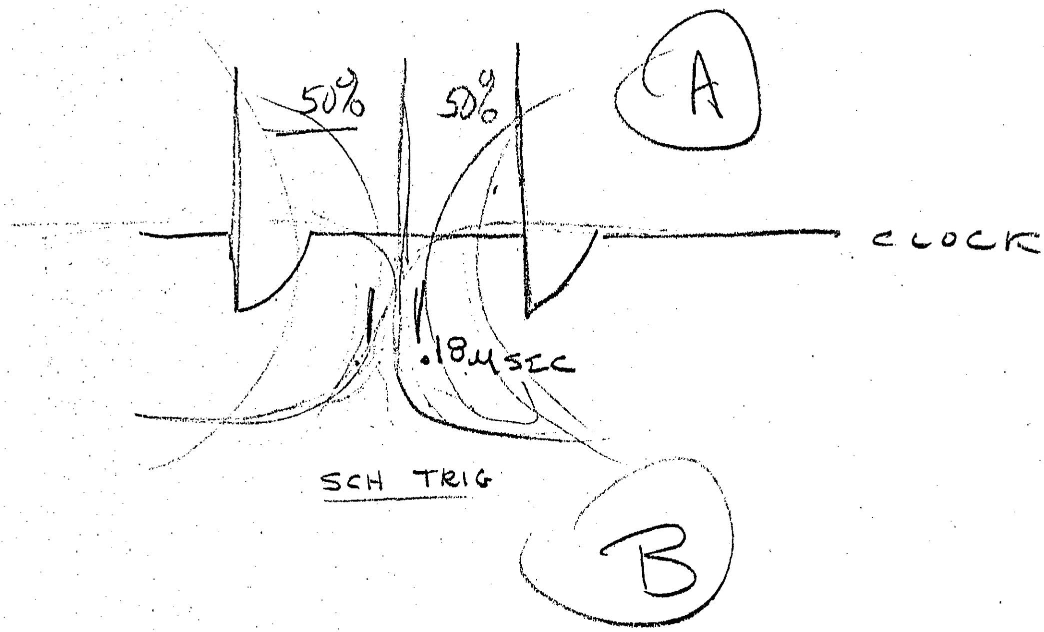
5. To fine tune the line length, decrease the time base on the scope to display three or four clocks and change the sync from Cs to F5 (3E5). Adjust the dispersion of the information such that it is centered between the rise of the clocks. The adjustment is made at the same location as the coarse tune procedure.

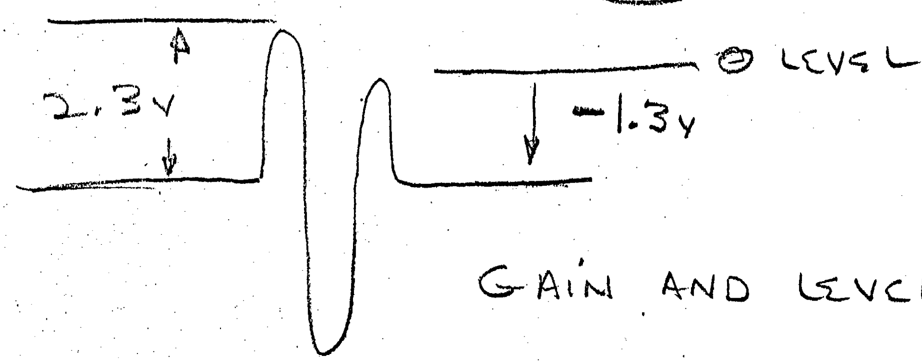
6. In making final length adjustment certain precautions should be taken.
   a. Ferranti-unsealed (MSR1 (long & medium) and MSR2 (short)): The final length adjustment may be made in the clockwise or counter-clockwise direction.
   b. Ferranti, Deltime, or Anderson, -- sealed, (MSR (long & medium)): Initially adjust the line to be .3 microsecond shorter than the correct delay. This is done by turning the length adjustment screw in the clockwise direction. The final length adjustment should then be made with a counter-clockwise rotation of the adjusting screw.
   c. Deltime-sealed (MSR 2 (short)): Adjust the line to be .3 micro-second shorter than the correct delay with counter-clockwise rotation of the adjusting screw. The final adjustment should then be made with clockwise rotation of the adjusting screw.

On completion of length adjustment, be sure to check dc level and gain and correct adjustment if necessary.

(#32)







GAIN AND LEVEL

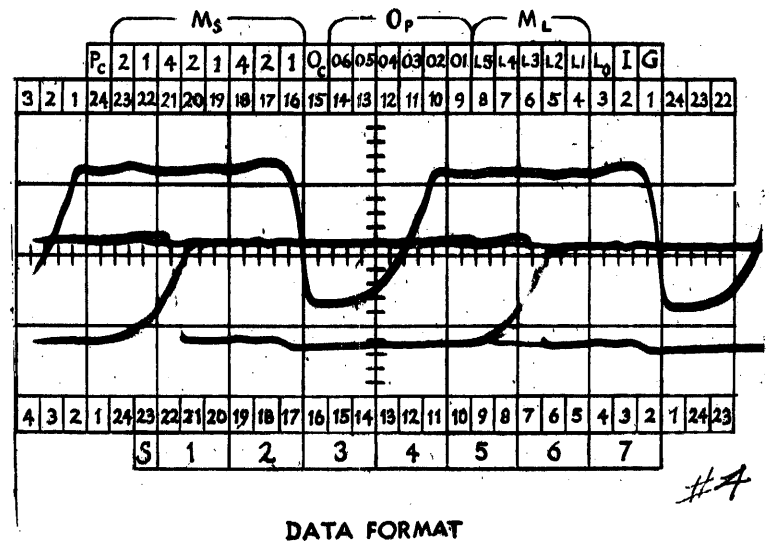
HORIZONTAL
DISPLAY

A only

d) With channel A of the vertical amplifier of the oscilloscope, observe test point TP 2 or TP 3 of the subject magnetostrictive delay line. The display should be shown in Figure 4-7.

e) Adjust the length of the delay line by moving the center of the spread in trigger transition time so that it locates in the center of the positive period of the memory clock. For means of adjustment, refer to Figure 4-5.

COMMAND FORMAT



DATA FORMAT

Oscilloscope Settings:

SWEEP	A
TIME/CM	0. 1μ sec
TRIGGER	P24 (3E4)
VOLTS/CM	5 volts
CHANNEL A Trace	Memory Clock. 19E6
CHANNEL B Trace	TP3-MSR-1 Module.

Computer Front Panel Settings:

TEST switch 1	off
TEST switch 2	off

Figure 4-7. Delay Line Adjustment

G. TEST POINT FUNCTIONS

Mounted on the left side of the PB250 Computer is a panel of fourteen test points (Figure 4-8) located in row "E", connector numbers two and three. The function of these test points is to make readily available certain terms for programming, maintenance, and troubleshooting analysis with an oscilloscope. These terms are shown in Table 4-5.

Table 4-5 (Sheet 1 of 3)

TEST POINT FUNCTIONS

Location	Term	Description
2E1	Ar	The A Register read flip-flop. This point will display the contents of the A Register.
2E2	Br	The B Register read flip-flop. This point will display the contents of the B Register.
2E3	Ir	The Instruction Register read flip-flop. This point will display the contents of the Instruction Register, which includes the Index Register,

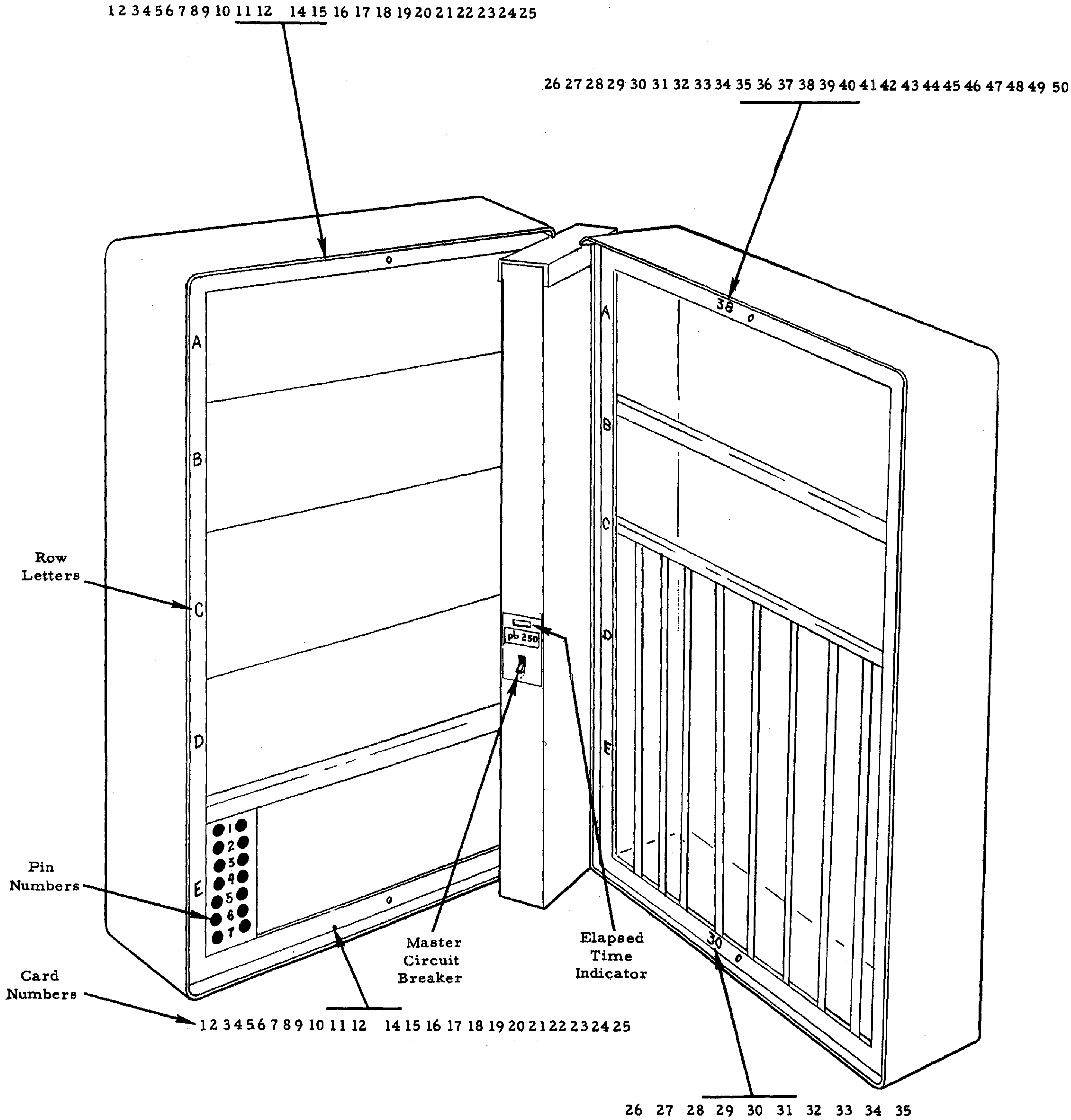


Figure 4-8. Test Points

Table 4-5. (Sheet 2 of 3)

TEST POINT FUNCTIONS

Location	Term	Description
2E4	Vg	The command gate. This point will display the contents of the line from which the computer is receiving its instructions.
2E5		Blank test point.
2E6	Cs	The cycle trigger. This pulse occurs once every machine cycle (approximately three msec) and is used for sync output to the oscilloscope. Pulse begins sweep at sector 000 during memory cycle.
2E7	GND	This point is computer ground.
3E1	Sr	The sector counter read flip-flop. This point will display the counting of the sector counter and also the input buffer.

Table 4-5. (Sheet 3 of 3)

TEST POINT FUNCTIONS

Location	Term	Description
3E2	Cr	The C Register read flip-flop. This point will display the contents of the C Register.
3E3	Fg	The "Fetch" gate. This point displays the data coming from the memory.
3E4	P24	The twenty-fourth pulse of the word counter. This is used to reference the display of a word on the oscilloscope.
3E5		Blank test point.
3E6	F5	The output of F5 is used to provide output for sync of the oscilloscope. F5 occurs during time P16 through P23.
3E7	GND	This point is computer ground.

G-1. USE OF OSCILLOSCOPE

The recommended oscilloscope is a Tektronix Type 545A with delay sweep. The required preamplifier is a Type CA plug-in unit for the dual channels. Refer to the applicable manufacturer's manual for details of operation of oscilloscope and preamplifier.

Calibrate the preamplifier and adjust the test probes. Ground the oscilloscope to the computer by means of a lead from the oscilloscope connected to the computer ground (2E7 or 3E7, Figure 4-8). Connect the sync from cycle trigger (2E6) to the oscilloscope sync input A or B.

Use the following procedure for preliminary adjustment. After the computer has been turned on (see paragraph III B, page 3-1, attach the oscilloscope probes to P24 (3E4). By adjusting the calibration knob of the TIME/CM control, position P24 to occur where indicated on the format pattern, on the oscilloscope screen (see Figure 4-9). If there is no format pattern, remove probe from P24 (3E4) and hook it to F1 (1A35) and calibrate until there are three bits per cm or grid line. This will establish a one-word reference on the oscilloscope. Figure 4-9 shows the P reticle format with a modified P24 pulse waveform added. The reticle is an optional item and may be purchased from Packard Bell Computer, Los Angeles, California.

G-2. A, B, AND C REGISTERS

The A, B and C Registers may be observed for analyzing programs and may be used in isolating possible malfunctions in the equipment. By using one oscilloscope probe on P24 and synchronizing on single cycle, it is possible by means of the delay sweep of the oscilloscope, to view the contents of the A, B, or C Register during a machine cycle. The operation of the computer may be single cycled by having the Flexowriter ENABLE switch (see Flexowriter Technical Manual, PBC 1016) down, and pressing the C key once for each machine command. This allows the operator to analyze the contents

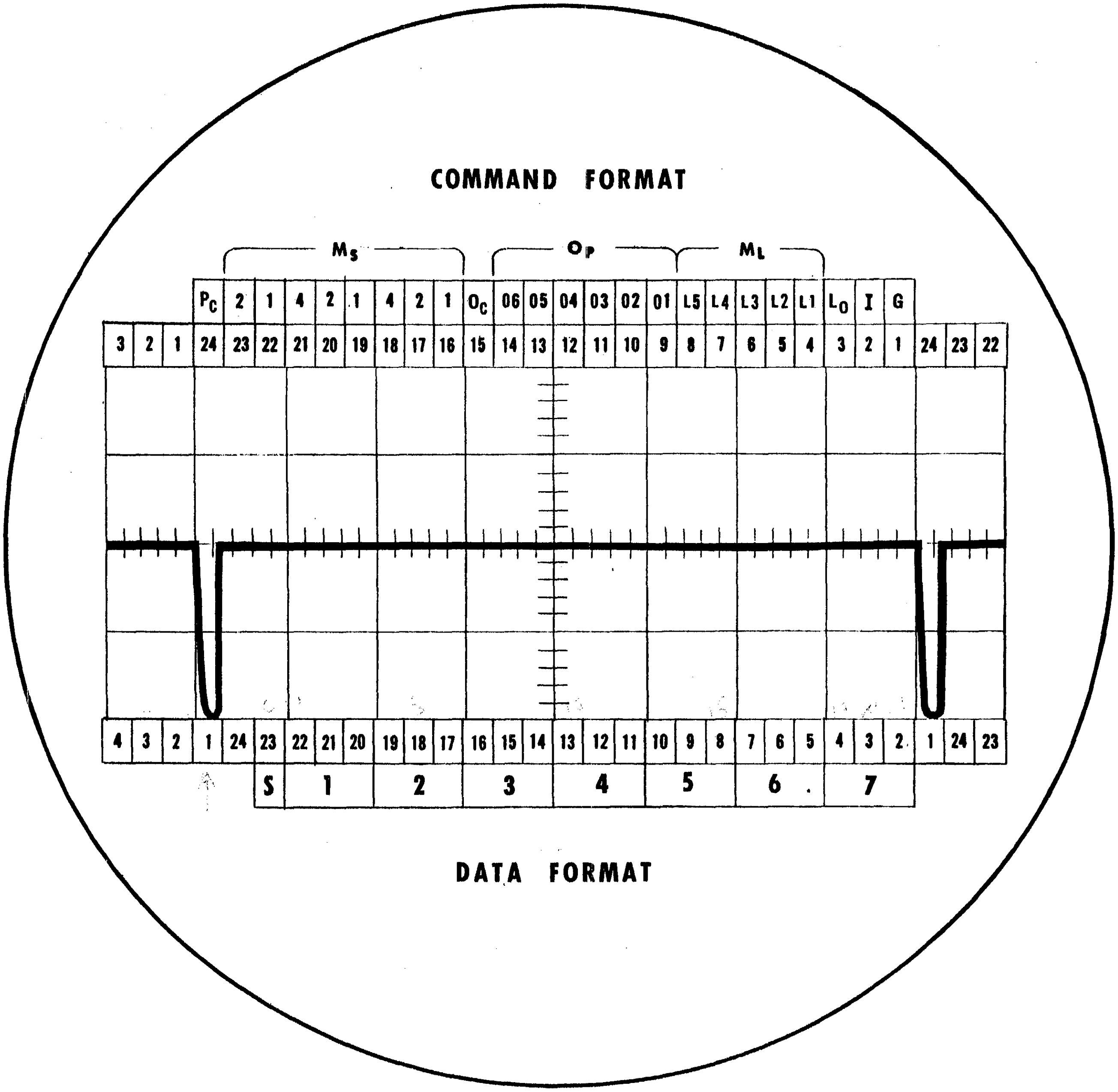


Figure 4-9. Oscilloscope Format

of the registers, as each cycle represents the reading and execution of one command.

By changing the sync input to different terms, the operation may be viewed during a particular command. Selection of a sync pulse ensures that the display of the registers viewed on the oscilloscope is occurring during the subject operation. For instance, a division may be viewed closely by synchronizing on the divide gate.

H. SA-100 SINEWAVE AMPLIFIER

The SA-100 sinewave amplifier module shown in Figure 4-10, is a tuned class C amplifier used for synchronization of a PB250 Computer system consisting of one or more computers and their peripheral equipment. Figure 4-11 shows an example of a distribution system from an SA-100 module to a PB250 Computer system consisting of three computers (one master and two slaves) each with a Memory Unit and two High-Speed Buffers.

The SA-100 accepts the two megacycle sinewave generated by the oscillator section of an XCG-101 module, amplifiers and distributes it to the various units which comprise a PB250 system. The output of the SA-100 is processed in each unit by the shaper section of the XCG-101 module to produce computer and memory clock signals. Distribution of the SA-100 output is established to allow synchronization of the clock signals within 0.01 microsecond between the computer system units. Specifications of the SA-100 are given in Table 4-6.

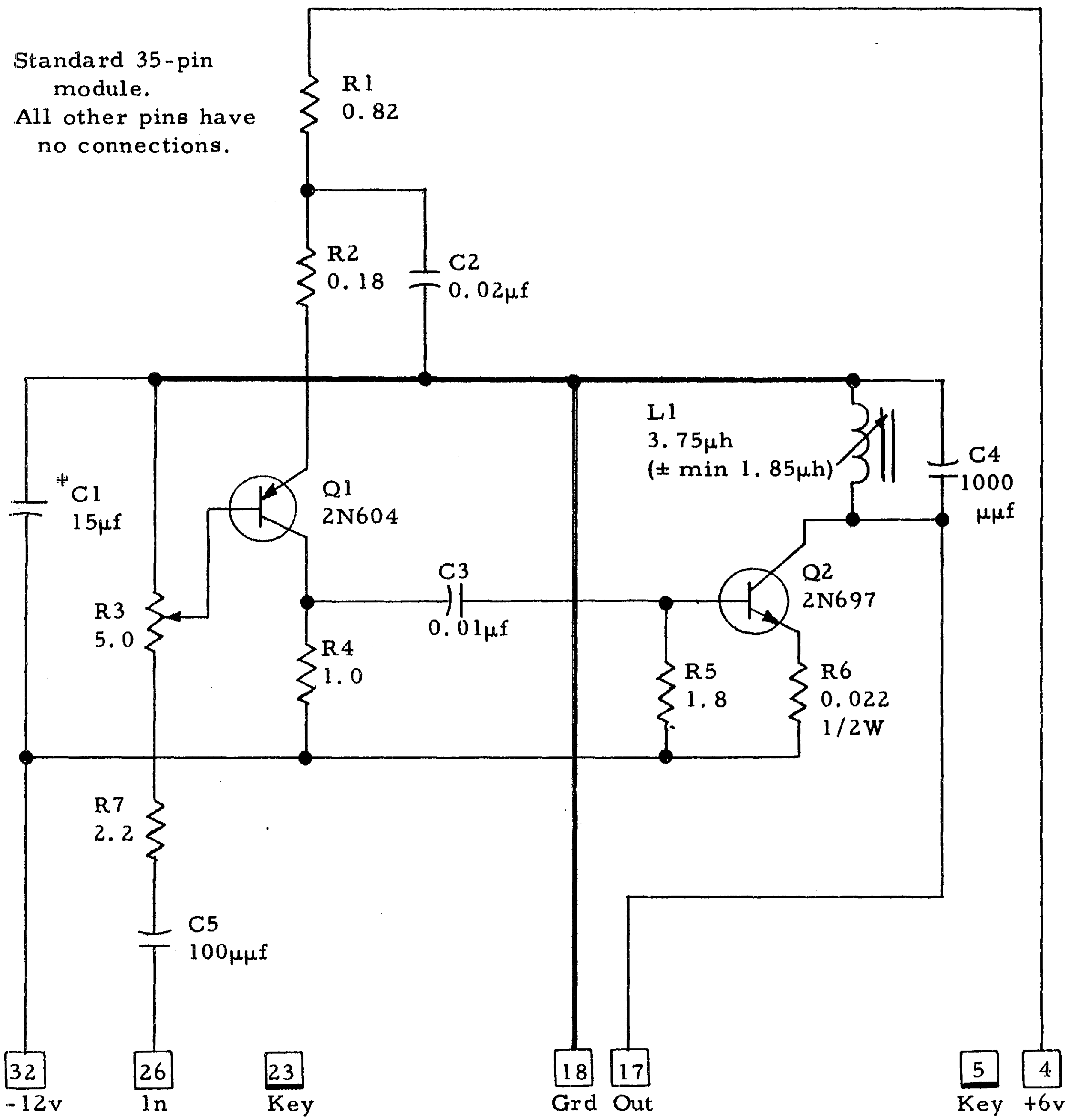


Figure 4-10. SA-100 Sinewave Amplifier Schematic

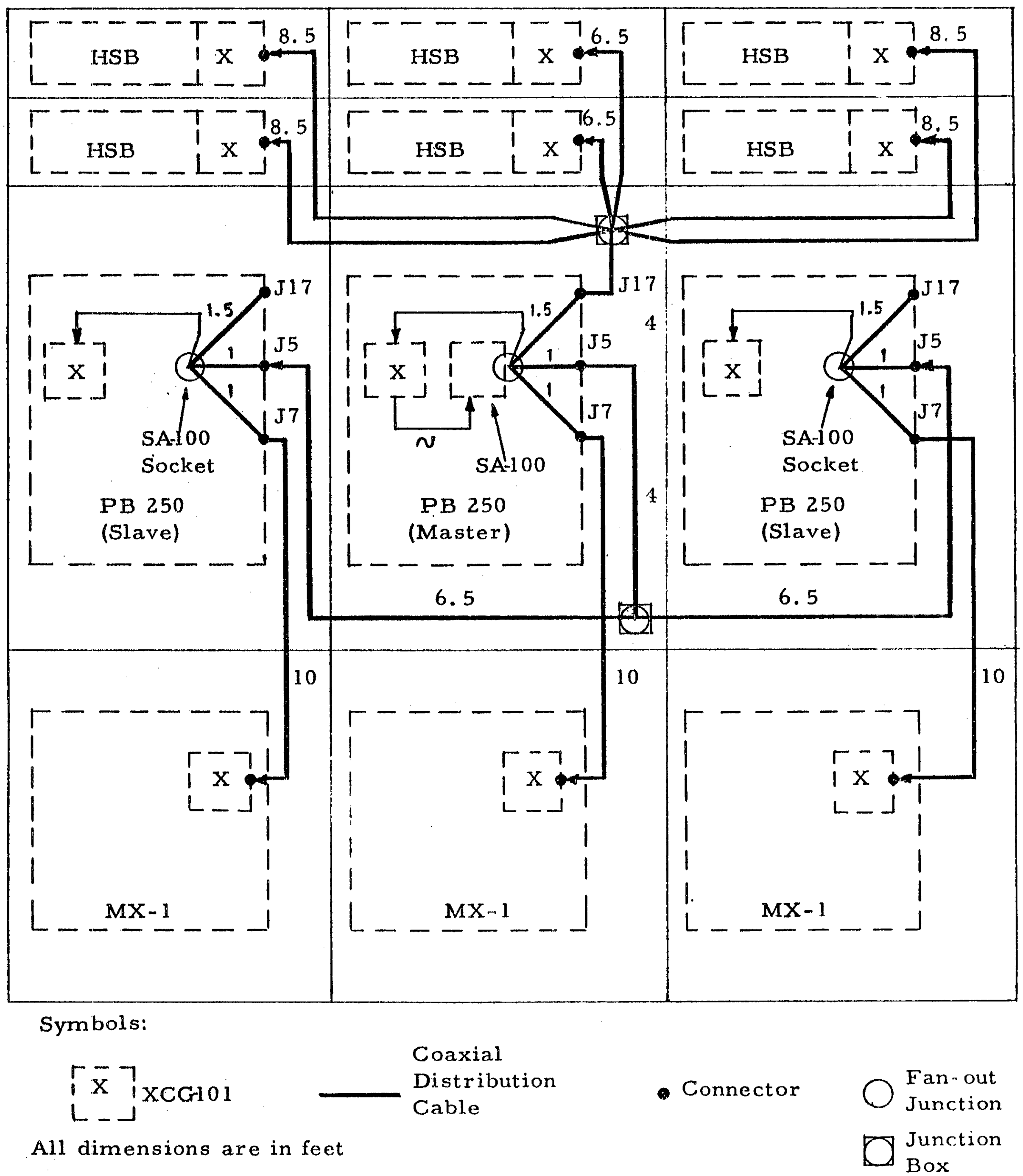


Figure 4-11. SA-100 Clock Distribution

Table 4-6

SA-100 SPECIFICATIONS

Requirements	Measurements
Input (sinewave with the following characteristics)	
Frequency	2Mc
Amplitude	3.5 to 5.5 volts rms
Impedance	4.3 kilohms at 2Mc
Output (at maximum load)	
Number of XCG shapers	12
Distribution cabling capacitance	1500
Power	
-12v	22ma
+ 6v	6ma

H-1. DISTRIBUTION CABLING

The first cable junction is at the socket of the SA-100, with a maximum fan-out of four primary lines. Any one of the primary lines may in turn have one junction with a maximum fan-out of six secondary lines. Where a primary line fans out into two secondary lines only, each secondary line is allowed a third junction with a fan-out of two tertiary lines.

Applicable cabling details are as follows:

a) All connections are made with Microdot 95-3920 coaxial cable (Z_o = 95 ohms, capacitance per foot = 13μμf).

b) Total cable length in distribution system is a maximum of 110 ft.

c) Cable length from the SA-100 to any load point is a maximum of 24 ft.

H-2. FINAL ADJUSTMENT

After the clock system is installed and turned on, the SA-100 is first tuned for maximum output by means of variable inductor L1 (see Figure 4-12 . The output amplitude is then set to 12 volts peak-to-peak by means of potentiometer R3 (see Figure 4-12).

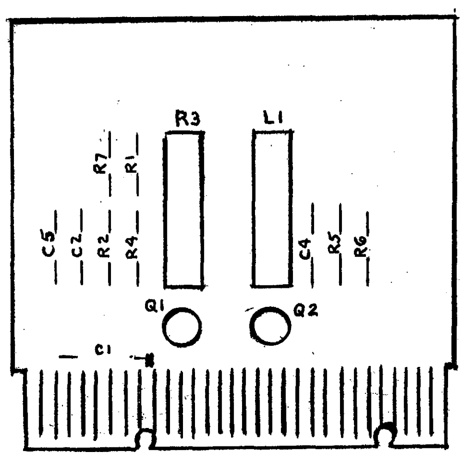


Figure 4-12. SA-100 Printed Wiring Assembly

To tune the SA-100 module for maximum output, it is necessary to remove the locking screw from the variable inductor L-1. After the required adjustment has been made, the locking screw must be replaced.

V. PARTS LIST

The PB250 Computer Assembly is shown in Figure 5-1. The number assigned to each subassembly or part in the figure corresponds to the number in the Figure and Index column of the Parts List in Table 5-1.

Information concerning parts and procurement may be obtained from the Packard Bell Computer Corporation, Los Angeles 25, California.

Table 5-1. (Sheet 1 of 2)

PB250 COMPUTER ASSEMBLY, PARTS LIST

Figure and Index	Part Description	Ref. Desig.	PBCC Part Number	Qty	Usable On Code
Fig. 5-1	PB250 ASSY		502617	1	
1, 2	. HANDLES ASSY		500033	1	
3	. FRAME ASSY, Right		502480	1	
4	. FRAME ASSY, Left		502464	1	
5	. POST, Center		502203	1	
6	. PLATE ASSY, Connector		502585	1	
7	. COVER, Front		502228	1	
8	. MOUNT ASSY, Time Indicator		504554	1	
9	. COVER, Standard Wiring		502487	5	
10	. COVER, Offset Wiring		502596	1	
11	. MODULE, Crystal Clock Generator, XCG-101		506521	1	
12	. MODULE, Clock Driver, CD-100		502692	1	
13	. MODULE, Gate Driver, GD-100		502492	6	
14	. MODULE, Driver, TD-100		502473	4	
15	. MODULE, Emitter-Follower, EF-100 . .		502454	5	
16	. MODULE ASSY, Memory, 1 Word, MSR-2		504398-11-23	3	
17	. MODULE, Flip-Flop, TF-100		502433	17	
18	. MODULE ASSY, Memory, 16 Word, MSR-1		504276-191	1	
19	. MODULE, Diode Gate, DG-102		502336	29	
20	. MODULE, Diode Gate, DG-101		502321	38	
21	. MODULE, Diode Gate, DG-100		502334	16	
22	. MODULE, Filter Card, FC-100		504580	3	
23	. MODULE, Emitter-Follower, EF-101 . .		504625	4	
24	. SCREW, Pan Head, No. 4-40 x 7/16 . . .		503505-7-2	16	
25	. SCREW, Pan Head, No. 6-32 x 5/16 . . .		503507-5-2	10	
26	. SCREW, Flat Head, No. 6-32 x 1/4, csk 100°		503506-4-2	48	
27	. SCREW, Flat Head, No. 8-32 x 7/16, csk 100°		503508-7-2	8	
28	. SCREW, Pan Head, No. 8-32 x 5/16 . . .		503509-5-2	10	
29	. SCREW, Pan Head, No. 6-32 x 1/2 . . .		503507-8-2	2	
30	. WASHER, Flat, No. 6		503519-4-2	2	
31	. SCREW, Flat Head, No. 6-32 x 7/8, csk 100°		503506-14-2	4	
32	. Deleted				
33	. CABLE, AC Power		504263	1	
34	. BUSHING		503149-10	1	
35	. BUSHING		503149-7	1	
36	. RELAY		503193	1	
37	. CABLE ASSY, Power Supply, PB250 . . .		504596	1	
38	. SLEEVING, Spiral Wrap		503077-2	AR	
39	. CORD, Black Lacing		503216-2	AR	
40	. SOLDER (QQ-S-571, Type SN60)			AR	
41	. WIRE, Stranded, Teflon Insulation . . .		503045-24	AR	
42	. WIRE, 24 AWG, Solid, Teflon Insulation .		503089-24	AR	
43	. CLAMP, Cable		503018-7	4	
44	. WIRE, 16 AWG, Stranded, Teflon Insulation		503091-16-2	AR	
45	. WIRE, 24 AWG, Stranded, Teflon Insulation		503091-24-2	AR	
46	. WIRE, 16 AWG, Stranded, Teflon Insulation		503045-16	AR	
47	WIRE, 16 AWG, Stranded, Teflon Insulation		503091-16-4	AR	
48	SLEEVING, Plastic, No. 24		503047-24	AR	

Table 5-1. (Sheet 2 of 2)

PB250 COMPUTER ASSEMBLY, PARTS LIST

Figure and Index	Part Description	Ref. Desig.	PBCC Part Number	Qty	Usable On Code
Fig. 5-1					
49	. SLEEVING, Plastic, No. 22		503047-22	AR	
50	. SLEEVING, Plastic, No. 24		503092-24-2	AR	
51	. SLEEVING, Plastic, No. 24		503092-24-1	AR	
52.	. TERMINAL, Solderless		503122-1	3	
53	. TERMINAL, Solderless		503122-2	10	
54	. WASHER, Lock, Flat, Internal Tooth, No. 6		503520-6-2	14	
55	. TERMINAL, Standoff, Molded, (modified) .		505060	2	
56	. DIODE, IN2069		503178	2	
57	. SLEEVING, Plastic, No. 16		503047-16	AR	
58	. WIRE, Solid Uninsulated No. 16		503048-16	AR	
59	. SLEEVING, Plastic, Clear, No. 14 . . .		503092-14-1	AR	
60	. RESISTOR, 6.8k ±5%, 1/4 w.		503100-682	18	
61	. RESISTOR, 2.7k ±5%, 1/4 w.		503100-272	6	
62	. RESISTOR, 5.6k ±5%, 1/4 w.		503100-562	25	
63	. RESISTOR, 15k ±5%, 1/4 w		503100-153	1	
64	. RESISTOR, 18k ±5%, 1/4 w		503100-183	5	
65	. NAMEPLATE, Escutcheon		504532	1	
66	. MODULE ASSY, Memory, 256 Words, MRS-1		504276-3071	3	
67	. RESISTOR, 1k ±5%, 1/4 w		503100-102	3	
68	. RESISTOR, 1.5k ±5%, 1/4 w		503100-152	8	
69	. RESISTOR, 1.2k ±5%, 1/4 w		503100-122	2	
70	. DIODE, Germanium, High Speed		503050	5	
71	. RESISTOR, 1.8k ±5%, 1/4 w		503100-182	1	
72	. MODULE ASSY, Memory, 1 Word, MSR-2 .		504398-11-24	2	
73	. RESISTOR, 10k ±5%, 1/4 w		503100-103	8	

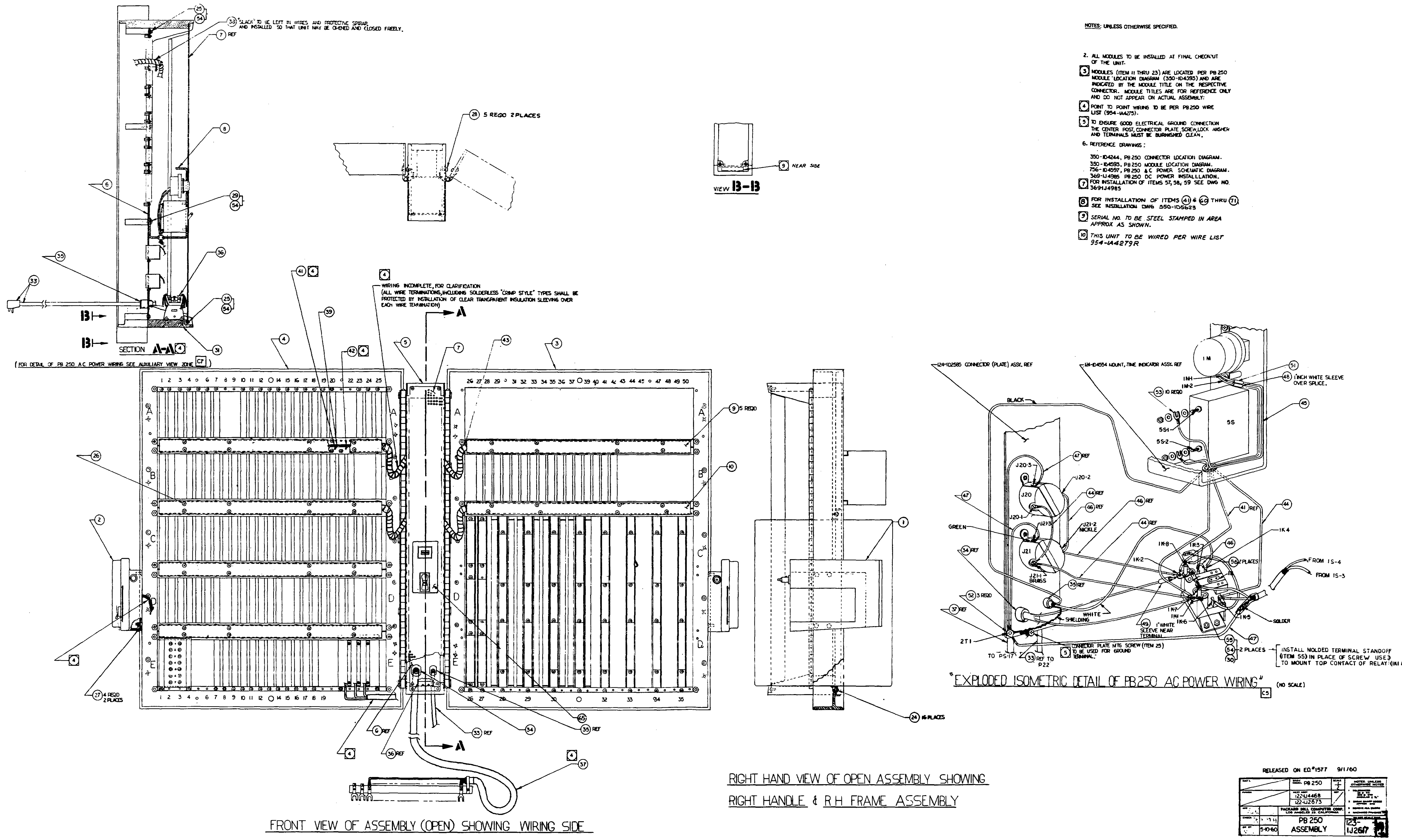


Figure 5-1. PB250 Assembly

VI. LOGIC DIAGRAMS

This section contains logic layout diagrams of the PB250 Computer. Table 6-1 identifies the module location with the logic layout sheet pertaining to the location of each module, and the type of module.

These logic diagrams may be used in conjunction with the module schematic diagrams in Section VII.

Table 6-1. (Sheet 1 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
1A	26, 35, 67	DG-102
2A	26	TF-100
3A	26	TF-100
4A	26, 28, 60, 67	DG-101
5A	26, 28	TF-100
6A	28, 29	DG-100
7A	29	MSR-2 SECTOR COUNTER
8A		
9A	26, 27, 29, 60, 67	EF-101
10A	27, 31, 74	GD-100
11A	27, 32, 75	DG-101
12A	27, 32, 74	DG-102
13A	30, 33	DG-101
14A	27, 28, 14, 69	DG-101
15A	27, 68, 69, 73	DG-101
16A	68	DG-101
17A	27, 60, 67, 68, 69	DG-102
18A	46, 67, 69, 73	EF-100
19A	36, 37, 38, 69	EF-100
20A	27, 69, 72	GD-100
21A	26, 30, 67, 72	DG-101
22A Comp. Coupling	26, 30	(EF-101)
23A	25, 67	FC-100
24A	25, 67	FC-100

Table 6-1. (Sheet 2 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
25A	25,67	FC-100
26A	47	DG-101
27A	47	DG-102
28A	47	DG-101
29A	47	DG-102
32A	77	GD-100
33A	77	GD-100
1B	34,35	DG-101
2B	34	MSR-2 INSTRUCTION REG.
3B		
4B	31,34	DG-101
5B	26,31,34,44,74	DG-102
6B	31	DG-100
7B	31	TF-100
8B	31,46	DG-101
9B	33,46	DG-101
10B	33,46	DG-100
11B	33,46	TF-100
12B	46	TF-100
13B	33,60	DG-102
14B	28,60	DG-101
15B	27,47,60,74	DG-102
16B	44,47,60	DG-101
17B	26,60,74	GD-100

Table 6-1. (Sheet 3 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
18B	44,69	DG-101
19B	36,37,38,39,40 46,?	EF-100
20B	66	DG-100
21B	66	TF-100
22B	24	CD-100
23B	24	EF-101
24B	24	SA-100
25B	24	XCG-101
26B	59,75	EF-101 used for memory test & complete [illegible]
27B	59,64,72	DG-101
28B	47,64	DG-101
29B	47	DG-101
30B	47	DG-102
31B	59,62	DG-101
32B	59	DG-101
33B	59	DG-101
34B	59,64,71,72	DG-102
35B	59,64	DG-101
36B	64,71	DG-101
37B	71,72	DG-101
38B	62,71	DG-101
39B	71	DG-102
40B	59,71	DG-101
41B	71	DG-101

Table 6-1. (Sheet 4 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
42B	71 extra jump control	DG-101
43B	63,76 mag tape only	DG-101
44B	76	TF-100
45B	63,65,76	DG-102
46B	63,65	DG-101
47B	63,65	DG-101
48B	63,65	DG-101
49B	63	EF-101
1C	35,37	DG-100
2C	32,35,36,37	DG-102
3C	35,37	TF-100
4C	36,37	DG-100
5C	36	TF-100
6C	36,37,42,43	DG-102
7C	36,37	DG-100
8C	36,37	TF-100
9C	36,37,38	DG-100
10C	37,38,43,49	DG-102
11C	38,43	TF-100
12C	43	DG-100
13C	41,42	TF-100
14C	41,42	DG-100
15C	27,40,42,43,60,61	DG-102
16C	40,41	DG-100

Table 6-1. (Sheet 5 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
17C	39, 40, 41, 42, 58, 60, 61	DG-102
18C	39, 40	DG-100
19C	39, 40	TF-100
20C	40, 76, 59, 51	DG-102
21C	42, 43, 45, 53, 61, 73	DG-102
22C	27, 44, 45, 66	DG-102
23C	40, 41, 42, 43, 45	EF-100
24C	44, 45, 60	DG-102
25C	44 N09 - N79	EF-100
26C	70	TD-100
27C	75	GD-100
28C	62, 63	MSR-1
29C	62	MSR-1
30C	62, 63	MSR-1
31C	62	MSR-1
32C	62	MSR-1
33C	62	MSR-1
34C	62	MSR-1
35C	62	MSR-1
1D	49	DG-101
2D	37, 49, 59	DG-102
3D	49	DG-101
4D	49, 73	DG-101
5D	36, 49, 51	DG-102

Table 6-1. (Sheet 6 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
6D	49,51	DG-101
7D	49 A REGISTER	MSR-2
8D		
9D	49,51	TF-100
10D	49,51,53	DG-102
11D	51 ~~REGISTER~~	DG-101
12D	51,61	DG-102
13D	51,55	DG-101
14D	51 B REGISTER	MSR-2
15D		
16D	58,61	DG-100
17D	58,61	DG-100
18D	53,61	TF-100
19D	53,61,76	DG-102
20D	53	DG-101
21D	53,61	DG-101
22D	53 C REGISTER	MSR-2
23D		
24D	43,76 mag tape & mem. gt	TF-100
25D	45	EF-100
26D	70	TD-100
27D		
28D	62,64	MSR-1
29D	62	MSR-1
30D	62	MSR-1

Table 6-1. (Sheet 7 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
31D	62,64	MSR-1
32D	62	MSR-1
33D	62	MSR-1
34D	62	MSR-1
35D	62,65	MSR-1
1E		
2E		Test jack
3E		Test jack
4E		
5E	46	DG-100
6E	46	TF-100
7E		
8E	49,51,55	EF-101
9E	54,55,56,76	DG-102
10E	54,55	DG-101
11E	54,55	DG-101
12E	55	DG-101
13E	49,51,54,57,58	DG-102
14E	56,67	DG-102
15E	24,57,58	DG-102
16E	56,58	DG-100
17E	56,58	TF-100
18E	57	DG-101
19E	24,53	EF-101

Table 6-1. (Sheet 8 of 8)

MODULE LOCATIONS IN LOGIC DIAGRAMS

Location	Sheet	Type
20E	24	GD-100
21E		
22E		Terminal strips
23E		Terminal strips
24E		Terminal strips
25E		
26E	67,70	TD-100
27E	70	TD-100
28E		
29E		
30E		

B. L.	E. O. NO	REV. LTR.	REVISION	BY	DATE	APP.	CHK
NO	—	Q	(HISTORY RECORDED L THRU Q) COVER PAGE REVISED. CHANGED PER EDR #338. IDENTIFIED PAGES AND REV OF THIS DWG WITH CHG LETTERS CORRESPONDING TO WIRE LIST CHGS. RELEASED.	RH	7/14/61	[illegible]	[illegible]
NO	—	R	CHANGED PER DCR 1190. (DELETED SHT. 68)	HM	7/3/61	[illegible]	[illegible]
NO	—	S	REVISED (PER DCR NO. 1349)	FG	1/7/61	[illegible]	[illegible]
NO	—	T	REVISED (PER DCR'S 1522 & 1051) SH. NO. CHANGES NOTED ON E.O	K.W	2/5/6		

COVER SHEET FOR PB-250 LOGIC LAYOUT DIAGRAM

THIS DRAWING CONSISTS OF 77 SHEETS:

1) TITLE PAGE

2 & 3) REVISION INDEX

4) ALPHABETICAL INDEX SHEET

5 THRU 77) LOGIC

RELEASED ON S.O. #630-1A4875/REV.10 DATED 7/10/61

MAT'L	BASIC MODEL PB-250	SCALE	NOTES: UNLESS OTHERWISE NOTED 1. TOLERANCES: .XX ± .03 .XXX ± .010 ANGULAR ± ½° 2. BREAK SHARP EDGES APPROX. .010 3. REMOVE ALL BURRS 4. MACHINED FINISHES 100 DO NOT SCALE DWG.
FINISH	NEXT ASSY.	REF.	

APP. J.W.W.	3/15/61	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		
CHECK K.A.B.	3/15/61	PB-250 LOGIC LAYOUT DIAGRAM	505782 SH. 1 OF 77	T CHG.
DR. BY H.M.	3/14/61			

REVISION INDEX SHEET

DWG NO. 505782 — REF T

SHEET NO. 2

SHEET	REVISION	SHEET	REVISION	SHEET	REVISION	SHEET	REVISION
1	T	19	T	37	T	55	T
2	T	20	T	38	T	56	T
3	T	21	DELETED PER REV R	39	T	57	T
4	T	22	T	40	T	58	T
5	T	23	T	41	T	59	T
6	T	24	T	42	T	60	T
7	T	25	T	43	T	61	T
8	T	26	T	44	T	62	T
9	T	27	T	45	T	63	T
10	T	28	T	46	T	64	T
11	T	29	T	47	T	65	T
12	T	30	T	48	T	66	T
13	T	31	T	49	T	67	T
14	T	32	T	50	T	68	T
15	T	33	T	51	T	69	T
16	T	34	T	52	T	70	T
17	T	35	T	53	T	71	T
18	T	36	T	54	T	72	T

PBC 335

REVISION INDEX SHEET

DWG NO. 505782 | REF T

SHEET NO. 3

SHEET	REVISION	SHEET	REVISION	SHEET	REVISION	SHEET	REVISION
73	T						
74	T						
75	T						
76	T						

PBC 335

PB 250 ALPHABETICAL INDEX

505782 T
SH. 4

TYPE 37P No. 1J FUNCTION FLEXO-INPUT

Origin	Pin No.	Dest.	Term
	1	23A5	T1
	2	24A12	T2
	3	23A12	T3
	4	25A12	T4
	5	24A5	T5
	6	25A5	T6
	7	23A31	Tc
	8	23A8	R1
	9	24A15	R2
	10	23A15	R3
	11	25A15	R4
	12	24A8	R5
	13	25A8	R6
	14	24A21	R7
	15	23A21	R8
	16	25A28	Rc
	17	25A31	$\overline{Rc}$
1J27	18	23A34	(En + $\overline{Rf}$Tf)
1J26	19	24A34	(Rf $\overline{Tf}$)
	20	25A25	Tb
	21	24A28	En
	22	24A31	$\overline{En}$
	23	24A25	Bp
1J25	24	23E5L	-12V
1J28	25	1J24	-12V
	26	1J19	(Rf $\overline{Tf}$)
	27	1J18	(En+$\overline{Rf}$Tf)
	28	1J25	-12V

TYPE 155 No. 2J FUNCTION CHARACTER OUT.

Origin	Pin No.	Dest.	Term
3J1	1	14J10	K3'
3J2	2	14J11	K2'
3J3	3	14J12	K1'
3J4	4	14J13	L1'
3J5	5	14J14	L2'
3J6	6	14J15	L3'
3J7	7	14J16	L4'
3J8	8	14J17	L5'
3J9	9	14J18	O1'
3J10	10	14J19	O2'
3J11	11	14J20	O3'
3J12	12	18J26	Cog
3J13	13	15J13	Gnd
3J14	14	15J14	+6
3J15	15	15J15	-12

TYPE 155 No. 3J FUNCTION CHARACTER OUT.

Origin	Pin No.	Dest.	Term
18A26	1	2J1	K3'
18A29	2	2J2	K2'
19B5	3	2J3	K1'
26D7	4	2J4	L1'
23C11	5	2J5	L2'
23C8	6	2J6	L3'
23C5	7	2J7	L4'
19B29	8	2J8	L5'
45B35	9	2J9	O1'
36B34	10	2J10	O2'
36B33	11	2J11	O3'
18A23	12	2J12	Cog
	13	2J13	Gnd
	14	2J14	+6
	15	2J15	-12

TYPE 25S No. 4J FUNCTION FLEXO-OUT

Origin	Pin No.	Dest.	Term
	1	26E24	LTC
	2	26C5	LT1
	3	26C9	LT2
	4	26C13	LT3
	5	26C20	LT4
	6	26C24	LT5
	7	26C28	LT6
	8	26E13	LPC
	9	26D5	LP1
	10	26D9	LP2
	11	26D13	LP3
	12	26D20	LP4
	13	26D24	LP5
	14	26D28	LP6
	15	27E5	LP7
	16	27E9	LP8
	17	26E9	(Rf $\overline{\text{Tf}}$)
	18	26E5	($\overline{\text{Rf}}$Tf)
	19		Spare
	20		Spare
7J20	21	4J24	-48
	22	4J23	
4J22	23		
4J21	24	4J25	-48
4J24	25	23E6R	-48

TYPE IIWIS No. 5J FUNCTION COMPUTER COUPLING

Origin	Pin No.	Dest.	Term
21A33	1		N7g
21A34	2		M3g
21A35	3		Cpg
27B33	4		M8r
26B20	5		F5
21A20	6		E5
24E1R	7		Gnd
26B6	8		M8r
	9		
	10		
24B17	A1		SA Out 2

TYPE 25P No. 7J FUNCTION MEMORY - EXT

Origin	Pin No.	Dest.	Term
23C26	1		M2g
38B5	2		M3g
25D5	3		M4g
25D8	4		M5g
25D11	5		M6g
25D14	6		M7g
25C5	7		N0g
25C8	8		N1g
25C11	9		N2g
25C14	10		N3g
25C20	11		N4g
25C23	12		N5g
25C26	13		N6g
35D26	14		N7g
26B14	15		Wxg
26B24	16		Ixg
	17		
	18	40B20	Fxg
14J21	19	18A20	Cpg
4J21	20		-48V
	21	22E2R	+6
	22	17J6	0
	23	23E5R	-12
	24		Shield
24B13	25		SA out 4

TYPE 11W1P No. 8J FUNCTION JUMP CONTROL IN.

Origin	Pin No.	Dest.	Term
42B33	1		J0
42B27	2		J1
42B23	3		J2
42B10	4		J3
42B6	5		J4
39B29	6		J5
41B33	7		J6
41B27	8		J7
	9	9J9	Gnd

TYPE 11W1P No. 9J FUNCTION JUMP CONTROL IN.

Origin	Pin No.	Dest.	Term
41B23	1		J8
41B10	2		J9
41B5	3		J10
39B25	4		J11
40B33	5		J12
40B27	6		J13
40B23	7		J14
40B10	8		J15
8J9	9	10J9	Gnd

TYPE 11W1P No. 10J FUNCTION JUMP CONTROL IN.

Origin	Pin No.	Dest.	Term
40B6	1		J16
39B12	2		J17
36B12	3		J18
36B7	4		J19
38B35	5		J20
38B29	6		J21
38B25	7	18J10	J22
38B12	8	18J11	J23
9J9	9	11J9	Gnd

TYPE 11W1P No. 11J FUNCTION JUMP CONTROL IN.

Origin	Pin No.	Dest.	Term
38B8	1	16J9	J24
39B10	2	15J9	J25
37B33	3	18J27	J26
37B27	4	18J9	J27
37B23	5	14J9	J28
	6		spare
	7		spare
	8		spare
10J9	9	24E5L	Gnd

TYPE 50S No. 12J FUNCTION BOOTSTRAPS IN.

Origin	Pin No.	Dest.	Term
	1	2D25	B6
	2	25A27	Rc
	3	9C2	B5
	4	25A33	Rc
	5	9C16	B4
	6	25A14	R4
	7	16D2	B1
	8	23A7	R1
	9		
	10		
	11		
	12	20B21	Mr
	13	22C34	Mr
	14		
	15	14J33	HSR Start
	16	18J33	MTUStart
14E33	17		H.S.Start
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
	32		
	33		
	34	14J6	S6
	35	18J6	U6
	36	14J5	S5
	37	18J5	U5
	38	14J4	S4
	39	18J4	U4
	40	14J1	S1
	41	18J1	U1
	42		
	43		
18J25	44	12J45	Gnd
12J44	45	24E4R	Gnd
14J25	46	12J47	-12
12J46	47	23E4R	-12
	48	14J37	HSR Stop
	49	18J37	MTU Stop
23B1	50		H.S.Stop

TYPE 37S No. 14J FUNCTION PHOTO - READER IN.

Origin	Pin No.	Dest.	Term
12J40	1	23A3	S1
	2	24A16	S2
	3	23A16	S3
12J38	4	25A16	S4
12J36	5	24A3	S5
12J34	6	25A3	S6
	7	24A20	S7
	8	23A20	S8
	9	11J5	Sc
2J1	10	15J1	K3'
2J2	11	15J2	K2'
2J3	12	15J3	K1'
2J4	13	15J4	L1'
2J5	14	15J5	L2'
2J6	15	15J6	L3'
2J7	16	15J7	L4'
2J8	17	15J8	L5'
2J9	18	18J18	O1'
2J10	19	18J19	O2'
2J11	20	18J20	O3'
15J12	21	7J19	Cpg
18A14	22	18J22	(Rf Tf)
	23	22E4L	+6
	24	18J23	0
	25	12J46	-12
	26		
	27		
	28		
	29		
	30		
	31		
	32		
12J15	33		B. Start
	34		
	35		
	36		
12J48	37		B. Stop

TYPE 15P No. 15J FUNCTION CONTROL PULSE OUT.

Origin	Pin No.	Dest.	Term
14J10	1	16J1	K3'
14J11	2	16J2	K2'
14J12	3	16J3	K1'
14J13	4	16J4	L1'
14J14	5	16J5	L2'
14J15	6	16J6	L3'
14J16	7	16J7	L4'
14J17	8	16J8	L5'
11J2	9		J25
	10		
	11		
16J12	12	14J21	Cpg
2J13	13	16J13	Gnd
2J14	14	16J14	+6
2J15	15	16J15	-12

TYPE 15P No. 16J FUNCTION CONTROL PULSE OUT.

Origin	Pin No.	Dest.	Term
15J1	1	17J1	K3'
15J2	2	17J2	K2'
15J3	3	17J3	K1'
15J4	4	18J13	L1'
15J5	5	18J14	L2'
15J6	6	18J15	L3'
15J7	7	18J16	L4'
15J8	8	18J17	L5'
11J1	9		J24
	10		
	11		
18J21	12	15J12	Cpg
15J13	13	24E3L	Gnd
15J14	14	22E4L	+6
15J15	15	23E5R	-12

TYPE 9P No. 17J FUNCTION SERIAL IN-OUT.

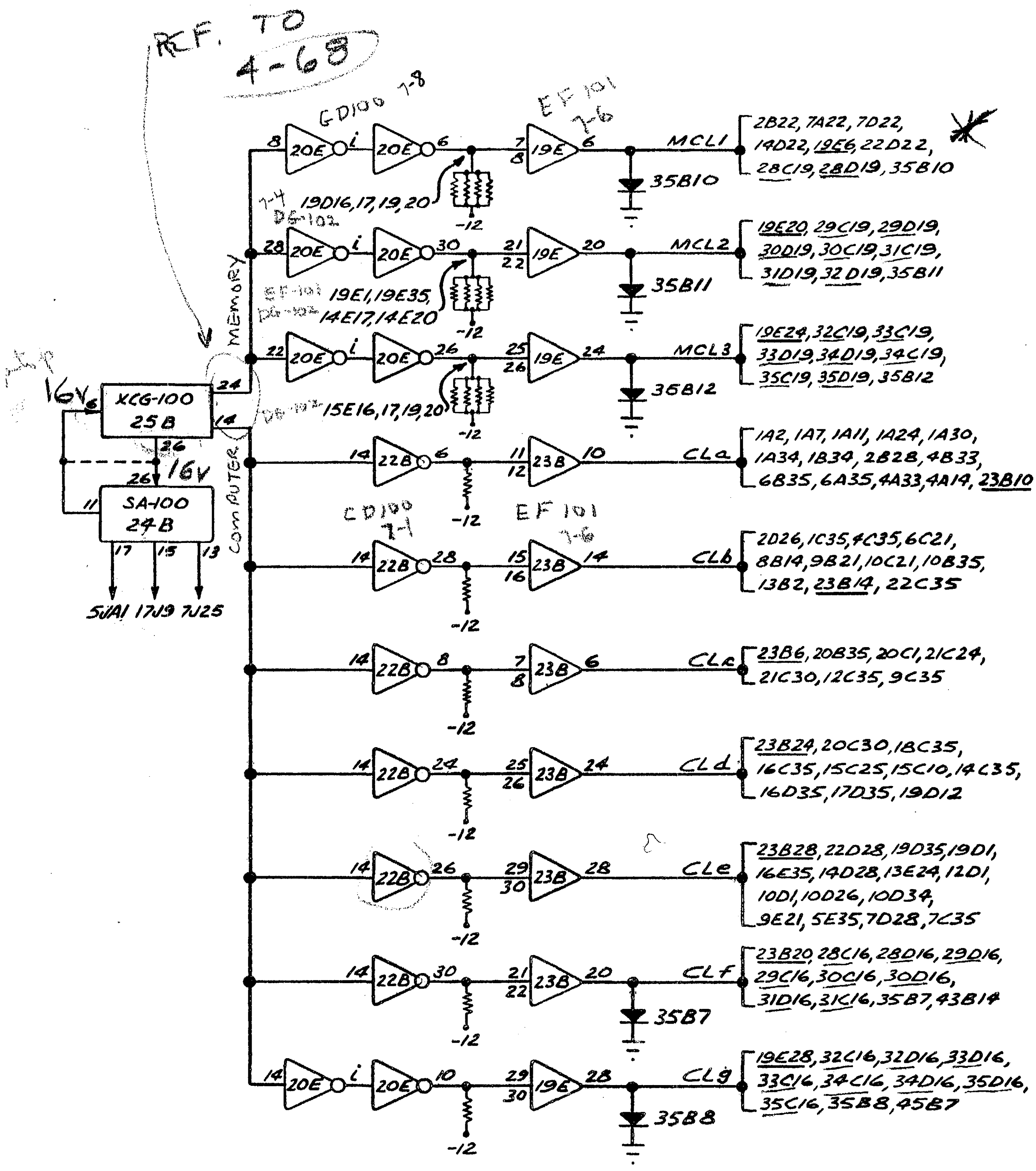
Origin	Pin No.	Dest.	Term
16J1	1		K3'
16J2	2		K2'
16J3	3		K1'
	4	20A30	Hsg
	5	14B7	Hdg
7J22	6		Shield
	7	27B19	Gsg
	8	35B19	Gdg
24B15	9		SA out 3

TYPE 37S No. 18J FUNCTION MAG. TAPE READER IN.

Origin	Pin No.	Dest.	Term
12J41	1	23A2	U1
	2	24A17	U2
	3	23A17	U3
12J39	4	25A17	U4
12J37	5	24A2	U5
	6	25A2	U6
	7	24A19	U7
	8	23A19	U8
	9	11J4	Uc
10J7	10		J22
10J8	11		J23
49B6	12		P24'
16J4	13		L1'
16J5	14		L2'
16J6	15		L3'
16J7	16		L4'
16J8	17		L5'
14J18	18		O1'
14J19	19		O2'
14J20	20		O3'
	21	16J12	Cpg
14J22	22		(Rf Tf)
14J24	23	18J24	0
18J23	24	18J25	0
18J24	25	12J44	0
2J12	26		Cog
11J3	27		J26
	28		
49B10	29		Sp'
	30		
	31		
	32		
12J16	33		B. Start
	34		
	35		
	36		
12J49	37		B. Stop

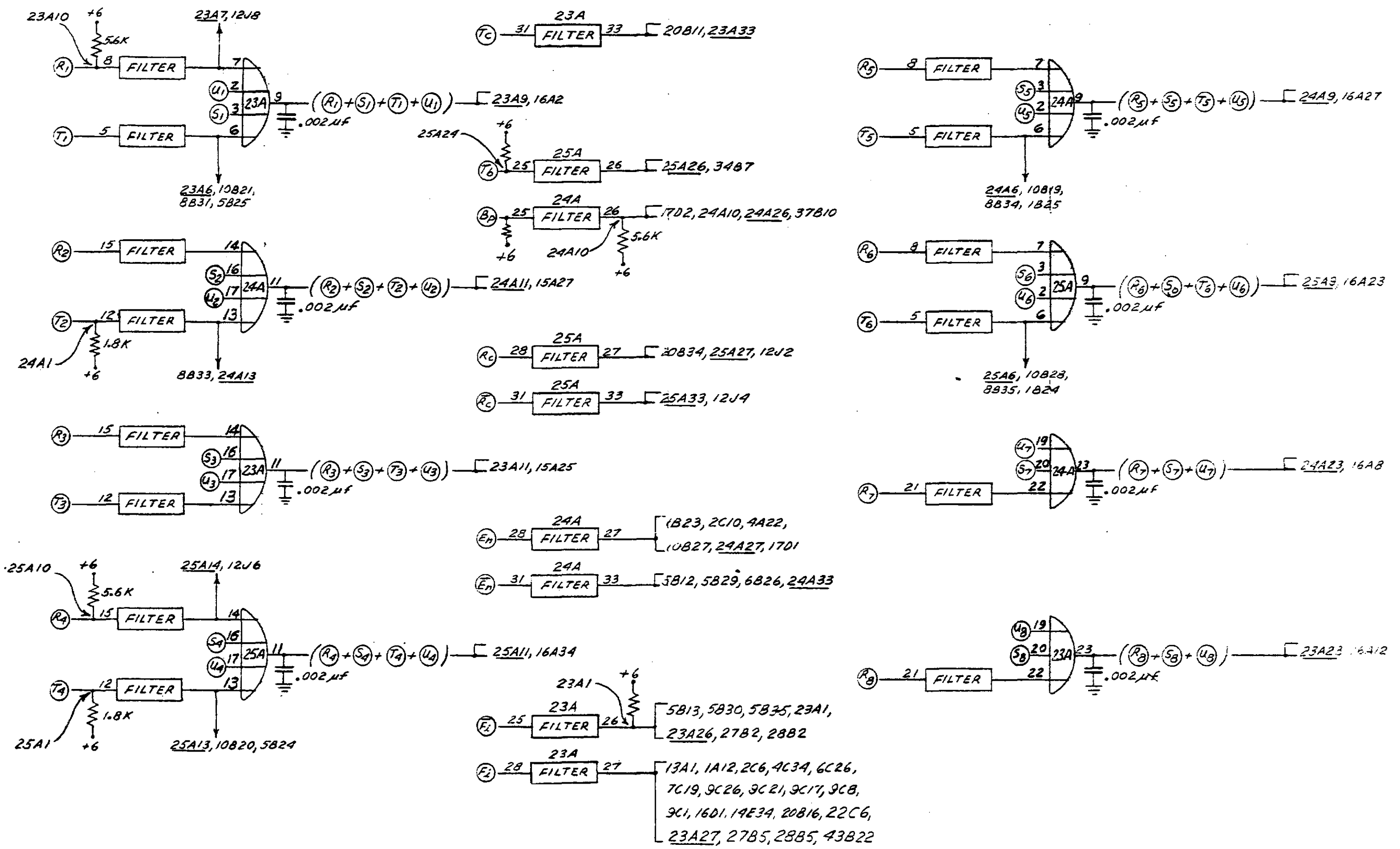
KOA-6-21-50PN-POS N PL 1	TERM	DCM 37S 1P
1	R1	8
2	R2	9
3	R3	10
4	R4	11
5	R5	12
6	R6	13
7	R7	14
8	R8	15
9	($Rf\ \overline{Tf}$)	19
10	Rc	16
11	($Rf\ \overline{Tf}$)	26
12	Rc	17
16	(En + $\overline{Rf}$ Tf)	18
17	T1	1
18	T2	2
19	T3	3
20	T4	4
21	T5	5
22	T6	6
23	Tc	7
24	(En + $\overline{Rf}$ Tf)	27
32	-12	24
33	Tb	20
34	En	21
35	-12	25
36	$\overline{En}$	22
37	Bp	23
38	-12	28
45		29
46		30
47		31

KOA-6-21-50PN POS Y PL 2	TERM	DBM 25 P 4P
1	LP1	9
2	LP2	10
3	LP3	11
4	LP4	12
5	LP5	13
6	LP6	14
7	LP7	15
8	LP8	16
9	LPC	8
10	-48V	21
11	LT1	2
12	LT2	3
13	LT3	4
14	LT4	5
15	LT5	6
16	LT6	7
19	LTC	1
20	-48V	24
21		
22	$L(\overline{Rf}\ Tf)$	18
23	-48V	25
24		
25		
26	LKL NEG.	22
27	NEG. OF INT. SUP.	23
28	$L(Rf\ \overline{Tf})$	17
46		19
47		20



LOGIC LAYOUT

LOGIC SECT. CLOCK DIST. TERM ______
DWG NO. 505782 T DATE 12-27-61
DRAWN BY M. Berman APP. ______
SH. 24

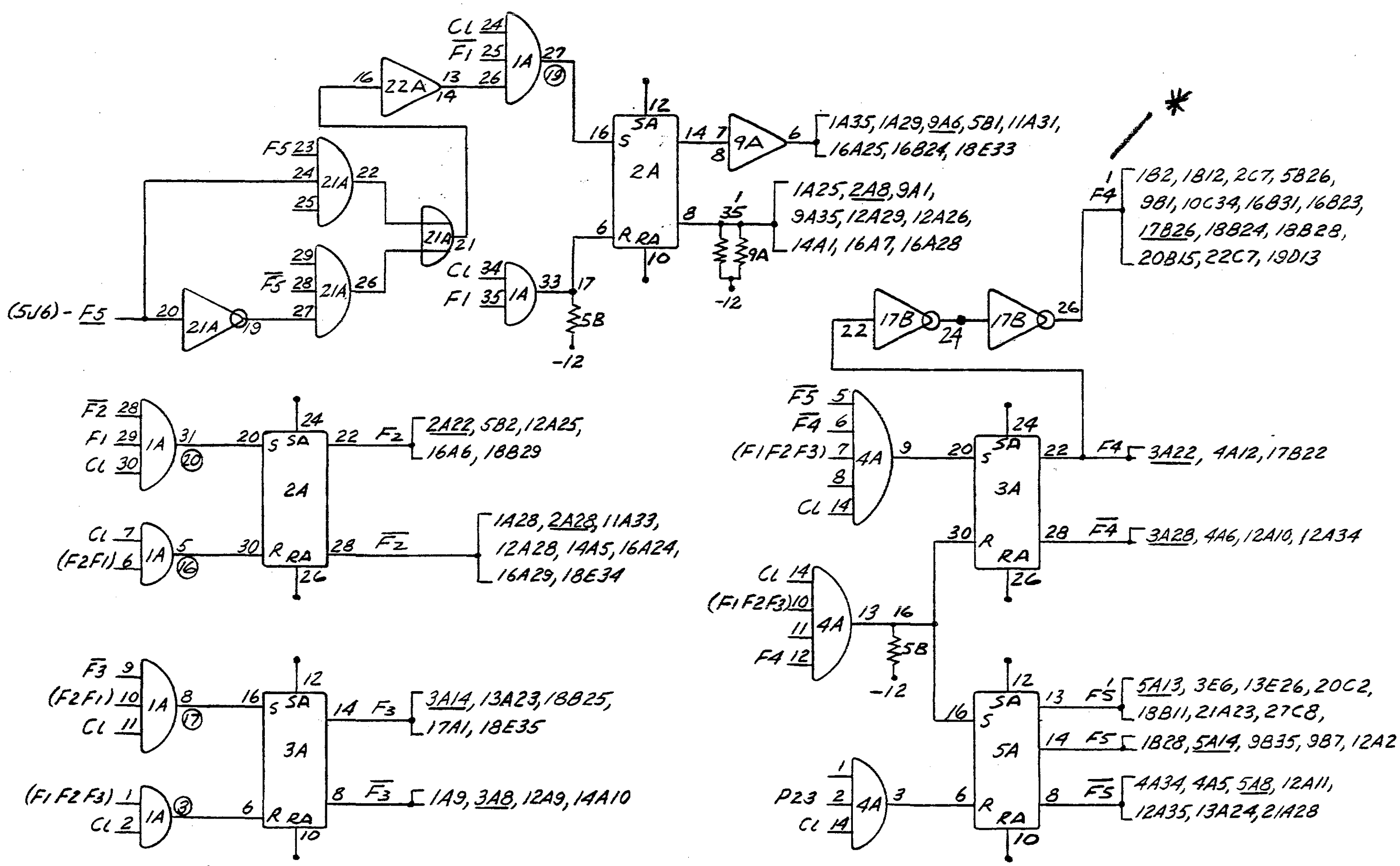


6-33

LOGIC LAYOUT

LOGIC SECT. CHAR. INPUT GATES TERM
DWG. NO. 505782 T DATE 1-10-62
DRAWN BY H. Hendelsohn APP

SH 25



$sF1 = \overline{F1}(\underline{F5}F5 + \overline{F5}\,\overline{F5})$

$rF1 = F1$

$sF2 = \overline{F2}F1$

$rF2 = F2F1$

$sF3 = \overline{F3}F2F1$

$rF3 = F3F2F1$

$sF4 = \overline{F5}\,\overline{F4}F3F2F1$

$rF4 = F4F3F2F1$

$sF5 = F4F3F2F1$

$rF5 = P23$

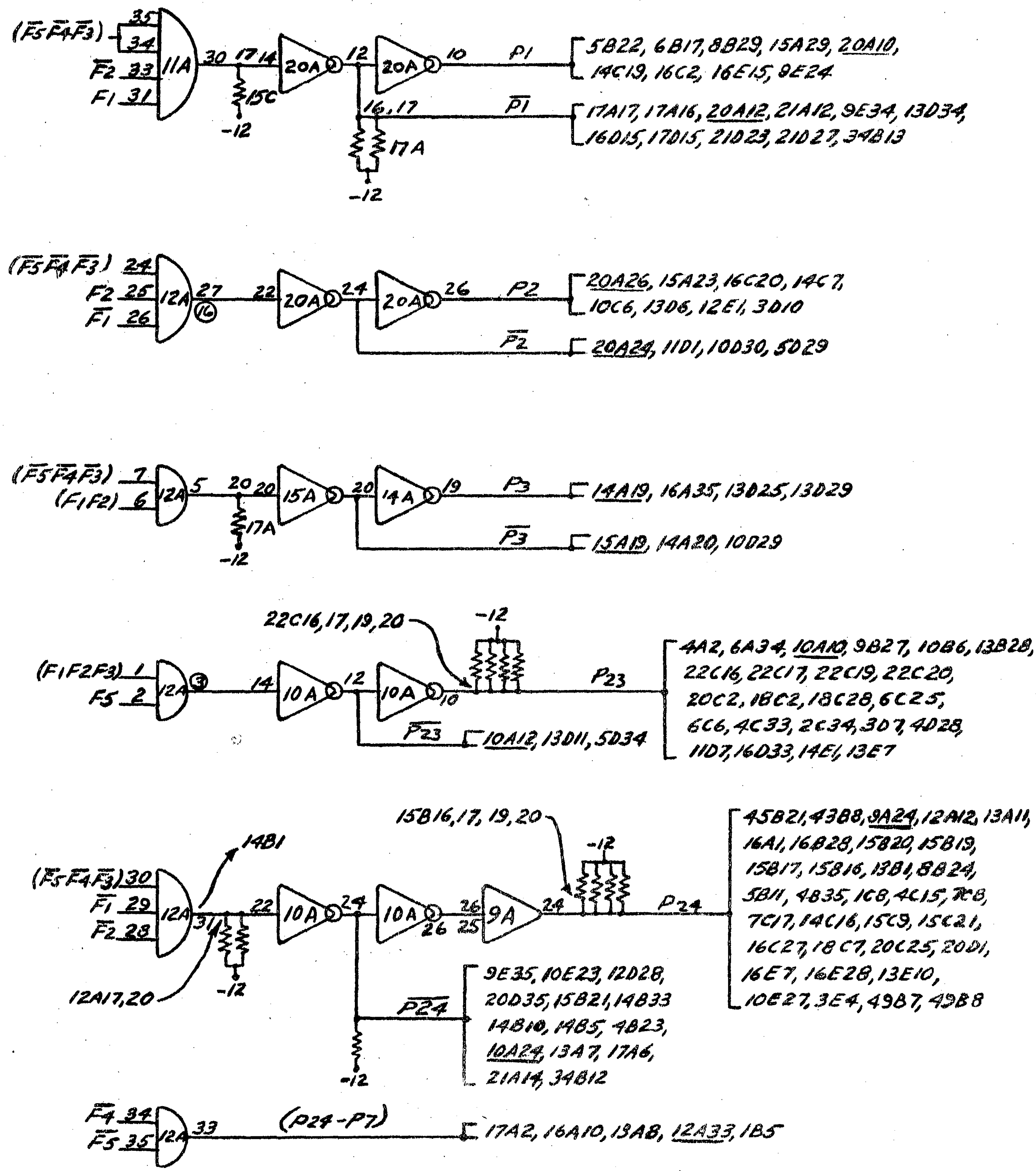
LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTER TERM ______

DWG. NO. 505782 T DATE 1-8-62

DRAWN BY H. Mendelsohn APP. ______

SH. 26



$P1 = \bar{F5}\bar{F4}\bar{F3}\bar{F2}F1$ $P23 = F5F3F2F1$

$P2 = \bar{F5}\bar{F4}\bar{F3}F2\bar{F1}$ $P24 = \bar{F5}\bar{F4}\bar{F3}\bar{F2}\bar{F1}$

$P3 = \bar{F5}F4\bar{F3}F2F1$ $(P24-P7) = \bar{F5}\bar{F4}$

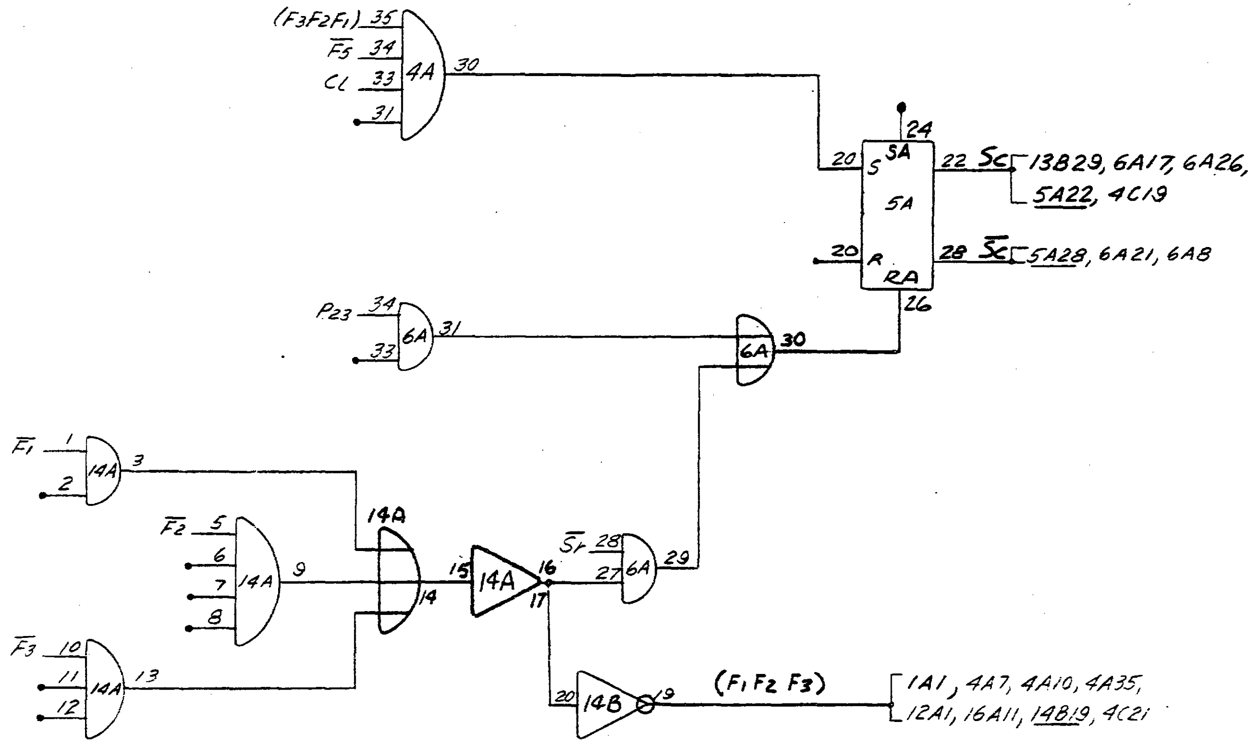
LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTER TERM ______

DWG. NO. 505 7E2 T DATE 1-8-62

DRAWN BY H. Mendelsohn APP ______

SH. 27



$sSc = \overline{F_5}F_3F_2F_1$

$rSc = P_{23} + \overline{S_r}(\overline{F_3} + \overline{F_2} + \overline{F_1})$

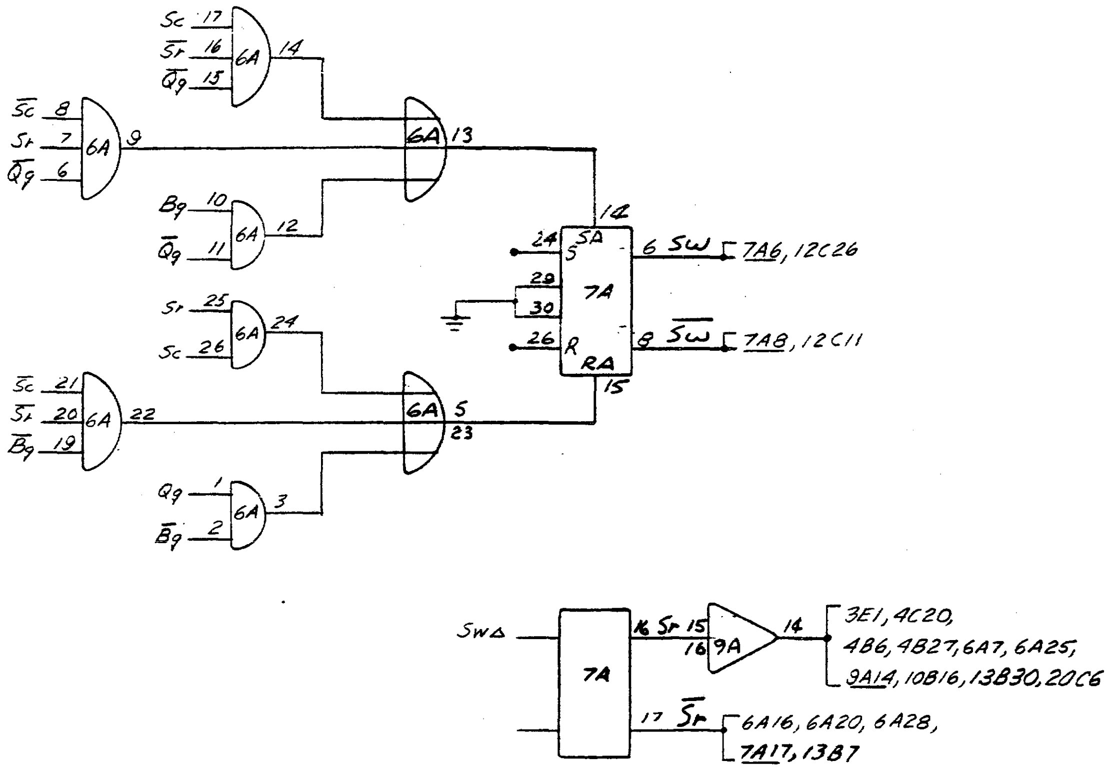
LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTERS TERM. $(F_1F_2F_3)$, Sc

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. [illegible] APP. ______

SH. 28



$sSw = Sc\,\overline{Sr}\,\overline{Q_9} + \overline{Sc}\,Sr\,\overline{Q_9} + B_9\overline{Q_9}$

$rSw = Sc\,Sr + \overline{Sc}\,\overline{Sr}\,\overline{B_9} + Q_9\overline{B_9}$

sSr = Sw DELAYED 22 PULSE TIMES

rSr = $\overline{Sw}$ DELAYED 22 PULSE TIMES

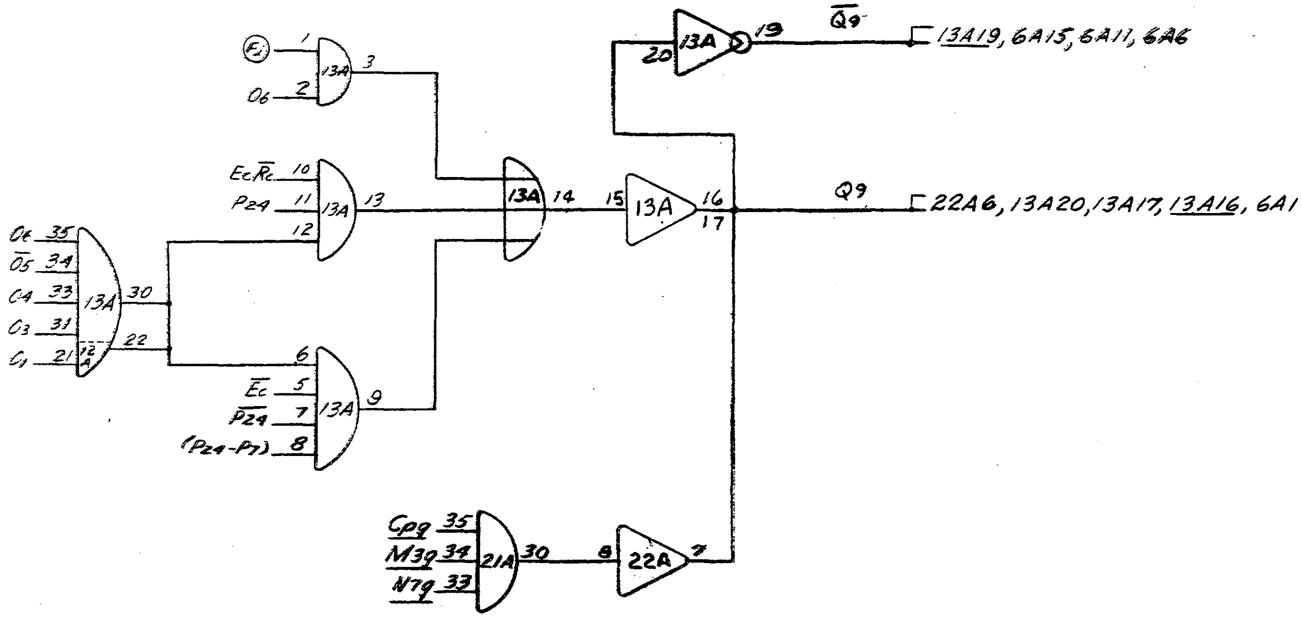
LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTERS TERM Sw & Sr

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. [illegible] APP.

SH. 29



$$Q_9 = \bar{E}_c O_6 \bar{O}_5 O_4 O_3 O_1 \bar{P}_{24} (P_{24} - P_7) + F_i O_6 + \underline{Cp_9}\ \underline{M_{39}}\ \underline{N_{79}} + E_c \bar{R}_c O_6 \bar{O}_5 O_4 O_3 O_1 P_{24}$$

$$\bar{Q}_9 = (\bar{Q}_9)$$

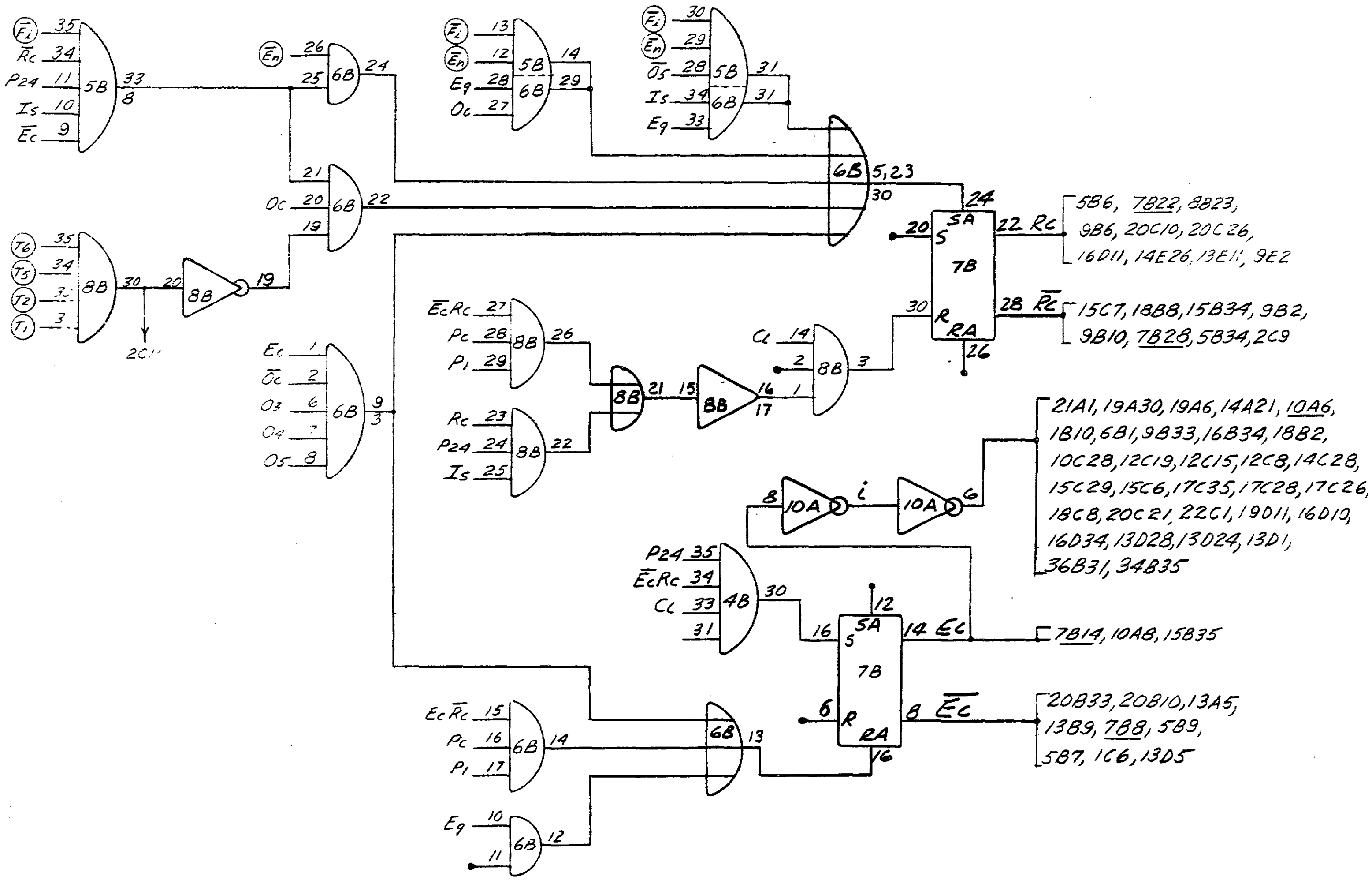
LOGIC LAYOUT

LOGIC SECT. P. & S. COUNTERS TERM. Q9

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. [illegible] APP.

SH. 30



$sE_c = P_{24}\bar{E}_cR_c$

$rE_c = E_q + E_cO_5O_4O_3\bar{O}_c + E_c\bar{R}_cP_cP_1$

$sR_c = \bar{E}_n\bar{F}_iE_qO_c + \bar{E}_n\bar{F}_iE_q\bar{O}_5I_s + P_{24}\bar{E}_c\bar{R}_cI_s(\bar{E}_n + O_c\overline{T_6T_5T_2T_1})\bar{F}_i + E_cO_5O_4O_3\bar{O}_c$

$rR_c = P_{24}R_cI_s + \bar{E}_cR_cP_cP_1$

LOGIC LAYOUT

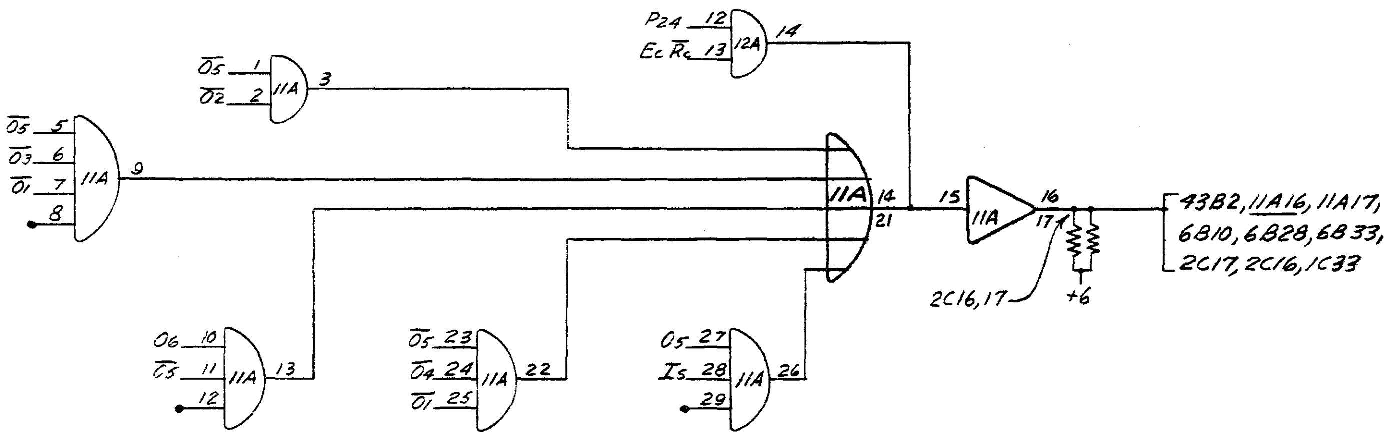
LOGIC SECT. INST. REG. & CONT. TERM E_c & R_c

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 31

6-40



$$E_9 = P24\,E_c\overline{R_c}(\overline{O_5}\,\overline{O_2} + \overline{O_5}O_6 + \overline{O_5}\,\overline{O_3}\,\overline{O_1} + \overline{O_5}\,\overline{O_4}\,\overline{O_1} + O_5 I_5)$$

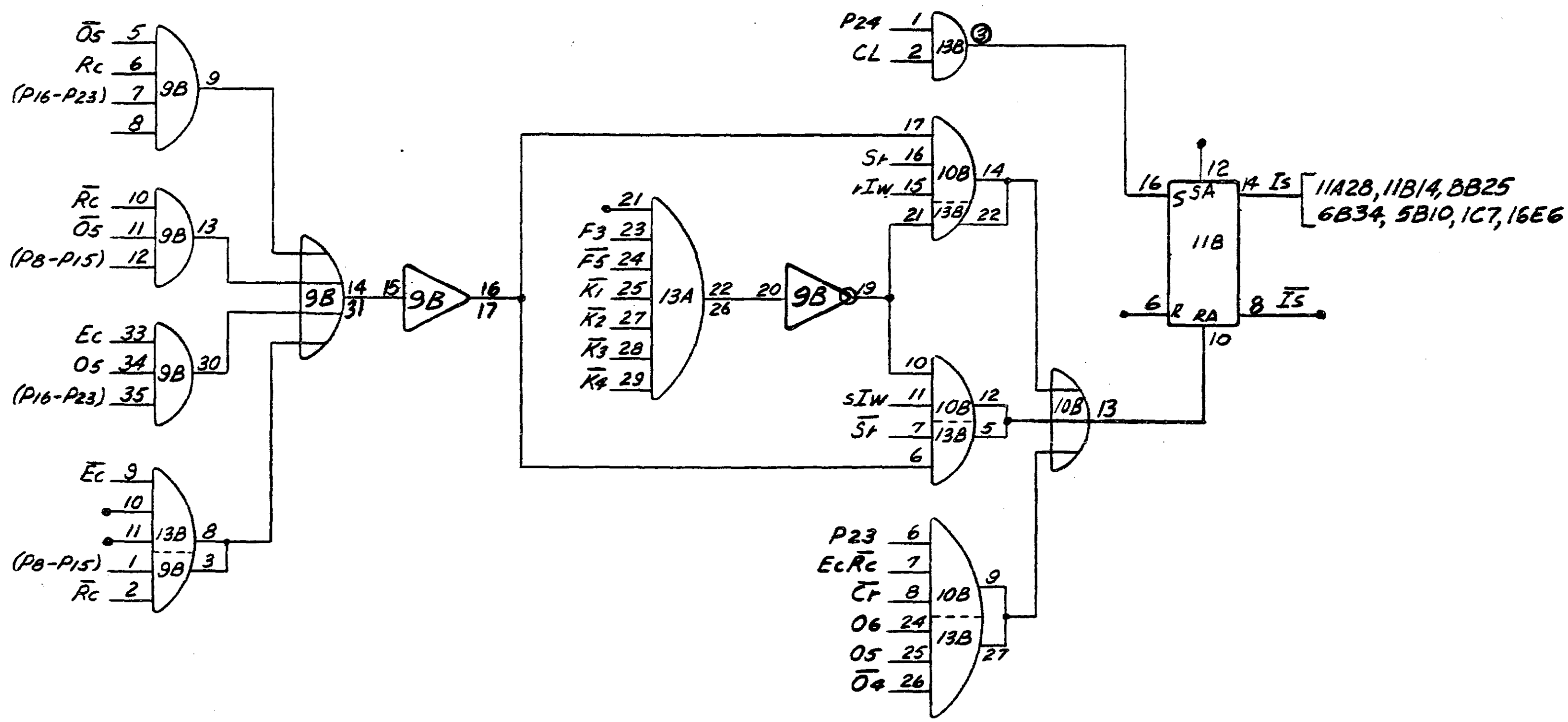
LOGIC LAYOUT

LOGIC SECT. INST. REG. & CONT. TERM E_9

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ____

SH. 32



$sI_s = P_{24}$

$rI_s = (\bar{S}_r\, sI_w + S_r\, rI_w)[\bar{E}_c\bar{R}_c(P_8-P_{15}) + \bar{O}_5 R_c(P_{16}-P_{23}) + \bar{R}_c\bar{O}_5(P_8-P_{15}) + E_c O_5(P_{16}-P_{23})]\overline{[K_4K_3K_2K_1F_5F_3]} + P_{23}E_c\bar{R}_c O_6 O_5 \bar{O}_4 \bar{C}_r$

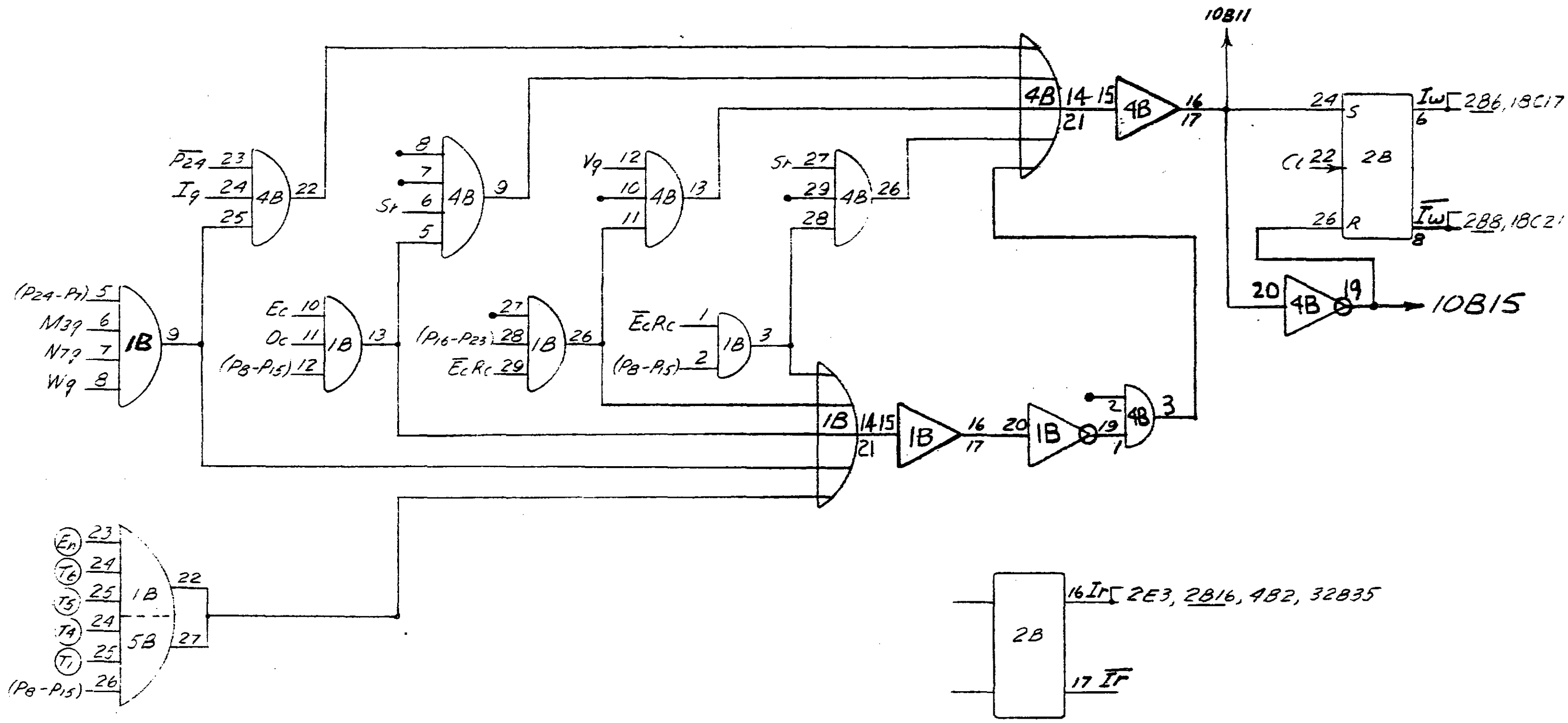
LOGIC LAYOUT

LOGIC SECT. INST. REG. & CONT. TERM I_s

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ______

SH. 33



$$sI_w = \bar{E}_c R_c (P_8 - P_{15}) S_r + \bar{E}_c R_c (P_{16} - P_{23}) V_q + E_c O_c (P_8 - P_{15}) S_r + \overline{P_{24}} (P_{24} - P_7) M_{3q} N_{7q} W_q I_q$$

$$+ I_r \left[\overline{\bar{E}_c R_c (P_8 - P_{15}) + \bar{E}_c R_c (P_{16} - P_{23}) + E_c O_c (P_8 - P_{15})} \right.$$

$$\left. \overline{+ (P_{24} - P_7) M_{3q} N_{7q} W_q + E_n T_6 T_5 T_4 T_1 (P_8 - P_{15})} \right]$$

$$rI_w = (\overline{sI_w})$$

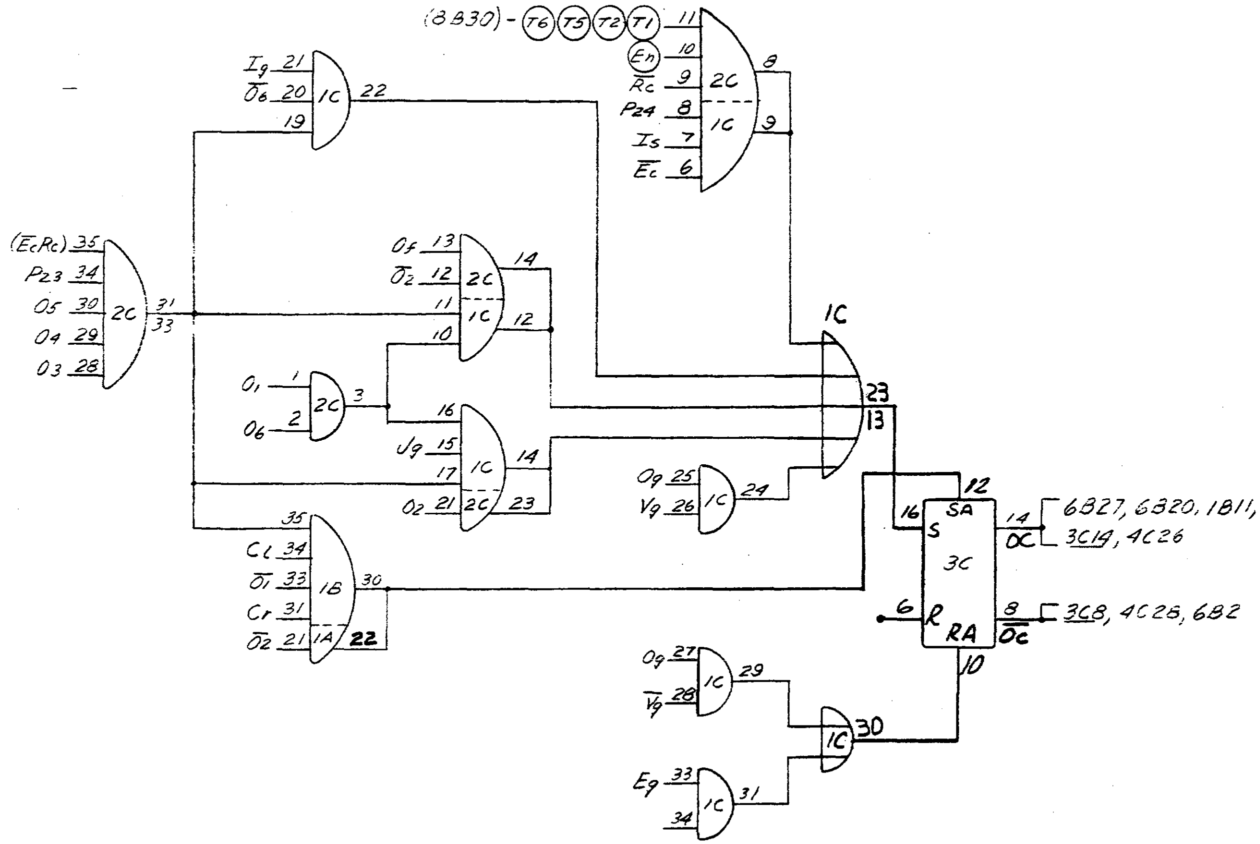
LOGIC LAYOUT

LOGIC SECT. INST. REG. & CONT. TERM. I_w & I_r

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. [illegible] APP.

SH 34



$sO_c = O_9V_9 + (E_n)P_{24}I_s\overline{E_c}\overline{R_c}(T6)(T5)(T2)(T1)$

$+ P_{23}\overline{E_c}R_cO_5O_4O_3(\overline{O_6}I_9 + O_6\overline{O_2}O_1O_4 + O_6O_2O_1J_9 + \overline{O_2}\overline{O_1}C_r)$

$rO_c = O_9\overline{V_9} + E_9$

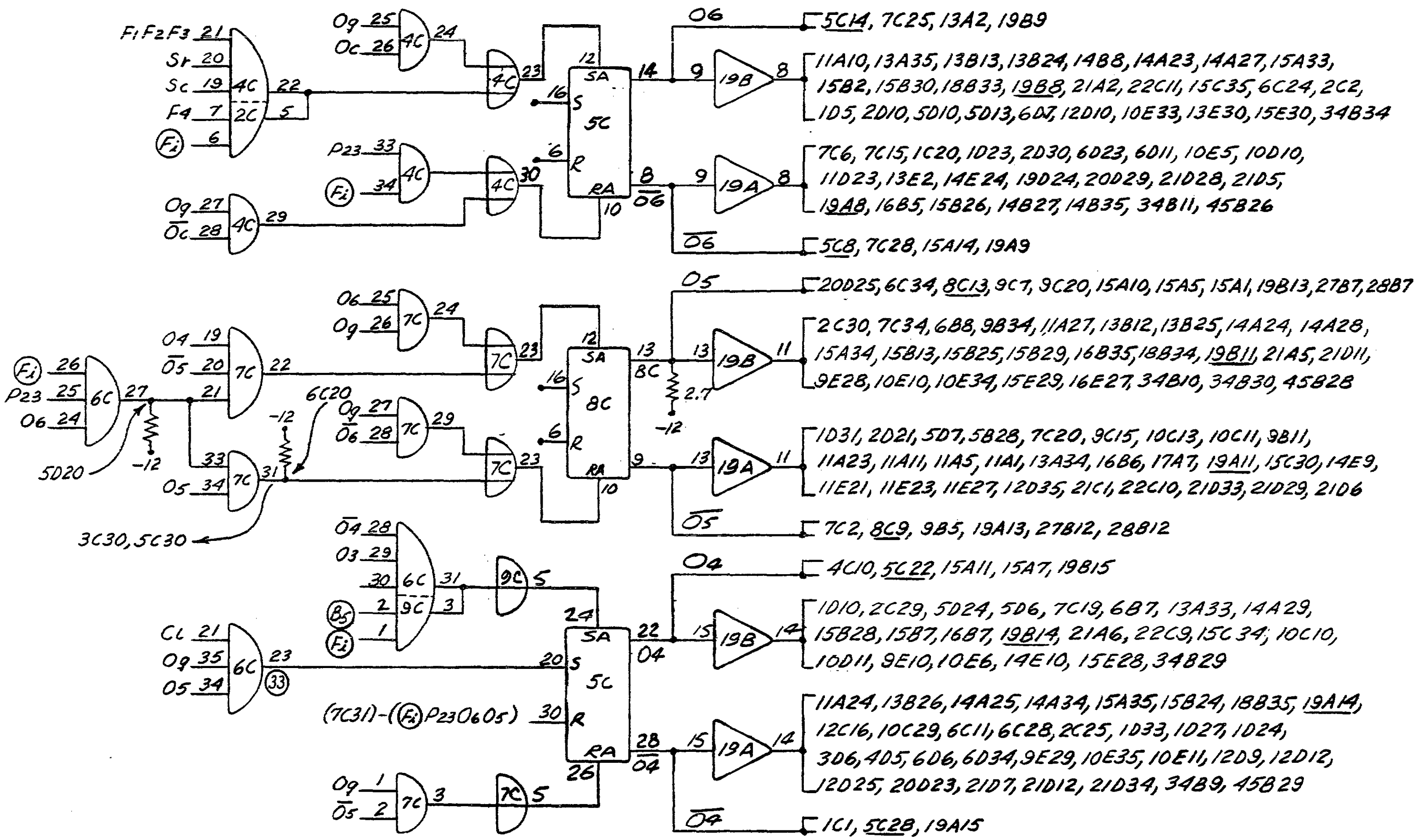
LOGIC LAYOUT

LOGIC SECT. OP. CODE REG. TERM O_c

DWG. NO. 5D5782 T DATE 1-6-62

DRAWN BY H. Hilliard [illegible] APP. ____

SH. 35



$sO6 = O9\,Oc + (Fi)\,F4F3F2F1\,Sr\,Sc$

$rO6 = (Fi)\,P23 + O9\,\overline{Oc}$

$sO5 = O9\,O6 + (Fi)\,P23\,O6\,\overline{O5}\,O4$

$rO5 = (Fi)\,P23\,O6\,O5 + O9\,\overline{O6}$

$sO4 = O9\,O5 + (Fi)(Bs)\,\overline{O4}\,O3$

$rO4 = (Fi)\,P23\,O6\,O5 + O9\,\overline{O5}$

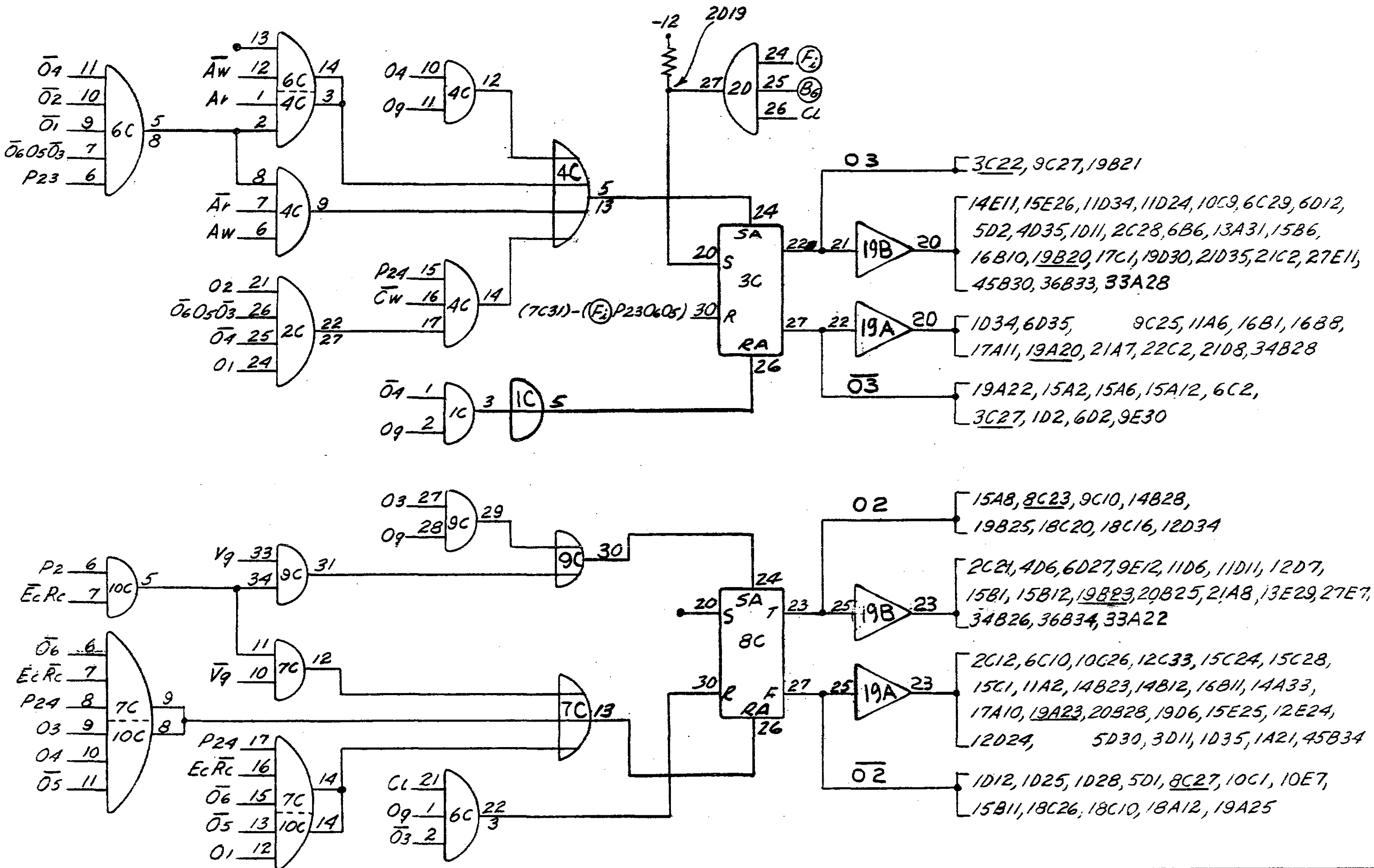
LOGIC LAYOUT

LOGIC SECT. OP. CODE REG. TERM O6, O5, O4

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 36



$sO3 = O_9O_4 + P_{23}\bar{O}_6O_5\bar{O}_4\bar{O}_3\bar{O}_2\bar{O}_1(A_w\bar{A}_r + \bar{A}_wA_r) + P_{24}\bar{O}_6O_5\bar{O}_4\bar{O}_3O_2O_1\bar{C}_w + F_i\,B_6$

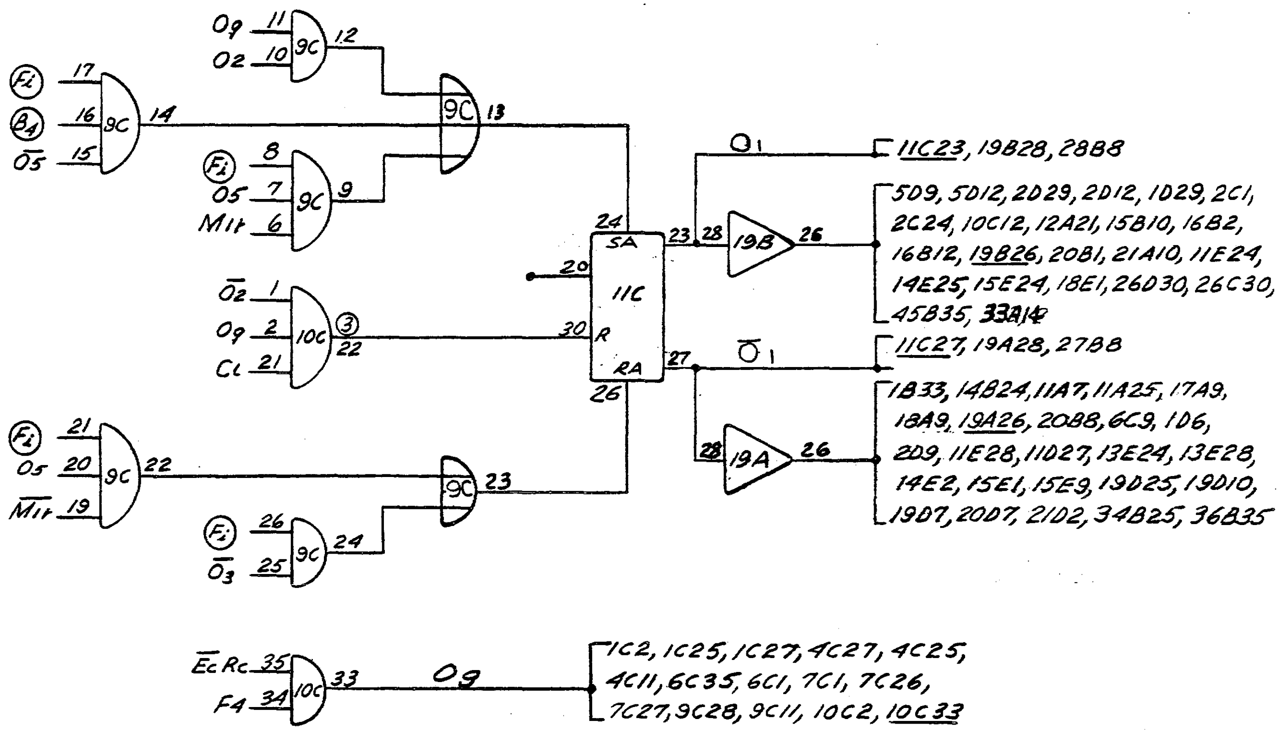
$rO3 = O_9\bar{O}_4 + F_i\,P_{23}O_6O_5$

$sO2 = O_9O_3 + \bar{E}_cR_cP_2V_9$

$rO2 = O_9\bar{O}_3 + P_{24}E_c\bar{R}_c\bar{O}_6\bar{O}_5O_1 + P_{24}E_c\bar{R}_c\bar{O}_6\bar{O}_5O_4O_3 + \bar{E}_cR_cP_2\bar{V}_9$

LOGIC LAYOUT

LOGIC SECT. OP. CODE REG. TERM O3, O2
DWG. NO. 505782 T DATE 1-6-62
DRAWN BY H. Mendelsohn APP.



$sO_1 = O_9 O_2 + F_i B_4 \bar{O}_5 + F_i O_5 M_{1+}$

$rO_1 = O_9 \bar{O}_2 + F_i \bar{O}_3 + F_i O_5 \overline{M_{1+}}$

$O_9 = \bar{E}_c R_c F4$

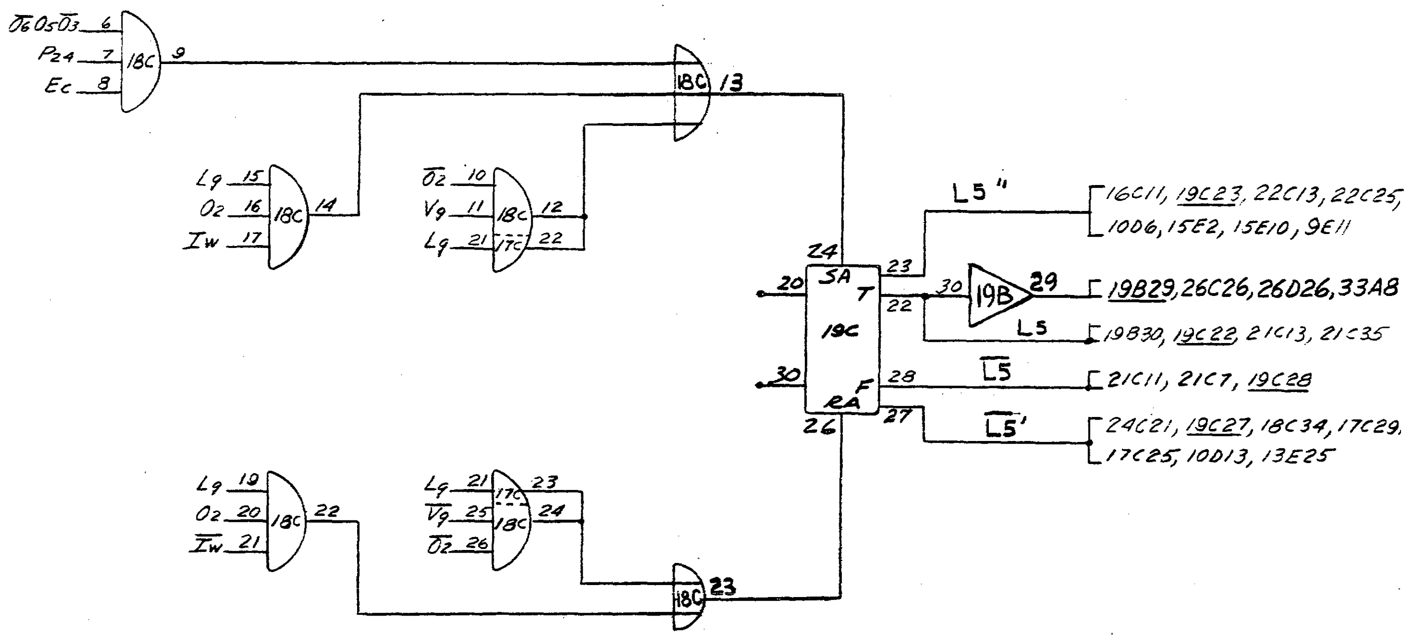
LOGIC LAYOUT

LOGIC SECT. OP. CODE REG. TERM O_1, O_9

DWG. NO. 505782 T DATE 1-6-62

DWN. BY H. Mendelsohn APP.

SH. 38



$$sL5 = L_9 \bar{O}_2 V_9 + L_9 O_2 I_w + \bar{O}_6 O_5 \bar{O}_3 P_{24} E_c$$

$$rL5 = L_9 \bar{O}_2 \bar{V}_9 + L_9 O_2 \bar{I}_w$$

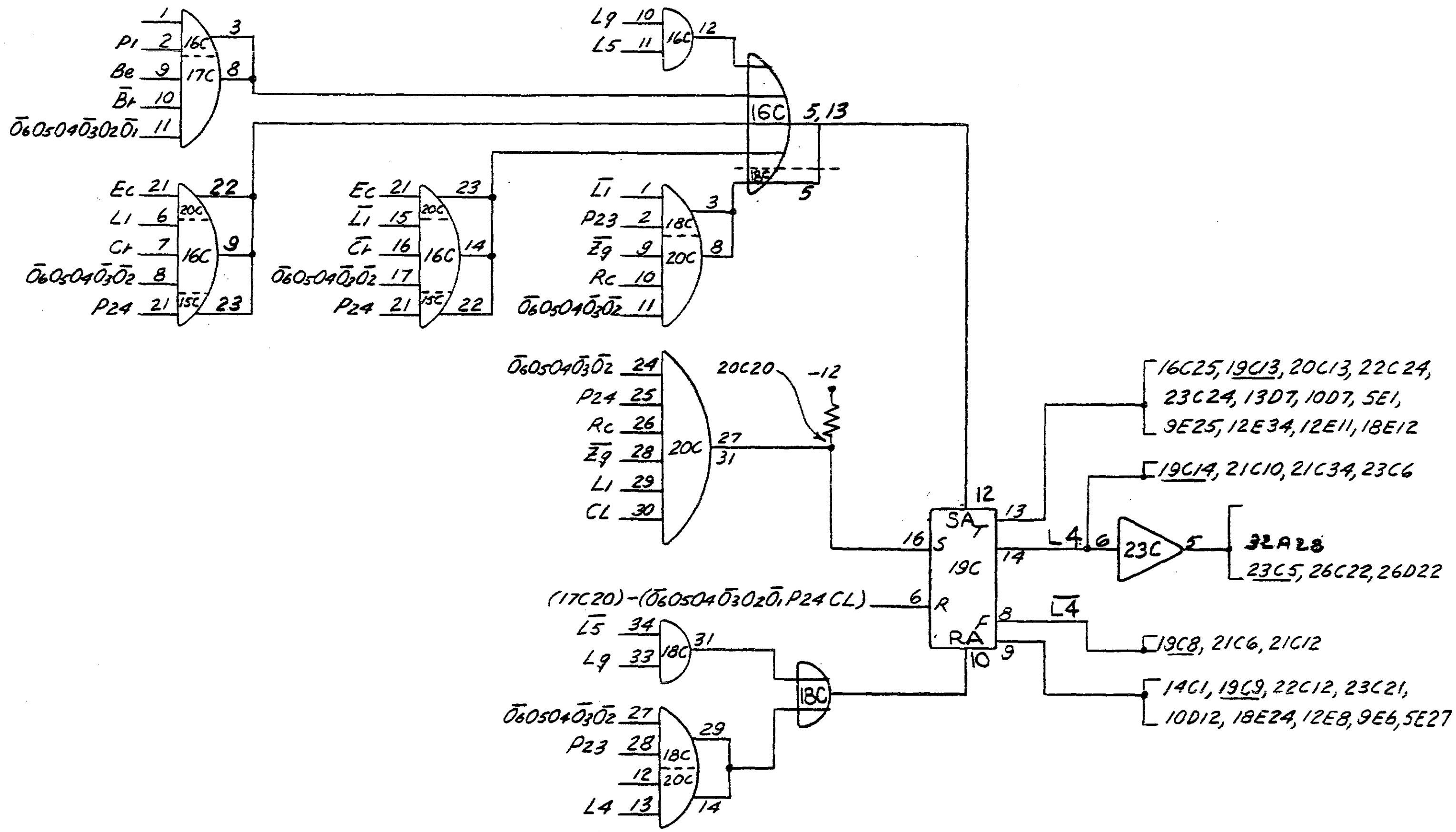
LOGIC LAYOUT

LOGIC SECT. CP. LINE SEL. TERM L5

DWG. NO. 505782T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ____

SH. 39



$$sL4 = L_9 L_5 + \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 [P24\, E_c (L_1 C_r + \bar{L}_1 \bar{C}_r) + P23\, R_c \bar{L}_1 \bar{Z}_9 + P24\, R_c L_1 \bar{Z}_9] + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 P_1 B_e \bar{B}_r$$

$$rL4 = L_9 \bar{L}_5 + \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 P23\, L4 + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 P24$$

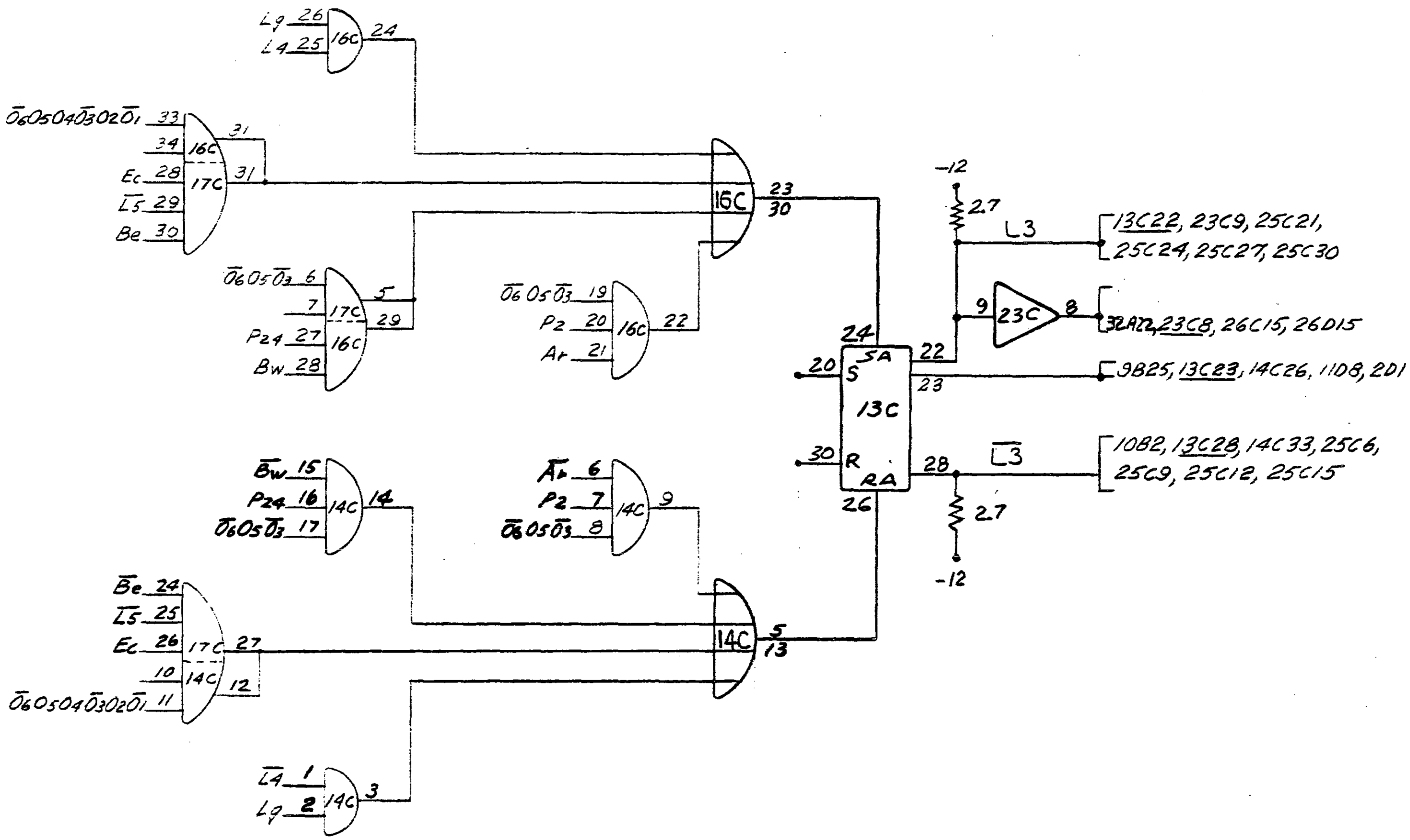
LOGIC LAYOUT

LOGIC SECT. OP. LINE SEL. TERM L4

DWG. NO. 505782T DATE 1-9-62

DRAWN BY H. Mendelsohn APP. ________

SH. 40



$$sL3 = L_9 L_4 + \overline{O}_6 O_5 \overline{O}_3 (P_{24} B_w + P_2 A_r) + \overline{O}_6 O_5 O_4 \overline{O}_3 O_2 \overline{O}_1 E_c \overline{L}_5 B_e$$

$$rL3 = L_9 \overline{L}_4 + \overline{O}_6 O_5 \overline{O}_3 (P_{24} \overline{B}_w + P_2 \overline{A}_r) + \overline{O}_6 O_5 O_4 \overline{O}_3 O_2 \overline{O}_1 E_c \overline{L}_5 \overline{B}_e$$

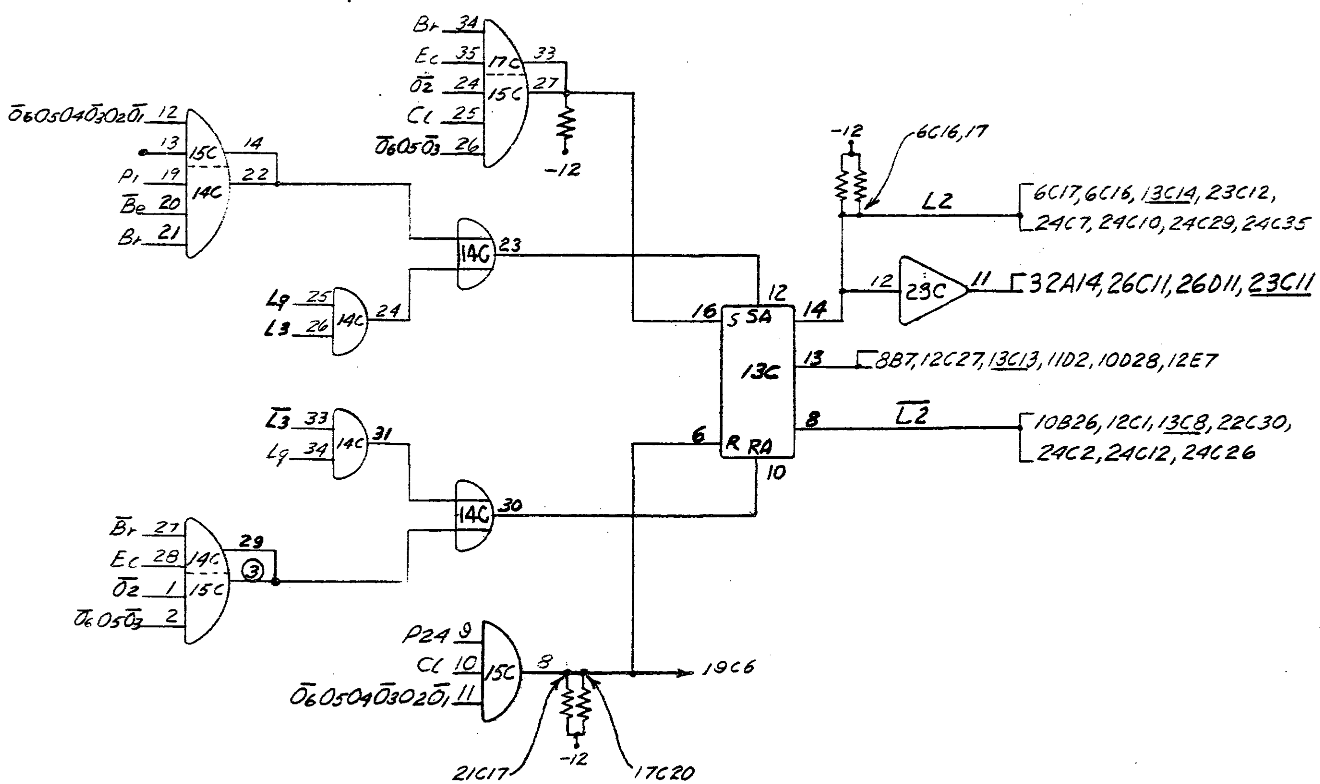
LOGIC LAYOUT

LOGIC SECT. OR. LINE SEL. TERM L3

DWG. NO. 505782T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 41



$$sL2 = L_9 L_3 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c B_r + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 \bar{B}_e B_r P_1$$

$$rL2 = L_9 \bar{L}_3 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c \bar{B}_r + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 P24$$

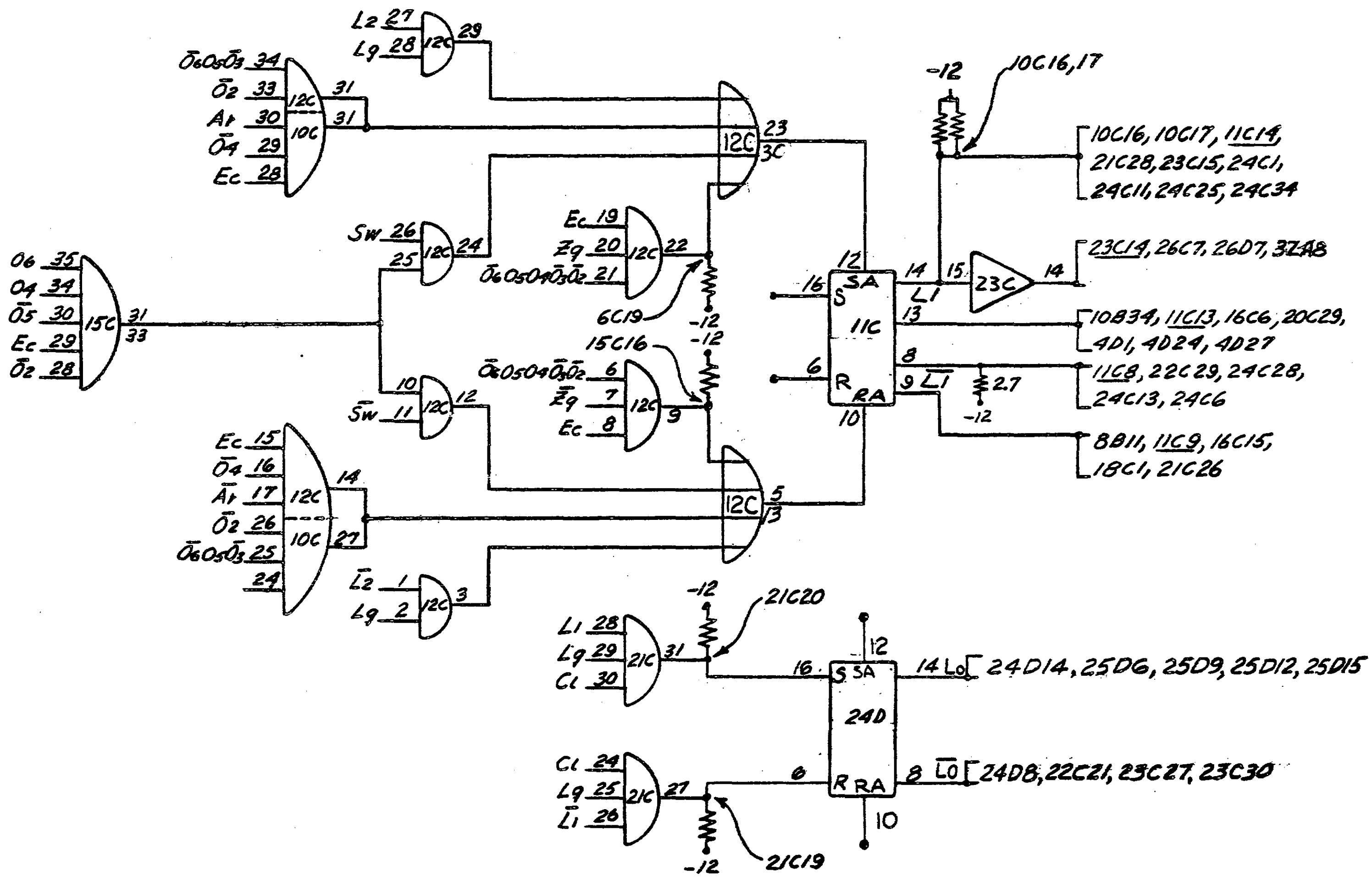
LOGIC LAYOUT

LOGIC SECT. OP. LINE SEL. TERM L2

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Wiendelsohn APP. ______

SH. 42



$sL_0 = L_1 L_g$

$rL_0 = \bar{L}_1 L_g$

$sL_1 = L_g L_2 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c (\bar{Z}_g O_4 + A_1 \bar{O}_4) + O_6 \bar{O}_5 O_4 \bar{O}_2 E_c S_w$

$rL_1 = L_g \bar{L}_2 + \bar{O}_6 O_5 \bar{O}_3 \bar{O}_2 E_c (\bar{Z}_g O_4 + \bar{A}_1 \bar{O}_4) + O_6 \bar{O}_5 O_4 \bar{O}_2 E_c \bar{S}_w$

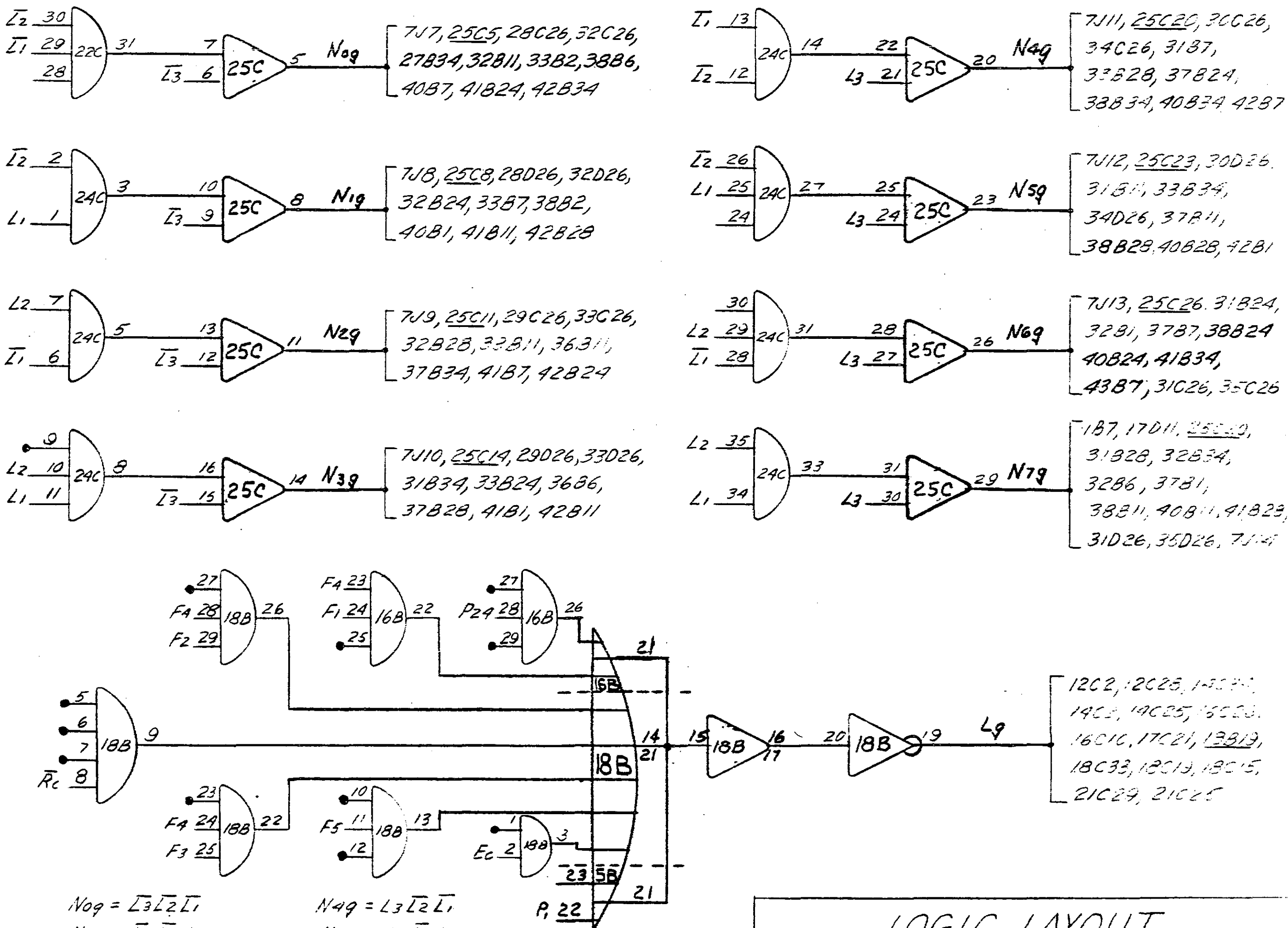
LOGIC LAYOUT

LOGIC SECT. OP LINE SEL. TERM L_1, L_0

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY [signature] APP. ____

SH. 43



$N_{0q} = \bar{L}_3\bar{L}_2\bar{L}_1$ $N_{4q} = L_3\bar{L}_2\bar{L}_1$

$N_{1q} = \bar{L}_3\bar{L}_2 L_1$ $N_{5q} = L_3\bar{L}_2 L_1$

$N_{2q} = \bar{L}_3 L_2\bar{L}_1$ $N_{6q} = L_3 L_2\bar{L}_1$

$N_{3q} = \bar{L}_3 L_2 L_1$ $N_{7q} = L_3 L_2 L_1$

$$L_q = \overline{E_c + \bar{R}_c + F_5 + F_4F_3 + F_4F_2 + F_4F_1 + P_{24} + P_1}$$

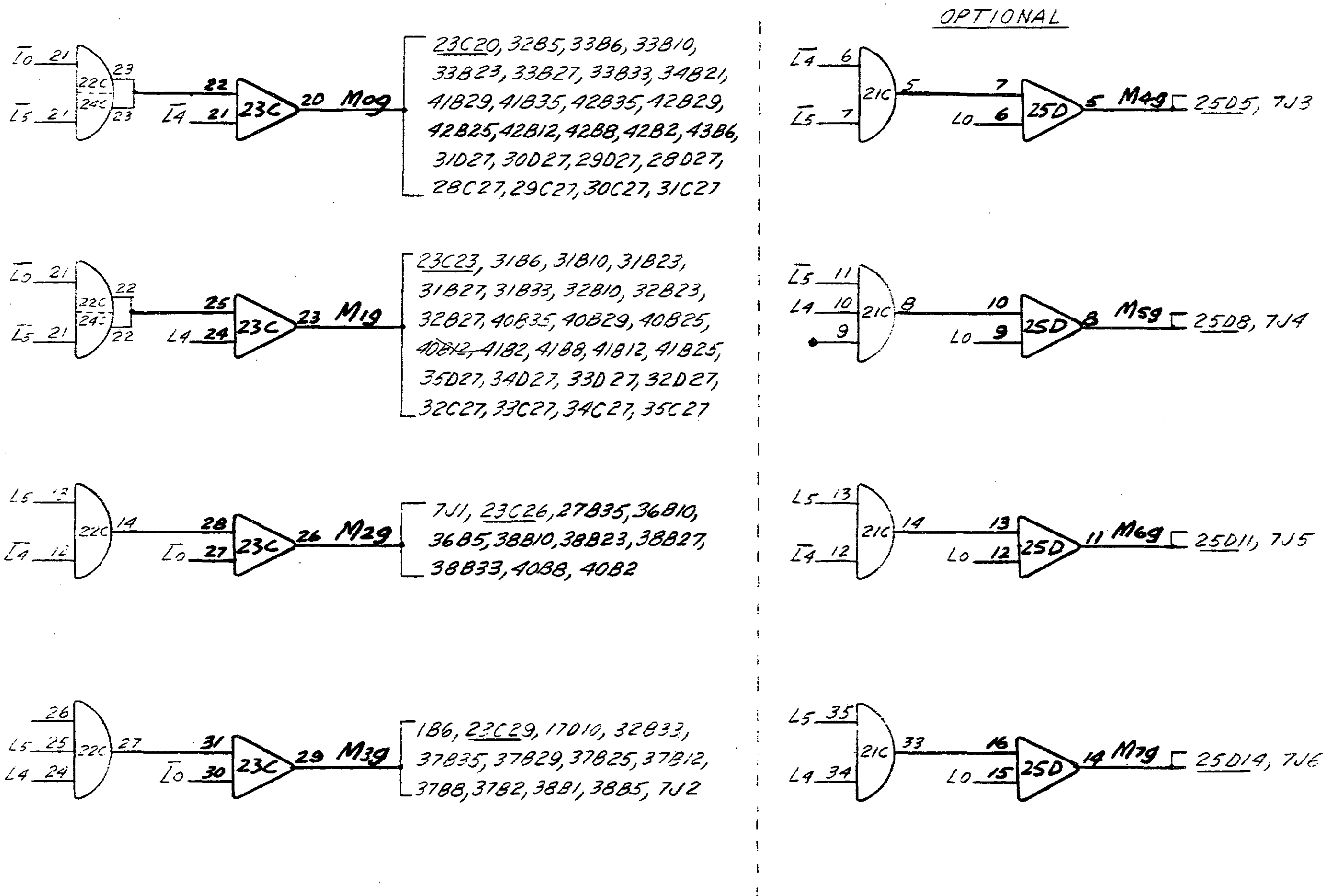
LOGIC LAYOUT

LOGIC SECT. OP. LINE SEL. TERM L_q & N_{0q}-N_{7q}

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 44



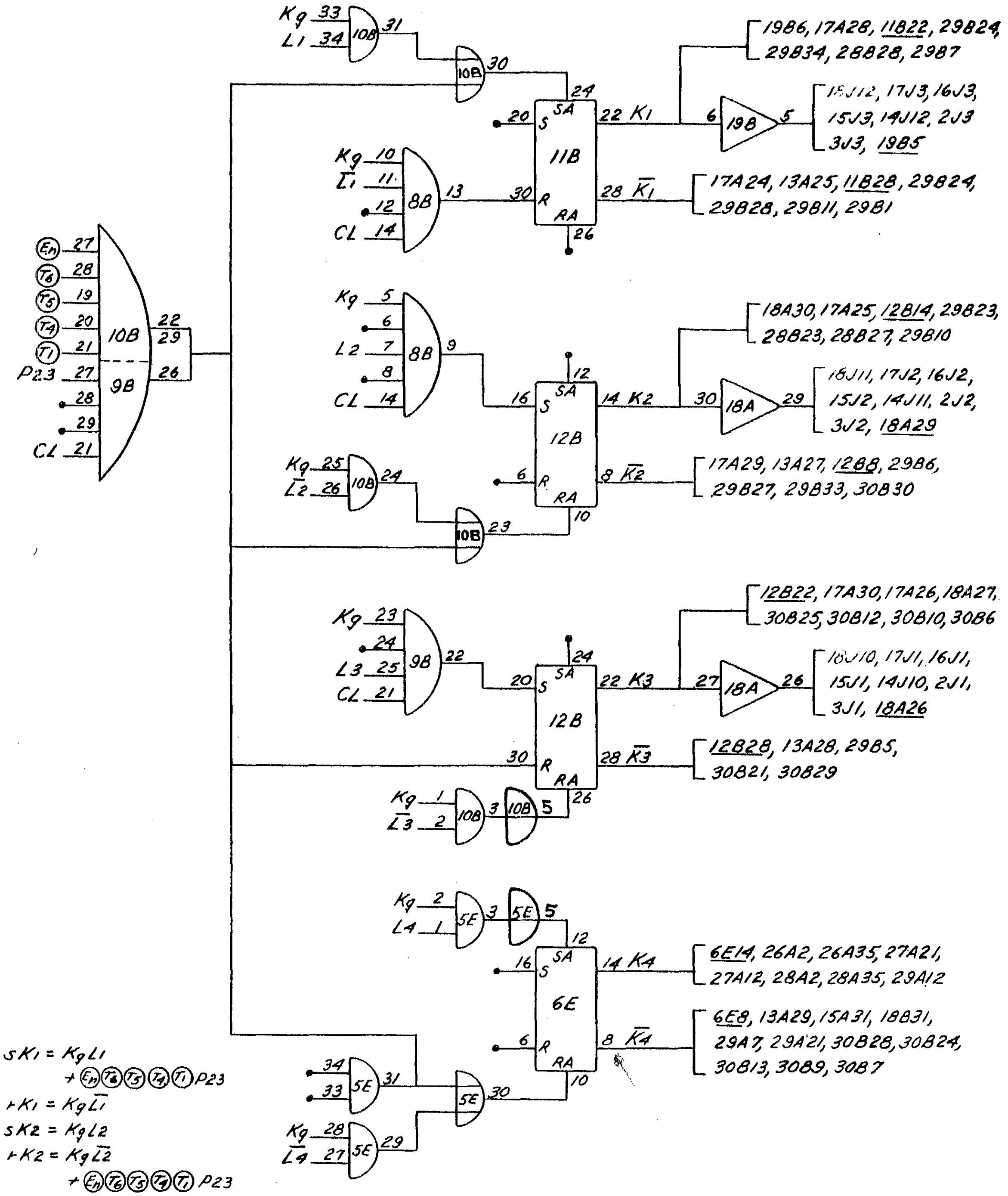
$M_{0g} = \bar{L}_0 \bar{L}_5 \bar{L}_4$
$M_{1g} = \bar{L}_0 \bar{L}_5 L_4$
$M_{2g} = \bar{L}_0 L_5 \bar{L}_4$
$M_{3g} = \bar{L}_0 L_5 L_4$

$M_{4g} = L_0 \bar{L}_5 \bar{L}_4$
$M_{5g} = L_0 \bar{L}_5 L_4$
$M_{6g} = L_0 L_5 \bar{L}_4$
$M_{7g} = L_0 L_5 L_4$

LOGIC LAYOUT

LOGIC SECT. OP. LINE SEL. TERM M_{0g} – M_{7g}
DWG. NO. 505782 T DATE 1-6-62
DRAWN BY H. Mendelsohn APP. ________

SH. 45



$sK_1 = K_9 L_1$
$\quad + (E_n)(T_6)(T_5)(T_4)(T_1) P23$
$rK_1 = K_9 \bar{L_1}$
$sK_2 = K_9 L_2$
$rK_2 = K_9 \bar{L_2}$
$\quad + (E_n)(T_6)(T_5)(T_4)(T_1) P23$
$sK_3 = K_9 L_3$
$rK_3 = K_9 \bar{L_3} + (E_n)(T_6)(T_5)(T_4)(T_1) P23$
$sK_4 = K_9 L_4$
$rK_4 = K_9 \bar{L_4} + (E_n)(T_6)(T_5)(T_4)(T_1) P23$

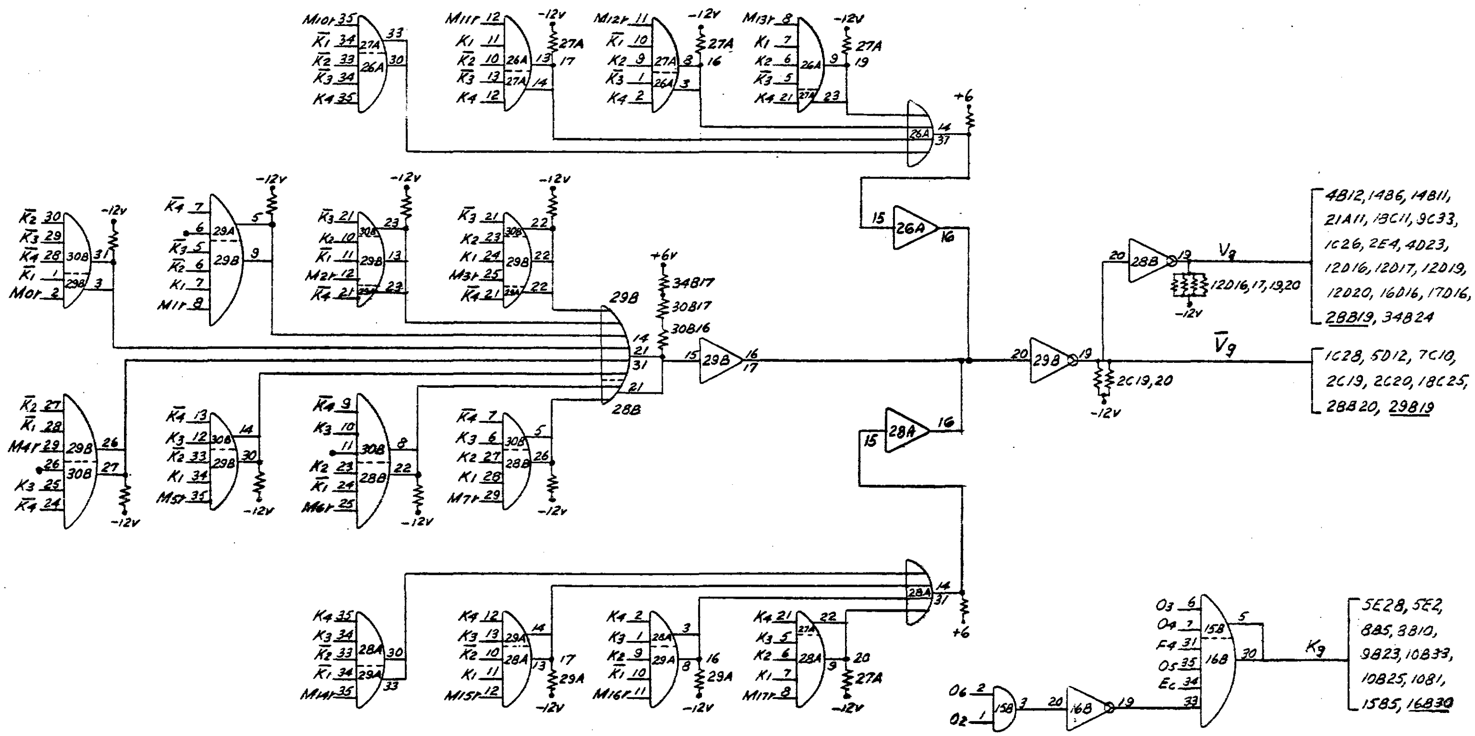
LOGIC LAYOUT

LOGIC SECT. COM. LINE SEL. TERM

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 46



$V_q = \bar{K}_4\bar{K}_3\bar{K}_2\bar{K}_1 M_{0r} + \bar{K}_4\bar{K}_3\bar{K}_2 K_1 M_{1r} + \bar{K}_4\bar{K}_3 K_2\bar{K}_1 M_{2r} + \bar{K}_4\bar{K}_3 K_2 K_1 M_{3r}$
$+ \bar{K}_4 K_3\bar{K}_2\bar{K}_1 M_{4r} + \bar{K}_4 K_3\bar{K}_2 K_1 M_{5r} + \bar{K}_4 K_3 K_2\bar{K}_1 M_{6r} + \bar{K}_4 K_3 K_2 K_1 M_{7r}$
$+ K_4\bar{K}_3\bar{K}_2\bar{K}_1 M_{10r} + K_4\bar{K}_3\bar{K}_2 K_1 M_{11r} + ------ + K_4 K_3 K_2\bar{K}_1 M_{16r} + K_4 K_3 K_2 K_1 M_{17r}$

$\bar{V}_q = \overline{(V_q)}$

$K_q = E_c O_5 O_4 O_3 F_4 (\bar{O}_6 + \bar{O}_2)$

LOGIC LAYOUT

LOGIC SECT. COM. LINE SEL. TERM Vq, Kq
DWG. NO. 505782 T DATE 1-9-62
DRAWN BY H. Mendelsohn APP.
SH. 47

$$
\begin{aligned}
sA_w = {} & E_c\bar{R}_c\bar{O}_6\bar{O}_4O_3\bar{O}_2O_1F_q \\
& + E_c\bar{R}_c\bar{O}_6\bar{O}_5O_4O_3\bar{O}_2Z_q \\
& + E_c\bar{R}_cO_6\bar{O}_5\bar{O}_4\bar{O}_3\bar{O}_2O_1P_c \\
& + E_c\bar{R}_cO_6\bar{O}_5O_4O_3\bar{O}_2O_1(L_1V_q + A_r\bar{V}_q) \\
& + E_c\bar{R}_c\bar{O}_6O_5\bar{O}_3\bar{O}_2(\bar{P}_{23}\bar{P}_2L_1 + P_2L_3 + P_{23}O_4L_1) \\
& + E_c\bar{R}_c\bar{O}_6O_5\bar{O}_4\bar{O}_3O_2\bar{P}_{23}A_e \\
& + \bar{O}_6O_5\bar{O}_4\bar{O}_3P_{23}A_r \\
& + E_c\bar{R}_cO_6\bar{O}_5\bar{O}_4\bar{O}_3\bar{O}_2\bar{O}_1F_qA_w \\
& + E_c\bar{R}_c\bar{O}_6\bar{O}_5\bar{O}_4\bar{O}_3\bar{O}_2O_1C_r \\
& + E_c\bar{P}_c\bar{O}_6O_5O_4\bar{O}_3O_2Z_q \\
& + A_r[\overline{E_c\bar{R}_c(\bar{O}_5\bar{O}_4\bar{O}_2O_1 + \bar{O}_5O_4O_3\bar{O}_2 + \bar{O}_6O_5\bar{O}_3 + O_6\bar{O}_5\bar{O}_4\bar{O}_3\bar{O}_2\bar{O}_1F_q + \bar{O}_6\bar{O}_4\bar{O}_2O_1)}]
\end{aligned}
$$

$$rA_w = (\overline{sA_w})$$

6-56

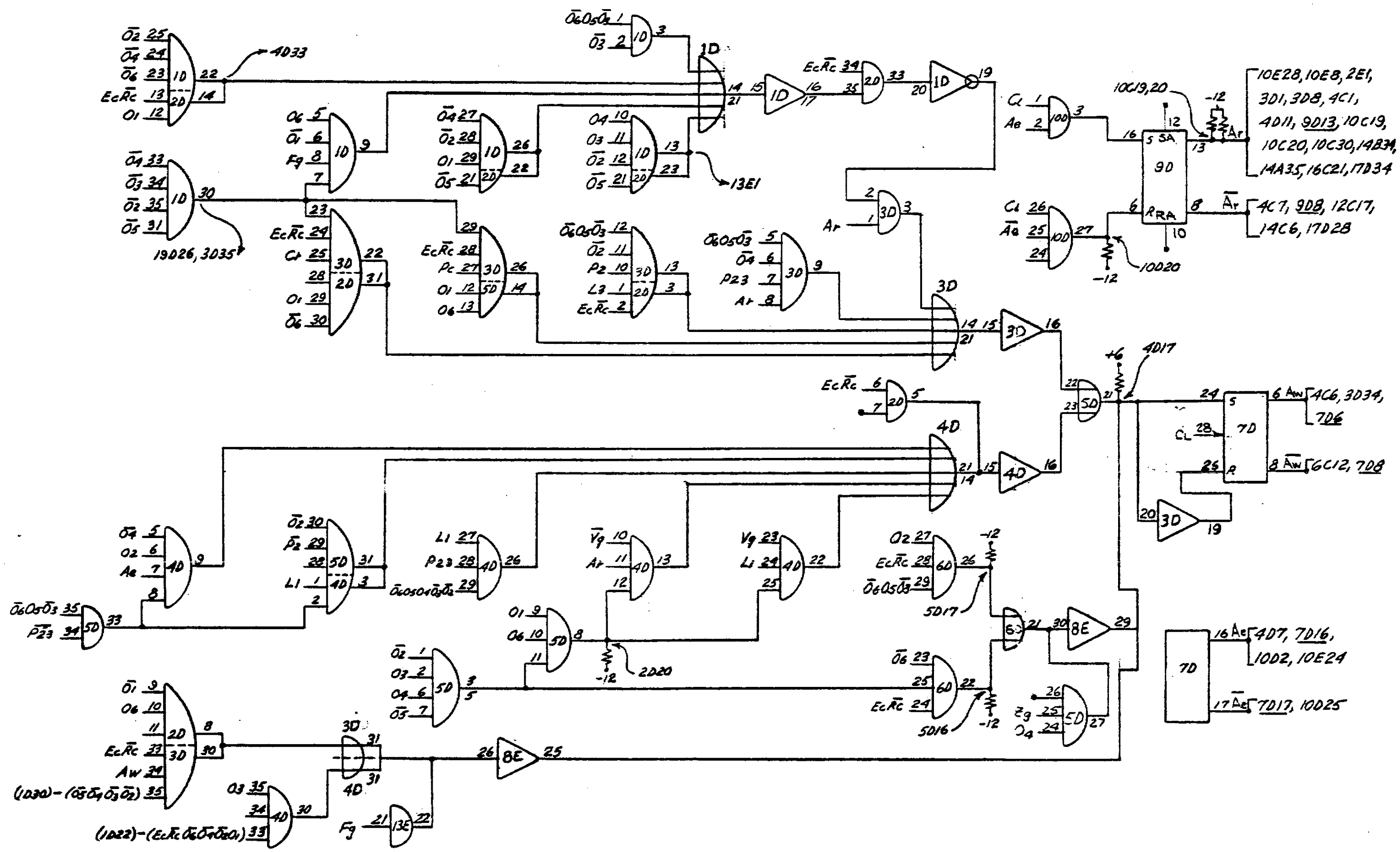
LOGIC LAYOUT

LOGIC SECT. A-REGISTER TERM sAw

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH.48



LOGIC LAYOUT

LOGIC SECT. A-REGISTER TERM

DWG. NO. 505782 T DATE 1-9-62

DRAWN BY H. Mendelsohn APP.

SH. 49

$$
\begin{aligned}
sB_w = {} & E_c \overline{R_c}\,\overline{O_6}\,\overline{O_5}\,\overline{O_4}\,O_3 O_2 F_q \\
& + E_c \overline{R_c}\,\overline{O_6}\,\overline{O_5}\,O_4 O_3 O_2 Z_q \\
& + E_c \overline{R_c}\,O_6 \overline{O_5}\,\overline{O_4}\,O_2 \overline{O_1} F_q C_r \\
& + E_c \overline{R_c}\,\overline{O_6}\,O_5 \overline{O_4}\,\overline{O_3}\,\overline{O_2}\,\overline{P_2} L_2 \\
& + E_c \overline{R_c}\,\overline{O_6}\,O_5 \overline{O_3}\,O_2 (\overline{P_{23}} B_e + P_{23} L_3) \\
& + E_c \overline{R_c}\,\overline{O_6}\,\overline{O_5}\,\overline{O_4}\,\overline{O_3}\,O_2 C_r \\
& + \overline{O_6}\,O_5 O_4 \overline{O_3}\,\overline{O_2} (E_c \overline{P_2}\,\overline{P_3} L_2 + E_c P_3 \overline{L_5}\,\overline{L_4} + E_c P_3 L_5 L_4 + \overline{E_c} P_2 L_4) \\
& + \overline{P_1} B_r \left[\overline{E_c \overline{R_c} (\overline{O_6}\,\overline{O_5}\,O_3 O_2 + \overline{O_6}\,O_5 \overline{O_3} + O_6 \overline{O_5}\,\overline{O_4}\,O_2 F_q + \overline{O_5}\,\overline{O_4}\,\overline{O_3}\,O_2)}\right]
\end{aligned}
$$

$$
rB_w = (\overline{sB_w})
$$

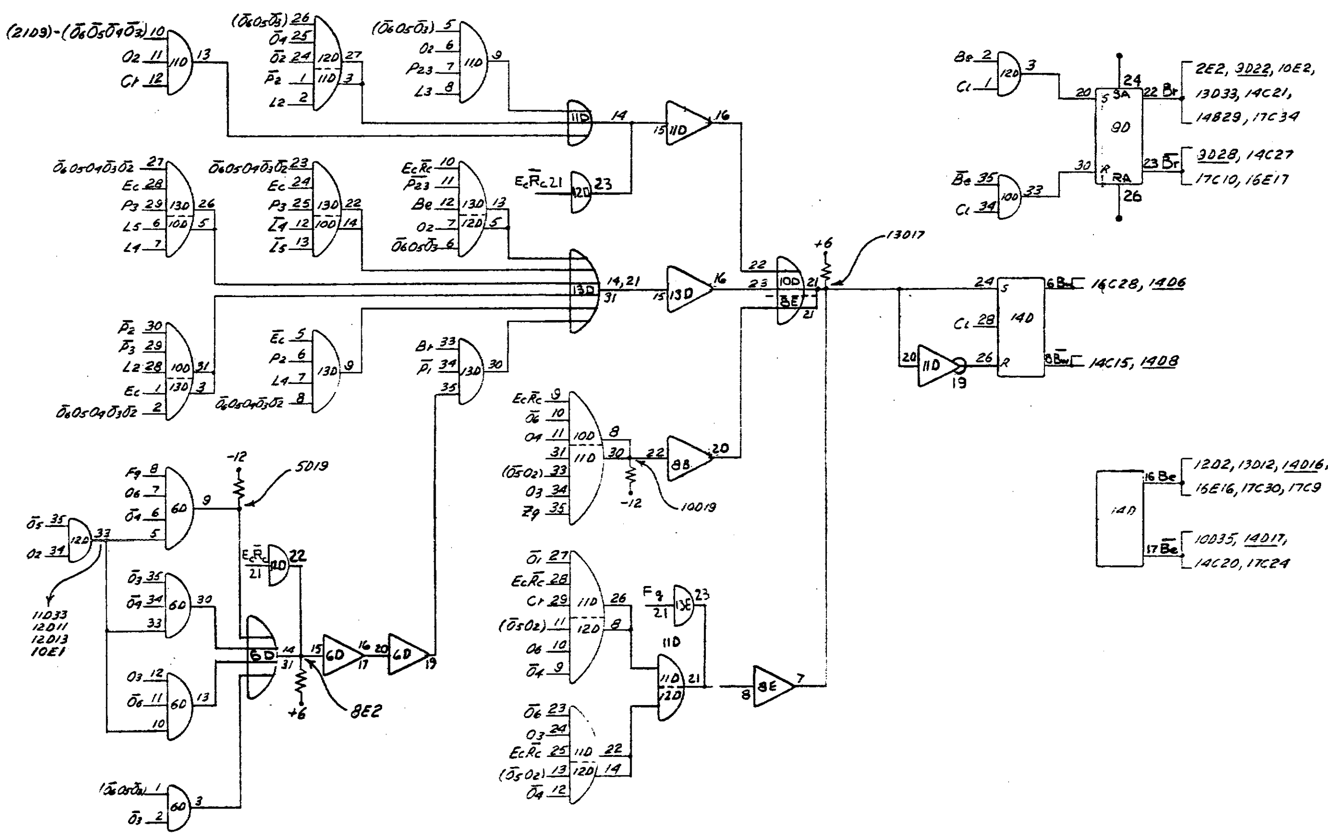
LOGIC LAYOUT

LOGIC SECT. B REGISTER TERM Bw

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 50



LOGIC LAYOUT

LOGIC SECT B-REGISTER TERM Bw, Br, Be
DWG. NO. 505782 T DATE 1-6-62
DRAWN BY H Mendelsohn APP.

SH. 51

$$
\begin{aligned}
sC_W = {} & E_c \overline{R_c}\, \overline{O_6}\,\overline{O_5}\,\overline{O_4}\, O_3\, \overline{O_2}\,\overline{O_1}\, F_9 \\
& + E_c \overline{R_c}\, \overline{O_6}\,\overline{O_5}\,\overline{O_4}\,\overline{O_3}\, I_9 \\
& + P_{24}\, C_W \\
& + E_c \overline{R_c}\, O_5 \overline{O_4}\, Z_9 \\
& + E_c \overline{R_c}\, \overline{O_6}\, O_5 O_4 \overline{O_3}\,\overline{O_2}\,\overline{O_1}\, D_9 \\
& + \overline{P_{24}}\, C_r \overline{\left[E_c \overline{R_c}\left(\overline{O_5}\,\overline{O_4}\, O_3 \overline{O_2}\,\overline{O_1} + \overline{O_6}\,\overline{O_5}\,\overline{O_4}\,\overline{O_3} + O_5 \overline{O_4} + \overline{O_6}\, O_5 O_4 \overline{O_3}\,\overline{O_2}\,\overline{O_1}\right)\right]}
\end{aligned}
$$

9-60

$$rC_W = (\overline{sC_W})$$

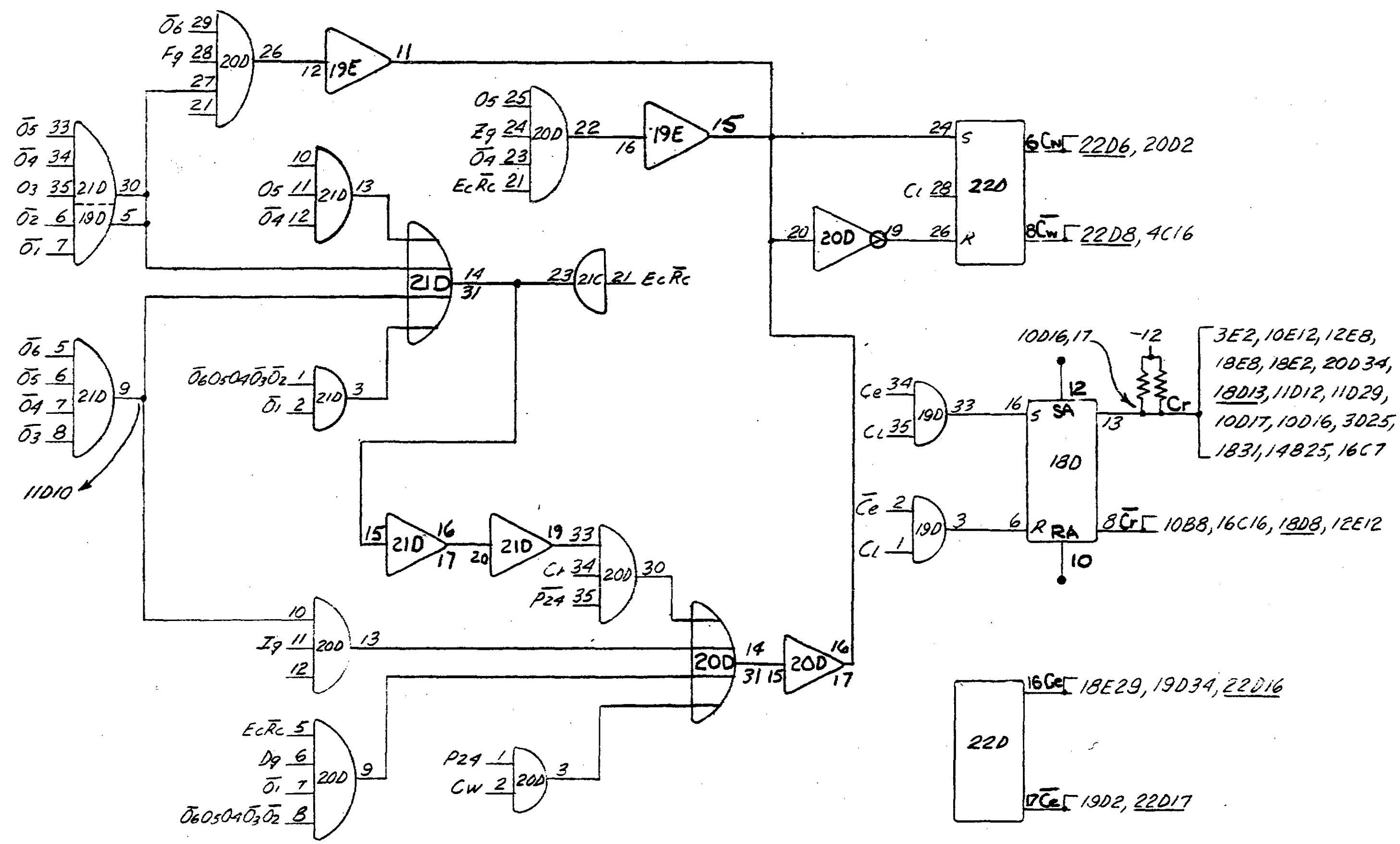
LOGIC LAYOUT

LOGIC SECT. C REGISTER TERM CW

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Hendrickson APP. ______

SH. 52



LOGIC LAYOUT

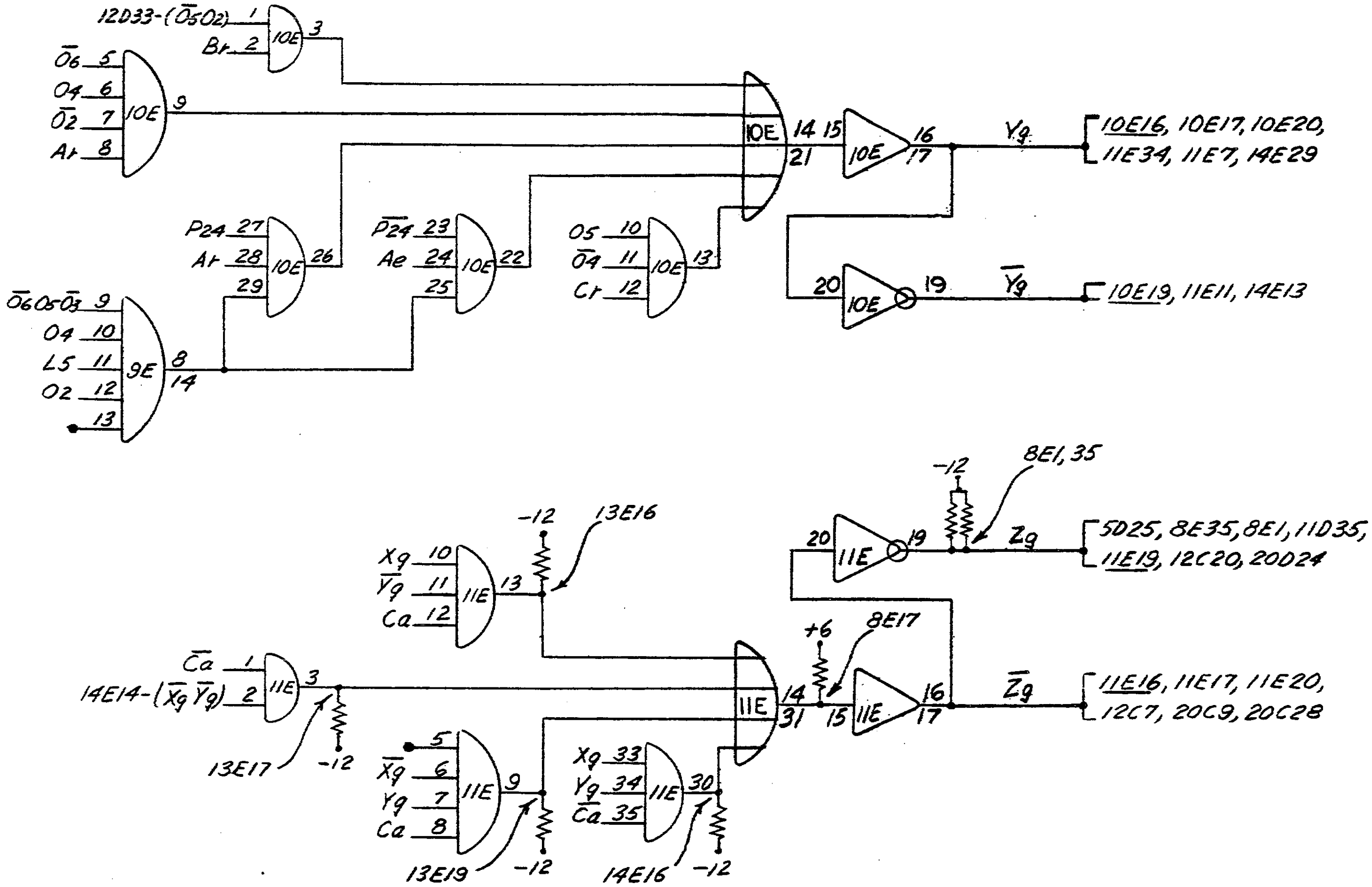
LOGIC SECT. C-REGISTER TERM Cw, Ce, Cr

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 53

6-62



$\mathrm{Y9} = \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 L_5 (\overline{P24}\,Ae + P24\,Ar) + \bar{O}_6 O_4 \bar{O}_2 Ar + \bar{O}_5 O_2 Br + O_5 \bar{O}_4 Cr$

$\overline{\mathrm{Y9}} = \overline{(\mathrm{Y9})}$

$\overline{\mathrm{Z9}} = X_9 Y_9 \overline{Ca} + X_9 \bar{Y}_9 Ca + \bar{X}_9 Y_9 Ca + \bar{X}_9 \bar{Y}_9 \overline{Ca}$

$\mathrm{Z9} = \overline{(\overline{\mathrm{Z9}})}$

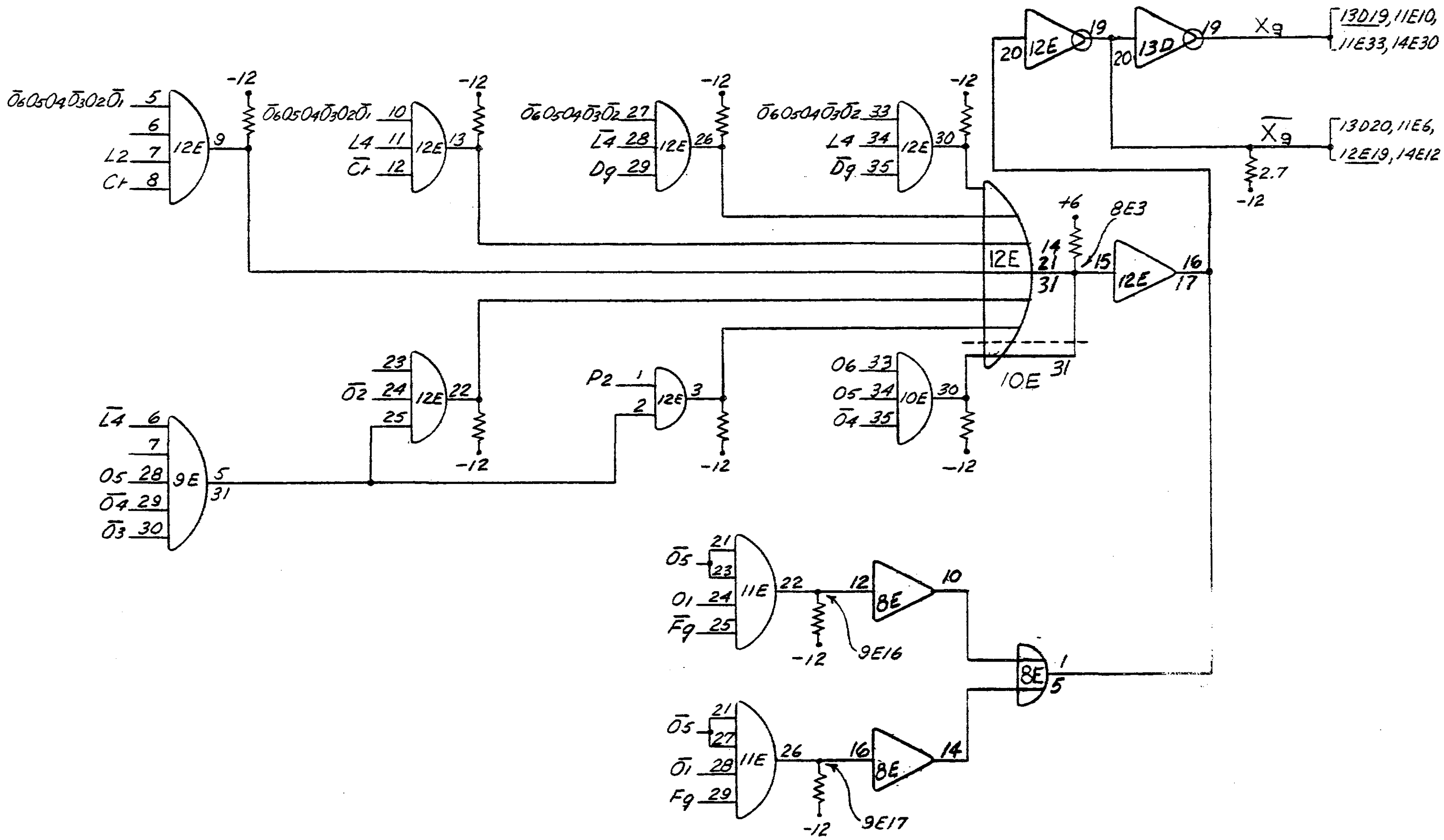
LOGIC LAYOUT

LOGIC SECT. ADDER TERM Y9 & Z9

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 54



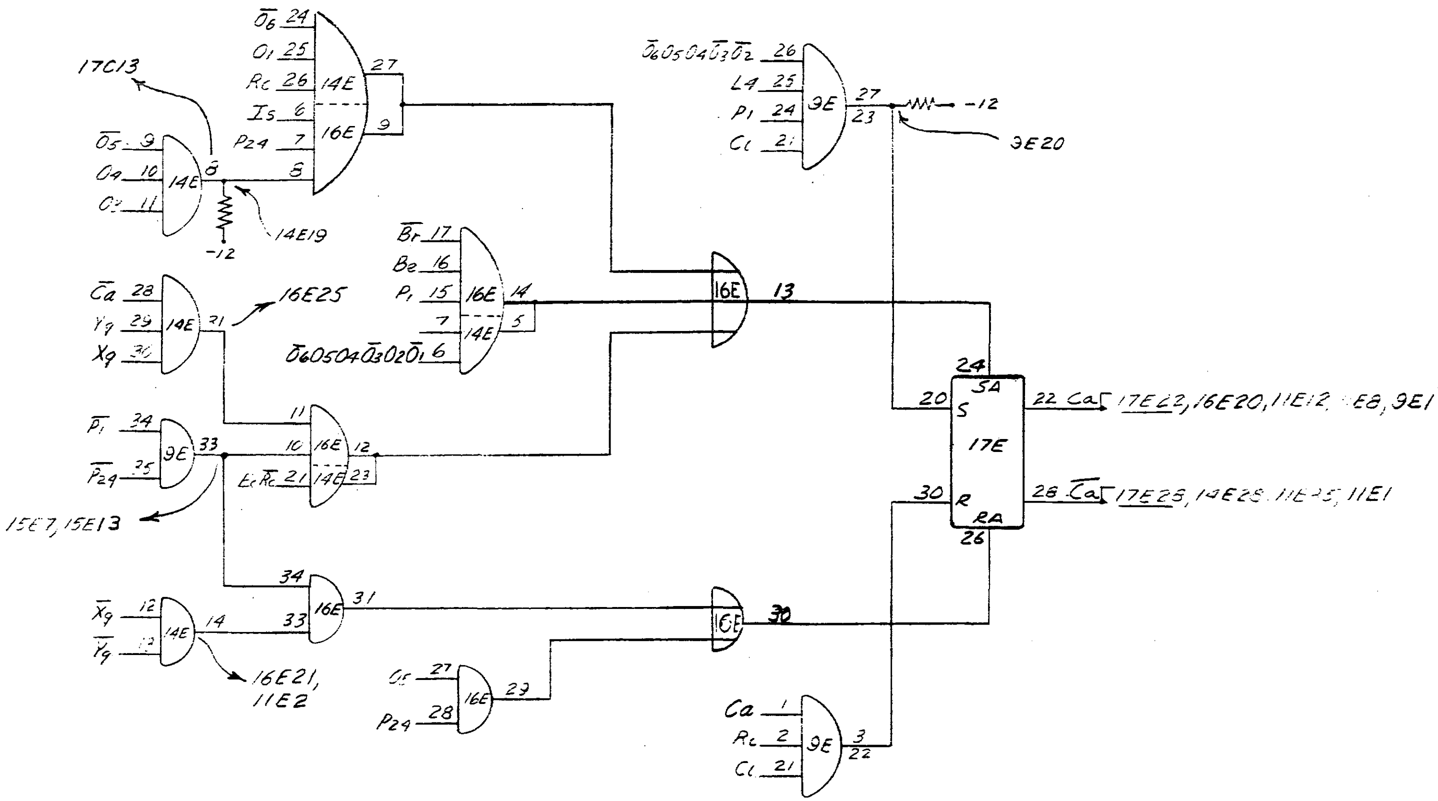
$$X_9 = \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 (\bar{L}_4 D_9 + L_4 \bar{D}_9) + \bar{O}_6 O_5 O_4 \bar{O}_3 O_2 \bar{O}_1 (L_2 C_r + L_4 \bar{C}_r)$$
$$+ \bar{O}_5 \bar{O}_1 F_9 + \bar{O}_5 O_1 \bar{F}_9 + O_6 O_5 \bar{O}_4 + O_5 \bar{O}_4 \bar{O}_3 \bar{L}_4 (\bar{O}_2 + P_2)$$

$$\bar{X}_9 = \overline{(X_9)}$$

LOGIC LAYOUT

LOGIC SECT.	ADDER	TERM	X9
DWG. NO.	505782 T	DATE	1-6-62
DRAWN BY	H. Mendelsohn	APP.	

SH. 55



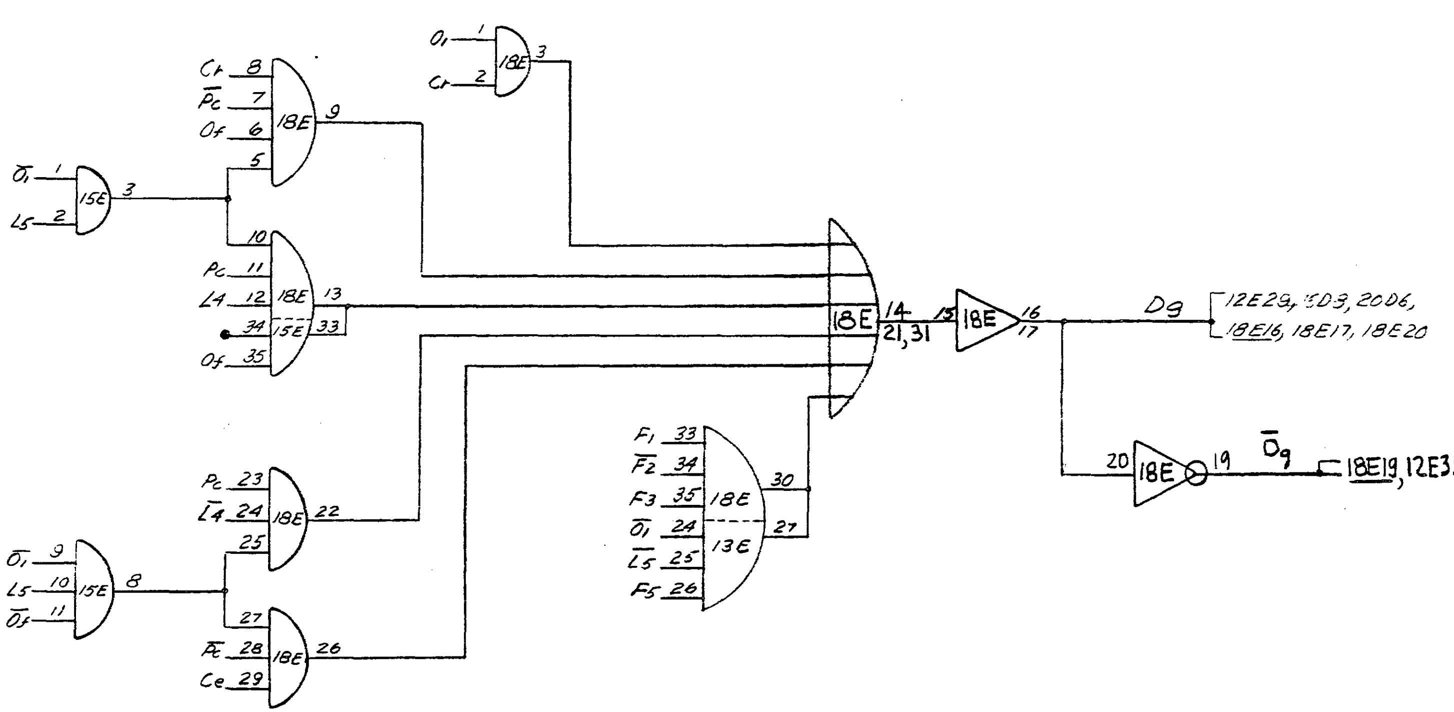
$sCa = \overline{P_1}\,\overline{P_{24}}\,\overline{Ca}\,E_c\overline{R_c}\,X_9 Y_9 + P_{24} R_c I_s \overline{O_6}\,\overline{O_5}\,O_4 O_3 O_1$
$+ \overline{O_6} O_5 O_4 \overline{O_3}\,\overline{O_2} P_1 L_4 + \overline{O_6} O_5 O_4 \overline{O_3} O_2 \overline{O_1} P_1 B_e \overline{B_r}$

$rCa = \overline{P_1}\,\overline{P_{24}}\,\overline{X_9}\,\overline{Y_9} + Ca R_c + O_5 P_{24}$

LOGIC LAYOUT

LOGIC SECT. ADDER TERM. Ca
DWG. NO. 5D5782 T DATE 1-6-62
DRAWN BY [illegible] AFM. ___

SH. 56



$$D_9 = O_1 C_r + \overline{O_1} L_5 (O_f \overline{P_c} C_r + O_f P_c L_4 + \overline{O_f} P_c \overline{L_4} + \overline{O_f}\, \overline{P_c} C_e) + \overline{O_1}\, \overline{L_5} F_5 F_3 \overline{F_2} F_1$$

$$\overline{D_9} = (\overline{D_9})$$

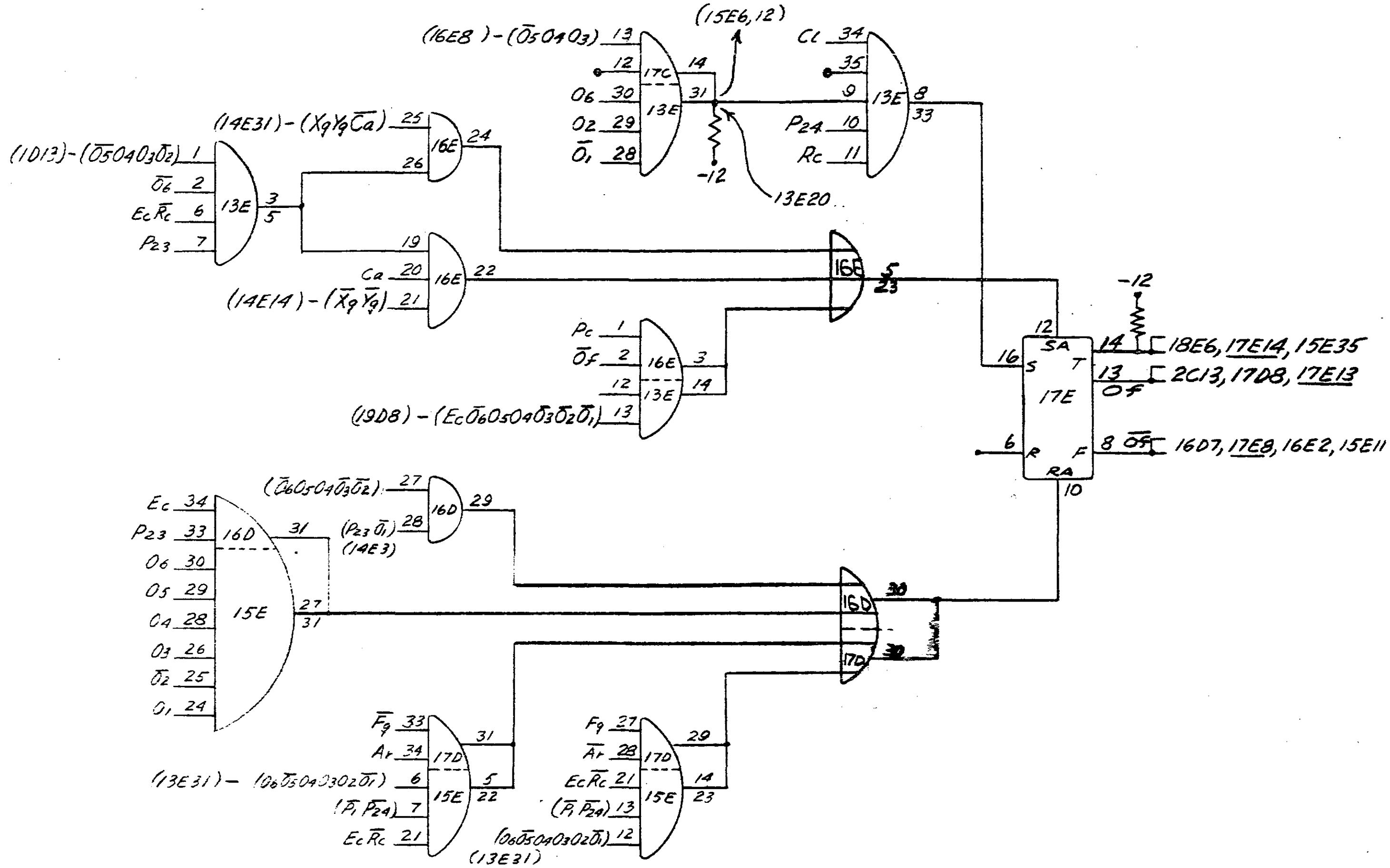
LOGIC LAYOUT

LOGIC SECT. ADDER TERM D_9

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 57



$$S O_f = P_{23} E_c \bar{R}_c \bar{O}_6 \bar{O}_5 O_4 O_3 \bar{O}_2 (\bar{X}_9 \bar{Y}_9 C_a + X_9 Y_9 \bar{C}_a)$$
$$+ \bar{O}_f E_c \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 P_c + P_{24} R_c O_6 \bar{O}_5 O_4 O_3 O_2 \bar{O}_1$$

$$R O_f = P_{23} E_c O_6 O_5 O_4 O_3 \bar{O}_2 O_1 + P_{23} \bar{O}_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1$$
$$+ \bar{P}_1 \bar{P}_{24} E_c \bar{R}_c O_6 \bar{O}_5 O_4 O_3 O_2 \bar{O}_1 (F_9 \bar{A}_r + \bar{F}_9 A_r)$$

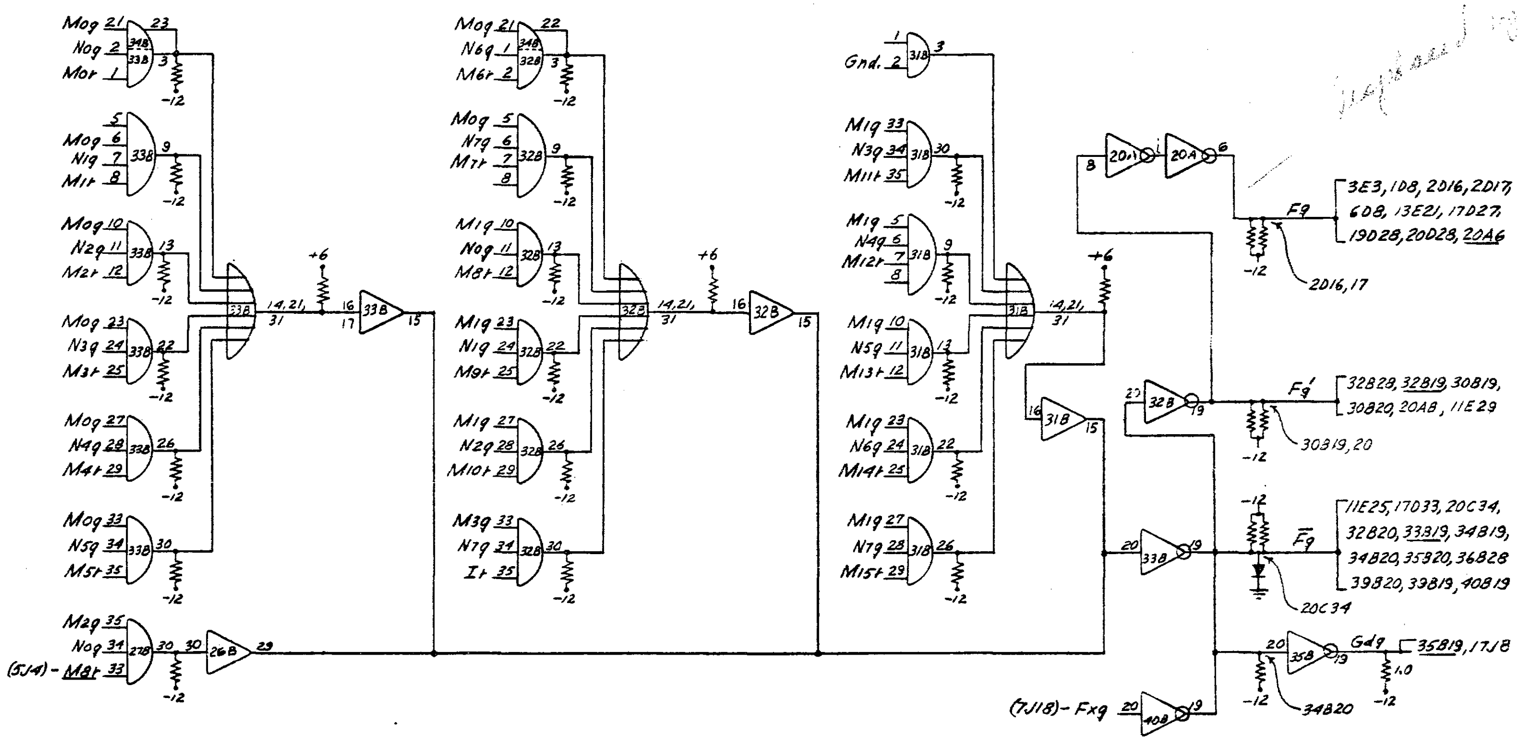
LOGIC LAYOUT

LOGIC SECT. ADDER — TERM O_f

DWG. NO. 505782 T — DATE 1-6-62

DRAWN BY H. Mendelsohn — APP.

SH. 58



Fg = M0g N0g M0r + M0g N1g M1r + ------ ------ + M1g N7g M15r + M3g N7g Ir + Fxg

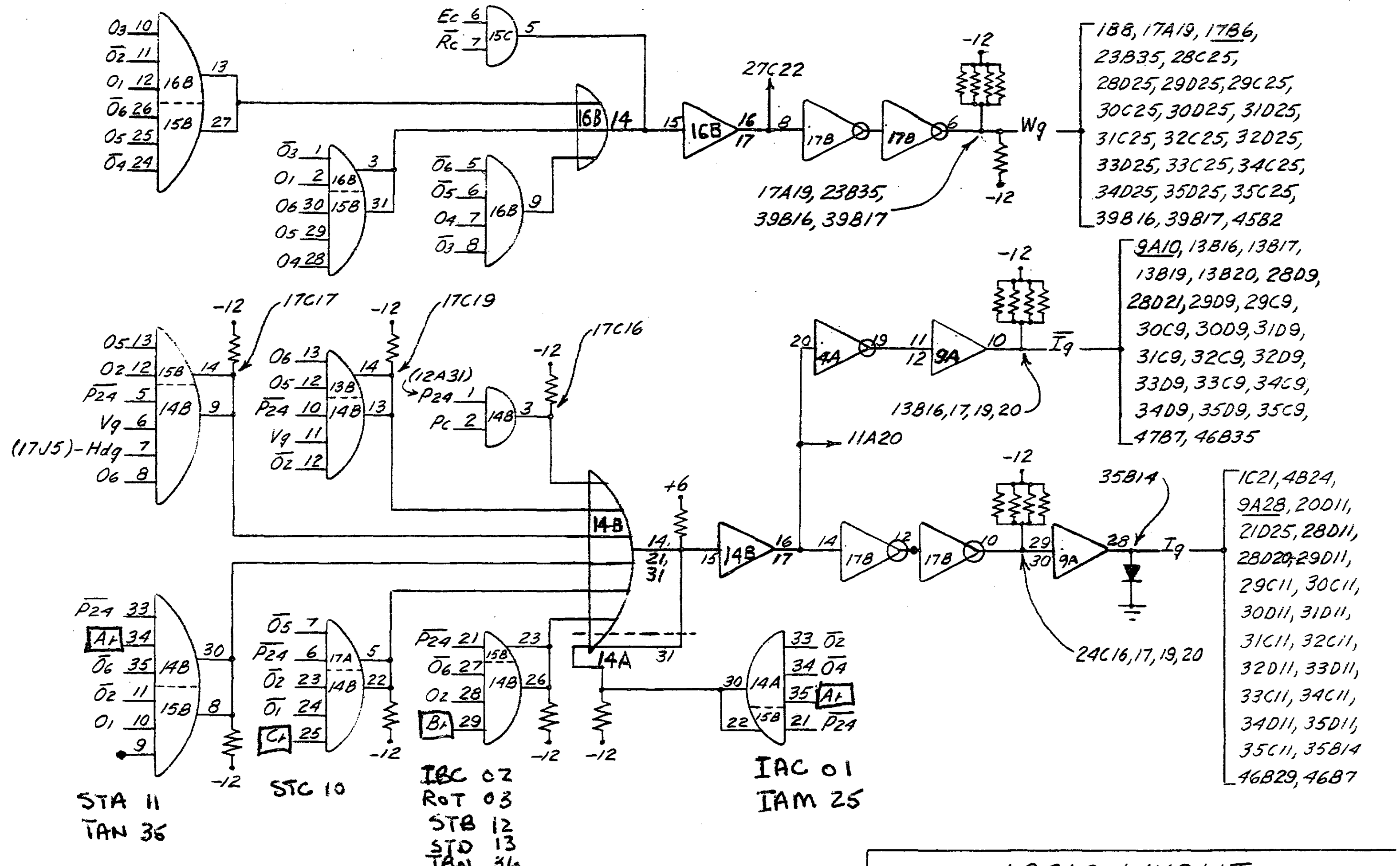
LOGIC LAYOUT

LOGIC SECT. DATA TRANS. GATES TERM Fg

DWG. NO. 505782 T DATE 1-9-62

DRAWN BY H. Mendelsohn APP. ____

SH. 59



$$W_q = (\bar{O}_6\bar{O}_5 O_4 \bar{O}_3 + O_6 O_5 O_4 \bar{O}_3 O_1 + \bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1)\, E_c \bar{R}_c$$

$$I_q = \overline{P24}\,\bar{O}_5\bar{O}_2\bar{O}_1 C_r + \overline{P24}\,\bar{O}_6\bar{O}_2 O_1 A_r + \overline{P24}\,\bar{O}_6 O_2 B_r + \overline{P24}\,\bar{O}_4\bar{O}_2 A_r + \overline{P24}\, O_6 O_5 \bar{O}_2 V_q + \overline{P24}\, O_6 O_5 O_2 V_q H_{dq} + P24\, P_c$$

$$\bar{I}_q = (\bar{I}_q)$$

LOGIC LAYOUT

LOGIC SECT. DATA TRANS. GATES TERM Wq & Iq

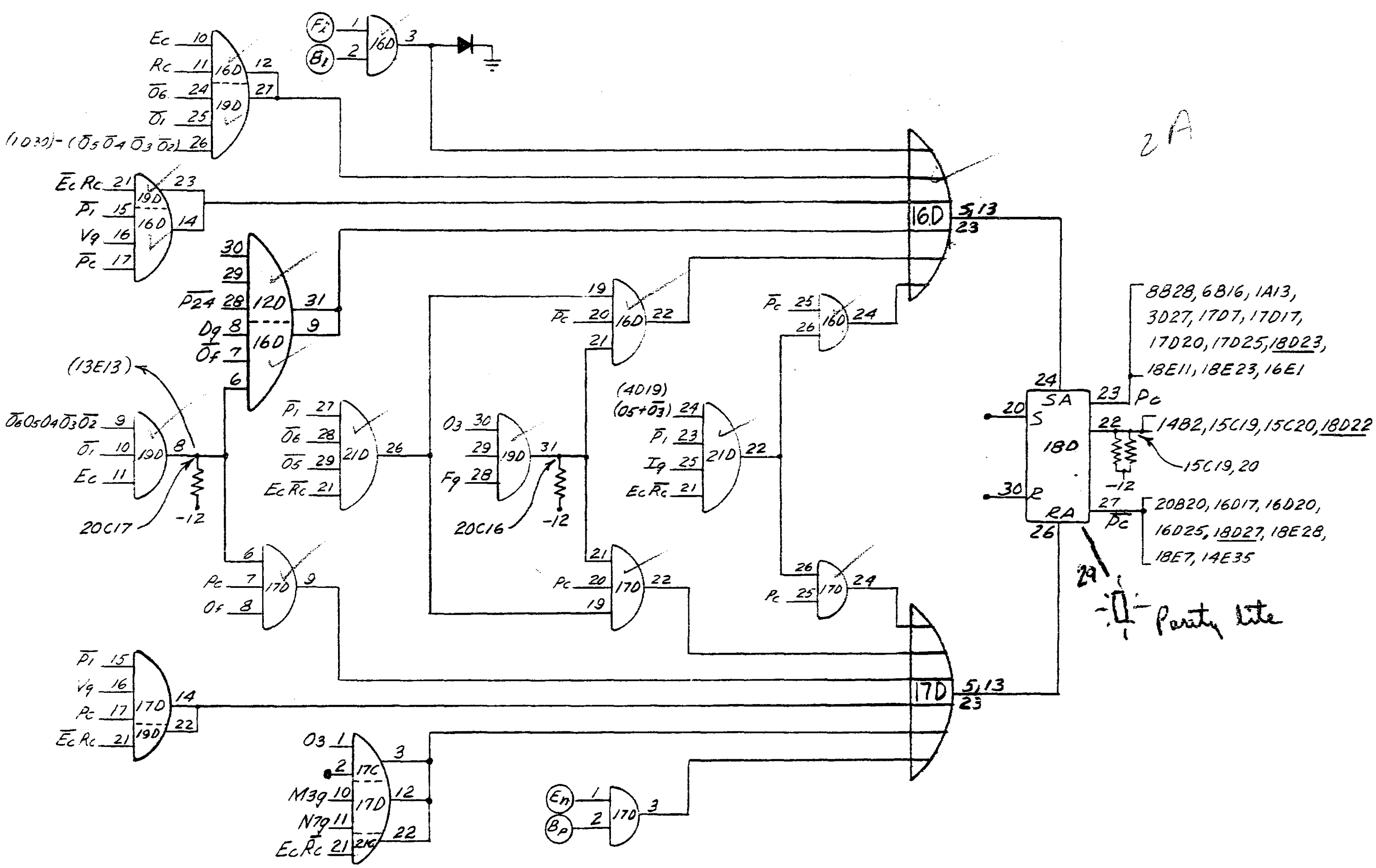
DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ______

SH. 60

6-69

2A



$sPc = Ec\bar{Rc}\bar{P_1}\overline{O_5O_3}I_q\bar{Pc} + \bar{P_1}Ec\bar{Rc}\bar{O_6}\bar{O_5}O_3F_q\bar{Pc} + \bar{P_1}\bar{Ec}RcV_q\bar{Pc}$
$+ \bar{P_{24}}Ec\bar{O_6}O_5O_4\bar{O_3}\bar{O_2}\bar{O_1}\bar{O_f}D_q + (F_1)(B_1) + EcRc\bar{O_6}\bar{O_5}\bar{O_4}\bar{O_3}\bar{O_2}\bar{O_1}$

$rPc = Ec\bar{Rc}\bar{P_1}\overline{O_5O_3}I_qPc + \bar{P_1}Ec\bar{Rc}\bar{O_6}\bar{O_5}O_3F_qPc + M_{3q}N_{7q}Ec\bar{Rc}O_3$
$+ \bar{P_1}\bar{Ec}RcV_qPc + (E_n)(B_p) + Ec\bar{O_6}O_5O_4\bar{O_3}\bar{O_2}\bar{O_1}O_fPc$

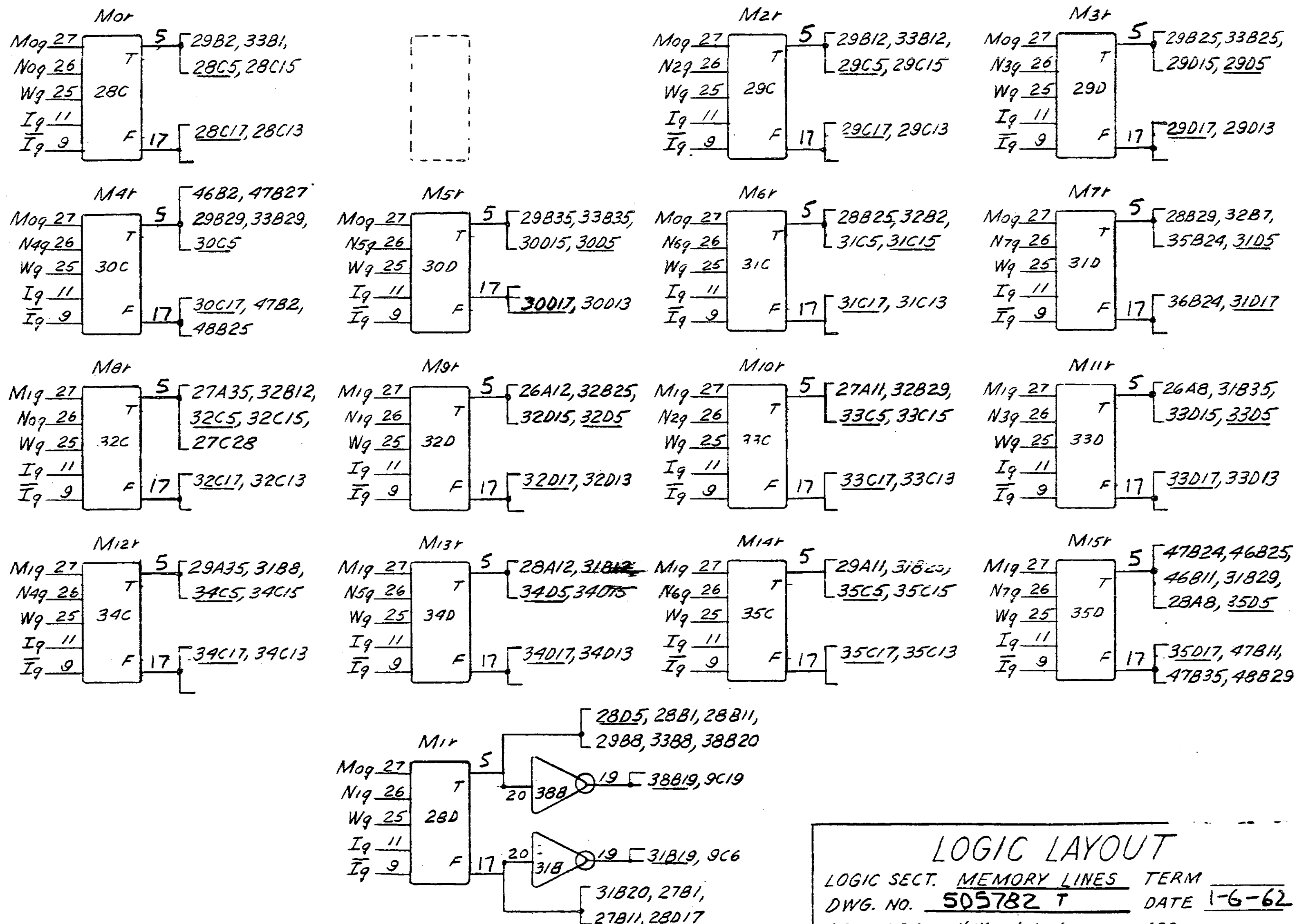
LOGIC LAYOUT

LOGIC SECT. DATA TRANSFER TERM Pc

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ______

SH 61



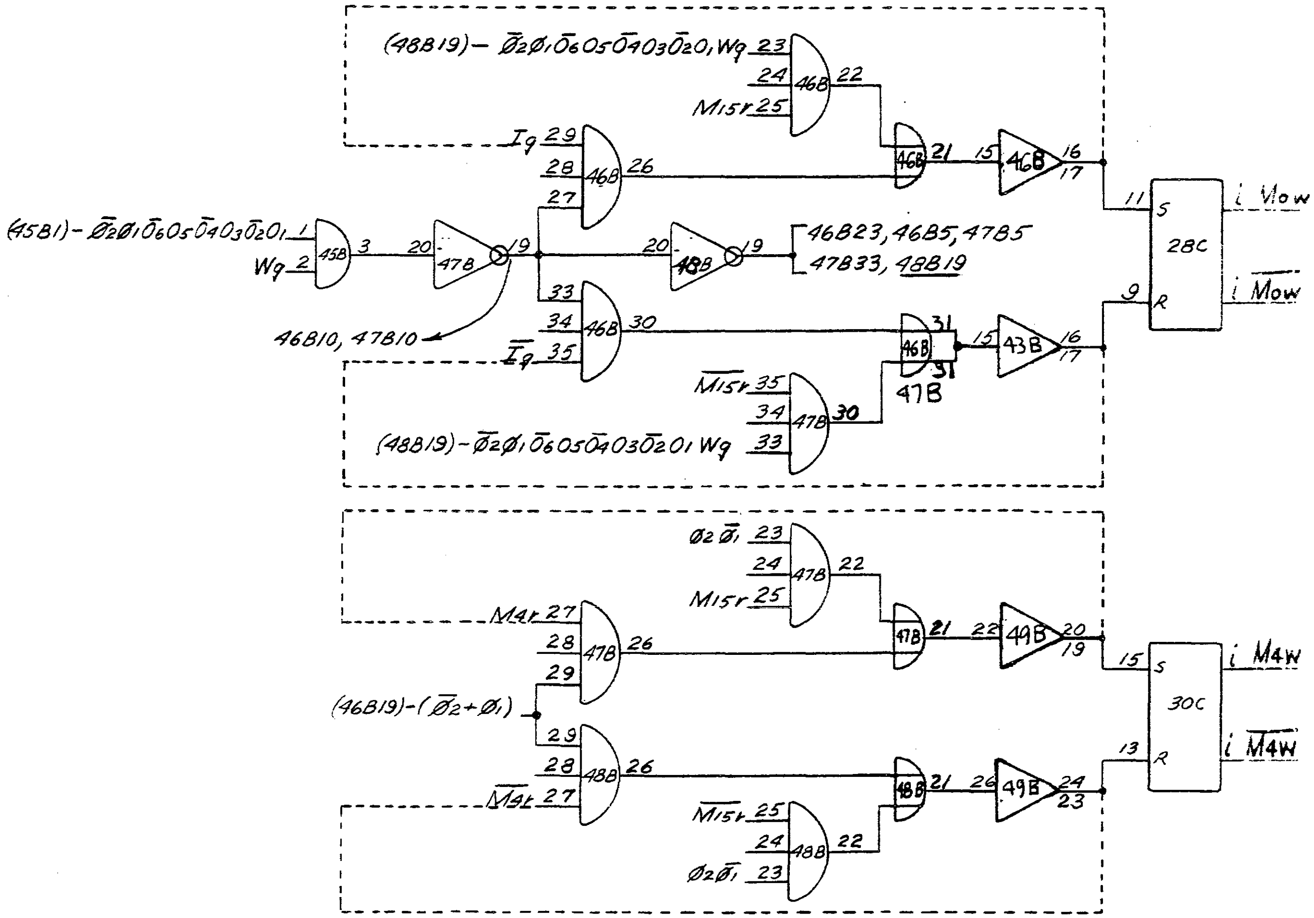
LOGIC LAYOUT

LOGIC SECT. MEMORY LINES TERM

DWG. NO. 5D5782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH 62



$$sMow = Mo_9 No_9 W_9[\bar{Ø}_2 Ø_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1)M_{15r} + \overline{W_9 \bar{Ø}_2 Ø_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) I_9}] + \text{- -}$$

$$rMow = Mo_9 No_9 W_9[\bar{Ø}_2 Ø_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1)\overline{M_{15r}} + \overline{W_9 \bar{Ø}_2 Ø_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) I_9}] + \text{- -}$$

$$sM4w = \text{- - -} + [\overline{Mo_9 N4_9 W_9}][Ø_2 \bar{Ø}_1 M_{15r} + (\bar{Ø}_2 + Ø_1)M_{4r}]$$

$$rM4w = \text{- - -} + [\overline{Mo_9 N4_9 W_9}][Ø_2 \bar{Ø}_1 \overline{M_{15r}} + (\bar{Ø}_2 + Ø_1)\overline{M_{4r}}]$$

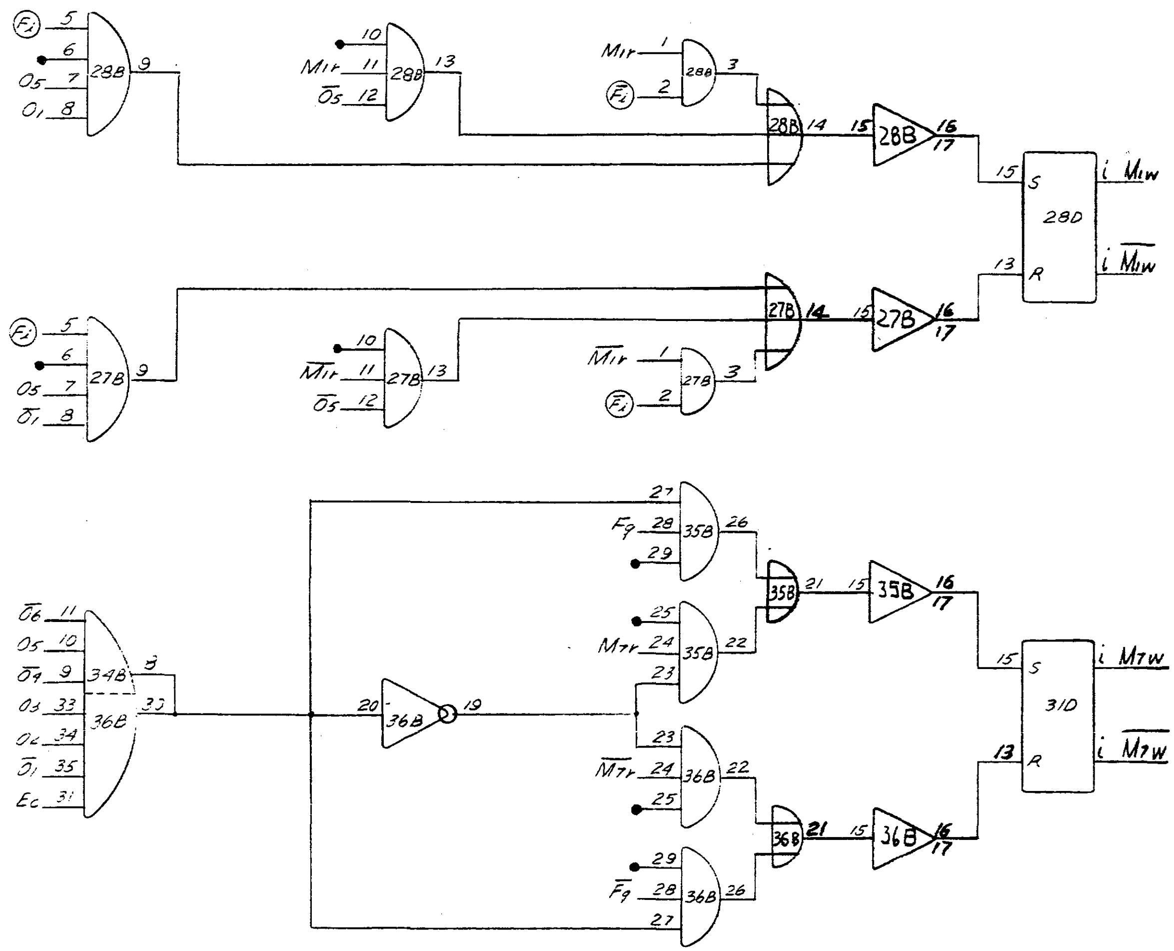
LOGIC LAYOU

LOGIC SECT. MEMORY LINES TERM Mow, M4W

DWG. NO. 505782 T DATE 1-6-

DRAWN BY H. APP.

SH. 63



$$sM_{1w} = M_{09} N_{19} W_9 I_9 + [\overline{M_{09} N_{19} W_9}][M_{1r}(\overline{F_i O_5}) + F_i O_5 O_1]$$

$$rM_{1w} = M_{09} N_{19} W_9 \bar{I}_9 + [\overline{M_{09} N_{19} W_9}][\overline{M_{1r}}(\overline{F_i O_5}) + F_i O_5 \bar{O}_1]$$

$$sM_{7w} = M_{09} N_{79} W_9 I_9 + [\overline{M_{09} N_{79} W_9}][M_{7r}(\overline{\bar{O}_6 O_5 \bar{O}_4 O_3 O_2 \bar{O}_1 E_c}) + (\bar{O}_6 O_5 \bar{O}_4 O_3 O_2 \bar{O}_1 E_c) F_9]$$

$$rM_{7w} = M_{09} N_{79} W_9 \bar{I}_9 + [\overline{M_{09} N_{79} W_9}][\overline{M_{7r}}(\overline{\bar{O}_6 C_5 \bar{C}_4 O_3 O_2 \bar{O}_1 E_c}) + (\bar{O}_6 C_5 \bar{C}_4 O_3 O_2 \bar{O}_1 E_c) \bar{F}_9]$$

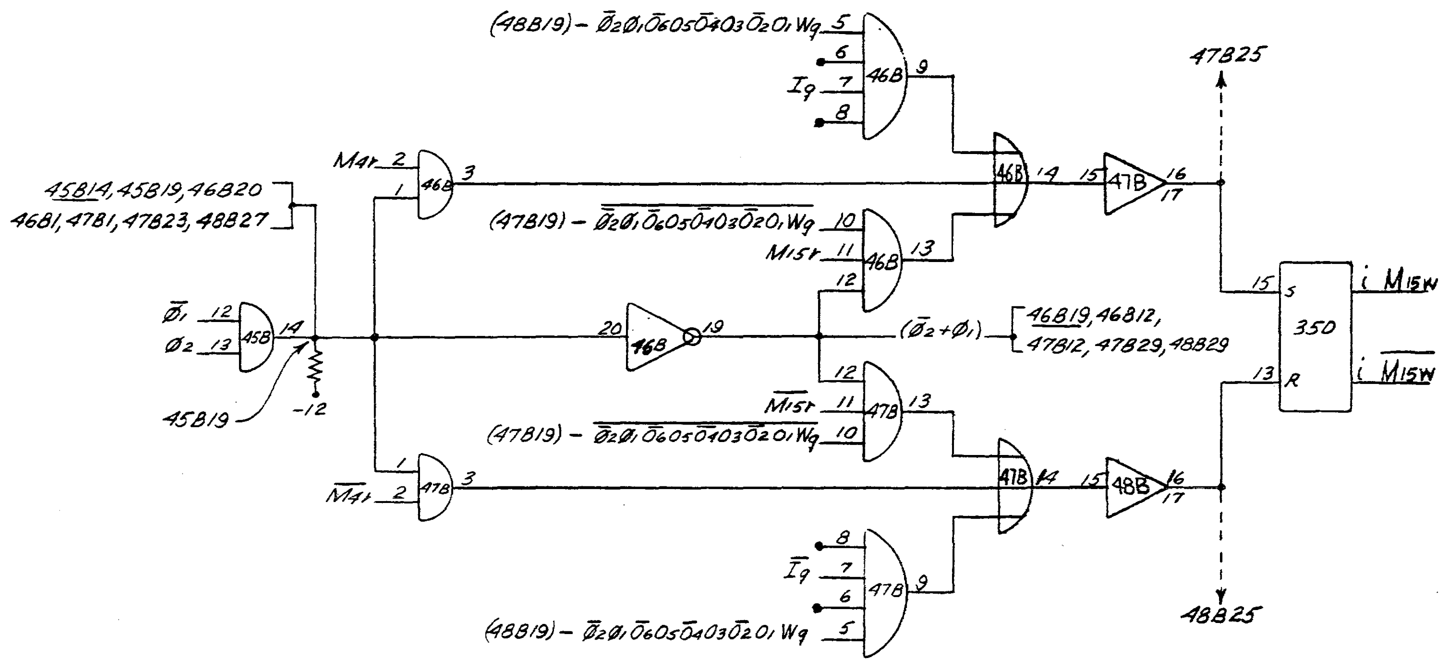
LOGIC LAYOUT

LOGIC SECT. MEMORY LINES TERM M_{1w} + M_{7w}

DWG. NO. 505782 T DATE 1-8-62

DRAWN BY H. Henderson APP.

SH. 64



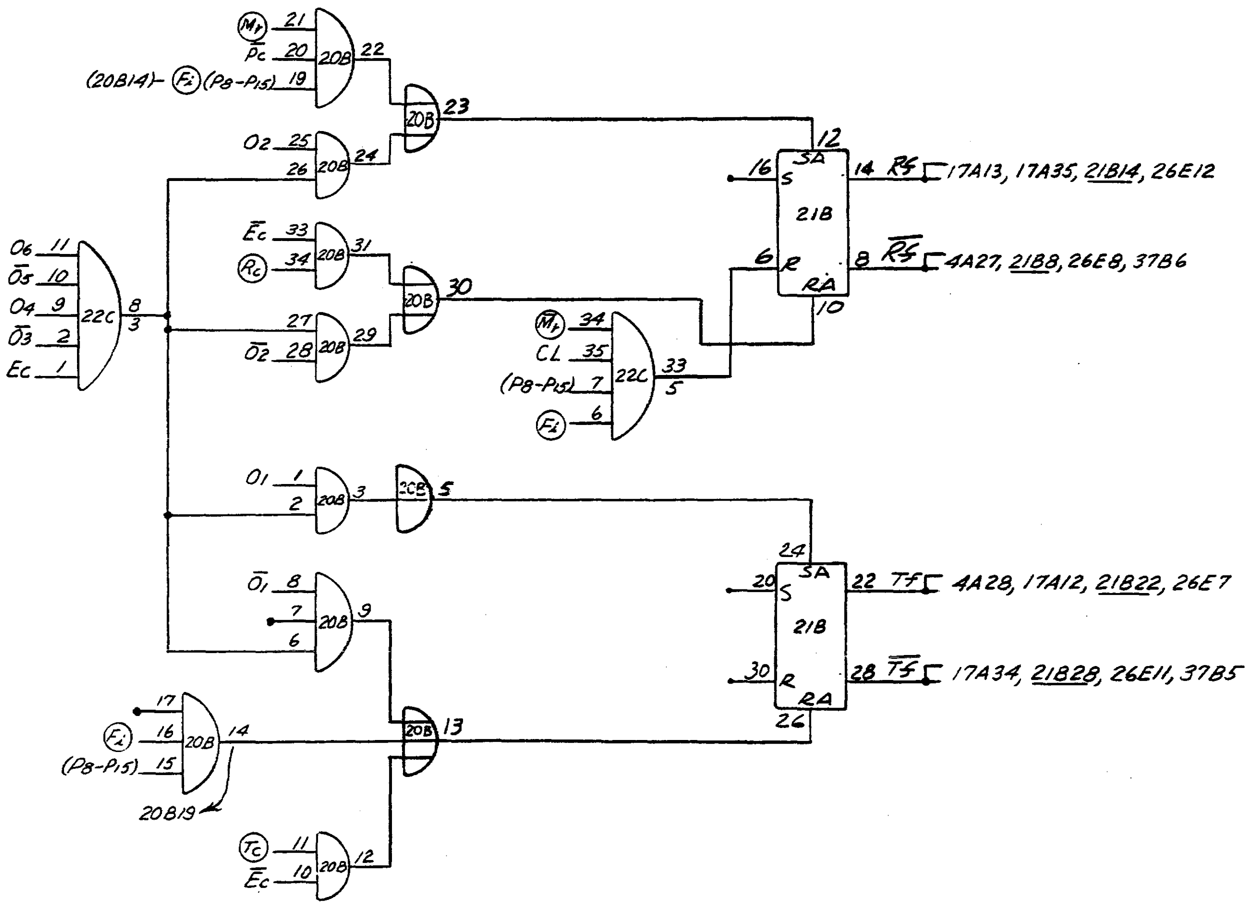
$$sM_{15W} = -- + [\overline{M_{1q}N_{7q}W_q}][\phi_2\bar{\phi}_1 M_{4r} + \bar{\phi}_2\phi_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) W_q I_q$$
$$+ (\bar{\phi}_2 + \phi_1)\, \overline{W_q \bar{\phi}_2 \phi_1 (\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) M_{15r}}]$$

$$rM_{15W} = -- + [\overline{M_{1q}N_{7q}W_q}][\phi_2\bar{\phi}_1 \overline{M_{4r}} + \bar{\phi}_2\phi_1(\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1) W_q \bar{I}_q$$
$$+ (\bar{\phi}_2 + \phi_1)\, \overline{W_q \bar{\phi}_2 \phi_1 (\bar{O}_6 O_5 \bar{O}_4 O_3 \bar{O}_2 O_1)}\, \overline{M_{15r}}]$$

LOGIC LAYOUT

LOGIC SECT. MEMORY LINES TERM M_{15W}
DWG. NO. 505782 T DATE 1-6-62
DRAWN BY H. Mendelsohn APP.

SH. 65



$SRf = E_c O_6 \bar{O}_5 O_4 \bar{O}_3 O_2 + F_i \bar{P}_c (P_8 - P_{15}) M_f$

$RRf = E_c O_6 \bar{O}_5 O_4 \bar{O}_3 \bar{O}_2 + F_i \bar{M}_f (P_8 - P_{15}) + R_c \bar{E}_c$

$STf = E_c O_6 \bar{O}_5 O_4 \bar{O}_3 O_1$

$RTf = E_c O_6 \bar{O}_5 O_4 \bar{O}_3 \bar{O}_1 + T_c \bar{E}_c + F_i (P_8 - P_{15})$

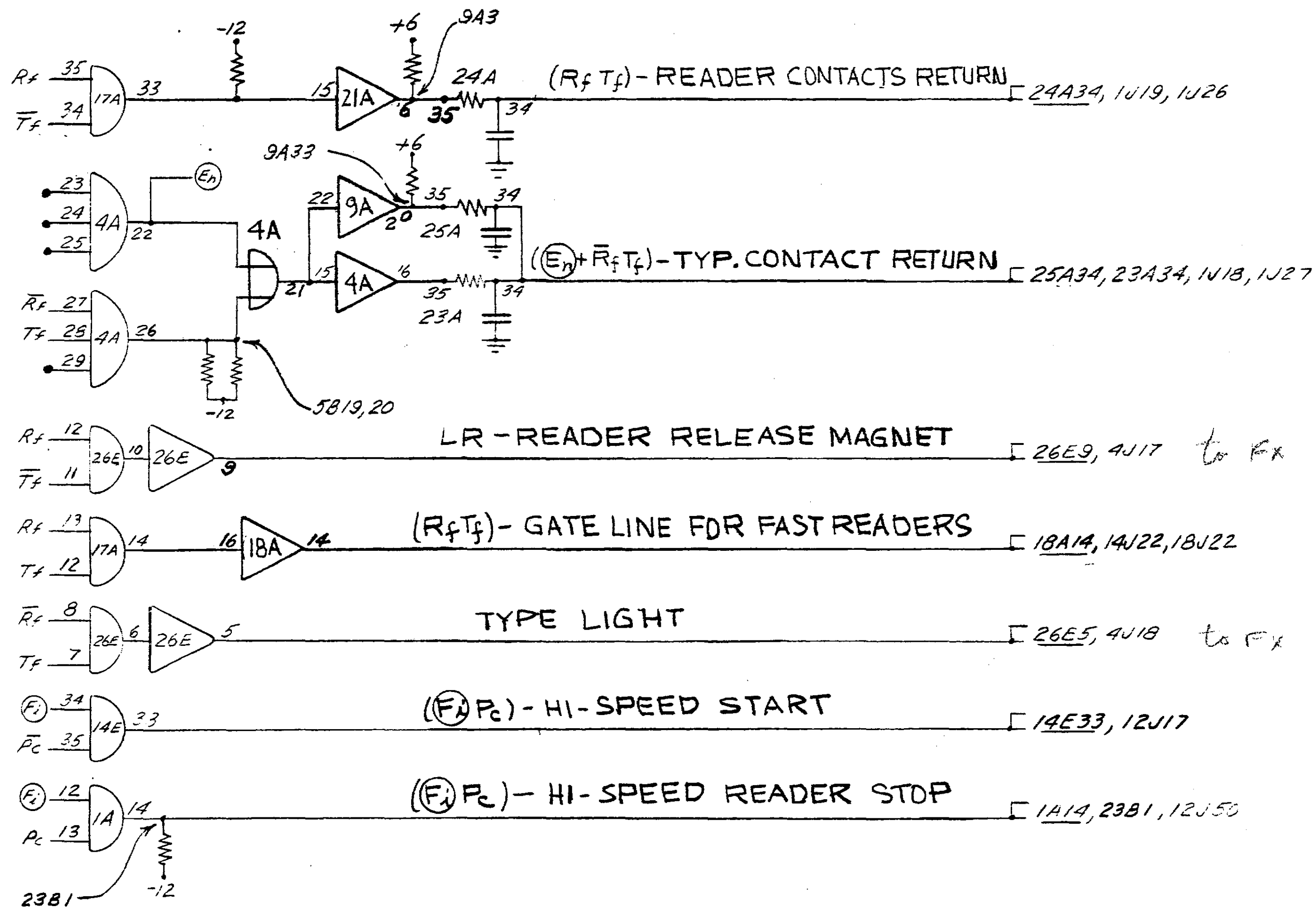
LOGIC LAYOUT

LOGIC SECT. CHAR. INPUT TERM Rf, Tf

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 66



LOGIC LAYOUT

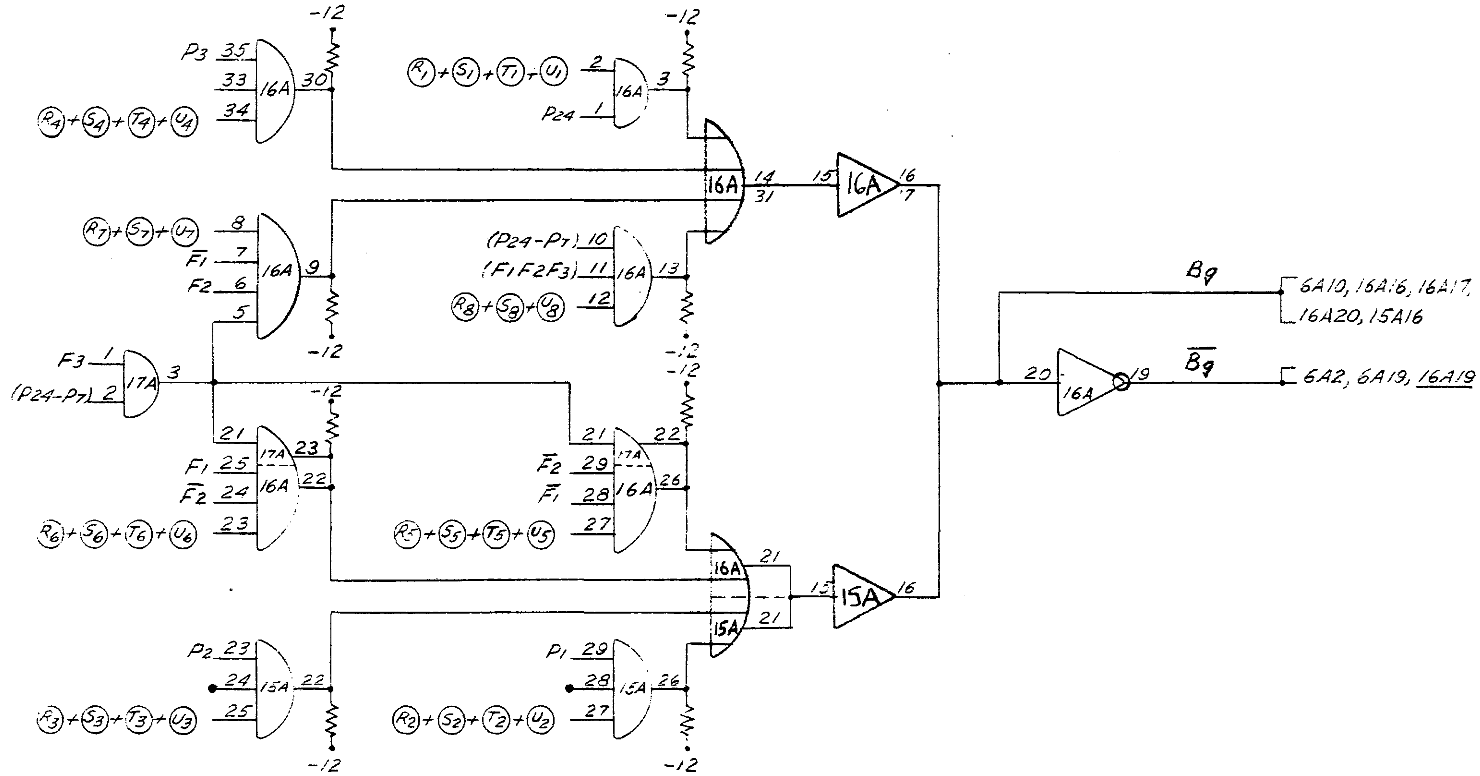
LOGIC SECT. CHAR. INPUT

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY

APP.

SH. 67



$$B_9 = P24(R_1+S_1+T_1+U_1) + (R_2+S_2+T_2+U_2)P_1 + P_2(R_3+S_3+T_3+U_3)$$
$$+P_3(R_4+S_4+T_4+U_4) + (P_{24}-P_7)F_3\bar{F}_2\bar{F}_1(R_5+S_5+T_5+U_5)$$
$$+(P_{24}-P_7)F_3\bar{F}_2F_1(R_6+S_6+T_6+U_6) + (P_{24}-P_7)F_3F_2\bar{F}_1(R_7+S_7+U_7)$$
$$+(P_{24}-P_7)F_3F_2F_1(R_8+S_8+U_8)$$

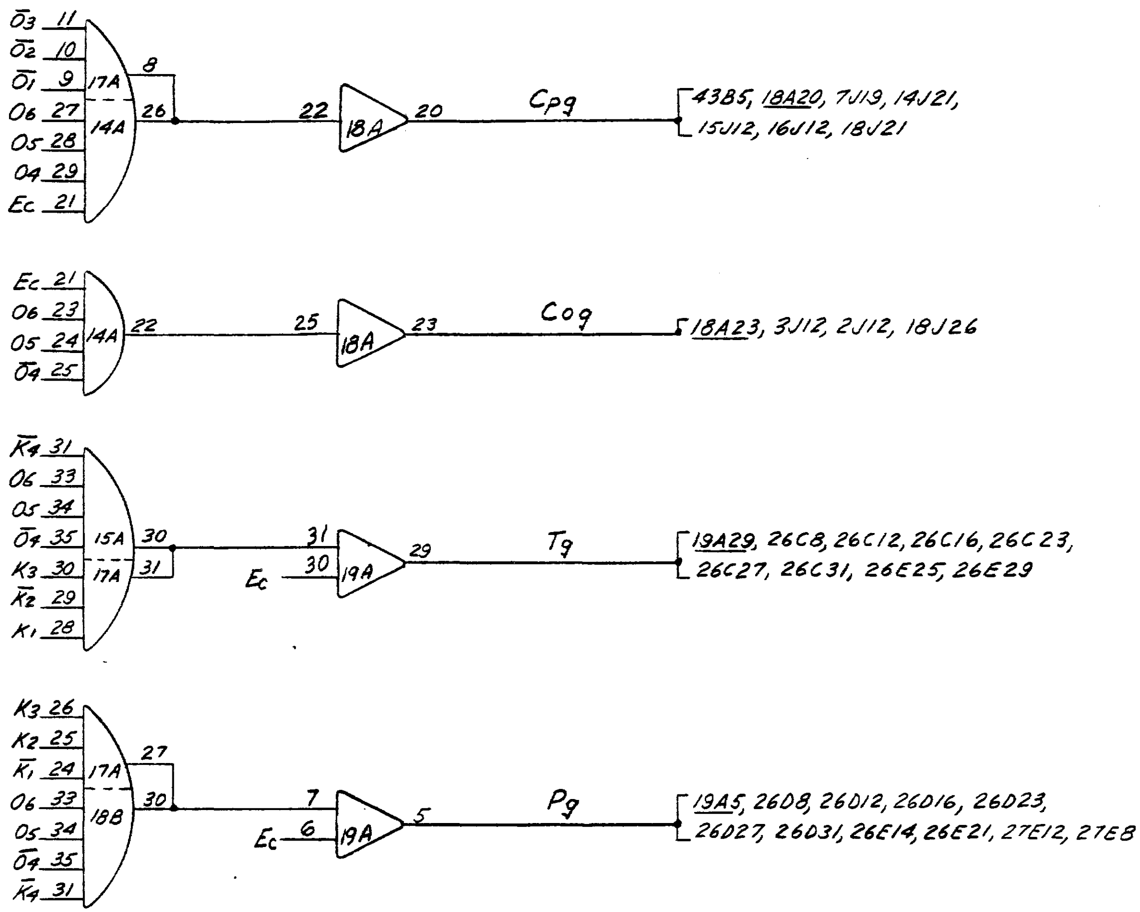
LOGIC LAYOUT

LOGIC SECT. CHARACTER INPUT TERM B_9

DWG. NO. 505782 T   DATE 1-6-62

DRAWN BY H. Mendelsohn   APP.

SH. 68



$$C_{pg} = E_c O_6 O_5 O_4 \bar{O}_3 \bar{O}_2 \bar{O}_1$$

$$C_{og} = E_c O_6 O_5 \bar{O}_4$$

$$T_g = E_c O_6 O_5 \bar{O}_4 K_3 \bar{K}_2 K_1 \bar{K}_4$$

$$P_g = E_c O_6 O_5 \bar{O}_4 K_3 K_2 \bar{K}_1 \bar{K}_4$$

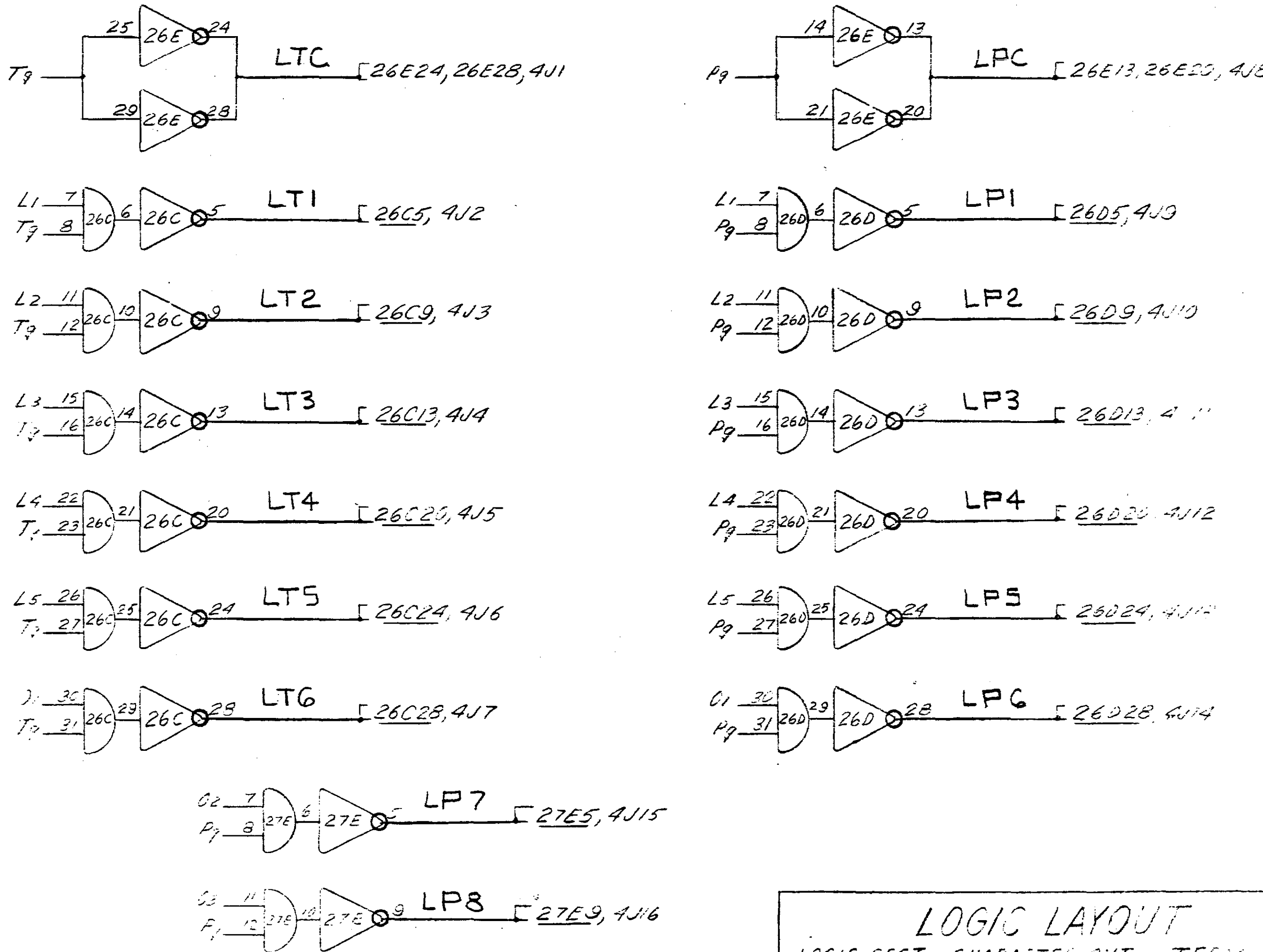
LOGIC LAYOUT

LOGIC SECT. CHAR. & CONT. OUT TERM ______

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP. ______

SH. 69



LOGIC LAYOUT

LOGIC SECT. CHARACTER OUT. TEF

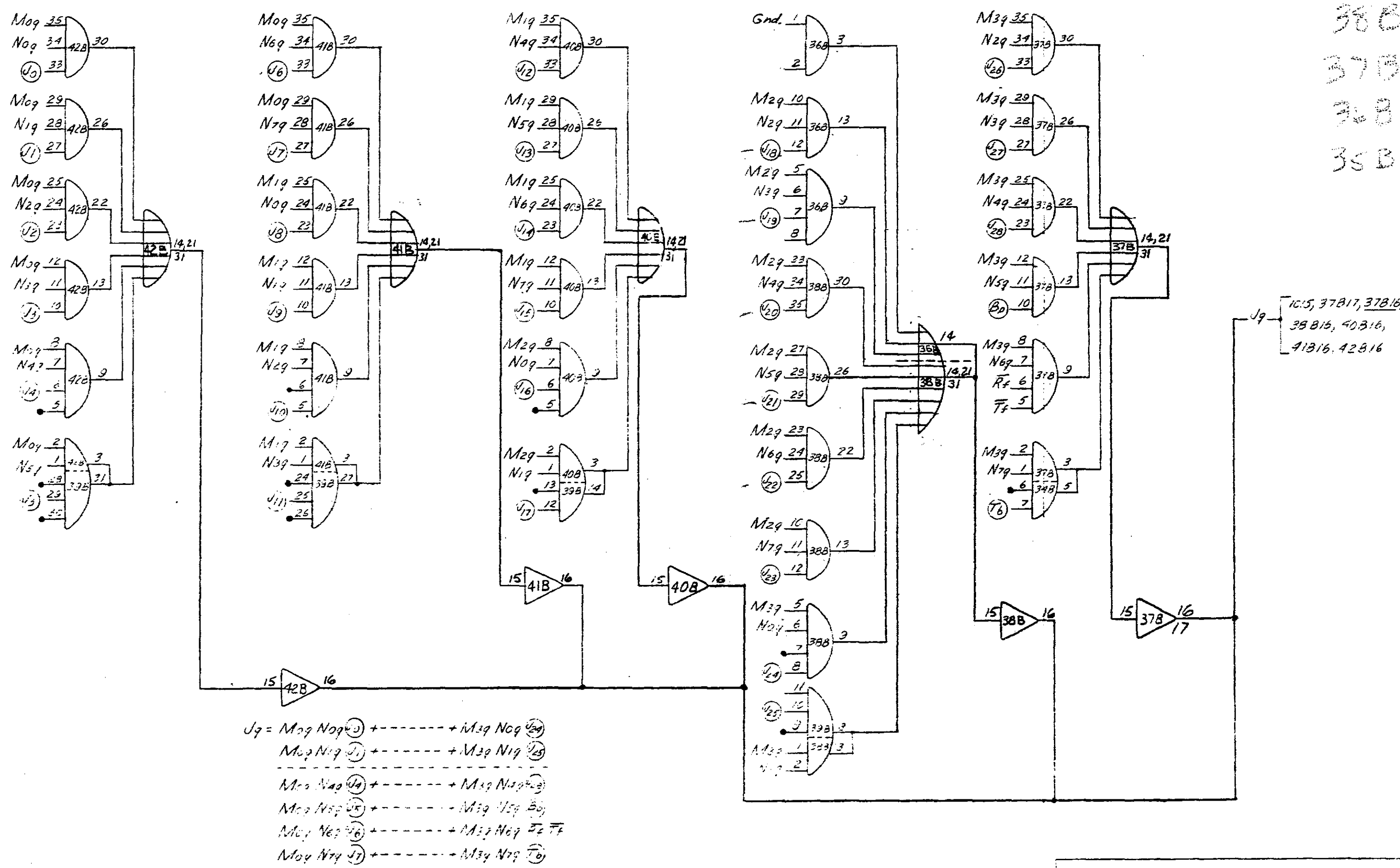
DWG. NO. 505782 T DATE 1-6-61

DRAWN BY H. [illegible] APP.

SH. 70

Available
38B
37B
36B
35B

6-79

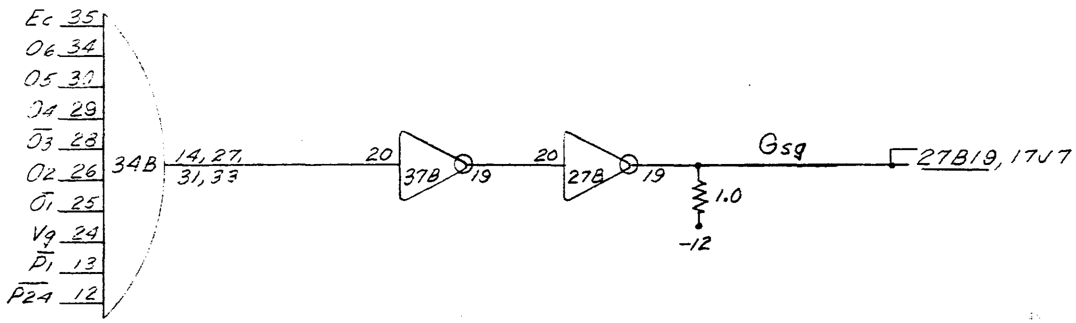


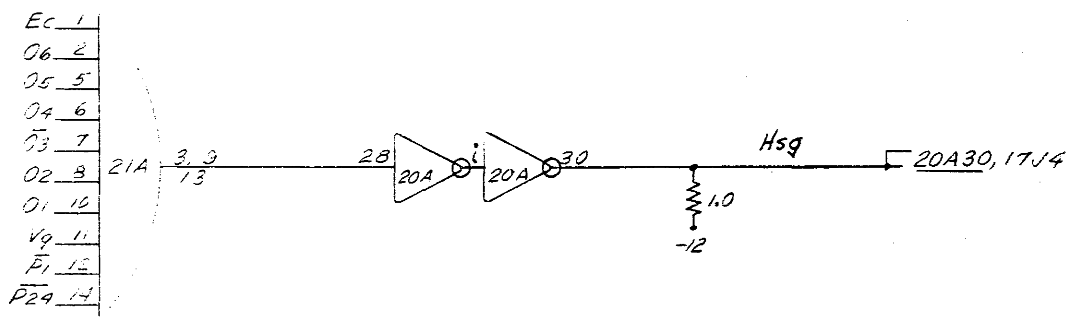
LOGIC LAYOUT

505782 T

1-6-62

SH. 71





$Gsq = Ec\ O6\ O5\ O4\ \overline{O3}\ O2\ \overline{O1}\ Vq\ \overline{P1}\ \overline{P24}$

$Hsq = Ec\ O6\ O5\ O4\ \overline{O3}\ O2\ O1\ Vq\ \overline{P1}\ \overline{P24}$

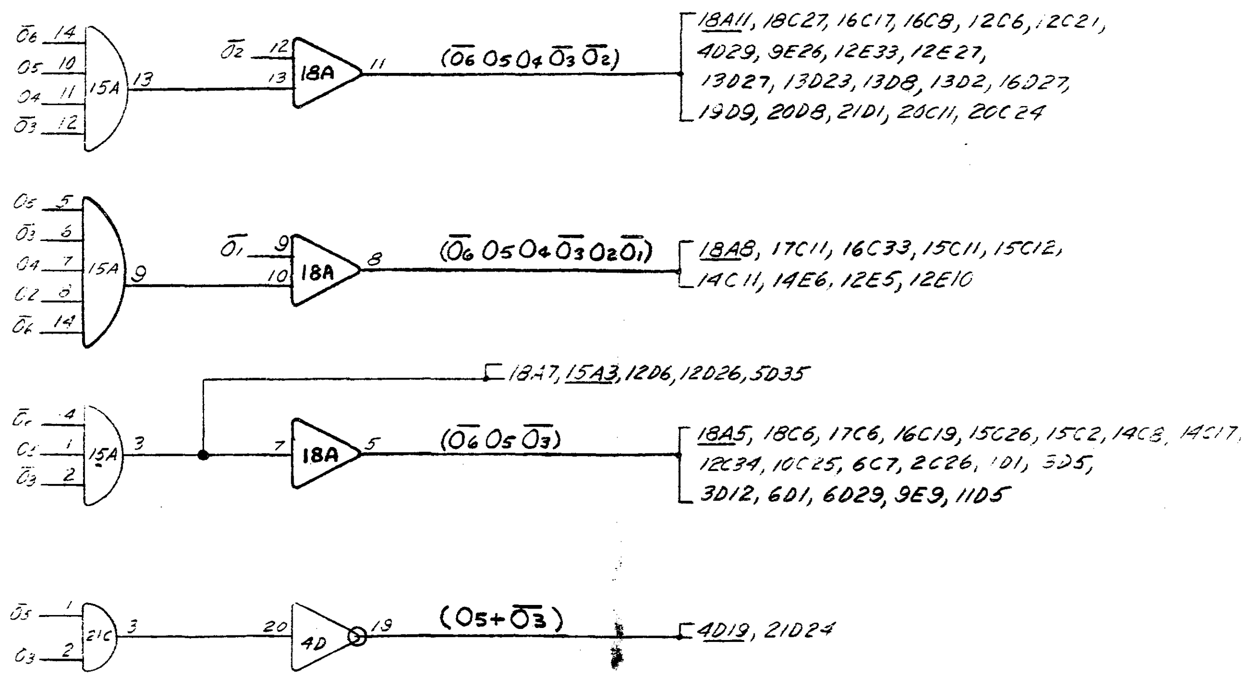
LOGIC LAYOUT

LOGIC SECT. SERIAL IN/OUT TERM

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 72



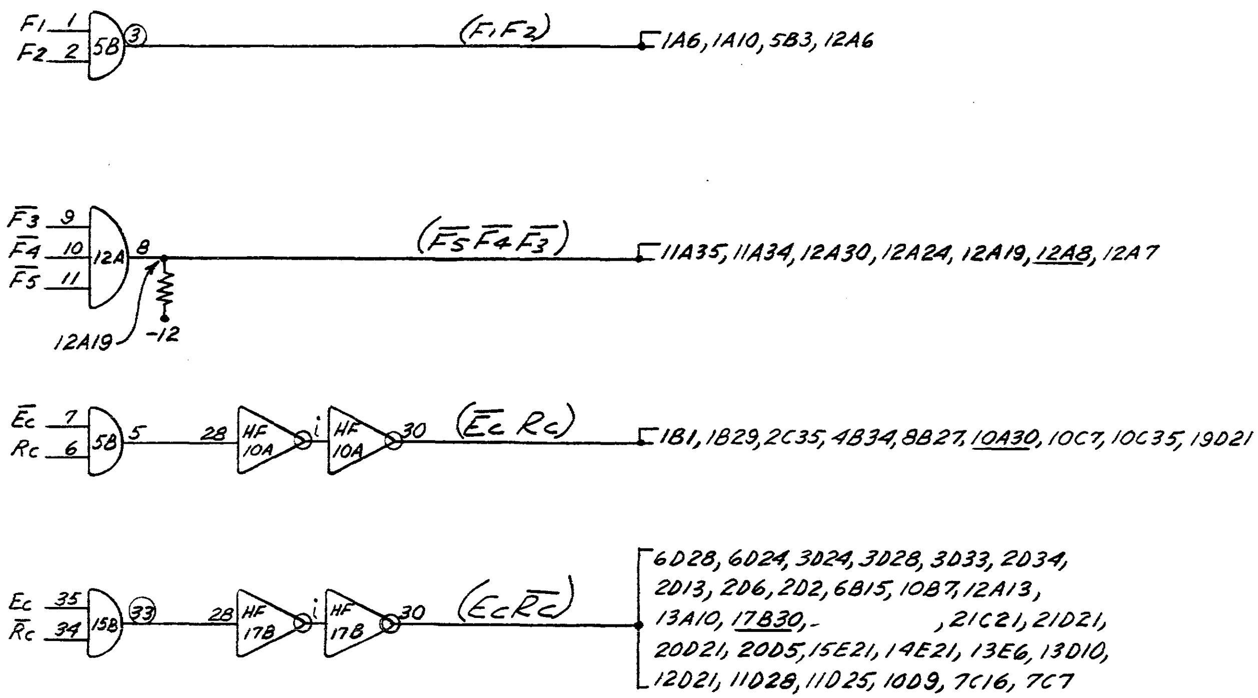
LOGIC LAYOUT

LOGIC SECT. DIST. LOGIC TERM

DWG. NO. 505782 T DATE 1-6-62

DRAWN BY H. Mendelsohn APP.

SH. 73



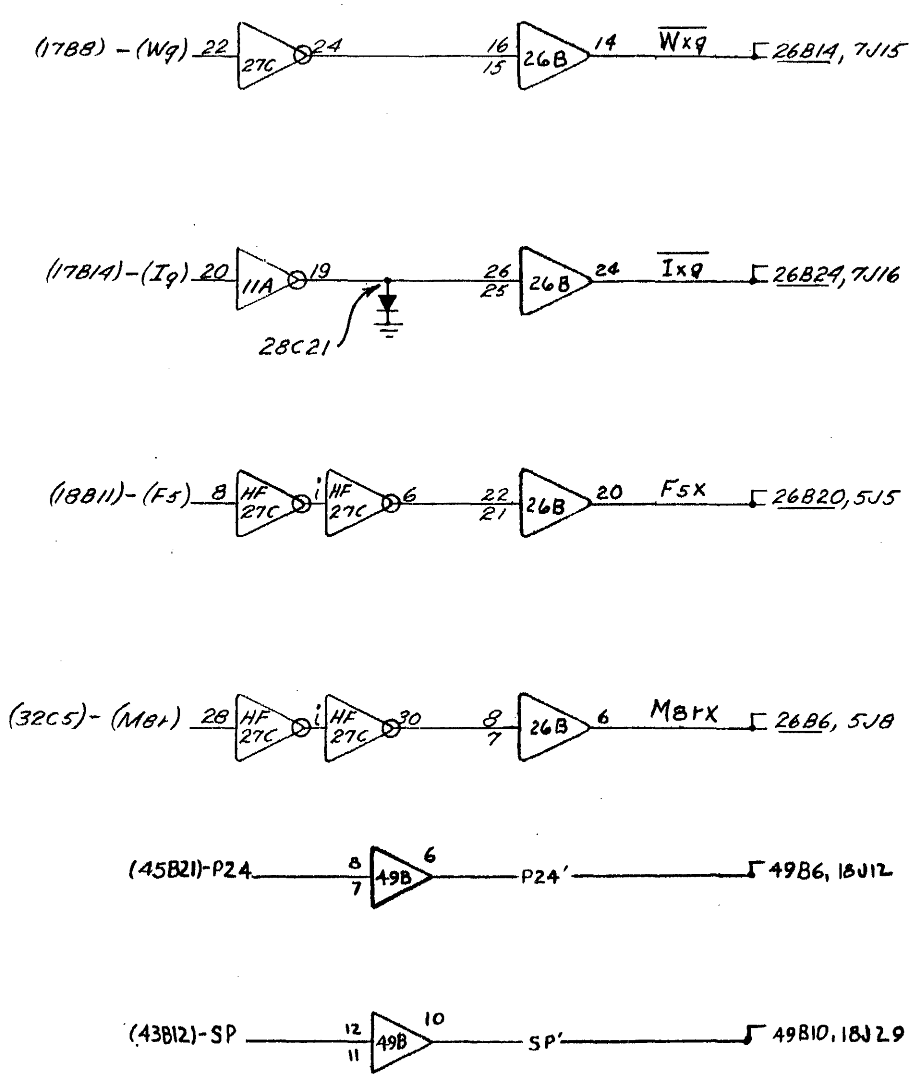
LOGIC LAYOUT

LOGIC SECT. DIST. LOGIC TERM ______

DWG. NO. 505782 T DATE 1-9-62

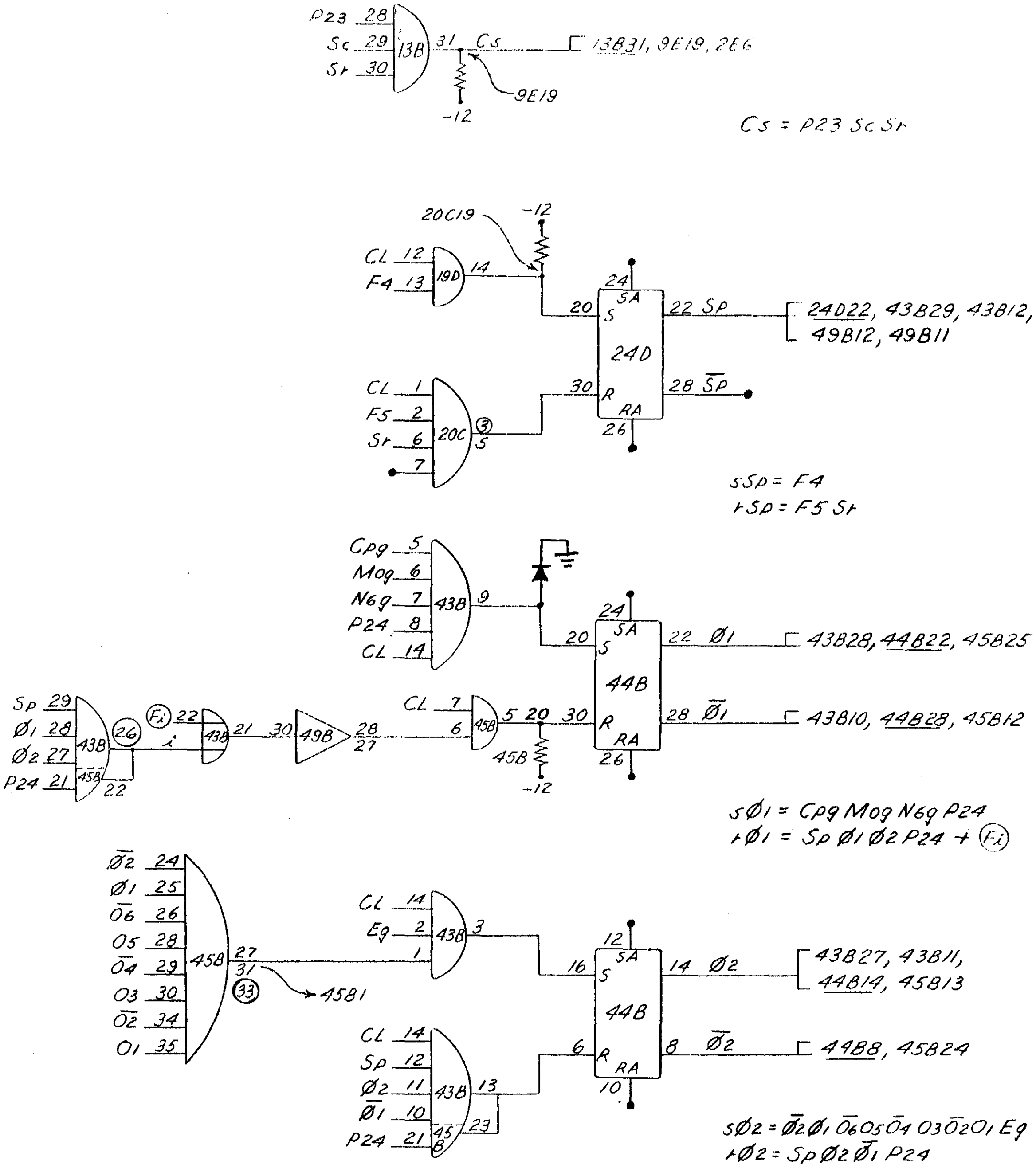
DRAWN BY H. Mendelsohn APP. ______

SH. 74



LOGIC LAYOUT

LOGIC SECT. ________ TERM ________
DWG. NO. 505782 T DATE 1-6-62
DRAWN BY H. Hendrickson APP. ________
SH. 75



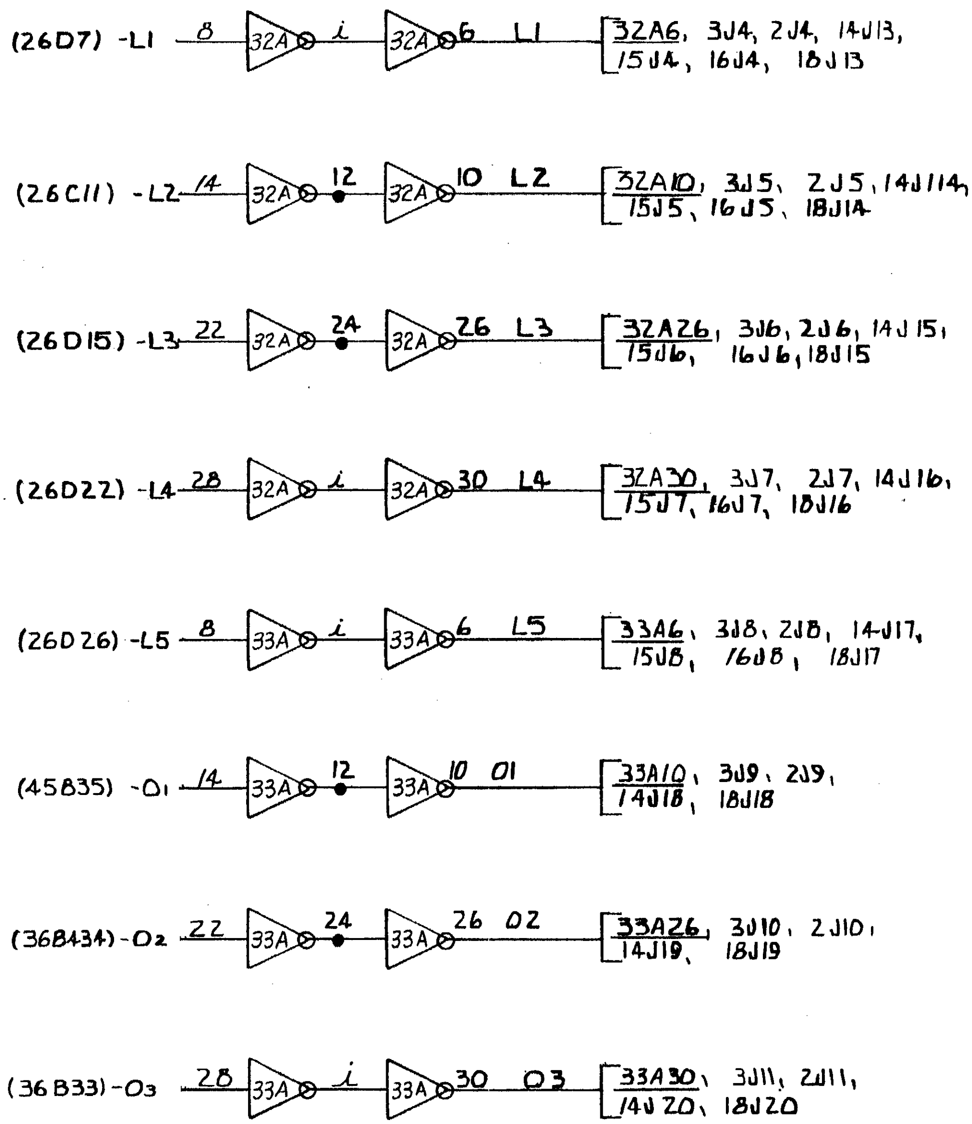
LOGIC LAYOUT

LOGIC SECT. ________ TERM Cs, Sp, Ø1, Ø2

DWG. NO. 505782 T DATE 1-9-62

DRAWN BY H. Mendelsohn APP. ________

SH. 76



LOGIC LAYOUT

LOGIC SECT SIGNAL BUFFERING TERM ______

DWG NO. 505782 U ______ DATE 2-2-62

DRAWN BY K. WOODIE APP. ______

SH. 77

VII. ENGINEERING DRAWINGS

This section contains engineering drawings. Table 7-1 lists the drawing number, title, and page number of drawings applicable to the PB250 Computer.

Table 7-1.

ENGINEERING DRAWINGS

Drawing No.	FIG Title	Page
1C2503	CD-100 Schematic 7-1	7-2
1C2333	DG-100 Schematic 7-2	7-3
1C2320	DG-101 Schematic 7-3	7-4
1C2335	DG-102 Schematic 7-4	7-5
1C2426	EF-100 Schematic 7-5	7-6
1C4535	EF-101 Schematic 7-6	7-7
1C4496	FC-100 Schematic 7-7	7-8
1C2477	GD-100 Schematic 7-8	7-9
1D2429	MSR-1 Schematic 7-9	7-10
1D2472	MSR-2 Schematic 7-10	7-11
1C2449	TD-100 Schematic 7-11	7-12
1C2425	TF-100 Schematic 7-12	7-13
1D6519	XCG-101 Schematic 7-13	7-14
1D4593	PB250 Module Location Diagram	7-15
1J4985	PB250 DC Power Wiring Installation Drawing	7-17
1D5623	PB250 Component Installation Drawing	7-19
1D4224	PB250 Connector Location Diagram	7-20
1C4597	PB250 AC Power Schematic	7-21
1D4411	Indicators Schematic	7-22

FIRST	LAST	DELETED
C1	C8	
CR1		
Q1	Q8	
R1	R29	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, 1/4 W.
2. ALL CAPACITORS ARE IN UUF.
3. ALL TRANSISTORS ARE 2N1500.
4. CR1 TO BE PER PBCC DWG NO. 358-1A3050.

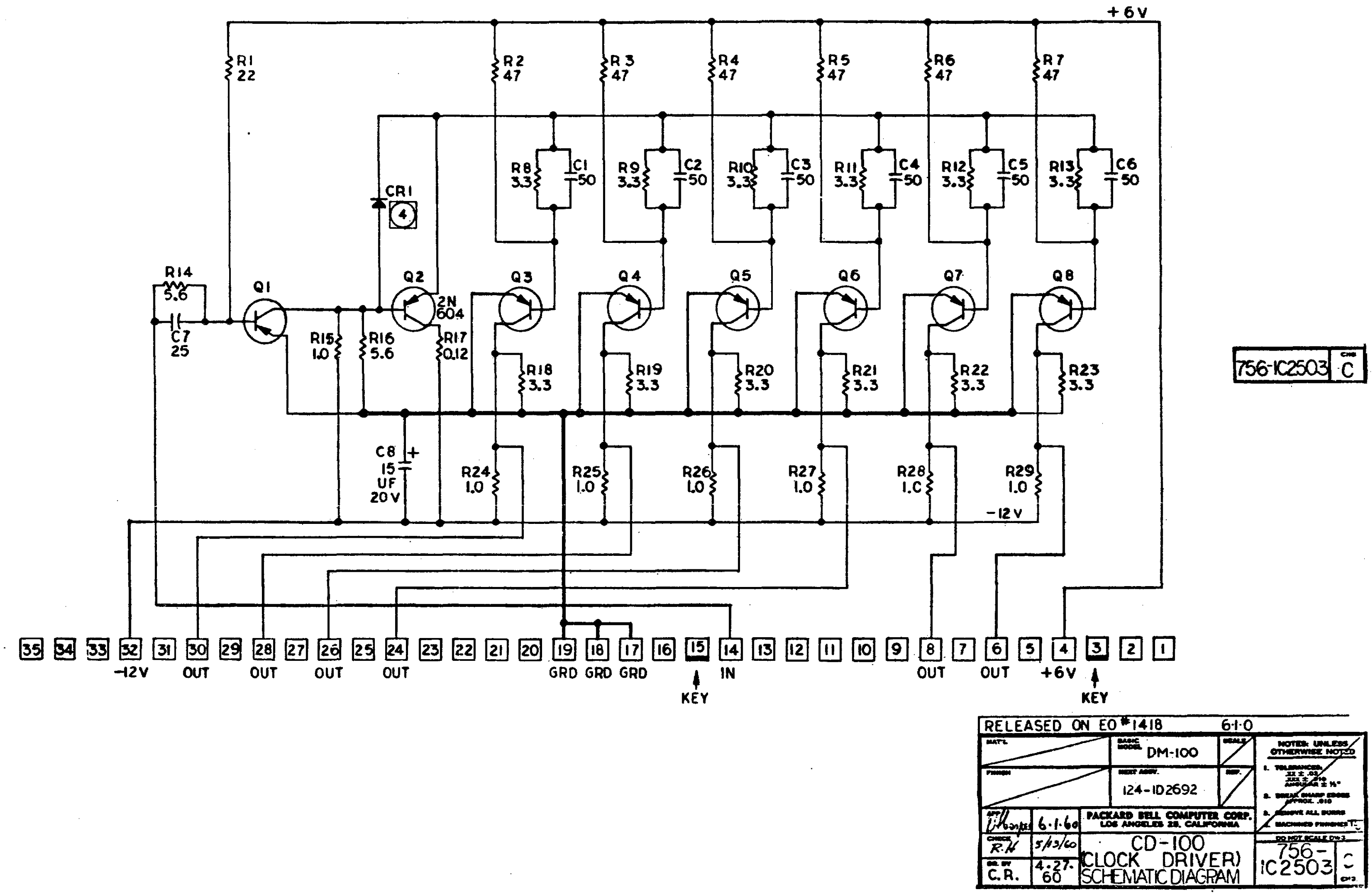
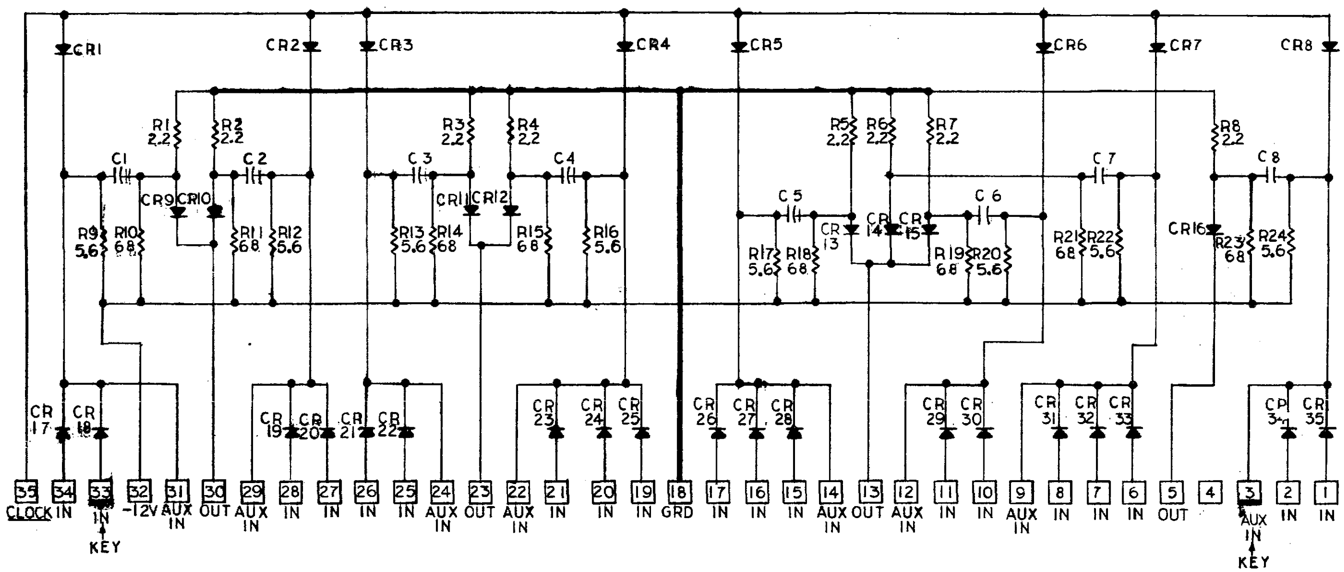


Figure 7-1 CD-100 Schematic

FIRST	LAST	DELETED
R1	R24	
C1	C8	
CR1	CR35	

NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE IN KILOHMS ±5%,1/4 W.
2 ALL DIODES TO BE PER PBCC DWG NO. 358-1A3C50.
3 ALL CAPACITORS ARE 50UUF.

NOTE; all Resistors valued @ 68 are 6,8K



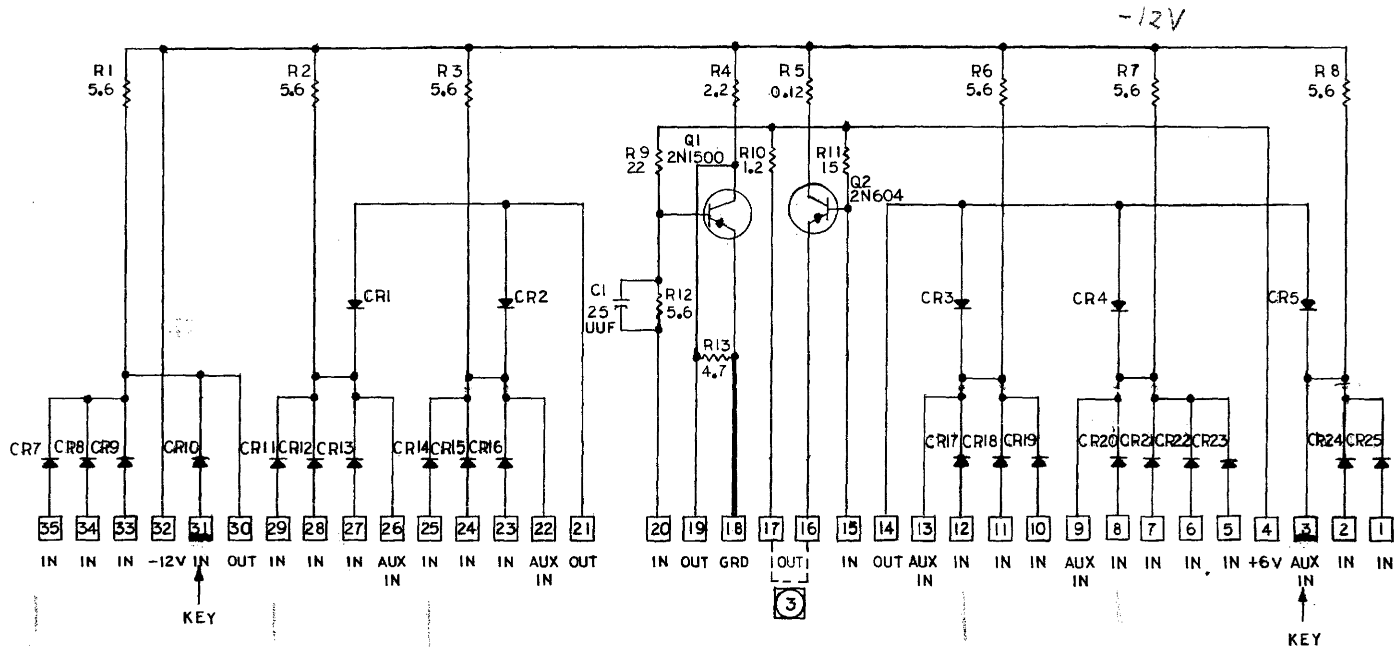
756-1C2333 C

RELEASED ON EO #1418 6-1-0			
MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED 1. TOLERANCES: .XX ± .03 .XXX ± .010 ANGULAR ± ½° 2. BREAK SHARP EDGES APPROX. .010 3. REMOVE ALL BURRS 4. MACHINED FINISHES
FINISH	NEXT ASSY. 124-1D2334	REF.	
[signature] 6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		DO NOT SCALE DWG.
CHECK RH 5/1/60	DG-100 SCHEMATIC DIAGRAM	756-1C2333	C CHG.
DR. BY p.j.d. 3/28/60			

Figure 7-2 DG-100 Schematic

FIRST	LAST	DELETED
R1	R13	
C1	C1	
CR1	CR25	CR6
Q1	Q2	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4 W.
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3. WHEN PARALLELING EMITTER FOLLOWERS, THE CONNECTION BETWEEN CONTACT TERMINAL 16 & 17 IS OMITTED.



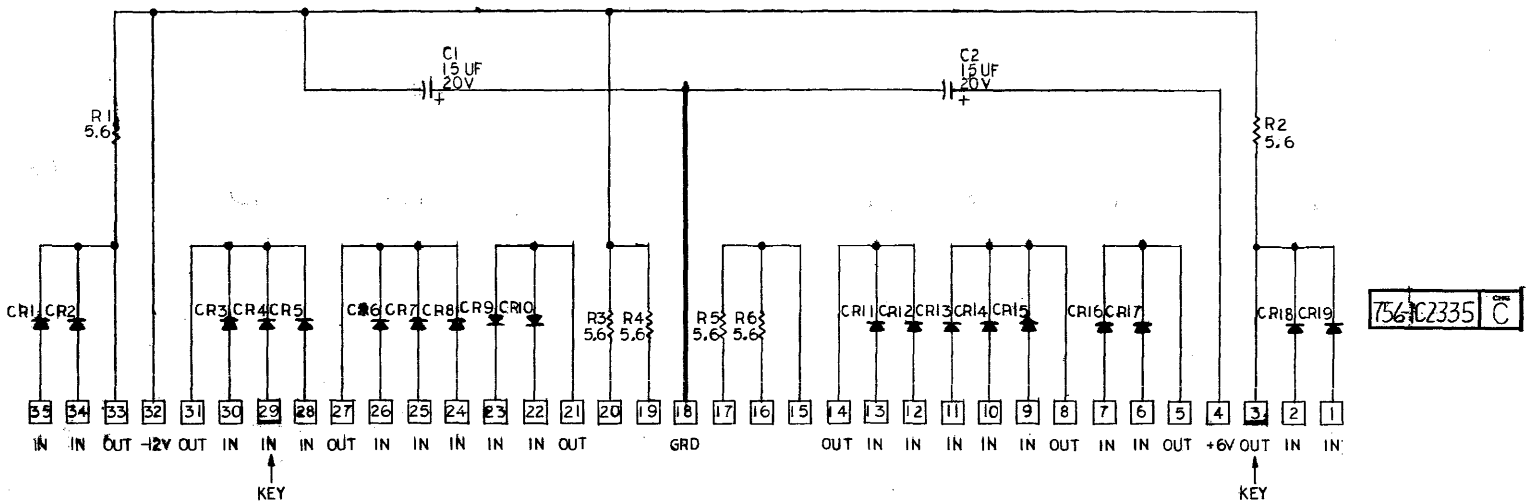
RELEASED ON EO# 1418 6-1-0

MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	NEXT ASSY. 124-1D2321	REF.	
APPD 6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		
CHECK 5/5/60	DG-101 SCHEMATIC DIAGRAM	756-1C2320	E
DR. BY PJD 3-17-60			

Figure 7-3 DG-101 Schematic

FIRST	LAST	DELETED
C1	C2	
CR1	CR19	
R1	R6	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4W
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.



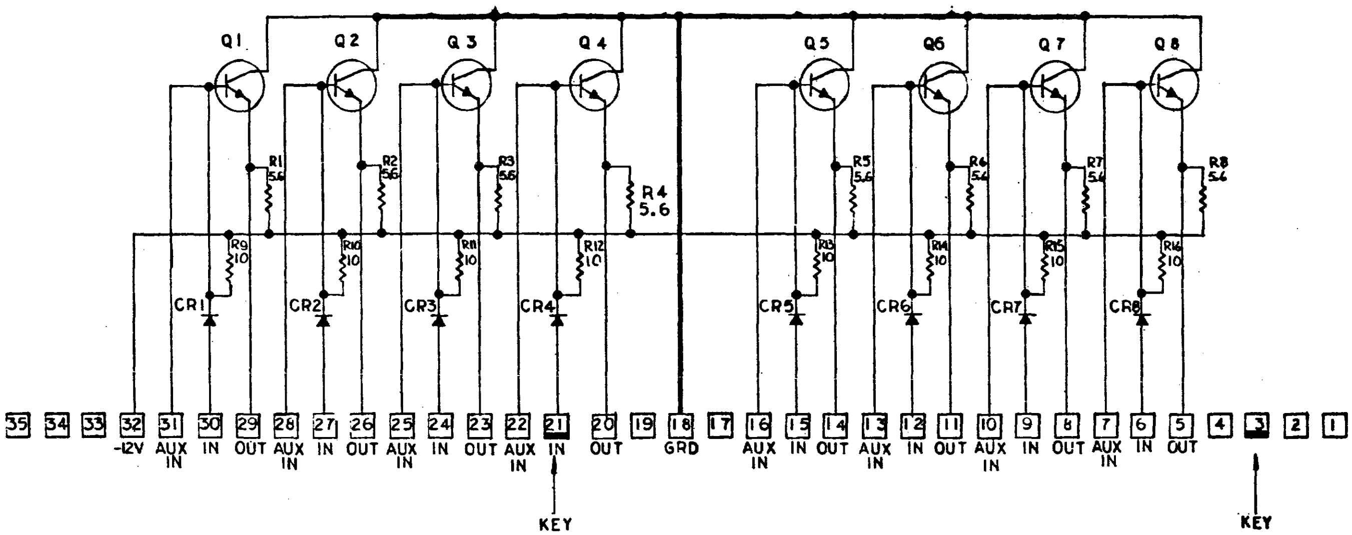
RELEASED ON EO # 1418	6-1-60		
MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED 1. TOLERANCES: .XX ± .03 .XXX ± .010 ANGULAR ± ½° 2. BREAK SHARP EDGES APPROX. .010 3. REMOVE ALL BURRS 4. MACHINED FINISHES
FINISH	NEXT ASSY. 124-1D2336	REF.	DO NOT SCALE DWG.
APP. [signature] 6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		
CHECK RH 3/5/60	DG-102 SCHEMATIC DIAGRAM	756-1C2335	C CHG.
DR. BY PJD 3-18-60			

Figure 7-4 DG-102 Schematic

FIRST	LAST	DELETED
CR 1	CR 8	
Q 1	Q 8	
R 1	R 16	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, 1/4W.
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3. ALL TRANSISTORS ARE 2N1605.



756-1C2426 C

RELEASED ON EO # 1418		6-1-0	
MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	NEXT ASSY. 124-1D2454	REF.	
6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		DO NOT SCALE DWG
CHECK 5/5/60	EF-100		
DR. BY pjd 4/18/60	SCHEMATIC DIAGRAM	756-1C2426 C	

Figure 7-5 EF-100 Schematic

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE PER PBCC DWG. NO. 358-1A3050
2. ALL RESISISTOR VALUES ARE IN KIL OHMS ±5% 1/4W
3. ALL TRANSISTORS ARE 2N604

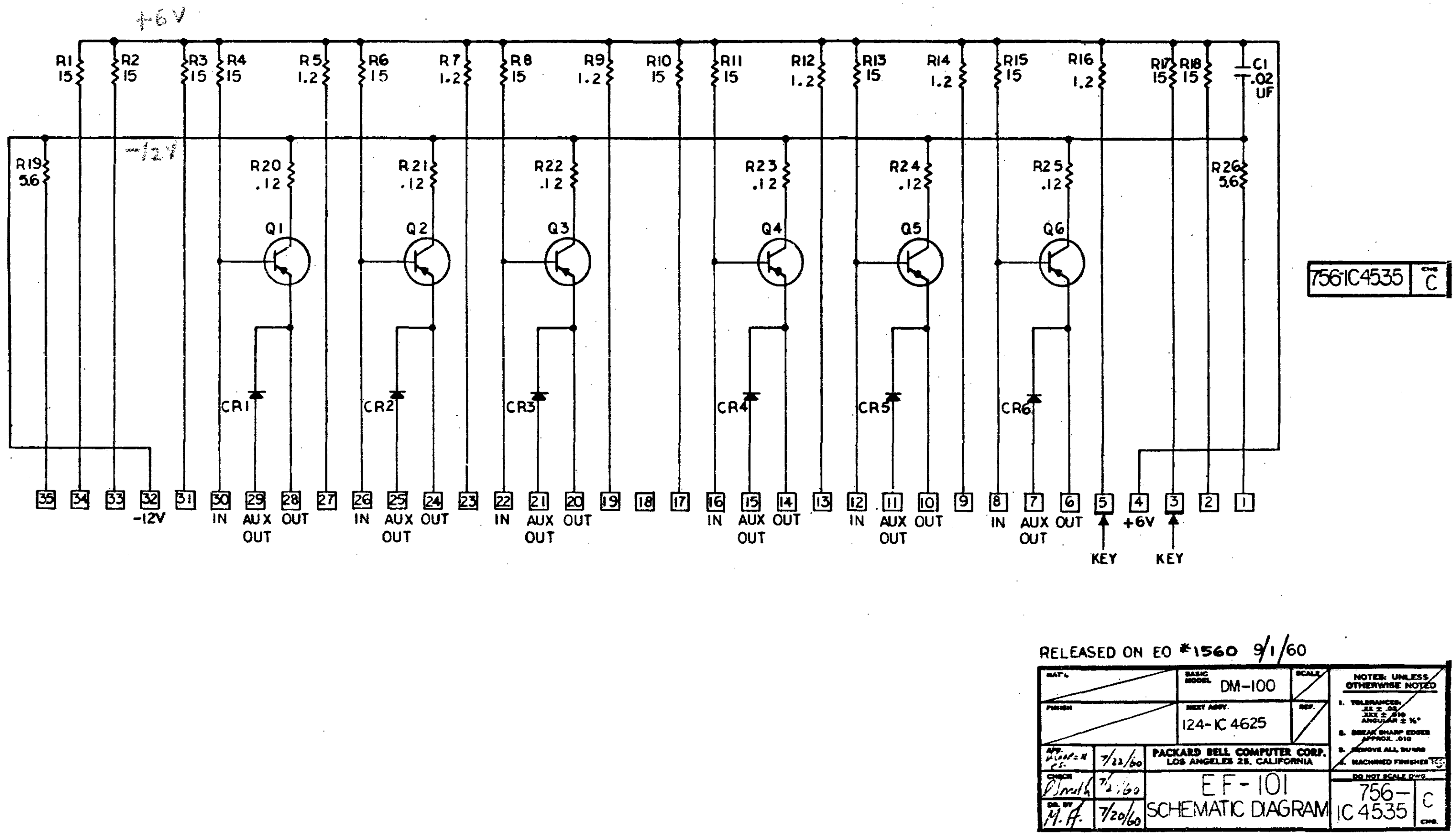


Figure 7-6 EF-101 Schematic

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050
2. ALL RESISTOR VALUES IN OHMS ±5% 1/4W.
3. CAPACITOR VALUES IN UF

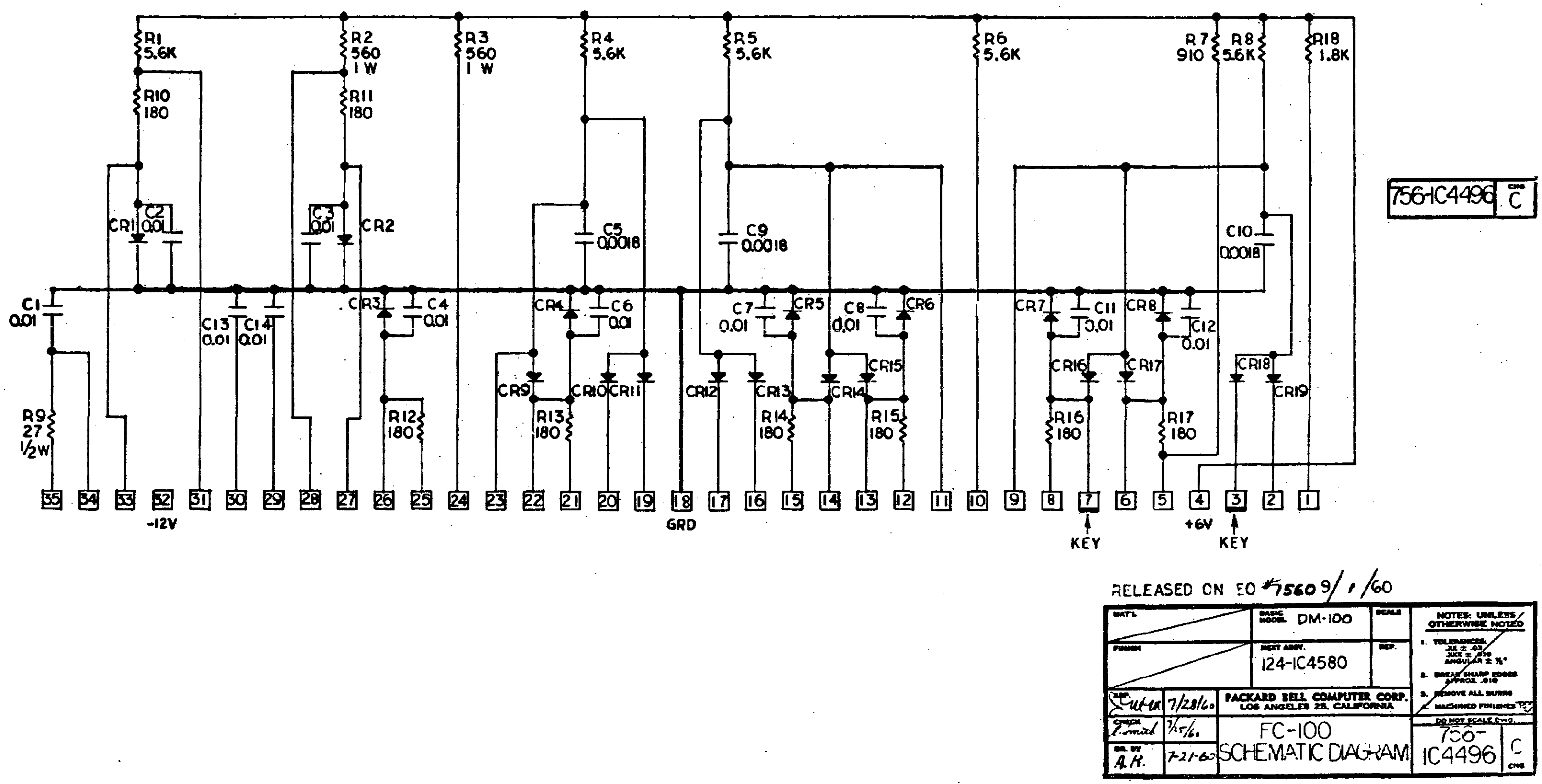
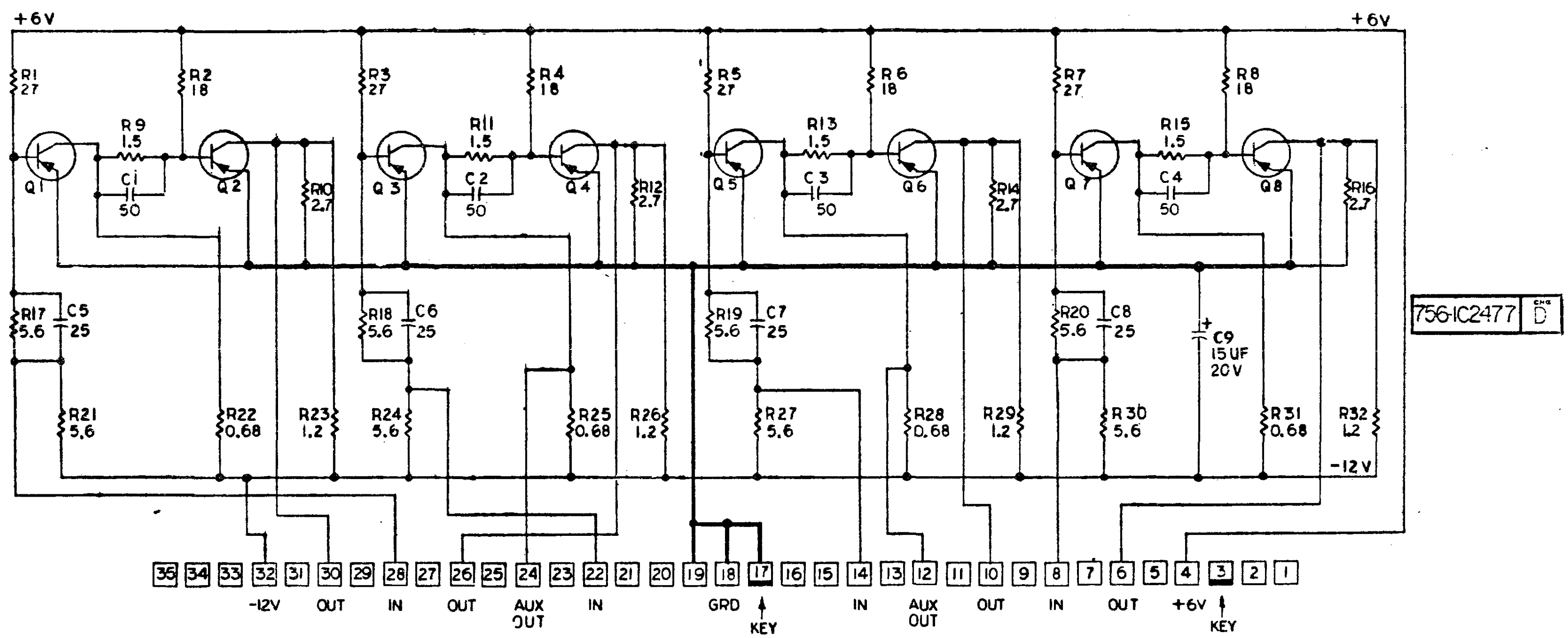


Figure 7-7 FC-100 Schematic

FIRST	LAST	DELETED
Q1	Q8	
R1	R32	
C1	C9	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES IN KILOHMS $\pm 5\%$, $\frac{1}{4}$W.
2. ALL CAPACITOR VALUES IN UUF.
3. ALL TRANSISTORS 2N1500.



756-1C2477 D

RELEASED ON EO# 1418 6-1-0

BASIC MODEL DM 100

NEXT ASSY. 124-1D2492

PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA

GD-100 SCHEMATIC DIAGRAM

756-1C2477

APP 6-1-60 | CHECK RK 6/5/60 | DR. BY M.C. 4-13-60

NOTES: UNLESS OTHERWISE NOTED 1. TOLERANCES: .XX ± .03, .XXX ± .010, ANGULAR ± ½° 2. BREAK SHARP EDGES APPROX. .010 3. REMOVE ALL BURRS 4. MACHINED FINISHES — DO NOT SCALE DWG.

Figure 7-8 GD-100 Schematic

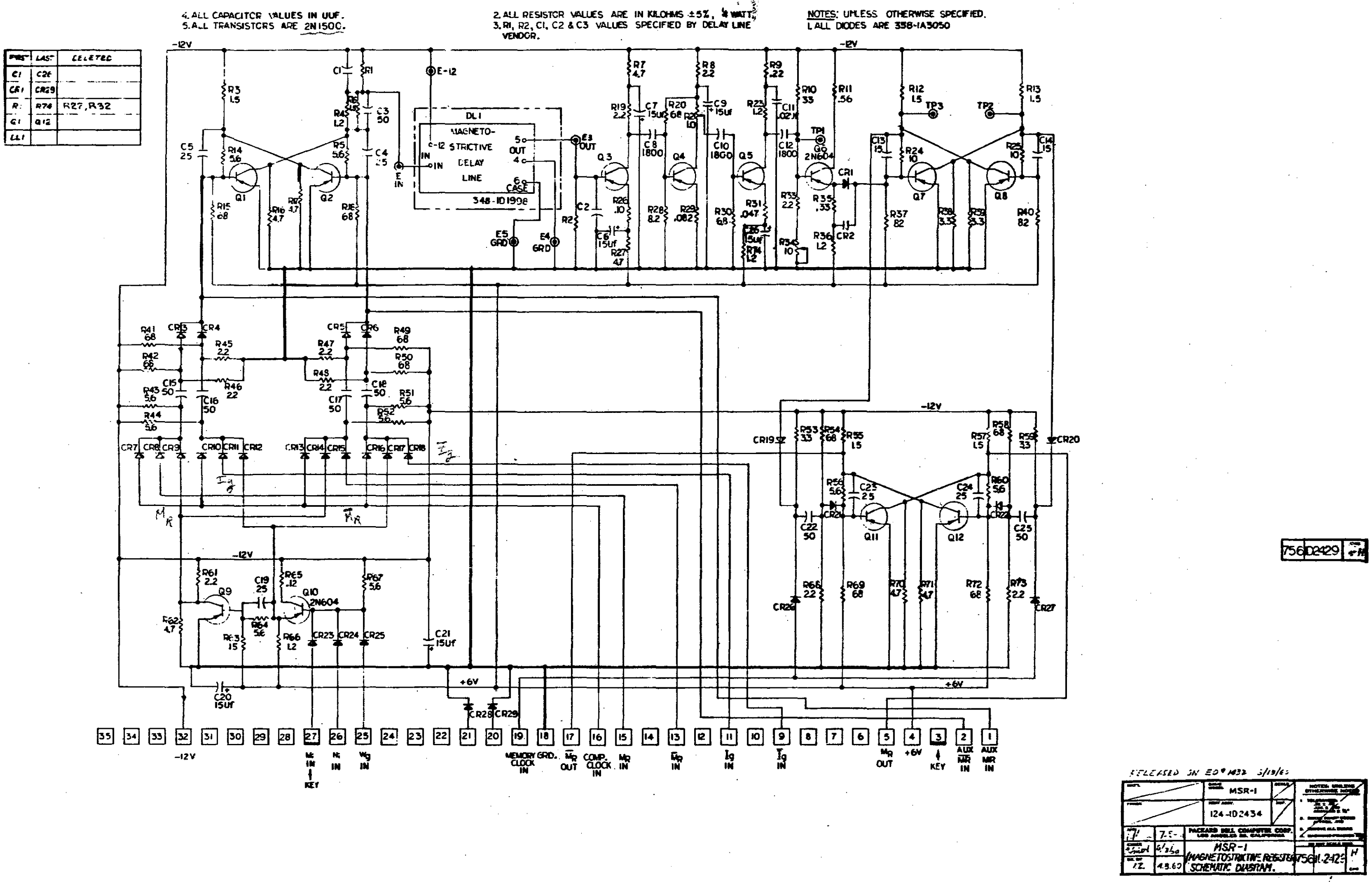


Figure 7-9 MSR-1 Schematic

256 words

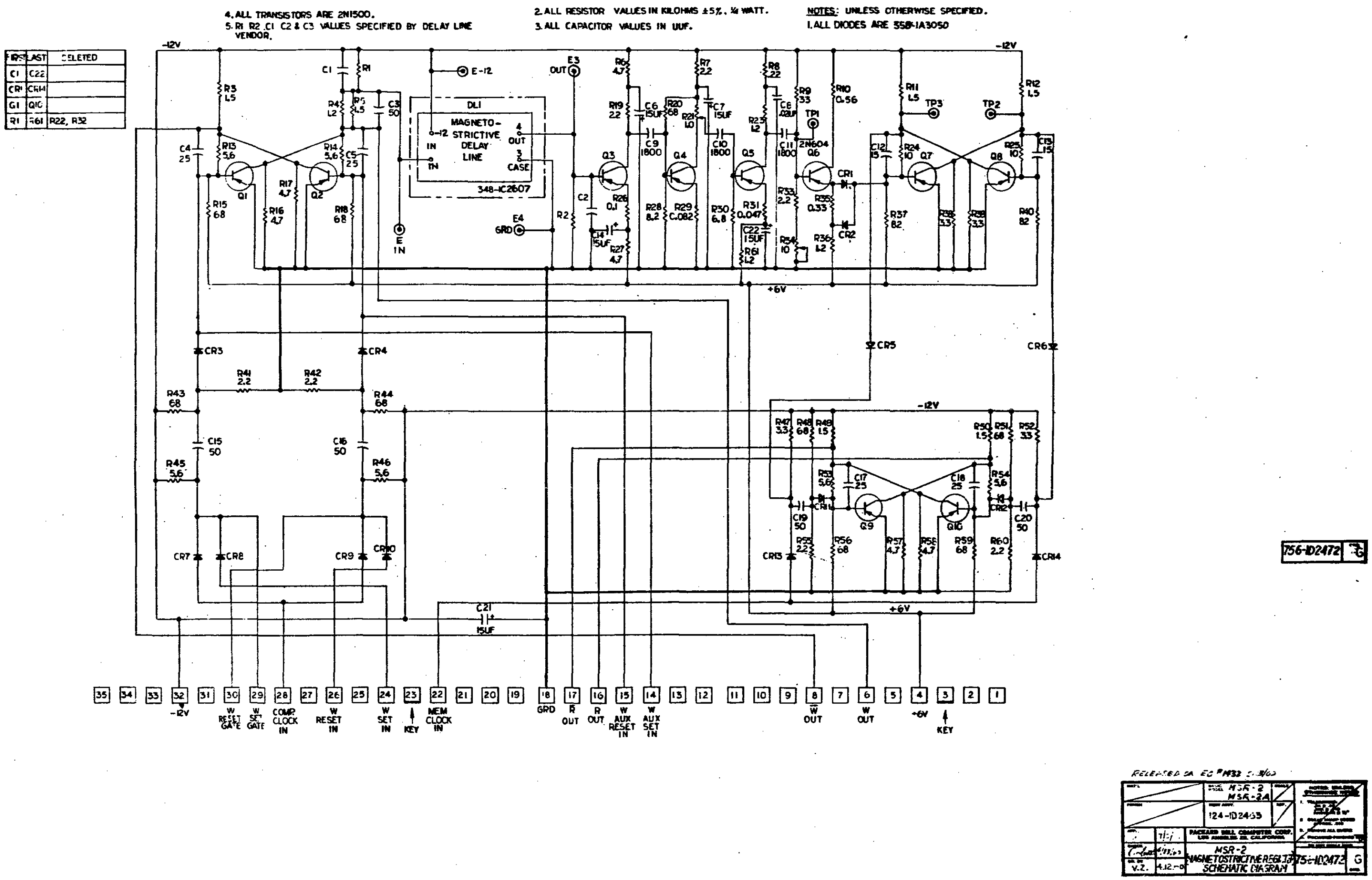
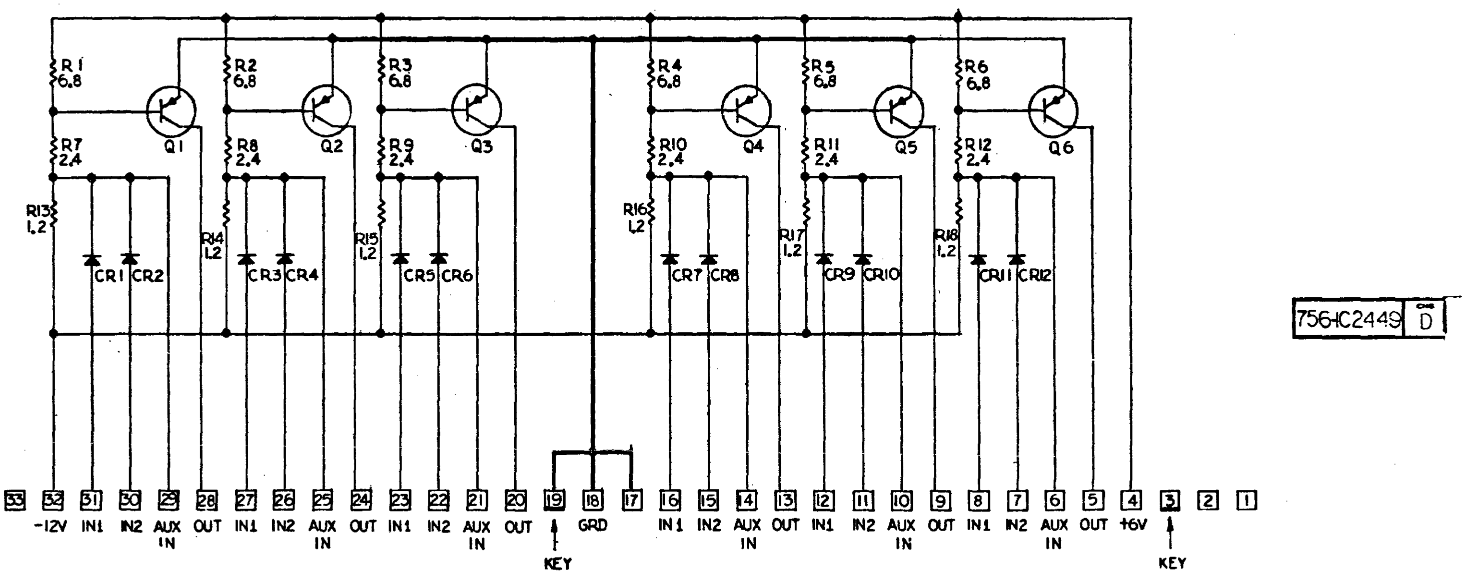


Figure 7-10 MSR-2 Schematic

FIRST	LAST	DELETED
Q1	Q6	
R1	R18	
CR1	CR12	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES IN KILOHMS ±5%, 1/4 W.
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3. ALL TRANSISTORS ARE 2N1184B.



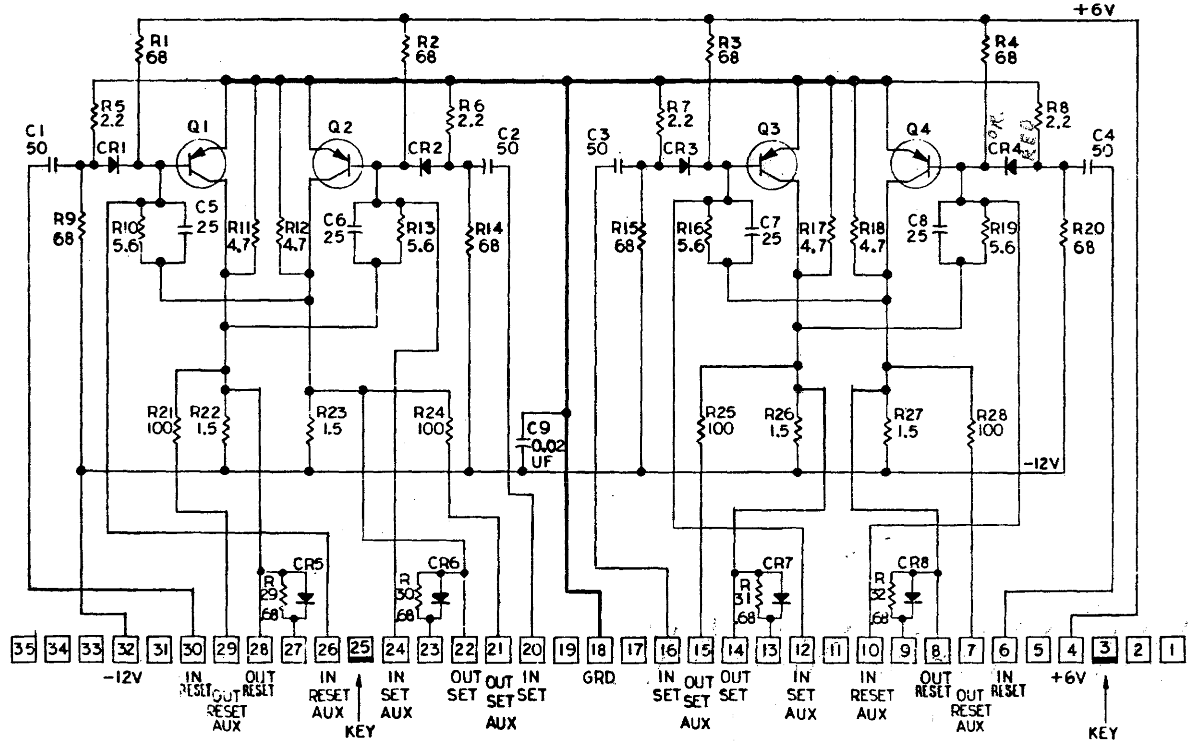
756-1C2449 D

RELEASED ON EO # 1418		6-1-0	
MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	NEXT ASSY. 124-1D2473	REF.	
DR. 6-1-60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		
CHECK 4/7/60	TD-100 (DRIVER)		756-
S.C. 4/7/60	SCHEMATIC DIAGRAM		1C2449 D

Figure 7-11 TD-100 Schematic

FIRST	LAST	DELETED
Q1	Q4	
R1	R32	
C1	C9	
CR1	CR8	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, 1/4 W.
2. ALL DIODES TO BE PER PBCC DWG NO.358-IA3050.
3. ALL CAPACITOR VALUES ARE IN UUF.
4. ALL TRANSISTORS ARE 2N1500



756-IC2425 | E

RELEASED ON EO #1418	6-1-0		
MAT'L	BASIC MODEL DM-100	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	NEXT ASSY. 124-1D2433	REF.	1. TOLERANCES: .XX ± .03, .XXX ± .010, ANGULAR ± ½° 2. BREAK SHARP EDGES APPROX. .010 3. REMOVE ALL BURRS 4. MACHINED FINISHES
APP. A.R.V. 11/15/60	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		DO NOT SCALE DWG
CHECK K.H. 9/5/60	TF-100	756-IC2425	E
DR. BY C.R. 4-5-60	SCHEMATIC DIAGRAM		CHG

Figure 7-12 TF-100 Schematic

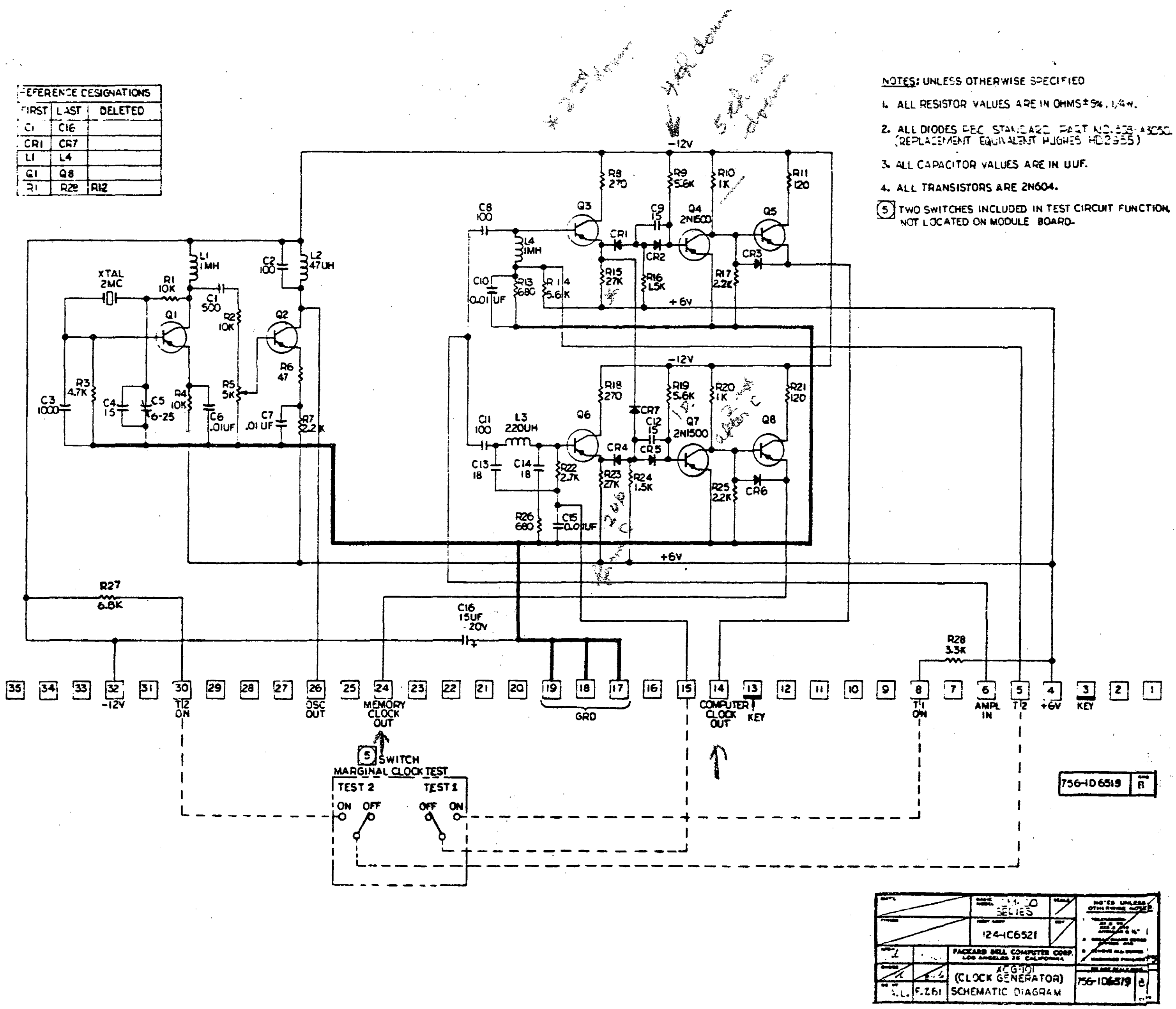


Figure 7-13. XCG-101 Schematic

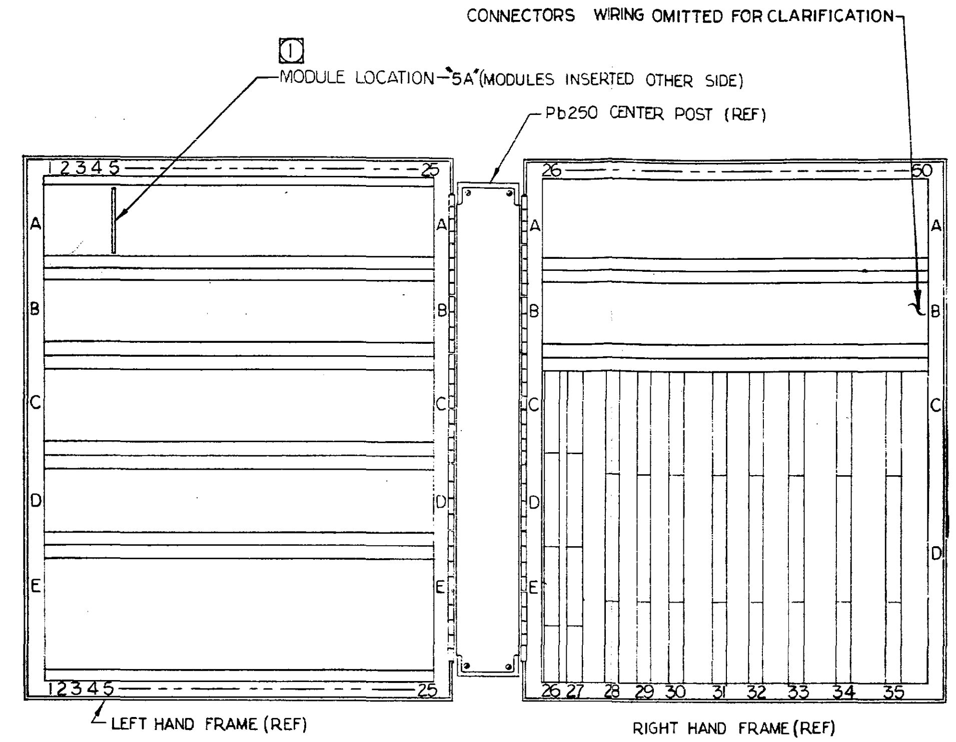
2. FOR MODULE CONNECTOR LOCATIONS SEE 350-1D4244.

NOTES: UNLESS OTHERWISE SPECIFIED

1. LOCATION "5A" AS SHOWN, WOULD BE THE ACTUAL LOCATION OF MODULE "TF-100" IN THE COMPUTER.

MODULE MODEL NO.

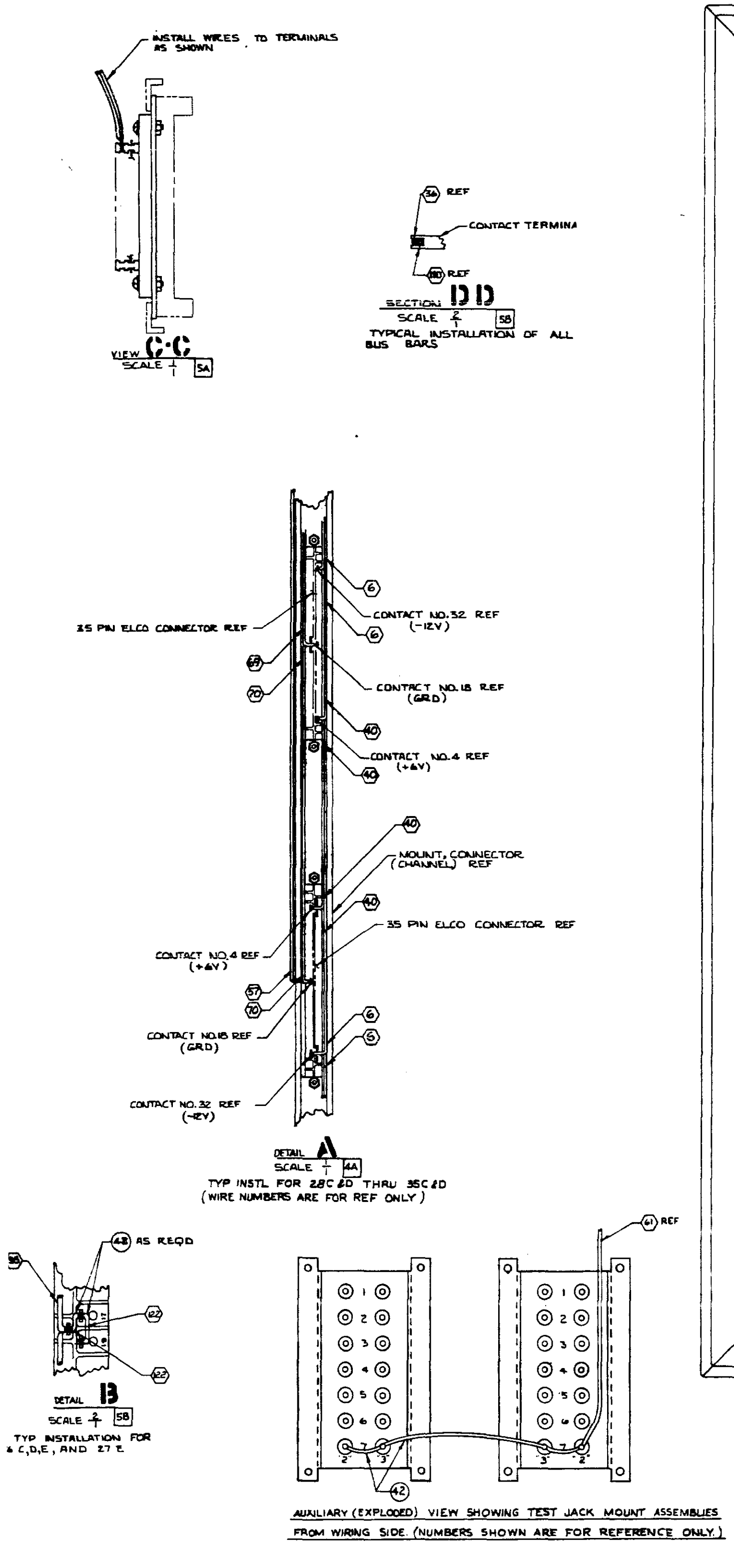
LOCATION IN FRAME ASSEMBLY	MSR-1B-191	~~XCG100~~	CD100	MSR-2	MSR-1B-3071	GD-100	EF-100	TF-100	DG-100	DG-101	DG-102	TD-100	FC-100	EF-101
	28 C	25 B	22 B	7 A		10 A	18 A	2 A	6 A	4 A	1 A	26 C	24 A	19E
				2 B	29 C	17 B	19 A	3 A	6 B	11 A	12 A	26 D	25 A	8E
				7 D	30 C	(27 C)	19 B	1 5 A	10 B	13 A	17 A	26 E	23 A	9A
				14 D	31 C	20E	23 C	7 B	20 B	14 A	5 B	27 E		23B
				22 D	26 D	20A	25 C	11 B	1 C	15 A	13 B			(22A)
					29 D	32A	~~32A~~	12 B	4 C	16 A	15 B			(26B)
					30 D	33A	~~33A~~	21 B	7 C	1 B	30 B			(29B)
					31 D		(25D)	3 C	9 C	4 B	34 B			
					32C			5 C	12 C	8 B	39 B			
					32D			8 C	14 C	9 B	2 C			
								11 C	16 C	14 B	6 C			
								13 C	18 C	16 B	10 C			
								17 E	16 D	18 B	15 C			
								19 C	17 D	27 B	17 C			
								9 D	16 E	28 B	21 C			
								18 D	5 E	29 B	24 C			
								6E		31 B	2 D			
								(44B)		32 B	5 D			
								(24D)		33 B	10 D			
										35 B	12 D			
										36 B	19 D			
										37 B	9 E			
										38 B	13 E			
										21 A	14 E			
										26A	15 E			
										28A	22 C			
										1 D	20 C			
										3 D	27A			
										4 D	29A			
										6 D	(45B)			
										11 D				
										13 D				
										20 D				
										21 D				
										10 E				
										11 E				
										12 E				
										18 E				
										40B				
										(41B)				
										42B				
										43B				
										[illegible]				

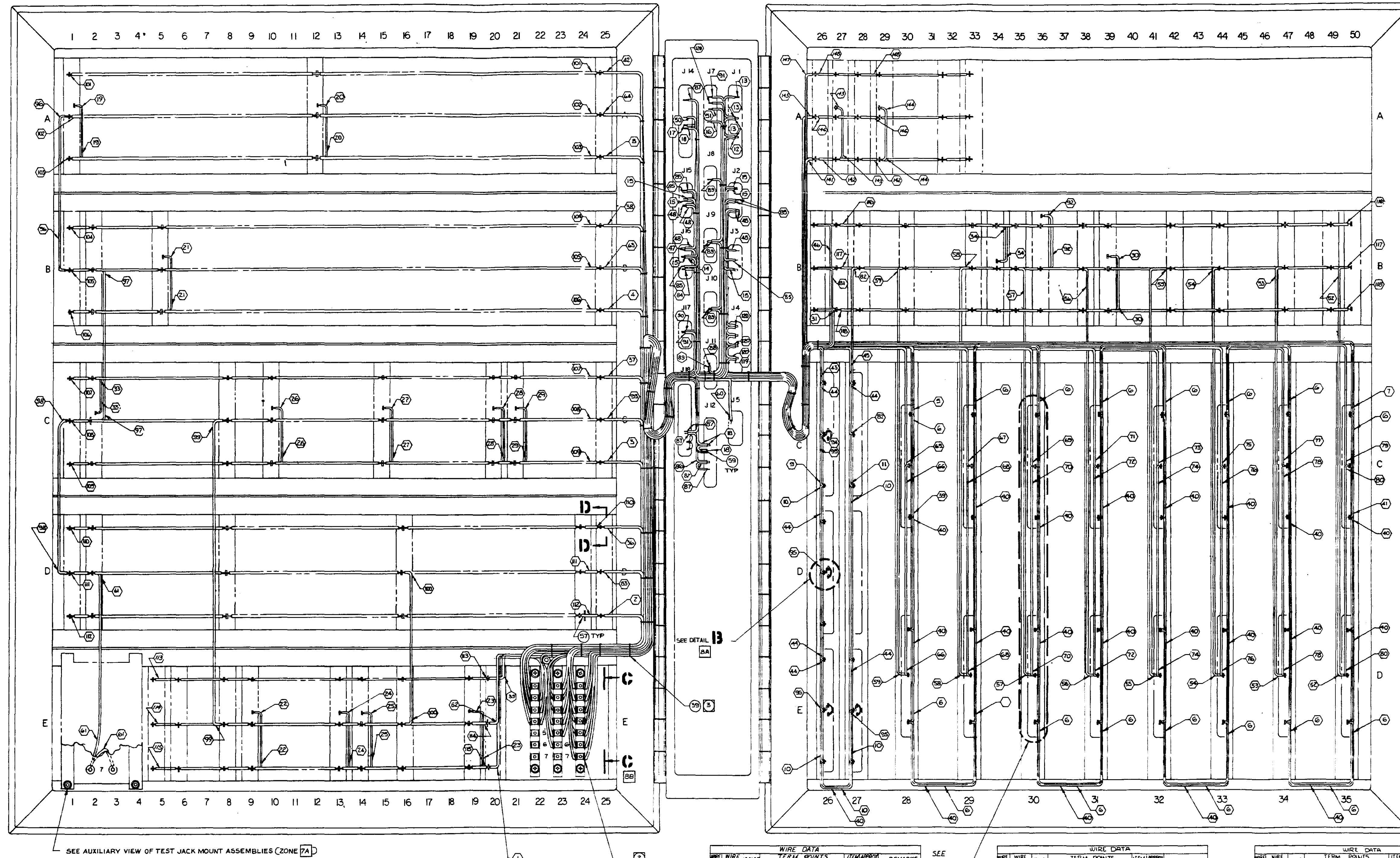


FRONT VIEW OF FRAME ASSEMBLIES (OPEN)-PB250 COMPUTER

MAT'L	BASIC MODEL PB-250	SCALE	NOTES: UNLESS OTHERWISE NOTED
FINISH	NEXT ASSY.	REF.	
	PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA		DO NOT SCALE DWG.
CHECK JH 8-1-60	PB250 MODULE LOCATION DIAGRAM	350-1D4593	G
DR. BY DE 7-28-60			

Figure 7-14 PB250 Module Location Diagram





WIRE NO.	WIRE GAUGE	COLOR	TERM POINTS FROM	TERM POINTS TO	ITEM NO.	APPROX LENGTH	REMARKS
141	16 SOLID	WHITE	23E1R →	26A32	57 58	7	-12V
142	16		26A32 THRU	33A32	57 58	3	-12V
143	24		27A32 →	27A15	42	2	-12V
144	24		29A32 →	29A15	42	2	-12V
145	16		24E7L →	26A18	57 58	7	GRD
146			26A18 THRU	33A18		3	GRD
147			22E4R →	26A4		5	+6V
148	16 SOLID	WHITE	26A4 THRU	33A4	57 58	3	+6V

SEE DETAIL A 8B

WIRE NO	WIRE GAUGE	COLOR	TERM POINTS FROM	TERM POINTS TO	ITEM NO.	APPROX LENGTH	REMARKS
125	24 SOLID	WHT	17A32 →	17A15	42	4	-12V
126			15B32 →	15B15			
127			13B32 →	13B15			
128			17C32 →	17C15			
129			22C32 →	22C15			
130			12D32 →	12D15			
131			10D32 →	10D15			
132	24 SOLID	WHT	24C32 →	24C15	42	4	-12 V

WIRE NO	WIRE GAUGE	COLOR	TERM POINTS FROM	TERM POINTS TO	ITEM NO	APPROX LENGTH	REMARKS
133	24 SOLID	WHT	06C32 →	6C15	42	4	-1
134			05D32 →	5D15			
135			15E32 →	15E15			
136			02D32 →	02D15			
137			35B18 → 35B13 → 35B09 →	35B13, 35B9, 35B03			
138			07A18 → 07A29 →	07A29, 07A30			
139			20C18 →	20C33			
140	24 SOLID	WHT	31B18 →	31B02	42	4	-1

Figu

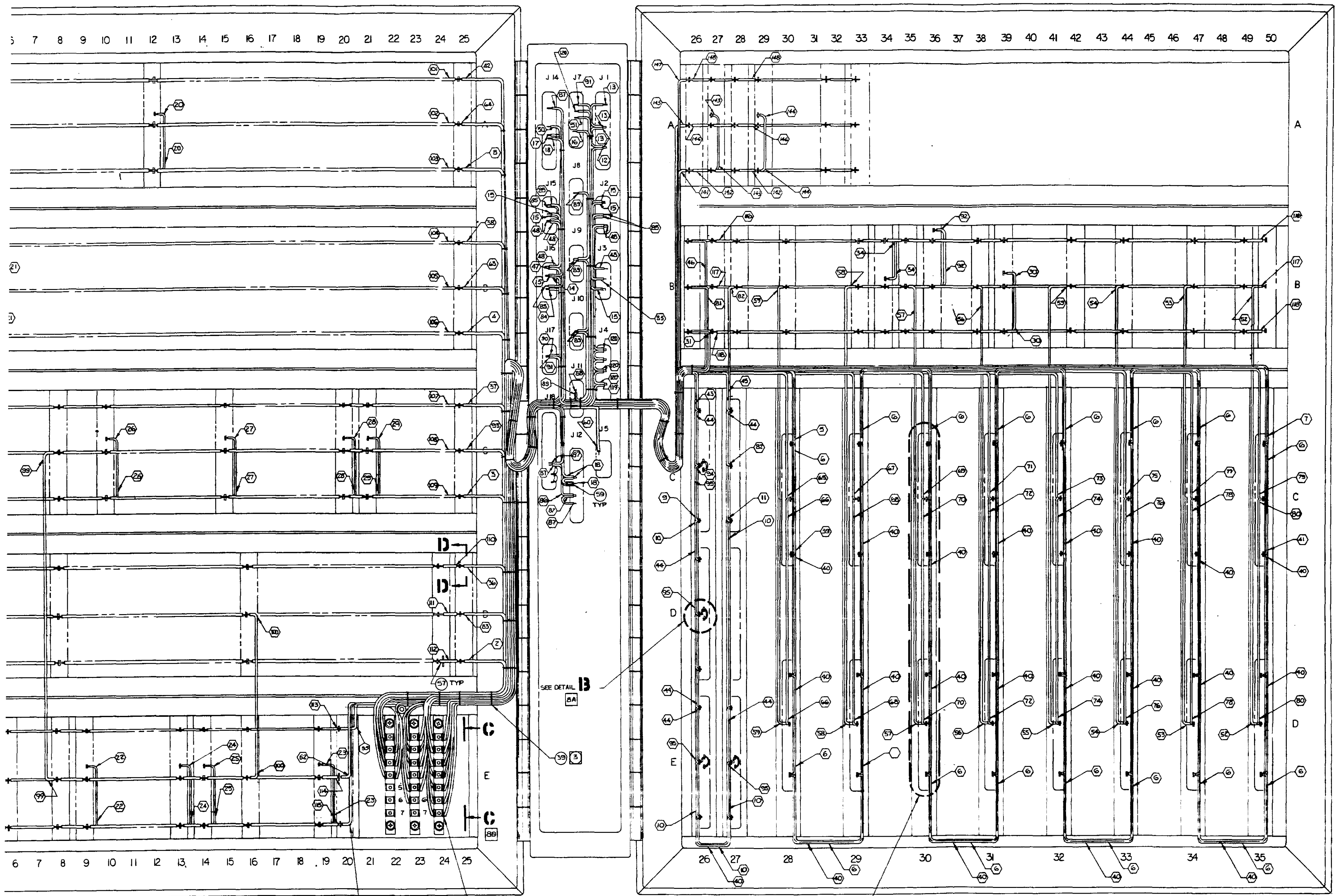
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE DRAWINGS:
DWG NO. 123-1J2617 PB250 ASSY
DWG NO. 954-1A4279 PB250 WIRING LIST

2. LOCATIONS 22E, 23E & 24E ARE AFFIXED WITH "L" OR "R" MEANING LEFT OR RIGHT SIDE OF TERMINAL. EX; WIRE 62 GOES FROM 24E7R WHICH IS RIGHT SIDE OF TERMINAL AT LOCATION 24E7

3. BALLOON ◯ INDICATES ITEM NO. IN B/M OF 123-1J2617 PB250 ASSY.

4. EXACT WIRE LENGTHS TO BE DETERMINED AT MANUFACTURING AND DRAFTING DEPARTMENT NOTIFIED.



WIRE DATA						
WIRE NO.	WIRE GAUGE	COLOR	TERM POINTS FROM TO	ITEM NO.	APPROX LENGTH	REMARKS
1	16 STRD	WHT	23E5L — 20E32	46	13	-12V
2	↕	↕	23E4L — 25D32	↕	10	↕
3	↕		23E3L — 25C32	↕	15	
4	16 STRD		23E2L — 25B32	46	22	
5	24 STRD		23E2R — 28C32	41	46	
6	24 SOLID		29D32 — 28D32 — 28C32, 29C32 — 30C32 — 30D32, 32C32 — 31C32 — 31D32, 32D32 — 33D32 — 33C32, 35D32 — 34D32 — 34C32, 35C32	42	130	
7	24 STRD		35C32 — 23E2L	41	60	
8	16 STRD		23E1L — 25A32	46	26	
9	24 STRD		23E1R — 26C32	41	41	
10	24 SOLID		26D32 — 26C32, 26E32 — 27E32 — 27C32	42	25	
11	24 STRD		23E1R — 27C32	41	50	
12	24 STRD		23E5L — 1J24	41	39	
13	24 SOLID		1J28 — 1J25 — 1J24	42	6	JUMPER
14	24 STRD		16J15 — 23E5R	41	34	
15	24 SOLID		16J15 — 15J15 — 2J15 — 3J15	42	24	
16	24 STRD		23E5R — 7J23	41	40	
17	24 STRD		23E4R — 14J25	41	40	↕
18	24 SOLID		12J47 — 12J44 — 14J25	42	19	-12V
19	↕		1A32 — 1A15	↕	6	-12V JUMPER
20			12A32 — 12A15		↕	↕
21			5B32 — 5B15			
22			9D32 — 9D15			
23			19E32 — 19E15			
24			13E32 — 13E15			
25			14E32 — 14E15			
26			10C32 — 10C15			
27			15C32 — 15C15			
28			20C32 — 20C15			
29	↕	↕	21C32 — 21C15	↕	↕	↕
30	24 SOLID	WHT	39B32 — 39B15	42	6	-12V JUMPER
31	16 STRD	WHT	23E2L — 26B32	46	41	-12V
33	24 SOLID	WHT	2C4 — 2C15	42	4	+6V JUMPER
34	24 SOLID	WHT	34B4 — 34B15	42	4	+6V JUMPER
35	16 STRD	WHT	22E4L — 20E4	46	10	+6V
36	↕	↕	22E4R — 25D4	↕	16	↕
37	↕		22E3L — 25C4	↕	19	
38	16 STRD		22E3R — 25B4	46	25	
39	24 STRD		22E2L — 28C4	41	50	
40	24 SOLID		29C4 — 29D4 — 28D4 — 28C4, 30C4 — 30D4 — 31D4 — 31C4, 33C4 — 33D4 — 32D4 — 32C4, 34C4 — 34D4 — 35D4 — 35C4	42	150	
41	24 STRD		22E2L — 35C4	41	66	
42	16 STRD		22E2R — 25A4	46	30	
43	24 STRD		22E1L — 26C4	41	40	
44	24 SOLID		26E4 — 26D4 — 26C4, 27E4 — 27C4	42	36	
45	24 STRD		22E1L — 27C4	41	45	
46	16 STRD		22E1R — 26B4	46	50	
47	24 STRD		22E4L — 16J14	41	40	
48	24 SOLID		3J14 — 2J14 — 15J14 — 16J14	42	29	
49						
50	24		14J25 — 22E4L	41	48	↕
51	24 STRD		22E2R — 7J21	41	45	+6V
52	24 SOLID		35D18 — 49B18	42	15	GRD JUMPER
53	↕		34D18 — 47B18	42	15	↕
54			33D18 — 44B18	↕	↕	
55			32D18 — 42B18			
56			31D18 — 38B18			
57			30D18 — 35B18			
58			29D18 — 33B18		↕	
59			28D18 — 30B18		15	
60	↕	↕	24E1L — 5J7	↕	30	↕
61	24 SOLID	WHT	2D18 — 2E7 — 3E7	42	10	GRD JUMPER

WIRE DATA						
WIRE NO.	WIRE GAUGE	COLOR	TERM POINTS FROM TO	ITEM NO.	APPROX LENGTH	REMARKS
62	16 STRD	WHT	24E7R — 20E18	46	14	GRD
63	↕	↕	24E4R — 25B18	↕	22	
64	↕		24E3L — 25A18	↕	30	
65	16 STRD		24E2R — 28C18	46	46	
66	24 SOLID		28D18 — 28C18	42	10	
67	16 STRD		24E7L — 29C18	44	50	
68	24 SOLID		29D18 — 29C18	42	10	
69	16 STRD		24E6R — 30C18	44	56	
70	24 SOLID		30D18 — 30C18	42	10	
71	16 STRD		24E5R — 31C18	44	64	
72	24 SOLID		31D18 — 31C18	42	10	
73	16 STRD		24E4L — 32C18	44	58	
74	24 SOLID		32D18 — 32C18	42	10	
75	16 STRD		24E5L — 33C18	44	55	
76	24 SOLID		33D18 — 33C18	42	10	
77	16 STRD		24E2L — 34C18	44	60	
78	24 SOLID		34D18 — 34C18	42	10	
79	16 STRD		24E1R — 35C18	44	60	
80	24 SOLID		35D18 — 35C18	42	10	
81	16 STRD		24E1L — 26B18	44	40	
82	24 SOLID		27C18 — 28B18	42	10	
83	16 STRD		24E6L — 25D18	44	14	
84	24 STRD		24E2L — 16J13	41	34	
85	24 SOLID		5J13 — 2J13 — 15J13 — 16J13	42	32	
86	24 STRD		24E4R — 12J45	41	32	
87	24 SOLID		14J24 — 18J23 — 19J24, 18J27 — 12J44 — 12J45	42	17	
88	24 STRD		24E5L — 11J9	41	30	
89	24 SOLID		5J9 — 3J9 — 10J9 — 11J9	42	15	
90	24 STRD		24E6R — 17J6	41	40	
91	24 SOLID		7J22 — 17J6	42	18	GRD
92	24 SOLID		34B1 — 34B18	42	4	GRD JUMPER
93	16 STRD		24E5R — 25C18	44	18	GRD
94	16 STRD		24E3R — 26C18	44	40	GRD
95	16 STRD		27E18 — 26E18 — 26D18 — 26C18	44	20	GRD
96	16 SOLID		1A18 — 1B18	57 58	8	SEE WIRES
97			2B18 — 2C18		8	46 THRU
98			1C18 — 1D18		8	49 REF
99			8C18 — 8E18		16	
100			16D18 — 16E18		8	GRD
101			1A4 THRU 25A4		18	(+6V) BUS BAR
102			1A18 THRU 25A18			(GRD)
103			1A32 THRU 25A32			(-12V)
104			1B4 THRU 25B4			(+6V)
105			1B18 THRU 25B18			(GRD)
106			1B32 THRU 25B32			(-12V)
107			1C4 THRU 25C4			(+6V)
108			1C18 THRU 25C18			(GRD)
109			1C32 THRU 25C32			(-12V)
110			1D4 THRU 25D4			(+6V)
111			1D18 THRU 25D18			(GRD)
112			1D32 THRU 25D32		18	(-12V)
113			5E4 THRU 20E4		10	(+6V)
114			5E18 THRU 20E18		10	(GRD)
115			5E32 THRU 20E32		10	(-12V)
116			26B4 THRU 49B4		12	(+6V)
117			26B18 THRU 49B18		12	(GRD)
118	16 SOLID		26B32 THRU 49B32	57 58	12	(-12V) BUS BAR
119	24 STRD		23E6R — 4J25	41	35	-48V
120	24 SOLID		7J20 — 4J21 — 4J24 — 4J25	42	8	-48V
121			26C18 — 26C17 — 26C19		1/2	GRD
122			26D18 — 26D17 — 26D19			
123			26E18 — 26E17 — 26E19			
124	24 SOLID	WHT	27E18 — 27E17 — 27E19	42	1/2	GRD

WIRE DATA						
WIRE NO.	WIRE GAUGE	COLOR	TERM POINTS FROM TO	ITEM NO.	APPROX LENGTH	REMARKS
141	16 SOLID	WHITE	23E1R — 26A32	57 58	7	-12V
142	16	↕	26A32 THRU 33A32	57 58	3	-12V
143	24		27A32 — 27A15	42	2	-12V
144	24		29A32 — 29A15	42	2	-12V
145	16		24E7L — 26A18	57 58	7	GRD
146	↕		26A18 THRU 33A18	↕	3	GRD
147	↕	↕	22E4R — 26A4	↕	5	+6V
148	16 SOLID	WHITE	26A4 THRU 33A4	57 58	3	+6V

WIRE DATA						
WIRE NO	WIRE GAUGE	COLOR	TERM POINTS FROM TO	ITEM NO.	APPROX LENGTH	REMARKS
125	24 SOLID	WHT	17A32 — 17A15	42	4	-12V
126	↕	↕	15B32 — 15B15	↕	↕	↕
127			13B32 — 13B15			
128			17C32 — 17C15			
129			22C32 — 22C15			
130			12D32 — 12D15			
131	↕	↕	10D32 — 10D15	↕	↕	↕
132	24 SOLID	WHT	24C32 — 24C15	42	4	-12V

WIRE DATA						
WIRE NO	WIRE GAUGE	COLOR	TERM POINTS FROM TO	ITEM NO	APPROX LENGTH	REMARKS
133	24 SOLID	WHT	06C32 — 6C15	42	4	-12V
134	↕	↕	05D32 — 5D15	↕	↕	↕
135			15E32 — 15E15			
136			02D32 — 02D15			
137			35B18 — 35B13, 35B13 — 35B9, 35B09 — 35B03			
138			07A18 — 07A29, 07A29 — 07A30			
139	↕	↕	20C18 — 20C33	↕	↕	↕
140	24 SOLID	WHT	31B18 — 31B02	42	4	-12

PB250
123-1J2617
PACKARD BELL COMPUTER CORP.
PB250 DC POWER WIRING INSTALLATION DRAWING
369-1J4895 E

Figure 7-15 PB250 DC Power Wiring Installation Drawing

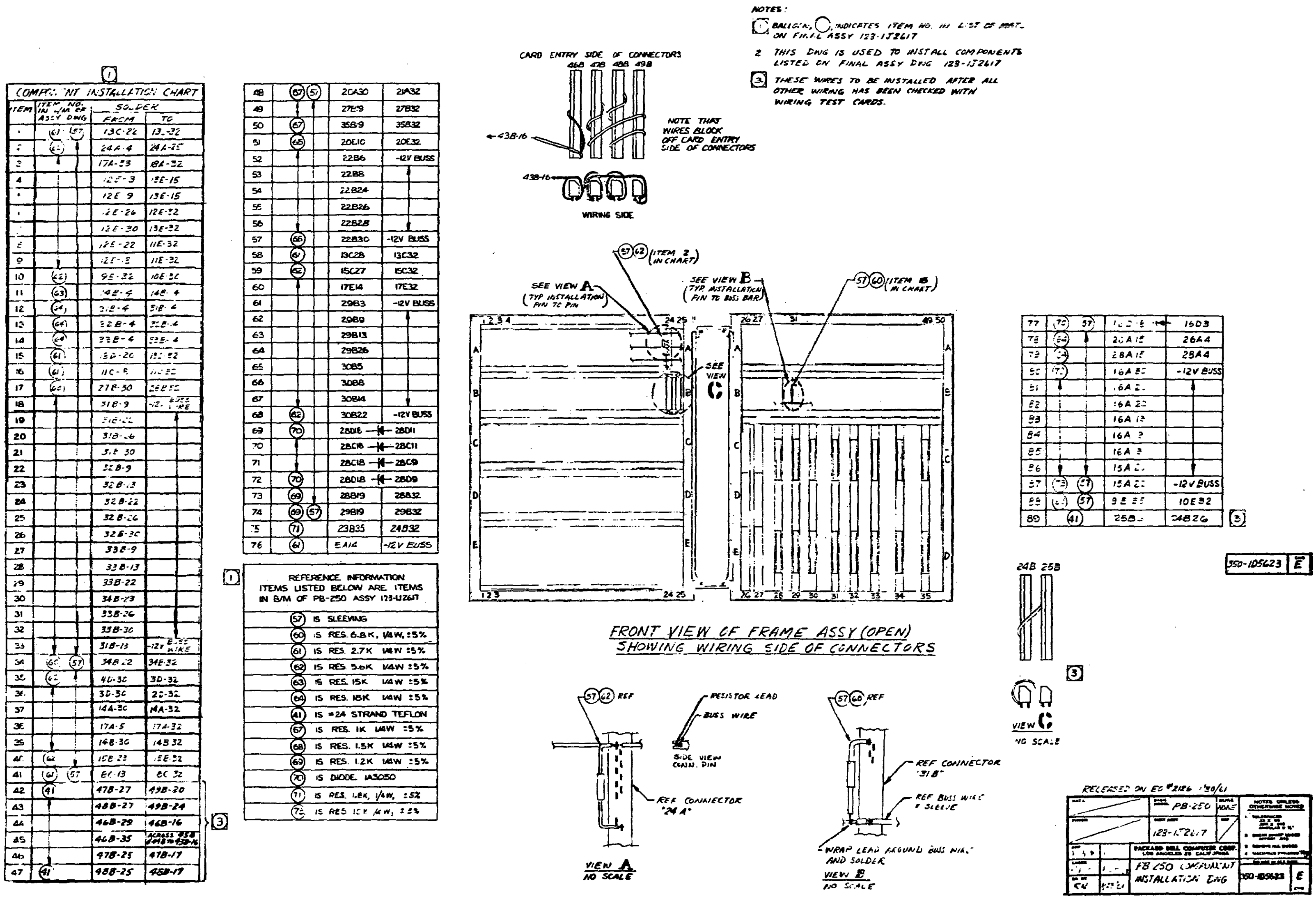


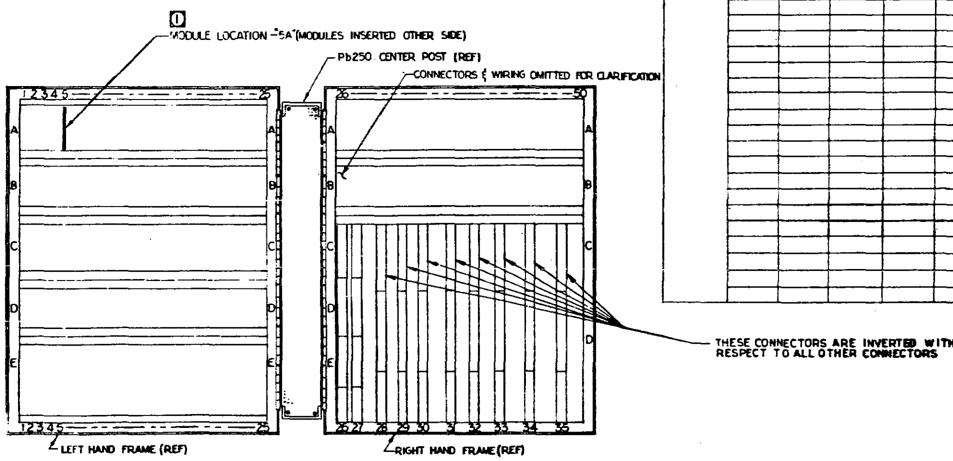
Figure 7-16 PB250 Component Installation Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

(1) LOCATION "5A" AS SHOWN, WOULD BE THE ACTUAL LOCATION OF MODULE TF-100 CONNECTOR IN THE COMPUTER.

MODULE MODEL NO. (CONNECTORS)

NO. →	XCG100	CD100	MSR-2	MSR-1	GD100	EF100	TF100	DG100	DG101	DG102	TD100	FC100	EF101	SA-100
KEYING →	3-13	3-15	3-23	3-27	3-17	3-21	3-25	3-33	3-31	3-29	3-19	3-7	3-5	5-23
LOCATION → IN FRAME ASSEMBLY	25 B	22 B	7 A	28 C	10 A	18 A	2 A	6 A	4 A	1 A	20 C	24 A	19 E	24 B
			2 B	29 C	17 B	19 A	3 A	6 B	11 A	12 A	26 D	25 A	8 E	
			7 D	30 C	27 C	19 B	(1) 5 A	10 B	13 A	17 A	26 E	23 A	9 A	
			14 D	31 C	20 A	23 C	7 B	20 B	14 A	5 B	27 E		23 B	
			22 D	32 C	20 E	25 C	11 B	1 C	15 A	13 B			26 B	
				33 C	[illegible]	25 D	12 B	4 C	16 A	15 B			49 B	
				34 C	[illegible]		21 B	7 C	1 B	30 B			22 A	
				35 C			3 C	9 C	4 B	34 B				
				28 D			5 C	12 C	8 B	39 B				
				29 D			8 C	14 C	9 B	2 C				
				30 D			11 C	16 C	14 B	6 C				
				31 D			13 C	18 C	16 B	10 C				
				32 D			24 D	16 [illegible]	18 B	15 C				
				33 D			19 C	17 [illegible]	27 B	17 C				
				34 D			9 [illegible]	16 E	28 B	21 C				
				35 D			18 [illegible]	5 E	29 B	24 C				
							17 E		31 B	2 D				
							44 B		32 B	5 D				
							6 E		33 B	10 D				
									35 B	12 D				
									36 B	19 D				
									37 B	9 E				
									38 B	13 E				
									40 B	14 E				
									41 B	15 E				
									42 B	22 C				
									1 D	20 C				
									3 D	45 B				
									4 D	27 A				
									6 D	29 A				
									11 D					
									13 D					
									20 D					
									21 D					
									10 E					
									11 E					
									12 E					
									18 E					
									21 A					
									46 B					
									43 B					
									47 B					
									48 B					
									26 A					
									28 A					



FRONT VIEW OF FRAME ASSEMBLIES (OPEN)-PB250 COMPUTER

350-1D4244 H

RELEASED ON E.O. #1513 8-2-60

PB250 | PACKARD BELL COMPUTER CORP. LOS ANGELES 25, CALIFORNIA | PB250 CONNECTOR LOCATION DIAGRAM | 350-1D4244 | H

Figure 7-17 **PB250 Connector Location Diagram**

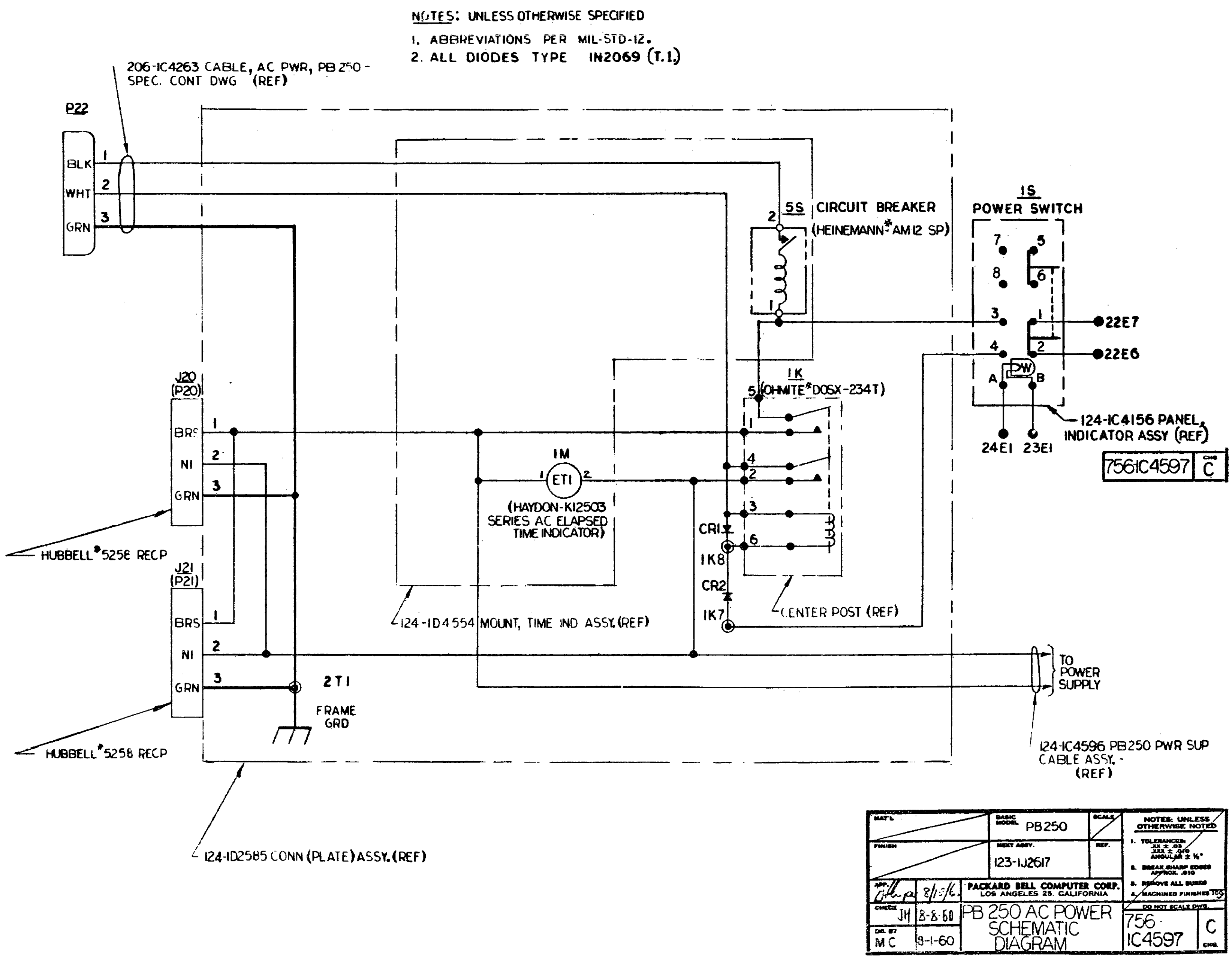


Figure 7-18 **PB250 AC Power Schematic**

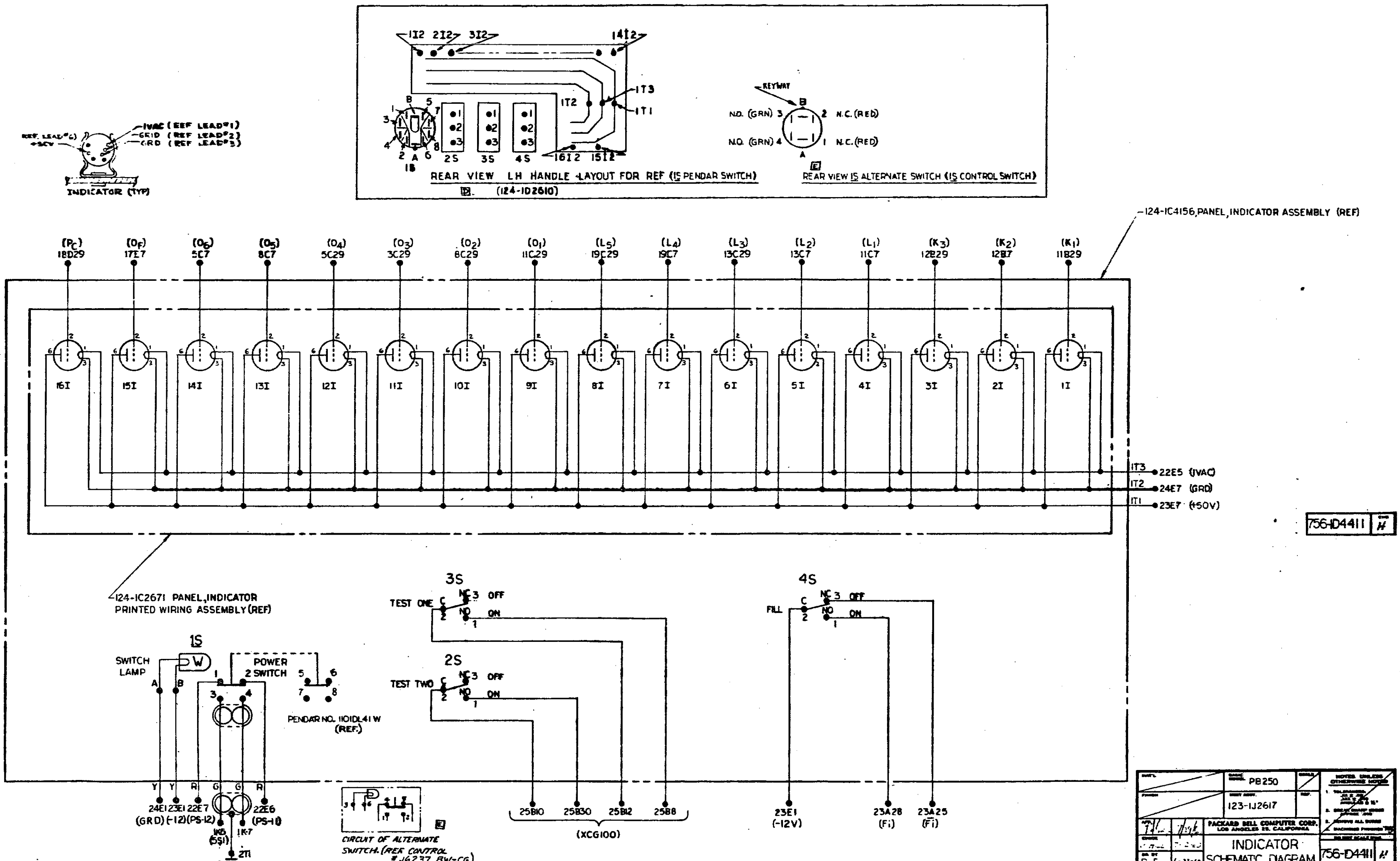


Figure 7-19 Indicators Schematic

RAYTHEON COMPUTER

CUSTOMER SERVICE CHANGE ORDER

C.S.C.O. No. 32

Company Name

Company Address

Serial Numbers Affected All

Previous C.S.C.O. Necessary None

Subject Delay Lines Adjustment

Purpose To standardize delay line adjustment procedure

Change Made By

Date Completed

Test Equipment Required:

Oscilloscope: Tektronix type 535 or 545 or equivalent
Plug in Unit: Tektronix type CA or equivalent
Probes: Tektronix type P6006 (2 each) or equivalent

Procedure:

Perform all adjustments in the order listed, see figure 1 for identification of points referred to.

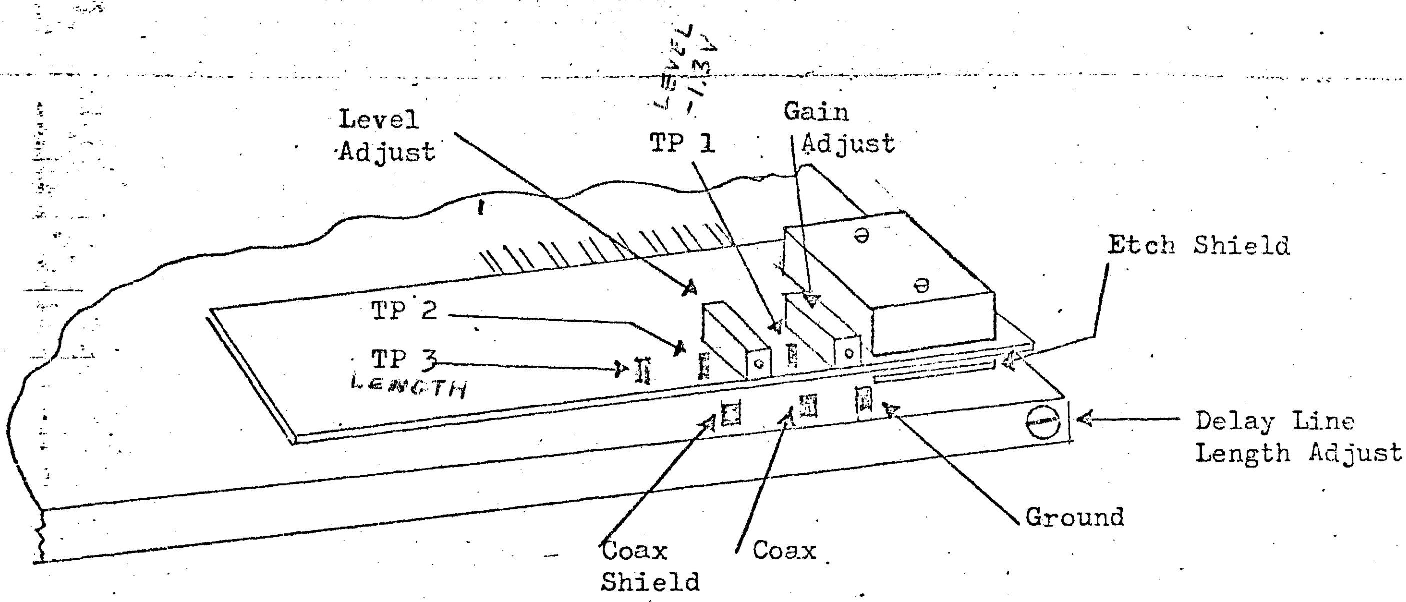


FIGURE 1

A. MSR 1 Length Adjustment

1. Coarse Adjustment:

Scope Setting:	Horiz. Display:	A Time Base
	Time/Cm:	.1 Ms/Cm
	Triggering Mode:	DC
	Trigger Slope:	- Ext.
	Stability:	Preset
	Trigger Input:	Cs (test panel 2E06)
Plug In Setting:	Mode:	A ONLY
	Volts/Cm:	.5 scale
	Channel A Mode:	DC, normal polarity
	Channel A Input:	Tp 3 of memory line

Insert random information into the line by wiping your finger across the coax connection of the line. The wave shape seen should be stable as shown in figure 2.

Note: width of pulses will depend upon information in the line, amount of pulses seen will depend upon sweep length

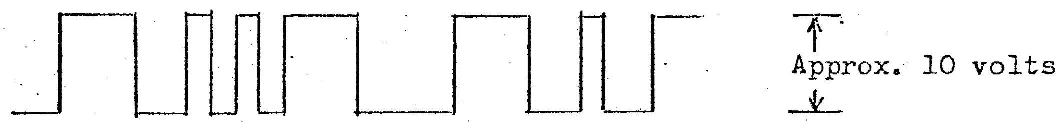


FIGURE 2

If the wave shape drifts adjust the delay line length adjustment until the pulse train is stable. After drifting stops turn the adjusting screw one full turn in the same direction as that which stopped the drifting. Check all MSR 1 delay lines for correct coarse length adjustment.

2. Fine Adjustment:

Scope Setting:	Horiz. Display:	A Time Base
	Time/Cm:	.1 us/Cm, calibrated
	Triggering Mode:	DC
	Trigger Slope:	- Ext.
	Stability:	Preset
	Trigger Input:	P24 (test panel 3E04)
Plug In Setting:	Mode:	Alternate
	Volts/Cm:	.5 scale
	Channel A & B Mode:	DC, normal polarity
	Channel A Input:	Tp 3 of memory line
	Channel B Input:	19E06 (memory clock)

Note: In making the fine length adjustment certain precautions should be taken. If the line is a sealed line manufactured by Ferranti, Deltime or Anderson initially adjust the line to be .3 microseconds shorter than the correct delay. This is done by turning the length adjustment screw in the clockwise direction. The final length adjustment should be made with a counter-clockwise rotation of the adjusting screw.

Adjust length adjustment screw until wave shape is obtained as shown in figure 3.

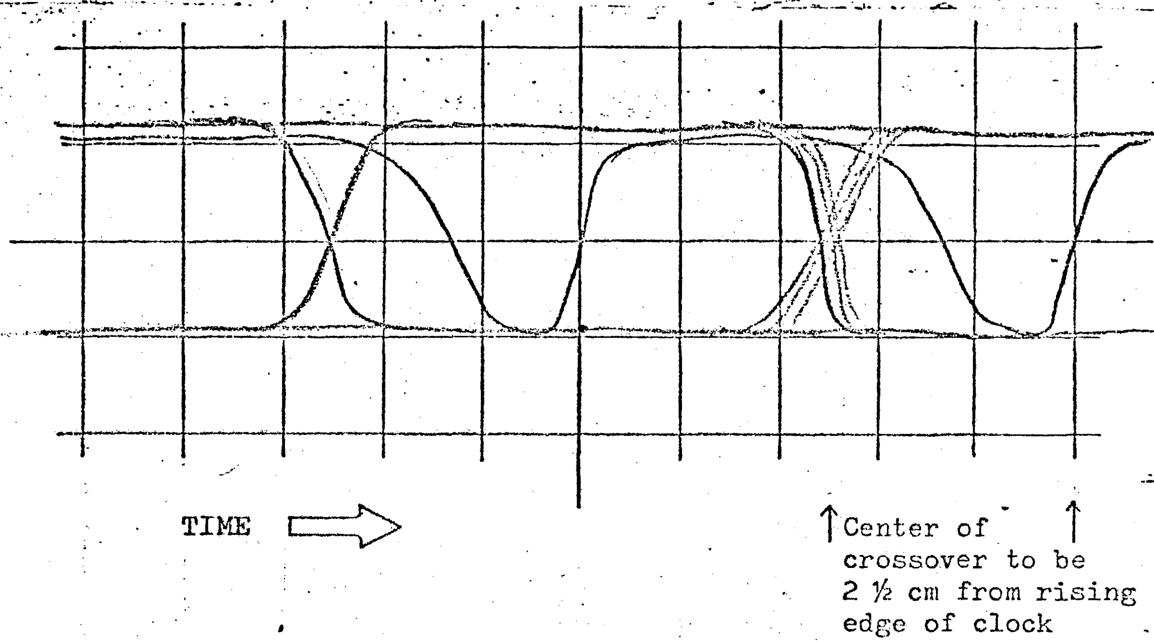


FIGURE 3

3. Dispersion Width Check:

Switch plug in Mode to A ONLY. Examine wave shape for correct width as shown in figure 4.

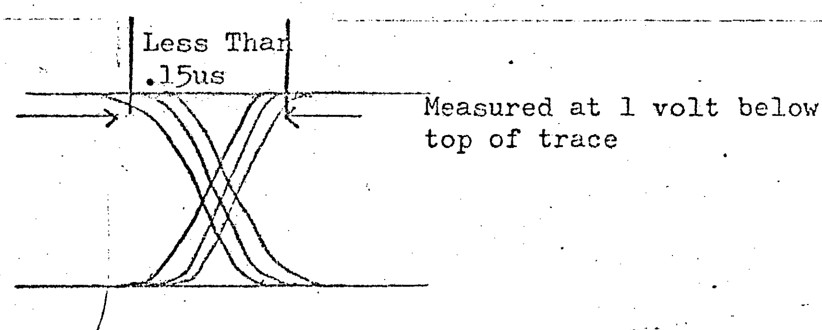


FIGURE 4

If the width of the dispersion is greater than .15 us the line should be removed for repair.

Check all MSR 1 for correct fine delay length adjustment and dispersion width.

B. MSR 1 Level

Scope Setting:	Horiz. Display:	A Time Base
	Time/Cm:	.2 us/Cm
	Triggering Mode:	DC
	Trigger Slope:	- Ext.
	Stability:	Preset
	Trigger Input:	P24 (test panel 3E04)
Plug In Setting:	Mode:	A ONLY
	Volts/Cm:	.1 scale
	Channel A Mode:	AC, normal polarity
	Channel A Input:	Tp 1 of memory line

Turn computer power off and then on to clear all memory memory lines to zero. Change input to plug in from AC to DC. The level should shift to -1.3 volts on DC. If it does not, turn Level Adjust Trimpot to obtain -1.3 volts shift.

Check all MSR 1 for correct level adjustment.

C. MSR 1 Gain

Scope Setting:	Horiz. Display:	A Time Base
	Time/Cm:	.2 us/Cm
	Triggering Mode:	DC
	Trigger Slope:	- Ext.
	Stability:	Preset
	Trigger Input:	P24 (test panel 3E04)
Plug In Setting:	Mode:	A ONLY
	Volts/Cm:	.1 scale
	Channel A Mode:	DC, normal polarity
	Channel A Input:	Tp 1 of memory line

With a jumper lead connect Tp 3 of memory line to P24. Wave shape obtained should be as shown in figure 5.

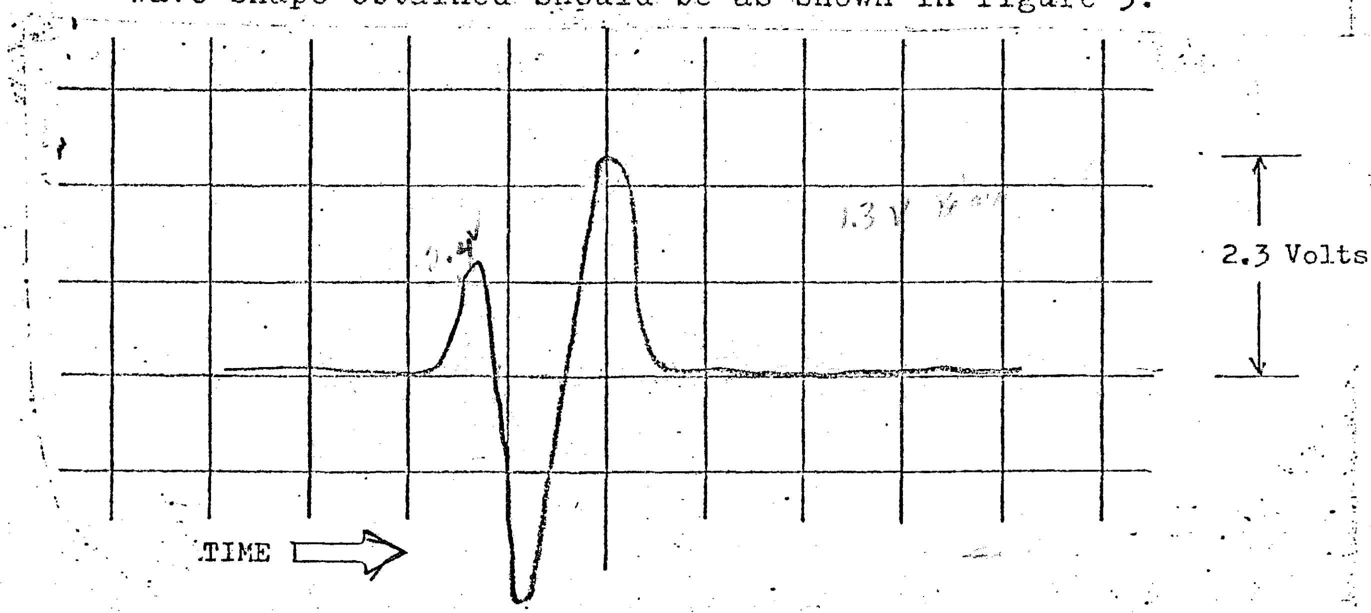


FIGURE 5

Adjust the pulse second in time for +2.3 volts amplitude with the Gain Adjust Trimpot. If +2.3 volts cannot be obtained remove the line for repair.

Check all MSR 1 for correct gain adjustment.

This completes the adjustments of MSR 1.

D. MSR 2 Length Adjustment

1. Coarse Adjustment:

Scope and Plug In Settings: Same as step A-1

This adjustment is only for the modules located at 7D, 14D, 22D and 2B. The module located at 7A will be adjusted later.

Insert random information into the line by touching a screwdriver to the coax connection of the line. The wave shape seen should be stable as shown in figure 2.

If the wave shape drifts adjust the delay line length adjustment until the pulse train is stable. After drifting stops turn the adjusting screw one full turn in the same direction as that which stopped the drifting. Check all MSR 2 delay lines for correct coarse length adjustment.

2. Fine Length Adjustment:

Scope and Plug In Settings: Same as step A-2

Note: In making the fine length adjustment certain precautions should be taken. If the line is a sealed line manufactured by Ferranti, Deltime or Anderson initially adjust the line to be .3 microseconds shorter than the correct delay. This is done by turning the length adjustment screw in a counter-clockwise direction. the final adjustment should be made with clockwise rotation of the adjusting screw

Adjust length adjustment until waveshape is obtained as shown in figure 6.

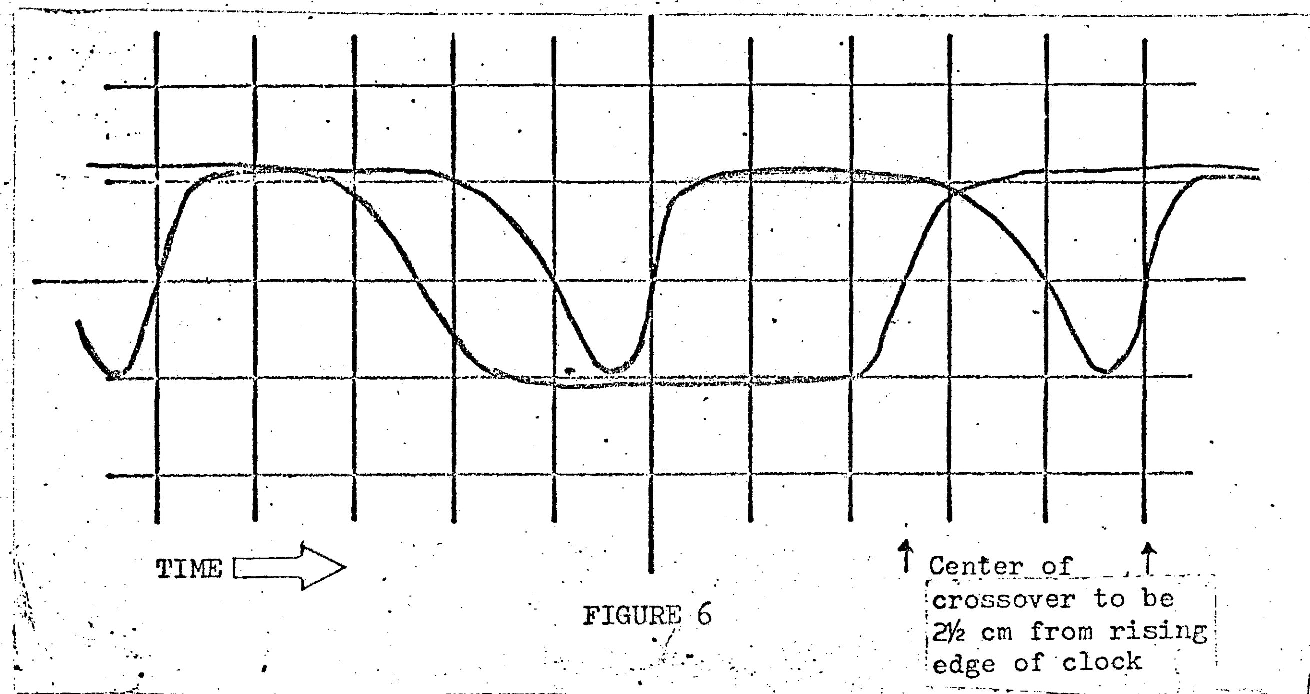


FIGURE 6

E. MSR 2 Level

Scope and Plug In Settings: Same as step B

Adjustment procedure is the same as step B.

F. MSR 2 Gain

Scope and Plug In Settings: Same as step C

Adjustment procedure is the same as step C.

G. Module 7A Adjustment:

Exchange the modules located at 2B and 7A. Perform adjustment steps D, E and F on the module now located at 2B. When completed with step F restore the modules 7A and 2B to their original positions.

This completes adjustment of all delay lines.

H. Helpful Hints

When making the gain adjustment sometimes it is very difficult to insert P24 into the line. This is not an indication of a bad line. It may help to insert a small capacitor in series with the P24 lead or to wet your finger and touch it to Tp 3 at the same time that you touch P24 to Tp 3. If the wave shape obtained is correct but very faint this is all right. It just means that you did not insert P24's into every word of the memory line.

If the adjustment of the line appears correct but the line still fails intermittently check that the two mounting studs on the etch shield have been filed to remove the anodizing and are making good contact with the etch.

Also insure that C.S.C.O. #39 has been installed if necessary.