MX-1 MEMORY EXTENSION
Technical Manual

PBC 1011

Packard Bell Computer

A SUBSIDIARY OF PACKARD BELL ELECTRONICS
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September 15, 1961

NOTICE

CONTENTS

FIGURES

TABLES

DESCRIPTION AND LEADING PARTICULARS

A. GENERAL

Model MX-1 (Figure 1-1) is a memory extension chassis manufactured by Packard Bell Computer, Los Angeles, California, for the addition of memory lines to the PB250 Computer. An MX-1 can contain any number up to 24 magnetostrictive delay lines of 256 words each representing a memory addition of up to 6144 words. It is possible to add a second memory extension to this configuration. The second memory extension chassis, which has identical wiring to the MX-1 but contains a maximum of 23 magnetostrictive delay lines of 256 words each, is designated MX-2. Addition of an MX-1 and an MX-2 connected to the PB250 will provide a maximum computer memory of 15,888 words.

B. PHYSICAL DESCRIPTION

Designed for rack mounting, the MX-1 connects directly to the computer and permits adding or removing plug-in memory modules as desired. The entire unit slides out of the rack mount and opens like a book to provide easy accessibility to components and wiring. Included in the MX-1 and MX-2 are solid-state circuits required for selection of one of the delay lines during the read or write operation. The MX-2 connects directly to the MX-1. Applicable leading particulars for both memory extension units are provided in Table 1-1.

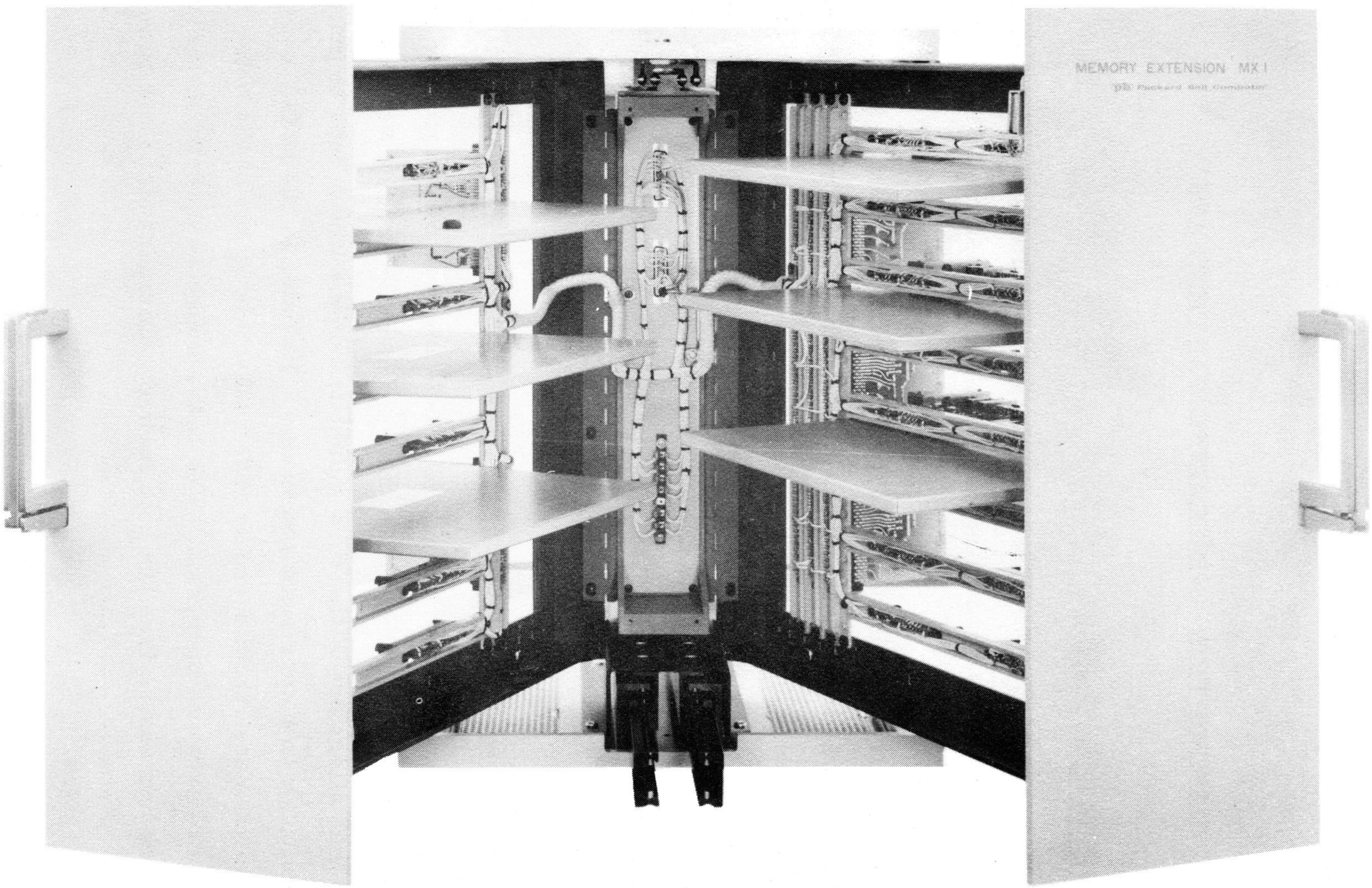


Figure 1-1. MX-1 **Memory Extension**

Table 1-1

LEADING PARTICULARS

Capacity	Model MX-1 has 24 delay lines Model MX-2 has 23 delay lines Two memory extension units with up to 47 delay lines, can be connected to the PB250
Control	Information into and out of the memory extension unit is controlled entirely by the PB250 to which it is linked
Input/Output	Data transferred into and out of the memory extension units from the PB250, at a rate of 2Mc.
Power Requirements	Supplied by the PB250
Dimensions	Rack mounted. Requires 22-3/4 inches of panel height in a standard 19-inch rack.
Weight	150 pounds
Location	Immediately beneath or above PB250 if mounted in the same rack, or in adjacent rack without separating walls. There is a 7 ft interconnecting cable between the PB250 and the MX-1 and a 7 ft interconnecting cable between the MX-1 and the MX-2.

II. PRINCIPLES OF OPERATION

Delay lines in the MX-1 and MX-2 are used for data in the same way as any lines 0 through 15 in the PB250. The logic functions used are as follows:

M2g, M3g,---N0g, N1g,---N7g for addressing

Information signal Ig and gate signal Wg to write into a line.

The "fetch" gate information Fg to read out from a line.

The addressing terms and information and gate signals are formed in the PB250. The write logic is similar to that used in the computer.

Example: For line 23

$$sM23w = M2g\ N7g\ Wg\ Ig + M2g\ N7g\ Wg\ M23r$$

$$rM23w = M2g\ N7g\ Wg\ \overline{Ig} + M2g\ N7g\ Wg\ \overline{M23r}$$

Fg is generated in the applicable memory extension unit as follows:

For the MX-1

$$Fg = \text{--} + M2g\ N0g\ M16r + M2g\ M1g\ M17r + \text{--}$$
$$+ \text{--} + M3g\ N6g\ M30r + M4g\ N0g\ M32r + \text{--}$$
$$+ M4g\ N7g\ M39r + M6g\ N6g\ M55r$$

For the MX-2

$$Fg = \text{--} + M5g\ N0g\ M40r + M5g\ N1g\ M41r + \text{--}$$
$$+ M6g\ N6g\ M54r + M7g\ N0g\ M56r + \text{--}$$
$$+ M7g\ N7g\ M63r.$$

Line number 31 is allocated to the index register and therefore cannot be used in the MX-1. The corresponding line number in the MX-2 would be 55. Because both MX-1 and MX-2 are similarly wired, a line number 31 left out in the MX-1 means that there will be no line number 55 in the MX-2. To correct this, the wiring provides for a line number 55 in the MX-1. Cabling to the MX-2 is such that the corresponding "fetch" gate is grounded in that unit.

To summarize: There are up to 24 memory lines in the MX-1. These are $20)_8$ to $47)_8$, and $67)_8$.

There are up to 23 memory lines in the MX-2. These are $50)_8$ to $66)_8$, and $70)_8$ to $77)_8$. Memory line locations are given in Table 2-1.

Table 2-1. (Sheet 1 of 2)

MEMORY LINE LOCATIONS

MX-1			MX-2		
Location	Octal Line No.	Decimal Line No.	Location	Octal Line No.	Decimal Line No.
4E	20	16	4E	50	40
5E	21	17	5E	51	41
6E	22	18	6E	52	42
7E	23	19	7E	53	43
8E	24	20	8E	54	44
9E	25	21	9E	55	45
10E	26	22	10E	56	46
11E	27	23	11E	57	47
4M	30	24	4M	60	48
4L	31	25	4L	61	49
5M	32	26	5M	62	50
5L	33	27	5L	63	51
6M	34	28	6M	64	52

Table 2-1. (Sheet 2 of 2)

MEMORY LINE LOCATIONS

MX-1			MX-2		
Location	Octal Line No.	Decimal Line No.	Location	Octal Line No.	Decimal Line No.
6L	35	29	6L	65	53
7M	36	30	7M	66	54
7L	40	32	7L	70	56
8M	41	33	8M	71	57
8L	42	34	8L	72	58
9M	43	35	9M	73	59
9L	44	36	9L	74	60
10M	45	37	10M	75	61
10L	46	38	10L	76	62
11M	47	39	11M	77	63
11L	67	55	11L		

III. OPERATION

A. GENERAL

An interconnecting cable is plugged into connector J7 (Figure 3-1) on the PB250 and connector 1MJ on the MX-1. An MX-2 unit can be plugged into connector 2MJ on the back of the MX-1. Connector pins for the MX-2 connection are wired in parallel with those of the MX-1 connection, except that M5g is connected in place of M2g, M6g in place of M3g, and M7g in place of M4g.

The SA100 sinewave amplifier module in the PB250 is a tuned class C amplifier used for synchronization of a PB250 Computer with its peripheral equipment.

The SA100 accepts the two megacycle sinewave generated by the oscillator section of an XCG-100 module, amplifies and distributes it to the MX-1. Output of the SA100 is processed in the MX-1 by the shaper section of the XCG-100 module to produce computer and memory clock signals. The distribution of the SA100 output allows synchronization of the clock signals within 0.01 microsecond between the PB250 and the MX-1.

The Ig, Fg, and Wg signals are also carried by coaxial cables between the PB250 and the MX-1. To eliminate delays in extra amplifier stages, $\overline{\text{Ig}}$ and $\overline{\text{Wg}}$ (rather than Ig and Wg) are sent to the MX-1.

All connections are made with Microdot 95-3920 coaxial cable (Z_o = 95 ohms, capacitance per foot = 13 $\mu\mu$f).

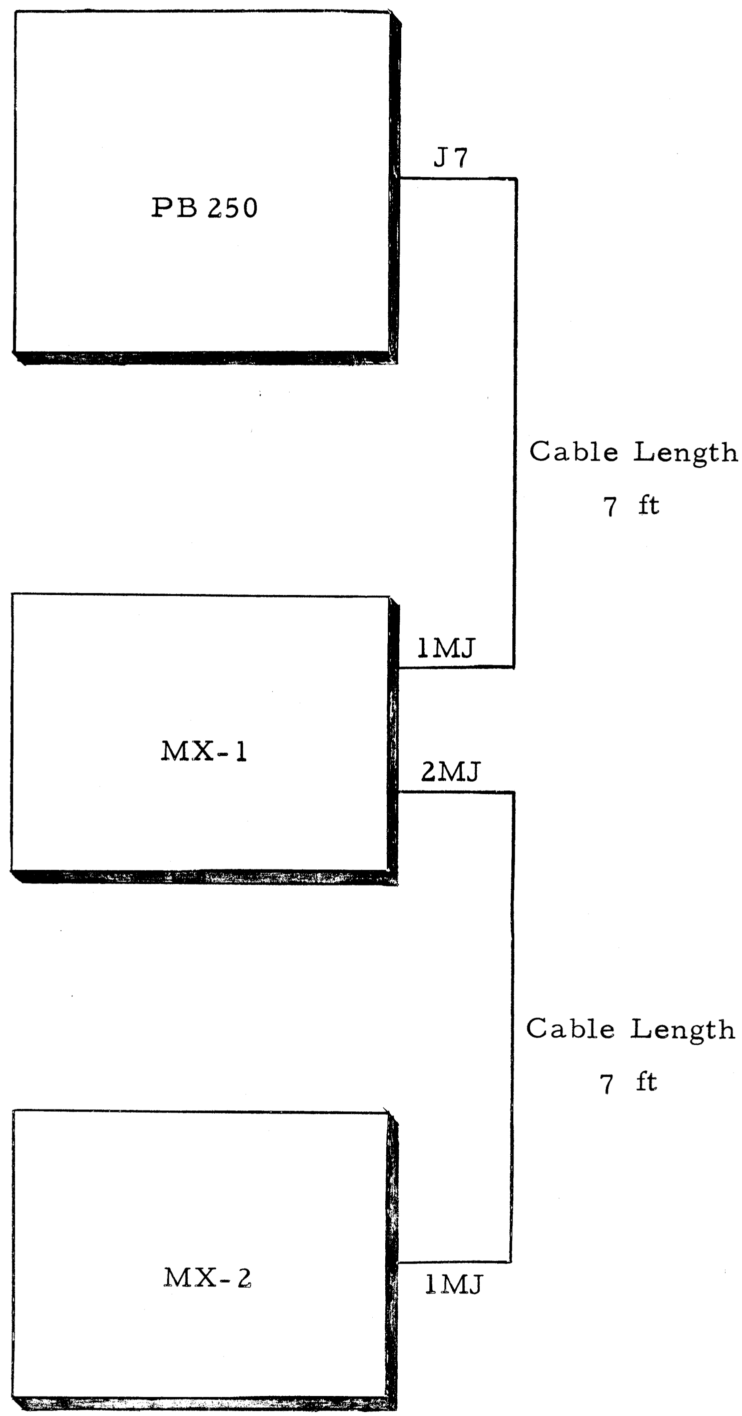


Figure 3-1. Interconnection Diagram

B. OPERATING INSTRUCTIONS

Memory line number $20)_8$ is also used in the event of multiple computer coupling. In this instance, Line $20)_8$ in the MX-1 cannot be used and the corresponding "fetch" gate M2g N0g M16r must be grounded to prevent a reading of all 1's in Fg if line $20)_8$ is selected. Necessary grounding is accomplished by a jumper plug in 2MJ of the MX-1. However, if line $20)_8$ is used in the MX-1 and there is no multiple computer coupling, "fetch" gate M2g N0g <u>M8r</u> in the PB250 must be grounded. Necessary grounding is accomplished by a jumper plug in connector 5J on the PB250 which forms part of the MX-1 system.

If no line numbers beyond 31 are used, the "fetch" gate for line numbers 31 through 38 and 55, should be grounded. This is accomplished by a jumper plug in 2MJ of the MX-1 grounding M4g and M6g. Grounding requirements are detailed in Table 3-1.

Table 3-1.

GROUNDING REQUIREMENTS

Coupling	Jumper
Multiple computer coupling; no line numbers used beyond line 31 in MX-1.	Jumper plug on MX-1 to ground (M16r M2g N0g), M4g and M6g
Multiple computer coupling; line numbers used beyond line 31 in MX-1 and/or MX-2.	Jumper plug on MX-1 to ground (M16r M2g N0g)
No computer coupling; no line numbers used beyond line 31 in MX-1.	Jumper plug on PB250 to ground <u>M8r</u>, jumper plug on MX-1 to ground M4g and M6g
No computer coupling; line numbers used beyond line 31 in MX-1 and/or MX-2	Jumper plug on PB250 to ground <u>M8r</u>

C. MODULES

The MX-1 requires the following module cards to be inserted in the PB250: card number 40, row B, DG-101; card number 26, row B, EF-101; card number 27, row C, GD-100. For line numbers in excess of 31, the following module cards are added to the PB250: card number 25, row D, EF-100; card number 24, row D, TF-100. A module location chart is provided in Table 3-2. Applicable module card schematics are provided in Section IV.

Table 3-2.

MODULE LOCATION CHART

CD-100	DG-101	DG-102	EF-101	GD-100	XCG-100
3J	1D	1J	3H	1H	2H
	3D		2J		
	1K				
	2K				
	3K				

IV. CHECKOUT

A. GENERAL

The quality and derating of all components used in the MX-1 provide for a trouble-free unit, with a required minimum of maintenance.

B. CHECKOUT PROCEDURE

1. Make a visual check of all component parts and wires and replace each damaged or broken part or wire.

2. Load Random Write-Read Program IIA (Table 4-1) into the PB250 Computer. Any group of successive lines can be tested up to and including line $36)_8$. Note that because line $37)_8$ is the index register it cannot be selected by the program and as a result it is not possible to check groups of successive line numbers including $37)_8$.

For example: To check lines $30)_8$ to $50)_8$ it would be necessary to select and check lines $30)_8$ to $36)_8$ first and then check lines $40)_8$ to $50)_8$.

Table 4-1. (Sheet 1 of 14)

RANDOM WRITE-READ IIA DIAGNOSTIC ROUTINE

Purpose:	To test the read-write circuitry of the PB250 under operator control. To test operation of the PB250 under various marginal conditions.
Restrictions:	Line 06 must be in the machine if error punch-out is to be performed. If an error occurs due to parity, the machine will halt. Clearing parity will resume testing and punch-out. No sequence of lines that includes line 37 may be tested. Such a sequence must be divided into two shorter sequences, the first ending with line 36 and the second beginning with line 40.
Space:	All sectors of line 01 are used by the program and its bootstrap. In addition, all fast-line channels are used for temporary storage.
Timing:	Approximately 3.0 seconds to write and read one line (optimized).
Loading	The program has its own bootstrap which may be loaded by the FILL switch on the computer console. After the bootstrap is loaded, the

	remainder of the tape may be read in by pressing the ENABLE and BREAK POINT switches, striking the I Key, and raising the ENABLE switch. When loading is completed, the light on the Flexowriter will come on and the computer will loop, waiting for a keyboard entry.
Input	After the bootstrap is loaded, insert the following sequence: K FF LL ±nnnnnnn (C/R) where: K is a control letter. FF is the first line to be tested. LL is the last line to be tested. ±nnnnnnn is a signed, seven octal digit number used by the program as the first random number. If K = C, the program will write-read continuously. K = O, the program will write-read once and return control to the keyboard.

	K = R, the program will read continuously. For example, if the operator wishes to test all command lines continuously, the following input sequence might be used: C 02 07 +1234567 (C/R) A space must separate the control letter, the first line, the last line, and the random number. A carriage return will start the computation. If an erroneous configuration is typed, the ENABLE and BREAK POINT switches should be pressed, the I Key struck and the ENABLE switch raised. This will reset the control and the correct sequence may be typed. When using the R mode, the memory must first be filled with random numbers using the O mode. Then the R mode is inserted using the same first random number.
Output	If an error is found, the program will punch the following: SSSLL ±bbbbbbb ±wwwwwww

Table 4-1. (Sheet 4 of 14)

RANDOM WRITE-READ IIA DIAGNOSTIC ROUTINE

	where: SSSLLL = the sector and line where error occurred. ±bbbbbbb = a signed, seven octal digit number which should have been found in this location. ±wwwwwww = a signed, seven octal digit number which was found in this location. In the event that the error involved included a parity error, the machine will halt when this number is picked up for punch-out. Punch-out may be resumed by clearing parity with the ENABLE and BREAK POINT switches. If, at any time, five consecutive sectors are found to be bad, it is assumed that the entire line is bad and no further punch-out for that line will occur. Anything less than five consecutive erroneous sectors will cause normal punch-out; i.e., each sector where an error occurred will be punched out.
Method:	The program generates a series of random numbers beginning with the initial number

RANDOM WRITE-READ IIA DIAGNOSTIC ROUTINE

	inserted. Each generated number is written into a different sector of the line. After writing, the program again generates the same series of numbers and compares against those previously written. If the numbers do not compare, an error occurs. Since the random numbers are generated by multiplication, an initial number of zero will cause the program to clear the specified memory area and compare for zero. If no initial number is typed, it will automatically be zero.

First line No in 1,0
Last " " " 2,0

Table 4-1 (Sheet 6 of 14)

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
000	024S4300;	CLB	Initially 007SLDC01;
001	-7740000	CONST	EBP mask & sector increment
002	013S2100;	LSD	8
003	006 5501;	LAI	New character → A
004	017 3601;	TBN	Transfer if word complete
005	001S4001;	EBP	To fill sign of A
006	+0000377	CONST	LAI mask
007	+0007332	CONST	Line count
010	011S0701;	LDP	Put marker in B
011	+0000077	CONST	
012	002S5200;	RPT	
013	014 5200;	RPT	Reject last character
014	013 7736;	TES	
015	012 7736;	TES	Wait for next character
016	014S5700;	CIB	
017	000 3401;	TCN	Transfer if line complete
020	$\boxed{025}$ 1101;	STA	Store word away
021	020 0501;	LDA	Increment store address
022	001 1501;	SUB	
023	020 1101;	STA	
024	010S3701;	TRU	Return for next word
025	232 0401;	LDC	Set exit for first space
026	046 1001;	STC	
027	032S4500;	CLA	
030	271 5501;	LAI	Read in new character
031	037S5601;	CAM	Compare for "C"
032	027S5100;	RTK	
033	034 5100;	RTK	Reject last character
034	033 7736;	TES	
035	032 7736;	TES	Wait for next character

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
036	034S5700;	CIB	
037	000 00541	CONST	"C" code
040	056 7501;	TOF	Transfer if C
041	243 5601;	CAM	Transfer if 0
042	056 7501;	TOF	
043	263 5601;	CAM	Transfer if R
044	056 7501;	TOF	
045	370 5601;	CAM	Transfer if space
046	060 7501;	TOF	
047	360 5601;	CAM	Transfer if C/R
050	101 7501;	TOF	
051	000 0200;	IBC	
052	056 2210;	RST	Assemble character in B
053	000 0100;	IAC	
054	100 2210;	RST	
055	032S4500;	CLA	Return to read next character
056	000 1100;	STA	Store control character and
057	026S4300;	CLB	return to read sequence
060	376 0401;	LDC	First space; set exit for
061	046 1001;	STC	second space
062	026S4300;	CLB	Return to read sequence
063	325 0501;	LDA	Second space, set exit
064	046 1101;	STA	for third space
065	377 0401;	LDC	Initialize first line store
066	070S3701;	TRU	
067	355 0401;	LDC	Initialize last line store
070	000 4500;	CLA	
071	077 1001;	STC	
072	114 2110;	LST	
073	017 1100;	STA	Rearrange Lo

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
074	000 4500;	CLA	
075	104 2110;	LST	
076	017 1400;	ADD	
077	$\boxed{002}$ 1100;	STA	Store address in fast line
100	026S4300;	CLB	Return to read sequence
101	011 1200;	STB	R. N. $\rightarrow K_o$, K_i
102	012 1200;	STB	
103	000 4400;	CLC	Set first time mode
104	013 1000;	STC	(Read phase in C)
105	000 0500;	LDA	
106	263 5601;	CAM	Control: R
107	130 7501;	TOF	
110	127 3401;	TCN	What phase?
111	113 2100;	LSD	Was read, set write
112	145 1001;	STC	
113	012 0500;	LDA	$K_o \rightarrow K_i$
114	011 1100;	STA	
115	000 0500;	LDA	
116	243 5601;	CAM	Control: 0
117	122 7501;	TOF	
120	002 0500;	LDA	First line $\rightarrow$ Index
121	133S1137;	STA	
122	013 0500;	LDA	First time?
123	000 3501;	TAN	Yes. Return to start
124	277 1401;	ADD	
125	013 1100;	STA	No. Reset first time flag
126	120S3701;	TRU	
127	131 2200;	RSI	Was write, set read
130	145 1001;	STC	
131	011 0500;	LDA	$K_o \rightarrow K_i$

Table 4-1 (Sheet 9 of 14)

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
132	012 1100;	LDA	
133	120S3701;	TRU	
134	140 3401;	TCN	What phase?
135	152 0501;	LDA	
136	143 1100;	STA	Read prestore CAM
137	143S3701;	TRU	
140	141S0501;	LDA	
141	200 1100!	STA	Write prestore STA
142	143 1100;	STA	
143	151S7100;	MCL	
144	225S0400;	LDC	
145	000 0000;	CONST	Store error test in fast line
146	242 7501;	TOF	
147	242 3401;	TCN	
150	356S3701;	TRU	
151	324S3701;	TRU	→ Clear Ce
152	200 5600!	CAM	
153	154S0401;	LDC	
154	046 2233!	CONST	Generate K_{i+1}
155	205S3200;	MUP	
156	157S1101;	STA	Save N_r
157	000 0000;	CONST	
160	003 0500;	LDA	
161	162S1501;	SUB	
162	000 5100;	CONST	Pick up Nw
163	164 1101;	STA	
164	000 0000;	LDA	
165	013 1101;	STA	
166	003 0600;	LDB	
167	000 4500;	CLA	

Table 4-1. (Sheet 10 of 14)

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
170	202 2110;	LST	
171	000 0100;	IAC	
172	174 0637;	LDB	Pick up SSSLL
173	214 2110;	LST	
174	000 0100;	IAC	
175	210 2210;	RST	
176	014 1200;	STB	
177	376 0706;	LDP	Save 37606 and 37706
200	016 1300;	STD	
201	000 4500;	CLA	Clear space counter
202	015 1100;	STA	
203	206S0601;	LDB	Punch limit = 5
204	000 6116;	WOC	C/R
205	212S1200;	STB	Store K_{i+1}
206	000 0001;	CONST	
207	254 1201;	STB	
210	211S0401;	LDC	
211	000 6020;	WOC	Prestore space punch
212	214S3701;	TRU	
213	223S3700;	TRU	⟶ Fast line
214	273 1001;	STC	
215	014 0600;	LDB	
216	000 4500;	CLA	Pick up next digit
217	223 2110;	LST	
220	014 1200;	STB	
221	000 4300;	CLB	
222	000 4400;	CLC	
223	224 0000;	MAC	
224	001 5601;	CAM	Assemble in A
225	000 4100;	GTB	

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
226	000 0100;	IAC	
227	372 3401;	TCN	
230	370S1401;	ADD	
231	232S4500;	CLA	
232	060 7501;	TOF	Clear Ce
233	234S1101;	STA	
234	000 0000;	CONST	
235	243S0500;	LDA	Pick up CAM/STA
236	376 1106;	STA	
237	240S0501;	LDA	
240	253S3701;	TRU	Punch assembled digit
241	247S3701;	TRU	
242	243S0500;	LDA	
243	000 0041;	CONST	Punch limit
244	245S1401;	ADD	
245	001 0000;	CONST	Increment sector
246	263S1100;	STA	
247	377 1106;	STA	
250	251S0401;	LDC	
251	000 1400;	CONST	→ Punch
252	376S3706;	TRU	
253	254S0501;	LDA	
254	000 0000;	CONST	
255	256S1501;	SUB	Word done?
256	000 00001	CONST	
257	262 3501;	TAN	
260	254 1101;	STA	No. Return for next digit
261	215S3701;	TRU	
262	273S0701;	LDP	Yes
263	000 00021	CONST	R code

Table 4-1. (Sheet 12 of 14)

PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
264	266 7501;	TOF	Last sector?
265	152S0600;	LDB	No. Return for $K_i + 1$
266	267S0437;	LDC	Yes. Pick up index
267	000 2000;	CONST	
270	271S4201;	AMC	
271	000 00571	CONST	
272	276S0300;	ROT	
273	000 6000;	WOC	Punch space or C/R
274	307S3701;	TRU	
275	376 1306;	STD	
276	267 0401;	LDC	
277	376S3706;	TRU	
300	301S5600;	CAM	Last line?
301	000 2000;	CONST	
302	306 7501;	TOF	
303	304S1401;	ADD	No. Increment index
304	000 0040;	CONST	
305	323S1137;	STA	
306	325S0400;	LDC	Pick up phase constant
307	273 0501;	LDA	Punching complete?
310	204 5601;	CAM	
311	350 7501;	TOF	
312	243 0601;	LDB	No. Punch limit = 8
313	254 1201;	STB	
314	015 0500;	LDA	Space counter negative?
315	344 3501;	TAN	
316	277 1401;	ADD	No. Make negative
317	015 1100;	STA	
320	157 0501;	LDA	Pick up N_r
321	014 1100;	STA	

Table 4-1. (Sheet 13 of 14)

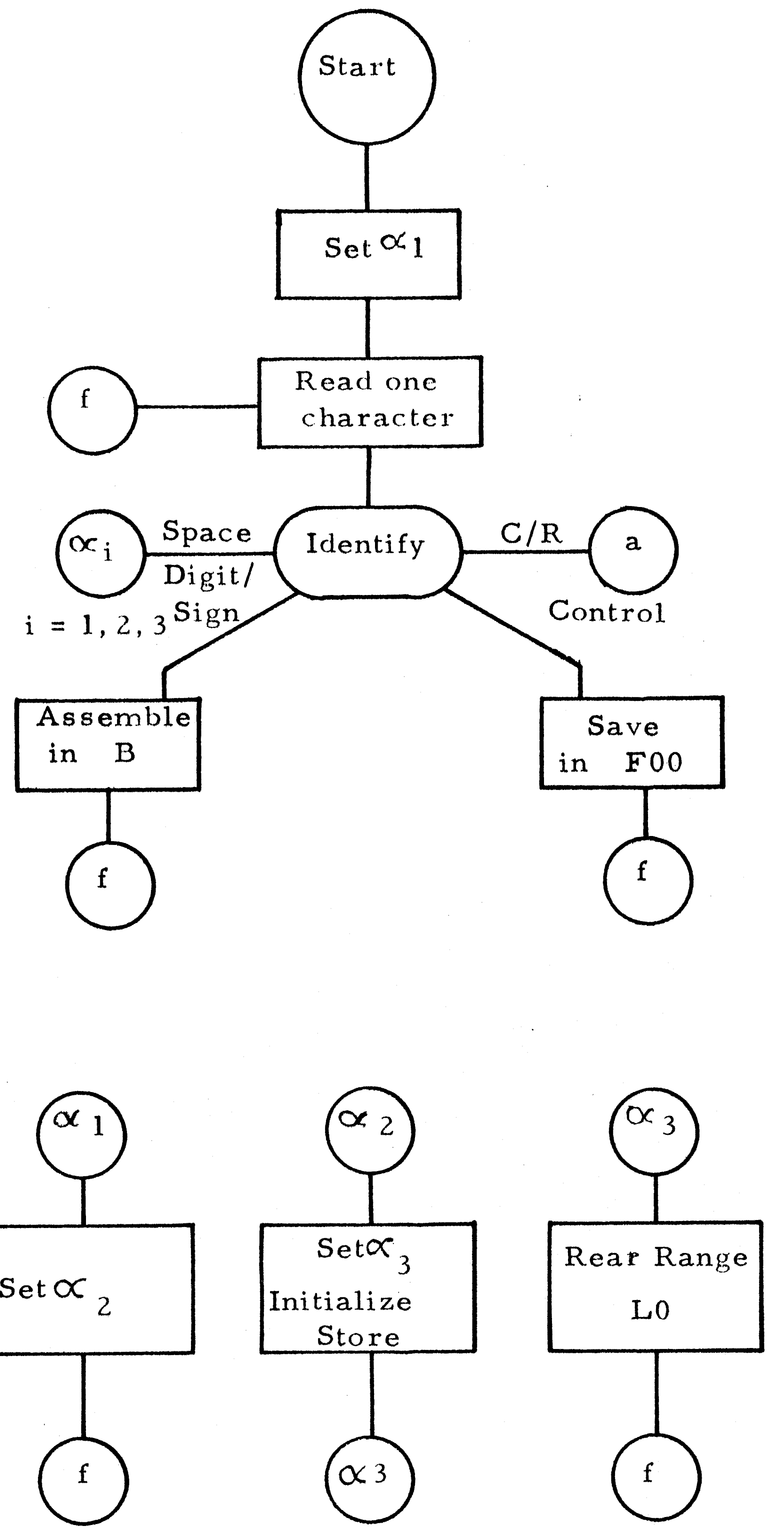
PROGRAM LISTING

LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
322	332 3501;	TAN	
323	327S0701;	LDP	
324	352S4500;	CLA	
325	066 7501;	TOF	
326	105S3701;	TRU	
327	000 6036;	WOC	
330	340S3701;	TRU	Punch sign
331	335S3701;	TRU	
332	333S0701;	LDP	
333	000 6037;	WOC	
334	340S3701;	TRU	
335	376 1306;	STD	
336	301 0401;	LDC	
337	376S3706;	TRU	
340	014 0600;	LDB	
341	343 2110;	LST	Pick up digit
342	014 1200;	STB	
343	216S3701;	TRU	
344	204 0501;	LDA	Yes. Prestore C/R punch
345	273 1101;	STA	
346	013 0501;	LDA	Pick up Nw
347	321S3701;	TRU	
350	016 0700;	LDP	Restore 37606 and 37706
351	376 1306;	STD	
352	242S3701;	TRU	Return
353	234 1101;	STA	Clear Ce
354	152S0600;	LDB	Return to generate K_{i+1}
355	001 1100;	STA	Last line store
356	234 0401;	LDC	Pick up Ce
357	360S0100;	IAC	

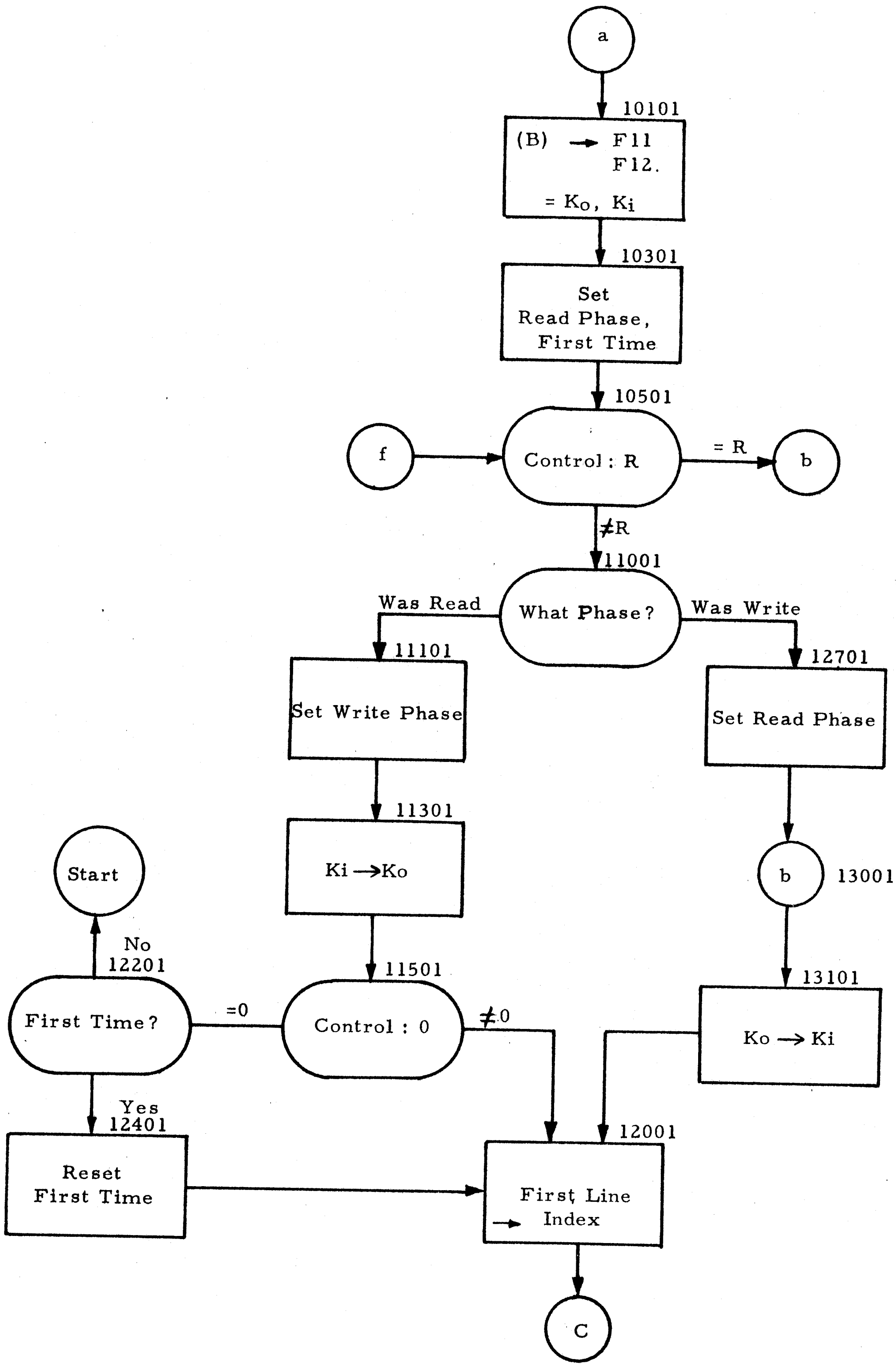
Table 4-1. (Sheet 14 of 14)

PROGRAM LISTING

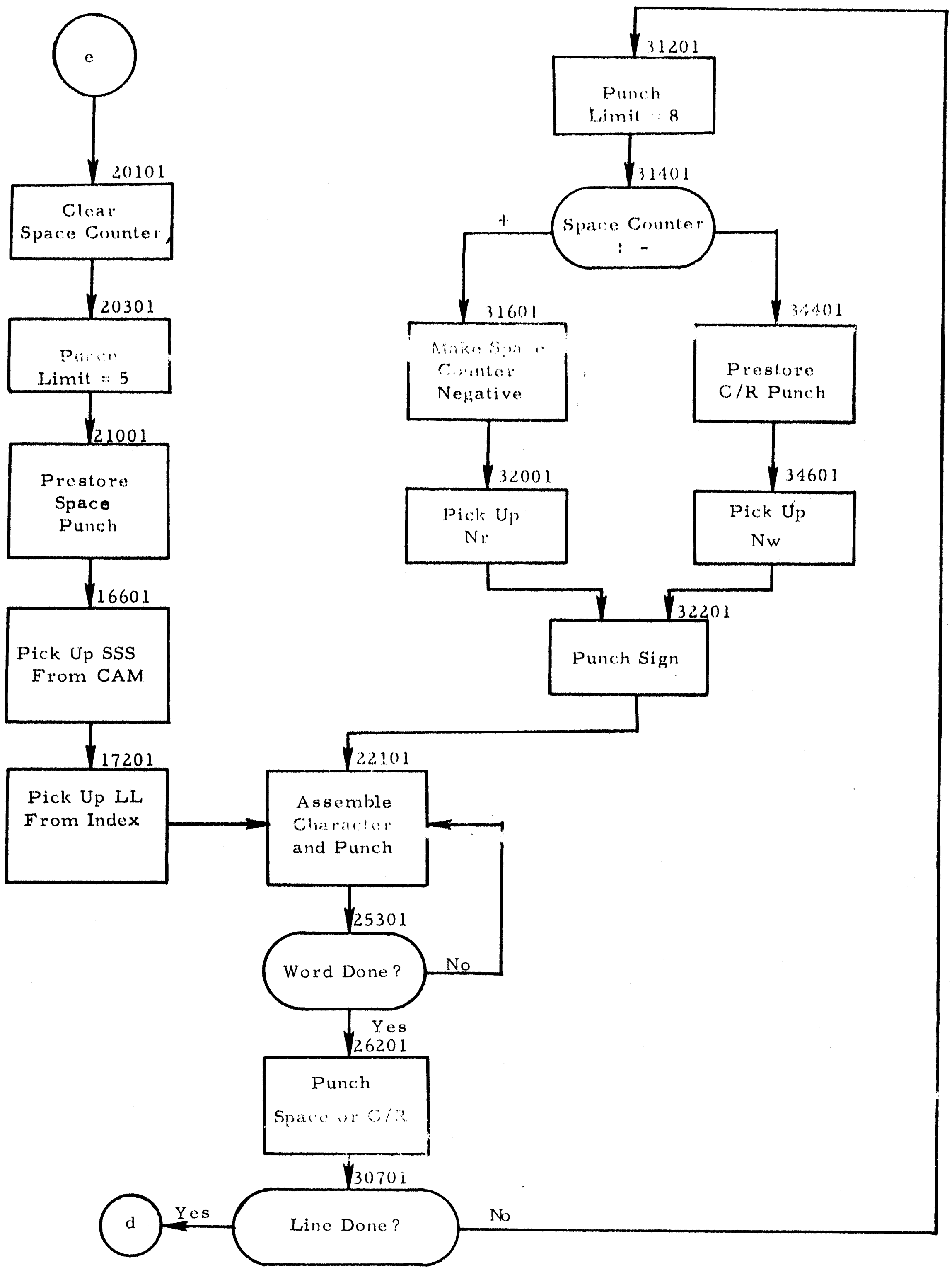
LOCATION	INSTRUCTION	SYMBOLIC OP CODE	REMARKS
360	000 0053;	CONST	C/R code
361	362S5601;	CAM	
362	000 00011	CONST	= 5 ?
363	242 7501;	TOF	
364	365S1401;	ADD	
365	000 00001	CONST	No. Increment Ce
366	234 1101;	STA	
367	155S0100;	IAC	——▶Punch out
370	000 0004;	CONST	
371	230 7501;	TOF	
372	375 2110;	LST	Assemble digit for punch out
373	374S1401;	ADD	
374	000 6000;	WOC	
375	236S3701;	TRU	
376	063 7501;	TOF	Second space exit
377	002 1100;	STA	First line store



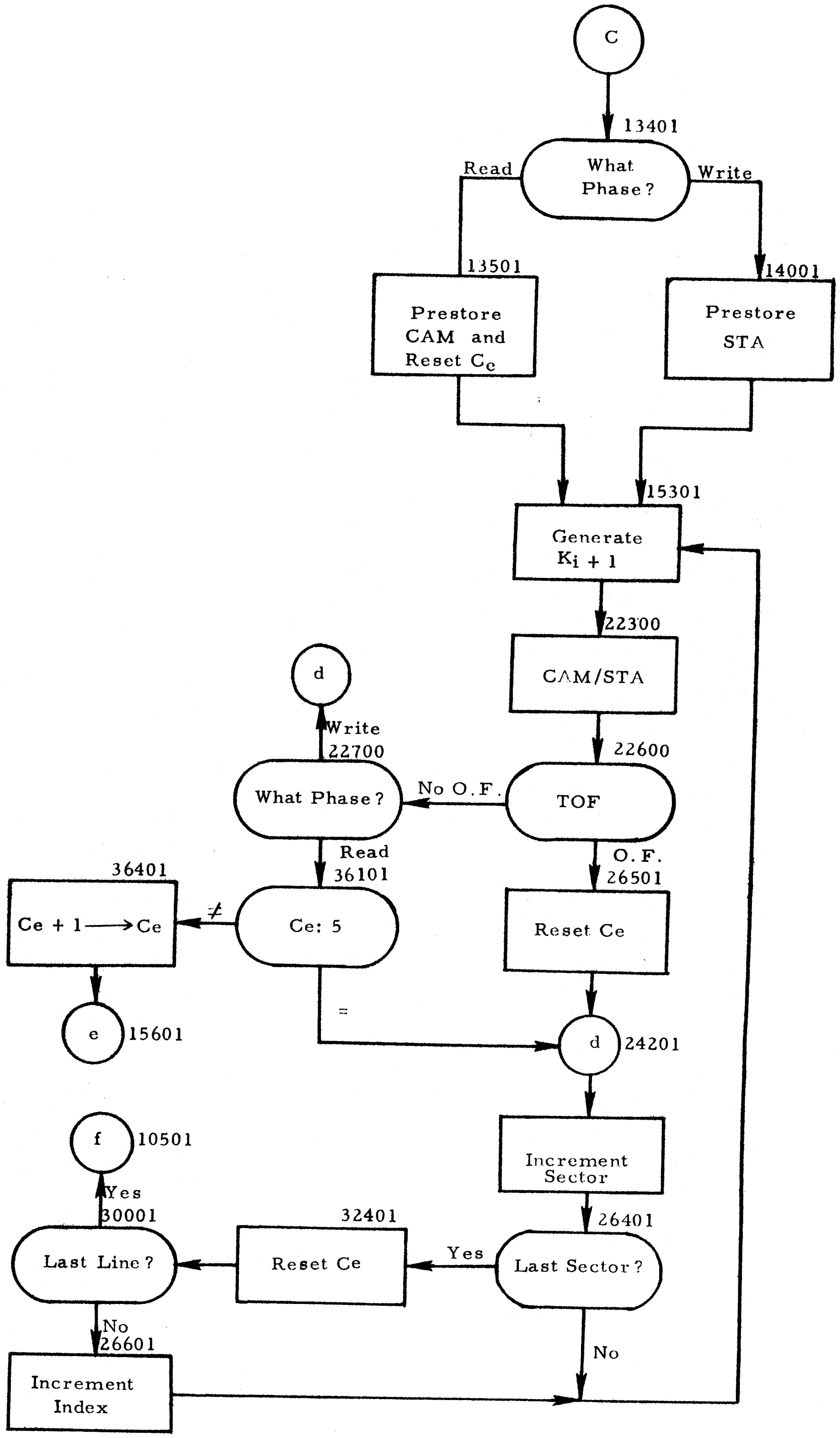
Random Write-Read IIA Flow Diagram (Sheet 1 of 4)



Random Write Read IIA Flow Diagram (Sheet 2 of 4)



Random Write-Read IIA Flow Diagram (Sheet 3 of 4)



Random Write-Read IIA Flow Diagram (Sheet 4 of 4)

FIRST	LAST	DELETED
C1	C8	
CR1		
Q1	Q8	
R1	R29	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS $\pm 5\%$, 1/4 W.
2. ALL CAPACITORS ARE IN UUF.
3. ALL TRANSISTORS ARE 2N1500.
4. CR1 TO BE PER PBCC DWG NO. 358-1A3050.

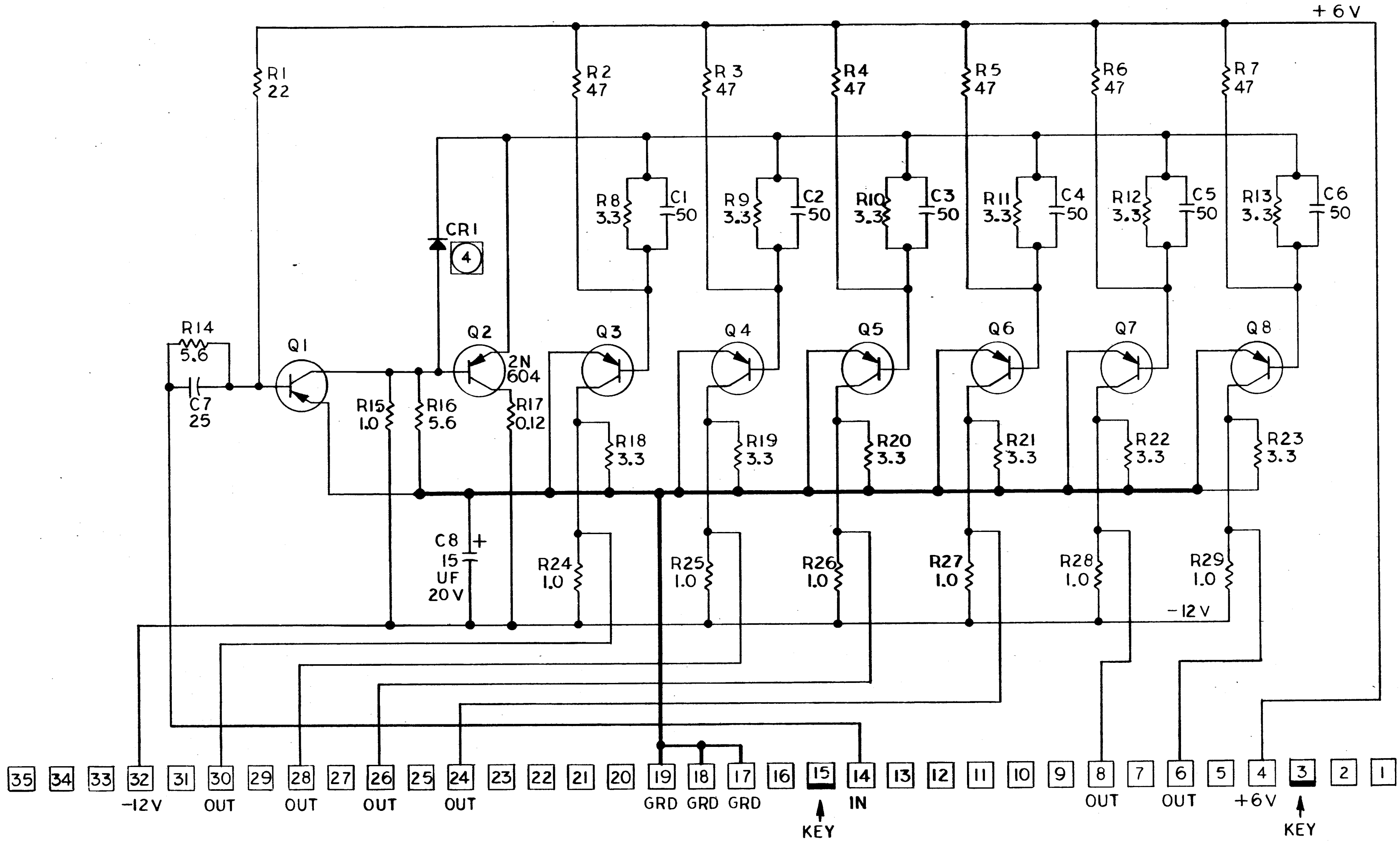


Figure 4-1. CD-100 Module (Schematic)

FIRST	LAST	DELETED
R1	R13	
C1	C1	
CR1	CR25	CR6
Q1	Q2	

NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4 W.
2 ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3 WHEN PARALLELING EMITTER FOLLOWERS, THE CONNECTION BETWEEN CONTACT TERMINAL 16 & 17 IS OMITTED.

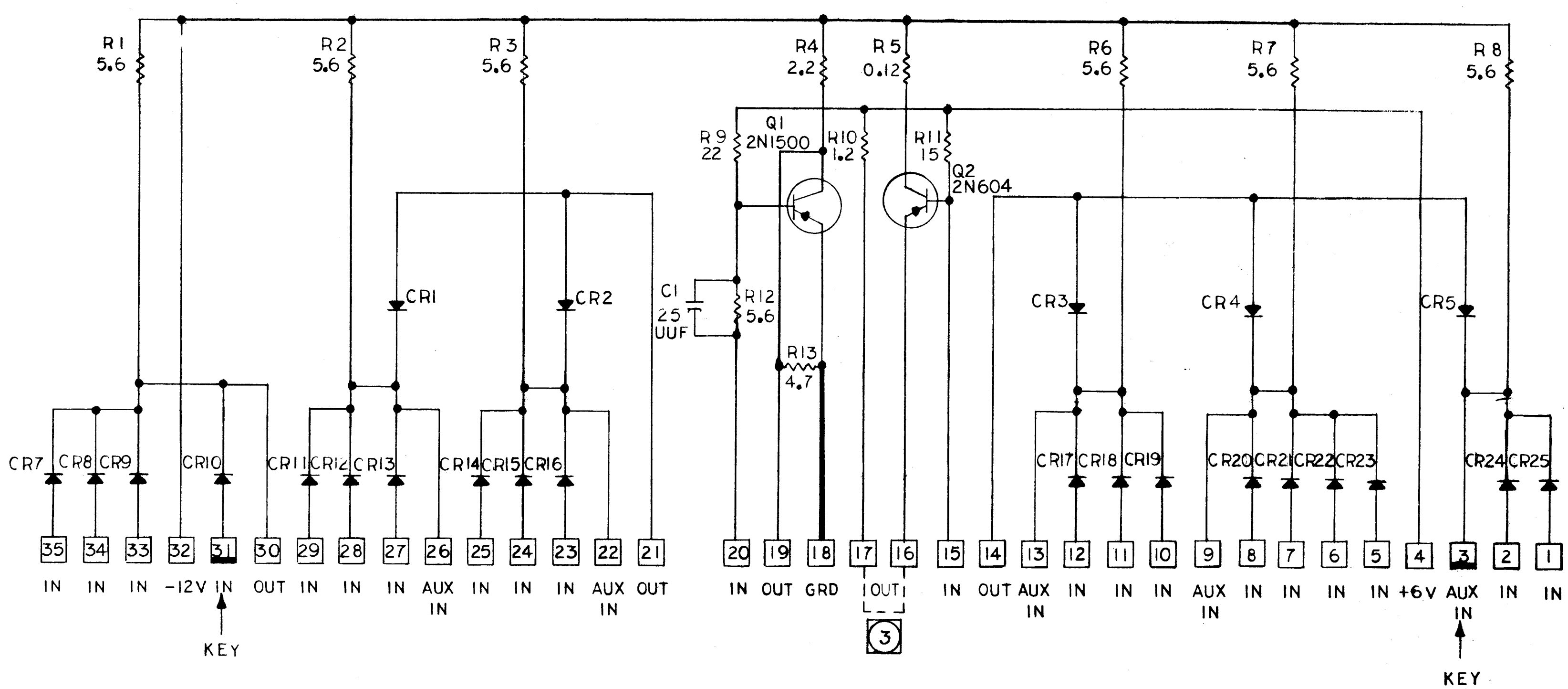


Figure 4-2. DG-101 Diode Gate (Schematic)

FIRST	LAST	DELETED
C1	C2	
CR1	CR19	
R1	R6	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4W
2. ALL DIODES TO BE PER P.B.C.C DWG NO. 358-1A3050.

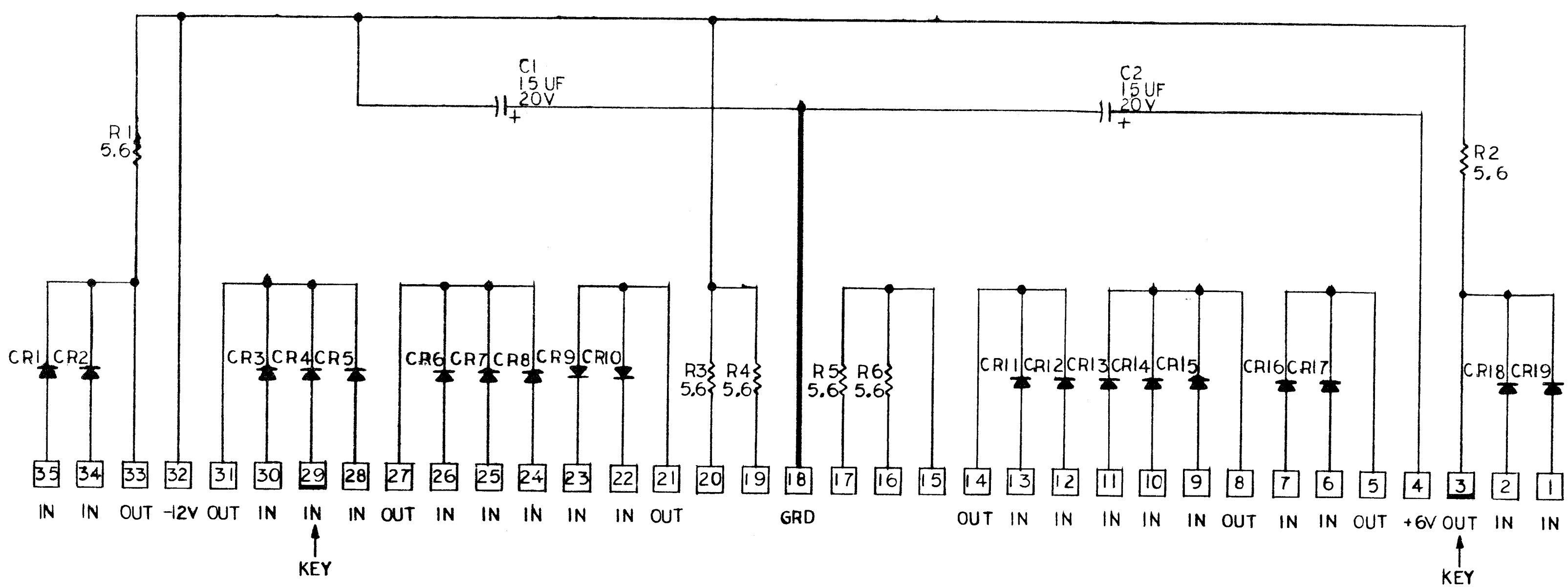


Figure 4-3. DG-102 Diode Gate (Schematic)

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE PER PBCC DWG. NO. 358-1A3050
2. ALL RESISISTOR VALUES ARE IN KIL OHMS ±5% 1/4W
3. ALL TRANSISTORS ARE 2N604

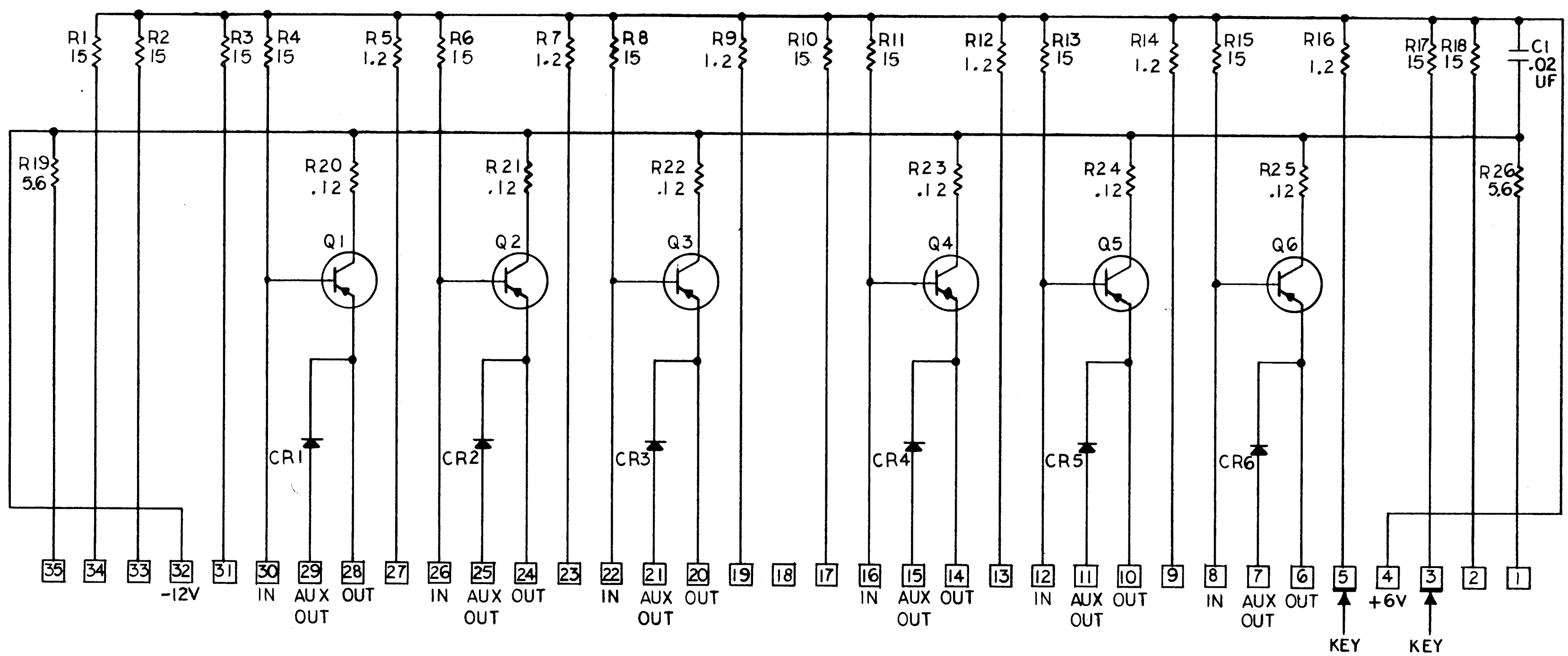


Figure 4-4. EF-101 Module (Schematic)

FIRST	LAST	DELETED
Q1	Q8	
R1	R32	
C1	C9	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES IN KILOHMS $\pm 5\%, \frac{1}{4}$W.
2. ALL CAPACITOR VALUES IN UUF.
3. ALL TRANSISTORS 2N1500.

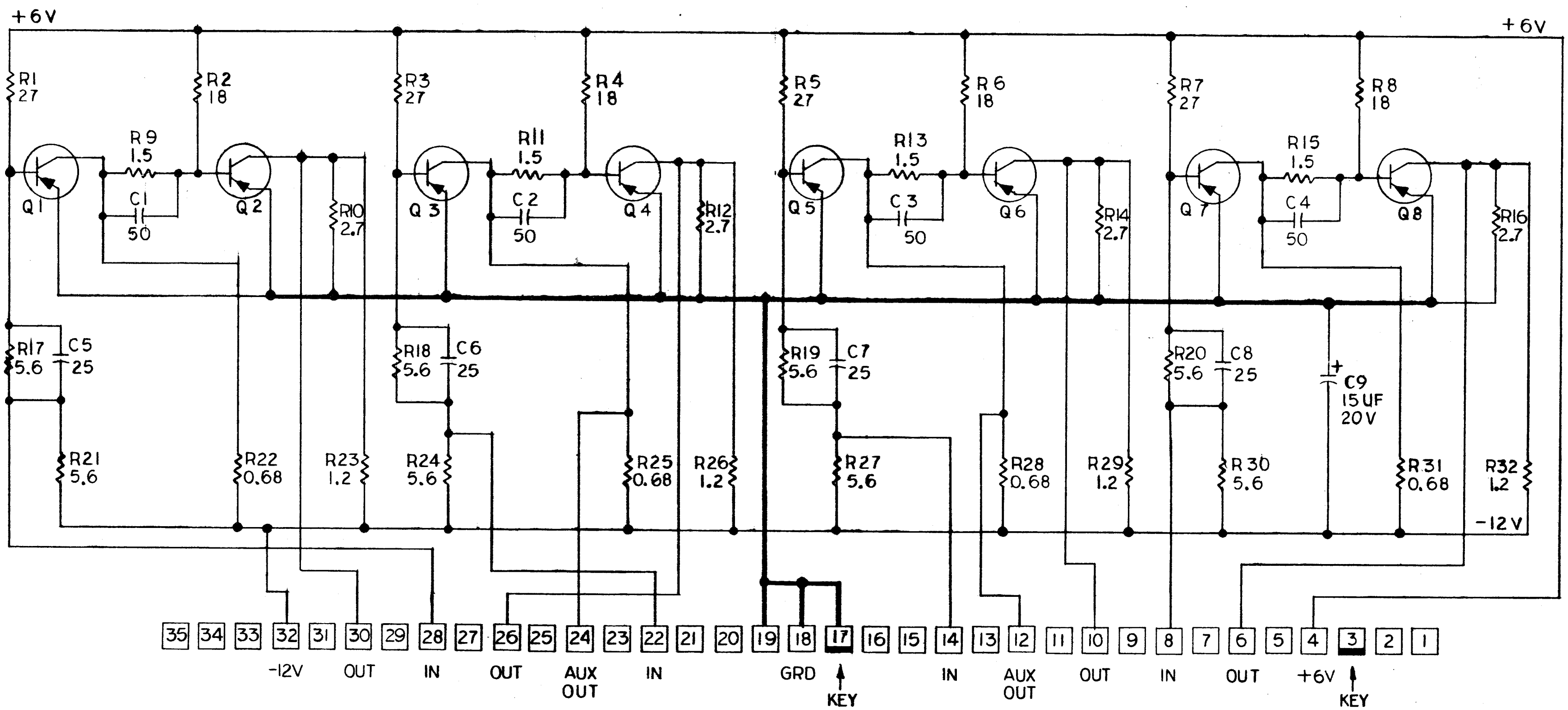


Figure 4-5. GD-100 Module (Schematic)

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL DIODES ARE 358-1A3050
2. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, ¼ WATT.
3. R1, R2, C1, C2 & C3 VALUES SPECIFIED BY DELAY LINE VENDOR.
4. ALL CAPACITOR VALUES IN UUF.
5. ALL TRANSISTORS ARE 2N1500.

FIRST	LAST	DELETED
C1	C26	
CR1	CR28	
R1	R74	R22, R32
Q1	Q12	
DL1		

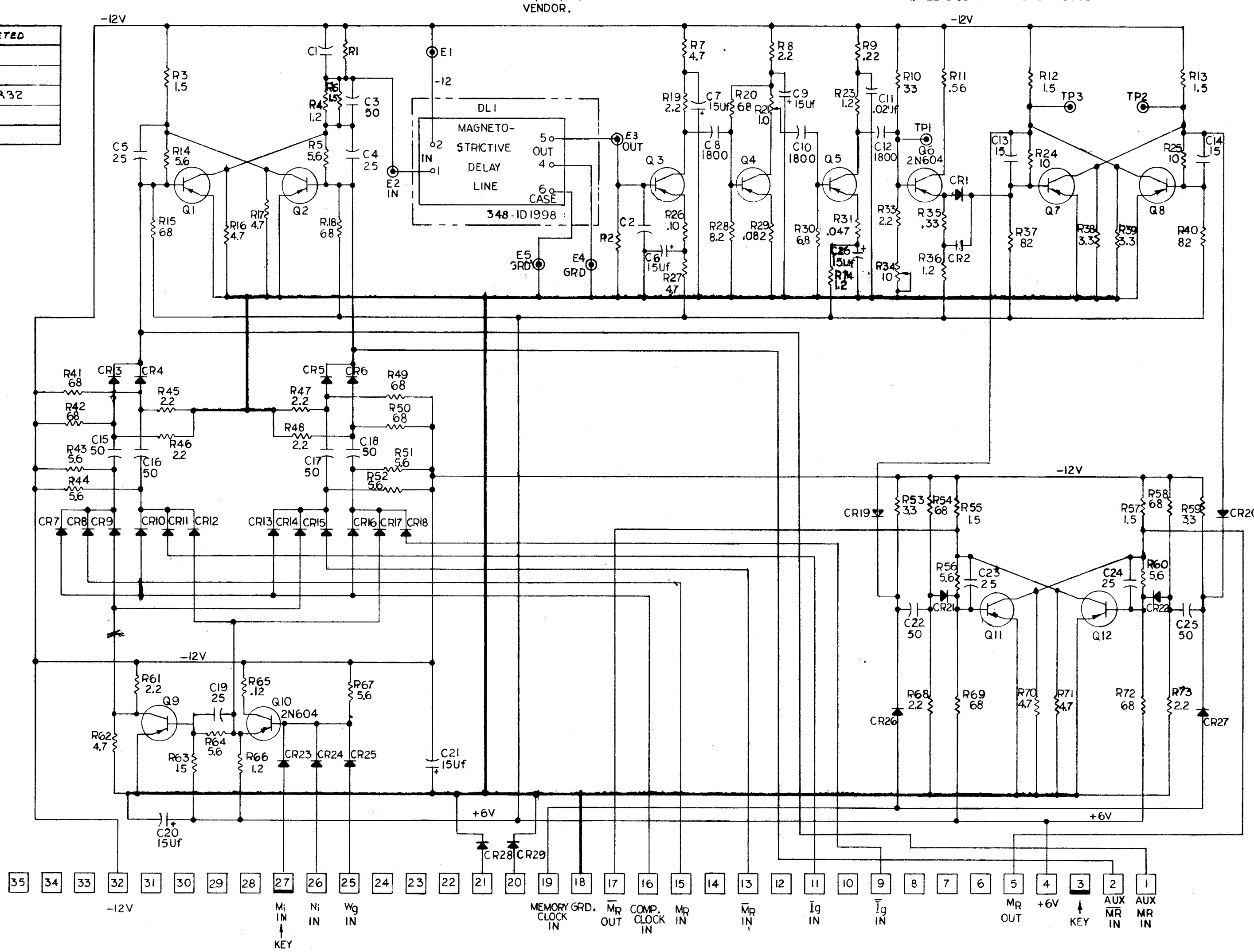


Figure 4-6. MSR-1 Module (Schematic)

FIRST	LAST	DELETED
C1	C14	
CR1	CR7	
L2	L4	L1
Q1	Q7	
R1	R24	R6
TP1		
Y1		

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, $\frac{1}{4}$ WATT.
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3. ALL CAPACITOR VALUES IN UUF.
4. ALL TRANSISTORS ARE 2N604.
5. TWO SWITCHES INCLUDED IN TEST CIRCUIT FUNCTION, NOT LOCATED ON MODULE BOARD.

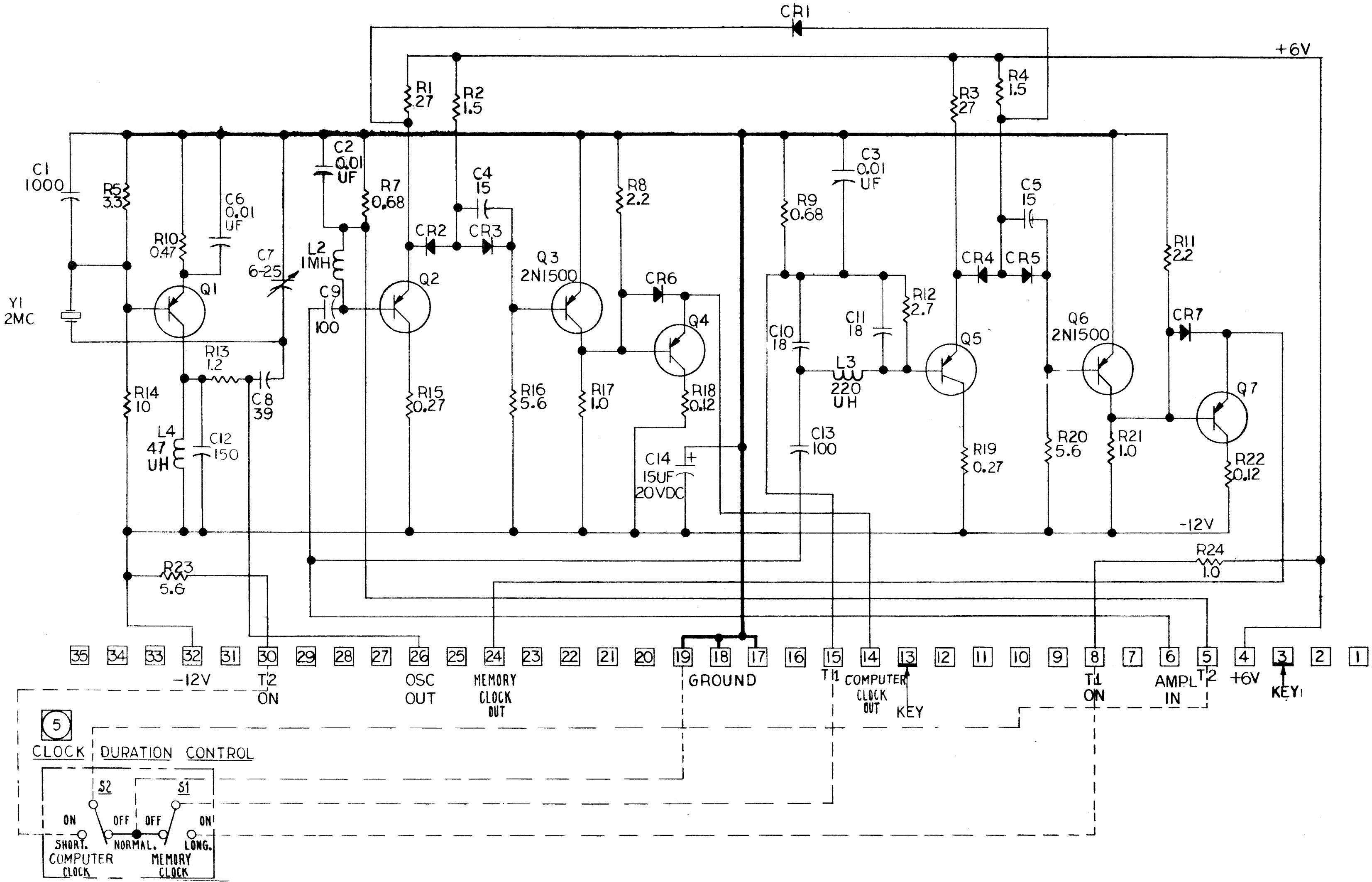


Figure 4-7. XCG-100 Module (Schematic)

V. MAINTENANCE

A. INSTALLATION

Refer to Figure 5-1 for details covering the installation of the MX-1 and MX-2. Ensure that the interconnecting cables between the PB250 and the MX-1 and the MX-1 and MX-2 are properly plugged into their respective connectors. Details of the jumper plugs are given in Table 3-1.

B. INTERCONNECTING CABLES

Refer to Table 5-1 for details covering the interconnecting cable between the PB250 and the MX-1 and Table 5-2 for details covering the connector on the MX-1 for this cable.

Table 5-3 gives details covering the interconnecting cable between the MX-1 and the MX-2 and Table 5-4 gives details covering the connector on the MX-1 for this cable.

Table 5-1.

INTERCONNECTING CABLE, PB250 TO MX-1

PB 250, DB - 25S 7P	Term	MX-1 DBM - 21W1S 1MP
1	M2g	1
2	M3g	2
3	M4g	3
4	M5g	4
5	M6g	5
6	M7g	6
7	N0g	7
8	N1g	8
9	N2g	9
10	N3g	10
11	N4g	11
12	N5g	12
13	N6g	13
14	N7g	14
15	$\overline{\text{Wxg}}$	15
16	$\overline{\text{Ixg}}$	16
17	Spare	
18	Fxg	17
19	Spare	
20	Spare	
21	+6v	18
22	Gnd	19
23	-12v	20
24	Shield	
25	SA out 4	A

Table 5-2.

CONNECTOR, MX-1 TO PB250

Type DBM - 21W1P, 1MJ		
Pin No.	Destination	Term
1	3D27	M2g
2	1J21	M3g
3	2K10, 2MJ3	M4g
4	2MJ1	M5g
5	2MJ2	M6g
6	2MJ3	M7g
7	2MJ7	N0g
8	2MJ8	N1g
9	2MJ9	N2g
10	2MJ10	N3g
11	2MJ11	N4g
12	2MJ12	N5g
13	2MJ13	N6g
14	2MJ14	N7g
15	2MJ15	$\overline{W}$xg
16	2MJ16	$\overline{I}$xg
17	2MJ18	Fxg
18	TB1-1L	+6v
19	TB1-3L	Gnd
20	TB1-6L	-12v
A	2MJ25	SA out

Table 5-3.

INTERCONNECTING CABLE, MX-1 TO MX-2

MX-1 DB - 25S 2MP	Term	MX-2 DBM - 21 W1S 1MP
1	M5g	1
2	M6g	2
3	M7g	3
4	M4g	4
5	Gnd	5
6	Jumper M16r M2g N0g	6
7	N0g	7
8	N1g	8
9	N2g	9
10	N3g	10
11	N4g	11
12	N5g	12
13	N6g	13
14	N7g	14
15	$\overline{Wxg}$	15
16	$\overline{Ixg}$	16
17		
18	Fxg	17
19	Spare	
20	Spare	
21	+6v	18
22	Gnd	19
23	-12v	20
24	Shield	
25	SA out 4	A

Table 5-4.

CONNECTOR, MX-1 TO MX-2

Type DB 25P - 2MJ			
Origin	Pin No.	Destination	Term
1MJ4	1		M5g
1MJ5	2	3K33	M6g
1MJ6	3		M7g
1MJ3	4		M4g
	5	TB1-4L	Gnd
1D8	6		Jumper M16r M2g N0g
1MJ7	7	4E26	N0g
1MJ8	8	5E26	N1g
1MJ9	9	6E26	N2g
1MJ10	10	7E26	N3g
1MJ11	11	8E26	N4g
1MJ12	12	9E26	N5g
1MJ13	13	10E26	N6g
1MJ14	14	11E26	N7g
1MJ15	15	1K20	Wxg
1MJ16	16	2K20	Ixg
1MJ17	17		
	18	3H28	Fxg
	19		Spare
	20		Spare
	21	TB1-1L	+6v
	22	TB1-3L	Gnd
	23	TB1-6L	-12v
	24	Spare	Shield
1MJA	25	2H6	SA out

VI. MX-1 PARTS LIST

Description	Manufacturer	Mfrs. Part No.	PBC Part No.	Qty.
Cable, Assembly			124-1A6416	1
Connector, MJ1	Cannon	DBM-21W1P	274-1A3366-21	1
Connector, MJ2	Cannon	DB-25P	274-1A3366-25-2	1
Connector, 35-pin	Elco	7001-35-5-1-2	274-1A3019-1	35
Module, CD-100	PBC		124-1D2692	1
Module, DG-101	PBC		124-1D2321	5
Module, DG-102	PBC		124-1D2336	1
Module, EF-101	PBC		124-1C4625	2
Module, GD-100	PBC		124-1D2492	1
Module, XCG-100	PBC		124-1C2689	1

LIST OF MANUFACTURERS

Cannon	Cannon Electric Company, Los Angeles 31, Calif.
Elco	Elco Corporation, Philadelphia 24, Pa.
PBC	Packard Bell Computer, Los Angeles 25, Calif.

VII LOGIC LAYOUTS

This section is comprised of logic layouts for clock distribution, signal distribution, memory lines and memory output.

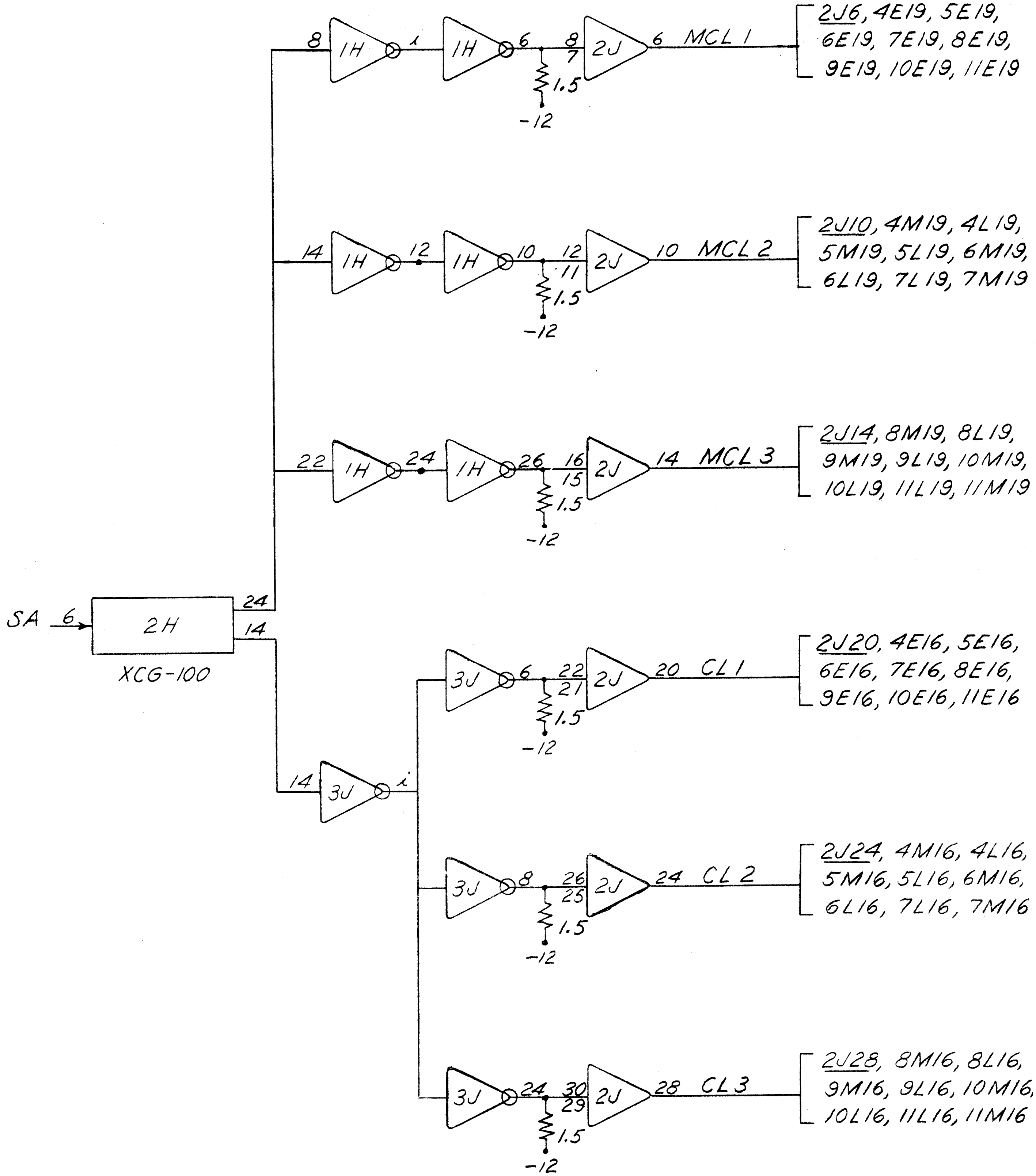


Figure 7-1. Clock Distribution

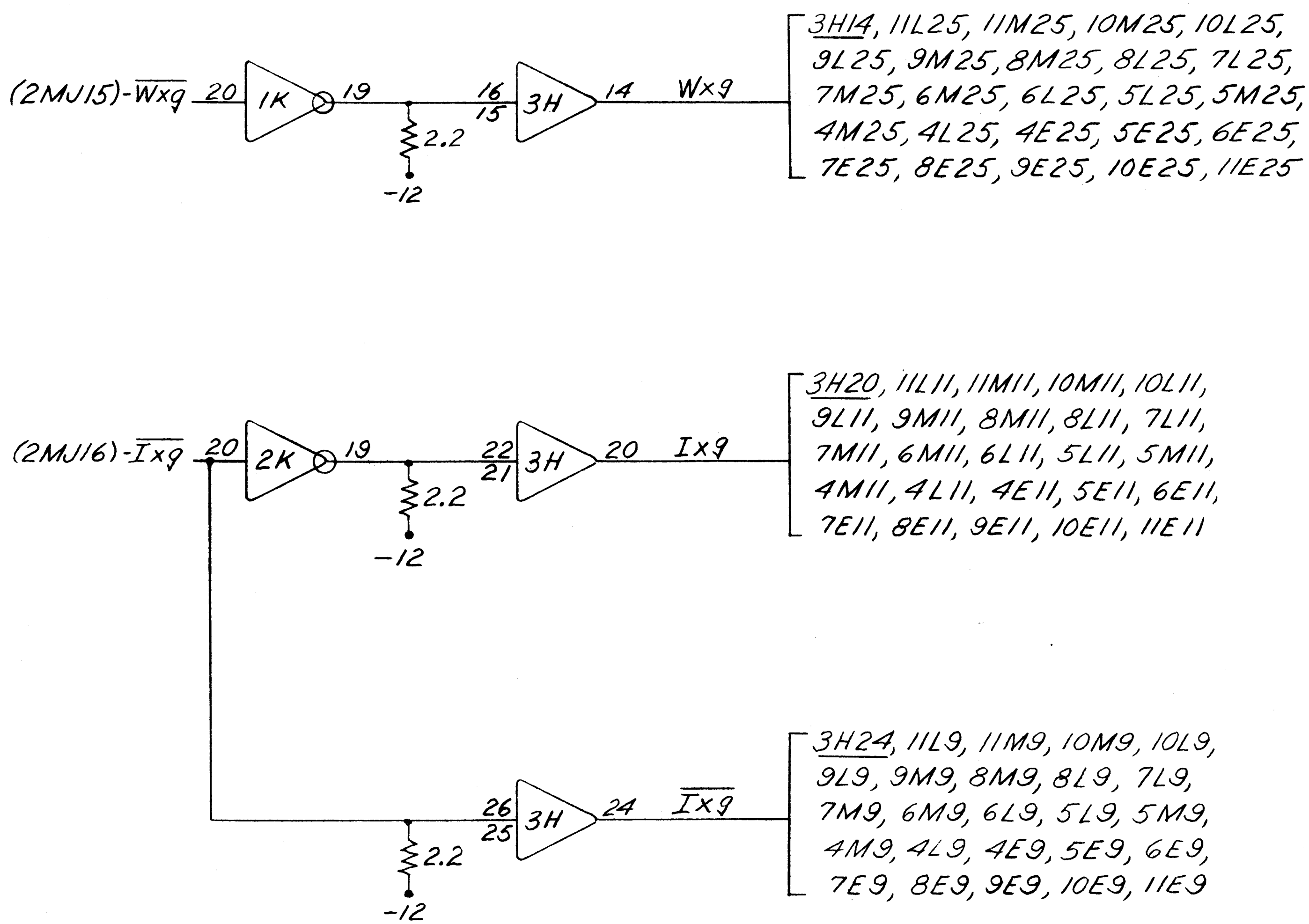


Figure 7-2. Signal Distribution

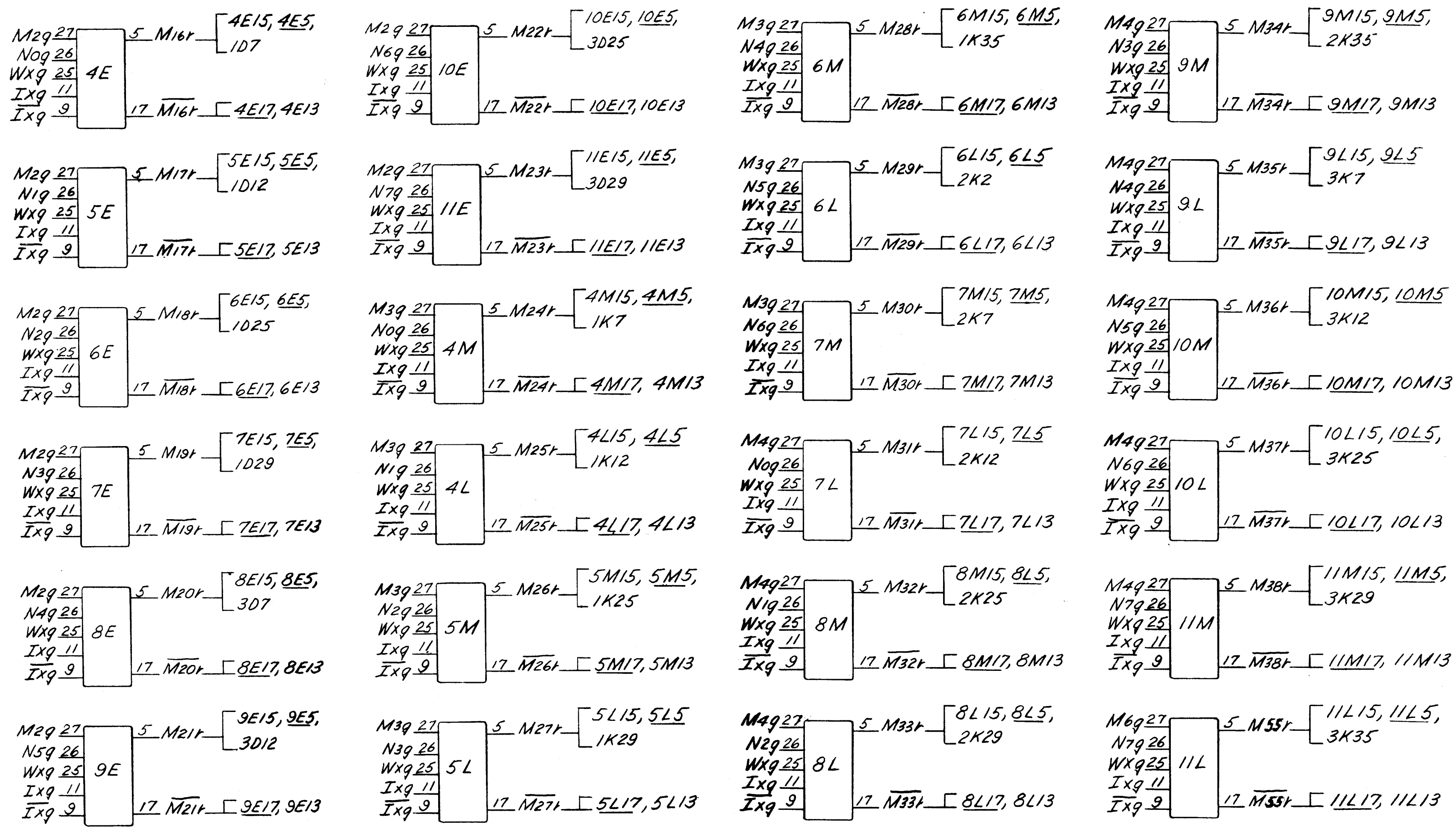


Figure 7-3. Memory Lines

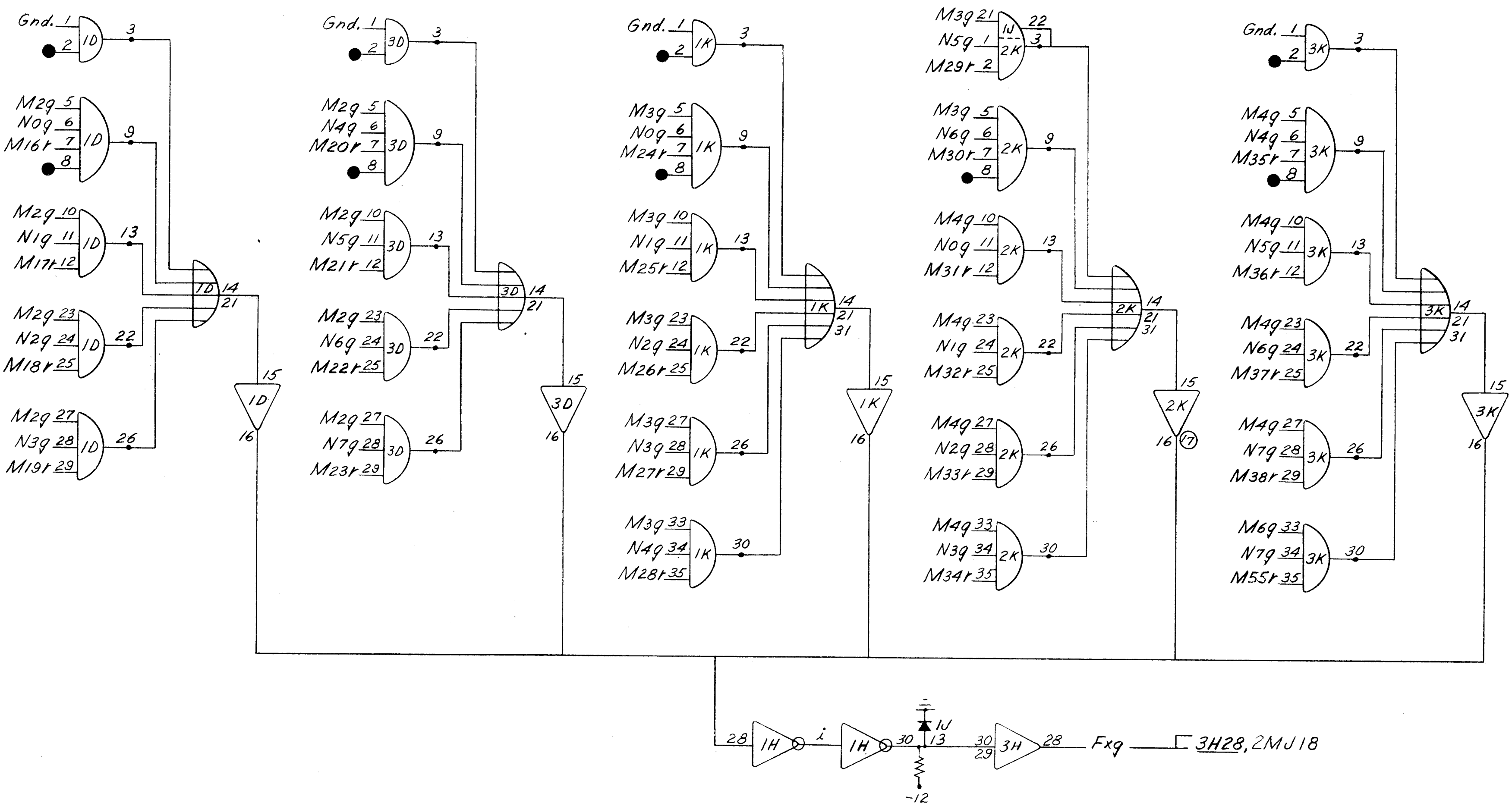


Figure 7-4. Memory Output