PHILCO

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GOVERNMENT & INDUSTRIAL GROUP

COMPUTER DIVISION
WILLOW GROVE, PA.

FIELD SALES BULLETIN

B. McCoy

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Attached is a COMPANY CONFIDENTIAL comparison between the 212 and the 7094 which should be of considerable value to you.

This must not be shown to or left with a customer.

We will attempt to give you further comparison of the 3600 and the 212 in the very near future.

This fine job was done by Gus Mechalas.

R. M. Briggs

RMB/sv

Enclosure

SYSTEM COMPARISON

212 - 7094

COMPANY CONFIDENTIAL

CENTRAL PROCESSOR

212	7094
o 3 addressable arithmetic registers	o 3 registers, only 2 addressable
o Extensive reg. to reg. transfer (direct)	o Most reg. to reg. transfers use memory
o 8 Index Registers	o 7 Index Registers (vs. 3 for 7090, therefore, incompatible programs, though not too serious) see below
o Index Registers compatible	o Problem must state if it is to use 3 or 7 Index Registers and change modes accordingly
o Index Registers can increment or decrement by 1 or any other value	o Only decrement
o 7 Instructions being processed	o 2 Instructions accessed sometimes
o Instructions and operand look ahead	o No look ahead, but merely double-fetch under limited circumstances
o Indirect addressing with 1 or 2 indirect addresses per loc.; 0.5 - 0.5 usec. per level	o Indirect addressing with only 1 indirect address per loc.; 2 usec. per level
o Base address may be in either Index Reg. or in 16-bit non-overlapped address field of instruction	o One 15-bit address field in most instructions; second 15-bit decrement field in only 8 instructions
o Increment or decrement in Index Register; counts up (or down) without using memory time (we cannot decrement automatically)	o Decrement only in Index Registers; counts only indirectly using memory and arithmetic time
o Arithmetic speeds higher :	o Arithmetic speeds lower :

±	.55-1.5	1,818,181	±	4.	250,000/sec
X	4.3	232,557	X	4. - 10	100,000/sec
÷	9.8	102,040	÷	4. - 16	62,500/sec
±	1.3	769,230	±		166,000
X	4.5	222,222	X		100,000
÷	12.3	81,300	-		55,500
±	8.0	125,000	±		125,000
X	25.0	40,000	X		45,000
÷	56.	21,000	÷		26,300

FIXED POINT

FLOAT POINT

DOUBLE PRECISION

212	7094
o Memory addressable to 65K direct or indirect; ~~up to~~ over 1 million words by mode setting (1048K) (Product Line)	o Memory addressable to 32K direct or indirect; to 65K by mode setting (special order only)

65536
16
393216
65536
1,048,576

ASYNCHRONOUS DESIGN

212	7094
o Asynchronous	o Synchronous
o Easy to modify; system components under continuing development	o Must redesign system for further significant advances
o Independent speed I/O	o I/O Programming must be related to machine cycle and I/O timing cycle
o No programming of timing cycle of I/O	o Timing is critical to get simultaneous reads, writes, and movements of data

BUILDING BLOCK

212	7094
NO REPROGRAMMING! (in most cases)	
o More controllers in IOP	o Most building block features cause reprogramming, translation & simulation OR
o Faster memory	
o Faster central processor	

MEMORIES

212	7094
o 4 concurrent memory accesses (partitioned memory) 4-way access of memory permits overlapped access for: 1) Instruction 2) Operands 3) Results 4) I/O	o 1 memory access (2 at a time for instruction, double precision floating-point, and double load instruction - will only double access ~~from~~ even-numbered location) starting with an
o Effective memory speed zero	o Effective memory speed is 1 or 2 usec. per ~~access~~
o 65K per bank; ~~up to~~ over 1 million total words	o 32K total; 65K by mode shift (on special order only)
o 48 bits + 8 parity; character parity carried all the way from I/O to memory	o 36 bits + 1 parity; parity checked? only at interfaces (memory word; I/O character) ?
o .5 usec. reference cycle	o 2. usec reference cycle

TAPES

212	7094
o Tape systems compatible; only one tape system needed by any user (compatible with ½" IBM tape is offered on satellite option)	o Tape systems not compatible; if use Hypertape, must use low-speed tape also
o 90KC transfer rate	o 22.5, 62.5, 90KC (729 tapes)
o 240KC transfer rate (6-bit - 1,936,000 max.)	o 170KC (Hypertape) (8-bit - 340,000 max.)
o 1" tape	o 1" tape — ½" tape on 727 or 729 tape drives
o 3600'	o 1800'
o 66 million characters/reel	o 25 million characters/reel
o $120 a reel	o $135 a reel
o Read forward or backward	o Backward read optional
o Read after write	o Read after write optional
o 64 tapes	o 20 tapes
o Direct selection of tape units independent of channels	o Tape selection restricted to their channels
o No lockout	o Other tapes or a channel lock-out if used by one tape ?
o Eight simultaneous I/O operations	o Two simultaneous I/O operations which can delay program execution
o 10½" diameter	o 10" - 17" - 2" (odd size means new shelving for storage) — 2" tape reels? diameter?
o no alteration of character codes on tape	o character codes altered when recorded on tape

IOP

212	7094
o Tapes use any Controller { 4 controllers (assumbleers) / IOP }	o Tapes fixed to I/O Channels Channel A tapes cannot be switched over to channel B and vice versa
o 32 Tapes to an IOP (32 tapes to a channel)	o 10 Tapes to a channel
o 2 IOPS - 64 tapes 8 Controllers	o 8 Channels (hypertape only 2 channels)
o 6 I/O instructions can do all I/O	o 21 I/O instructions
o Compatible tape systems	o Tape systems not compatible
o Any channel may be reading or writing from any controller RRRR RRRR WWWW WWWW RWWR RRWR (any combination)	o If 2 hypertape channels, only one can be reading and one can be writing R W W R Not Allowed RR WW
o No lockout of tapes All tapes always accessable	o Other tapes ~~locked-out~~ not accessable when channel is used
o 1 and 2 bit error correction	o 1 and 2 bit error correction

MASS STORAGE (DISC)

212	7094
o 160 million what? words or characters	o 258 million words or characters
o 960 KC	o 90 KC
o Does not tie-up data controllers (independent asynchronous transfer)	o Uses special data channel

INSTRUCTIONS

2000/212	7094
o Over 250 instructions	o 189 instructions
o 2 instructions per word	o 1 instruction per word
o 4 instruction access	o 2 instruction access
o 7 instructions being processed, inst. and operand look-ahead	o No look-ahead
o 112 arithmetic instructions	o 39 arithmetic instructions
o Repeat instructions (up to 4 instructions)	o No repeat
o 6 I/O instructions can do all I/O	o 21 I/O instructions
o A compare can jump directly to a routine but our compare costs an instruction to load a register from memory (cannot compare with memory)	o A (CAS) compare must go to a jump because it only skips upon meeting a condition (costs an access and a jump) Not ALWAYS TRUE (18 will skip 18 will branch
o 8X	o 7X
o Index Register Compatibility	o Problem must state if it is to use 3 or 7 index registers and change modes accordingly
o Infinite level of indirect addressing	o Limited level of indirect addressing

WORD CAPACITY

212	7094
Single Precision	**Single**
o 36 bit mantissa	o 28 bit mantissa
o 12 bit exponent	o 8 bit exponent
o 10 significant decimal digits	o 8 significant decimal digits
o $\pm$ 10 $\pm$ 616	o $\pm$ 10 $\pm$ 38
Double Precision	**Double Precision**
o 70 bit mantissa	o 54 bit mantissa
o 12 bit exponent	o 8 bit exponent
o 24 significant decimal digits	o 14 significant decimal digits
Characters	Characters
o 8 six bit characters	o 6 six-bit characters
o 64 character codes	o 51 character codes

REAL TIME

212	7094
o Real Time Scanner, 8 High-speed, multiplexed, real-time channels	o Real- time ~~seems to be~~ is by special order
o Auto Control	o No comparable item
o Interval Timer	o No comparable item
o Does not tie-up data controller - independent asynchronous transfer	o Uses data channel

ON-LINE PAPER TAPE

2000/212	7094
o Reads 1000 c/s	o Reads 500 c/s
o Punches 100 c/s (5, 6, 7, or 8 channel)	o Can not punch
o Does not tie-up Data Controller - independent asynchronous transfer	o Uses Data Controller

PHILCO 1000

212/1000	7094/1401
o Can communicate with 2000 (memory to memory)	o Cannot directly communicate with large computer
o Character computer	o Character computer
o Can simulate any fixed word length (N - Reg.)	o
o Fixed inst. length (4 char.)	o Variable inst. length (avg. 6 char.)
o 3u memory if greater than 4K otherwise 5u	o 11.5u memory
o 4 base address registers	o 2 base address registers
o Binary arithmetic (decimal arithmetic - optional)	o Only decimal arithmetic
o 0, 1, 2 or 3 address instructions	o 2 address instructions
o BTD & DTB hardware	o BTD & DTB under program control (optional inst. package)
o 2 simultaneous I/O operations	o 1 I/O operation
o HSP - 900 L/M	o HSP - 600 L/M
o Photo-electric card reader - 2000 C/M Punch 100 C/M	o Card Reader - 800 C/M Punch 250 C/M
o Photo-electric paper tape - 1000 C/S Punch 100 C/S	o Paper tape - 500 C/S Can not punch
o Printer Plotter	o
o 90KC 240KC 729 tapes Hypertapes (any other competitive tape)	o Only 729 tapes
o Two completely independent programs Ex: C - T T - P	o One program Ex: C - T
o Asynchronous	o Synchronous
o Link with 212 1) All tapes common with 212 2) Memory to memory transfer 3) Communication through real-time scanner (command & control application)	o Link with 7094 1) 1 Common tape with 7094

Author: Betty Jane McCoy
Senior Instructor
Field Operations Division
International Electric Corp.
A Subsidiary of International Telephone
and Telegraph Corp.

IBM 7094 VS. PHILCO 2000/212

A COMPETITIVE ANALYSIS

In the creation of fictional characters for novels, the basic rule is "there are neither all-bad villains nor all-good heroes." This axiom, it can be said, is also true of the computer industry: there are neither all-bad nor all-good computers.

There exists today a tendency for computer salesmen to down-grade competitive equipment and up-grade their own particular system. In the interests of users who may be pondering the relative merits of large-scale, high-speed systems (and also the relative frankness of salesmen), a summary of the salient features of two highly competitive systems is presented: the IBM 7094 and PHILCO 2000 Model 212.

It is curious to note that, while both systems are designed as general-purpose arithmetic data processors, the 7094 offers the least number of arithmetic instructions (39). On the other hand, Philco uses a stored-logic concept which permits the programmer to call upon a variety of operations, registers and options to create a composite and highly versatile group of 112 arithmetic instructions.

It is well known that designers and manufacturers rarely ever develop a machine having a one-to-one instruction relationship. IBM's philosophy prefers to say that the instruction set becomes meaningful only when applied to a particular application. However, by comparing the instruction micro-flow charts for both machines, the exceptional capability of one system over another becomes apparent. The results of such an analysis are summarized by instruction class.

TOTAL INSTRUCTIONS BY CLASS	7094	2000/212
Fixed Point Arithmetic	14	56
Floating Point Arithmetic	25	56
Logical	14	10
Data Transmission	13	23
Shifting	7	15
Branching	21	38
Index Register	24	35
Table-Lookup	3	2
Indicator Sensing	24	0
Input-Output	28	6
Miscellaneous	16	11
TOTAL:	189	252

ARITHMETIC INSTRUCTIONS

Arithmetic operations may be performed in both machines with the operands expressed in either fixed-point or floating-point notation. Fixed-point notation in the 7094 is expressed by a sign and 35 bits; in the 2000/212, it is expressed by a sign and 47 bits. Accuracy in the 7094 is maintained to 10 decimal digits; in the 2000/212, to 14 decimal digits.

In the 7090, extended precision of both mantissa and magnitude can be obtained by the use of extra-cost hardware, involving additional instructions and programming effort. In the 7094, this feature has been replaced by a series of double-precision floating-point instructions which make use of the two 36-bit words which may be simultaneously fetched from memory. These instructions provide an increase in mantissa precision from 8-digit to 16-digit accuracy without an increase in the standard magnitude of 10 ± 38.

Philco provides two standard instructions which enable all floating-point arithmetic operations to be performed in double-precision mode. This produces a signed 70-bit mantissa, increasing the accuracy from 10-digits, single precision, to 24-digits, double precision, without any increase in the already sufficient 10 ± 616 magnitude. The double-precision mode also enables unnormalized results to be obtained, with automatic normalization of the arithmetic registers taking place when the mode is terminated.

LOGICAL INSTRUCTIONS

The functions of AND, inclusive OR and exclusive OR may be performed by both machines. In the 7094, only the Accumulator register and a memory word are involved, but the 2000/212 can use one, two, or all three of its addressable arithmetic registers and a memory word. It should be pointed out that, of the 10 logic instructions in the 212 repetoire, all perform two-valued Boolean-Algebra operations. On the other hand, the 7094 utilizes more than half of its 14-instruction group to perform unique bit-complementing, exchange, sign manipulation, and end-around-carry operations which involve, in most cases, the use of the additional "P" bit of the Accumulator. These so-called logic operations cannot be performed by the 212 since it lacks the additional "P" bit involved.

DATA TRANSMISSION

The score speaks for itself. More flexible data transmission operations can be performed by the 212 with its 23 instructions than can be performed by the 7094 with only 13 highly stylized data transfer instructions. The 212 permits transfer of information entirely within its arithmetic section, an operation which cannot be performed in the 7094 without involving a temporary storage word in memory. An attractive feature of the 212 arithmetic section is the addressable D (or Data) register, comparable to the SR (Storage Register) of the 7094.

The addressability of the D register enables the programmer to do fast data manipulation, similar to that done in the 650, saving considerable time and instructions involving temporary storage and the attendant memory accesses.

SHIFT INSTRUCTIONS

When shifting bits in the 7094, the Sign bit of the Accumulator is never moved, but it will be altered to match the sign of the register from which the bits are shifted under long-left or long-right (LLS or LRS) shift operations. The number of bits to be shifted is modulo 256; therefore, it is possible to clear both the Accumulator and the Multiplier-Quotient registers in one operation. There is absolutely no advantage to this ability; instead, it presents a potential hazard to programming operations. Another drawback of the 7094 is that the Multiplier-Quotient register cannot be shifted as an independent register. On the other hand, the 2000/212 permits independent shifting of all three of its arithmetic registers. The number of bits to be shifted is Modulo 64; therefore, it is impossible to vacate both the Arithmetic and Quotient registers in one operation. The Sign bit of any of the three registers may be shifted when treating the bits as coded characters or may be preserved when shifting numerical data.

As an incidental note, the 212 places negative values into the registers in two's complement form. When right-shifting bits as numerical data, the sign of the arithmetic register determines the mode of the vacated bits; zeroes for insignificant leading bits in a positive number, ones for insignificant leading bits in the two's complement representation of a negative number. Thus, the validity of numerical values is preserved. In the 7094, negative values are presented in the registers and in memory words in an uncomplemented form, but considerable time is utilized in arithmetic operations by complementing the word, performing the operation, and uncomplementing the negative results for appropriate storage.

BRACHING

Branching instructions in the 7094 can be generally divided into two categories: conditional skip and transfer of control. In a conditional skip instruction, if a given condition is satisfied, the next instruction is skipped and the program proceeds from that point. If the condition is not met, the next instruction in sequence is taken. Of the combined total of 37 instructions which are provided, 18 will permit conditional skipping and 18 will permit conditional transfer of control. The remaining instruction provides an unconditional transfer of control (TRA). Of the entire group of conditional branching instructions, Input-Output Control operations define the conditions for 8 instructions (2 transfer, 6 skip), sensable indicators define the conditions for another 8 instructions (5 transfer, 3 skip), and comparison of bits, words and conditions in the central processor define the conditions for the remaining group (11 transfer, 9 skip).

All of the branching instructions in the 212 provide conditional or unconditional transfer of program control. Only three instructions which are concerned solely with input-output operations, provide conditional skipping of the next instruction sequence. Branching instructions are called Jumps in the 212 and the instruction address to which a jump is to be made is indicated in the address field and in one bit of the command field due to the appearance of two instructions in one computer word. The half-word instruction is addressed as the left or right half of a full word by the inclusion of L or R in the jump instruction. Symbolic addressing of instructions does not require the programmers' attention to this detail however, since the assignment of instructions to absolute half-word locations is handled by the assembler program. In 212 branching, if a specified condition is met, transfer of control takes place, otherwise the next instruction in sequence is taken. In either case, the address of the next sequential instruction (the one that immediately follows the jump instruction) is placed

into the program-accessable Jump Address (JA) register for use if a return to the point of program deviation is desired.

A branching-instruction set in the 212 provides an attractive one-instruction method of handling sort keys and performing related bit-testing. The high or low order bit of the Quotient register is tested and the contents of the register cycled one bit to the left or the right respectively, bringing the next bit into position for testing. If the specified condition is met, transfer of control will also take place.

INDEX REGISTER OPERATIONS

The 7094 provides 7 index registers for programmer use and are addressed 1 through 7 respectively. Since multiple tag operations were permitted in the 709 and 7090, a set of instructions are made available in the 7094 which permit multiple tag operation mode (logical ORing of two or three registers to produce an effective memory address). The 2000/212 provides 8 index registers addressed 0 through 7 or 1 thru 8 (where) = 8). Multiple tag operations are not permitted, as they are in the 7094.

In address modification operations, it must be noted that the index registers of each machine works exactly opposite to those of the other. In the 7094, the effective address produced is the difference between the instruction address field contents and the index register contents, while in the 212, the effective address produced is the sum of the contents of instruction address field and index register. To further complicate matters, the index registers of the 212 have two associated bits which, depending upon their setting, will permit automatic incrementation (by one) of the register contents after the effective address is produced, incrementation or decrementation by a variable quantity contained in the instruction address field, or no modification of the register whatsoever.

Iterative loops can be performed quite readily in both machines, however, the testing and branching instructions of the 7094 are more easy to use since the 2000/212 requires the loading of the Data register with a comparison quantity and a branching address in most cases, even though the instructions are more powerful in their overall accomplishments. A set of instructions discussed in the summary provide the 2000/212 with the ability to repeat automatically 1, 2, 3 or 4 instructions in sequence without requiring the attendant index register modification, testing and branching instructions.

TABLE LOOK-UP

In the table-look type instructions provided for both machines, (Convert for 7094, Smaller-word/Larger-word for 212), it is best not to look either of these gift-horses in the mouth since the care and feeding involved far outweighs the end product in many cases.

INPUT-OUTPUT OPERATIONS

The dissimilarity between any two competitive systems is usually illustrated most graphically by the relative input-output operations that can be performed. The 7094, in magnetic tape operations, permits the writing and reading of variable-length records which can be grouped together in seperate files of information. The 2000 permits the writing and reading of fixed-length blocks of information, each of which can constitute a part of a record, a full record, several records, or even a complete file. A high-speed (240KC) tape unit will soon be standard equipment on the 212 and will permit up to 16 variable length records (of from 1 word to 4096 words per record) to be written on the tape at one time instead of the now standard fixed-length-block tape units. The 7094 requires that a seperate program of instructions be written for input-output operations, to be executed at the same time as the processing program when appropriate instructions are given. In the Philco 2000, a single order is set up in the Data Register which is transferred to the appropriate input-output device

by a transfer Input-Output instruction. There, the component parts of the order are seperated and are executed independent of, but simultaneously with, the program being executed in the central computer.

INSTRUCTION SUMMARY

Both machines provide forms of indirect addressing wherein instruction X can call on instruction Y to provide the address of word Z that is to be utilized in the execution of instruction X. Also, both machines will accept the instruction repetoires of their predecessors since they are merely extensions of the pre-established set. IBM had to add a group of 8 instructions to permit existing 704/709/7090 programs to be run on the 7094. Not so of Philco, since less than 20 new instructions were merely added to the existing 210/211 repetoire.

Another programming advantage that the 212 has over the 7094 is the Repeat and Double Repeat instruction group which will permit the repetition of 1, 2, 3, or 4 instructions in sequence and thus is a powerful aid to the performance of short iterative loops. The Repeat instruction will permit up to 4095 iterations to be performed; Double Repeat will permit up to 255 iterations.

HARDWARE HIGHLIGHTS

As far as input-output hardware is concerned, the 7094 is equipped with one (but optionally with up to 8) data channels to which may be connected up to ten tapes, a printer, card reader and card punch, all operated on-line in programmed asynchronous mode. Disc Files, Hypertapes and real time devices are optional equipment. If they are added, and an entire array of required input-output instructions must be added to the basic instruction repetoire.

The 2000/212 offers one or two Input-Output Processors which are similar to the 7094 data channels, but to which are connected up to 32 magnetic tapes, or a combination of online tapes, switchable tapes, and Universal Buffer Controllers to which are connected printers, card systems, (reader and punch), paper tape systems (reader and punch). This combination permits either online or offline

operation of the devices attached to the Universal Buffer Controller. Magnetic Drums, Disc Files, real time devices, accounting clock, X-Y plotter, on-line paper tape, and a variety of devices are optional equipment, but none require any addition to the instruction repetoire since the input-output orders required by these devices are handled appropriately by the same basic I/O instruction.

The core memory unit of the 7094 is limited to a maximum of 32, 768 36-bit words. Philco has brilliantly provided for expandable 48-bit word core storage in 8K, 16K, 32K and up to 16 banks of 65,536 words, putting the data handling potential of the 212 into the million-word Ferranti Atlas class. Philco has also made provisions for program multisequencing and automatic program interrupt operations which are becoming basic necessities in complex computer-controlled systems.

Most impressive, overall, is the phenominal speed of the 212. The entire system works in asynchronous mode with a memory access cycle of 1.0 micro-seconds and variable instruction timing in the central processor. The 7094 is harnessed to a fixed timing cycle of 2 microseconds in the memory and central processing units. Only the input-output data channels operate in an asynchronous mode but they can delay execution of instructions at least one timing cycle. Both machines feature an instruction overlap since, in most cases, two instructions are fetched from memory during one access cycle, but in the 212, four instructions (two per word) are available for execution in the instruction unit as contrasted to two (one per word) instructions in the 7094.

The latest version of Philco's algebraic translator, ALTAC, is running on the 212 and accepting standard FORTRAN-language programs. A 7090 FORTRAN program was quoted by the Philco New York Office as being run on the 212 at what seemed to be a fantastic speed six times faster than the 7090.

A check with the Philco factory proved this to be conservative, as the figure proved to be in the neighborhood of from 7 or 8 to 1 faster.

SUMMARY

The functional characteristics of the 7094 system components remain unchanged from those of the 7090 system. All that is new is the addition of four index registers to the existing three, 20 new programming instructions (plenty more when additional I/O units are added), and the ability to do double precision floating-point arithmetic. The basis system operating cycle has been lowered from 2.18 microseconds on the 7090 to 2.0 microseconds for the 7094 and two instructions are fetched from memory whenever possible, a feature that has always been standard on all Philco systems. The overall effect, as quoted by IBM, is to present a computer that is at the most 1.5 to 2 times faster than the 7090.

With the 212, an entirely new central computer and a high-speed memory was developed to work compatably with the standard I/O components of the 2000 system. New high-performance tapes which will transfer 240,000 six-bit characters per second have been made an optional feature to offset the 7340 Hypertapes whose transfer rate is only 170,000 six-bit characters per second.

As to cost, it appears that the 212 will be leased for a price considerably less than a comparable 7094 system. All in all, it looks as if Philco, with the new FORD look, ~~will~~ could give IBM's 7000 series a real run for the money.

TABLE OF COMPARISONS

AREA	7094	2000/212
Bits per word	36	48
Decimal accuracy maintained	10 digits	14 digits
Floating-point mantissa	S, 27 bits	S, 35 bits
Mantissa decimal accuracy	8 digits	10 digits
Exponent representation	8-bit characteristic	S, 11 bits
Exponent Magnitude	10 ± 38	10 ± 616
Double Precision Floating-Point	Yes	Yes
D. P. Mantissa decimal accuracy	16 digits	24 digits
Unnormalized Floating-Point	Yes	Yes
Single Addressing	Yes	Yes
Instructions per word	One	two
Indirect Addressing	Yes	Yes
Number of Index Registers	7	8
Automatic Index Modification	No	Yes
Instruction Overlap	Yes	Yes
Asynchronous operation	No (tape channels only)	Yes
Memory size (max. words)	32K only	from 8K to 1048K
Memory access cycle	2.0 usec	1.0 usec
Tape Control Devices	8 Data Channels	2 Input-Output Processors
No. of tapes per device	10	32
No. of tapes in simultaneous operation	1 per data channel	4 per IOP
Tape transfer rate (6 bit characters/sec.)	62.5K HiDensity (729IV)	90K