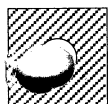


PHILIPS



Electrical Adjustments CDM3600

Version: 3.1

December 2th, 1997

		Electrical Adjustments CDM3600		3104 147 0137 0		97/13/05			
		Version 3.0 printed: 10/19/98				97/09/15			
						97/12/02			
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1. Test equipment.

- Popeye testtool version 6.5. All the adjustments are done with the help of Popeye testtool.. Macro's make it easier to give the proper commands.
- Laser measurement tool EBM HCCM-7 7104 089 0360.2.
- Voltmeter PM 2544
- Oscilloscope w 3.5 ns. eg. PM 3394A.
- Power supply eg. PE 1542
- Measuring circuit for digital servo loops CE3026
- Dynamic signal analyzer HP3562A
- Testdiscs

5B2 TEST SAMPLE 5B 814 127-2 batch YG

SBC444 testdisc selected for substrate current and betatarget.

ATER/TLN testdisc (3104 149 00410, see sheet 112 for latest change figure)

2. First check.

- Check the supply voltages:

5V $\pm$ 1%

12V $\pm$ 1%

- Check version number CDM-EEPROM.

- Update CDM-eprom to latest version.

Reset : After reset the sledge is moving to the inside. The selftest must be zero and no errors may occur. With software DE41 (HC11) and EEPROM version V50

- Adjustment Read power

The read power has to be adjusted before the write power.

Use the EBM power meter to measure the output power out of the objective lens.

* Adjust the readpower to $700 \pm 20 \mu\text{W}$ by controlling DAC_READ_POWER (DAC08).

* Store the DAC value into EEPROM address 0x14.

* Store the DAC value for N=1 and N=2 to address 0x21, 0x41, 0xC1 and 0xD1.

* Multiply the value with 1.4 (< FFh !) and store for N=6 to address 0x61, 0xE1 and to address 0xF1 (CDE read OPC power).

Use the macro 'laser.mcr'.

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3. Adjustment Write power

3.1 Write power level.

13.4 mW for & N=1 and
18.2 mW for & N=2 separately.

3.2 Write power N=1.

All the settings for write power adjustment can be found in the macro: laser.mcr.
Use the EBM power meter to measure the output power.

- Set the following DAC's:

DAC_DELTA_P	(DAC 04) :	255	DeltaP = 0%
DAC_FS0	(DAC 02) :	255	FS0 = 255
DAC_ALPHA0	(DAC 0E) :	255	ALPHA0 = 255
DAC_WRITE_COARSE	(DAC 0D) :	255	
DAC_WRITE_FINE	(DAC 03) :	255	
DAC_N2	(DAC 19) :	0	N = 1

- Adjust DAC_WRITE_COARSE starting from 255 to 0 for an output power between 9.5 mW (70%) and 13.4 mW (100%).
 - Store DAC_WRITE_COARSE value N=1 into EEPROM address 0x23.
 - Adjust DAC_WRITE_FINE starting from 255 until 13.4 mW is reached within 0 and +0.3mW.
 - Store value DAC_WRITE_FINE value N=1 into EEPROM address 0x24.
- User the macro 'laser.mcr'.

3.3 Write power N=2

- Place the EBM power meter above objective lens.
- Start with the following DAC settings:

DAC_DELTA_P	(DAC 04) :	255	DeltaP = 0%
DAC_FS0	(DAC 02) :	255	FS0 = 255
DAC_ALPHA0	(DAC 0E) :	255	ALPHA0 = 255
DAC_WRITE_COARSE	(DAC 0D) :	255	
DAC_WRITE_FINE	(DAC 03) :	255	
DAC_N2	(DAC 19) :	255	N = 2

- Adjust DAC_WRITE_COARSE starting from 255 until DAC_WRITE_COARSE_{N=1} value is reached.
 - Store DAC_WRITE_COARSE value N=2 into EEPROM address 0x43
 - Adjust DAC_WRITE_FINE starting from 255 until 18.2mW is reached within 0 and +0.4mW.
 - Store DAC_WRITE_FINE value N=2 into EEPROM address 0x44.
- Use the macro 'laser.mcr'.

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3.4 Delta-P

Use the EBM power meter to measure the output power.
Set the following DAC's:

DAC_DELTA_P:	255	DeltaP= 0%
DAC_FS0:	255	FS0= 255
DAC_ALPHA0:	255	ALPHA0=255
DAC_N2:	0	N=1

- For 0% deltaP store the value 255 into EEPROM.
- Adjust with DAC_DELTA_P until deltaP 10 % is reached within $\pm 1\%$.
- Store into EEPROM address 0x1A.
- Adjust with DAC_DELTA_P until deltaP 20 % is reached within 0 and -2%.
- Store into EEPROM address 0x18.
- Adjust with DAC_DELTA_P until deltaP 30 % is reached within $\pm 1\%$.
- Store into EEPROM address 0x1B.

In fig.1 one can see how the DeltaP is defined.

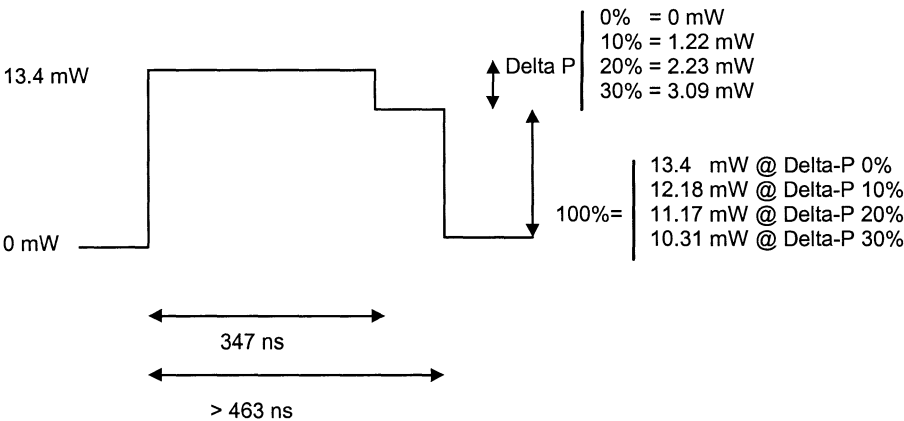


Fig. 1: Definition of Delta-P at N=1.

Use the macro 'Delta-p.mcr'.

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4. Adjustment CDE powers

set timing for N=2 by I2Sout =2fs

Use the EBM power meter to measure the output power.

Set the following DAC's:

DAC_DELTA_P (DAC 04)	: 255	DeltaP = 0%
DAC_CDE (DAC 80)	: 255	Timing CDE
DAC_PMAX (DAC 0B)	: 255	
DAC_PMIN (DAC 07)	: 0	
DAC_N2 (DAC 19)	: 255	N = 2
DAC_WRITE_COARSE (DAC 0D)	: 255	
DAC_WRITE_FINE (DAC 03)	: 255	
DAC_FS0 (DAC 02)	: 255	FS0 = 255
DAC_ALPHA0 (DAC 0E)	: 255	ALPHA0 = 255

Adjust DAC_P_ERASE N=2 (DAC 04) starting from 128 until 10 mW is reached within -0 and +0.4mW.

Adjust DAC_WRITE_COARSE (DAC 0D) CDE N=2 until 18.7mW is reached within -0.3 and +0.3mW.

Store value DAC_WRITE_COARSE CDE N=2 into EEPROM address 0xD3.

Adjust DAC_WRITE_FINE (DAC 03) CDE N=2 until 18.7mW is reached within -0.3 and + 0.3mW.

Store value DAC_WRITE_FINE N=2 into EEPROM address 0xD4.

Set the following DAC :

DAC_ALON (DAC 25)	: 0	Alpha off
-------------------	-----	-----------

Adjust DAC_FS0 (DAC 02) until 14 mW is reached within -0 + 0.4mW.

Adjust DAC_P_ERASE N=2 (DAC 04) until Pe equals 40% of Pw within -0 + 0.4mW.

Store value DAC_P_ERASE N=2 (DAC 04) into EEPROM address 0xD7.

Adjust DAC_P_ERASE N=2 (DAC 04) until Pe equals 66% of Pw within -0 + 0.4mW.

Store value DAC_P_ERASE N=2 into EEPROM address 0xDE.

Calculate the other Erase powers :

A = value for Pe/Pw 40 % B= value for Pe/Pw 66 %

Pe/Pw 43% = A + ((B-A) *3/26) store into EEPROM address 0xD8

Pe/Pw 46% = A + ((B-A) *6/26) store into EEPROM address 0xD9

Pe/Pw 50% = A + ((B-A) *10/26) store into EEPROM address 0xDA

Pe/Pw 54% = A + ((B-A) *14/26) store into EEPROM address 0xDB

Pe/Pw 58% = A + ((B-A) *18/26) store into EEPROM address 0xDC

Pe/Pw 62% = A + ((B-A) *22/26) store into EEPROM address 0xDD

Use the macro 'lsr_cde.mcr.'

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5. Adjustment readpower.

0.7 mW for readpower CDR-disc and CDRW-disc

5.1. Adjustment readpower with substrate current

- Use SBC444 disc.
- Reset Main board.
- Connect voltmeter between +12V and substrate.
- Put voltmeter to zero.
- Adjust the substrate voltage to $118 \text{ mV} \pm 2 \text{ mV}$ by controlling DAC_READ_POWER.
- The value for DAC_READ_POWER must be ≤ 182 .

Store the DAC_READ_POWER values into EEPROM for

N=1 to address 0x21 and 0xC1
 N=2 to address 0x41 and 0xD1
 N=6 to address 0x61 (= 1.4 * readpower N=1(0x21))
 0xE1 (= 1.7 * readpower N=1 (0x21))

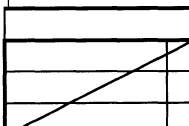
CDE read OPC to adress 0xF1 (= 1.4 * readpower N=1 (0x21))

Use the macro 'substr.mcr'.

6. Adjustment TLN.

- Use ATER/TLN testdisc.
- Reset MAIN PCB.
- Connect a low pass filter 10k and $47\mu\text{F}$ (bipolair) between TLN and GND.
- Connect DC voltmeter across the $47\mu\text{F}$.
- Adjust TLN-lowpass to $0 \pm 30 \text{ mV}$ by controlling DAC_TLN_OFFSET.
- Store the DAC value into EEPROM 0x17.

Use the macro 'tln.mcr'.

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7. Adjustment beta target.

- Use the TESTDISC SBC444 at 1 min and the macro 'betarget.mcr'. The NEC software measures at the given time 50 samples of A1 and A2. Popeye reads these values and calculates beta and betatarget with the following formulas:

$$\text{Beta} = (\text{som A1} - \text{som A2}) / (\text{som A1} + \text{som A2}).$$

$$\text{Beta0} = \text{Beta} * 8192.$$

$$\text{Betatarget} = (\text{Beta0} / 6.4) + 64.$$

The value Beta is also available in the NEC uP in memory at adress XX

- Store the betarget values into EEPROM at address 0x20 for N=1 and at address 0x40 for N=2.

Use the macro 'tln.mcr'.



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8. Adjustment Balance circuit.

- Use the ATER/TLN testdisc.

This disc is recorded at N=2 with a high beta.

The beta is approximately 12% on a reference CDM12 player (see p. 112, 3104 149 00412).

The disc is written from 02.00.00 till 07.00.00

- Use the DC-NOISE testcircuit appendix 4.

This circuit uses PP and measure the noise from 50 kHz to 200 kHz.

The player has to be in PAUSE to be independent of sledge steps.

The disturbance from the pause jump is killed by using the OTD (off track detector) signal.

- Use the macro 'balance.mcr'.

This macro should be used as follows:

- Adjust DAC_BALANCE untill DC-NOISE is minimum (DC-NOISE {min}).

When starting this adjustment, start with the electrical minimum balance value which is already in the EEPROM (retrieve from EEPROM).

This value has been stored in the EEPROM when the PCB was measured. Do not change this value.

- Calculate $1.4 \cdot \text{DC-NOISE}_{\min}$ and adjust DAC_BALANCE for DAC_BALANCE- and DAC_BALANCE+ until for both values $1.4 \cdot \text{DC-NOISE}_{\min}$ is reached. See fig.2.
- Calculate $\text{DAC_BALANCE}_{\text{adj}} = (\text{DAC_BALANCE-} + \text{DAC_BALANCE+})/2$ and store this value into EEPROM address 0x16.

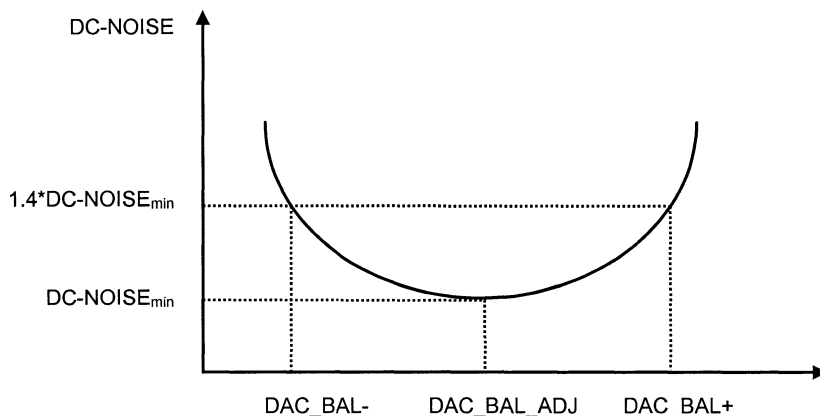
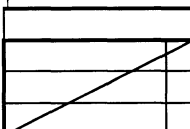


Fig.2: Adjustment balance

Use the macro 'balance.mcr'.

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9. Adjustment focus and radial gain.

9.1 General.

For the adjustment of the gain of the radial and focus servo loop the circuit is used as described in "A measuring circuit for digital servo loops" AHR-36-03-012. At 1800Hz the open loop gain is measured. This gain can be adjusted with a coefficient in the EEPROM.

If the gain needs a correction the concerning coefficient is read from EEPROM, corrected and written back.

The easiest way to do this is to use the special utility in Popeye. With this utility the original gain is read from EEPROM and by pressing the "+" and "-" key a new gain value is sent to the servo. This can be done until the proper gain is reached. Next this value is written to EEPROM.

Use testdisc: SBC444 and Dynamic signal analyzer HP3562A.

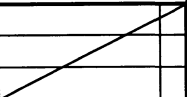
9.2 Settings analyzer:

- measuring mode: swept sine
- select measurement: frequency response
- averages: 10
- frequency: start 200 Hz
- frequency: stop 20 kHz
- source: 100 mVt
- measurement display: frequency response
- coordinates: trace A mag(lin)
- coordinates: trace B phase
- trace A y fixed scale 0...2
- source, source level focus: 0.5 Vpk
- source, source level radial: 0.1 Vpk
- start
- source, manual sweep: 1800 Hz, sweep hold

9.3 Procedure

Use popeye; (commands in *italics*) connect the measuring circuit to R3039 for focus or R3038 for radial and the clock to R3041. Use the macro 'bandw.mcr'.

- N=2: retrieve data 00 min 2 sec 16 fr 100.000 blocks
- Adjust the gain at the frequency according to the table below
- Popeye: *diagnost*, focus, radial gain
- press "+" or "-" key to adjust
- write the gain to eeprom
- requirement: $|H_{desired}| \pm 3\%$

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Sservo	measuring point	frequency	Hdesired	EEPROM address
focus N=2	R3039	1800 Hz	0,65	4E
radial N=2	R3038	1800 Hz	0.75	5B

- Calculate the values for radial n=1 and n=6 as follows:

EEPROM V53/54:

RECORDABLE:

$\text{Rad-gain}_{N=1} = 1.06 * \text{rad-gain}_{N=2}$ and $\text{rad-gain}_{N=6} = 0.53 * \text{rad-gain}_{N=2}$.

- Save the values into EEPROM address 0x3B and 0x7B.
 $\text{Foc-gain}_{N=1} = 1.0 * \text{foc-gain}_{N=2}$ and $\text{foc-gain}_{N=6} = 0.58 * \text{foc-gain}_{N=2}$.
- Save the values into EEPROM address 0x2E and 0x6E.

REWRITABLE:

$\text{Foc-gain}_{N=1} \text{ CDE} = 0.7 \times \text{Foc-gain}_{N=1} \text{ CDR}$.

- Save the value into EEPROM address 0x27 .
 $\text{Foc-gain}_{N=2} \text{ CDE} = 0.7 \times \text{Foc-gain}_{N=2} \text{ CDR}$.
- Save the value into EEPROM address 0x47 .
 $\text{Foc-gain}_{N=6} \text{ CDE} = 0.7 \times \text{Foc-gain}_{N=6} \text{ CDR}$.
- Save the values into EEPROM address 0x67.

Use the macro 'bandw.mcr'.

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10. Appendix 1, Macros.

10.1 Laser.mcr

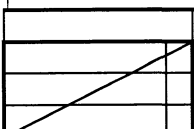
```

401 Adjust laser READ and WRITE power
199 002 066 001          ; laserread on
401 Place photodiode above objective lense
401 Adjust 0.79 mW= 0.7 mW (CA**) with DAC_READ_POWER
94                        ; Edit dac data
401 Write power n=1
199 003 072 025 0        ; DAC_N2  N=1
199 003 072 013 255      ; DAC_WRITE_COARSE
199 003 072 03 255       ; DAC_WRITE_FINE
199 003 072 004 255      ; DAC_DELTA_P
199 003 072 002 255      ; DAC_FS0
199 003 072 0014 255     ; DAC_ALPHA0
199 003 070 001 001      ; laser write on alpha on
401 Adjust write power with DAC_WRITE_COARSE to 13.4mW and store into EEPROM
94                        ; edit dac data
401 Adjust write power with DAC_WRITE_FINE to 13.4mW and store into EEPROM
94                        ; edit dac data
,*****
401 Write power n=2
199 003 072 013 255      ; DAC_WRITE_COARSE
199 003 072 03 255       ; DAC_WRITE_FINE
199 003 072 025 255      ; DAC_N2  N=2
199 003 070 001 001      ; laser write on alpha on
401 Adjust write power with DAC_WRITE_COARSE to DAC_WRITE_COARSEN=1 value and
store into EEPROM
94                        ; edit dac data
401 Adjust write power with DAC_WRITE_FINE to 18.2mW and store into EEPROM
94                        ; edit dac data
401 Ready; reset main PCB with button.
CA** = calculated with average ratio satellite/central spot
    
```

10.2 Delta-p.mcr

```

401 Adjust LASER DELTA-P
154 1                    ; set speed N=1
199 002 066 001          ; laserread on
199 003 072 025 0        ; DAC_N2  N=1
199 003 072 002 255      ; DAC_FS0
199 003 072 014 255      ; DAC_ALPHA0
199 003 070 001 001      ; laser write on alpha on
401 Adjust Delta-P 10 % and store into EEPROM
94                        ; edit dac data
401 Adjust Delta-P 20 % and store into EEPROM
94                        ; edit dac data
401 Adjust Delta-P 30 % and store into EEPROM
94                        ; edit dac data
401 Ready; reset main PCB with button.
    
```

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10.3 Lsr_cde.mcr

401 Adjust Laser CDRw power
199 002 20 05 ; I2 OUT = 2fs
401 laser : read on
199 002 066 001 ; laserread on
401 Place photodiode above objective lens
401laser: write on, alpha on
199 003 070 001 001 ; laser write on alpha on
199 003 072 004 255 ; DAC_DELTA_P
199 003 072 128 255 ; DAC_CDE
199 003 072 011 255 ; DAC_PMAX
199 003 072 007 000 ; DAC_PMIN
199 003 072 025 255 ; DAC_N2
199 003 072 013 255 ; DAC_WRITE_COARSE
199 003 072 003 255 ; DAC_WRITE_FINE
199 003 072 002 255 ; DAC_FSO
199 003 072 014 255 ; DAC_ALPHAO
401 Adjust DAC_P_ERASE N=2 (40%) to 10 mW (Write power verloopt)
94 ; edit dac data
401 Adjust DAC_WRITE_COARSE to 18.7 mW and store to EEPROM
94 ; edit dac data
401 Adjust DAC_WRITE_FINE to 18.7 mW and store to EEPROM
94 ; edit dac data
199 003 072 009 000 ; DAC_ALON
401 Adjust DAC_FSO to 14 mW
94 ; edit dac data
401 Adjust DAC_P_ERASE N=2 to 40% of Write Power and store in EEPROM
94 ; edit dac data
401 Adjust DAC_P_ERASE N=2 to 66% of Write Power and store in EEPROM
94 ; edit dac data
401 Calculate other Erease powers and store in EEPROM
94 ; edit dac data
401DRUK OP RESET KNOPJE



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10.4 Substr.mcr

```

401 Adjust substrate current.
102                               ; tray out
101                               ; tray in
401 Insert disc SBC444.
401 Connect DC Meter between '+12V' and 'SUBSTR'.
401 Set meter to zero to remove offset!
199 002 017 001                 ; set speed n=1
401 Start
199 001 002                     ; start
401 Seek 3 sec
199 005 006 000 003 000 001     ; seek 0 3 0 data
401 Adjust substrate to 115..120mV with DAC_READ_POWER and save to EEPROM
94                               ; edit dac
401 Ready, reset main PCB with button.
    
```

10.5 TLN.mcr

```

102                               ;tray out
401 Insert ATER disc
101                               ; tray in
401 Connect DC voltmeter between TLN filter and GND
199 001 002                     ; service start
199 002 069 000                 ; rad off
401 Adjust TLN to 0+/-30mV with DAC_TLN_OFFSET and save into EEPROM
94                               ; edit dac
401 Reset main PCB with button
    
```

10.6 Balance.mcr

```

102                               ; tray out
401 Insert ATER/TLN testdisc.
101                               ; tray in
401 Connect DC voltmeter between 'DCNOISE' and GND.
154 001                         ; speed n=1
103                             ; start
105 003 000 000 001             ; read 1 block at 3.00 min
401 Adjust balance with DAC_BALANCE
401 First find minimum DCNOISE value.
401 Then find + and -140% values and calculate the average value.
94                               ; edit DAC_BALANCE
401 Save into eeprom.
94                               ; edit DAC_BALANCE
104                             ; stop
401 Ready; reset main PCB with button.
    
```

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10.7 Betarget.mcr

```

401 ADJUST BETA TARGET.
102                               ; tray open
401 Insert disc SBC444.
101                               ;tray close
156 001 001 000 008             ; set read mode audio
156 001 002                     ; service start
209 200                         ; delay 200 ms
401 Adjust betarget at 1 min for n=1 and n=2.
95                               ; beta
401 Reset main PCB with button.
    
```

10.8 Bandw.mcr

```

102                               ; tray open
401 Insert disc SBC444.
101                               ; tray close
156 001 001 000 008             ; set read mode audio
103                             ; start
105 1 0 0 100000                ; retrieve 1 min
192                             ; adjust foc and rad gain
    
```

02/12/97



		Electrical Adjustments CDM3600 Version 3.0 printed: 10/19/98		-		97/13/05
				3104 147 0137 0		97/09/15
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11. Appendix 2, EEPROM contents.

eprom_v53.txt

eprom_v54.txt

NOTE: 'A' means needs adjusting, value is deck dependent.

'V' means variabel, value depends of adjustment (date /station)

PAGE 0

• Bank 0

default values (hex)

EEPROM_VERSION	0x00	53		/ 54	
EEPROM_YEAR	0x01	96	V	/ 97	V
EEPROM_WEEK	0x02	47	V	/ 09	V
EEPROM_DAY	0x03	01	V	/ 02	V
EEPROM_LOADER_NO_MSB	0x04	00	V		
EEPROM_LOADER_NO_LSB	0x05	00	V		
EEPROM_LOADER_INSPECT_STATUS	0x06	00	V		
EEPROM_CDM_INSPECT_STATION	0x07	00	V		
	0x08	FF			
	0x09	FF			
	0x0A	FF			
	0x0B	FF			
	0x0C	FF			
EEPROM_DEBUG_FLAGS	0x0D	00			
EEPROM_LAST_PAGE	0x0E	01			
checksum	0x0F				

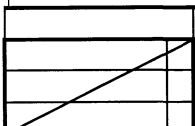
• Bank 1

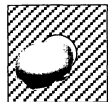
⇒ SRINIT

EEPROM_REN_OFFSET	0x10	00			
EEPROM_REN_GAIN	0x11	D0			
EEPROM_TLN_OFFSET	0x12	06			
EEPROM_DAC8_INIT_CAGAIN	0x13	6E			
EEPROM_DAC1_READ_POWER_0_7_MW	0x14	00	A		
EEPROM_DAC6_BALANCE_ELEC_MIN	0x15	7F	A		
EEPROM_DAC6_BALANCE	0x16	7F	A		
EEPROM_DAC5_TLN_OFFSET	0x17	7F	A		
EEPROM_DAC2_DELTA_P_20PRC	0x18	FF	A		
EEPROM_DAC2_DELTA_P_0	0x19	FF	A		
EEPROM_DAC2_DELTA_P_10PRC	0x1A	FF	A		
EEPROM_DAC2_DELTA_P_30PRC	0x1B	FF	A		
EEPROM_DAC3_INIT_CAIN	0x1C	B9			
EEPROM_DA_1_OFFSET_FOC_OFF	0x1D	45			
EEPROM_DA_1_OFFSET_FOC_ON	0x1E	45			
checksum	0x1F				

• Bank 2

EEPROM_N1_BETARGET	0x20	7F	A		
EEPROM_N1_DAC1_READ_POWER	0x21	40	A		
EEPROM_N1_DAC8_READ_CAGAIN	0x22	6E			
EEPROM_N1_DAC11_WRITE_COARSE	0x23	FF			
EEPROM_N1_DAC12_WRITE_FINE	0x24	FF	A		
EEPROM_N1_DAC3_CAIN	0x25	B9			
	0x26	FF			
⇒ SFCOEF1 for N=1(seperate for CDE)					
EEPROM_N1_CDE_FOC_GAIN	0x27	35	A	/ 27	A

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Date: 97/13/05				© N.V. PHILIPS ELECTRONICS	
				A4	



⇒ SFCOEF1 for N=1

EEPROM_N1_FOC_PARM3	0x28	2D			
EEPROM_N1_FOC_INT	0x29	01			
EEPROM_N1_RAMP_INCR	0x2A	14			
EEPROM_N1_RAMP_HEIGHT	0x2B	22			
EEPROM_N1_RAMP_OFFSET	0x2C	00			
EEPROM_N1_FE_START	0x2D	15			
EEPROM_N1_FOC_GAIN	0x2E	42	A	/ 38	A
checksum	0x2F				

• Bank 3

⇒ SFCOEF2 for N=1

EEPROM_N1_RAD_PARM_INIT		0x30	59		
EEPROM_N1_RAD_PARM_JUMP	0x31	4B			
EEPROM_N1_VEL_PARM2	0x32	12			
EEPROM_N1_VEL_PARM1	0x33	E8			
EEPROM_N1_FOC_PARM1	0x34	1D			
EEPROM_N1_FOC_PARM2	0x35	3F			
EEPROM_N1_MIR_DROP	0x36	10			

⇒ SRCOEF for N=1

EEPROM_N1_RAD_LENHT_LEAD	0x37	90			
EEPROM_N1_RAD_INT	0x38	18			
EEPROM_N1_RAD_PARM_PLAY	0x39	5C			
EEPROM_N1_RAD_POLE_NOISE	0x3A	1F			
EEPROM_N1_RAD_GAIN	0x3B	70	A	/ 69	A
EEPROM_N1_SLEDGE_PARM2	0x3C	14			
EEPROM_N1_SLEDGE_PARM1	0x3D	00			
EEPROM_N1_EXCENTR_FILTER_COEF	0x3E	06			
checksum	0x3F				

• Bank 4

EEPROM_N2_BETARGET	0x40	8F	A		
EEPROM_N2_DAC1_READ_POWER	0x41	40	A		
EEPROM_N2_DAC8_READ_CAGAIN	0x42	6E			
EEPROM_N2_DAC11_WRITE_COARSE	0x43	FF	A		
EEPROM_N2_DAC12_WRITE_FINE	0x44	FF	A		
EEPROM_N2_DAC3_CAIN	0x45	B9			
	0x46	FF			

⇒ SFCOEF1 for N=2 (seperate for CDE)

EEPROM_N2_CDE_FOC_GAIN	0x47	35	A	/ 27	A
------------------------	------	----	---	------	---

⇒ SFCOEF1 for N=2

EEPROM_N2_FOC_PARM3	0x48	2D			
EEPROM_N2_FOC_INT	0x49	01			
EEPROM_N2_RAMP_INCR	0x4A	14			
EEPROM_N2_RAMP_HEIGHT	0x4B	22			
EEPROM_N2_RAMP_OFFSET	0x4C	00			
EEPROM_N2_FE_START	0x4D	15			
EEPROM_N2_FOC_GAIN	0x4E	42	A	/ 38	A
checksum	0x4F				

• Bank 5

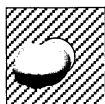
⇒ SFCOEF2 for N=2

EEPROM_N2_RAD_PARM_INIT		0x50	42		
EEPROM_N2_RAD_PARM_JUMP	0x51	4B			
EEPROM_N2_VEL_PARM2	0x52	12			
EEPROM_N2_VEL_PARM1	0x53	EF			
EEPROM_N2_FOC_PARM1	0x54	1D			
EEPROM_N2_FOC_PARM2	0x55	3F			
EEPROM_N2_MIR_DROP	0x56	10			

SRCOEFforN=2

EEPROM_N2_RAD_LENHT_LEAD	0x57	90			
EEPROM_N2_RAD_INT	0x58	18			
EEPROM_N2_RAD_PARM_PLAY	0x59	5C			

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EEPROM_N2_RAD_POLE_NOISE 0x5A 1F
 EEPROM_N2_RAD_GAIN 0x5B 70 A / 6F A
 EEPROM_N2_SLEDGE_PARM2 0x5C 32
 EEPROM_N2_SLEDGE_PARM1 0x5D 00
 EEPROM_N2_EXCENETR_FILTER_COEF 0x5E 06
 checksum 0x5F

• Bank 6

EEPROM_N6_BETARGET 0x60 00
 EEPROM_N6_DAC1_READ_POWER 0x61 40 A
 EEPROM_N6_DAC8_READ_CAGAIN 0x62 A0
 EEPROM_N6_DAC11_WRITE_COARSE 0x63 FF
 EEPROM_N6_DAC12_WRITE_FINE 0x64 FF
 EEPROM_N6_DAC3_CAIN 0x65 B9
 0x66 FF

⇒ SFCOEF1 for N=2 (seperate for CDE)

EEPROM_N6_CDE_FOC_GAIN 0x67 1E A / 17 A

⇒ SFCOEF1 for N=6

EEPROM_N6_FOC_PARM3 0x68 AD
 EEPROM_N6_FOC_INT 0x69 02
 EEPROM_N6_RAMP_INCR 0x6A 07
 EEPROM_N6_RAMP_HEIGHT 0x6B 13
 EEPROM_N6_RAMP_OFFSET 0x6C 00
 EEPROM_N6_FE_START 0x6D 15
 EEPROM_N6_FOC_GAIN 0x6E 26 A / 20 A
 checksum 0x6F

• Bank7

⇒ SFCOEF2 for N=6

EEPROM_N6_RAD_PARM_INIT 0x70 4F
 EEPROM_N6_RAD_PARM_JUMP 0x71 4B
 EEPROM_N6_VEL_PARM2 0x72 12
 EEPROM_N6_VEL_PARM1 0x73 AF
 EEPROM_N6_FOC_PARM1 0x74 19
 EEPROM_N6_FOC_PARM2 0x75 3F
 EEPROM_N6_MIR_DROP 0x76 10

⇒ SRCOEF for N=6

EEPROM_N6_RAD LENGHT_LEAD 0x77 60
 EEPROM_N6_RAD_INT 0x78 10
 EEPROM_N6_RAD_PARM_PLAY 0x79 4C
 EEPROM_N6_RAD_POLE_NOISE 0x7A 1F
 EEPROM_N6_RAD_GAIN 0x7B 41 A / 38 A
 EEPROM_N6_SLEDGE_PARM2 0x7C 55
 EEPROM_N6_SLEDGE_PARM1 0x7D 00
 EEPROM_N6_EXCENETR_FILTER_COEF 0x7E 06
 checksum 0x7F

• Bank 8

⇒ main motor processor settings

EEPROM_CURRENT_LIMIT 0x80 73
 EEPROM_LOOP_SELECT 0x81 84
 EEPROM_POLE_PAIRS 0x82 06
 EEPROM_EFM_PARM 0x83 0D
 EEPROM_F_TRESH 0x84 14
 0x85 08

EEPROM_T8_12 0x86 20
 EEPROM_EFM_GAIN_8 0x87 82
 EEPROM_EFM_GAIN_12 0x88 03

0x89 FF
 0x8A FF
 0x8B FF
 0x8C FF

EEPROM_ADJUSTMENT_STATION 0x8D 00 V
 EEPROM_LOADER_INSPECT_STATION 0x8E 00 V

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										Electrical Adjustments CDM3600										3104 147 0137 0																				97/09/15																													
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Version 3.0 printed: 10/19/98																																																																					
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EEPROM_CDE_PMAX_PERCENT	0xF4	78
EEPROM_CDE_FS_ERASE_PERCENT	0xF5	78
EEPROM_CDR_MMIN	0xF6	32
EEPROM_OPC_CDE_FS_LOW_PERCENT	0xF7	3C
EEPROM_OPC_CDE_FS_HIGH_PERCENT	0xF8	78
EEPROM_OPC_FS_LOW_PERCENT	0xF9	3C
EEPROM_OPC_FS_HIGH_PERCENT	0xFA	82
EEPROM_OPC_PMIN_PERCENT	0xFB	32
EEPROM_OPC_PMAX_PERCENT	0xFC	96
EEPROM_OPC_FS_COUNT	0xFD	C8
	0xFE	FF
checksum	0xFF	

PAGE 1

• Bank 0

default values (hex)

EEPROM_UPL_CDRW_N1_WR_HR_MSB	0x100	00
EEPROM_UPL_CDRW_N1_WR_HR_LSB	0x101	00
EEPROM_UPL_CDRW_N1_WR_MIN	0x102	00
EEPROM_UPL_CDRW_N1_WR_SEC	0x103	00
EEPROM_UPL_CDRW_N2_WR_HR_MSB	0x104	00
EEPROM_UPL_CDRW_N2_WR_HR_LSB	0x105	00
EEPROM_UPL_CDRW_N2_WR_MIN	0x106	00
EEPROM_UPL_CDRW_N2_WR_SEC	0x107	00
EEPROM_UPL_CDRW_N4_WR_HR_MSB	0x108	00
EEPROM_UPL_CDRW_N4_WR_HR_LSB	0x109	00
EEPROM_UPL_CDRW_N4_WR_MIN	0x10A	00
EEPROM_UPL_CDRW_N4_WR_SEC	0x10B	00
	0x10C	FF
	0x10D	FF
	0x10E	FF
checksum	0x10F	

• Bank 1

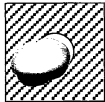
EEPROM_UPL_CDR_N1_WR_HR_MSB	0x110	00
EEPROM_UPL_CDR_N1_WR_HR_LSB	0x111	00
EEPROM_UPL_CDR_N1_WR_MIN	0x112	00
EEPROM_UPL_CDR_N1_WR_SEC	0x113	00
EEPROM_UPL_CDR_N2_WR_HR_MSB	0x114	00
EEPROM_UPL_CDR_N2_WR_HR_LSB	0x115	00
EEPROM_UPL_CDR_N2_WR_MIN	0x116	00
EEPROM_UPL_CDR_N2_WR_SEC	0x117	00
EEPROM_UPL_CDR_N4_WR_HR_MSB	0x118	00
EEPROM_UPL_CDR_N4_WR_HR_LSB	0x119	00
EEPROM_UPL_CDR_N4_WR_MIN	0x11A	00
EEPROM_UPL_CDR_N4_WR_SEC	0x11B	00
	0x11C	FF
	0x11D	FF
	0x11E	FF
Checksum	0x11F	

• Bank 2

EEPROM_UPL_N1_RD_HR_MSB	0x120	00	
EEPROM_UPL_N1_RD_HR_LSB		0x121	00
EEPROM_UPL_N1_RD_MIN	0x122	00	
EEPROM_UPL_N1_RD_SEC	0x123	00	
EEPROM_UPL_N2_RD_HR_MSB	0x124	00	
EEPROM_UPL_N2_RD_HR_LSB	0x125	00	
EEPROM_UPL_N2_RD_HR_MIN	0x126	00	
EEPROM_UPL_N2_RD_HR_SEC	0x127	00	
EEPROM_UPL_N6_RD_HR_MSB	0x128	00	
EEPROM_UPL_N6_RD_HR_LSB	0x129	00	
EEPROM_UPL_N6_RD_MIN	0x12A	00	
EEPROM_UPL_N6_RD_SEC	0x12B	00	
	0x12C	FF	
	0x12D	FF	

				Electrical Adjustments CDM3600				-		97/13/05					
										97/09/15					
				3104 147 0137 0		97/12/02									
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checksum 0x12E FF
0x12F

• Bank3

0x130 FF
0x131 FF
0x132 FF
0x133 FF
0x134 FF
0x135 FF
0x136 FF
0x137 FF
0x138 FF
0x139 FF
0x13A FF
0x13B FF
0x13C FF
0x13D FF
0x13E FF
0x13F

checksum

• Bank4

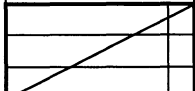
0x140 FF
0x141 FF
0x142 FF
0x143 FF
0x144 FF
0x145 FF
0x146 FF
0x147 FF
0x148 FF
0x149 FF
0x14A FF
0x14B FF
0x14C FF
0x14D FF
0x14E FF
0x14F

checksum

						-		97/13/05	
								97/09/15	
						3104 147 0137 0		97/12/02	
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		Date: 97/13/05						A4	
								© N.V. PHILIPS ELECTRONICS	

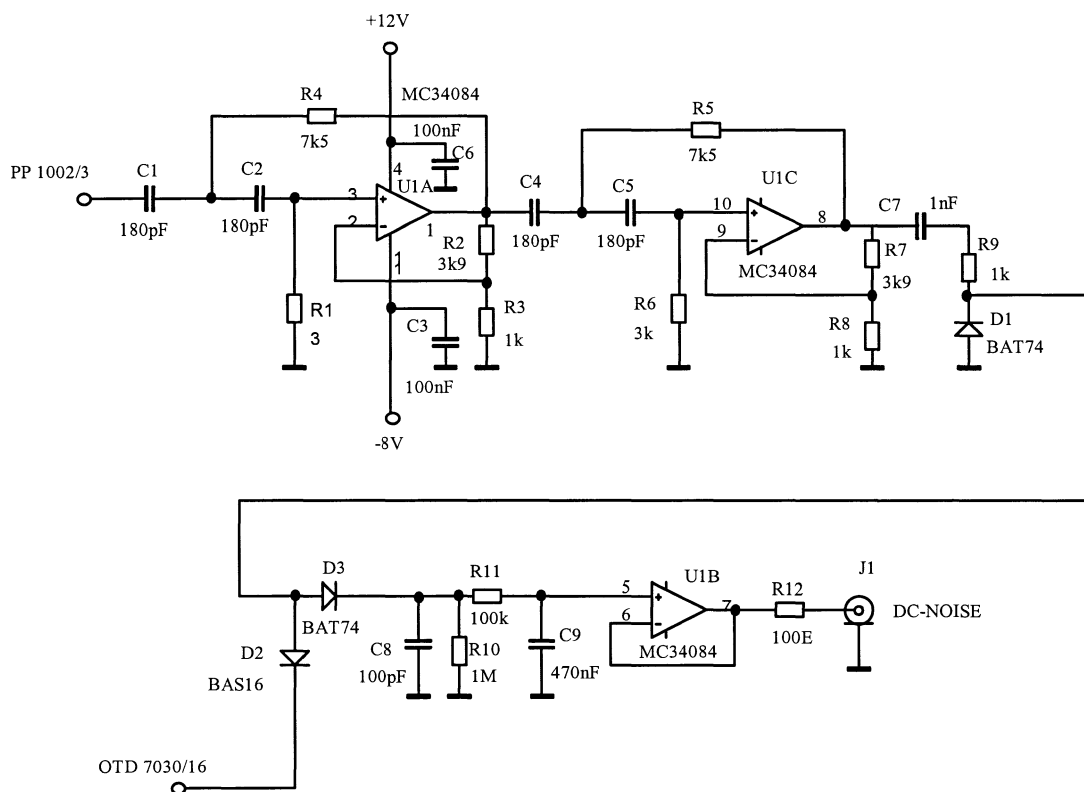
12. Appendix 3, DAC.

	Address	DAC
DAC_READ_POWER	0x08	AD01
DAC_DELTA_P	0x04	AD02
DAC_P_ERASE	0x04	AD02
DAC_BARON	0x2C	AD03
DAC_CAIN	0x0F	AD03
DAC_FS0	0x02	AD04
DAC_TLN_OFFSET	0x0A	AD05
DAC_BALANCE	0x06	AD06
DAC_ALPHA0	0x0E	AD07
DAC_CAGAIN	0x01	AD08
DAC_N2	0x19	AD09
DAC_PMAX	0x0B	AD09
DAC_PMIN	0x07	AD10
DAC_ALON	0x25	AD10
DAC_WRITE_COARSE	0x0D	AD11
DAC_WRITE_FINE	0x03	AD12
DAC_DC_ERASE	0x40	AD00
DAC_CDE	0x80	AD00

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13. Appendix 4, DC-noise circuit.



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