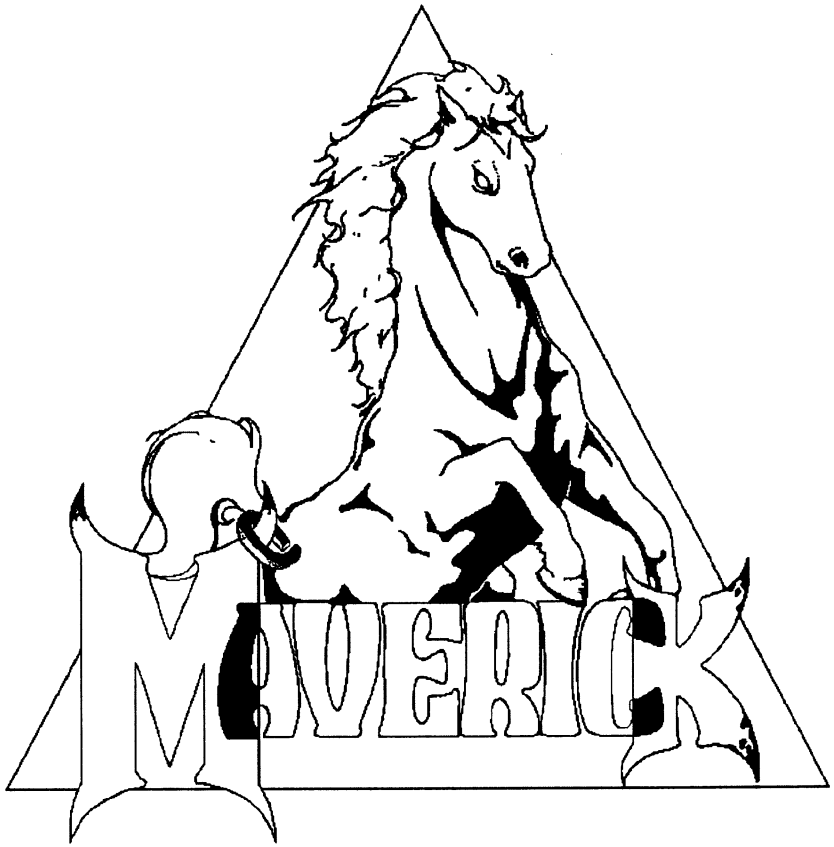
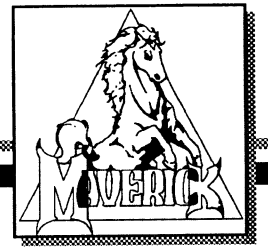
Maverick 270/540 AT
Training
Prepared for Compaq

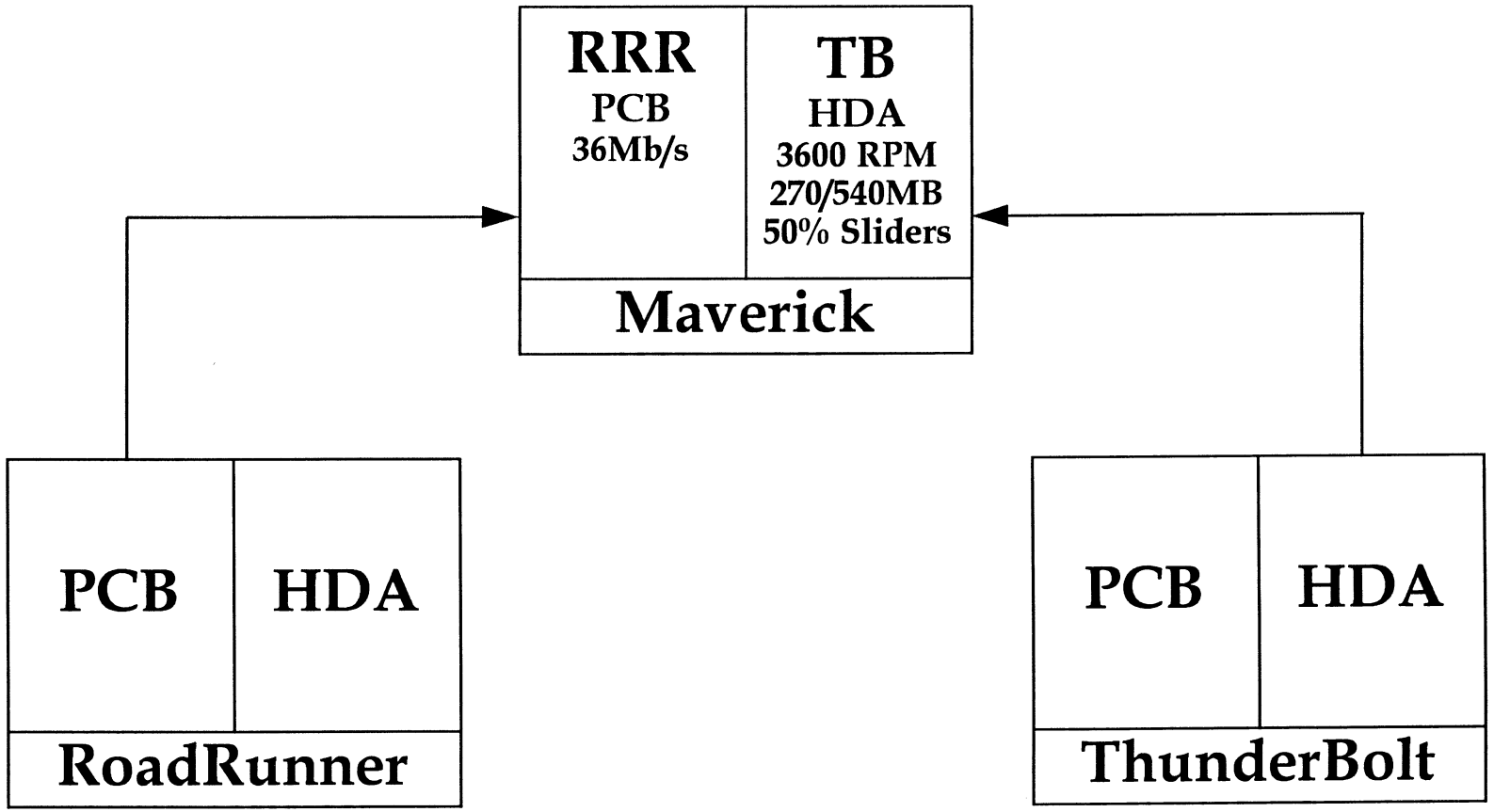


AGENDA

- PROGRAM OVERVIEW --- MIKE HENNINGS
- ELECTRICAL --- TOM HUGUNIN
- FIRMWARE --- BOB MOORE



Maverick Product Leverage



Drive Configuration - Electronic

Changes From RoadRunner PCB

- Read Channel - Ryan II → Inu Tested to 36 Mb/s
- Synthesizer - Sakana II → Sakana Tested to 54 MHz
- 8011 Read Filter → 8012 Read Filter
- ECL Preamp → Hitachi or VTC TTL
- PCB Fab → > 96 % RoadRunner

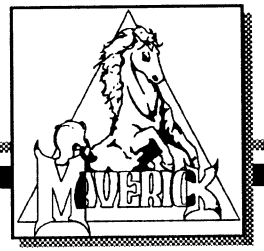
- Form Factor → Ryan 44 PQFP Package
  → 3.9 mm Jumpers
  → TB I/F Connector

Drive Configuration - Firmware

Changes From RoadRunner Code

- RoadRunner code
  - No Changes in Features, Functions, Test Process, Host Interface, etc.
  - Capacity or Yield Related Changes Only

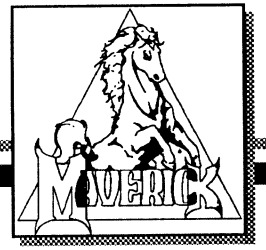
- Leveraged Customer Qualifications
  - If a Customer Qualifies RoadRunner Code, Maverick Code is Qualified



Drive Configuration - HDA

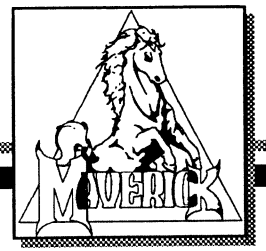
Changes from ThunderBolt HDA

■ 3600 RPM Spindle Motor	→	Lower Data Rate/ Lower Power
■ 7 Gram Load w/Modified Rails	→	Proper Fly Height at New RPM
■ 50% Sliders	→	Increased Data Stroke
■ New OD Crash Stop	→	More Tracks / Lowers FCI
■ One Side VCM Magnets	→	Reduced Seek Spec
■ Redesigned Flex Circuit w/New Preamp	→	Interface RRR PCB to TB HDA
■ Add RRR PCB Mounting Holes	→	Interface RRR PCB to TB HDA
■ Slots in Base for Push Pin Servowriter	→	Servowrite w/Cover On
■ Machined Surface on E-Block	→	Reliable Push Pin Contact

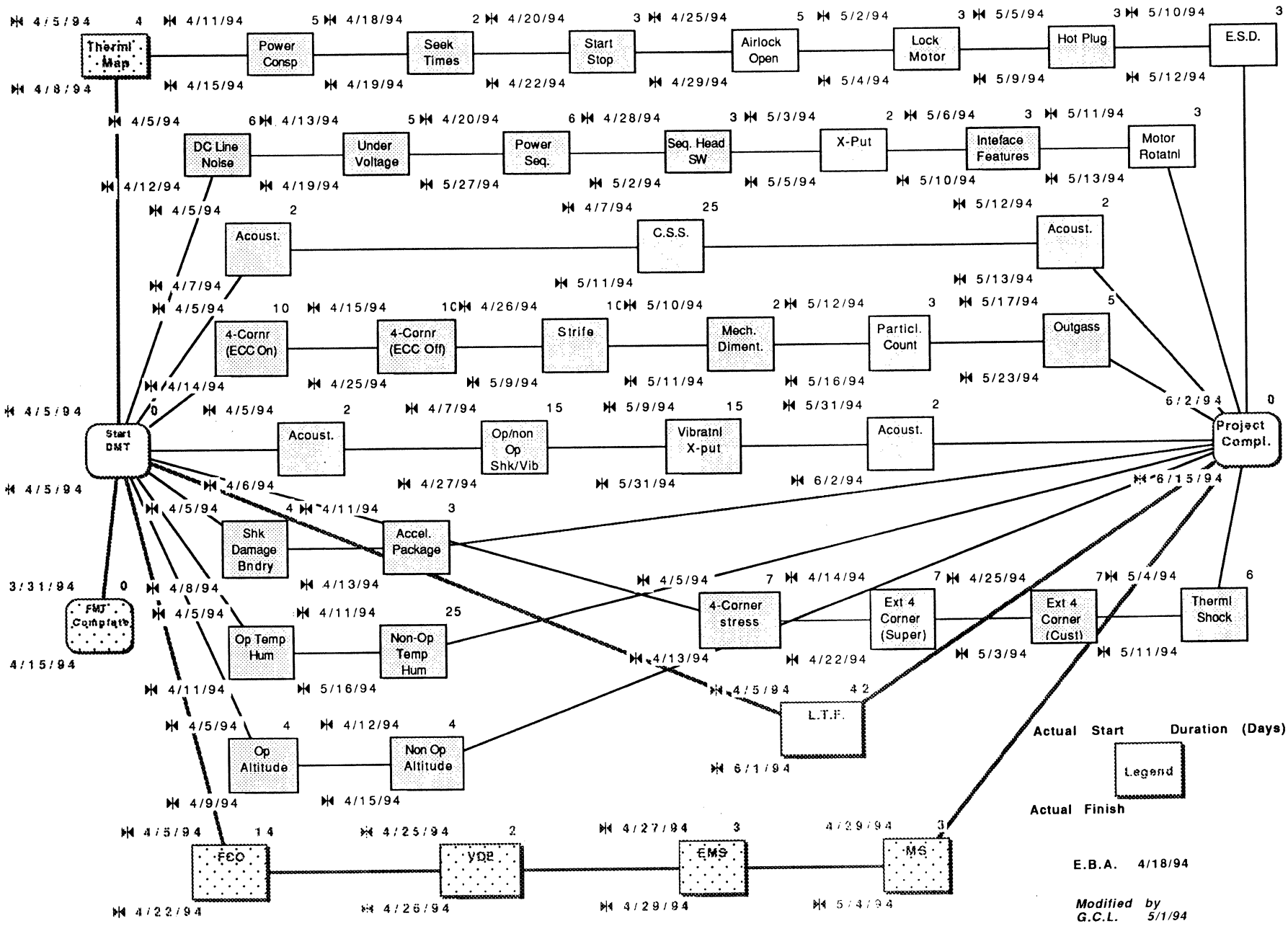


Program Status

- Maverick AT Mass Production Began 5/31
  - 2500 units/day @ >90% yield
- DMT Testing Complete
- Compatibility Testing in Progress



Maverick AT/SCSI Qualification Test Pert



Compatibility Test Engineering
Maverick Testing for Compaq

- **Pre-Mass Pro Drives now being tested.**
  - CTE startedtesting with earliest versions through PMP.
  - Approximately 40 drives in Compatibility test.

- **Two ROM versions being tested concurrently.**
  - Both ROM codes 5 and 6 are in the test matrix.
    - » ROM 5 & FW A05.0505 matrix is nearly complete.
    - » ROM 6 & FW A06.0506 is approx 40% through the full Compaq matrix.

- **New Tests from Compaq have been incorporated.**
  - Compaq FixedTest
  - DOS62.BAT

- **"Smoothest new product testing we've ever had"**

Quantum

Compatibility Test Engineering
Maverick Testing for Compaq

Next on the Test Plan

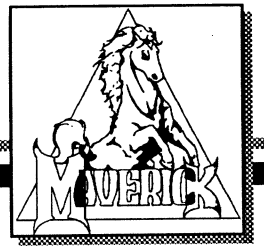
- **Complete the Compatibility Matrix**
  - **Benchmarks (AUTOBENCH)**
  - **Diagnostics**
- **Network Testing**
  - **Novell Netware 3.12 and 4.01**
- **Features Testing**
  - **Power Management**
  - **DMA**

Quantum

MAVERICK

ELECTRICAL

Presentor: Tom Hugunin



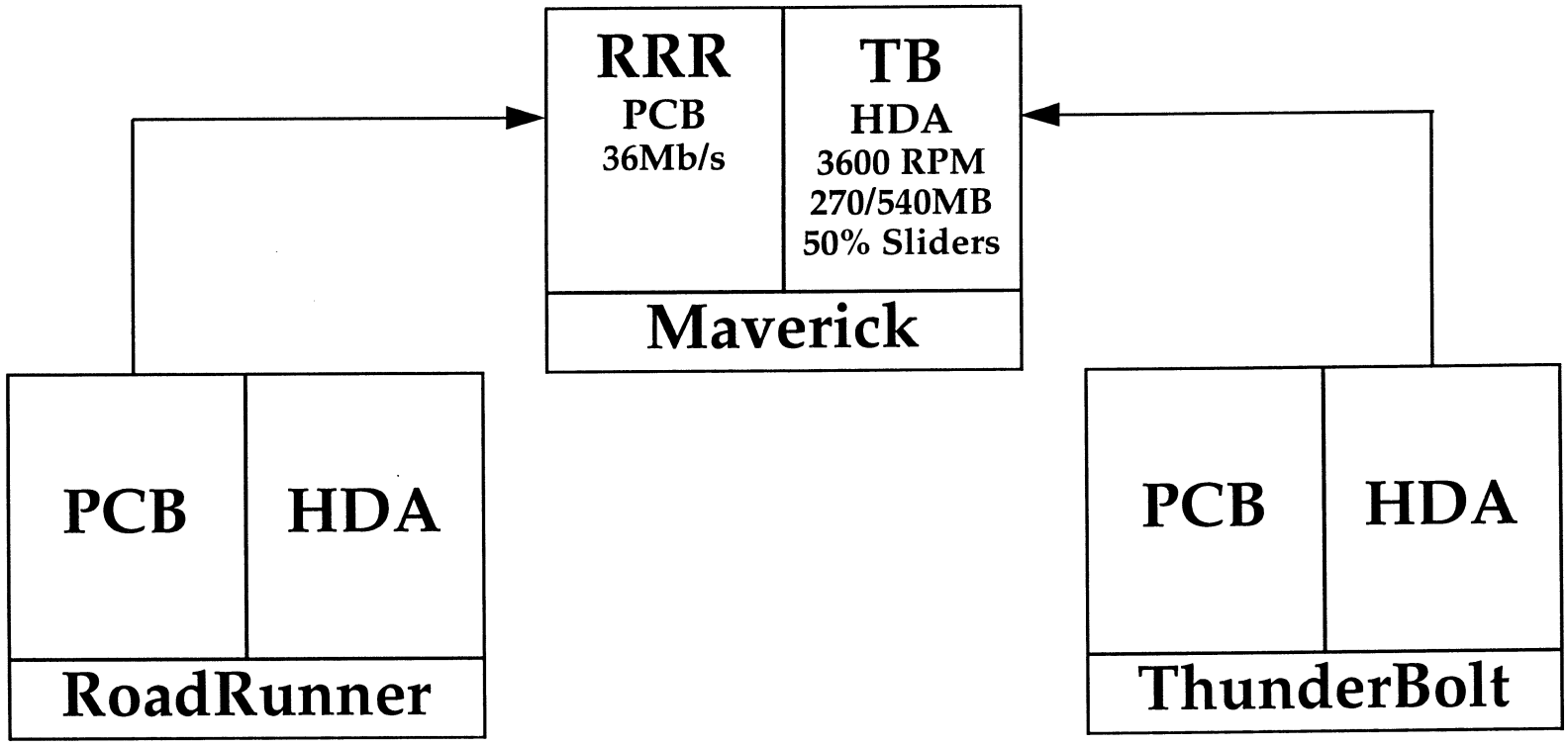
Maverick 270/540

For Compaq Computer

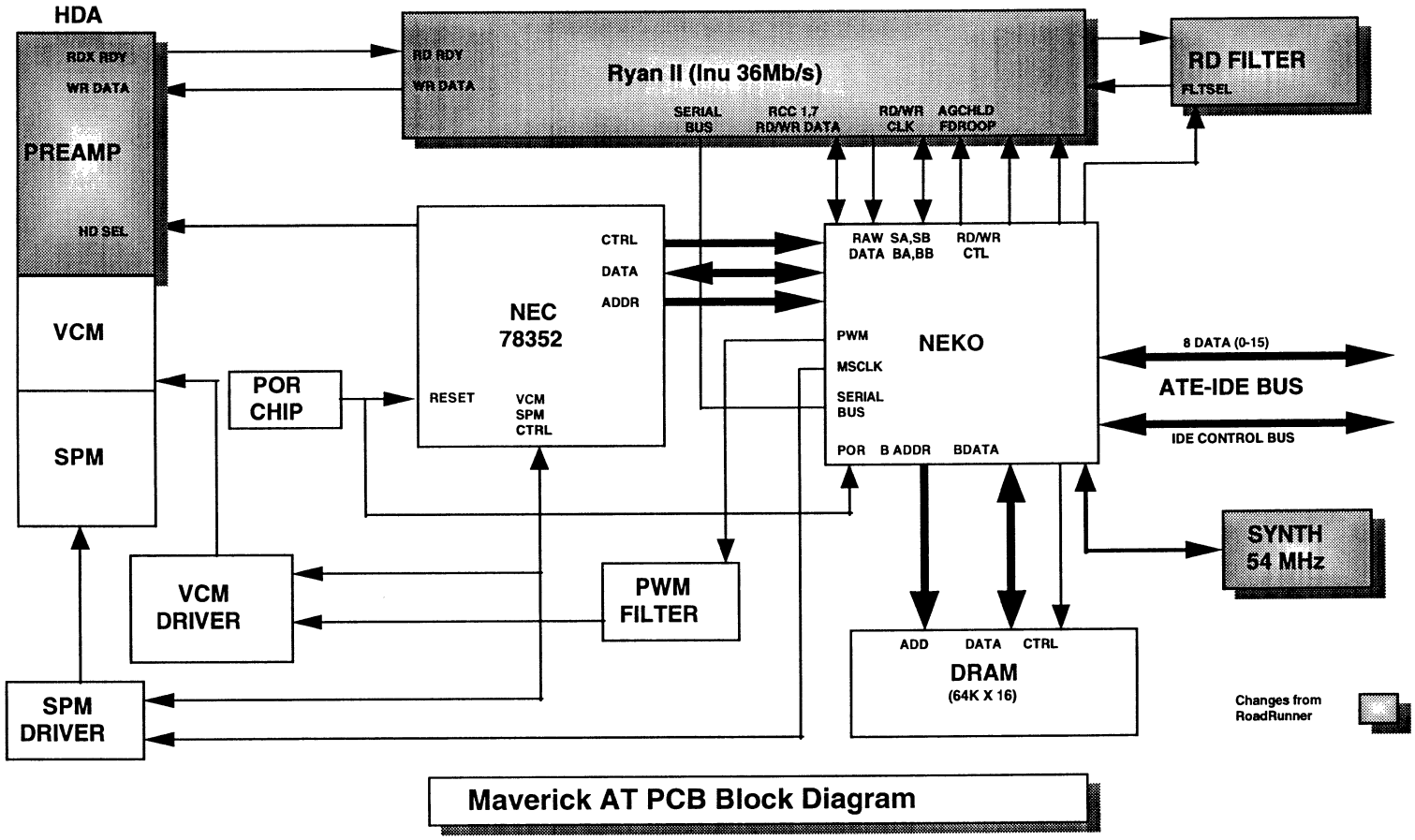
By Tom Hugunin

DESIGN PHILOSOPHY

ROADRUNNER+THUNDERBOLT=MAVERICK



SYSTEM



Maverick AT PCB Block Diagram

SERVO-MECHANICAL

TPI	2950
TRACK PITCH	339 µin
USER CYLINDERS	2853
ROTATIONAL SPEED	3600 rpm
SERVO SAMPLES/REV	78
SERVO SAMPLE RATE	4.68 KHz
SERVO SAMPLE TIME	214 µs
SERVO BANDWIDTH	350 Hz
AVERAGE SEEK TIME	14 ms

SERVO MECHANICAL

COIL RESISTANCE	**16.2 Ω**
HEAD RADIUS	**5.98 cm**
INERTIA 1 DISK	**50 g-cm^2**
INERTIA 2 DISK	**60 g-cm^2**
K_{torque} 1 DISK	**712 g-cm/amp**
K_{torque} 2 DISK	**787 g-cm/amp**

SERVO ARCHITECTURE

EMBEDDED SERVO

DIGITAL COMPENSATION SYSTEM

ESTIMATOR BASED SEEK SYSTEM

DIGITAL PID BASED TRACK FOLLOW

SERVO RECAL

Initialize servo parameters to defaults.

Start Spindle.

Wait for spindle to reach 3600 rpm.

Unpark actuator.

Map all heads.

Calibrate course head gains.

Lock onto track.

Calibrate fine head gains.

Calibrate torque bias.

SERVO RECAL

Calibrate seek velocity.

Seek to track zero.

SERVO WRITE UNSAFE CRITERIA

2 Bad syncs or SAM's in a row.

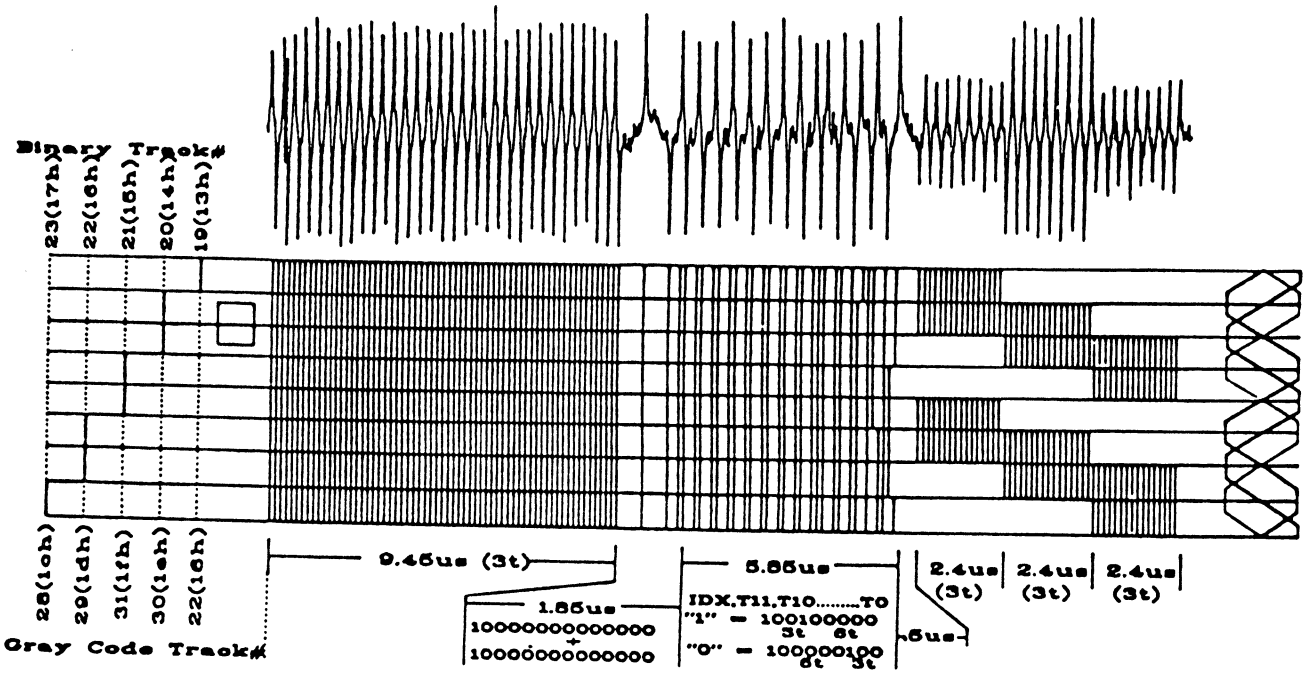
2 Track ID errors in a row.

Bumped Wedge ≥ 10%

Defect Wedge ≥ 40 %

Out of speed error ≥ 0.3%

SERVO WEDGE



AGC/SYNC SAM GREY A B C

READ WRITE ARCHITECTURE

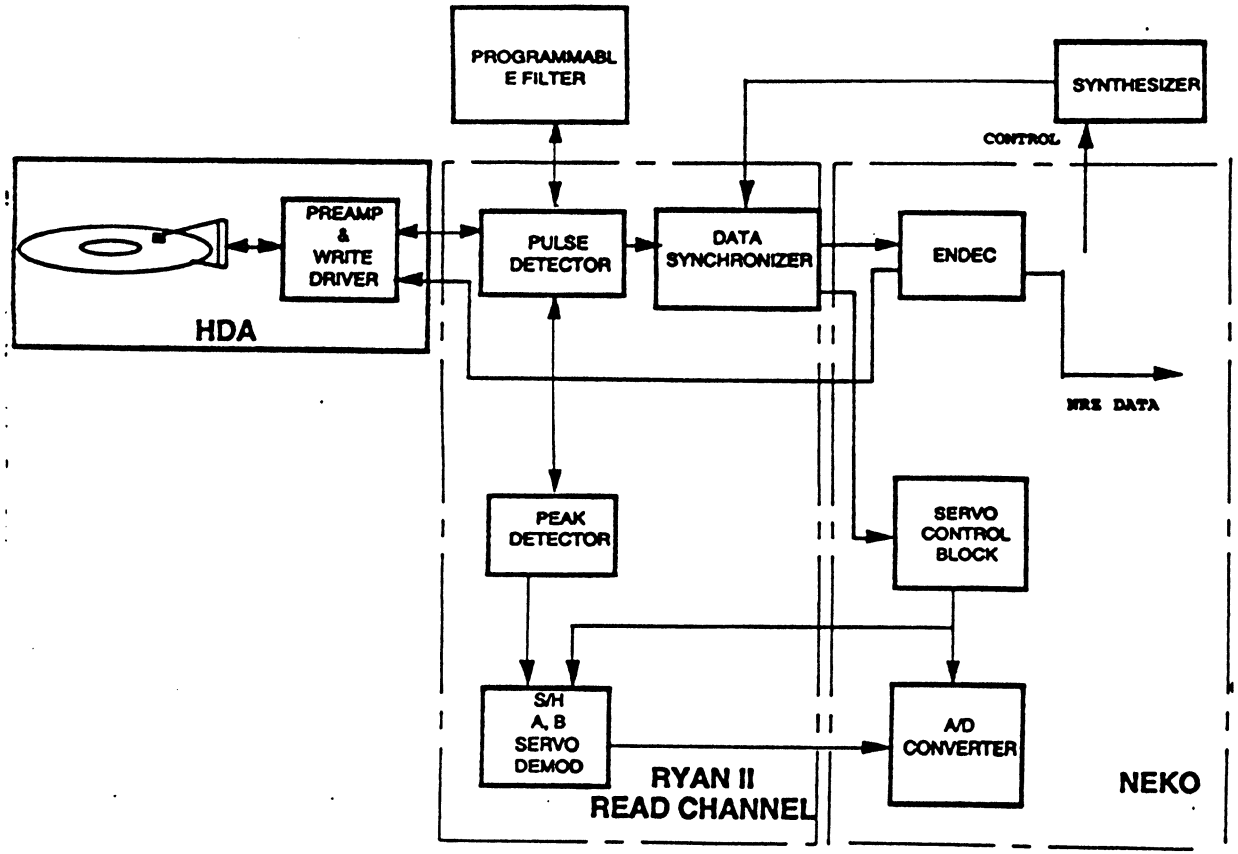
ZONE DENSITY RECORDING

PROGRAMMABLE EQUALIZATION

ECC ON THE FLY ERROR CORRECTION

ID AFTER WEDGE FORMAT

READ WRITE


PROGRAMMABL
E FILTER
SYNTHESIZER
CONTROL
PREAMP
&
WRITE
DRIVER
PULSE
DETECTOR
DATA
SYNCHRONIZER
ENDEC
HDA
NRZ DATA
PEAK
DETECTOR
SERVO
CONTROL
BLOCK
S/H
A, B
SERVO
DEMOD
A/D
CONVERTER
RYAN II
READ CHANNEL
NEKO

READ WRITE

HEADS	**THIN FILM**
SLIDERS	**50 %**
ENCODING SCHEME	**1,7 RLL**
MAXIMUM DATA RATE	**36.08 Mb/S**

READ WRITE

MAVERICK 540 TRACK LAYOUT

16 zones - ID after Wedge

Last Rev:	2/16/94 3:29 PM
Req Cap	541.4994 Million Bytes
Spare	2 per cyl
Surfaces	4
Rod	1.7992 "
Rid	0.8301 "
Stroke	0.9691 "
RPM	3599.54 rpm
Trot	16666.800 uSec
Frot	59.9923 Hz
TPI	2950.0
Tot. tracks	2858
Trks/zone	166
max. FCI	45594
% of req.	100.01%
Total Cap	541.5721 Million bytes
User sectors	1057758

	Bytes	uSec
ID Sync	9	
ID AM	2	
ID Data	6	
ID CRC	3	
ID Pad	3	
Total	23	
Data bytes	512	
Data Sync	13	
Data AM	2	
Data ECC	14	
Data Pad	3	
Tot. bytes	544	
Split ovhd	18	
AGC/Wiggle Gap	3	1.29 max.

Srv Fq	26.653869 MHz	
Srv Clk	37.518005 nSec	
Srv T	1.801 uSec	(Pre & Post gaps)
Srv N	417 Clocks	(Total of fields other than gaps)
Nservos	78 samples	
Tservo	17.446006 uSec	(includes pre & post gaps)
Tdata	196.250 uSec	
Servo sample freq =	4679.4011 Hz	Srv OH 8.16%
Wedge-to-Wedge time =	213.7026 µs	Fmt OH 9.70%

	Pre & Post Gaps	AGC Time	Servo Sync	SAM	Index	Gray code (12 bits)	DC Erase	A,B&C Bursts (each)
µs	1.801	3.30158447	1.5007202	1.38817	0.337662	4.051945	0.337662048	1.575756225
Clks	48.00361807	88	40	37	9	108	9	42

Total Servo Burst length = 17.446 µs = 465.00362 T

Zone	Zone Rod	Zone Rid	Cyls	Max. FC/in.	Data Rate [Mb/s]	Fclk [MHz]	Fmax [MHz]	½Twindow [nS]	ID time [µs]	Sect. time [µs]	Sect/burst w/o split	Time left [µs]	Preamble & AM [µs]	Split Sect	Total Sect (incl. spares)	Zone Cap per surface
OD		1.7992														
System	1.7992	1.7972	5	32127	29.02	43.529	10.882	11.49	6.34	149.97	1	39.115	4.96	16	94	239360
0	1.7972	1.7294	200	41508	36.08	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	12032000
1	1.7294	1.6755	159	42843	36.08	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	9565440
2	1.6755	1.5948	238	45011	36.08	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	14318080
3	1.5948	1.5447	148	45083	35.00	52.500	13.125	9.52	5.26	124.34	1	65.964	4.11	38	114	8600576
4	1.5447	1.5013	128	45217	34.12	51.176	12.794	9.77	5.39	127.56	1	62.595	4.22	34	112	7307264
5	1.5013	1.4477	158	45273	32.94	49.412	12.353	10.12	5.59	132.11	1	57.821	4.37	30	108	8696320
6	1.4477	1.3840	188	45399	31.58	47.368	11.842	10.56	5.83	137.81	1	51.850	4.56	27	104	9962496
7	1.3840	1.3237	178	45095	30.00	45.000	11.250	11.11	6.13	145.07	1	44.250	4.80	20	97	8794624
8	1.3237	1.2599	188	45209	28.63	42.941	10.735	11.64	6.43	152.02	1	36.962	5.03	16	93	8903680
9	1.2599	1.1928	198	45594	27.33	41.000	10.250	12.20	6.73	159.22	1	29.421	5.27	11	88	8870400
10	1.1928	1.1393	158	45203	25.88	38.824	9.706	12.88	7.11	168.15	1	20.068	5.56	5	83	6673920
11	1.1393	1.0586	238	44963	23.92	35.882	8.971	13.93	7.69	181.93	1	6.627	6.02	-1	78	9443840
12	1.0586	1.0186	118	45580	23.33	35.000	8.750	14.29	7.89	186.61	1	0.821	6.17	-1	74	4440576
13	1.0186	0.9718	138	45044	22.00	33.000	8.250	15.15	8.36	197.82	0	186.795	6.55	71	89	4839936
14	0.9718	0.9115	178	45115	20.67	31.000	7.750	16.13	8.90	210.58	0	186.185	6.97	65	85	5878272
15	0.9115	0.8301	240	44743	18.67	28.000	7.000	17.86	9.86	233.14	0	185.107	7.71	59	58	7065600
ID	0.8301		2853													

Total cap =	541.5721
% of goal =	100.01%

Bytes/surface =	135393024
Bytes/disk =	270786048

READ WRITE

MAVERICK 270 TRACK LAYOUT

16 zones - ID after Wedge

Last Rev:	2/16/94	3:26 PM
Req Cap	270.748896 Million Bytes	lc270d.xls
Spare	1 per cyl	
Surfaces	2	
Rod	1.7992 "	
Rid	0.8301 "	
Stroke	0.9691 "	
RPM	3599.64 rpm	
Trot	16666.7666 uSec	
Frot	59.9923 Hz	
TPI	2950	
Tot. tracks	2953	5711
T#s/zone		
max. FCI	45594	
% of req.	100.01%	
Total Cap	270.7980 Million bytes	
User sectors	481879	

	Bytes	uSec
ID Sync	9	
ID AM	2	
ID Data	6	
ID CRC	3	
ID Pad	3	
Total	23	
Data bytes	512	
Data Sync	13	
Data AM	2	
Data ECC	14	
Data Pad	3	
Tot. bytes	544	
Split ovhd	18	
AGC/Wiggle Gap	3	1.29
		max.

Srv Fq	26.654 MHz	
Srv Clk	37.518 nSec	
Srv T	1.801 uSec	(Pre & Post gaps)
Srv N	417 Clocks	(Total of fields other than gaps)
Nservos	78 samples	
Tservo	17.446 uSec	(includes pre & post gaps)
Tdata	196.250 uSec	
Servo sample freq =	4679.4011 Hz	Srv OH 8.16%
Wedge-to-Wedge time =	213.7026 µs	Fmt OH 9.70%

	Pre & Post Gaps	AGC Time	Servo Sync	SAM	Index	Gray code (12 bits)	DC Erase	A,B&C Bursts (each)
µs	1.801	3.302	1.501	1.388	0.338	4.052	0.338	1.576
Clks	48	88	40	37	9	108	9	42

Total Servo Burst length = 17.446 µs = 465 T

Zone	Zone Rod	Zone Rid	START CYLINDER	Cyls	Max. FC/in.	Data Rate [Mb/s]	Fclk [MHz]	Fmax [MHz]	½Twindow [nS]	ID time [µs]	Sect. time [µs]	Sect/burst w/o split	Time left [µs]	Preamble & AM [µs]	Split Sect	Total Sect (incl. spares)	Zone Cap per surface
OD		1.7992															
System	1.7992	1.7972	-5	5	32127	29.02	43.529	10.882	11.49	6.34	149.97	1	39.115	4.86	16	93	236800
0	1.7972	1.7294	0	200	41506	36.06	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	12032000
1	1.7294	1.6755	200	159	42843	36.06	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	9565440
2	1.6755	1.5948	359	238	45011	36.06	54.118	13.529	9.24	5.10	120.63	1	69.859	3.99	42	118	14319080
3	1.5948	1.5447	597	148	45083	36.00	52.500	13.125	9.52	5.26	124.34	1	65.984	4.11	38	114	8600676
4	1.5447	1.5013	745	128	45217	34.12	51.178	12.794	9.77	5.39	127.56	1	62.596	4.22	34	112	7307264
5	1.5013	1.4477	873	158	45273	32.94	49.412	12.353	10.12	5.58	132.11	1	57.821	4.37	30	108	8696320
6	1.4477	1.3840	1,031	188	45399	31.58	47.368	11.842	10.56	5.83	137.81	1	51.850	4.56	27	104	9962496
7	1.3840	1.3237	1,219	178	45096	30.00	45.000	11.250	11.11	6.13	145.07	1	44.250	4.80	20	97	8794624
8	1.3237	1.2589	1,397	188	45209	28.63	42.941	10.736	11.64	6.43	152.02	1	36.962	5.03	16	93	8803680
9	1.2589	1.1928	1,585	198	45594	27.33	41.000	10.250	12.20	6.73	159.22	1	29.421	5.27	11	88	8870400
10	1.1928	1.1393	1,783	158	45203	25.88	38.824	9.706	12.88	7.11	168.15	1	20.068	5.56	5	83	6673920
11	1.1393	1.0586	1,941	238	44963	23.92	35.882	8.971	13.93	7.69	181.93	1	5.627	6.02	-1	78	8443840
12	1.0586	1.0186	2,179	118	45580	23.33	35.000	8.750	14.29	7.89	186.51	1	0.821	6.17	-1	74	4440576
13	1.0186	0.9718	2,297	138	45044	22.00	33.000	8.250	15.15	8.36	197.82	0	186.786	6.55	71	89	4839936
14	0.9718	0.9115	2,435	178	45115	20.67	31.000	7.750	16.13	8.90	210.58	0	186.186	6.97	65	85	5878272
15	0.9115	0.8301	2,613	240	44743	18.67	28.000	7.000	17.86	9.86	233.14	0	185.107	7.71	59	58	7065600
ID	0.8301		TOTAL	2953													

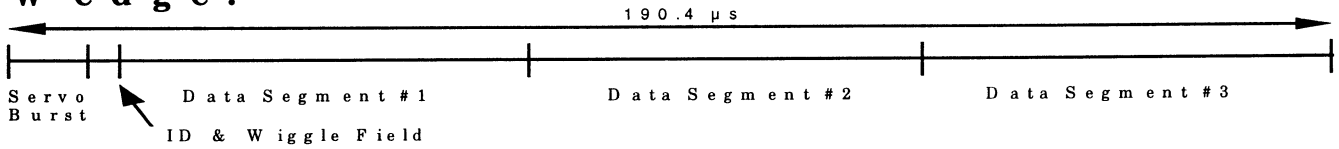
Total cap =	270.78805
% of goal =	100.01%

Bytes/surface =	135393024
Bytes/disk =	270786048

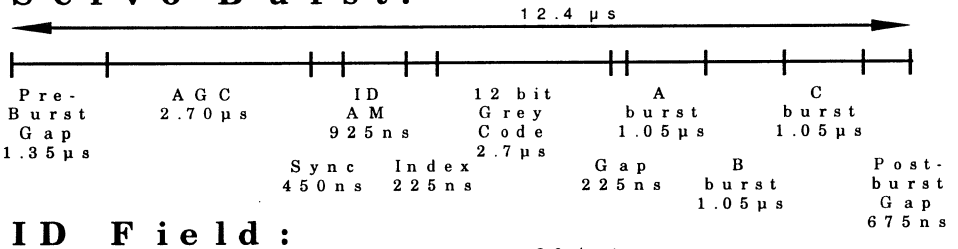
TRACK FORMAT

Maverick Track Format
ID-After-Wedge

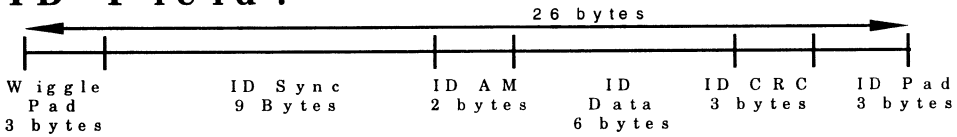
Wedge:



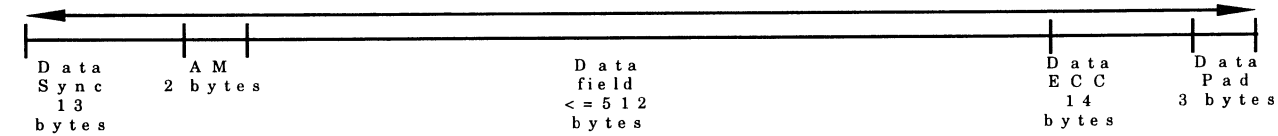
Servo Burst:



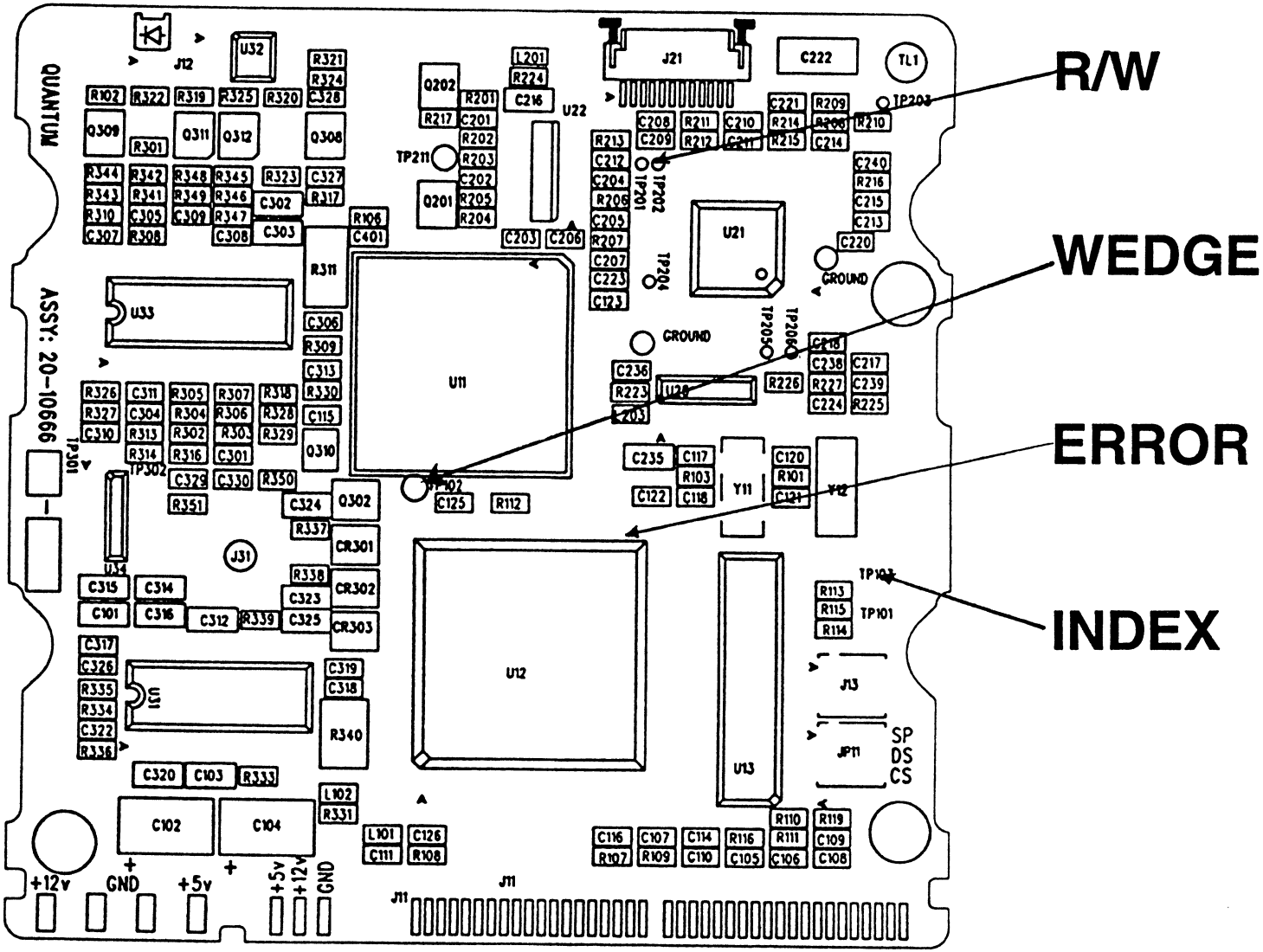
ID Field:



Data Segment:



TEST POINTS


R/W
WEDGE
ERROR
INDEX
QUANTUM
ASSY: 20-10666
GROUND
GROUND
+12v
GND
+5v
+5v
+12v
GND
SP
DS
CS

DIAG HINTS

DISABLING POWER SAVE MODE:

SUPER,SP 0,DEPB 0 48h,WRCONF 16

TURNING OFF READ AHEAD:

CACHE OFF

TRANSLATING LOGICAL TO PHYSICAL:

SUPER,CLBA

DISABLING RETRIES:

SP 0,ATRDCONF,RETRIES 0,ATWRCONF

ERROR TRIGGER

Config page 12 byte 0

7	6	5	4	3	2	1	0
Seq. Time-out	Seq. Data Error	Uncorr. Error	ECC Corr. Error	Wedge Error	Seek Fault	Seek Time-out	Servo Bump

Trigger Output is pin 34 of microprocessor.

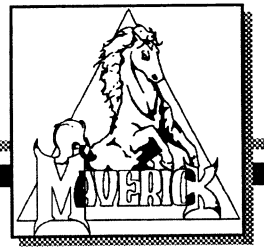
Diag command:

SUPER,SP 0,DEPB 0 020h,WRCONF 12

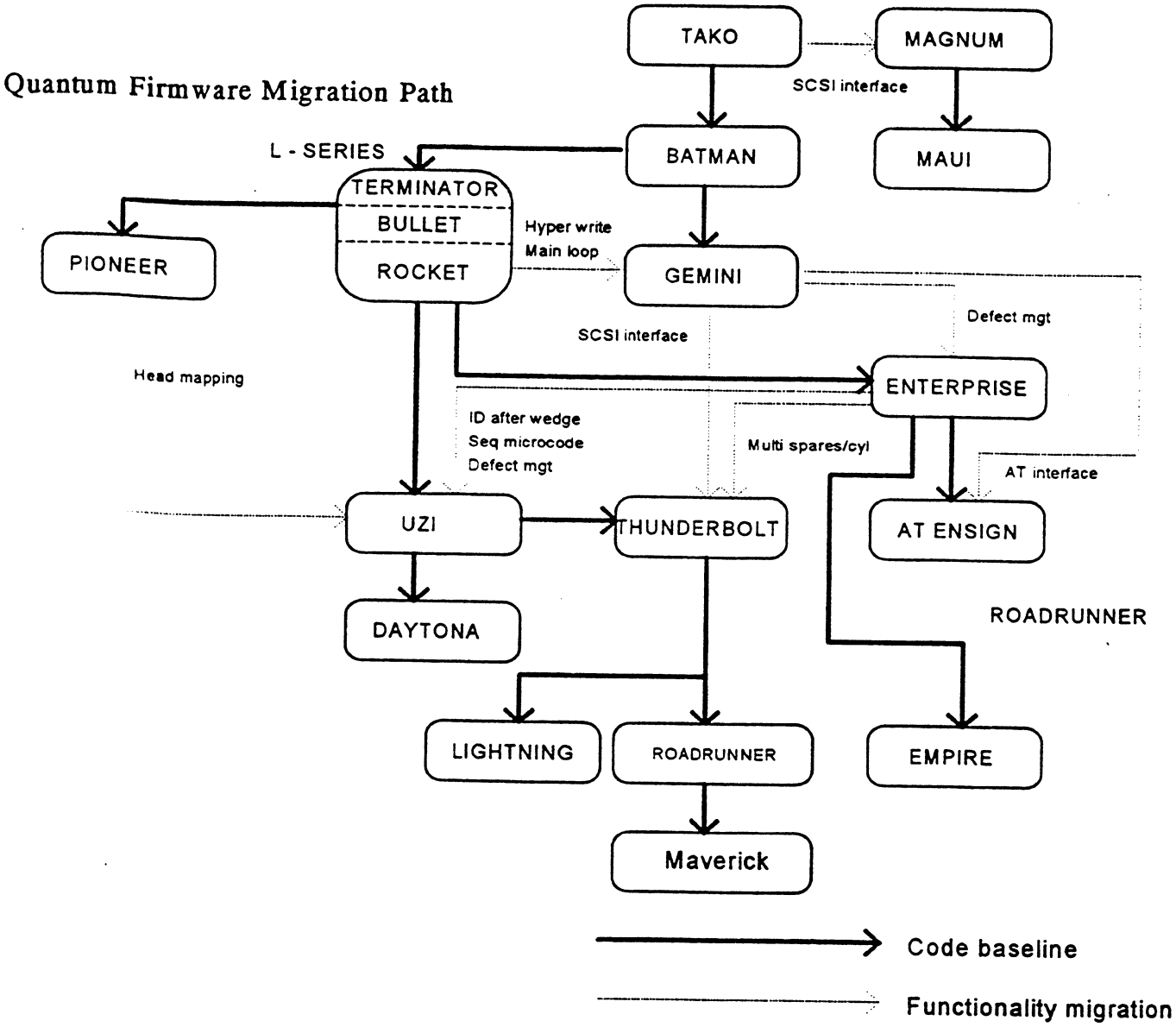
MAVERICK

FIRMWARE

Presentor: Bob Moore



Quantum Firmware Migration Path



Maverick PP2 Firmware

Differences from RoadRunner

Change	Reason	Implication
Wiggle recovery procedure. (In PP2 F/W)	RoadRunner used MIG head design on their HDA. Maverick HDA has thin film heads as used on the Thunderbolt HDA. Thin film heads known for "Barkhausen" noise phenomenon. Recovery procedure required for certain media related errors.	Possibly longer SelfScan time if test is added to determine head susceptibility to Barkhausen noise.
Geometry parameter changes (In PP1 F/W)	Different capacity. New TPI, maximum number of tracks, sectors per track, etc.	Needed for capacity.
LBA mode support. (In PP2 F/W)	2 platter capacity exceeds BIOS limited 528mb capacity. LBA mode added to support addressing above this limit. Note: Customers have devised alternate C:H:S methods to get around this limitation. LBA will become more standard in 1995!	Thunderbolt implementation added.
Adaptive Equalization. (In Process Test at PP2)	Wider variety of heads and media combinations warrant maximizing each head for each surface.	Longer test process time as the heads are optimized for each surface.
Cache algorithm. (In PP2 F/W)	Increase probability of a cache hit.	Better benchmark performance.
External Diskware patches moved to internal ROM. (In PP2 F/W)	Free up Diskware space to allow for new Diskware patches.	None.
Interface fixes for IBM AT Loop test. (In PP2 F/W)	RoadRunner AT never went through an IBM Qualification so some IBM specific issues still remain.	Will use Thunderbolt code as a starting point. Maverick still needs testing IBM compatibility testing to identify problem areas.

MAVERICK
Cache Change

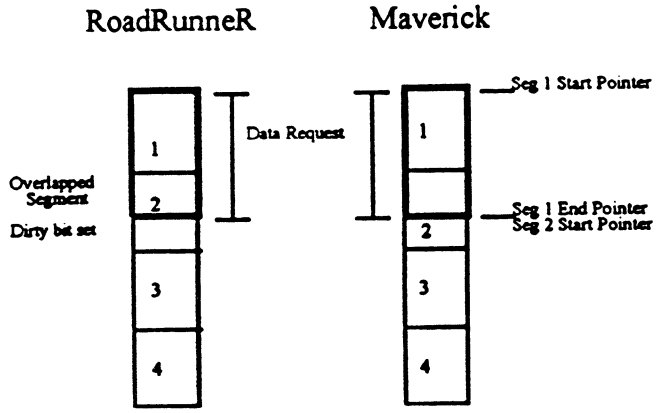
Read Cache Optimization
(Algorithm same as RRR)

RoadRunneR
During Cache/Prefetch if the block of data requested is larger than the cache segment, the algorithm would extend the ending pointer into the next segment overlapping existing data thus setting the "Dirty" bit in segment being "overlapped". If the next request for data was in the "dirtied" segment then data would be retrieved from disk.

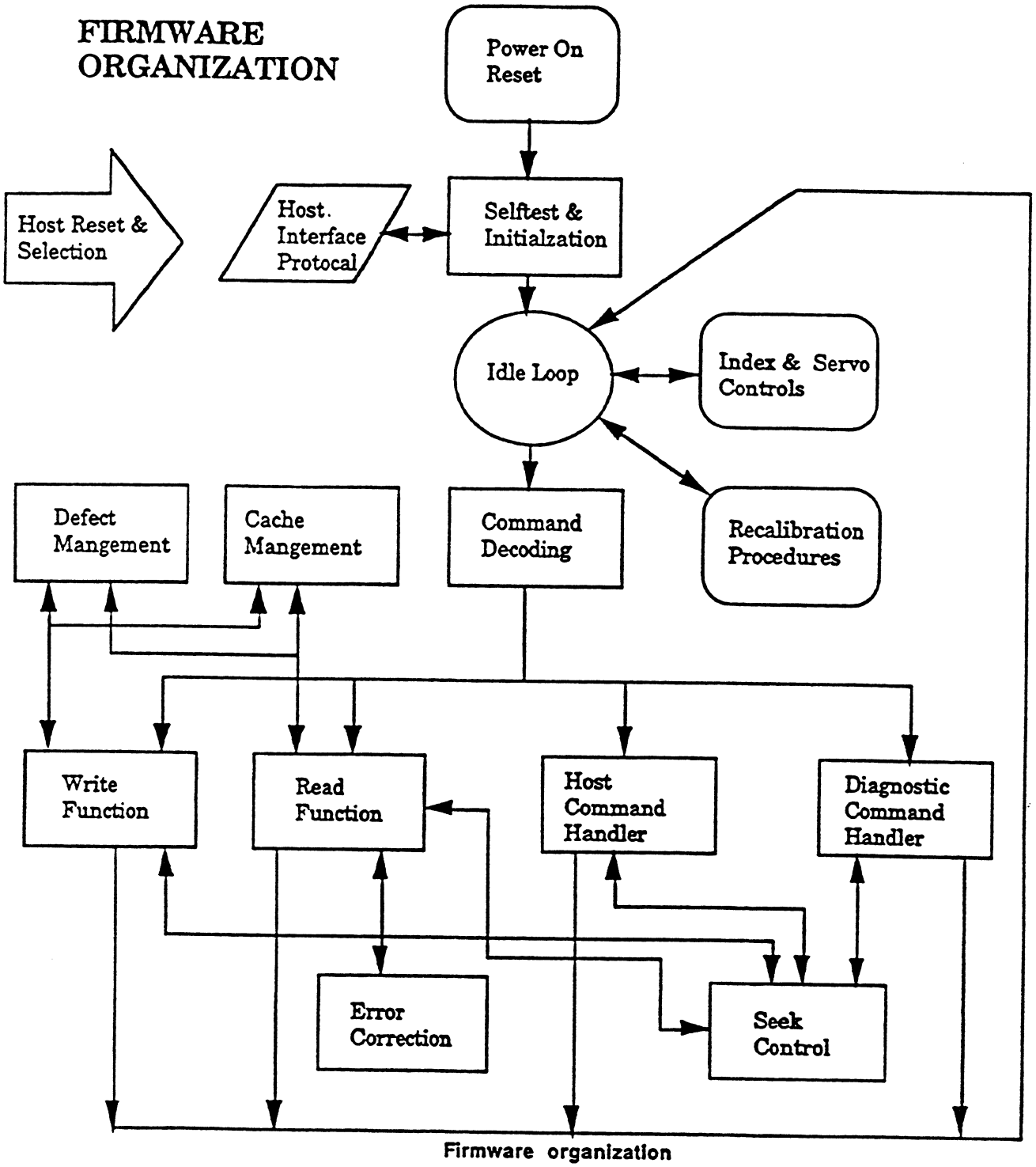
Maverick
The handling of data in Cache was changed in that when a block of data requested is larger than the cache segment, the algorithm allows the segment to "overlap" the next, but without setting the "Dirty" bit of the segment being overlapped. What happens is the starting pointer for the segment being "overlapped" is moved and the data is left intact in the buffer for future retrieval from a cache hit.

This allows higher throughput performance on random cache hits as the data is stored longer in cache.

EXAMPLE:



FIRMWARE ORGANIZATION



Firmware organization