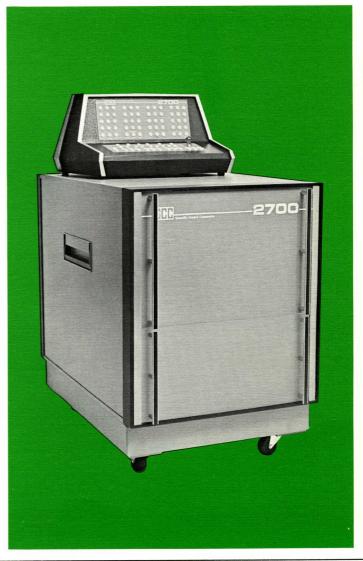
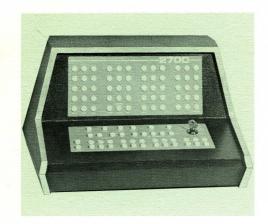


SCC 2700 DIGITAL COMPUTER 880 nanosecond





The SCC 2700 880 Nanosecond Digital Computer



The SCC 2700 digital computer represents a completely new approach to the small computer field. Because of its utilization of the most advanced concepts and techniques, the SCC 2700 presents the user a cost-performance ratio that cannot be matched by any other machine of its class. The SCC 2700 achieves a degree of maintainability not previously realized. This is accomplished with design features such as a "Read Only Memory" for internal sequences control and high speed integrated circuit components mounted on extra large printed circuit boards in a "Register Slice" arrangement.

FEATURES

- HIGH SPEED MEMORY
- 880 ns full cycle time. Memory is completely asynchronous to the CPU. The memory capacity is expandable to 65,536 words in 4096 word increments. Memory parity may be added as an optional feature.

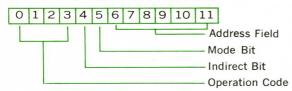
Basic memory module is a 21/2 D 4096 core memory with an

- FULLY INTEGRATED
- Uses the most advanced TTL integrated circuit components.
- MICRO-PROGRAMMED ORGANIZATION
- Micro-programmed for added reliability and maintainability. Permits the addition of optional instruction sets such as floating point arithmetic to be implemented at modest cost.
- POWER FAILURE
 PROTECTION (Optional)
- A unique power supply design insures program integrity in the event of power system failures. The SCC 2700 is not affected by power interruptions of less than 20 milliseconds duration. Power interruptions of longer than 20 milliseconds duration generate a power failure interrupt. Reserved power permits 15 milliseconds of normal operation after the detection of power failure.
- HARDWARE INDEX REGISTER
- In addition to providing address modification for memory reference instructions, the index register is a valuable aid in logical operations. A special set of instructions provide logical and arithmetic operations which use the index register and the accumulator as operands.
- VERSATILE I/O
- Both partyline and buffer channels available with up to 32 duplex devices per channel.
- MAPPING AND PROTECTION (Optional)
- Memory mapping provides two memory maps for both system and user. Allows implementation of multiprocessing systems with full memory access control. System and all users may be fully protected.
- PRIORITY INTERRUPTS
- Fully nested priority interrupts can be incorporated which permit external devices to command computer to enter a specific subroutine.
- REMOTE CONTROL CONSOLE (Optional)
- Lends versatility to the general purpose installation where operator or programmer needs ready access to controls.

STANDARD INSTRUCTION LIST

The following instructions are standard on all 2700's. The timing given for all instructions is in micro-steps which are 220 nanoseconds.

BASIC INSTRUCTION FORMAT



ARITHMETIC INSTRUCTIONS

Mnemonic	Instruction Name	Micro-Steps
ADD	Add to Accumulator	8
SUB	Subtract from Accumulator	8
XOR	Exclusive OR with Accumulator	8
AND	AND with Accumulator	8
MIN	Memory Increment and Skip on Zero	10

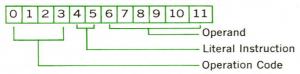
LOAD AND STORE INSTRUCTIONS

0
0
8
8

JUMP INSTRUCTIONS

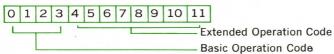
JMF	Jump Forward	4
JMB	Jump Backward	4
JSL	Jump and Store Location	17
SKN	Skip if Accumulator and	
	Memory Not Equal	8

LITERAL INSTRUCTION FORMAT



Mnemonic	Instruction Name	Micro-Steps
ANL	AND Literal	6
XOL	Exclusive OR Literal	6
LDL	Load Accumulator Literal	6
ADI	Add to Accumulator Literal	6

EXTENDED INSTRUCTION FORMAT



SYSTEM INSTRUCTIONS

Mnemonic	Instruction Name	Micro-Steps
HLT	Halt	6
LMR	Load Map Register	8
IMS	Indirect Map Set	6
IMR	Indirect Map Reset	6
ENA	Enable Interrupt System	6
DIS	Disable Interrupt System	6
CLI	Clear Current Interrupt	6
SRT	System Return	24

I/O INSTRUCTIONS

Mnemonic	Instruction Name	Micro-Steps *
XMT	Transmit	9
SKR	Skip on Device Ready	9
SCS	Set Channel Status	8
SUS	Set Unit Status	8
XCC	Execute Channel Command	8
XUC	Execute Unit Command	8
ISW	Input Status Word	8
IIU	Input Interrupting Unit	8
SEL	Select	8
TMR	Terminate	8

NOTE: With optional memory protection feature, System and I/O Instruction may only be executed while in System Mode.

*Timing Device Dependent

CLUET	INICTOI	ICTIONS

SAR LAR SAL LAL SLR SLL LLL SRR SRR LRR SRL LRL SCR LCCR SCL LCL	Short Arithmetic Right Shift Long Arithmetic Right Shift Short Arithmetic Left Shift Long Arithmetic Left Shift Long Arithmetic Left Shift Short Logical Right Shift Long Logical Right Shift Short Logical Left Shift Long Logical Left Shift Short Rotate Right Shift Long Rotate Right Shift Short Rotate Left Shift Short Rotate Left Shift Long Rotate Left Shift Short Circulate Right Shift Long Circulate Right Shift Short Circulate Right Shift Long Circulate Left Shift Long Circulate Left Shift	666666666666666
FGISTER	MANIPULATION	

REGISTER MANIPULATION

AAX	AND Accumulator and Index	7
AOX	OR Accumulator and Index	7
ADC	ADD Carry	6
LAS	Load Accumulator from Console Switches	5
ESA	Extend Sign of Accumulator	5
LDS	Load Status into Accumulator	5
CAX	Copy Accumulator into Index	5
CXA	Copy Index into Accumulator	5
XAX	Exchange Accumulator and Index	7
XHA	Exchange Halves of Accumulator	12

CONTROL AND TEST INSTRUCTIONS

COT	Carry Out Test	5
OFT	Overflow Test	5
SCN	Set Carry On	5
SCF	Set Carry Off	5
XSS	Index State Set	5
XSR	Index State Reset	5
IXS	Indirect Index State Set	5
IXR	Indirect Index State Reset	5
JRT	Jump Return	16

SYSTEM CALLS

SISILIVI	CALLS	
SC1	System Call 1	20
SC2	System Call 2	20
SC3	System Call 3	20
SC4	System Call 4	20
SC5	System Call 5	20
SC6	System Call 6	20
SC7	System Call 7	20
SC8	System Call 8	20

OPERATE GROUP

FIRST OPERATION

Select the register defined by Bit 7

0 = A Register 1 = X Register

SECOND OPERATION

Perform (one of eight functions as specified by Bits 8-10
000	Test Selected Register only
001	Increment Selected Register
	(Sel Reg) $(+)1 \rightarrow$ Sel Reg
010	Add Unselected Register to Selected Register
	$(A) + (X) \rightarrow Sel Reg$
011	Exclusive OR A & X
	$(A) \bigoplus (X) \rightarrow Sel Reg$
100	One's complement of Selected Register
	$(Sel Reg) \rightarrow Sel Reg$
101	Two's complement of Selected Register
	$(Sel Reg) + 1 \rightarrow Sel Reg$
110	Decrement Selected Register
	(Sel Reg) $-1 \rightarrow$ Sel Reg
111	Subtract Selected Register from Unselected Register
	(Unsel Reg) — (Sel Reg) \rightarrow Sel Reg

THIRD OPERATION

Test the results of the above functions and skip as follows: R_4 R_5 0 0 No Skip 0 1 Skip if positive (>0) 1 0 Skip if negative 1 1 Skip if Zero

FOURTH OPERATION

Clear selected register if specified by Bit 6. If Bit 6=0, do not clear selected register.

OPTIONAL INSTRUCTION GROUPS

DOUBLE PRECISION OPTION

DOUBLE PRECISION INSTRUCTION FORMAT

0 1 2 3 4 5 6 7 8 9 10 11

Extended Operation Code

Indirect Bit

Basic Operation Code

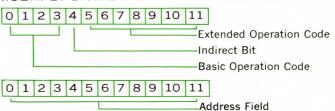
0 1 2 3 4 5 6 7 8 9 10 11 Address Field

Mnemonic	Instruction Name	Micro-Steps
LDD	Load Double	16
STD	Store Double	16
DAD	Double Add	17
DSB	Double Subtract	17
DMY	Double Multiply	60
DDV	Double Divide	60
CAB	Copy Accumulator into B	5
CBA	Copy B into Accumulator	5
XAB	Exchange Accumulator and B	7
CLB	Clear B	5
ESH	Extended Shift	12 + N
NDX	Normalize and Decrement Index	8 + 2N

NOTE: The Double Precision instruction group requires the Multiply-Divide instruction group and the Extended Accumulator (B Register).

MULTIPLY-DIVIDE OPTION

MULTIPLY-DIVIDE INSTRUCTION FORMAT

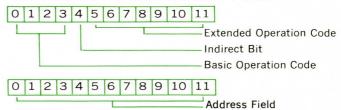


I nemonic	Instruction Name	Micro-Steps
MPY	Multiply	25
DIV	Divide	26

マグスクミリモアモアモアモアモアモアモアモア

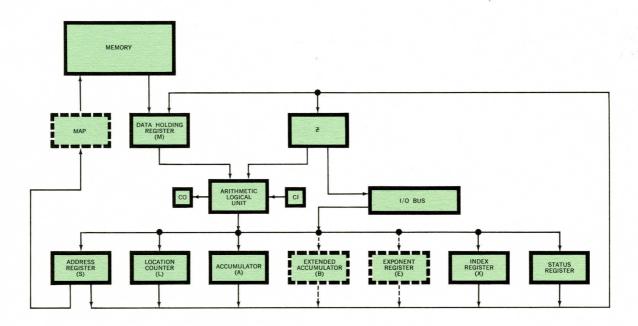
FLOATING POINT ARITHMETIC OPTION

FLOATING POINT INSTRUCTION FORMAT

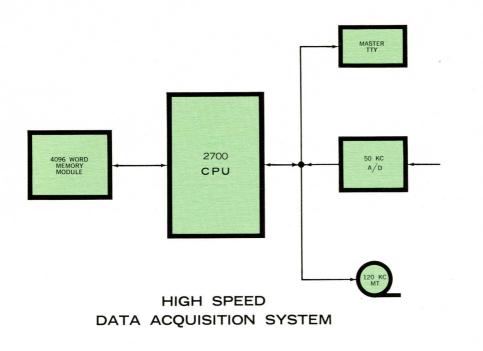


Mnemonic	7,641,633,1,614		
	Instruction Name	Micro-Steps (Typ.)	
LDF	Load Floating	20	
STF	Store Floating	20	
FAD	Floating Add	32	
FSB	Floating Subtract	35	
FMP	Floating Multiply	75	
FDV	Floating Divide	75	

NOTE: The Floating Point Instruction group requires the Double Precision instruction group and the Exponent Register (E).



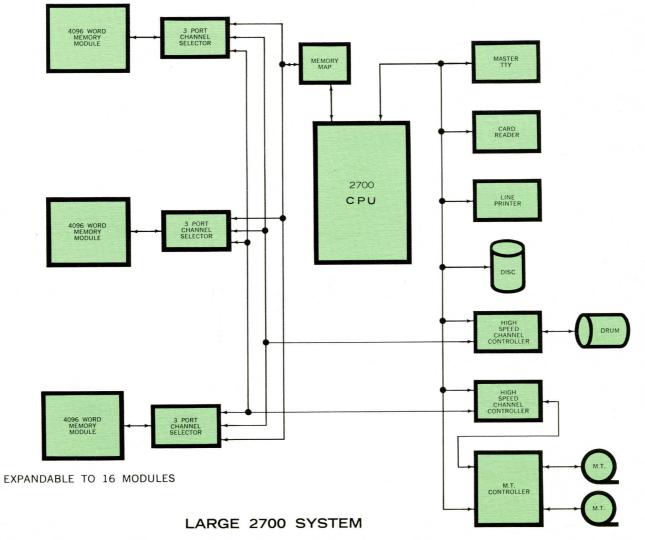
PRINCIPAL REGISTERS AND DATA PATHS

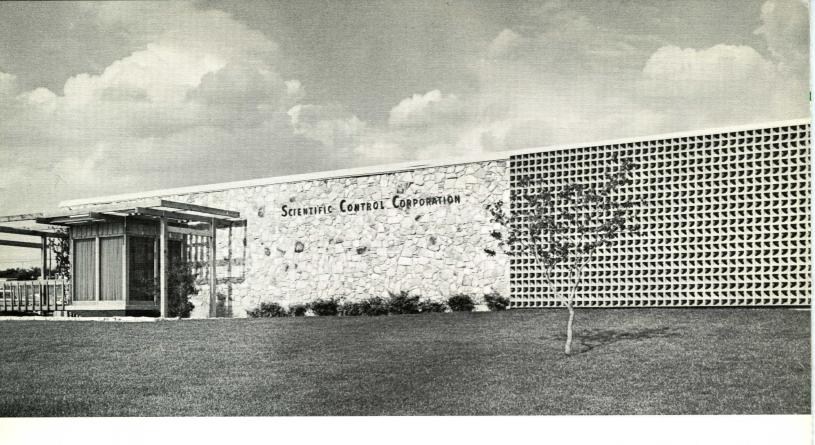


PERIPHERAL EQUIPMENT

- MEMORY MODULES
- HIGH SPEED TAPE READER
- PAPER TAPE PUNCH
- CARD READER
- CARD PUNCH
- INCREMENTAL PLOTTER
- LINE PRINTER
- DATAPHONE* CONTROLLER
- MAGNETIC TAPE TRANSPORTS
- MAGNETIC DISC
- TELETYPE INPUT/OUTPUT DEVICE
- PULSE HEIGHT ADAPTER
- REMOTE TELETYPE UNIT
- SELECTRIC TYPEWRITER
- CRT DISPLAY
- ANALOG MULTIPLEXER
- ANALOG TO DIGITAL CONVERTER
- DIGITAL TO ANALOG CONVERTER
- MEMORY MAP UNIT
- 3 PORT MEMORY ADAPTER
- INTERRUPT CLOCK OR REAL TIME CLOCK

*TRADE MARK AT&T





SCC maintains complete support activities for its users. Installation and maintenance services are available through SCC offices strategically located throughout the United States. For pre-procurement demonstration of hardware and programs in Dallas, contact nearest regional office or the marketing department in Dallas.

EASTERN REGION

College Park, Maryland (Washington, D.C.) 301/779-2510

SOUTHEASTERN REGION

Huntsville, Alabama 205/881-8805

WESTERN REGION

Los Angeles, California 213/272-9311

SOUTHWESTERN REGION

Dallas, Texas 214/241-2111

MIDWESTERN REGION

Dallas, Texas 214/241-2111

CORPORATE MARKETING

Dallas, Texas 214/241-2111



Scientific Control Corporation

P.O. Box 34529 • Dallas, Texas 75234 • 214 — 241-2111 • TWX 910-860-5509