XDS 901565A-1
$11.75

TECHNICAL MANUAL

EXTENDED PERFORMANCE RAPID ACCESS DATA FILE

MODELS 7231/7232

October 1969
(Revised June 1970)

Xerox Data Systems 701 South Aviation Blvd., El Segundo, California 90245 (213) 772-4511, 679-4511

LIST OF EFFECTIVE PAGES

Total number of pages is 356, as follows:

Page No.	Issue
Title	Original
A	Original
Foreword	Original
i thru x	Original
1-1 thru 1-6	Original
2-1 thru 2-4	Original
3-1 thru 3-14	Original
4-1 thru 4-152	Original
5-1 thru 5-24	Original
6-1 thru 6-30	Original
7-1 thru 7-14	Original
8-1 thru 8-26	Original
8-27 thru 8-28	Revised June 1970
8-29 thru 8-32	Original
9-1 thru 9-66	Original

FOREWORD

This publication supersedes XDS publication No. 901565A and incorporates the information previously supplied by PDQ No. 70-018.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

LIST OF TABLES (Cont.)

LIST OF RELATED PUBLICATIONS

The following publications contain information not included in this manual but necessary for a complete understanding of the Extended Performance Rapid Access Data (EP RAD) File when used with related XDS equipment.

Publication Title	Publication No.
Extended Performance RAD Storage System, Models 7231/7232, Reference Manual	901557
Sigma Computer Systems Interface Design Manual	900973
Power Supply Model PT20, Technical Manual	901157
Sigma 5 and 7 Extended Performance Rapid Access Data (RAD) File, Program No. 704978B, Diagnostic Program Manual	901540
Peripheral Equipment Tester Model 7901, Technical Manual	901004
Sigma 2 Computer, Technical Manual	900630
Sigma 2 Computer, Reference Manual	900964
Sigma 5 Computer, Technical Manual	901172
Sigma 5 Computer, Reference Manual	900959
Sigma 7 Computer, Technical Manual	901060
Sigma 7 Computer, Reference Manual	900950
Multiplexing Input/Output Processor, Models 8271/8471 and 8272/8472, Technical Manual	901515
Selector Input/Output Processor (SIOP), Model 8285 and 8485, Technical Manual	901195
Diagnostic Control Program for Sigma 5 and Sigma 7 Computer Peripheral Devices, Reference Manual	900712
Sigma 2 Systems Test Monitor, Diagnostic Program Manual	900841
Sigma 5 and 7 Systems Test Monitor, Diagnostic Program Manual	901076
Sigma 2 High Capacity Rapid Access Data (RAD) File Test, Diagnostic Program Manual	901538
Sigma 5 and 7 Relocatable Diagnostic Program Loader, Diagnostic Program Manual	900972
Sigma 2 Relocatable Diagnostic Program Loader, Diagnostic Program Manual	901128

SECTION I
INTRODUCTION

1-1 SCOPE OF MANUAL

This manual provides technical information pertaining to the Extended Performance Rapid Access Data File (EP RAD file), which consists of the EP RAD Controller Model 7231 and from one to eight EP RAD Storage Units Model 7232. An EP RAD file is an item of peripheral equipment which can be used with any of the Sigma series computers (Sigma 2, Sigma 5, or Sigma 7). The EP RAD file is manufactured by Xerox Data Systems, El Segundo, California.

The documents in the list of related publications should be consulted to supplement the information in this manual. A complete set of documents for this equipment consists of this manual, related publications, engineering drawings, wire lists, diagnostic programs, and other data supplied with the equipment.

1-2 ORGANIZATION OF MANUAL

The information contained in this manual is organized as follows:

a. Section I outlines the content and organization of the manual and provides a brief description of the EP RAD file and its function.

b. Section II describes the location and function of each switch and indicator and provides simple machine language programs which illustrate the relation of the EP RAD file to the computer operation.

c. Section III describes the operation of the EP RAD file in terms of data flow through registers in response to signals generated by the computer. No reference is made to signals or logic equations, and block diagrams and flow diagrams support the text.

d. Section IV contains a detailed description of the operation of all circuits of the EP RAD file. The purpose of each signal, the logic equations which control the signal level, and the relations between signals are described; supporting logic diagrams, timing diagrams, and flow diagrams are included.

e. Section V lists all signals of the EP RAD file, describes the function of each signal, and contains phase sequence charts for each EP RAD file operation.

f. Section VI includes schematic diagrams for control panels, power distribution, terminal boards, logic diagrams, and other engineering drawings and provides a list of engineering drawings required to supplement this manual.

g. Section VII contains cable diagrams; module location charts; power, cooling, and space requirements; and other data required for installation, including preoperational check procedures.

h. Section VIII provides lists of special tools and test equipment; schedules and procedures for cleaning, lubricating, and preventive maintenance testing; and procedures for performance testing, trouble analysis, and adjustment.

i. Section IX contains an illustrated parts breakdown and parts list.

1-3 DESCRIPTION

1-4 EP RAD FILE

An EP RAD file consists of from one to eight EP RAD storage units and associated interconnecting cables. Each EP RAD storage unit consists of a cabinet that contains a disc file, an EP RAD selection unit, a power distribution panel, a motor control assembly, a Power Supply Model PT20, and interconnecting cables, wiring harnesses, and pressure lines. (See figures 1-1 and 1-2.) An EP RAD controller is collocated with one of the EP RAD storage units. (See figure 1-3.)

Each EP RAD storage unit can accommodate more than 6 million bytes of data. An EP RAD file with the maximum eight EP RAD storage units can store more than 50 million bytes of data. Data bytes may be read from, or written into, the EP RAD storage unit at an average rate of more than 350,000 bytes per second.

1-5 EP RAD CONTROLLER

An EP RAD controller consists of three 32-module chassis and the 74 modules required for operation with an eight-bit data path. For the optional 16-bit data path, five additional modules are needed for a total of 79 modules; for the optional 32-bit data path, eight additional modules are needed for a total of 82 modules.

The EP RAD controller, which is the interface between the IOP and the EP RAD storage units, responds to command signals from the IOP. Signals returned from the EP RAD controller to the IOP indicate the status of an EP RAD storage unit and the status of the control timing of data transfers between an EP RAD storage unit and the IOP.

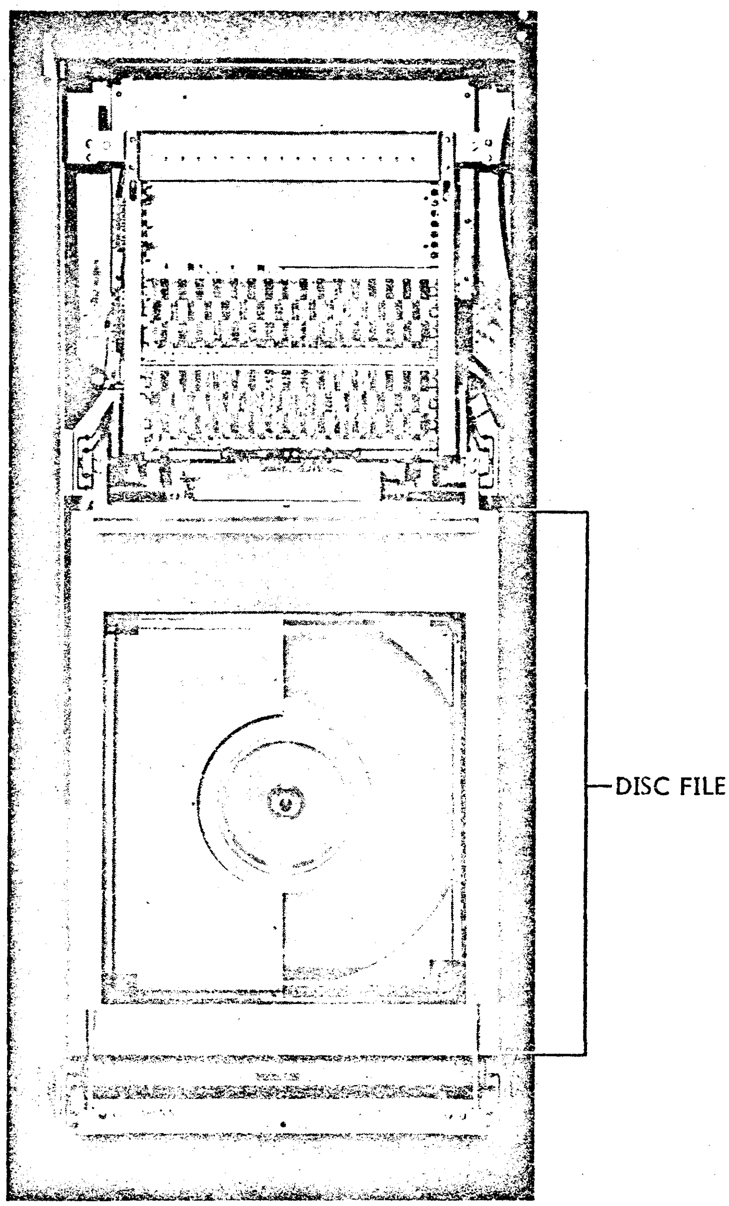


Figure 1-1. EP RAD Storage Unit, Front View

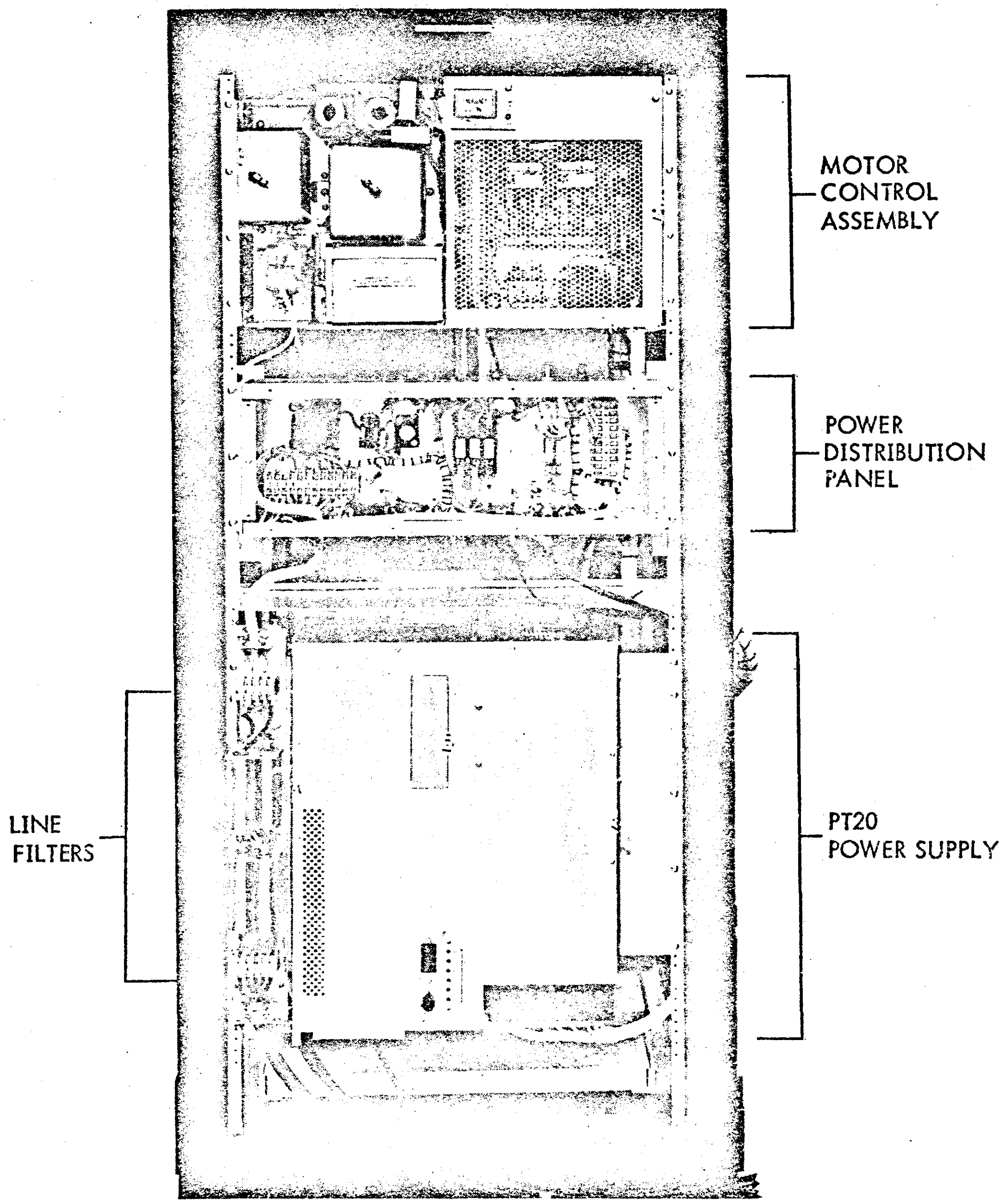


Figure 1-2. EP RAD Storage Unit, Rear View

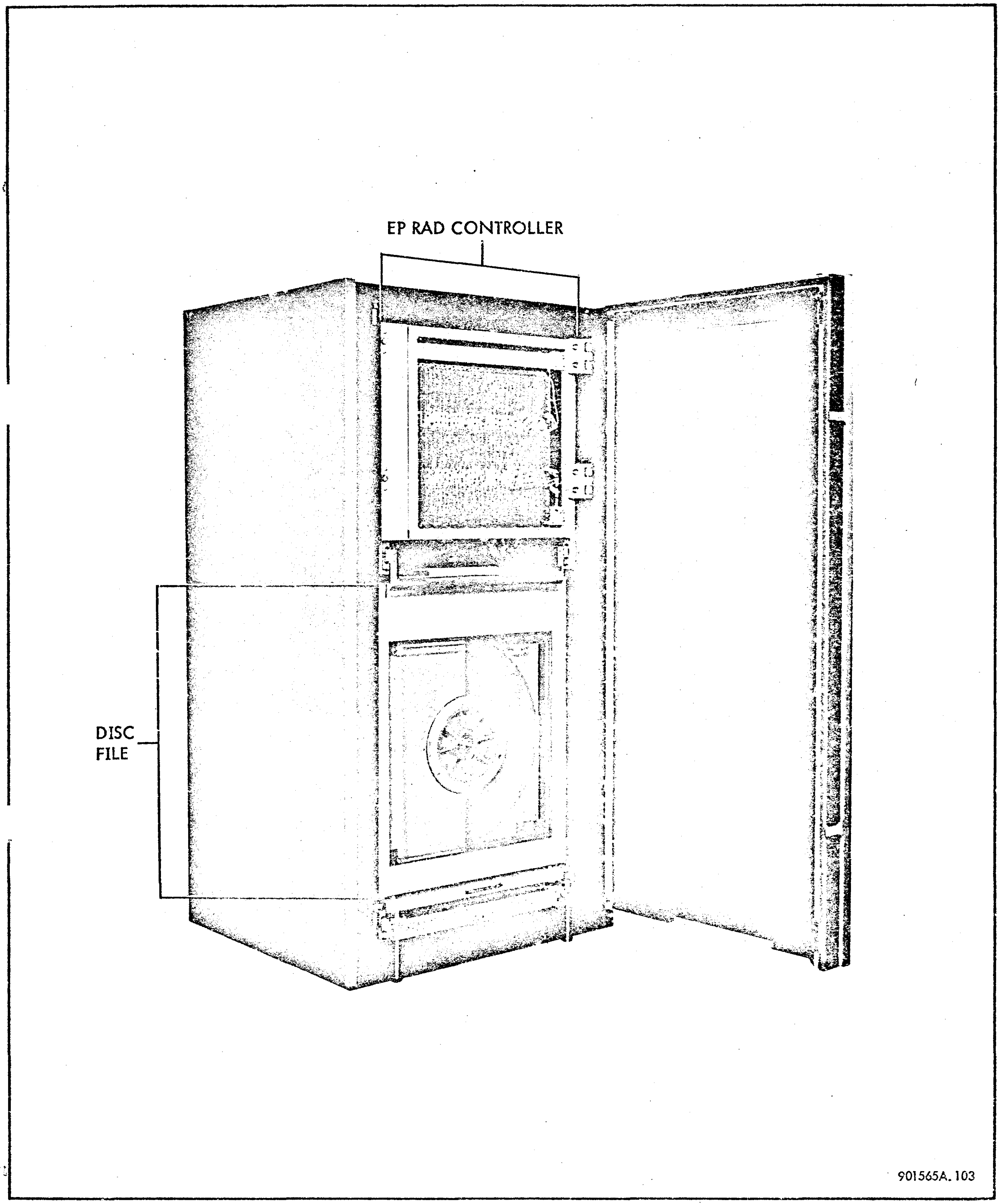


Figure 1-3. EP RAD Storage Unit with EP RAD Controller, Front View

1-6 EP RAD SELECTION UNIT

An EP RAD selection unit consists of two 32-module chassis and the 36 modules required for operation. If the logical sparing option is selected, a maximum of 13 additional modules may be used, for a total of 49 modules. The EP RAD selection unit responds to signals received from the EP RAD controller and writes data on the disc file or reads data from the disc file, as required.

1-7 DISC FILE

The disc file contains four rotating magnetic surfaces for recording digital data on 512 tracks. A separate read/write head is provided for each of the 512 tracks, and 64 spare read/write heads and tracks are available. One of the magnetic surfaces has an active sector timing track and read head. (A timing track is written on each surface of the disc, so that three spare timing tracks are available.) The magnetic surfaces are sealed in a pressurized bulkhead which is maintained at a pressure higher than standard atmospheric pressure.

1-8 MOTOR CONTROL ASSEMBLY

The motor control assembly controls the sequence of operations for starting and stopping the disc file motor and monitors the status of the disc file motor during operation. During the start sequence, the motor control assembly aborts operation if the disc file does not reach 300 rpm within a preset time delay. When power is removed for shutdown or if a power failure is sensed, the motor control assembly controls both dynamic and mechanical braking.

1-9 POWER DISTRIBUTION PANEL

The power distribution panel controls power from either the control console of the computer installation or the EP RAD storage unit.

1-10 POWER SUPPLY MODEL PT20

Power Supply Model PT20 (also referred to in this manual as the PT20 power supply) is a standard XDS power supply and is described in detail in XDS publication No. 901157. The power input required is approximately 9A from a single-phase 117V, 60Hz source. The power supply provides outputs of +4V, +8V, -8V, +25V, -25V, and +45V, with current capability sufficient for an EP RAD selection unit and an EP RAD controller if both items are installed in the EP RAD storage unit. When an EP RAD file contains more than one EP RAD storage unit, connections from PT20 power supplies should be distributed among all phases of the three-phase source. Overvoltage and short circuit protection for the PT20 power supply is provided by modules and by a resettable circuit breaker.

SECTION II
OPERATION AND PROGRAMMING

2-1 GENERAL

The EP RAD file is controlled by programmed instructions processed by the CPU and responds to commands and orders from the IOP. Controls of the EP RAD file establish its address, indicate whether an EP RAD storage unit is online or offline, provide for write protection of selected groups of tracks, and provide for turn-on and shutdown of EP RAD file operations. Controls of the EP RAD file are described in this section. A portion of a program, in machine language, is provided to illustrate the relation between the programs and the EP RAD file operations.

2-2 CONTROLS

2-3 EP RAD CONTROLLER ADDRESS SWITCHES

Four switches on an LT26 Switch Comparator module (location C24, figure 7-5) establish the four-bit address of the EP RAD controller. (See table 2-1 and figure 2-1.)

Table 2-1. EP RAD Controller Address Switch Positions (Location C24)

S4-2*	S3-2	S2-2	S1-2	Address†
Up	Down	Down	Down	1000
Up	Down	Down	Up	1001
Up	Down	Up	Down	1010
Up	Down	Up	Up	1011
Up	Up	Down	Down	1100
Up	Up	Down	Up	1101
Up	Up	Up	Down	1110
Up	Up	Up	Up	1111

*Switch S4-2 position cannot be changed while the LT26 module is in place

†Up is 1; down is 0. Switch position designations cannot be read while the LT26 module is in place

2-4 EP RAD STORAGE UNIT ADDRESS SWITCHES

Three switches on an LT26 Switch Comparator module (location A7, figure 7-4) establish a three-bit address for each EP RAD storage unit. (See table 2-2 and figure 2-1.)

2-5 ONLINE/OFFLINE SWITCH

A switch on the LT25 Special Purpose module (location C23) transfers the EP RAD file from online to offline operation. When the switch is in the 0 position, the EP RAD file is offline; when the switch is in the 1 position, the EP RAD file is online. (See figure 2-2.)

2-6 MEMORY PROTECTION SWITCHES

Sixteen switches on the front panel of the EP RAD selection unit (figure 1-1) may be used to prevent any CPU program from writing on selected groups of tracks on the disc file. The toggle switches are labeled MEMORY PROTECTION

Table 2-2. EP RAD Storage Unit Address Switch Positions (Location A7)

S3-1	S2-1	S1-1	Address*
Down	Down	Down	000
Down	Down	Up	001
Down	Up	Down	010
Up	Down	Down	100
Up	Down	Up	101
Up	Up	Down	110
Up	Up	Up	111

*Up is 1; down is 0. Switch position designations cannot be read while the LT26 module is in place

Location C24 , F7

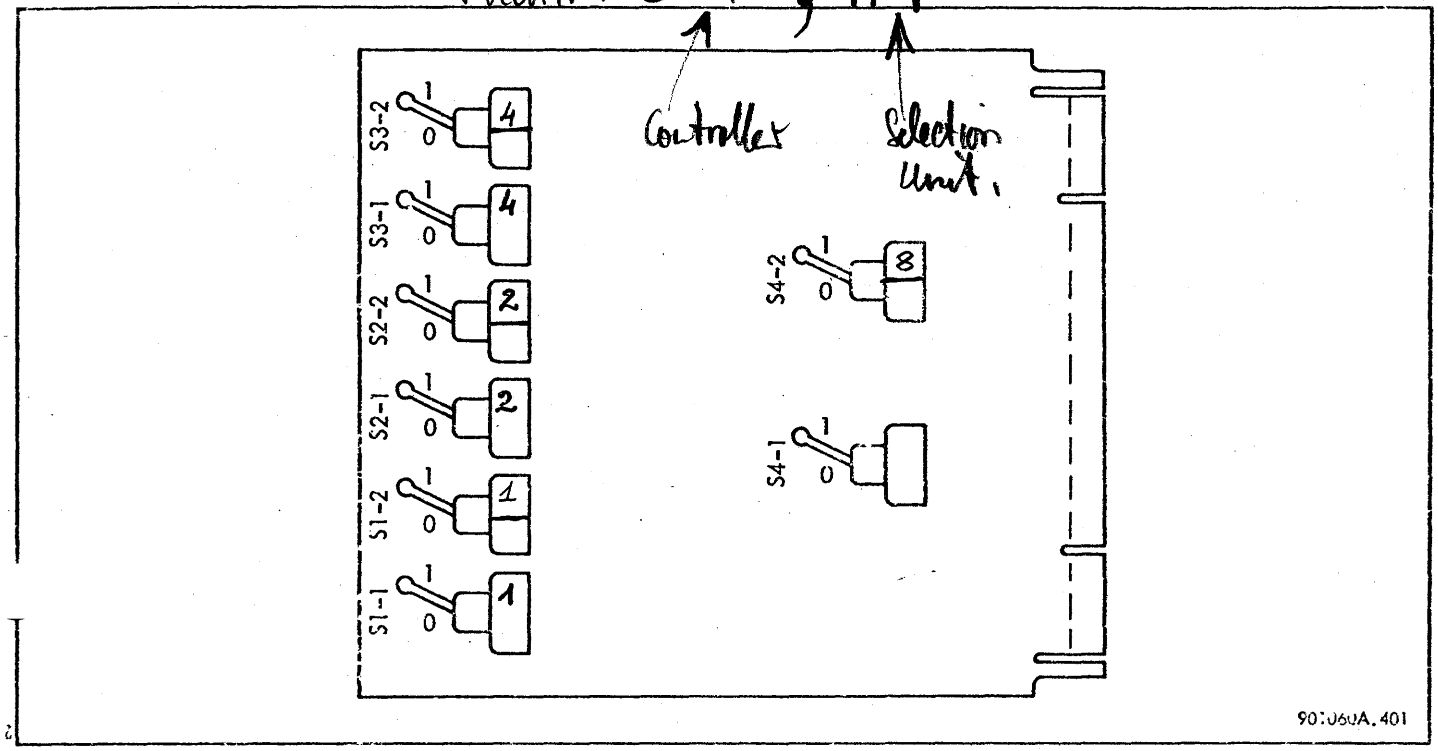


Figure 2-1. LT26 Switch Comparator Module

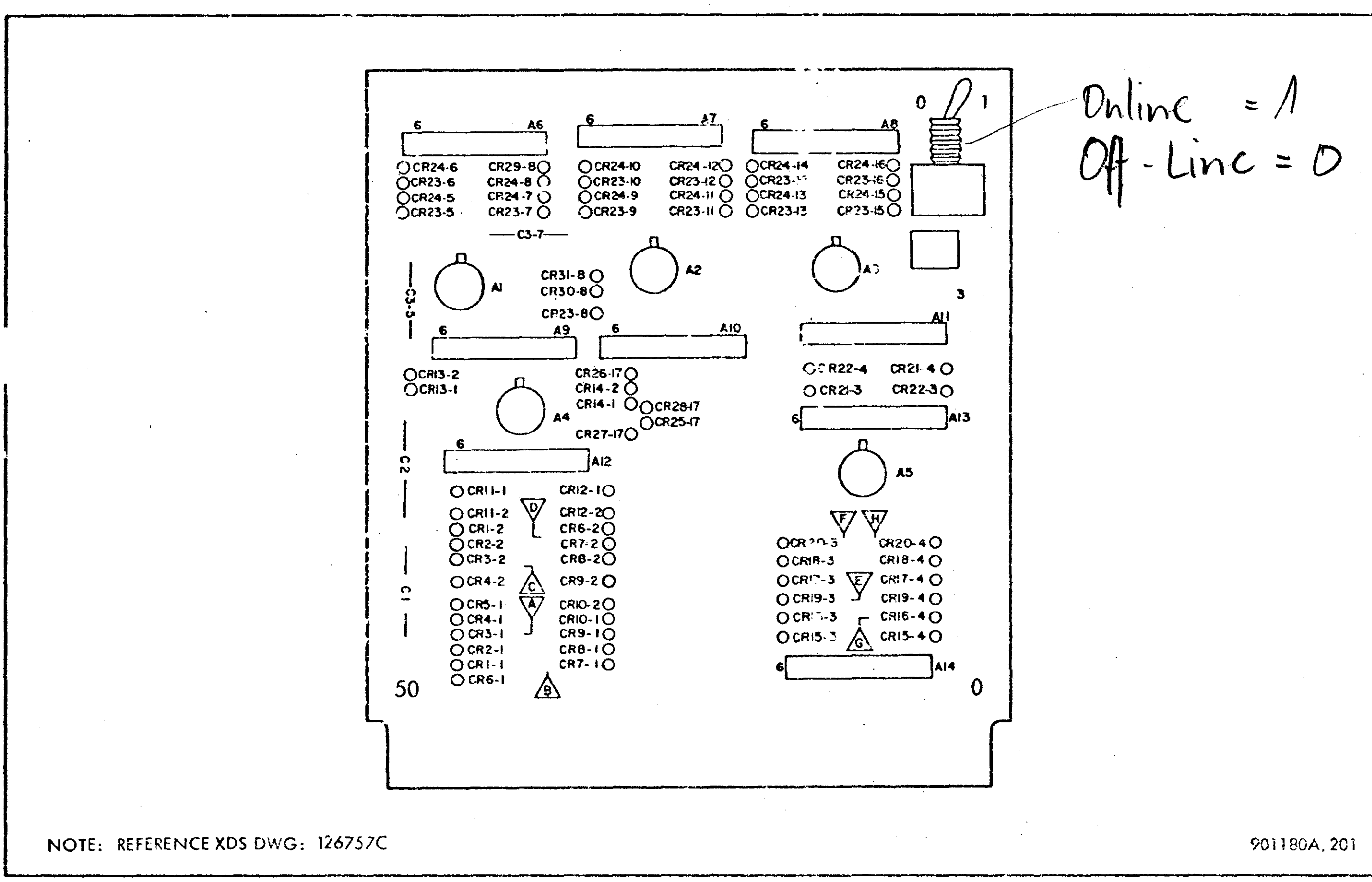


Figure 2-2. LT25 Special Purpose Logic Module

Location C23

SWITCHES, and the instruction SET SWITCH IN UP POSITION TO PROTECT INDICATED MEMORY TRACK ADDRESSES is marked on the panel. The 512 tracks are divided into 16 groups of 32 tracks each for control by MEMORY PROTECTION SWITCHES. The 32 tracks protected by each switch are indicated in decimal notation, beginning with 000 to 031 and ending with 480 to 511.

2-7 POWER DISTRIBUTION PANEL

The power distribution panel contains a toggle switch labeled REMOTE-OFF-ON. No power is available for the selection unit, controller, or fans when the toggle switch is in the OFF (center) position. When the switch is in the REMOTE position, application of power is controlled from control panels of the CPU. When the switch is in the ON position, the ac power source is directly connected to the EP RAD storage unit.

2-8 MOTOR CONTROL ASSEMBLY

The motor control assembly contains a circuit breaker and a toggle switch. A protective plastic cover on the circuit breaker reads EMERGENCY USE ONLY to indicate that the circuit breaker is normally ON and should not be used in routine turn-on or shutdown procedures. The POWER ON-OFF switch applies three-phase power to the motor control assembly. This power is independent of the power distribution panel.

2-9 POWER SUPPLY MODEL PT20

The PT20 power supply contains a circuit breaker and a MARGIN switch. Power is applied to the PT20 power supply through the circuit breaker. The MARGIN switch, which has three positions labeled H, N, and L, is used to select a high (H), normal (N), or low (L) output voltage. Refer to XDS publication No. 901157 for additional information.

2-10 OPERATING PROCEDURES

After an EP RAD file has been installed and checked as described in section VII, no special turn-on or shutdown procedures are required. The normal control positions are as follows:

a. The EP RAD controller address switches are set to the four-bit address assigned to the controller of the EP RAD file (1000 through 1111).

b. The EP RAD storage unit address switches are set to the three-bit address assigned to the EP RAD storage unit (000 through 111).

c. The online/offline switch is set to 1.

d. The MEMORY PROTECTION SWITCHES are set in the up position to protect any group of 32 tracks or are set in the down position to allow writing on tracks by CPU programs.

e. The REMOTE-OFF-ON switch on the power distribution panel is set to REMOTE.

f. The POWER ON-OFF switch on the motor control assembly is set to ON.

g. The circuit breaker on the motor control chassis is ON and the protective cover is closed.

h. The circuit breaker on the PT20 power supply is ON.

i. The MARGIN switch on the PT20 power supply is set to N.

2-11 PROGRAMMING

2-12 INSTRUCTIONS

Control signals and data signals exchanged between the EP RAD file and the CPU through the IOP are related to the input/output instructions. (Refer to the technical manual and reference manual associated with the computer installation for details.) After a start input/output operation (SIO), halt input/output operation (HIO), test input/output (TIO), or test device (TDV) instruction is processed by the CPU, the IOP generates signals which require a response from the addressed peripheral device controller. If the EP RAD file is addressed, the IOP generates signals which contain the information required by the instruction. After an acknowledge I/O interrupt (AIO) instruction is processed by the CPU, the IOP generates signals which require a response from the highest priority peripheral device controller that has an interrupt pending. If the controller of the EP RAD file responds, the IOP returns its address and the address of the EP RAD storage unit currently stored in the unit register.

2-13 SAMPLE PROGRAM

XDS publication No. 901557 describes two sample programs. One program is for use in either a Sigma 5 or a Sigma 7 computer, and one is for use in a Sigma 2 computer. A group of machine language instructions, which form a part of the Sigma 5 and 7 programming example labeled IOINTSUP, is listed in table 2-3.

Table 2-3. Portion of Machine Language Program Controlling EP RAD File

Instruction*	Remarks
2280 0020	Load immediate (LI). Causes 0000 0200 to be stored in general register 8 to permit arming I/O interrupts
6D80 1200	Write direct (WD). This WD instruction in interrupt control mode causes arm and enable (code 010) of all group 0000 interrupts selected by a one
220M MMMM	Load immediate (LI). Causes a doubleword command in location M MMMM to be stored in general register 0. Value assigned to M MMMM is controlled by the program
4CAX UUUU†	Start input/output operation (SIO). Causes the operation coded by doubleword command in location M MMMM (now in general register 0) to begin in EP RAD file at address UUUU. (UUUU addresses the EP RAD file controller and one of eight EP RAD storage units. The track address and the word count are contained in the doubleword.)
74NX SSSS†	Store conditions and floating point control (STCF). For this program, the significant part of the STCF instruction is that which causes the condition code response to the previous SIO instruction to be stored in memory location SSSS. The value of SSSS is controlled by the program. N has no significance
68CX LLLL†	Branch on conditions reset (BCR). This BCR instruction forms the logical product (AND) of its R-field (1100) and the condition code saved by the previous STCF instruction. If the SIO is accepted, the logical product is zero, and the WAIT instruction in location LLLL is executed. If the SIO is not accepted, the logical product is not zero, and the next instruction in sequence is executed. LLLL is established by the program
331X PPPP†	Modify and test word (MTW). If the MTW program is executed, its R-field (0001) is added to the effective word stored in the effective location of X PPPP, and the sum is stored in the effective location. Execution of this instruction causes a branch back to the main program. PPPP is established by the program
2ENX RRRR†	WAIT instruction. After this instruction is executed, no other instructions are executed until an interrupt signal is received at the end of the I/O operation started by the accepted SIO instruction. The next AIO instruction in sequence is then executed. RRRR is established by the program
6EAX JJJJ	Acknowledge I/O interrupt (AIO). Causes status bits (0 through 15) and I/O address code bits (21 through 31) from the EP RAD file to be stored in general register 10. JJJJ is established by program

*Instructions are coded in hexadecimal notation. Symbols other than 0 through 9 and A through F are explained

†X represents a three-bit index register. Additional bits are part of the data in bits 15 through 31 or are not significant

SECTION III
FUNCTIONAL OPERATION

3-1 GENERAL

An EP RAD file consists of one EP RAD controller and from one to eight EP RAD storage units (figure 3-1). A Sigma series computer controls the EP RAD file through either a multiplexing input/output processor (MIOP) or a selector input/output processor (SIOP). The maximum capacity of each EP RAD storage unit is more than 6 million data bytes. Data bytes may be written into, or read from, the EP RAD file under program control, as described in paragraph 2-11.

Each EP RAD storage unit contains a disc file, a selection unit, a PT20 power supply, a power distribution panel, a motor control assembly, and interconnecting cables, wiring harnesses, and pressure lines. One of the EP RAD storage units contains the EP RAD controller that functions as the interface between the EP RAD file and the IOP.

The EP RAD controller and all selection units form a buffer between storage devices operating at independent clock rates. The clock rate of the computer is established by its timing circuits; the clock rate of an EP RAD storage unit is established during the writing process by the use of the Manchester encoding technique. The EP RAD storage unit may be required to read or write 12 sets of 1024 data bytes in one revolution of the disc. To meet this requirement, the EP RAD controller must accept data from one storage device at one clock rate, temporarily store the data, and transmit the data to the other storage device at another clock rate. In addition, the EP RAD controller must make a parallel-to-serial change in format for data being transferred from the computer memory through the IOP to the EP RAD storage unit and must make a serial-to-parallel change in format for data being transferred from the EP RAD storage unit through the IOP to the computer memory.

Signals passing between the EP RAD controller and any EP RAD storage unit are exchanged through a set of transmission lines common to all EP RAD storage units. However, the EP RAD controller communicates with only one of the EP RAD storage units during any operation. The storage unit is selected by an address which is part of the command doubleword accepted by the IOP from the computer memory. Terms frequently used in this manual are defined in table 5-1.

3-2 DATA ORGANIZATION

Data stored in the disc file is organized as indicated in figure 3-2. Four magnetic surfaces are used, each surface having 128 read/write heads. Data may be written by, or read from, only one of the read/write heads at any time. The surface of the disc associated with a particular read/write head is called a track. Each track is divided into 12 equal sectors by timing signals permanently recorded on one surface of the disc. These timing signals are read by circuits of the selection unit. One of the 512 read/write heads is selected by a nine-bit track address. Each sector is identified by a four-bit sector address.

Within each sector, 1024 bytes of eight bits each are stored. The total data capacity of the disc file is obtained by multiplying 1024 bytes/sector by 12 sectors/track by 128 tracks/surface by 4 surfaces. This is a total of 6,291,456 bytes. An EP RAD file with the maximum complement of eight EP RAD storage units can store more than 50 million data bytes.

Preceding each set of 1024 data bytes is a five-byte preamble. This preamble is written by the EP RAD controller to identify the beginning of a sector of data and to synchronize controller, selection unit, and disc file operations. Following the 1024 data bytes is a two-byte checksum and a one-byte postamble. The checksum is generated by controller circuits during the write sequence, and is written after all data bytes have been stored. The postamble is a string of eight zeros which identifies the end of the sector. A gap containing no data of any kind separates the sectors. During the time that this gap is under the read/write heads, preparatory operations are performed by the controller.

3-3 MECHANICAL FUNCTIONS

During operation of the EP RAD file, the read/write heads which write on (or read from) the magnetic surfaces of the disc file are held from contact with the magnetic surfaces by a thin film of air. This technique, called floating head or flying head, permits each head to be very close to a surface without contact and eliminates design problems associated with fixed heads. For example, if the position of a read/write head is fixed, the distance between the head and the moving surface varies slightly because of irregularities of surface flatness or because of a slight eccentricity of the disc axis of rotation. The variation in flux strength introduced by this variation in distance causes variation in signal levels. In addition, because the distance must be relatively large to prevent the possibility of contact, much of the strength of the magnetic field is used in the resultant air gap. However, with the flying head system of the EP RAD file, the design distance between head and surface is maintained only while the disc is spinning faster than 300 rpm. Therefore, contact between the flying heads and the disc surfaces must be relieved until the

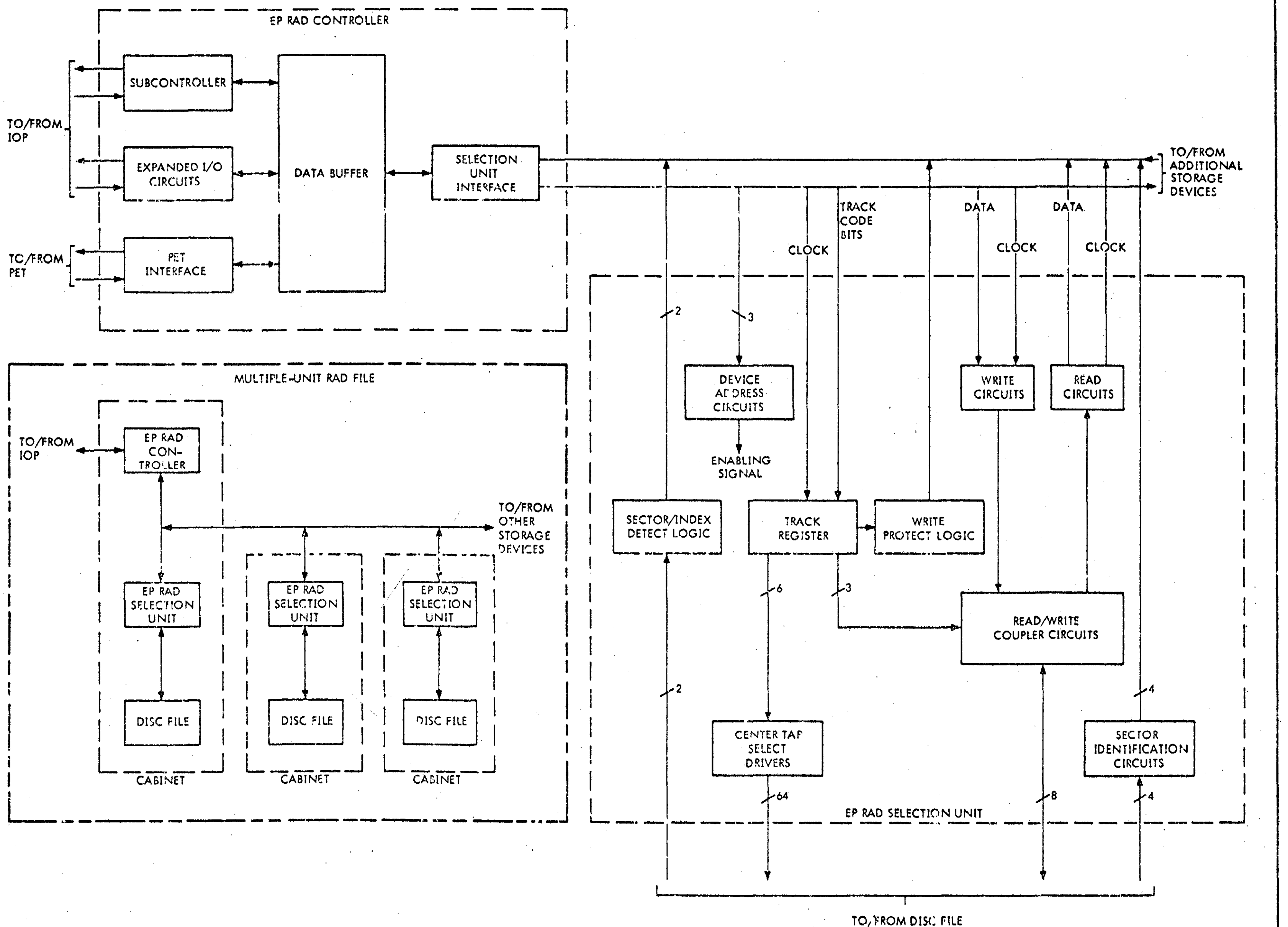


Figure 3-1. EP RAD File, Block Diagram

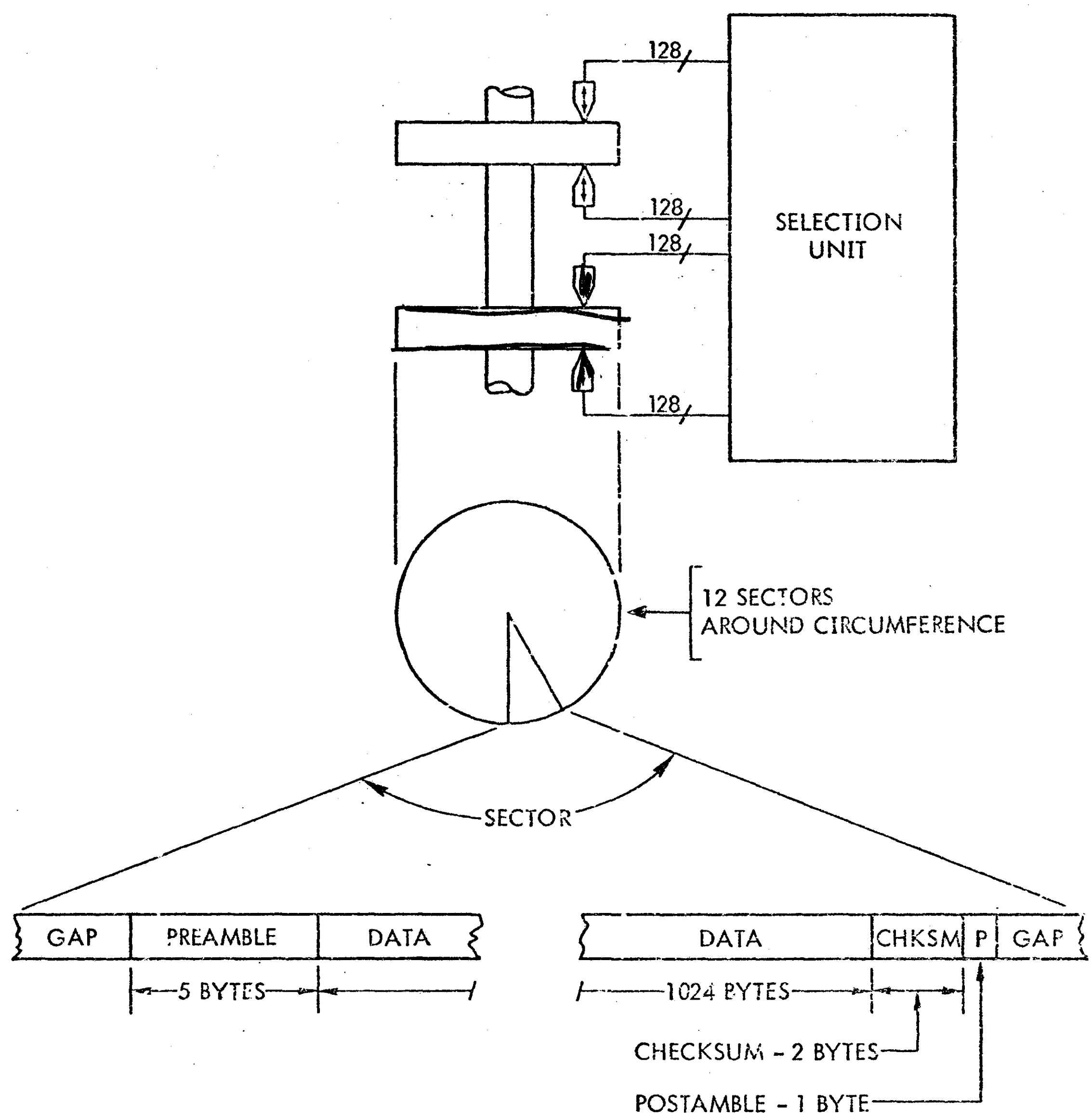


Figure 3-2. EP RAD Disc File, Data Organization

300 rpm rate is attained. During a start sequence, the motor control assembly relieves the pressure holding the heads against the disc surface. During a stop sequence, the motor control assembly controls dynamic and mechanical braking of the disc. During a start sequence or a stop sequence, the motor control assembly monitors a signal which indicates the speed of the disc file motor.

3-4 POWER DISTRIBUTION

External three-phase ac power is applied to the power distribution panel through an rf filter assembly. The ac power passes directly from the power distribution panel to the motor control assembly. Application of ac power for the controller, selection unit, or fans may be controlled either from the operator panel of the computer or from the EP RAD storage unit. When the LOCAL/REMOTE switch on the power distribution panel is in the LOCAL position, ac power is applied directly to the PT20 power supply and the fans. When the LOCAL/REMOTE switch is in the REMOTE position, ac power is controlled from the operator control panel of the computer. A delay circuit in the power distribution panel prevents application of ac power to more than one EP RAD storage unit at a time when ac power is first applied. This delay causes a sequential application of ac power to each EP RAD storage unit, thereby minimizing starting surges. A power fail-safe circuit senses two signals derived from the ac power source and one dc signal from the PT20 power supply. Power failure causes a controlled shutdown of the EP RAD storage unit. If the EP RAD storage unit is in communication with the IOP at the time of shutdown, a signal is sent to the IOP to indicate the unusual end.

3-5 EP RAD CONTROLLER

In a computer installation, the EP RAD controller is only one of several device controllers exchanging data with the computer memory through the IOP. Two techniques are used to limit communication with the IOP to only one controller at any time: For some IOP commands, only one controller is addressed, and only the addressed controller can respond. For other IOP commands, a priority chain established by cable routing limits response to the highest priority controller that is awaiting that command.

The subcontroller portion of the EP RAD controller (figure 3-1) monitors signals from the IOP and determines if and how the EP RAD file responds to commands. The subcontroller responds to all control signals, either by passing the signals to other controllers associated with the computer installation or by returning signals to the IOP. The subcontroller controls exchange of data on the eight-bit data path. The expanded interface circuits provide up to 24 additional data lines when a 16-bit or a 32-bit data path is used. When the EP RAD file is operating offline, signals are received from the Peripheral Equipment Tester (PET) Model 7901 through the PET interface.

Commands from the IOP cause phase control circuits of the data buffer to cycle through a definite sequence of phases. During each phase of the sequence, the phase control circuits respond to IOP signals, selection unit signals, and internally generated signals to determine when to go from one phase to another. During this sequence of phases, data is transferred between the selection unit and the IOP through the data buffer, the selection unit interface, and the subcontroller and expanded interface circuits.

3-6 IOP INTERFACE

The response of the subcontroller to IOP commands is summarized in figure 3-3. The five commands associated with CPU instructions are as follows:

Mnemonic	Function
AIO	Acknowledge input/output interrupt
HIO	Halt input/output operation
TDV	Test device
TIO	Test input/output
SIO	Start input/output

The acknowledge service call (ASC) command is generated by the IOP in response to a service call from the subcontroller.

3-7 AIO Command

The AIO command, which is generated by the IOP when an interrupt is detected, is not addressed to any device or device controller. Only the highest priority device controller with an interrupt pending can respond to the AIO command. Any device controller without an interrupt pending passes the signals to the next device controller in the priority sequence. If the EP RAD controller is the highest priority device controller with an interrupt pending, it responds to the AIO command by transmitting its address and the contents of its device address register (U-register) to the IOP and by transmitting signals that indicate the cause of the interrupt. When an AIO command is accepted, the interrupt condition is cleared.

3-8 HIO Command

The HIO command, which is addressed to a specific device controller, halts an input/output operation being processed by the EP RAD controller and returns function response signals and condition code signals to the IOP. These signals indicate the status of the EP RAD controller to the IOP and the CPU.

3-9 TDV Command

The TDV command, which is addressed to a specific device controller, returns function response signals and condition code signals to the IOP. These signals indicate any errors

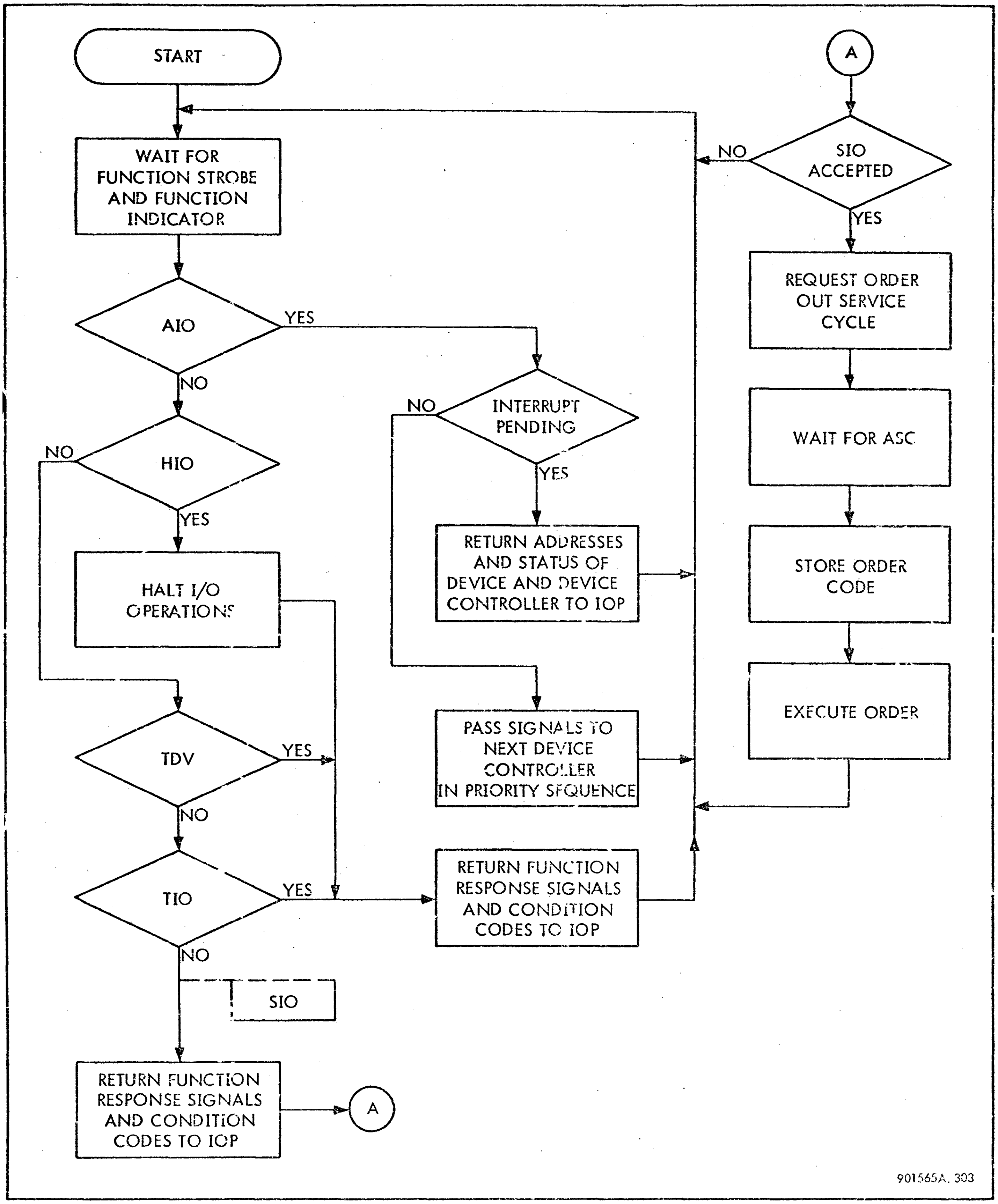


Figure 3-3. Response to IOP Commands, Flow Diagram

that occur during an input/output operation and the nature of any detected errors.

3-10 TIO Command

The TIO command, which is addressed to a specific device controller, returns function response signals and condition code signals to the IOP. These signals indicate the status of the EP RAD controller to the IOP and the CPU. The TIO command performs a function similar to that of the HIO command, without causing a halt.

3-11 SIO Command

The SIO command, which is addressed to a specific device controller, returns function response signals and condition code signals to the IOP. These signals indicate the status of the EP RAD controller to the IOP and the CPU. In addition, the SIO command starts an input/output operation if the EP RAD file is ready. The first response is to request an order out service cycle from the IOP. During this service cycle, a code for one of five orders (seek, sense, read, write, or checkwrite) is stored in the order register of the EP RAD controller. A sequence of ASC commands in response to service calls from the EP RAD controller then causes the order to be executed.

3-12 INTERNAL OPERATIONS

In response to an AIO, HIO, TIO, TDV, or SIO command from the IOP, the EP RAD controller gathers data available in registers and flip-flops of the controller, or from signals available at the selection unit interface, and transmits the data to the IOP as function response signals or condition code signals. If an SIO command is accepted, the I/O operation that results depends on the order received during the order out service cycle. For each order, the IOP responds to a sequence of service calls from the EP RAD controller by generating ASC commands. Each service call is identified by a two-bit code as requesting one of the four types of service cycles listed in table 3-1.

Regardless of the order received, a specific number of bytes are exchanged as the phase control circuits of the data buffer cycle through a definite sequence of phases. If a seek order is stored, subsequent data out service calls cause two bytes of data to be stored in controller registers. If a sense order is stored, subsequent data in service calls cause three bytes of data to be transmitted to the IOP. If a write order is stored, subsequent data out service calls cause data bytes in memory to be stored in the disc file. If a read order is stored, subsequent data in service calls cause data from the disc file to be stored in memory. If a checkwrite order is stored, data accepted from memory is compared with data read from the disc file. During or following execution of any of these orders, terminal order data may be received from the IOP or an order in service call may cause data to be sent to the IOP.

Table 3-1. Service Cycle Operations

Service Cycle	Operation
Order out	Control information is transmitted from the IOP to the controller. First service cycle of any input/output operation
Order in	Control information is transmitted from the controller to the IOP. Last service cycle of any input/output operation
Data out	Data is transmitted from the computer memory through the IOP to the disc file. Four bytes of data are transmitted during each service cycle; therefore, a rapid sequence of service cycles is required during execution of a write order or a checkwrite order. For a seek order, two data out service cycles are required
Data in	Data is transmitted from the disc file through the IOP to the computer memory. Four bytes of data are transmitted during each service cycle; therefore, a rapid sequence of service cycles is required during execution of a read order. For a sense order, three data in service cycles are required

3-13 Seek Order

A diagram that summarizes the transfer of data into the EP RAD controller during the execution of a seek order is presented in figure 3-4. During execution of a seek order, two bytes of data are stored in the track address register (T-register) and the sector register (S-register). Execution of a subsequent read order, write order, or checkwrite order begins at this location in the disc file. (When no seek order is used, operations begin at the location stored in the T-register and S-register at the time that the order is received.)

A byte of data is first accepted from the IOP and is stored in the I-register. As this byte is transferred to the J-register, an additional byte is requested from the IOP. Bits 1 through 7 of the first byte are stored in the higher order flip-flops of the T-register. After the second byte is moved from the I-register to the J-register, the four higher order bits (bits 0 through 3) of the second byte are placed in the lower order flip-flops of the T-register, and the four lower order bits (bits 4 through 7) are placed in the S-register.

The byte counter of the controller identifies the bytes received and generates timing signals which control the transfer of data from the J-register. An incorrect length signal is generated by the controller if a byte count other than two is specified in the I/O doubleword associated with the seek order.

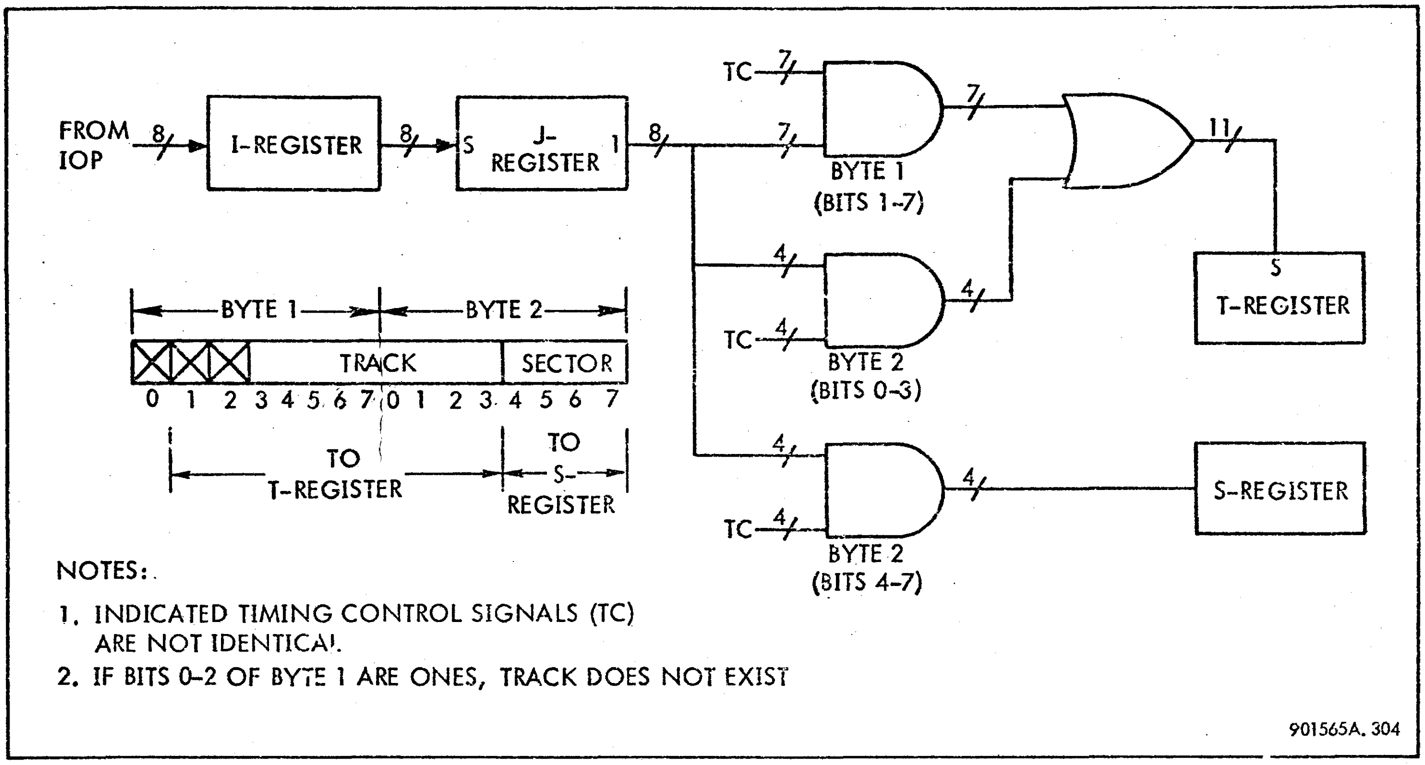


Figure 3-4. Seek Order Data Path, Block Diagram

3-14 Sense Order

Figure 3-5 summarizes the transfer of data from the EP RAD controller during execution of a sense order. Three bytes of data are transferred from the EP RAD controller to the computer memory through the IOP. The sense order is used to speed up input/output operations by permitting the CPU program to determine the location available before starting a transfer of data. The average waiting time of half a disc revolution can thereby be reduced to one sector time.

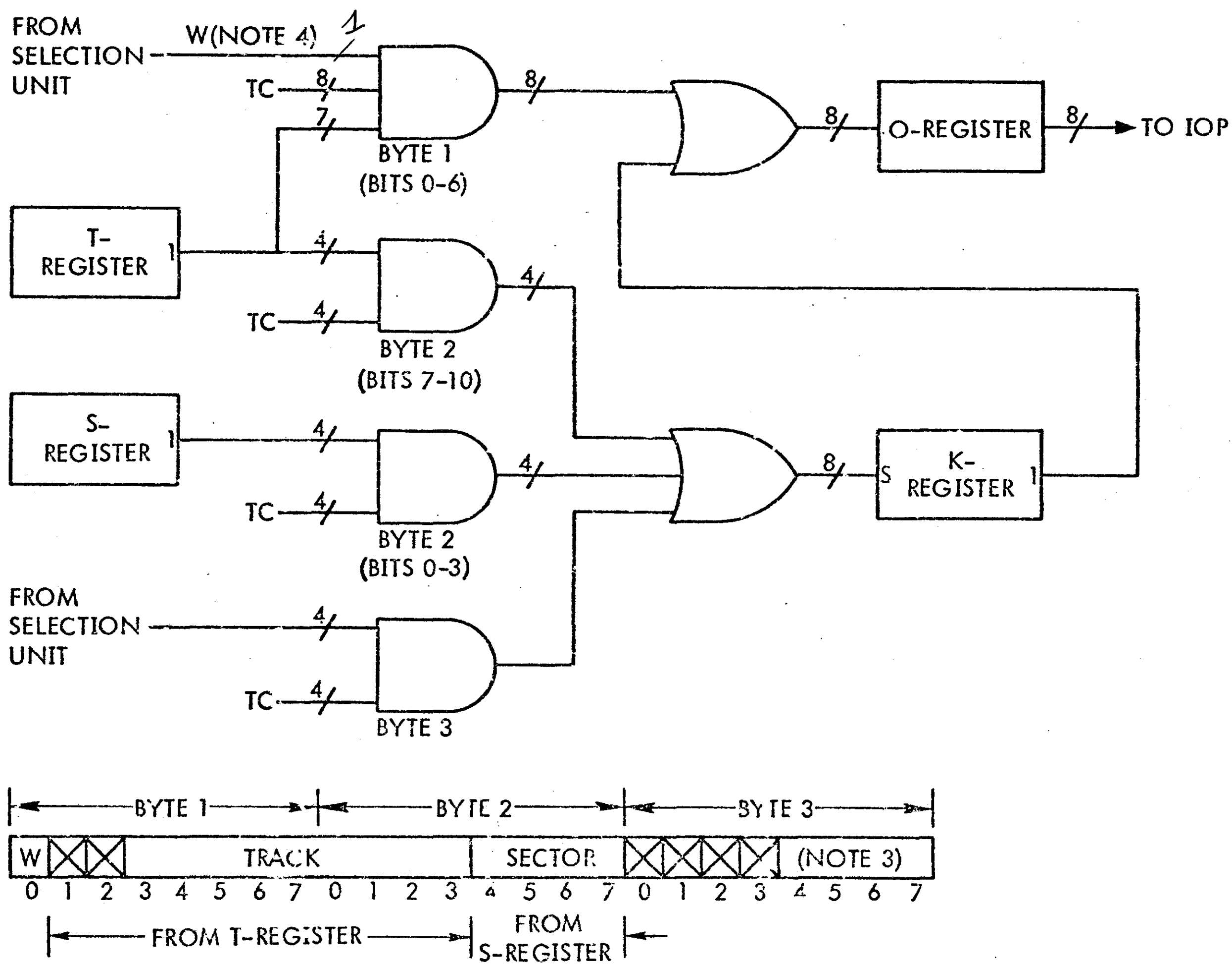
The first byte of data to be stored in the O-register consists of bits 0 through 6 from the track address register (T-register) and one bit from the selection unit. The bit from the selection unit indicates whether the addressed track is write-protected. The second byte of data consists of bits 7 through 10 from the T-register and four bits from the sector register (S-register). The bits from the T-register are stored in bits 0 through 3 of the K-register; the bits from the S-register are stored in bits 4 through 7 of the K-register. This byte is transferred to the O-register after the first byte is accepted from the O-register by the IOP. The third byte of data consists of four unused bits and four bits which indicate the address of the sector currently under the read/write heads of the disc file. (The bits in the S-register indicate the sector addressed by the EP RAD controller.) The third byte, in its turn, is transferred to the O-register, then to the IOP.

The byte counter of the controller identifies the bytes received and generates timing signals which control transfer of data from one register to another. Transfer of data from the O-register to the IOP is controlled by the phase control circuits. An incorrect length signal is generated by the controller if a byte count other than three is specified in the I/O doubleword associated with the sense order. A sector unavailable signal is generated if the T-register and S-register have incremented beyond the last available sector.

3-15 Write Order

A diagram that summarizes data transfers within the EP RAD controller during execution of a write order is presented in figure 3-6. During execution of a write order, data bytes for an integral number of sectors are transferred from the computer memory to the disc file through the IOP, the controller, and the selection unit. (If less than 1024 data bytes are transferred for a sector, bytes consisting of eight zeros (0000 0000) are written until the sector is complete.) All 1024 data bytes for each sector are written the first time the addressed sector passes under the read/write heads. If a write operation is attempted in a write-protected track, the write order is not executed and the write-protect violation is reported to the IOP.

Four bytes of data are accepted by the I-register during each data out service cycle. For an eight-bit data path from the IOP, one data byte is accepted and transferred to the J-register before the next data byte is requested. For a 16-bit or 32-bit data path from the IOP, two or four bytes are accepted simultaneously. Each byte is moved to

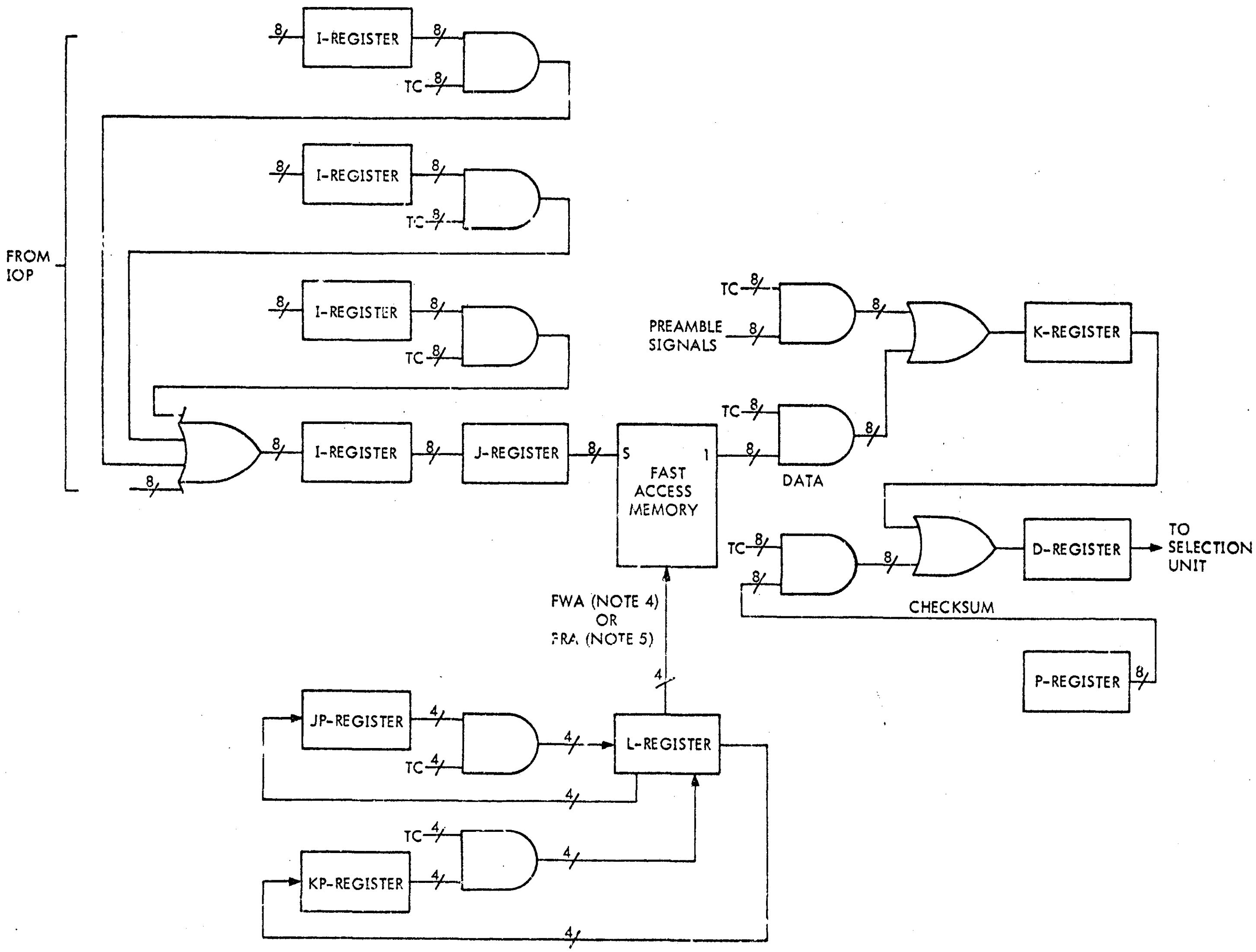


NOTES:

1. INDICATED TIMING CONTROL SIGNALS (TC) ARE NOT IDENTICAL
2. IF BITS 1 AND 2 OF BYTE 1 ARE ONES, SECTOR IS UNAVAILABLE
3. SELECTION UNIT PROVIDES 4 BITS, WHICH INDICATE CURRENT SECTOR AT READ/WRITE HEADS
4. SELECTION UNIT PROVIDES W BIT, WHICH INDICATES IF TRACK IS WRITE-PROTECTED (W = 1 IF WRITE-PROTECTED)

901565A.305

Figure 3-5. Sense Order Data Path, Block Diagram



NOTES:

1. IOP DATA PATH MAY BE 8, 16 OR 32 BITS WIDE
2. JP-REGISTER, KP-REGISTER AND L-REGISTER CONTROL ACCESS TO 16 REGISTERS IN FAST ACCESS MEMORY
3. INDICATED TIMING CONTROL (TC) SIGNALS ARE NOT IDENTICAL
4. FWA IS 4-BIT FAST MEMORY WRITE ADDRESS
5. FRA IS 4-BIT FAST MEMORY READ ADDRESS

901565A.306

Figure 3-6. Write Order or Checkwrite Order Data Path, Block Diagram the higher order byte of the I-register and is transferred to the J-register before additional data bytes are requested.

Data bytes in the J-register are transferred to the fast access memory (FAM) module under control of the J-pointer register (JP-register) and timing circuits. The FAM module contains 16 addressable eight-bit registers. The JP-register stores a four-bit code which addresses one of the 16 registers. A byte transferred from the J-register to the FAM module is stored in the location addressed by the L-register. After a byte is stored in the FAM module, the number in the JP-register is incremented. The incrementing process is accomplished by causing the outputs of the L-register to generate a code next in binary sequence to the code stored in the JP-register. In the FAM write cycle, a data byte is transferred from the J-register to an addressed register in the FAM module, and the incremented address is transferred from the L-register to the JP-register.

Data bytes in the FAM module are read into the K-register under control of the K-pointer register (KP-register) and timing circuits. The KP-register is incremented by reading the outputs of the L-register during a FAM read cycle in which data is read from the addressed register in the FAM module into the K-register. The L-register stores a four-bit code which addresses one of the 16 registers in the FAM module.

Data stored in the K-register is transferred to the D-register one byte at a time. Data stored in the D-register is transferred serially through the selection unit to the addressed track and sector of the disc file. This data transfer takes place at a clock rate established by timing circuits in the controller. Execution of a write order requires control of independently timed data transfers. Transfer of data from the IOP to the I-register is dependent on the speed of response of the IOP to a service call from the controller. Since transfer of data from the D-register to the disc file must keep pace with the clock signals generated in the controller, the FAM module must have data available for the K-register in time for transfer to the D-register. Additional circuits associated with the data path monitor and control the process so a continual flow of data takes place. The phase control circuits and associated timing circuits regulate the process of data transfer from the IOP to the I-register into the J-register.

The RK-counter keeps count of the number of active bytes in the FAM module. Each time a byte is written into the FAM module, the count is decreased by one; each time a byte is read from the FAM module, the count is increased by one. Signals controlled by the RK-counter request a FAM write cycle whenever the number of active bytes is 8 or less. Signals generated within the controller indicate whether the J-register or K-register is filled. The K-register takes priority when the K-register is not filled (thereby causing a request for reading data from the FAM module to the K-register), and the J-register is filled (thereby causing a request for writing data from the J-register into the FAM module). This priority assures that a byte is always available for the D-register. The FAM module is kept filled by storing a large number of bytes initially and by retaining service connect status with the IOP for a period long enough to store 8 to 12 bytes or to fill the FAM module, whichever is required.

The writing process includes writing a preamble and postamble in addition to the 1024 data bytes (figure 3-2). This sequence is controlled by timing circuits associated with the selection unit interface. After a write order is stored, a search is conducted for the addressed track and sector. The bit and byte counter (B-counter) then controls the sequence of storing the preamble codes in the K-register, counting the 1024 data bytes, and storing the checksum in the K-register following the last data byte. The checksum is developed in the P-register while the data bytes are being transferred from the D-register to the selection unit.

While the gap separating each sector on the disc file is under the read/write heads, an incrementing process takes place between the T-register and S-register, and the P-register. If data is to be written into the next sector, the number in the S-register must be increased by one so that a match between the S-register code and the selection unit sector signal code is possible. If the S-register contains the code 1011, which identifies sector 11, the next code in sequence must be 0000 and the track address in the T-register must be increased by one. Therefore, the contents of the T-register and the S-register are temporarily stored in the P-register. This value is incremented by one in the process of return to the S-register and the T-register, so that these two registers contain the correct codes before the next sector is available. The contents of the T-register are also transmitted to the selection unit by way of the P-register.

The technique used for encoding the sequence of bits on the magnetic surface of the disc is known by various names (such as Manchester, modified nonreturn-to-zero, frequency modulation, and Ferranti). The technique (called Manchester encoding in this manual) has the advantage that a separate clock track is not required on the magnetic surface and that a clock signal can be extracted from the data signal as data is read from the magnetic surface. (The separate sector pulse track and index pulse track do not provide a clock for each bit.) In summary, during errorless execution of a write order, the following operations take place:

a. Immediately following storage of the write order, at least eight data bytes are accepted from the IOP into the I-register and are transferred through the J-register into the FAM module.

b. A search for the addressed sector is conducted. After the addressed location is found, the B-counter is used to control storage of the preamble in the K-register. This preamble is transferred in parallel to the D-register eight bits at a time and is transmitted from the D-register to the selection unit in serial format.

c. After the preamble code has been transferred from the K-register, data bytes are read from the FAM module into the K-register and are transferred from the K-register to the D-register for transmission to the selection unit. Data bytes are continually accepted from the IOP through the I-register and the J-register and are stored in the FAM module. The RK-counter keeps track of the number of active bytes in the FAM module. The B-counter keeps track of the number of data bytes which have been written. If less than 1024 data bytes are received from the IOP, data bytes of all zeros are written until a total of 1024 bytes is stored.

d. A checksum developed in the P-register is transferred to the K-register following the last data byte. After the checksum is transferred, the P-register is used to increment the track address and sector address to prepare for writing in the next sector, if necessary. (If the write order is ended, the track address and sector address are retained until a new order is executed or until a seek order is used to store a new track address and sector address.)

3-16 Read Order

A summary of data transfers within the EP RAD controller during execution of a read order is presented in figure 3-7. During a read order, data bytes for an integral number of sectors are transferred from the disc file to the computer memory through the selection unit, controller, and IOP. All 1024 data bytes for each sector are read the first time the addressed sector passes under the read/write heads. Two types of read orders are possible: a sector read order and a record read order. For a sector read order, a parity error is reported to the IOP at the end of a sector in which the error occurred; for a record read order, a parity error is reported to the IOP after a count done terminal order is received by the controller.

After the read order is stored, a search for the addressed sector is conducted. When the addressed sector is found, the timing circuits of the controller must by synchronized with clock signals transmitted from the selection unit. These clock signals are derived from the Manchester encoded data. The preamble, which is initially a sequence of ones and zeros (...0101010...), develops an easily identifiable clock signal to indicate the start of data written in a sector. A synchronization pattern of 1100 ends the preamble and identifies the clock immediately preceding the 1024 data bytes.

Bits are read serially from the selection unit into the D-register. Only data bytes are transferred to the J-register, one byte at a time, in the interval between the last bit of one byte and the first bit of the succeeding byte.

Data bytes in the J-register are transferred to the fast access memory (FAM) module under control of the J-pointer register (JP-register) and timing circuits. The FAM module contains 16 addressable eight-bit registers. The JP-register stores a four-bit code which addresses one of the 16 registers. A byte transferred from the J-register to the FAM module is stored in the location addressed by the L-register. After a byte is stored in the FAM module, the number in the JP-register is incremented by causing the outputs of the L-register to generate a code next in binary sequence to the code stored in the JP-register. In the FAM write cycle, during which a byte is transferred from the J-register to an addressed register in the FAM module, the incremented address is transferred from the L-register to the JP-register.

Data bytes are read from the FAM module under control of the K-pointer register (KP-register) and timing circuits. The KP-register is incremented by reading the outputs of the L-register during a FAM read cycle in which data is read from the addressed FAM module location. The L-register stores a four-bit code which addresses one of the 16 registers in the FAM module. The procedure is similar to that for a FAM write cycle. The RK-counter keeps count of the number of active bytes in the FAM module. Each time a byte is written into the FAM module the count is increased by one; each time a byte is read from the FAM module, the count is decreased by one. Signals generated within the controller indicate whether the J-register or the K-register is filled. If the K-register is not filled (thereby causing a request for reading data from the FAM module) and the J-register is filled (thereby causing a request for writing data from the J-register into the FAM module), the J-register takes priority. This priority assures that a byte available in the D-register is accepted by the FAM module before the selection unit transmits the first bit of the next byte.

Each time that the FAM module stores four data bytes, an order in service cycle is requested by the controller. If more than eight data bytes are stored in the FAM module, the controller requests two successive order in service cycles without relinquishing control of the I/O channel. The means for transfer of data from the FAM module to the O-register depends on the path width of the I/O channel. The phase control circuits and the associated timing circuits regulate the process of data transfer from the O-register to the IOP.

For an eight-bit data path, bytes are read from the FAM module to the K-register, then to the higher-order byte of the O-register. The IOP accepts the data from the O-register. For a 16-bit data path, the first byte is read from the FAM module to the K-register, and the second byte is read from the FAM module into the next-to-higher order byte of the I-register. After two bytes have been counted, they are transferred simultaneously to the O-register. For a 32-bit data path, the first byte is read from the FAM module to the K-register, and the second byte is read from the FAM module to the next-to-higher order byte of the I-register, as for the 16-bit data path. The next two bytes are read into successively lower order bytes of the I-register. After four bytes have been counted, they are

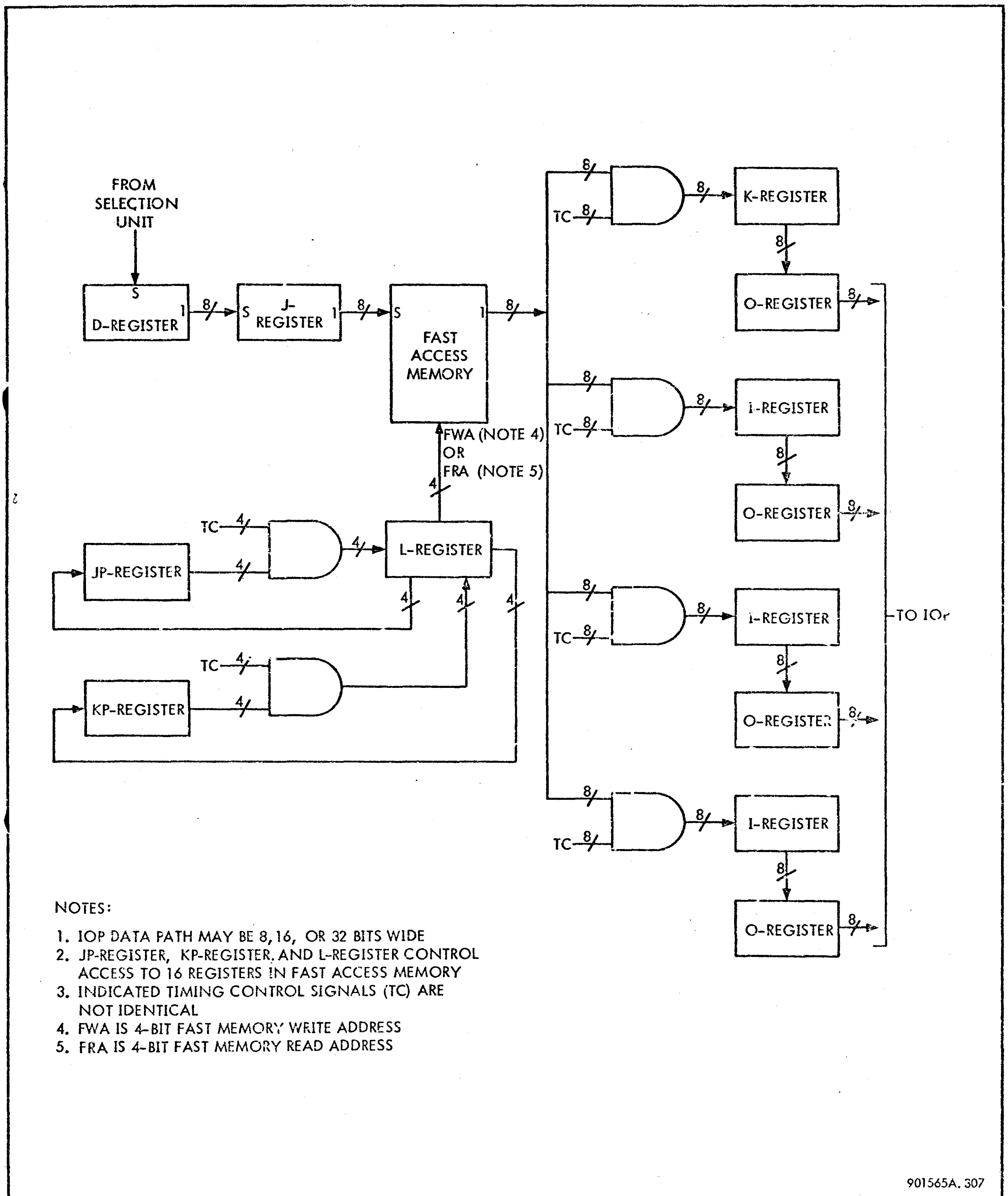


Figure 3-7. Read Order Data Path, Block Diagram

transferred simultaneously from the I-register and K-register into the O-register.

After all data bytes have been counted, stored in the D-register, and transferred, the checksum written during the write order is read from the selection unit. This checksum is compared with a checksum developed in the P-register during the read operation. If the two are not identical, an error has occurred. For a sector read order, the error is reported immediately; for a record read order, the error is reported at the end of the record. The checksum is not transferred to the FAM module.

While the gap separating each sector on the disc file is under the read/write heads, an incrementing process takes place between the T-register and S-register, and the P-register. If data is to be read from the next sector, the number in the S-register must be increased by one so that a match between the S-register code and the selection unit sector signal code is possible. If the S-register contains the code 1011, which identifies sector 11, the next code in sequence must be 0000, and the track address in the T-register must be increased by one. Therefore, after the checksum stored in the P-register is compared with the checksum read from the selection unit, the contents of the T-register and S-register are stored in the P-register. This value is incremented by one in the process of return to the S-register and T-register so that these two registers contain the correct codes before the next sector is available. The contents of the T-register are also transmitted to the selection unit by way of the P-register.

In summary, during errorless execution of a read order, the following operations take place:

a. Immediately following storage of a read order, a search for the addressed sector is conducted. When the addressed sector is found, timing signals from the selection unit control the B-counter to synchronize the selection unit circuits. The preamble code stored during the write operation identifies the beginning of data bytes.

b. Bits are received from the selection unit in serial form, stored in the D-register, and transferred in eight-bit bytes to the J-register. Data from the J-register is written into the FAM module. Service calls are requested by the controller whenever four or more active bytes are in the FAM module.

c. For an eight-bit data path I/O channel, bytes are read from the FAM module into the K-register, then to the O-register, and are accepted by the IOP from the O-register. For the 16-bit or 32-bit data paths, bytes are read from the FAM module into the K-register and I-register, transferred to the O-register, then accepted by the IOP.

d. After all data bytes have been read, a checksum developed during the read operation is compared with a checksum developed and written during the write operation. After comparison of the checksums, the P-register is used to increment the track address and sector address to prepare for reading the next sector, if necessary. (If the read order is ended, the track address and sector address are retained until a new order is executed or until a seek order is used to store a new track address and sector address.)

3-17 Checkwrite Order

Data transfer during a checkwrite order is similar to that for a write order (figure 3-6). However, data is not transferred from the D-register to the selection unit. Instead, the data that would normally be serially shifted out of the D-register to the selection unit is compared, bit-by-bit, with data read from the selection unit. The two sets of data should be identical, because the checkwrite order is used to compare data previously written and still in computer memory with data read from the same sector in which it was written.

3-18 SELECTION UNIT INTERFACE

The primary function of selection unit interface circuits is to receive signals from and to generate and transmit signals to the selection units. Signals passing between the EP RAD controller and an EP RAD selection unit are exchanged on lines common to all selection units in the EP RAD file. These signals perform the following functions:

a. Address one of eight possible selection units.

b. Identify the sector under the read/write heads of the addressed selection unit.

c. Transmit data and track address codes and associated timing signals between the controller and the selection unit.

d. Transmit status of the disc file to the controller for use in response to IOP commands.

e. Transmit sector and index identification signals.

f. Transmit signals which identify the type of order (write or read) to be executed.

3-19 EP RAD SELECTION UNIT

An EP RAD selection unit writes data on, or reads data from, the magnetic surface of the disc file in response to orders from the EP RAD controller. For each order, the controller addresses a selection unit, transmits a track address to it, and controls the process of writing or reading. (See figure 3-1.)

The controller stores a three-bit address and transmits three signals to device address circuits of all selection units. The device address circuits of the addressed selection unit generate an enabling signal which allows that selection unit to make use of the common transmission lines.

The controller transmits an 11-bit code, of which 9 bits are a track address and 2 bits are not used, to the selection unit. The write-protect logic reads the code stored in the track register and generates a signal that indicates whether the addressed track is write-protected. During execution of a read order, write order, or checkwrite order, the controller transmits this 11-bit code at the start of each sector. Signals from the track register permit only one of the 512 read/write heads of the disc file to be active. Three bits select one of eight read/write coupler circuits; six bits select the center tap of one of the 64 read/write heads associated with the selected read/write coupler circuit.

A four-bit counter in the EP RAD storage unit contains the address of the sector under the read/write heads. This counter is cleared to 0000 by the index pulse read from the sector timing track. As each sector pulse is read at the start of a new sector, the counter is incremented. After the counter has advanced from 0000 to 1011, it is cleared by the index pulse. Output signals of this counter are compared with the contents of the sector register in the EP RAD controller to determine when the addressed sector is available.

When the controller is processing a write order, it transmits a clock signal and a data signal to the write circuits. The write circuits use the Manchester encoding technique to store the data on the disc file through the selected read/write head.

When the controller is processing a read order, the read circuits extract a data signal and a clock signal from the signal originating at the selected read/write head. The data signal and the clock signal are transmitted to the controller. Additional signals from the selection unit indicate the status of the device.

SECTION IV
PRINCIPLES OF OPERATION

4-1 SCOPE AND ORGANIZATION OF SECTION

This section describes the operation of all circuits of the EP RAD file, including power distribution and control, electronic control of mechanical functions, EP RAD controller circuits, and EP RAD selection unit circuits. Descriptions of circuit operation and function are supported by logic equations, logic diagrams, flow diagrams, timing diagrams, and schematic diagrams. Individual circuits related to the transfer of data through the EP RAD file are described in a sequence that proceeds from circuits functionally close to the IOP interface to circuits functionally close to the disc file. Cross-references relate the circuit being described to circuits that provide inputs or accept outputs.

The phase sequence charts described in paragraph 4-93 include the controlling equations for changes of state, data transfers, and timing, with primary emphasis on the IOP interface. Operations related to a typical sequence of orders are described in paragraph 4-112. References to detailed descriptions of individual circuits are included. Paragraphs 4-112 and 4-93 may be used for a review of the detailed principles of operation or as a guide to the relation of the detailed circuit descriptions to the overall sequence of events during operation.

The description of offline operation in paragraph 4-83 is related to the offline tests provided in paragraph 8-11. However, only the manually controlled signals are described because operations following manual generation of control signals are identical to related online operation.

4-2 ELECTROMECHANICAL OPERATION

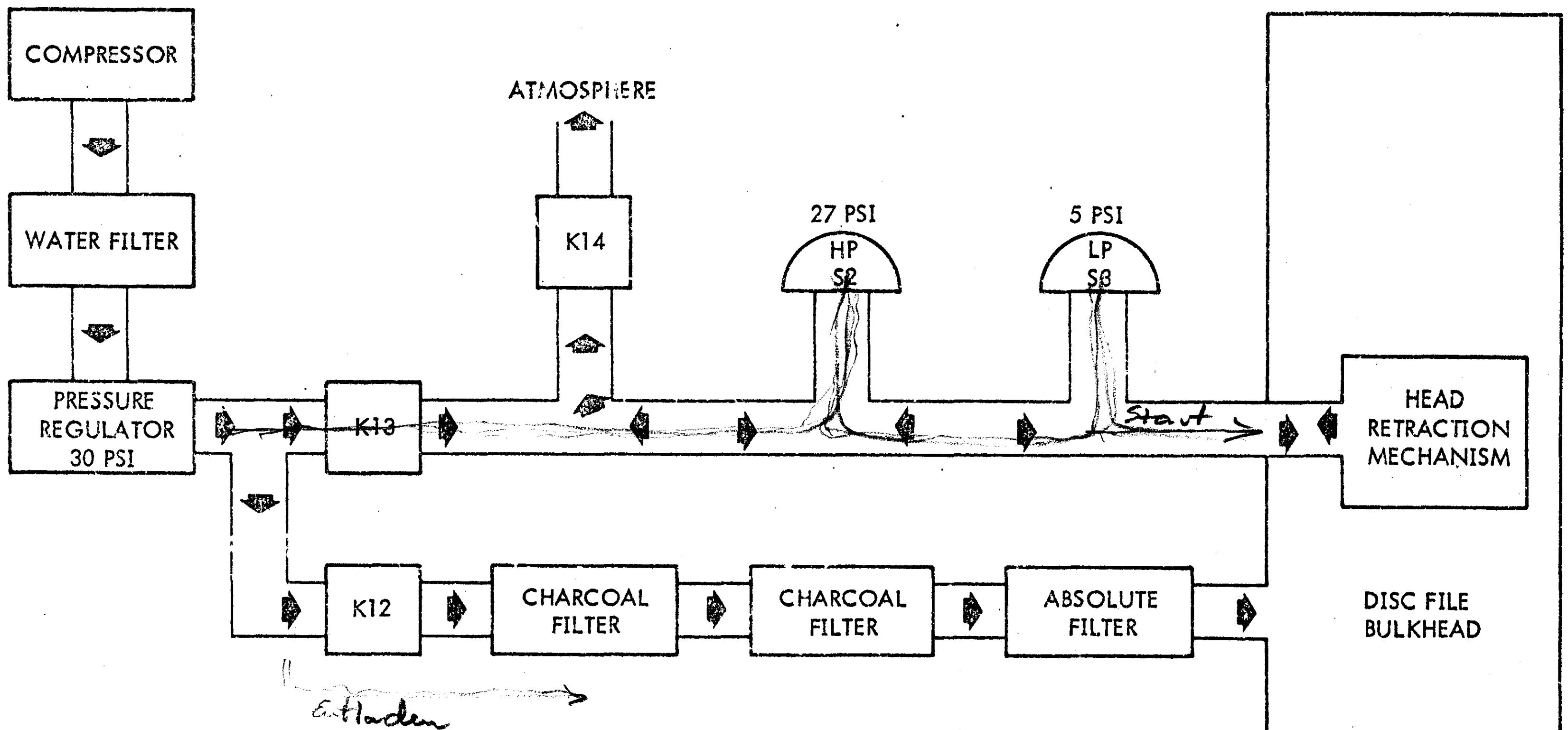
The read/write heads of the EP RAD storage unit are contained in a pressurized section of the disc file not normally serviced in the field. Spacing between the read/write heads during normal operation and start sequences is governed by the motor control assembly and the pneumatic system. During normal operation, spacing between read/write heads and a magnetic surface of the disc file is maintained by a thin film of air. During a start sequence, the read/write heads are held from the surface by a pneumatically-controlled head retraction mechanism. The pneumatic system (figure 4-1) is operated through the motor control assembly.

4-3 PNEUMATIC SYSTEM

The pneumatic system of the EP RAD storage unit maintains the disc file bulkhead at a positive pressure during normal operation. During the start sequence, the pneumatic system relieves the force holding the read/write heads against the disc file surfaces. The compressor operates whenever ac power is applied through the circuit breaker on the motor control assembly. If the POWER ON-OFF switch is OFF, relays K12 and K14 are energized and relay K13 is deenergized, so that the air in the head retraction mechanism is vented to the atmosphere and the compressor maintains the pressure in the disc file bulkhead. After the POWER ON-OFF switch is set to ON, K12 and K14 are deenergized and K13 is energized. This forces air into the head retraction mechanism to reduce the pressure of the read/write heads against the disc surfaces before the disc file motor is started. Low-pressure switch S3 closes when pressure reaches 5 psi; high-pressure switch S2 closes when pressure reaches 27 psi. At this time, power is applied to the disc file motor, and a timing circuit is started. If the disc file motor reaches 300 rpm within 4.5 seconds, K13 is deenergized and K12 and K14 are energized, venting the head retraction mechanism to atmospheric pressure. The read/write heads then ride on a thin film of air. If the 4.5-second period ends before the disc file motor reaches 300 rpm, a mechanical brake is applied, the disc file motor is stopped, and the pneumatic system returns to its initial state. If the POWER ON-OFF switch is set to OFF during normal operation, the disc file motor is stopped and the pneumatic system returns to its initial state.

4-4 MOTOR CONTROL ASSEMBLY

Circuit elements of the motor control assembly (figure 6-4) sense phase connections of the ac power source, speed of the disc file motor, pressure, and temperature. The circuits of the motor control assembly control the compressor, the disc file motor, and the mechanical brake of the disc file and provide voltage for dynamic braking. The circuit that includes transistors Q7, Q8, Q11, and T2 senses all three phases of the ac power source and connects relay K4 to ground through Q11 if the source is improperly wired or if power on any phase is lost. The circuit that includes Q1, Q2, Q3, Q4, and Q9 senses the speed of the disc file motor and provides a signal to other circuits when the speed reaches 300 rpm (nominal). The circuit that includes Q5, Q6, and Q10 is a timing circuit that connects K4 to ground 4.5 seconds after a trigger signal is received. The circuit that includes SCR1, SCR2, and SCR3 provides dc voltage for dynamic braking. This voltage is applied to the disc file motor through contacts T1 and L1 of K6. The mechanical brake is controlled by +50V power applied through contacts of relay K4. Low-pressure switch S3 closes at 5 psi; high-pressure switch S2 closes at 27 psi. If the disc file becomes overheated (greater than 130°F, nominal), the thermostat closes, connecting K4 to ground.



NOTES:

1. PATH TO HEAD RETRACTION MECHANISM CLOSED WHEN K12 AND K14 DEENERGIZED
2. PATH TO DISC FILE BULKHEAD CLOSED WHEN K12 AND K14 ENERGIZED

901565A.416

Figure 4-1. Pneumatic System, Simplified Block Diagram

Circuits of the motor control assembly control the application of ac power to the disc file motor, prevent the operation of the disc file motor if it does not reach 300 rpm within 4.5 seconds after application of power, control the pneumatic system to prevent damage to the read/write heads or to the magnetic surfaces, monitor speed and temperature during normal operation, and control the stop sequence. The order of events during a start sequence is indicated in figure 4-2; timing diagrams are provided in figure 4-3. The order of events during a stop sequence is indicated in figure 4-4.

4-5 POWER DISTRIBUTION

The primary power source is connected to each EP RAD storage unit. Power can be controlled from the power distribution panel or from a remote location and is provided to the motor control assembly, the PT20 power supply, the fans, and the WT29 Power Monitor module. Power from the PT20 power supply is provided to the EP RAD controller and to the EP RAD selection unit (figure 6-2).

4-6 POWER DISTRIBUTION PANEL

The power distribution panel of each EP RAD storage unit controls the distribution of primary ac power to components within the EP RAD storage unit as well as to other EP RAD storage units. (See figure 6-1.) Three-phase 60-Hz power is always available at TB1 of an EP RAD storage unit. Application of this ac power to the disc file motor is under the control of the motor control assembly. Application of ac power to the PT20 power supply, the fans, and the power fail-safe circuit is under the control of the REMOTE-OFF-ON switch S1 of the power distribution panel.

When S1 is in the ON position, K1 is energized and ac power from phase C is applied through F1 to the primary of T1, to the PT20 power supply, and to all fans. The output of the secondary of T1 is applied to the power fail-safe circuits. (See paragraph 4-7.) After the +25V power supply of the PT20 power supply is operating, relay K3 is energized and a circuit is completed to ground through contacts K3-2, K3-3, K1-6, and K1-3. This circuit controls online/offline operations in the EP RAD controller. (See paragraph 4-83.)

When S1 is in the REMOTE position, application of ac power is controlled from the computer. When ac power from the remote source appears at the contacts of J1, time delay relay K5 is energized through J1-X, the heating element of K5, contacts K4-5 and K4-4, resistor R1, and J1-W. After the contacts of K5 close, relay K4 is energized and latched and ac power goes from J1-X to J2-X through K4-6 and K4-5. The output of J2 goes to the next EP RAD storage unit in the EP RAD file. This ac power also goes through the contacts of S1 to relay K1, causing the same sequence of events initiated when S1 is in the ON position.

4-7 POWER FAIL-SAFE CIRCUITS

Each EP RAD selection unit includes a WT29 Power Monitor module in location 4B. (See figure 6-3.) Circuits of this module sense ac outputs of the power distribution panel (ACSENSE1 and ACSENSE2) and the +25V output of the PT20 power supply (POS25SENSE). When these signals indicate normal operation, signal AOK enables a gate controlling a one-shot. If these signals indicate abnormal operation, the one-shot is triggered and remains on for 10 seconds (nominal) after normal operation has resumed. This operation causes writing to be inhibited, the selection unit to be disconnected, and any operation in process to halt. Signal AOK controls the PWERMON signal to the controller (figure 6-7).

The slow ac sensor circuit of the power monitor reads the average value of the ac signal but is insensitive to noise spikes. The fast ac sensor circuit of the power monitor responds within a fraction of a cycle to rapid changes in the ac signal. The dc sensor is triggered when the dc voltage falls below a preset level. A delay built into the circuit prevents operation during a start sequence. Waveforms for the circuit are illustrated in figure 4-5.

4-8 EP RAD CONTROLLER

4-9 SUBCONTROLLER

Each device controller (DC) communicating with an IOP (as, for example, the EP RAD controller) includes a subcontroller which provides the following circuits:

a. Relay logic and switches for placing the DC online or offline

b. Logic elements to determine priority of the DC

c. Cable drivers and cable receivers to connect the eight-bit data path interface

d. Switches for establishing the address of a DC and for providing a means of comparing the DC address generated by the IOP with the address of the DC

e. A flip-flop that, when set, indicates that the device is connected for service through the DC

Not all possible functions of the subcontroller are used in each DC. Subcontroller function used by the EP RAD controller are described in paragraphs 4-10 through 4-19.

The subcontroller consists of the following modules incorporated in the EP RAD controller to interface with the IOP:

Location	Module Type
C23	LT25 Special Purpose Logic Module
C24	LT26 Switch Comparator Module
C26	AT17 Special Purpose Logic Module
C27	LT24 Special Purpose Logic Module
C28	AT10 Cable Receiver Module
C29	LT41 Special Purpose Logic Module
C30	AT11 Cable Receiver/Driver Module
C31	LT43 Special Purpose Logic Module
C32	AT12 Cable Driver Module

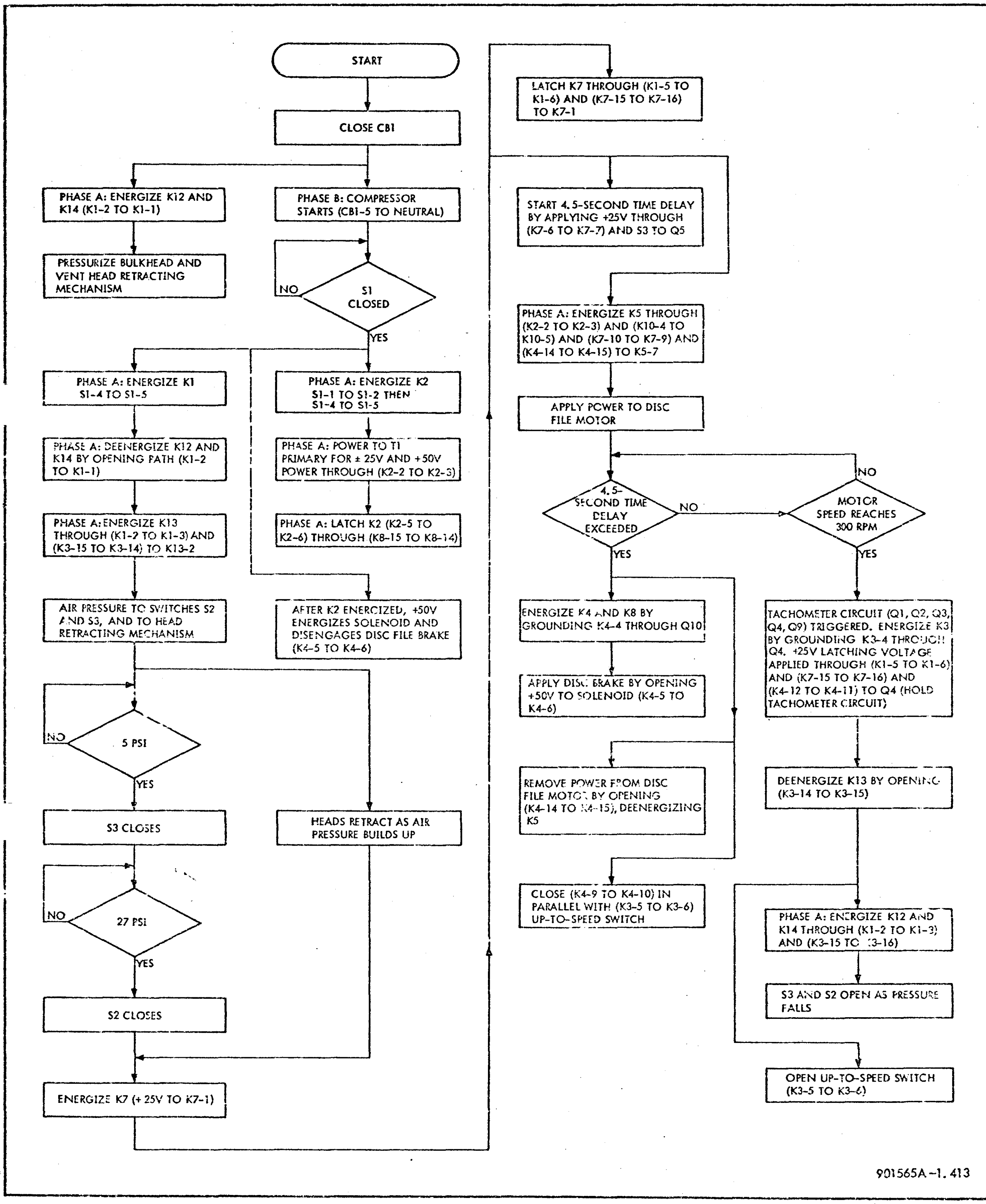


Figure 4-2. Motor Control Assembly Start Sequence, Flow Diagram

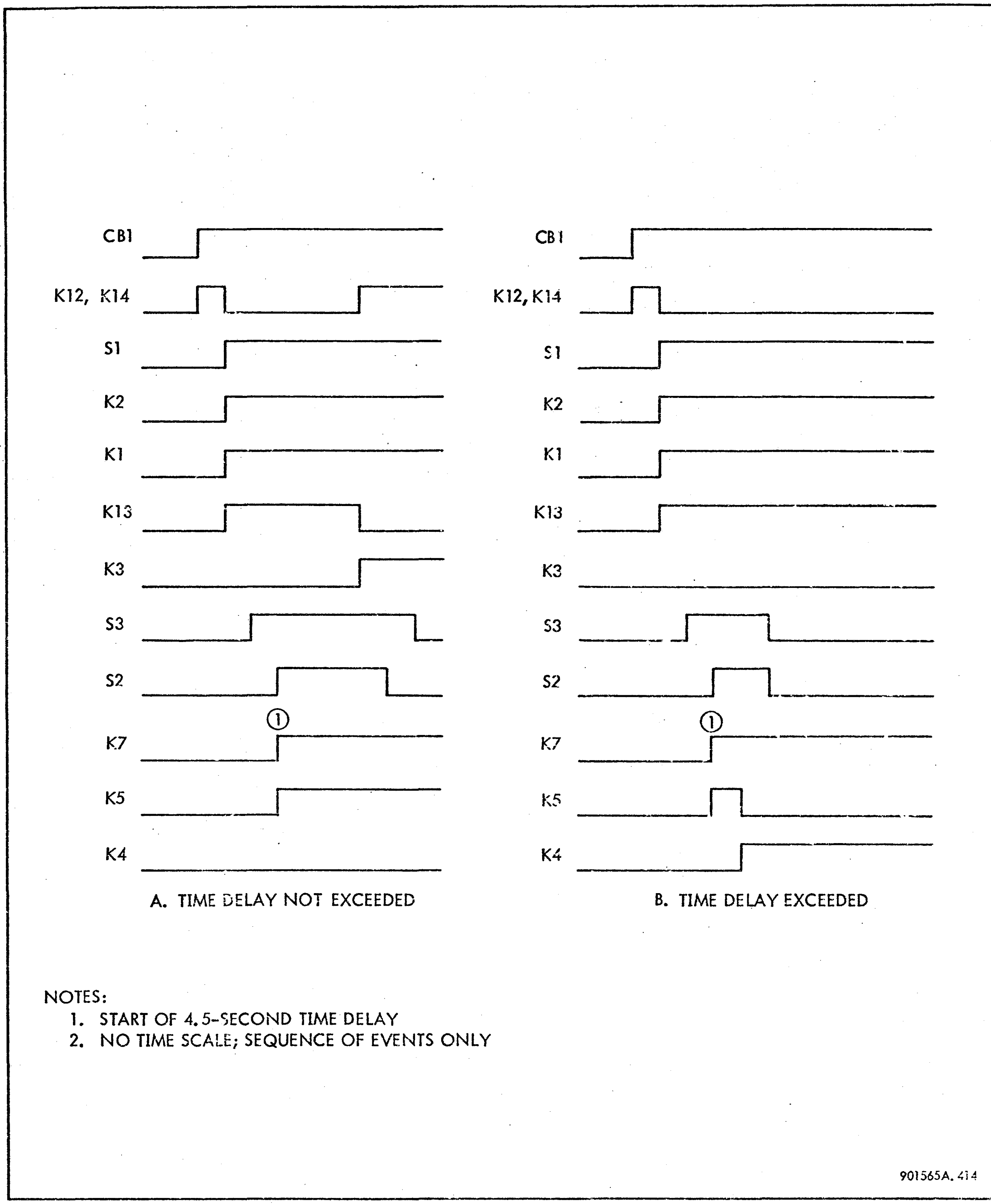


Figure 4-3. Motor Control Assembly Start Sequence, Timing Diagram

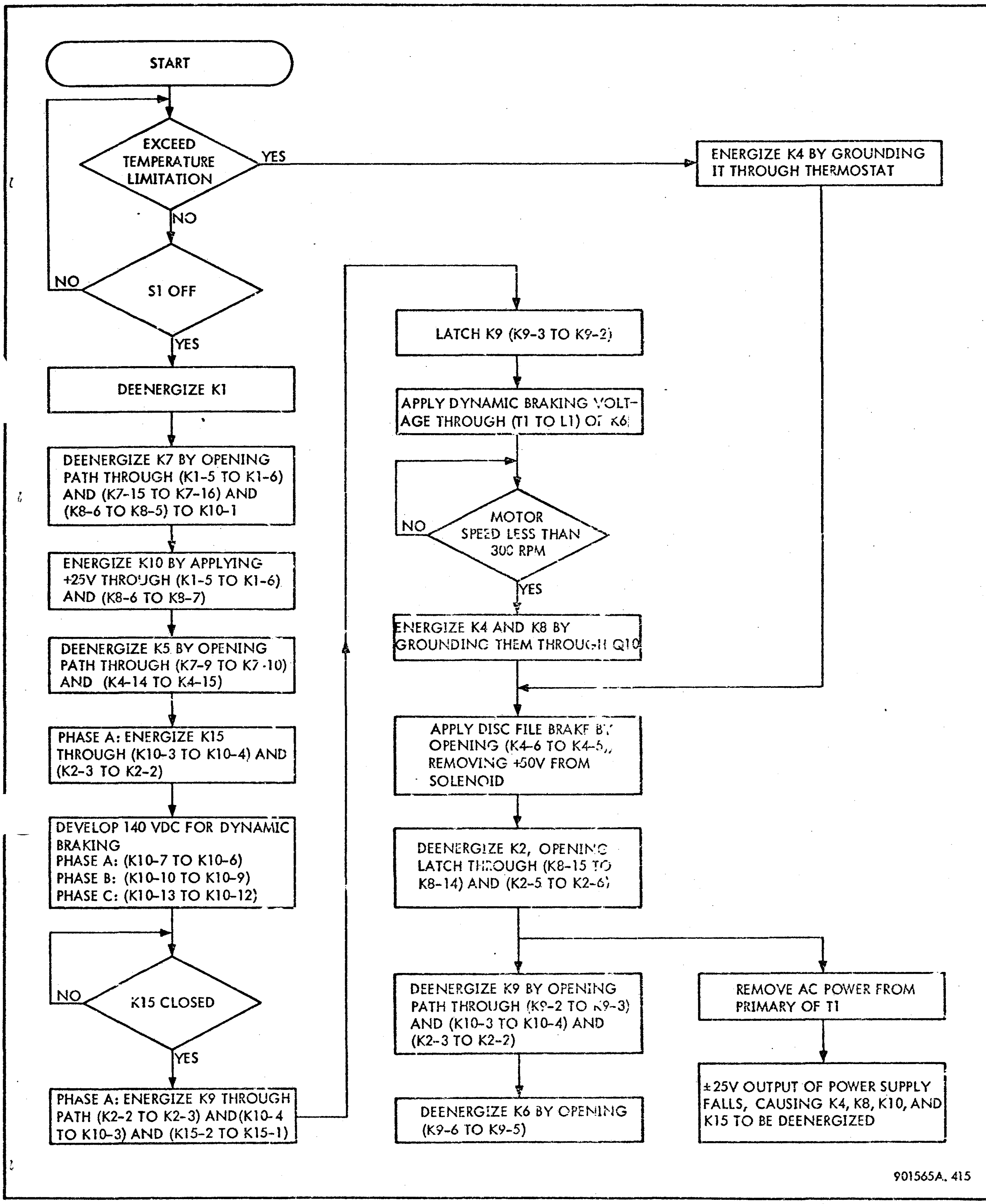
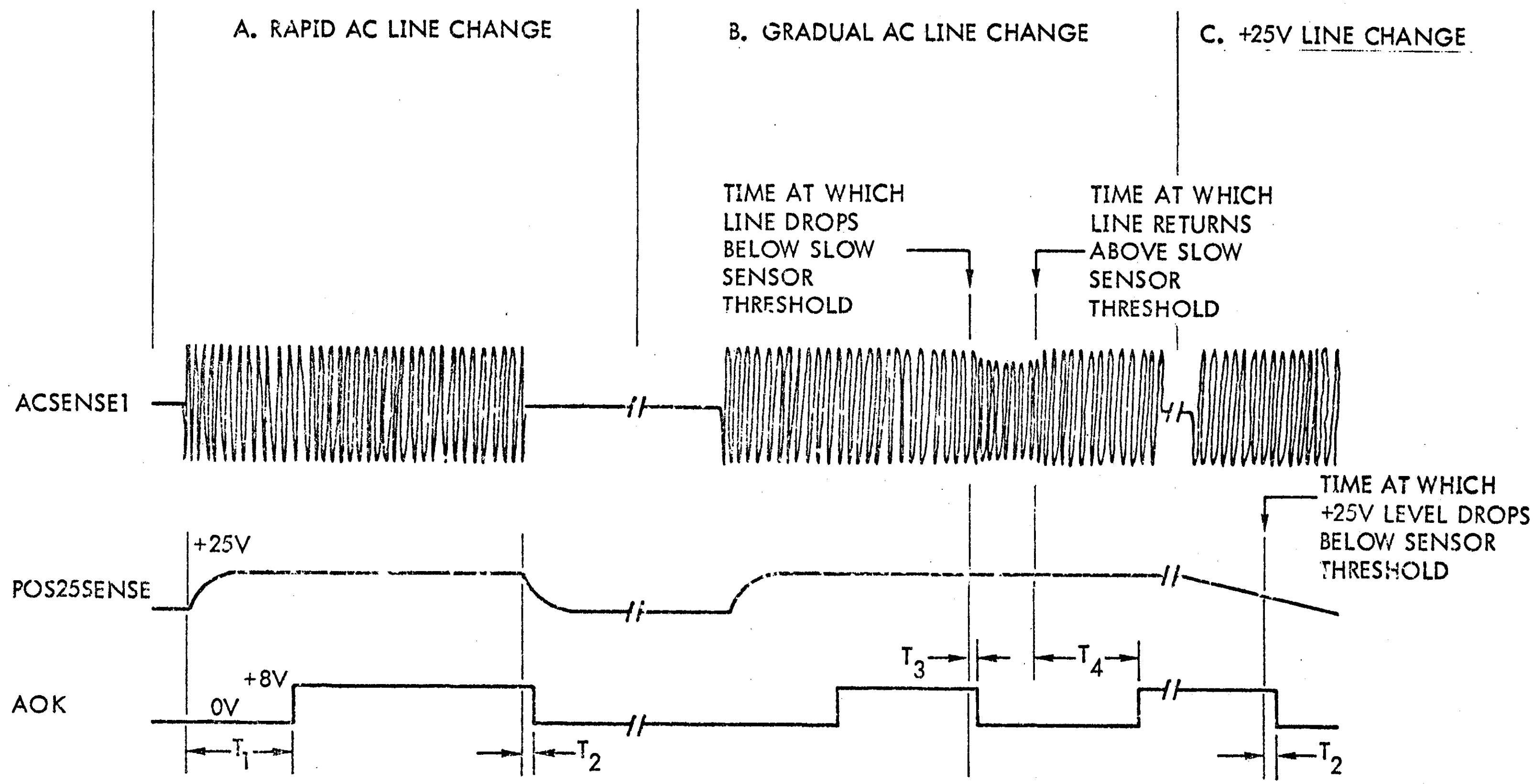


Figure 4-4. Motor Control Assembly Stop Sequence, Flow Diagram



NOTES:

1. $T_1 = T_4 = 300 ^{+100}_{-0}$ MS = TURN ON DELAY
2. T_2 = 1 MS MAX = FAST AC SENSOR AND DC SENSOR RESPONSE
3. T_3 = 5 ± 1 MS = SLOW AC SENSOR RESPONSE

901565A. 417

Figure 4-5. WT29 Power Monitor Module, Typical Waveform

4-10 Function Strobe and Function Indicators

The subcontroller can respond to a function strobe signal /FS/ accompanied by one of the following function indicator signals:

Function Indicator	Function
AIOR	Acknowledge interrupt call
ASCR	Acknowledge service call
HIOR	Halt input/output
SIOR	Start input/output
TDVR	Test device
TIOR	Test input/output

The HIO, SIO, TDV, and TIO functions are always addressed to a specific DC, and only the subcontroller associated with the addressed DC can respond. The AIO and ASC functions are not addressed to a specific DC, and each subcontroller associated with an IOP receives the function strobe and function indicator in a priority sequence established by cable connections. If a subcontroller in a DC does not respond, the AIOR or ASCR function indicator enables the subcontroller of the next DC in the priority sequence to respond. If the subcontroller does respond, it acknowledges the function strobe and generates function response signals, condition code signals, and other signals related to the function.

The HIOR, SIOR, TDVR, and TIOR function indicator signals are generated when the CPU processes an instruction. The AIOR function indicator signal is generated in response to an interrupt call by a DC (as, for example, the EP RAD controller).

ICD = LIL

LIL = NAIOR INC CIL (True when CIL set)
+ AIOR INI LIL NRSTR (Latched until AIOR false)

The conditions for which flip-flop CIL is set are described in paragraph 4-34.

The ASC function indicator signal is generated in response to a service call by a DC.

SCD = LSL

LSL = NASCR INC SCN (True when SCN set)
+ ASCR INI LSL NRSTR SCN (Latched until ASCR false)

The conditions for which flip-flop SCN is set are described in paragraph 4-32.

4-11 IOP Data Line Signals

The IOP data line signals consist of DA0R through DA7R, which may contain an address or terminal order information. (During execution of orders, these lines transmit data bytes.)

Signals DA0R through DA3R are compared with the settings of the switches on the LT26 Switch Comparator module to generate device controller addressed signal DCA.

DCA = N(DA3R NSWA3 + NDA3R SWA3
+ NDA2R SWA2 + DA2R NSWA2
+ DA1R NSWA1 + NDA1R SWA1
+ DA0R NSWA0 + NDA0R SWA0)

If any pair of corresponding bits of the DAnR inputs and the SWAn inputs (where n represents any integer from 0 to 3) are different, signal DCA is false; therefore, signal DCA is true when the IOP data line code is identical to the address code set in the switches, indicating that the device controller is addressed.

Signals DA5R through DA7R contain the device address code and control signals SU0D through SU2D.

SU0D = DA5R IOP + ...

SU1D = DA6R IOP + ...

SU2D = DA7R IOP + ...

For terminal orders, signals DA0R through DA3R indicate interrupt, count done, command chaining, or IOP halt, as described in detail in paragraph 4-34.

4-12 Priority Signals

Signals HPI, HPS, LIL, LSL, AVI, and AVO control priority when the EP RAD controller is online. The IOP generates an AVIR signal that is always true. This signal goes to the highest priority device controller at all times. When the IOP generates a true function strobe signal (FSR), each DC, beginning with the highest priority DC, responds to the AVIR signal in priority sequence. If a DC does not generate a function strobe acknowledge signal, the DC passes the AVIR signal on to the next DC in sequence in the form of a true AVOD signal.

In the EP RAD controller, a true AVOD signal is generated in one of three ways.

AVOD = AVIR FSR AIOR NAIOM (AIO function)
+ AVIR FSR ASCR NASCM (ASC function)
+ AVIR FSR NDCA TTSH (TDV, TIO, SIO, or HIO function)

TTSH = TDVR + TIOR + SIOR + HIOR

For an AIOR function indicator, a true AVOD signal is generated if either interrupt flip-flop CIL is reset or if high priority interrupt bus HPI is at the true level.

AVOD = AVIR FSR AIOR NAIOM + ...

AIOM = NHPIL LIL + LIH

HPIL = NAIOR HPIR + AIOR HPIL

LIL = NAIOR INC CIL
+ AIOR INI LIL NRSTR

LIH = NAIOR INC CIL GND
+ AIOR INI NRSTR LIH } Always false

For a service call function indicator (ASCR), a true AVOD signal is generated if service call flip-flop SCN is in the reset state or if high priority service signal HPSR is at the true level.

AVOD = AVIR FSR ASCR NASCM + ...

ASCM = NHPSL LSL + LSH

HPSL = NASCR HPSR + ASCR HPSL

LSL = NASCR INC SCN
+ ASCR INI LSL NRSTR SCN

LSH = NASCR INC SCN GND
+ ASCR INI LSH NRSTR SCN } Always false

For all other function indicators (TDVR, TIOR, SIOR, or HIOR), a true AVOD signal is generated if the device controller is not addressed.

AVOD = AVIR FSR NDCA TTSH + ...

TTSH = TDVR + TIOR + SIOR + HIOR

DCA = Device controller addressed

4-13 Subcontroller Response

When the subcontroller does not generate a true AVOD signal, it generates a true function strobe acknowledge signal, regardless of the type of function indicator. The conditions which control PHFSL are described in paragraphs 4-20 through 4-29.

FSLD = PHFSL-1 TTSH DCA
(TDVR, TIOR, SIOR, HIOR)
+ PHFSL-1 BSYC (ASCR or AIOR)

BSYC = AVIR FSR ASCR ASCM (ASCR)
+ AVIR AIOR AIOM PHFSL-1 (AIOR)

PHFSL-1 = PHFSL

After generating the function strobe acknowledge signal, the subcontroller generates additional signals that depend on the function indicator signal. The signals include function response signals, condition code signals, request strobe signals, and service cycle identification signals. These signals are used by the IOP to determine the type of response required. Paragraphs 4-14 through 4-19 group these signals for each type of function indicator.

4-14 TDV FUNCTION INDICATOR. For a TDV function indicator, function response signals FR0D, FR2D, and FR3D contain information, and other function response signals are always false.

FR0D = (TDVR DCA FSD) RER
+ ... (True if rate error detected)

FR2D = (TDVR DCA FSD) SUN
+ ... (True if sector unavailable)

FR3D = (TDVR DCA FSD) WPV
+ ... (True if write protection violation)

The conditions for which flip-flops RER, SUN, and WPV are set are described in paragraph 4-72.

Condition code signals (IORD, DORD) are controlled by error flip-flops RER, SUN, and WPV and by device operational flip-flop OPER.

IORD = PHFSL IORDEN
+ ... (True if no errors have occurred)

IORDEN = NIORDEN1 + ...

NIORDEN1 = TDVU NFAULT + ...

NFAULT = NRER NSUN NWPV

DORD = DORDEN PHFSL
+ ... (True if device operational)

DORDEN = OPER + ...

The conditions for which flip-flop OPER is set are described in paragraph 4-23.

4-15 TIO FUNCTION INDICATOR. For a TIO function indicator, FR0D through FR6D contain information as listed in table 4-1. Function response signal FR7D is always false.

The function response signal equations are:

FR0D = BFSD TSH CIL + ...

BFSD = FSLD

TSH = DCA (TIOR + HIOR + SIOR)

FR1D = BFSD TSH DVBSY + ...

DVBSY = DCB DVSEL

Table 4-1. Information in Function Response Signals for TIO, HIO, or SIO Commands

INFORMATION	FUNCTION RESPONSE SIGNAL*							
	FR0D	FR1D	FR2D	FR3D	FR4D	FR5D	FR6D	FR7D
Interrupt pending	1	X	X	X	X	X	X	0
Device automatic	X	X	X	1	X	X	X	0
Unusual end	X	X	X	X	1	X	X	0
EP RAD ready	X	0	0	X	X	X	X	0
EP RAD busy	X	1	1	X	X	X	X	0
EP RAD not operational	X	0	1	X	X	X	X	0
Controller ready	X	X	X	X	X	0	0	0
Controller busy	X	X	X	X	X	1	1	0

*An X indicates that the signal is not related to that information

FR2D = BFSD TSH STSH02 + ...

STSH02 = DVBSY + NOPER

FR3D = BFSD TSH DVTR + ...

FR4D = BFSD TSH UNE + ...

FR5D = BFSD TSH DCB + ...

FR6D = BFSD TSH DCB + ...

FR7D = BFSD TSH GND + ...

The data/order signal equations are:

IORD = PHFSL IORDEN + ...

IORDEN = NIORDEN1 + ...

NIORDEN1 = TIOU OPER NCIL NDCB + ...

DORD = DORDEN PHFSL + ...

DORDEN = OPER + ...

4-16 HIO FUNCTION INDICATOR. For an HIO function indicator, function response signals FR0D through FR6D contain information as listed in table 4-1. Function response signal FR7D is always false. The equations for function response signals are the same as those for the TIO function indicator.

The condition code signals (IORD, DORD) are controlled by device busy signal DVBSY and device operational flip-flop OPER.

IORD = IORDEN PHFSL + ...

IORDEN = NIORDEN1 + ...

NIORDEN1 = NDVBSY HIOU + ...

DORD = DORDEN PHFSL + ...

DORDEN = OPER + ...

4-17 SIO FUNCTION INDICATOR. For an SIO function indicator, function response signals FR0D through FR7D contain information as listed in table 4-1. Function response signal FR7D is always false. The equations for function response signals are the same as those for the TIO function indicator.

The condition code signals (IORD, DORD) are:

IORD = PHFSL IORDEN + ...

IORDEN = DCBSET + ...

DCBSET = OPER SIOPOSS PHFSL

SIOPOSS = NCIL NDCB SIOU

DORD = PHFSL DORDEN + ...

DORDEN = OPER + ...

Flip-flop CIL is the interrupt pending flip-flop, which is set by a terminal order as described in paragraph 4-34. Flip-flop DCB is the device busy flip-flop, which is set when an SIO is accepted by the device controller. This flip-flop prevents any new SIO from being accepted until processing is completed. The possible condition codes and their meaning are:

IORD	DORD	Meaning
0	0	Device not operational
0	1	Interrupt pending, device busy, or controller busy
1	1	SIO accepted

4-18 AIO FUNCTION INDICATOR. For an AIO function indicator, the EP RAD controller places its address on function response lines FR0D through FR3D and places the unit address stored in the unit register (U0 through U2) on function response lines FR5D through FR7D. Function response signal FR4D is always false.

The logic equations for the function response signals are:

FR0D = BSYC SWA0 + ...

BSYC = AIOM AIOR AVIR PHFSL-1 + ...

FR1D = BSYC SWA1 + ...

FR2D = BSYC SWA2 + ...

FR3D = BSYC SWA3 + ...

FR4D = BSYC GND + ...

FR5D = BSYC U0 + ...

FR6D = BSYC U1 + ...

FR7D = BSYC U2 + ...

The condition code (IORD, DORD) is (1, 1) only for the subcontroller having the highest priority and a pending interrupt (CIL set).

IORD = PHFSL IORDEN + ...

IORDEN = NIORDEN1 + ...

NIORDEN1 = AIOC NFAULT + ...

NFAULT = NRER NSUN NWPV

AIOC = AIOM AIOR AVIR
+ AIOC PHFSL-1 INI NRSTR

DORD = DORDEN PHFSL + ...

DORDEN = AIOC + ...

A condition code (IORD, DORD) of (0, 1) indicates a fault condition (RER, SUN, or WPV) in the controller responding to the AIO command.

In addition to function response signals and condition code signals, status signals are generated and transmitted through signals /DA0/, /DA2/, and /DA3/.

/DA0/ = O00 + ...

O00 = OXAIOST RER + ...

OXAIOST = AIOC FSU

/DA2/ = O02 + ...

O02 = OXAIOST SUN + ...

/DA3/ = O03 + ...

O03 = OXAIOST WPV + ...

4-19 ASC FUNCTION INDICATOR. The ASC function indicator is a response of the IOP to a service call from the EP RAD controller and can occur only after an SIO command has been accepted, causing service call flip-flop SCN to be direct set and service call signal SCD to be raised.

SCD = LSL

LSL = NASCR INC SCN + ...

Service calls are a part of the execution of the seek order, sense order, write order, read order, and checkwrite order. For an ASC function indicator, the function response signal contains the same address information as described for an AIO function indicator (paragraph 4-18), but the BSYC signal is controlled by different signals.

BSYC = ASCM ASCR AVIR FSR + ...

The ASC function indicator causes service connect flip-flop FSC to be set.

S/FSC = ASCB

ASCB = (delayed NFSC) ASCM ASCR AVIR FSR

C/FSC = NFSC FSR + ...

Service connect flip-flop FSC is normally set during the order out service cycle that starts an input/output sequence and is not reset until the IOP generates end service signal ESR.

R/FSC = FSC ESR

C/FSC = FSC RSD + ...

the timing of signals controlling typical input/ourput operations.

4-21 TCL Delay Line (See figure 4-7)

The TCL delay line, which provides timing signals for changes of phase, is controlled by IOP signals and by signals originating in the controller.

For online operations, signal CYCLE/C remains true after each cycle of the TCL delay line, because CYCSET latches when TCS300 is true.

CYCLE/C = CYCSET IOP + ...

CYCSET = NTCL050 (TCS300 + CYCSET + ...)

Signal CYCLE/C is an input to start gates of the TCL delay line. Other signal inputs to these gates come true for various conditions of the phase flip-flops and subcontroller signals, as described in paragraphs 4-22 through 4-29. When all inputs to one of the start gates are true, signal DCL is true and the TCL delay line is started.

After a 50-ns delay, signal CYCSET goes false as TCL050 goes true. However, the delay line pulse is stretched to 80 ns by a gate which is held true while signal NTCS080 is true.

DCL = TCS000-2 NTCS080 + ...

The TCL delay line provides an 80-ns pulse at delays of 0, 50, 80, 100, 180, and 300 ns. When the 300-ns signal is true, CYCSET becomes true and is latched as before.

4-22 Phase Flip-Flops

Phase flip-flops NPHFS, PHFSZ, PHFSL, PHRSA, PHRS, and PHTO, which control inputs to the TCL delay line, cycle through a sequence of phases determined by commands and orders received from the IOP. (See figure 4-8.) All phase flip-flops are clocked by signal TCS100-3, which is true 100 ns after the TCL delay line is started. (The flip-flops change state on the falling edge of this signal.)

C/NPHFS = TCS100-3

C/PHFSZ = TCS100-3

C/PHFSL = TCS100-3

C/PHRSA = TCS100-3

C/PHRS = TCS100-3

C/PHTO = TCS100-3

When flip-flop DCB is reset, flip-flops PHRSA, PHRS, and PHTO are direct reset.

E/PHRSA = NDCB-1

NDCB-1 = NDCB IOP + ...

E/PHRS = NDCB-1

E/PHTO = NDCB-1

A reset signal received from the computer through the IOP direct resets flip-flops NPHFS, PHFSZ, and PHFSL.

E/NPHFS = MANRST-1

MANRST-1 = RSTR + ...

E/PHFSZ = MANRST-1

E/PHFSL = MANRST-1

Since this signal also reset DCB, the initial condition of the phase flip-flops is all reset so that signal PHFS is true and all other signals (PHFSZ, PHFSL, PHRSA, PHRS, and PHTO) are false. Only one phase flip-flop can be in the set state at any time.

4-23 RESPONSE TO IOP COMMANDS. The sequence of phases in response to an IOP command (SIO, AIO, HIO, TIO, or TDV) is independent of the function indicator. A function indicator and its associated function strobe (FSU) start the TCL delay line when an addressed TIO, TDV, SIO, or HIO command is received (TTSHU DCAU) or when an AIO is received and the controller has an interrupt pending (AIOC).

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHFS FSU TTSHU DCAU
+ PHFS FSU AIOC + ...

After an 80-ns delay, OPER is reset to prepare for sampling a signal from the selection unit.

R/OPER = PHFS

C/OPER = NTCS080

Transfer from phase FS to phase FSZ takes place 100 ns after the TCL delay line is started.

S/NPHFS = PHFS

S/PHFSZ = PHFS

The TCL delay line is started as soon as PHFSZ is set.

DCL = CYCLE/C PHFSZ + ...

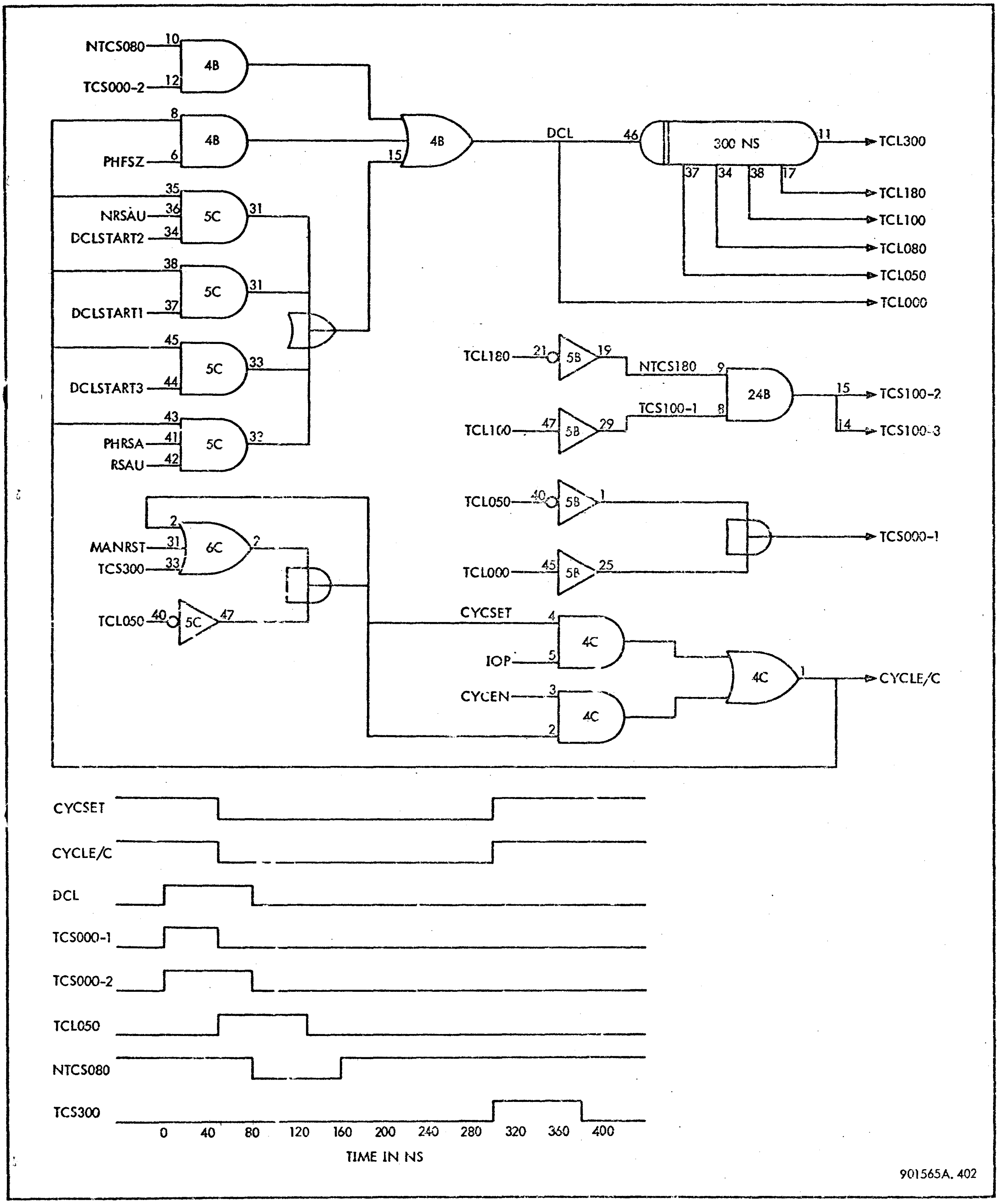


Figure 4-7. TCL Delay Line, Timing and Logic Diagram

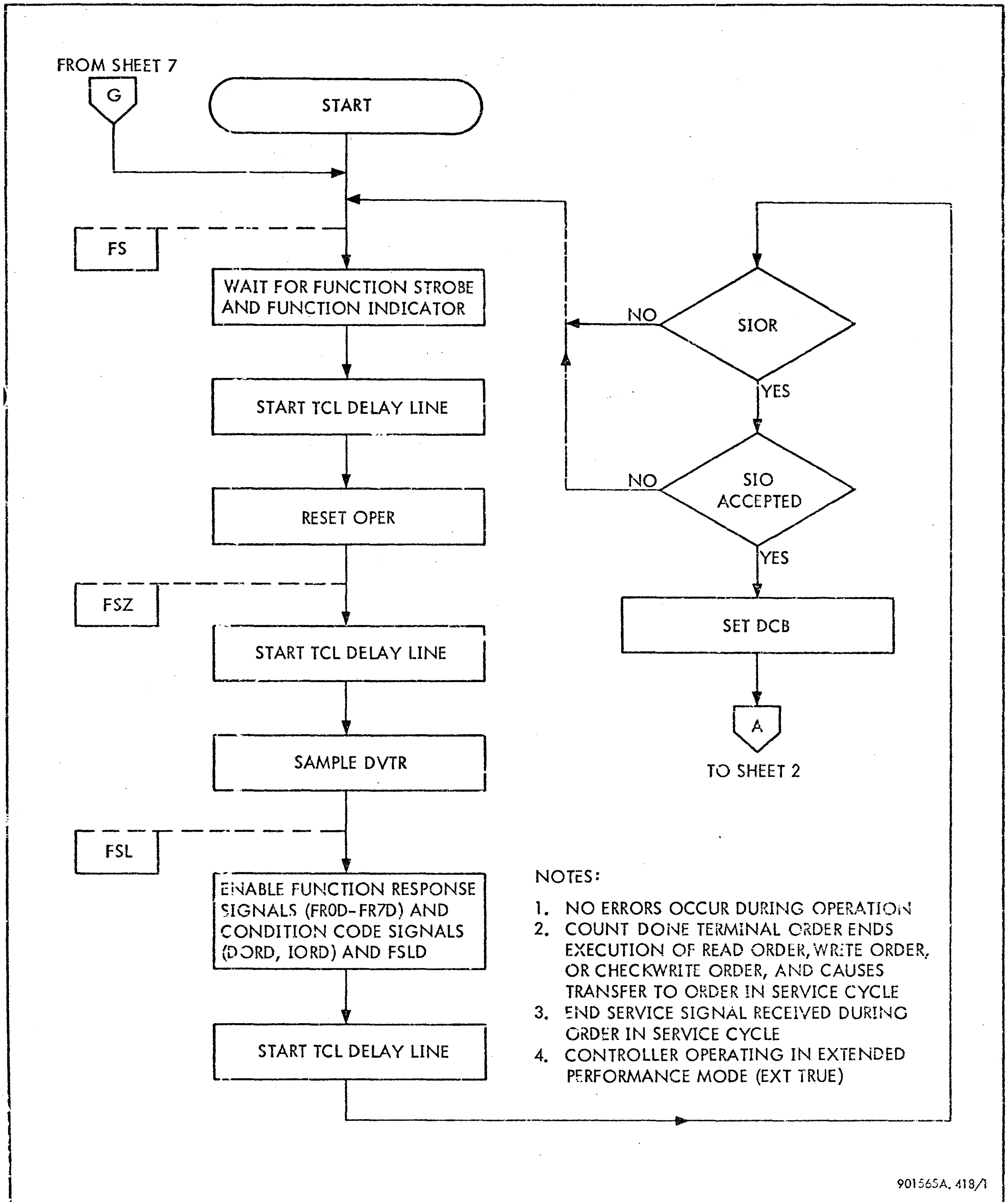


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 1 of 7)

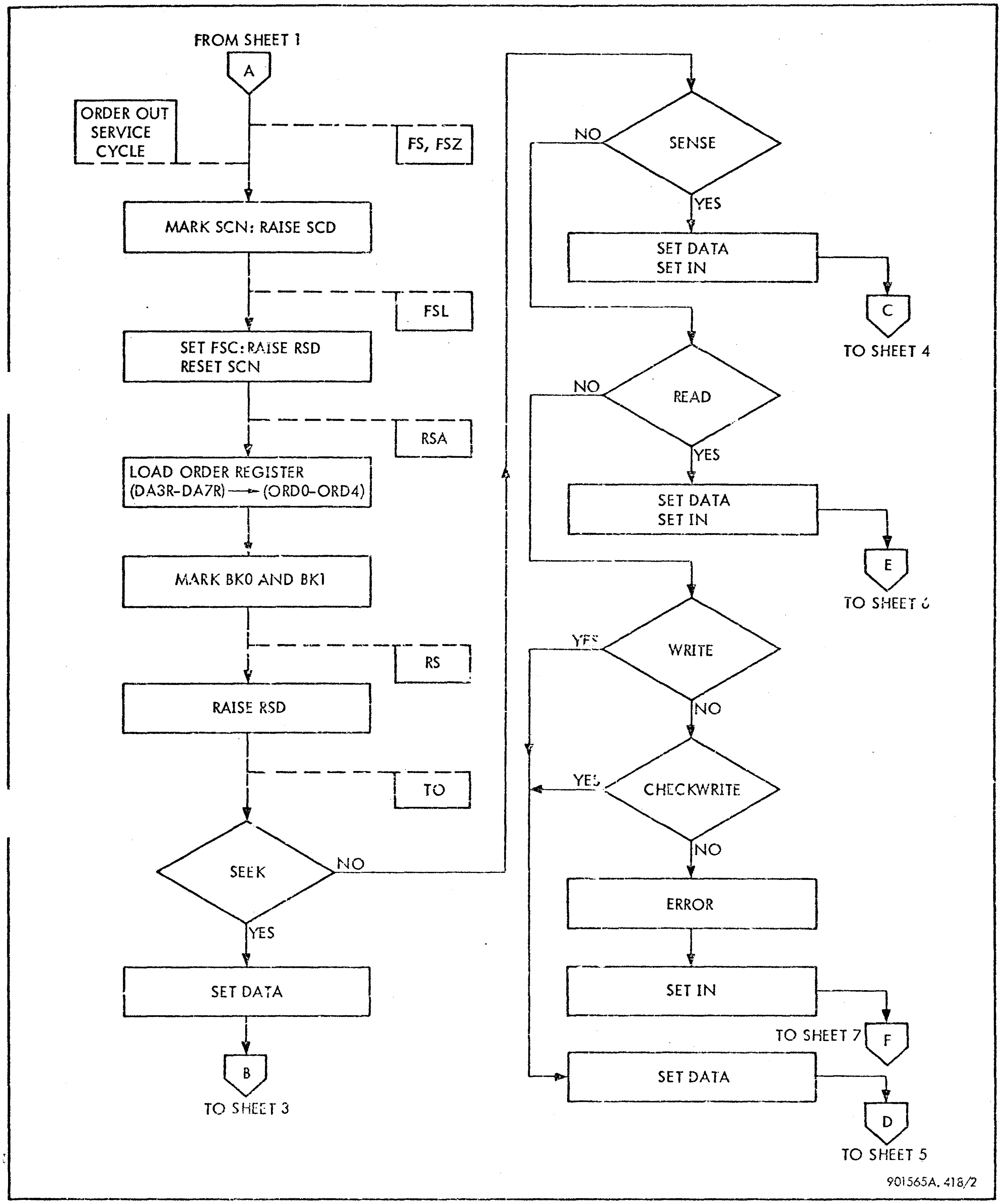


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 2 of 7)

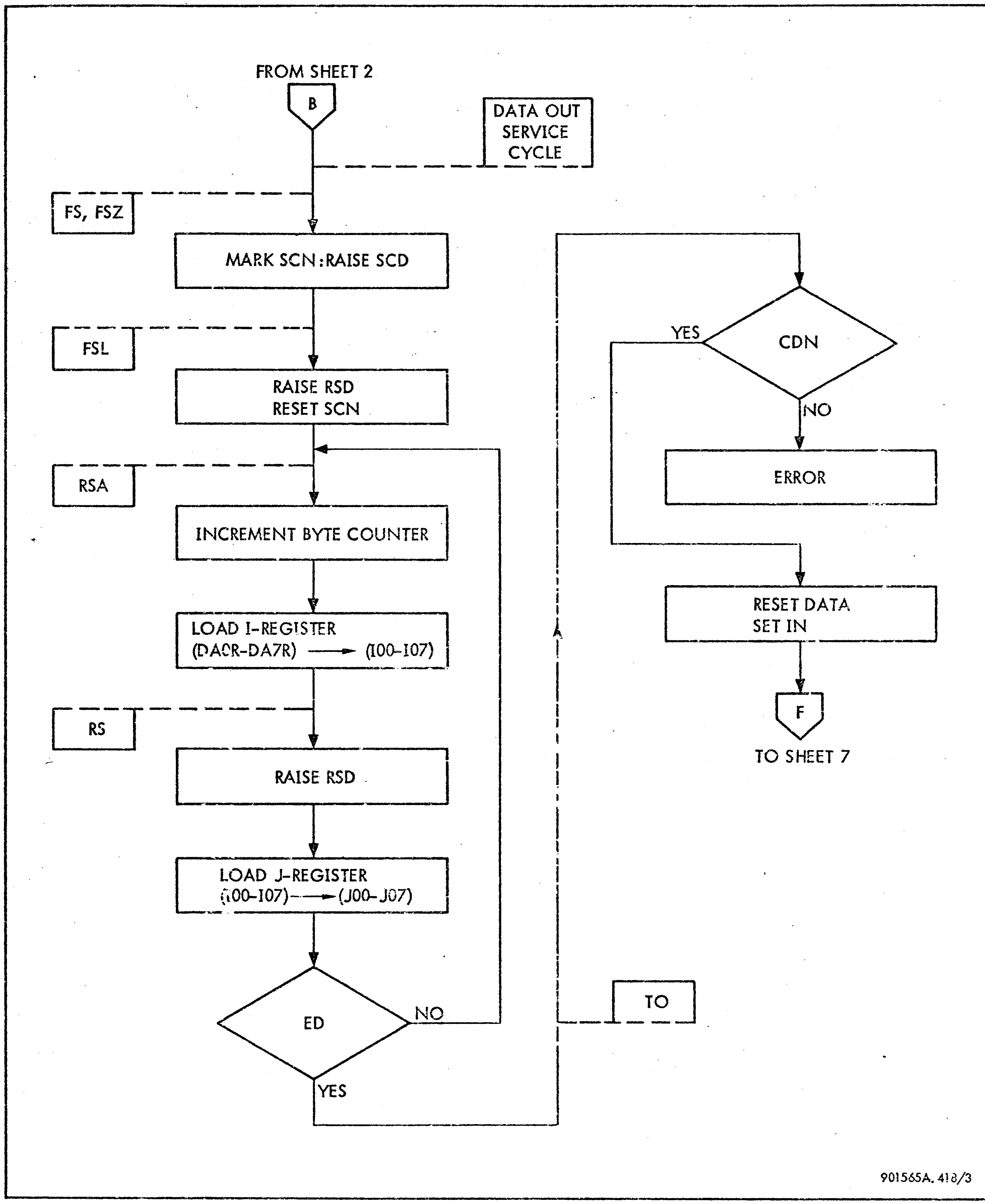


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 3 of 7)

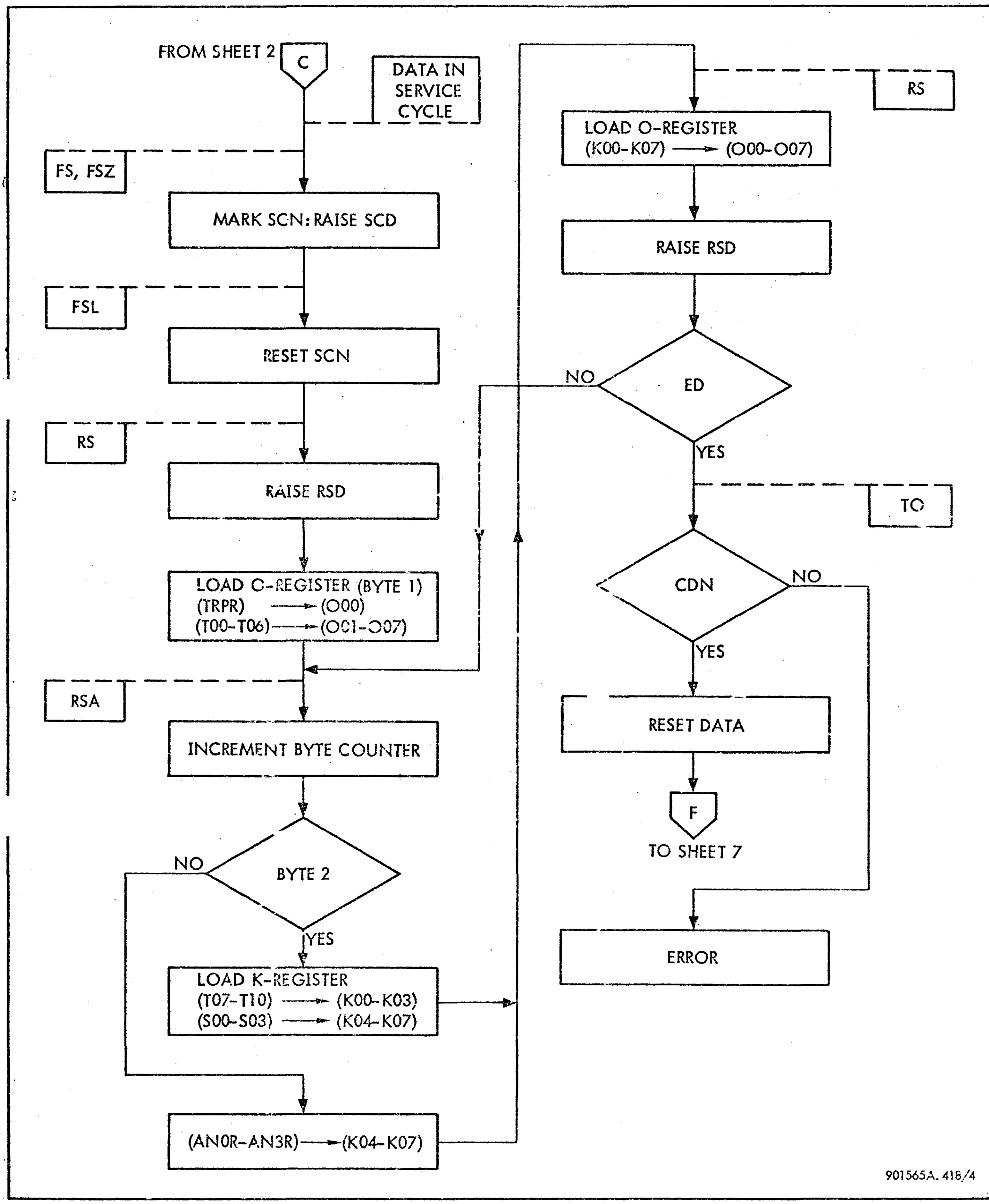


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 4 of 7)

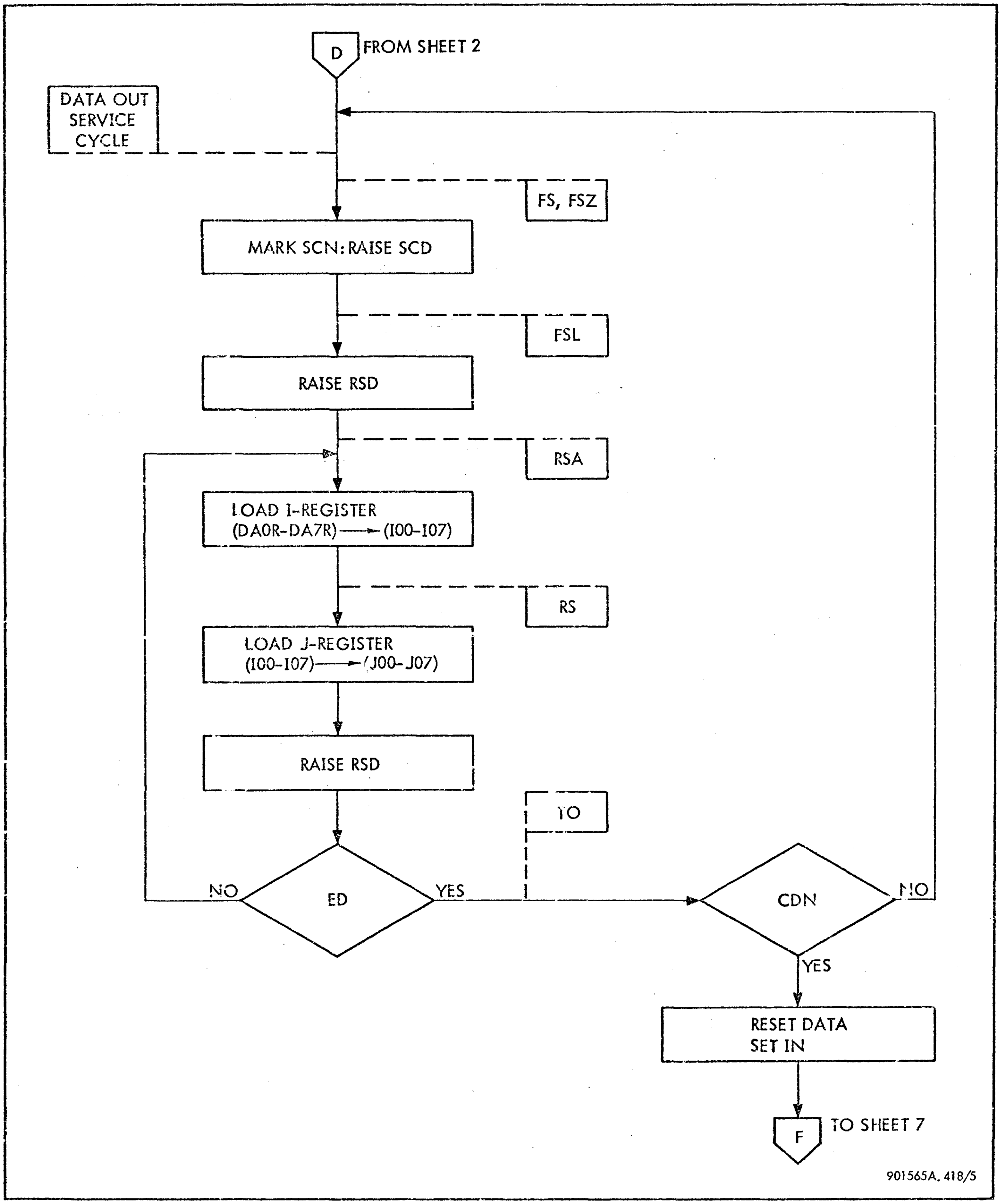


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 5 of 7)

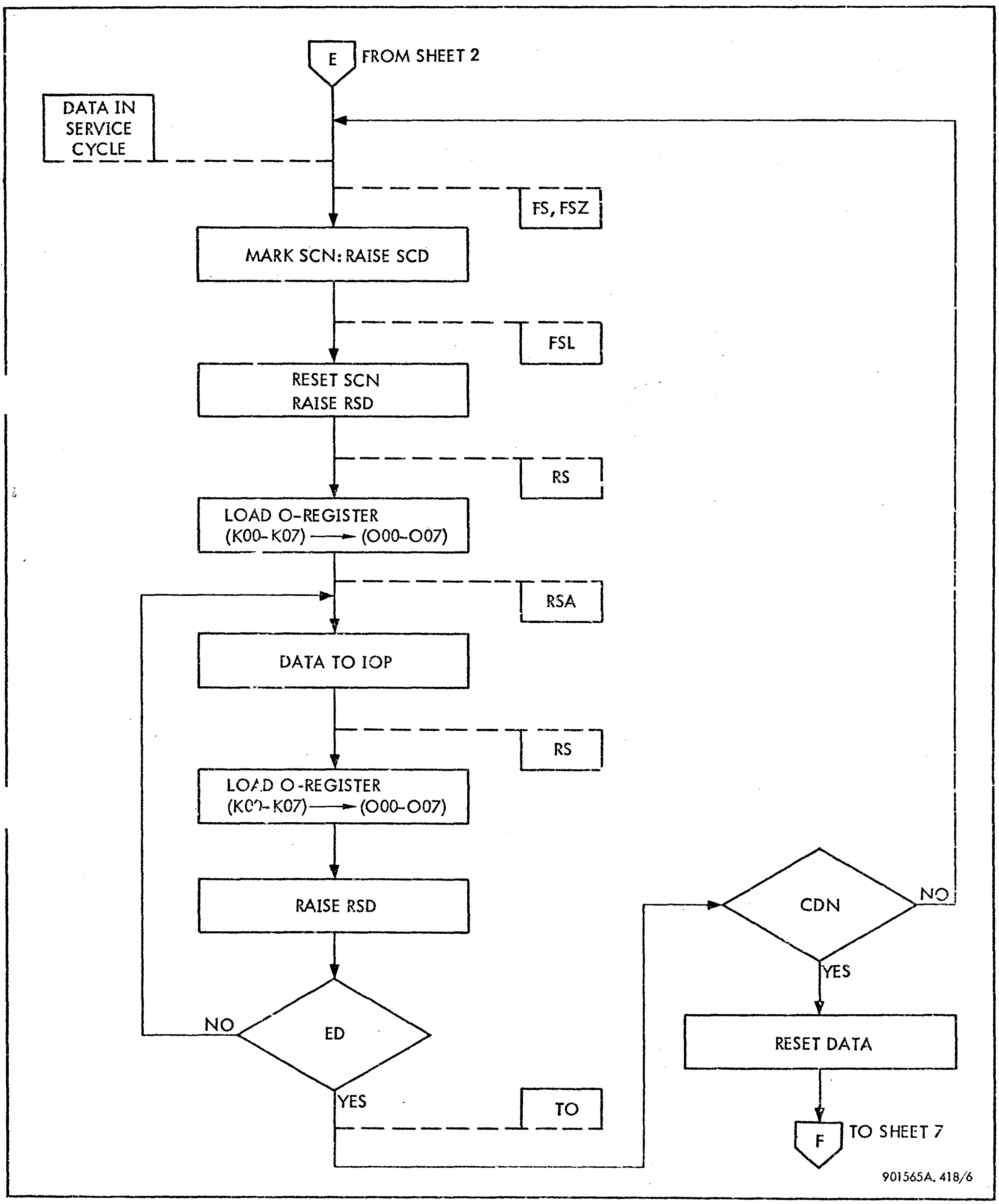


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 6 of 7)

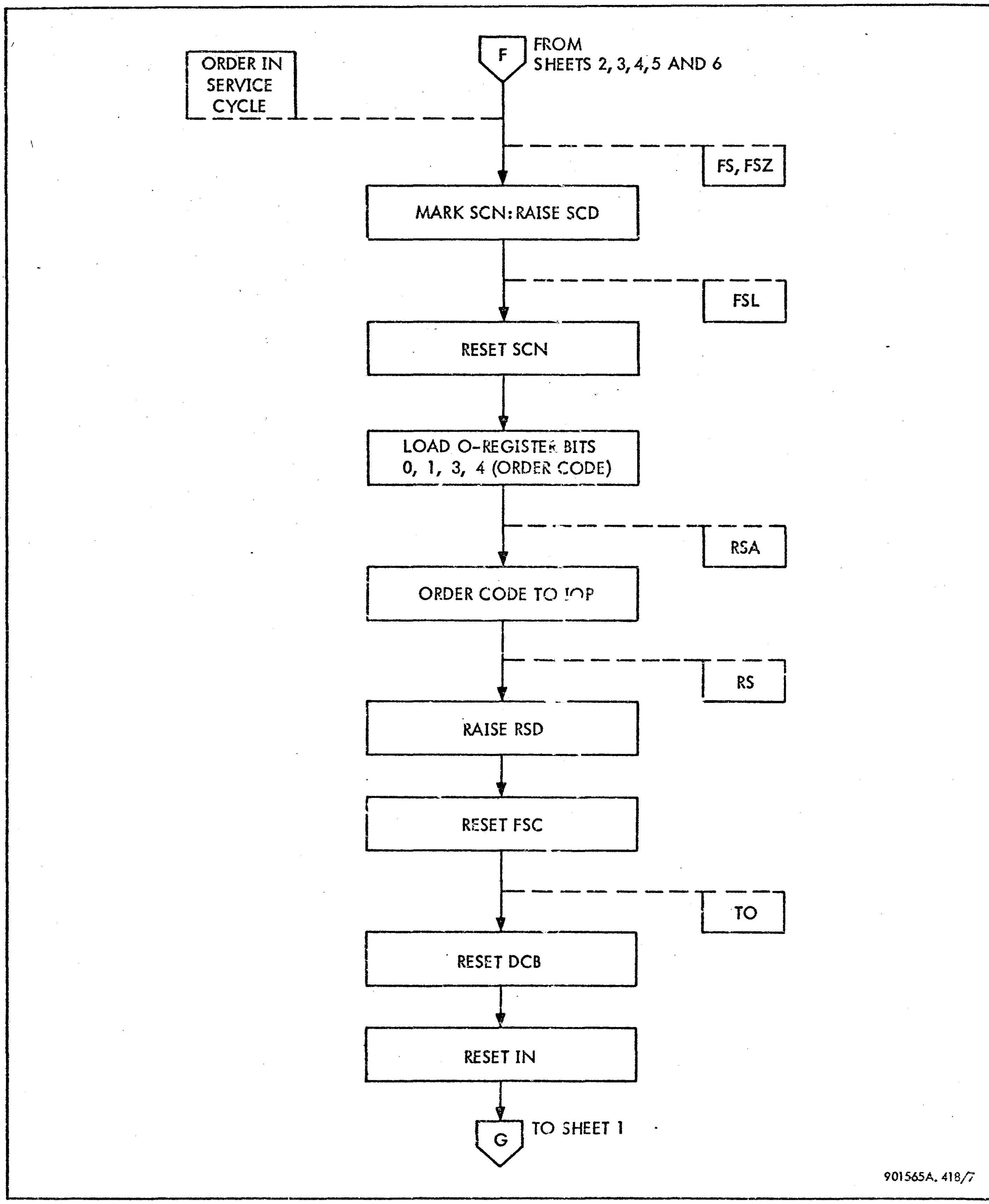


Figure 4-8. Simplified Phase Sequence, Flow Diagram (Sheet 7 of 7)

Before PHFSZ is reset, OPER samples device test signal DVTR.

S/OPER = DVTR OPERSET

OPERSET = TTSHU PHFSZ

C/OPER = NTCS080

After a 100-ns delay, PHFSZ is reset and PHFSL is set.

R/PHFSZ = ...

S/PHFSL = PHFSZ

While PHFSL is set, function response signals and condition code signals are enabled in the subcontroller and transmitted to the IOP as described in paragraphs 4-13 through 4-19. The TCL delay line is started as function strobe signal FSU goes false.

DCL = CYCLE/C DCLSTART3 + ...

DCLSTART3 = PHFSL NFSU + ...

After a 100-ns delay, NPHFS and PHFSL are reset. (Service connect flip-flop FSC is set only after an SIO command is accepted.)

R/PHFSL = ...

R/NPHFS = PHFSET

PHFSET = NFSCU PHFSL + ...

FSCU = IOP FSC + ...

For all IOP commands but an accepted SIO, the phase flip-flops wait for a new command. If an SIO is accepted, device controller busy flip-flop DCB is set during phase FSL.

S/DCB = DCBSET

DCBSET = OPER PHFSL SIOPOSS

SIOPOSS = NCIL NDCB SIOU

C/DCB = NTCS080

An SIO is accepted if the controller is not busy with a previous I/O operation (NDCB), no interrupt is pending (NCIL), and the device is operable (OPER). If DCB is set, service call flip-flop SCN is direct set after a return to phase FS, and the service call line is raised. (See paragraph 4-32.)

M/SCN = CYCLE/C SCNMEN

SCNMEN = DCB PHFS N(NSCNMEN)

N(NSCNMEN) = (NDATA SCNMEN2 + ...) NUNE

SCNMEN2 = NRWE (NWCHW + ...)

SCD = LSL

LSL = NASCR INC SCN + ...

The phase control circuits wait for an acknowledgement of a service call. Flip-flop DCB can be reset only during phase TO of an order in service cycle (except for manual reset).

R/DCB = DCBRST

DCBRST = DCBRST1 + ...

DCBRST1 = DCBRSTEN ORDIN PHTO

DCBRSTEN = NCCH + ES + UNE

During phase TO, DCB is reset if an end service signal is received (ES), if an unusual end occurs (UNE), or if command chaining is not ordered (NCCH). Therefore, once an SIO has been accepted and DCB has been set, an I/O operation takes place.

4-24 ORDER OUT SEQUENCE. An order out service cycle immediately follows acceptance of an SIO command from the IOP. When function strobe FSR coincides with an acknowledge service call addressed to the EP RAD controller (ASCM ASCR), the TCL delay line is started.

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHFS FSU BSYCU + ...

BSYCU = BSYC IOP + ...

BSYC = ASCM ASCR AVIR FSR

Phases FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, service connect flip-flop FSC is set during phase FSL as the function strobe goes false.

S/FSC = ASCB

ASCB = (NFSC delayed) ASCM ASCR AVIR FSR

C/FSC = NFSC FSR + ...

Therefore, after a 100 ns delay, PHFSL is reset, PHRSA is set, and request strobe signal RSD is raised.

R/PHFSL = ...

S/PHRSA = PHRSASET FSCU

FSCU = FSC IOP + ...

PHRSASET = PHFSL NIN + ...

RSD = FSC NRSAR (FSCU RSD + RSET NPHRSA + ...)

RSET = PHFSL NIN

Service connect flip-flop FSC remains in the set state until end service signal ES is true. Signal ES, which is generated by the IOP, causes a reset as request strobe signal RSD goes false in response to a true request strobe acknowledge signal RSAR.

R/FSC = ESR FSC

C/FSC = FSC RSD + ...

RSD = FSC NRSAR (FSCU RSD + ...)

FSCU = FSC IOP + ...

When the IOP acknowledges the request strobe, signal RSAR is true, signal RSD goes false, and the TCL delay line is started.

DCL = CYCLE/C PHRSA RSAU + ...

During phase RSA of an order out service cycle, the order code is stored in the order register as described in paragraph 4-31. After a 100-ns delay, PHRSA is reset and PHRS is set.

R/PHRSA = ...

S/PHRS = FSCU PHRSET

PHRSET = PHRSA + ...

Request strobe line RSD is raised when phase RS is entered.

RSD = FSC NRSAR (FSCU RSD
+ PHRS TCS000-2 + ...)

The TCL delay line is started after request strobe acknowledge signal RSAU is false. (Signal NDATA is true because an order out service cycle is in process.)

DCL = CYCLE/C DCLSTART3 + ...

DCLSTART3 = PHRS NDATA NRSAU + ...

After a 100-ns delay, phase TO is entered, and the TCL delay line is started when the request strobe is acknowledged.

R/PHRS = ...

S/PHTO = PHRS ED

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHTO RSAU + ...

After a 100-ns delay, phase FS is entered.

R/PHTO = ...

R/NPHFS = PHFSET

PHFSET = PHTO + ...

Subsequent operations depend upon the order code stored. (See table 4-2 for order codes.)

Table 4-2. Order Signals

ORDER	CODE*	SIGNALS	
		Always True†	True When NPHRSAOO
Seek	X XX11	SEEK	SEKSEND
Sense	X 0100	SENSE	SEKSEND
Read	X XX10	READ	RCHW, WRCH
Write	X X001	WRITE	WCHW, WRCH
Checkwrite	X X101	CHWR	RCHW, WCHW, WRCH

*Order register bits 0, 1, 2, 3, 4; IOP data line bits 3, 4, 5, 6, 7

†Except during order register load, when all signals are false, and after which one signal becomes true

4-25 SEEK ORDER SEQUENCE. If a seek order code is stored during the order out service cycle, the (DATA, IN) flip-flops request a data out service cycle (1, 0) as described in paragraph 4-30. While signal PHFS is true, a service cycle is requested by setting SCN. The TCL delay line is started when the function strobe signal and the acknowledge service call signal are received.

M/SCN = CYCLE/C PHFS DCB
N(NSCNMEN)

N(NSCNMEN) = NCDN DATAOUT SCR + ...

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHFS FSU BSYCU + ...

(Flip-flop SCR is set during the order out service cycle.)

Phases FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, at the end of phase FSL, PHRSA is set, the request strobe signal RSD is raised, and the byte counter is decremented. (See paragraph 4-33 for a description of the byte counter.)

R/PHFSL = . . .

S/PHRSA = PHRSASET FSCU

PHRSASET = PHFSL NIN + . . .

FSCU = IOP FSC + . . .

RSD = FSC NRSAR (FSCU RSD + PHRSA RSET + . . .)

RSET = PHFSL NIN

NBKCK = PHRSA SEKSEND TCS000-3 + . . .

SEKSEND = SEEK NPHRSAOO + . . .

When the request strobe is acknowledged, the TCL delay line is started and IOP data is stored in the I-register.

DCL = CYCLE/C PHRSA RSAU + . . .

RSAU = IOP RSAR + . . .

IXD = PHRSADO TCS000-3

PHRSADO = PHRSA DATAOUT

After a 100-ns delay, PHRSA is reset and PHRS is set.

S/PHRS = FSCU PHRSET

PHRSET = PHRSA + . . .

Once PHRS is set, the TCL delay line is started when RSAR is false and RSD is raised once more.

DCL = CYCLE/C DCLSTART2 NRSAU + . . .

DCLSTART2 = PHRS SEKSEND + . . .

RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + . . .)

Transfer from phase RS is to phase RSA or to phase TO, depending upon the end data signal. (See figure 4-8.)

S/PHRSA = PHRSASET FSCU

PHRSASET = PHRSNED + . . .

PHRSNED = PHRS NED

S/PHTO = PHRS ED

Signal ED comes true after the second byte has been accepted from the IOP, as indicated by the byte counter. (See paragraph 4-35.)

EDI = EDISET1 NPHRSA + FSCU EDI + . . .

EDISET1 = SEEK BKZW + . . .

Thus the flip-flops cycle between phase RSA and phase RS until the end data signal enables transfer to phase TO. The TCL delay line may be started in either of two ways in phase TO.

DCL = CYCLE/C DCLSTART1 + CYCLE/C DCLSTART2 NRSAU + . . .

DCLSTART1 = PHTO RSAU + . . .

DCLSTART2 = PHTO ES + . . .

Therefore, if the IOP has generated an end service signal, the TCL delay line is started after phase TO is entered without waiting for acknowledgement of the request strobe raised at the start of phase RS. Otherwise, the TCL delay line is not started until RSAR is true. In either case, phase FS is entered from phase TO. After 100 ns, the (DATA, IN) flip-flops are placed in the (0, 1) state to request an order in service cycle, as described in paragraph 4-30.

R/PHTO = . . .

R/NPHFS = PHFSET

PHFSET = PHTO + . . .

4-26 <u>SENSE ORDER SEQUENCE.</u> If a sense order code is stored during the order out service cycle, the (DATA, IN) flip-flops request a data in service cycle (1, 1) as described in paragraph 4-30. While signal PHFS is true, a service cycle is requested by setting SCN. The TCL delay line is started when a function strobe signal is received.

M/SCN = PHFS DCB N(NSCNMEN)

N(NSCNMEN) = NCDN SEN NTSE + . . .

DCL = CYCLE/C DCLSTART1 + . . .

DCLSTART1 = PHFS FSU BSYCU + . . .

Phase FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, at the end of phase FSL, PHRS is set and the first byte of sense data is stored in the O-register.

R/PHFSL = . . .

S/PHRS = FSCU PHRSET

FSCU = FSC IOP + . . .

PHRSET = PHFSL IN + . . .

OXSENSE1 = SENSE OXKEN BKZZ

OXKEN = DATAIN NED PHRS

After PHRS is set, the TCL delay line is started and request strobe signal RSD is raised.

```
DCL          = CYCLE/C DCLSTART2 NRSAU
               + ...

  DCLSTART2  = PHRS SEKSEND + ...

  SEKSEND    = SENSE NPHRSAOO + ...

  PHRSAOO    = PHRSA ORDOUT

RSD          = FSC NRSAR (FSCU RSD
               + PHRS TCS000-2 + ...)
```

After a 100-ns delay, PHRS is reset and PHRSA is set.

```
R/PHRS       = ...

S/PHRSA      = PHRSASET FSCU

  PHRSASET   = PHRSNED + ...

  PHRSNED    = PHRS NED
```

When the request strobe is acknowledged, the TCL delay line is started and the byte counter is decremented.

```
DCL          = CYCLE/C PHRSA RSAU + ...

  RSAU       = RSAR + ...

NBKCK        = PHRSA SEKSEND TCS000-3 + ...

  SEKSEND    = SENSE NPHRSAOO + ...
```

After a 100-ns delay, PHRSA is reset and PHRS is set.

```
R/PHRSA      = ...

S/PHRS       = FSCU PHRSET

  PHRSET     = PHRSA + ...
```

The request strobe is raised as in the previous RS phase, and data is transferred through the K-register to the O-register. (For this operation, the K-register functions as a gate.)

```
OXK          = OXKEN TCS000-2

  OXKEN      = DATAIN PHRS NED
```

(During the previous RS phase, no data was in the K-register.) When the request strobe is acknowledged, PHRSA is set as before. Transfer between phase RS and phase RSA continues until all sense data has been transmitted to the IOP, as indicated by the end data signal through the byte counter which is incremented during phase RSA. (See figure 4-8.)

```
EDI          = EDISET1 TSC000-2
               + EDI FSCU + ...

  EDISET1    = SENSE BKWZ + ...
```

After ED is true, PHTO is set, as described in paragraph 4-25. The (DATA, IN) flip-flops are set to (0, 1) to request an order in service cycle, and phase FS is entered.

```
R/PHTO       = ...

R/NPHFS      = PHFSET

  PHFSET     = PHTO + ...
```

4-27 WRITE ORDER OR CHECKWRITE ORDER SEQUENCE. If either a write order code or a checkwrite order code is stored during the order out service cycle, the (DATA, IN) flip-flops request a data out service cycle (1, 0) as described in paragraph 4-30. While signal PHFS is true, a service cycle is requested by setting SCN. The TCL delay line is started when a function strobe signal is received.

```
M/SCN          = CYCLE/C PHFS DCB
                 N(NSCNMEN)

  N(NSCNMEN)   = NCDN DATAOUT SCR + ...

DCL            = CYCLE/C DCLSTART1 + ...

  DCLSTART1    = PHFS FSU BSYCU + ...
```

Phases FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, at the end of phase FSL, PHRSA is set and request strobe signal RSD is raised.

```
R/PHFSL      = ...

S/PHRSA      = PHRSASET FSCU

  FSCU       = FSC IOP + ...

  PHRSASET   = PHFSL NIN + ...

RSD          = FSC NRSAR (FSCU RSD
               + PHRSA RSET + ...)

  RSET       = PHFSL NIN
```

When the request strobe is acknowledged, the TCL delay line is started and IOP data is stored in the I-register.

```
DCL          = CYCLE/C PHRSA RSAU + ...

  RSAU       = IOP RSAR + ...

IXD          = PHRSADO TCS000-3

  PHRSADO    = PHRSA DATAOUT
```

After a 100-ns delay, PHRSA is reset and PHRS is set.

R/PHRSA = ...

S/PHRS = FSCU PHRSET

PHRSET = PHRSA + ...

Once PHRS is set, the TCL delay line cannot be started until RSAR is false and the J-register is empty (NJFI true). When these conditions are true, request strobe signal RSD is raised as the TCL delay line is started.

DCL = CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART2 = PHRS WCHW NJFI + ...

RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)

At the same time, the J-register is filled from the I-register (for operation with a one-byte interface).

JXI1B = IOP BYT1ID PHRSDO TCS000-2

PHRSDO = PHRS DATAOUT

Transfer from phase RS is to phase RSA or to phase TO, depending upon the end data signal ED. (See figure 4-8.)

S/PHRSA = PHRSASET FSCU

PHRSASET = PHRSNED + ...

PHRSNED = PHRS NED

S/PHTO = PHRS ED

Signal ED comes true under control of flip-flop EDISET3, as described in paragraph 4-35. (The IOP may terminate the operation by causing signal ESET to be true.)

EDI = EDISET1 TCS000-2 + FSCU EDI + ...

EDISET1 = EDISET3 + ...

Thus the flip-flops cycle between phase RSA and phase RS until an end data signal enables transfer to phase TO. After ED is true, PHTO is set, as described in paragraph 4-25. If the IOP does not signal count done or IOP halt during phase TO, the (DATA, IN) flip-flops remain in state (1, 0) and the sequence of data out service cycles continues. If the IOP does signal count done during phase TO, the (DATA, IN) flip-flops are placed in state (0, 1) to request an order in service cycle. In either case, phase FS is entered from phase TO.

R/PHTO = ...

R/NPHFS = PHFSET

PHFSET = PHTO + ...

4-28 READ ORDER SEQUENCE. If a read order code is stored during the order out service cycle, the (DATA, IN) flip-flops are set in state (1, 1) to request a data inservice cycle, as described in paragraph 4-30. While signal PHFS is true, a service cycle is requested by setting SCN. The TCL delay line is started when a function strobe signal is received.

M/SCN = PHFS DCB N(NSCNMEN)

N(NSCNMEN) = NCDN READ KFID BYT4ID + NCDN READ KFID NSCR + NCDN READ KFID POST + ...

The initial service cycle is requested under control of the RK-counter through flip-flop SCR. When at least four data bytes are stored in the FAM module, flip-flop SCR is reset and SCN is direct set when KFID is true. Subsequent service cycles are requested as a true NSCR signal indicates that there are sufficient data bytes in the FAM module. A service cycle may be requested any time after postamble flip-flop POST is set. This condition can occur if data bytes remain in the FAM module after the postamble is detected. The data bytes are transferred even if fewer than four bytes remain. For a four-byte IOP interface (BYT4ID true), all service cycles are controlled by signal KFID.

Phases FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, at the end of phase FSL, PHRS is set.

R/PHFSL = ...

S/PHRS = FSCU PHRSET

FSCU = FSC IOP + ...

PHRSET = PHFSL IN + ...

After PHRS is set, the TCL delay line is started. As the TCL delay line is started, the request strobe signal is raised and data is stored in the O-register. These operations cannot take place until the K-register is filled (KFID true).

DCL = CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART2 = PHRS READ KFID + ...

OXK = OXKEN TCS000-2

OXKEN = DATAIN PHRS NED

RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)

After a 100-ns delay, PHRSA is set and PHRS is reset.

R/PHRS = ...

S/PHRSA = PHRSASET FSCU

PHRSASET = PHRSNED + ...

PHRSNED = PHRS NED

When the request strobe is acknowledged, the TCL delay line is started.

DCL = CYCLE/C PHRSA RSAU + ...

RSAU = RSAR + ...

After a 100-ns delay, PHPS is set and PHRSA is reset.

R/PHRSA = ...

S/PHRS = FSCU PHRSET

PHRSET = PHRSA + ...

The request strobe is raised as in the previous RS phase. When the K-register is filled, the TCL delay line is started and data is stored in the O-register as before.

Transfer from phase RS is to phase RSA or to phase TO, depending on end data signal ED. (See figure 4-8.)

S/PHRSA = PHRSASET FSCU

PHRSASET = PHRSNED + ...

PHRSNED = PHRS NED

S/PHTO = PHRS ED

Signal ED comes true under control of the RK-counter in the FAM circuits when signal KA8 indicates that the FAM module is empty. Signal ED is normally controlled by the IOP, and signal KA8 controls operation only if the IOP is offline or if the last data byte is transferred from the FAM module before the IOP generates an end data signal.

EDI = EDISET2 NPHRSA + FSCU EDI + ...

EDISET2 = KA8 OXKEN

Thus the flip-flops cycle between phase RSA and phase RS until an end data signal enables transfer to phase TO. For transfer from phase RS to phase TO, the TCL delay line is started when ED is true and before a request strobe acknowledge is received.

DCL = CYCLE/C DCLSTART3 + ...

DCLSTART3 = PHRS ED READ NRSAU + ...

After ED is true, PHTO is set as described in paragraph 4-25.

If the IOP does not signal count done or IOP error halt during phase TO, the (DATA, IN) flip-flops remain in state (1, 1) and the sequence of data in service cycles continues. If the IOP does signal count done during phase TO, the (DATA, IN) flip-flops are placed in state (0, 1) to request an order in service cycle. In either case, phase FS is entered from phase TO.

R/PHTO = ...

R/NPHFS = PHFSET

PHFSET = PHTO + ...

4-29 <u>ORDER IN SEQUENCE</u>. An order in service cycle follows execution of a completed order (seek, sense, read, write, or checkwrite) or an unusual end indicated by flip-flop UNE. In either case, the (DATA, IN) flip-flops are placed in the (0, 1) state as described in paragraph 4-30. While signal PHFS is true, a service cycle is requested by setting SCN. The TCL delay line is started when a function strobe signal is received.

M/SCN = CYCLE/C PHFS DCB N(NSCNMEN)

N(NSCNMEN) = NDATA NRWE NWCHW + ...

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHFS FSU BSYCU + ...

Phases FS, FSZ, and FSL are controlled by the same equations described in paragraph 4-23. However, at the end of phase FSL, PHRS is set.

R/PHFSL = ...

S/PHRS = FSCU PHRSET

FSCU = FSC IOP + ...

PHRSET = PHFSL IN + ...

The TCL delay line is started immediately, since the DATA flip-flop is in the reset state.

DCL = CYCLE/C DCLSTART3 + ...

DCLSTART3 = PHRS NDATA NRSAU + ...

As the TCL delay line is started, request strobe signal RSD is raised and order data is stored in O-register bits 0, 1, 3, and 4, as described in paragraph 4-38.

OXORDIN = PHRSNED ORDIN

PHRSNED = PHRS NED

RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)

After a 100-ns delay, PHRS is reset and PHRSA is set.

R/PHRS = ...

S/PHRSA = PHRSASET FSCU

PHRSASET = PHRSNED + ...

While PHRSA is set, signal ED comes true as described in paragraph 4-35.

EDI = EDISET1 TCS000-2 + FSCU EDI + ...

EDISET1 = NDATA + ...

The TCL delay line is started when the request strobe is acknowledged.

DCL = CYCLE/C PHRSA RSAU + ...

RSAU = RSAR + ...

After a 100-ns delay, PHRSA is reset and PHRS is set.

R/PHRSA = ...

S/PHRS = FSCU PHRSET

PHRSET = FSC IOP + ...

The TCL delay line is started when RSAR is false. As the RSAR signal goes false, a signal RSD clocks FSC, and FSC is reset if the IOP drives ESR true.

DCL = CYCLE/C DCLSTART3 + ...

DCLSTART3 = PHRS NDATA NRSAU + ...

R/FSC = ESR FSC

C/FSC = FSC RSD + ...

If the IOP does not drive ESR true, the controller remains service-connected to request a terminal order.

After a 100-ns delay, PHRS is reset and PHTO is set.

R/PHRS = ...

S/PHTO = PHRS ED

Terminal order operations are described in paragraph 4-34. If the IOP has driven ESR true, DCB is reset 80 ns after the TCL delay line is started.

R/DCB = DCBRST

DCBRST = DCBRST1 + ...

DCBRST1 = DCBRSTEN ORDIN PHTO

DCBRSTEN = ES + ...

C/DCB = NTCS080

The TCL delay line may be started in either of two ways in phase TO.

DCL = CYCLE/C DCLSTART1 + CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART1 = PHTO RSAU + ...

DCLSTART2 = PHTO ES + ...

Therefore, if the IOP has generated an end service signal, the TCL delay line is started after phase TO is entered without waiting for acknowledgement of the request strobe raised at the start of phase RS. Otherwise, the TCL delay line is not started until RSAR is true. After a 100-ns delay, the (DATA, IN) flip-flops are placed in a state corresponding to the manner in which the order in service cycle is terminated. In either case, phase FS is entered from phase TO.

R/PHTO = ...

R/NPHFS = PHFSET

PHFSET = PHTO + ...

4-30 Service Cycle Identification Logic

The type of service cycle is identified by flip-flops DATA and IN, and associated output signals, as follows:

DATA	IN	Service Cycle	Output Signal
0	0	Order out	ORDOUT
0	1	Order in	ORDIN
1	0	Data out	DATAOUT
1	1	Data in	DATAIN

When an input/output sequence is completed, DATA and IN are direct reset after flip-flop DCB is reset.

E/DATA = NDCB-1

NDCB-1 = NDCB IOP + NDCB PET

E/IN = NDCB-1

Therefore, DATA and IN are both in the reset state (order out) when an SIO command is accepted from the IOP. The flip-flops are clocked only during phase FS or phase TO.

C/DATA = PHFSTOD TCS100-3

PHFSTOD = PHFSDAT + PHTO

PHFSDAT = PHFS DAT

C/IN = PHFSTOD TCS100-3

When the (DATA, IN) flip-flops detect a PET count done signal (CDNPET), an online count done signal (CDN), or an unusual end signal (UNE), the flip-flops are placed in the (0, 1) state to request an order in service cycle. (Signal NSKSBK is true when neither a seek order nor a sense order is being executed.)

S/DATA = DATASET NORDIN

DATASET = NCDN NCDNPET NUNE NSKSBK

SKSBK = SEEK BKWZ + SENSE BKWW

R/DATA = ...

S/IN = INSET NORDIN

INSET = NDATASET + ...

R/IN = ...

During the execution of an order, the (DATA, IN) flip-flops assume a sequence of states determined by the order in which they are stored during the order out service cycle.

If a seek order is stored, signal DATASET is true until SKSBK indicates that all bytes have been transferred. Therefore the (DATA, IN) flip-flops are placed in the (1, 0) state during phase TO of the order out service cycle.

After all bytes have been transferred, SKSBK is true and the (DATA, IN) flip-flops are placed in the (0, 1) state.

R/DATA = ...

S/IN = INSET NORDIN

INSET = NDATASET + ...

NDATASET = SEEK BKWZ + ...

If a sense order is stored, ORD4 is false and DATASET is true until SKSBK indicates that all bytes have been transferred. Therefore the (DATA, IN) flip-flops are placed in the (1, 1) state during phase TO of the order out service cycle. After all bytes have been transferred, SKSBK is true and ORD4 remains false, so that the (DATA, IN) flip-flops are placed in the (0, 1) state.

S/DATA = DATASET NORDIN

DATASET = NCDN NCDNPET NUNE NSKSBK

SKSBK = SENSE BKWW + ...

S/IN = INSET NORDIN

INSET = NORD4 + ...

If a write order or checkwrite order is stored during the order out service cycle, DATASET is true and ORD4 is true, so that the (DATA, IN) flip-flops are placed in the (1, 0) state to request a data out service cycle similar to a seek order. For errorless operation, DATASET remains true until phase TO of the service cycle is reached. If count done flip-flop CDN is set during phase TO, DATASET becomes false, and the (DATA, IN) flip-flops are placed in the (0, 1) state.

If a read order is stored during the order out service cycle, DATASET is true and ORD4 is false, so that the (DATA, IN) flip-flops are placed in the (1, 1) state to request a data in service cycle similar to the sense order. For errorless operation, DATASET remains true until phase TO is reached. If count done flip-flop CDN is set during phase TO, DATASET becomes false and the (DATA, IN) flip-flops are placed in the (0, 1) state.

If an invalid order is detected, both DATA and IN are set.

S/DATA = DATASET NORDIN

DATASET = NCDN NCDNPET NUNE NSKSBK

S/IN = INSET NORDIN

INSET = N(DATASET ORD4)

A service call for a data in service cycle begins. However, unusual end flip-flop UNE is direct set during phase FS, and an unusual end takes place. (See paragraph 4-73.)

4-31 Order Register

The order register consists of flip-flop ORD0, buffered latches ORD1 through ORD4, and associated logic elements. The order register stores an order code during the order out service cycle which occurs as the first step of an input/output sequence. The order code is retained during execution of the order and controls the following signals (also see table 4-2):

SEEK = ORD3 ORD4 (03)

SENSE = ORD2 NORD3 NORD4 (04)

READ = ORD3 NORD4 (02)

WRITE = NORD2 NORD3 ORD4 (01)

CHWR = ORD2 NORD3 ORD4 (05)

SEKSEND = NPHRSAOO SEEK
+ NPHRSAOO SENSE

RCHW = NPHRSAOO READ
+ NPHRSAOO CHWR

WCHW = NPHRSAOO WRITE
+ NPHRSAOO CHWR

WRCH = NPHRSAOO WRITE
+ NPHRSAOO RCHW

For online operation (IOP true), the order code is stored during phase RSA of the order out service cycle.

S/ORD0 = DA3R IOP

R/ORD0 = ...

C/ORD0 = ORDXIOP

ORDXIOP = IOP PHRSAOO TCS000-3

PHRSAOO = PHRSA ORDOUT

ORD1 = DA4R ORDXIOP + ...

ORD2 = DA5R ORDXIOP + ...

ORD3 = DA6R ORDXIOP + ...

ORD4 = DA7R ORDXIOP + ...

The order code bits are retained in buffered latches ORD1 through ORD4 while ORDX0 is true.

ORD1 = ORD1 ORDX0 + ...

ORD2 = ORD2 ORDX0 + ...

ORD3 = ORD3 ORDX0 + ...

ORD4 = ORD4 ORDX0 + ...

After an input/output operation is completed, flip-flop DCB is reset and the order register is cleared. (For command chaining, DCB is not reset.)

NORDX0 = PHFS NDCB + ...

A new order code is stored as signal ORDX0 goes true during phase RSA of an order out service cycle.

NORDX0 = PHRSAORD TCS000-1 + ...

PHRSAORD = PHRSA NDATA

The order code is retained during execution of orders while the DATA flip-flop is in the set state (data in or data out).

4-32 Service Call Logic

Signal SCD, which requests a service call from the IOP, is controlled by service call flip-flop SCN. (See figure 4-9.) Service call signal SCD is raised to the true level when SCN is set and remains at the true level until SCN is reset.

SCD = LSL

LSL = NASCR INC SCN
+ ASCR INI LSL NRSTR SCN

Service call flip-flop SCN is direct reset when the controller is not busy and can be placed in the set state only by the direct set input. The direct set input can be true only during phase FS after DCB has been set by an SIO command.

E/SCN = NDCB

M/SCN = CYCLE/C SCNMEN

SCNMEN = PHFS DCB N(NSCNMEN)

After SCN has been set, it may be retained in the set state for certain conditions if the controller is operating in the extended performance mode (EXT true) and is executing a read order, write order, or checkwrite order. Signal SCNEN is true when additional service calls are required to maintain the data transfer rate during extended performance operation and prevents reset of SCN during phase FSL.

S/SCN = SCNEN

SCNEN = SCN DATA EXT SCSET

SCSET = READ NRK1 + WCHW RK1SCR

RK1SCR = RK1 SCR

C/SCN = TCS100-3

If SCN is set during phase FS, SCN is reset during phase FSL.

R/SCN = SCNRST

SCNRST = PHFSL + ...

C/SCN = TCS100-3

Preventing reset of SCN allows the FAM module to be filled during write or checkwrite operations and to be emptied during read operations without requiring the controller to wait for priority on the data lines from the IOP.

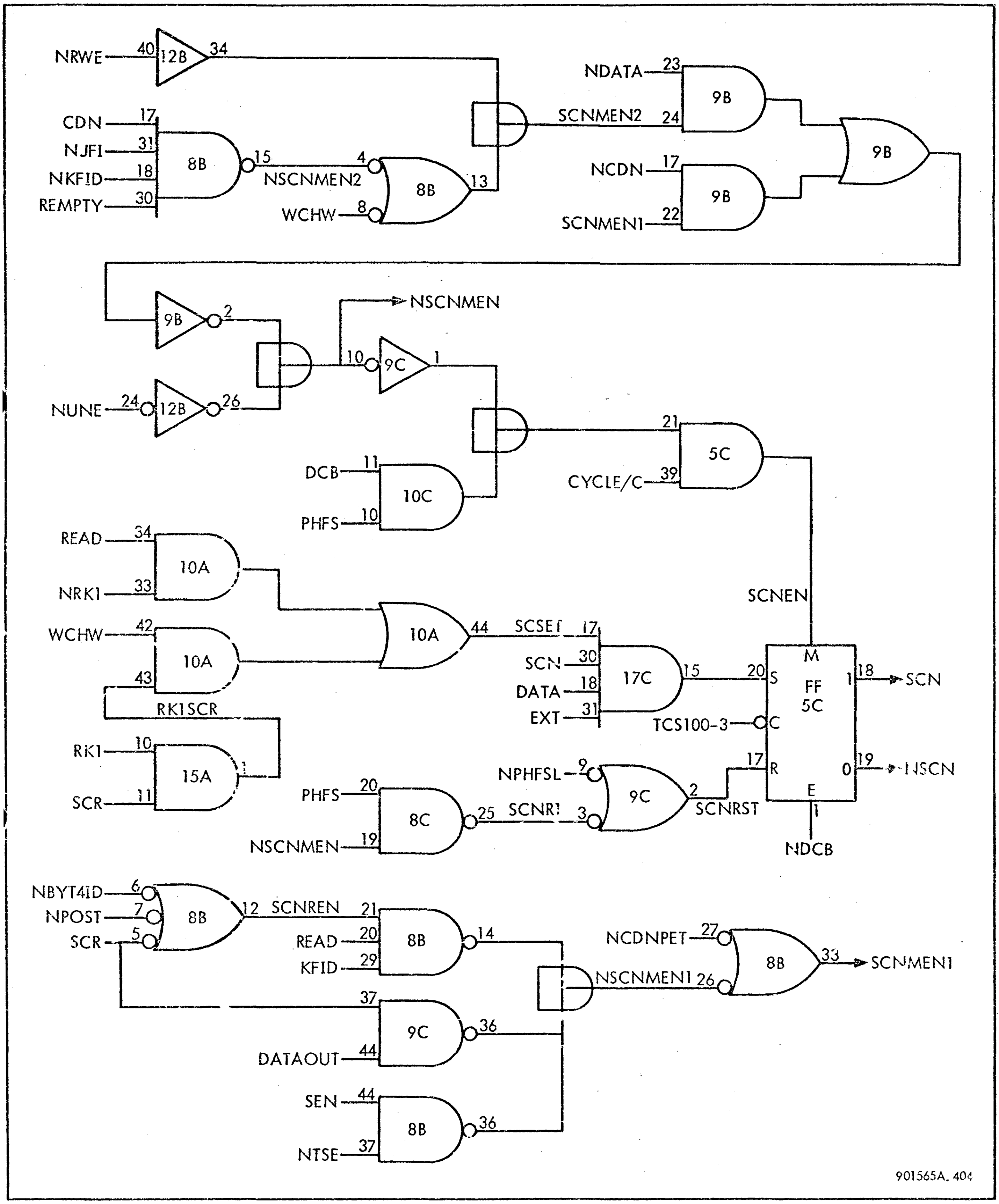


Figure 4-9. Service Call Flip-Flop SCN, Logic Diagram

After a service call involving data transfer is processed, additional service calls will be necessary unless all bytes required by the order have been transferred. However, if no additional service calls are necessary and SCN has been prevented from resetting on the previous service call, an additional service call will be requested unless SCN is reset in phase FS. (This condition can occur only for read orders, write orders, or checkwrite orders when the controller is operating in the extended performance mode.) If all bytes have not been transferred, SCN will be held in the set state after phase FS is entered; if all bytes have been transferred, SCN will be reset after phase FSL is entered.

M/SCN = CYCLE/C DCB PHFS N(NSCNMEN)

R/SCN = SCNRST

SCNRST = PHFS NSCNMEN + ...

C/SCN = TCS100-3 + ...

The conditions that generate a true N(NSCNMEN) signal are:

N(NSCNMEN) = UNE (Unusual End)
+ NDATA NRWE CDN NJFI NKFID REMPTY
+ NDATA NRWE NWCHW
+ NCDN DATAOUT SCR
+ NCDN SEN NTSE
+ NCDN READ KFID BYT4ID
+ NCDN READ KFID POST
+ NCDN READ KFID NSCR
+ NCDN CDNPET

4-33 Byte Counter

The byte counter is used during execution of seek orders and sense orders and during execution of read orders, write orders, or checkwrite orders for a multiple-byte IOP interface. For a sense order, the byte counter controls the transfer of data bytes into the K-register and O-register and raises the end data signal. For a seek order, the byte counter controls the transfer of data bytes from the J-register to the T-register and raises the end data signal. For read orders on a multiple-byte interface, the byte counter controls the transfer of data from the FAM module to the K-register or I-register. For write orders or checkwrite orders on a multiple-byte interface, the byte counter controls the transfer of data from the extended I-register to the lower order byte of the I-register.

The byte counter consists of flip-flops BK0 and BK1 and associated logic elements. Each byte of a service cycle is identified by states of the byte counter as follows:

BK0	BK1	Output Signal
0	0	BKWW
0	1	BKWZ
1	0	BKZW
1	1	BKZZ

When an I/O sequence is completed, BK0 and BK1 are direct reset after device controller busy flip-flop DCB is reset.

E/BK0 = NDCB-1

NDCB-1 = NDCB IOP + NDCB PET-1

E/BK1 = NDCB-1

Therefore, the byte counter (BK0, BK1) is in the (0, 0) state (BKWW true) when an SIO command is accepted from the IOP.

The byte counter is direct set to state (1, 1) when signal BKX1 is true. Signal BKX1 is true during phase RSA of an order out service cycle, when the J-register is filled during execution of a write order or checkwrite order and when the O-register is cleared during execution of a read order.

M/BK0 = BKX1

BKX1 = PHRSAOO + NBKX1EN

PHRSAOO = PHRSA ORDOUT (Phase RSA of order our service cycle)

NBKX1EN = WCHW JFIX1 (J-register filled in write or checkwrite)
+ READ KX0EN

KX0EN = OXKEN TCS100-3

OXKEN = PHRS DATAIN NED

(READ KX0EN, KX0EN, OXKEN: O-register cleared in read)

M/BK1 = BKX1

The byte counter is clocked on the falling edge of signal BKCK (which is equivalent to the rising edge of signal NBKCK).

S/BK0 = NBK0

R/BK0 = ...

C/BK0 = NBK1

S/BK1 = NBK1

R/BK1 = ...

C/BK1 = BKCK

As the byte counter (BK0, BK1) is clocked, it passes from state (1, 1) to state (1, 0), then state (0, 1), then state (0, 0) unless cleared or direct set.

When a seek order or sense order is to be executed, the byte counter is initially placed in state (1, 1) during phase RSA of the order out service cycle, then is counted down to control transfer of data.

NBKCK = PHRSA SEKSEND TCS000-3 + ...

When a read order is to be executed, the byte counter is used only if the controller is using a two- or four-byte interface (NBYT1ID).

NBKCK = BKCKEN TRS270 + ...

BKCKEN = NBYT1ID (READRR RREAD-1 + BKCKEN NTRS030 + ...)

READRR = READ RREAD-2

When a write order or a checkwrite order is executed, the byte counter is used only if the controller is operating with a two- or four-byte interface (NBYT1ID).

NBKCK = BKCKEN TRS270 + ...

BKCKEN = NBYT1ID (WCHW RWRITE-1 + BKCKEN NTRS030 + ...)

4-34 Terminal Order Operations

Terminal order phase TO is the last phase of any service cycle. During phase TO, flip-flop PHTO is in the set state and terminal order data may be received from the IOP. Terminal order data is accepted only if all data associated with the service cycle has been transferred (ED true), and if the IOP does not signal end of service (ES false). Under these conditions, terminal order data may be received on lines DA0R through DA3R, as follows:

IOP Signal	Flip-Flop	Function
DA0R	CIL	Request interrupt
DA1R	CDN	Indicate count done at end of I/O operation
DA2R	(none)	Command chaining
DA3R	UNE	Unusual end condition originating in IOP

The command chaining signal, which is sampled only at the end of an order in service cycle, is valid only if no unusual end condition exists. The command chaining signal is equivalent to:

CCH = IOP DA2R NDA3R

If the IOP orders command chaining, DCB is not reset at the end of an order in service cycle; if command chaining is not requested, DCB is reset.

R/DCB = DCBRST

DCBRST = DCBRST1 + ...

DCBRST1 = DCBRSTEN ORDIN PHTO

DCBRSTEN = N(CCH NES NUNE)

C/DCB = NTCS080

Flip-flops CIL, CDN, and UNE are controlled by signal TORD, which is true only when terminal order data is to be accepted.

TORD = IOP NES ED PHTO

If the IOP commands an interrupt, signal DA0R is true and CIL is set.

S/CIL = DA0R TORD

C/CIL = NTCS000

After CIL is set, an interrupt call is generated.

ICD = LIL

LIL = NAIOR CIL INC + ...

When the IOP responds to the interrupt call, CIL is reset.

R/CIL = CILRST

CILRST = AIOC + ...

C/CIL = NTCS000

After all data of the I/O operation have been transferred, the IOP causes signal DA1R to be true and sets CDN.

S/CDN = DA1R TORD

C/CDN = NTCS000

After CDN is set, an order in service cycle is requested. Flip-flop CDN is not reset until an order out service cycle takes place at the start of a new I/O sequence.

R/CDN = ORDOUT

C/CDN = NTCS000

If the IOP indicates an unusual end, signal DA3R is true and flip-flop UNE is set.

S/UNE = DA3R TORD

C/UNE = NTCS000

Flip-flop UNE can be set by conditions existing in the controller, as indicated in paragraph 4-72. Once set, UNE can be reset only by a manual reset signal or by a new SIO or HIO command.

E/UNE = MANRST

R/UNE = RESET

RESET = DVSEL HIOU PHFSL + DCBSET + ...

DCBSET = OPER SIOPOSS PHFSL

Exit from phase TO takes place 180 ns after the TCL delay line is started. If the IOP signals end of service, /ES/ is true during phase RSA and the TCL delay line is started immediately after entering phase TO.

DCL = CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART2 = PHTO ES + ...

If the IOP does not signal end of service, the TCL delay line is not started until a request strobe acknowledge has been received.

DCL = CYCLE/C DCLSTART1 + ...

DCLSTART1 = PHTO RSAU + ...

Transfer to phase TO cannot occur until end of data has been reached.

S/PHTO = PHRS ED

Therefore, signal TORD is true during phase TO if /ES/ was not true during phase RSA. Signal TORD allows the controller to store terminal order data in flip-flops CIL, CDN, or UNE.

4-35 End Data and End Service Logic

The end data and end service logic (figure 4-10) controls changes of state of the phase flip-flops. A true end service signal ESR can originate only in the IOP; a true end data signal EDR can originate in either the IOP or the controller. A true ESR signal is required to reset service connect flip-flop FSC and to disconnect the controller from the IOP. A true ED signal is required to enable an exit from phase RS and entry into phase TO.

The IOP generates a true /ES/ signal to end service. If signal ESR is true during phase RSA, signal ES comes true and is latched.

ES = ESET TCS000-2 + FSCU ES

ESET = IOP PHRSA ESR

Signal ES generates a true ED signal after exit from phase RSA.

ED = NPHRSA ES + FSCU ED + ...

Therefore, an /ES/ signal from the IOP terminates a service cycle and disconnects the controller.

The controller generates a true ED signal for all situations in which a true /ED/ signal is required from the IOP. A true ED signal is generated from EDD through EDR and EDU.

ED = EDSET TCS000-2 + FSCU ED + ...

EDSET = PHRSA EDU

EDU = EDR IOP + ...

EDR = EDD + /ED/

EDD = EDI FSC

Therefore, a true ED signal may be generated from the IOP through /ED/ or internally through EDD. Signal ED comes true during the last phase RSA of a service cycle and causes an end to the service cycle during the following RS phase.

For an order in service cycle or an order out service cycle, signal EDI is driven true by the DATA flip-flop.

EDI = EDISET1 NPHRSA + FSCU EDI + ...

EDISET1 = NDATA + ...

For a seek order, signal EDI is driven true when signal BKZW from the byte counter is true.

EDI = EDISET1 NPHRSA + FSCU EDI + ...

EDISET1 = SEEK BKZW + ...

For a sense order, signal EDI is driven true when signal BKWZ from the byte counter is true.

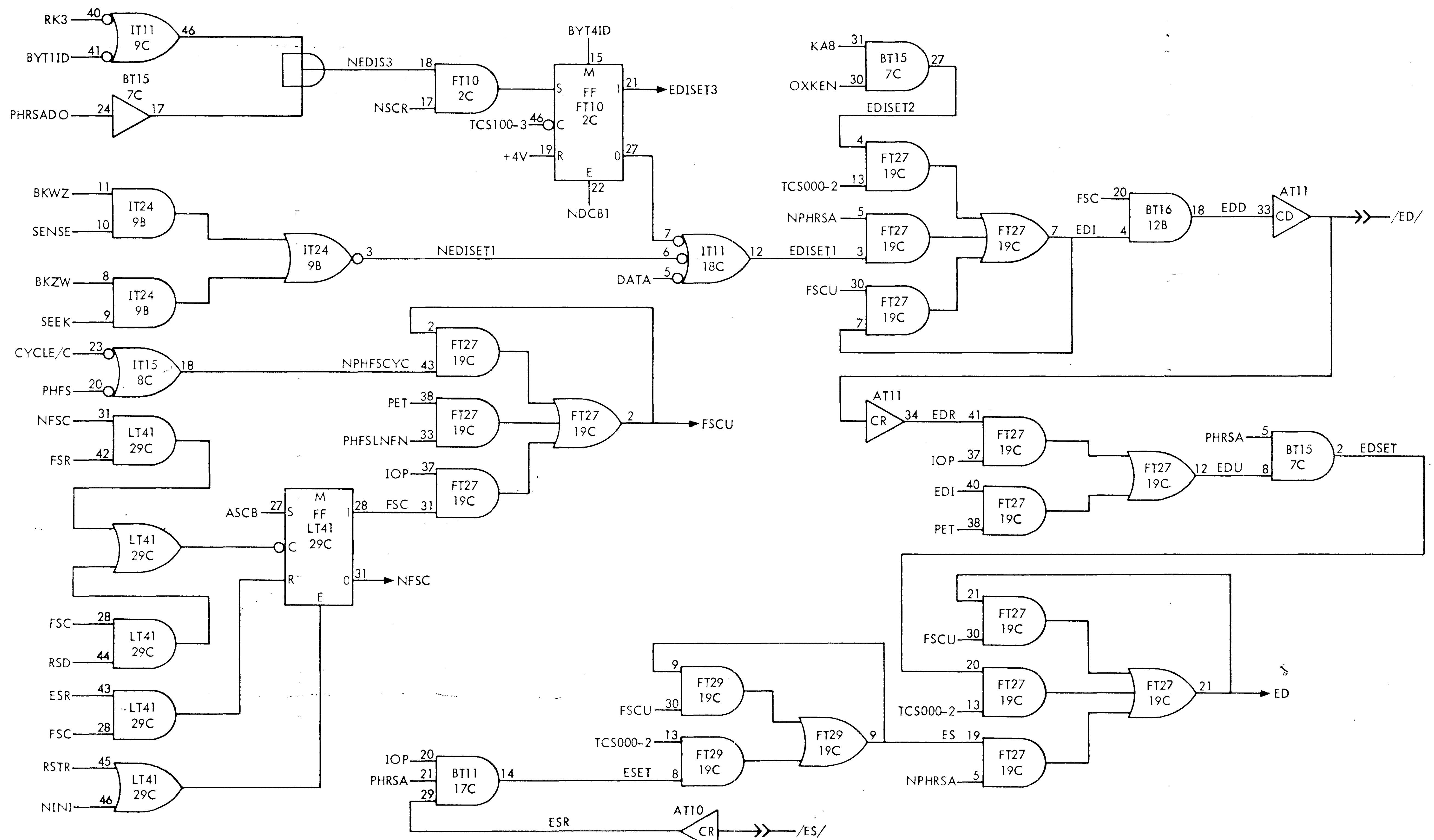


Figure 4-10. End Data and End Service Logic, Logic Diagram

901565A.419

EDI = EDISET1 NPHRSA + FSCU EDI + ...

EDISET1 = SENSE BKWZ + ...

For a read order, signal EDI is driven true when the FAM module is empty (KA8 true) and the last byte is being transferred to the O-register.

EDI = EDISET2 TCS000-2 + FSCU ED + ...

EDISET2 = KA8 OXKEN + ...

OXKEN = DATAIN PHRS NED

Signal KA8 can be true only after SCR has been set and the FAM module is empty. (See paragraph 4-42.) As the last data byte is read from the FAM module, a true KFISET signal allows KFI to latch true. If signal REMPTY is true, signal KA8 is true.

KA8 = N(NKA8) SCR

N(NKA8) = KA8 KFID + KFIDX1 REMPTY

KFID = KX0 (KFID + KFIDX1)

KFIDX1 = KFI TRS270

KFI = KX0 (KFIX1 + KFI NPHRSAOO)

KFIX1 = KFISET RREAD-2 TRS130

For a write order or a checkwrite order, signal EDI is driven true when flip-flop EDISET3 is set.

EDI = EDISET1 NPHRSA + FSCU EDI + ...

EDISET1 = EDISET3 + ...

If the controller is operating with a four-byte interface, all four data bytes are transferred at once so that data input ends in one data out service cycle. Therefore, EDISET3 is direct set for operation with a four-byte interface.

M/EDISET3 = BYT4ID

For a one- or a two-byte interface, flip-flop EDISET3 is set after all four data bytes have been accepted. For a one-byte interface, EDISET3 is set when byte 15 is received, and /ED/ is driven true when byte 16 is requested. Refer to paragraph 4-42 for operation of the RK-counter.

S/EDISET3 = NEDIS3 NSCR

NEDIS3 = PHRSADO NRK3 + ...

C/EDISET3 = TCS100-3

For a two-byte interface, EDISET3 is set when bytes 13 and 14 are received, and /ED/ is driven true when bytes 15 and 16 are requested.

S/EDISET3 = NEDIS3 NSCR

NEDIS3 = PHRSADO NBYT1ID + ...

C/EDISET3 = TCS100-3

Flip-flop EDISET3 is direct reset when the controller is not busy.

E/EDISET3 = NDCB1

4-36 INPUT/OUTPUT DATA BUFFER

The registers of the input/output data buffer store data accepted from the IOP for transfer to the FAM module and store data accepted from the FAM module for transfer to the IOP.

4-37 I-Register

The I-register consists of buffered latches I00 through I31 and associated logic elements. During execution of a write order or checkwrite order, data bytes are accepted from the IOP and are transferred from the higher order byte of the I-register (I00 through I07) to the J-register. If the controller is operating with a two- or four-byte interface, data must be transferred from lower order bytes of the I-register to the higher order byte for transfer to the J-register. During execution of a read order, the lower order bytes of the I-register are used if the controller is operating with a two- or four-byte interface. In these cases, the I-register accepts data from the FAM module for transfer to the O-register. During execution of a seek order, two consecutive data bytes are transferred from the IOP to the I-register, then from the I-register to the J-register.

During phase RSA of a data out service cycle (write order, checkwrite order, or seek order), IOP data is stored in the I-register. For a write order or checkwrite order, the data path may be 8 bits, 16 bits, or 32 bits wide.

Byte 1:

I00 = DA0R IXD-1 + ...

IXD = (IXD-1 through IXD-4)

IXD = PHRSADO TCS000-3

PHRSADO = PHRSA DATAOUT

I01 = DA1R IXD-1 + ...

. .

. .

. .

I07 = DA7R IXD-1 + ...

```
I08 = DB0R IXD-2 + ...  ⎫
 .        .             ⎪
 .        .             ⎬ Byte 2
 .        .             ⎪
I15 = DB7R IXD-2 + ...  ⎭

I16 = DC0R IXD-3 + ...  ⎫
 .        .             ⎪
 .        .             ⎬ Byte 3
 .        .             ⎪
I23 = DC7R IXD-3 + ...  ⎭

I24 = DD0R IXD-4 + ...  ⎫
 .        .             ⎪
 .        .             ⎬ Byte 4
 .        .             ⎪
I31 = DD7R IXD-4 + ...  ⎭
```

For a controller operating with a two- or four-byte interface, data bytes accepted from the IOP are transferred to the higher order byte under control of the byte counter (BK0, BK1). Refer to paragraph 4-33 for a description of the byte counter.

Transfer from (I08 through I15) to (I00 through I07) takes place after the first data transfer from (I00 through I07) to the J-register.

```
I00              = I08 IXI-1 + ...               ⎫
    IXI-1        = RWRITEDO IXEN BKZZ            ⎪
    RWRITEDO     = RWRITE-2 DATAOUT              ⎪
    IXEN         = NBYT1ID NTRL240 TRL180        ⎬ Byte 2
I01              = I09 IXI-1 + ...               ⎪
 .                    .                          ⎪
 .                    .                          ⎪
 .                    .                          ⎪
I07              = I15 IXI-1 + ...               ⎭
```

Signals TRL240, TRL180, and RWRITE-2 are generated by the TRL delay line. Signal BKZZ is generated by the byte counter.

Data transfer from (I16 through I23) and (I24 through I31) to (I00 through I07) take place under the control of the byte counter.

```
I00          = I16 IXI-2 + ...          ⎫
    IXI-2    = RWRITEDO IXEN BKZW       ⎪
I01          = I17 IXI-2 + ...          ⎬ Byte 3
 .                 .                    ⎪
 .                 .                    ⎪
I07          = I23 IXI-2 + ...          ⎭
```

```
I00          = I24 IXI-3 + ...          ⎫
    IXI-3    = RWRITEDO IXEN BKWZ       ⎪
I01          = I24 IXI-3 + ...          ⎬ Byte 4
 .                 .                    ⎪
 .                 .                    ⎪
 .                 .                    ⎪
I07          = I31 IXI-3 + ...          ⎭
```

During execution of a read order for a controller using a two- or a four-byte interface, data bytes are transferred from the FAM module (R00 through R07) to the I-register.

```
I08            = IXR-1 R00 + ...              ⎫
    IXR-1      = READRR BKZW IXEN             ⎪
    IXEN       = NBYT1ID NTRL240 TRL180       ⎪
    READRR     = READ RREAD-2                 ⎬ Byte 2
I09            = IXR-1 R01 + ...              ⎪
 .                     .                      ⎪
 .                     .                      ⎪
 .                     .                      ⎪
I15            = IXR-1 R07 + ...              ⎭
```

Signals TRL240, TRL180, and RREAD-2 are controlled by the TRL delay line. Signal BKZW is controlled by the byte counter. (This transfer takes place at the same time that data transfers are made between bytes of the I-register.)

```
I16          = R00 IXR-2 + ...            ⎫
    IXR-2    = READRR IXEN BKWZ + ...     ⎪
I17          = R01 IXR-2 + ...            ⎬ Byte 3
 .                  .                     ⎪
 .                  .                     ⎪
 .                  .                     ⎪
I23          = R07 IXR-2 + ...            ⎭

I24          = R00 IXR-3 + ...            ⎫
    IXR-3    = READRR IXEN BKWW + ...     ⎪
I25          = R01 IXR-3 + ...            ⎬ Byte 4
 .                  .                     ⎪
 .                  .                     ⎪
 .                  .                     ⎪
I31          = R07 IXR-3 + ...            ⎭
```

Signals IX0-1 through IX0-4 are used to clear the I-register before data is stored and to retain data stored in the I-register. Data is cleared when the signal is false and is retained while the signal is true.

```
I00            = I00 IX0-1 + ...     ⎫
  .                  .               ⎪
  .                  .               ⎪
  .                  .               ⎪
I07            = I07 IX0-1 + ...     ⎪ Byte
                                     ⎬ 1
NIX0-1         = RWRITEDO TRS130 NTRS180
                 + PHRSAOUT TCS000-1 ⎪
                                     ⎪
    PHRSAOUT   = PHRSA NIN           ⎭

I08            = I08 IX0-2 + ...  ⎫
  .                  .            ⎪
  .                  .            ⎬ Byte 2
  .                  .            ⎪
I15            = I15 IX0-3 + ...  ⎭

I16            = I16 IX0-3 + ...  ⎫
  .                  .            ⎪
  .                  .            ⎬ Byte 3
  .                  .            ⎪
I23            = I23 IX0-3 + ...  ⎭

I24            = I24 IX0-4 + ...  ⎫
  .                  .            ⎪
  .                  .            ⎬ Byte 4
  .                  .            ⎪
I31            = I31 IX0-4 + ...  ⎭

(IX0-2 - IX0-4) = IX0

NIX0           = PHRSAOUT TCS000-1 + KX0EN

    PHRSAOUT   = PHRSA NIN       { Clear after data
                                 { transfer from IOP

    KX0EN      = OXKEN TCS100-3  { Clear after
                                 { data transfer
    OXKEN      = DATAIN PHRS NED { to IOP
```

4-38 O-Register

The O-register, which consists of buffered latches O00 through O31 and associated logic elements, stores data for transfer to the IOP. During phase RS of a data in service cycle, the contents of the K-register are transferred to bits 0 through 7 of the O-register, and the contents of the I-register bits 8 through 31 are transferred to bits 8 through 31 of the O-register. (If the controller is operating with a one-byte interface, only the K-register contains data; if the controller is operating with a two-byte interface, only the K-register and bits 8 through 15 of the I-register contain data. For a four-byte interface, all signals contain data.) Since a data in service cycle is part of a read order and a sense order, the O-register is loaded from the K-register or I-register for execution of these orders.

```
(OXK-1 - OXK-4) = OXK

O00             = K00 OXK          ⎫
                  + ...            ⎪
                                   ⎪
    OXK         = OXKEN            ⎪ Store contents
                  TCS000-2         ⎪ of K-register
                                   ⎬ in (O00-O07)
    OXKEN       = DATAIN           ⎪ (Read order or
                  PHRS NED         ⎪ sense order)
                                   ⎪
O01             = K01 OXK + ...    ⎪
  .                  .             ⎪
  .                  .             ⎪
  .                  .             ⎪
O07             = K07 OXK + ...    ⎭

O08             = I08 OXK + ...    ⎫ Store contents
  .                  .             ⎪ of (I08-I31)
  .                  .             ⎬ in (O08-O31)
  .                  .             ⎪ (Read order
O31             = I31 OXK + ...    ⎭ only)
```

Signal OX0 is used to clear the O-register before storage of new data and to retain the stored data. The O-register is cleared when signal OX0 is false and retains data while signal OX0 is true. Signal OX0 is equivalent to request strobe signal RSD.

```
(OX0-1 - OX0-4) = OX0

O00             = O00 OX0 + ...

    OX0         = RSD

O01             = O01 OX0 + ...
  .                   .
  .                   .
  .                   .
O31             = O31 OX0 + ...
```

During execution of orders, signal RSD becomes true when a strobe is requested from the IOP and is latched until the request strobe is acknowledged.

```
RSD     = FSC NRSAR (PHRS TCS000-2
          + RSET NPHRSA + FSCU RSD)

    FSCU = FSC IOP + ...

    RSET = PHFSL NIN
```

After RSD is true, data is stored in the O-register. After the data is read by the IOP, RSAR becomes true and RSD is false.

During execution of a sense order, the track protect bit from the selection unit (TRPR) and bits 0 through 6 of the track address are stored in the O-register while the byte counter indicates byte zero (BKZZ).

```
O00            = OXSENSE1 TRPR + ...

    OXSENSE1   = SENSE OXKEN BKZZ

O01            = OXSENSE1 T00 + ...
 .                  .
 .                  .
 .                  .
O07            = OXSENSE1 T06 + ...
```

(Additional bytes of the sense order are transferred to the O-register from the K-register.)

During phase RS of an order in service cycle, four bits of control information are sent to the IOP from the O-register.

```
O00            = OXORDIN TER   (Control error,
                 + ...          parity error, or
                                rate error)
    TER        = CER + PER + RER
    OXORDIN    = ORDIN PHRSNED
    PHRSNED    = PHRS NED
O01            = OXORDIN INL   (Incorrect length)
                 + ...
O03            = OXORDIN + ... (Always true)
O04            = OXORDIN UNE   (Unusual end)
                 + ...
```

When the controller responds to an AIO signal, three bits of information are sent to the IOP from the O-register.

```
O00            = OXAIOST RER   (Rate error)
                 + ...

    OXAIOST    = AIOC FSU

O02            = OXAIOST SUN (Sector unavailable)
                 + ...

O03            = OXAIOST WPV (Write protect
                 + ...         violation)
```

The conditions which control flip-flops TER, INL, UNE, RER, SUN, and WPV are described in paragraph 4-72.

4-39 J-Register

The J-register consists of buffered latches J00 through J07 and associated logic elements. During execution of a write order or checkwrite order, the J-register accepts data from the I-register for transfer to the FAM module. During execution of a read order, the J-register accepts data from the D-register for transfer to the FAM module. During execution of a seek order, the J-register accepts two bytes of data from the I-register to the T-register and S-register.

During execution of a write order or checkwrite order, data from the higher order byte of the I-register (I00 through I07) is transferred to the J-register. If the controller is operating with an 8-bit interface (BYT1ID), the transfer takes place during phase RS under control of the TCL delay line.

```
J00            = I00 JXI1B + ...

    JXI1B      = IOP BYT1ID PHRSDO TCS000-2

    PHRSDO     = PHRS DATAOUT

J01            = I01 JXI1B + ...
 .                  .
 .                  .
 .                  .
J07            = I07 JXI1B + ...
```

If the controller is operating with a 16- or 32-bit interface (NBYT1ID), transfer of data from the I-register to the J-register must allow time for transfer from higher to lower order bytes of the I-register (refer to paragraph 4-37 for a description of the I-register). Therefore, for 16- or 32-bit interface operations, the transfer is controlled by the TRL delay line.

```
J00            = I00 JXIN1B + ...

    JXIN1B     = IOP NBYT1ID DATAOUT
                 RWRITE-2 TRS060

J01            = J01 JXIN1B + ...
 .                  .
 .                  .
 .                  .
J07            = I07 JXIN1B + ...
```

During execution of a read order, data bytes are transferred from the D-register to the J-register. This transfer takes place after the preamble has been detected (NPRE) under control of the TDL delay line (TDT2).

```
J00        = D00 JXD + ...

    JXD    = READ NPRE TDT2

J01        = D01 JXD + ...
 .              .
 .              .
 .              .
J07        = D07 JXD + ...
```

If the controller is operating offline, the J-register accepts PET-generated signals under control of the TRL delay line.

J00 = DP00 JXDP + ...

JXDP = PET-1 RWRITE-2 TRS060 DATAOUT

J01 = DP01 JXDP + ...

.
.
.

J07 = DP07 JXDP + ...

Signal JX0 is used to clear the J-register before storage of new data and to retain the stored data. The J-register is cleared when signal JX0 is false and retains the stored data while signal JX0 is true.

J00 = J00 JX0 + ...

.
.
.

J07 = J07 JX0 + ...

During execution of a read order, the J-register is cleared just before data is stored.

NJX0 = READ TDT1 + ...

During execution of a write order or a checkwrite order, the J-register is cleared by a signal related to the signal which causes data transfer. For a one-byte interface the J-register is always cleared during phase RS of a data out service cycle.

NJX0 = PHRSDO TC3000-1 + ...

For a two- or four-byte interface, the J-register is cleared during each FAM write cycle.

NJX0 = RWRITE-2 TRS270 NTRS000 NBYT11D + ...

4-40 FAST ACCESS MEMORY (FAM) CIRCUITS

FAM circuits consist of the TRL delay line, the RK-counter, the J-pointer register (JP-register), the K-pointer register (KP-register), one FT25 Fast Access Memory module (FT25 FAM module), and interconnecting logic elements. (See figure 4-11.)

FAM circuits are used only during execution of a read order, a write order, or a checkwrite order. During execution of a write order or a checkwrite order, data bytes pass from the IOP through the I-register, the J-register, the FAM module, the K-register, and the D-register to the selection unit. (See figure 3-6.) During execution of a read order, data bytes pass from the selection unit through the D-register, the J-register, the FAM module, the K-register, and the O-register, to the IOP. For a two- or four-byte interface width between the controller and the IOP, data bytes pass from the FAM module to the K-register and the I-register, then through the O-register to the IOP. (See figure 3-7.) Thus, data bytes pass from the J-register to the FAM module, and from the FAM module to the K-register (or the I-register) regardless of the direction of data flow between the IOP and a selection unit.

The TRL delay line is started each time a data byte is to be written into the FAM module (FAM write cycle) or read from the FAM module (FAM read cycle). The RK-counter keeps track of the number of active bytes in the FAM module (bytes written into, but not yet read from, the FAM module). The L-register addresses a location in the FAM module into which a byte is written, or from which a byte is read, and generates outputs that indicate the next FAM module location addressed. During a FAM write cycle, the JP-register accepts from the L-register the address of the next FAM module location into which a byte is written. During a FAM read cycle, the KP-register accepts from the L-register the address of the next FAM module location from which a byte is read.

The FAM module (figure 4-12) contains 16 addressable eight-bit registers. The four-bit address determines which of the 16 registers is available for input or output. A data byte is stored in the addressed register as the input clock signal goes false. Data may be read from the addressed location at any time.

4-41 TRL Delay Line

The TRL delay line (figure 4-13), which consists of a 300-ns delay line and associated gates, controls data transfer into and out of the FAM module, increment and decrement of the RK-counter, and transfer of addresses from the L-register to the KP-register or the JP-register. During the execution of a seek order, the TRL delay line controls storage of data into the T-register and the S-register.

While device controller busy flip-flop DCB is in the reset state, CYCLER is true and remains latched after DCB is set by an accepted SIO command.

CYCLER = NTRS030 (NDCB + CYCLER + ...)
14002

When SREAD (or SWRITE) comes true during execution of an order, the TRL delay line is started. After a 30-ns delay, a true TRS030 signal inhibits the inputs, the signal CYCLER goes false, and the SREAD (or SWRITE) signal does not control the delay line. After a 130-ns delay, a true TRS130 signal inhibits the SREAD (or SWRITE) signal.

SREAD = NTRS130 NREMPTY (DCB SREAD + ...)

SWRITE = NTRS130 RK0 (DCB SWRITE + ...)

Because the CYCLER signal is an input to starting gates for SREAD and SWRITE, the SREAD and SWRITE signal cannot

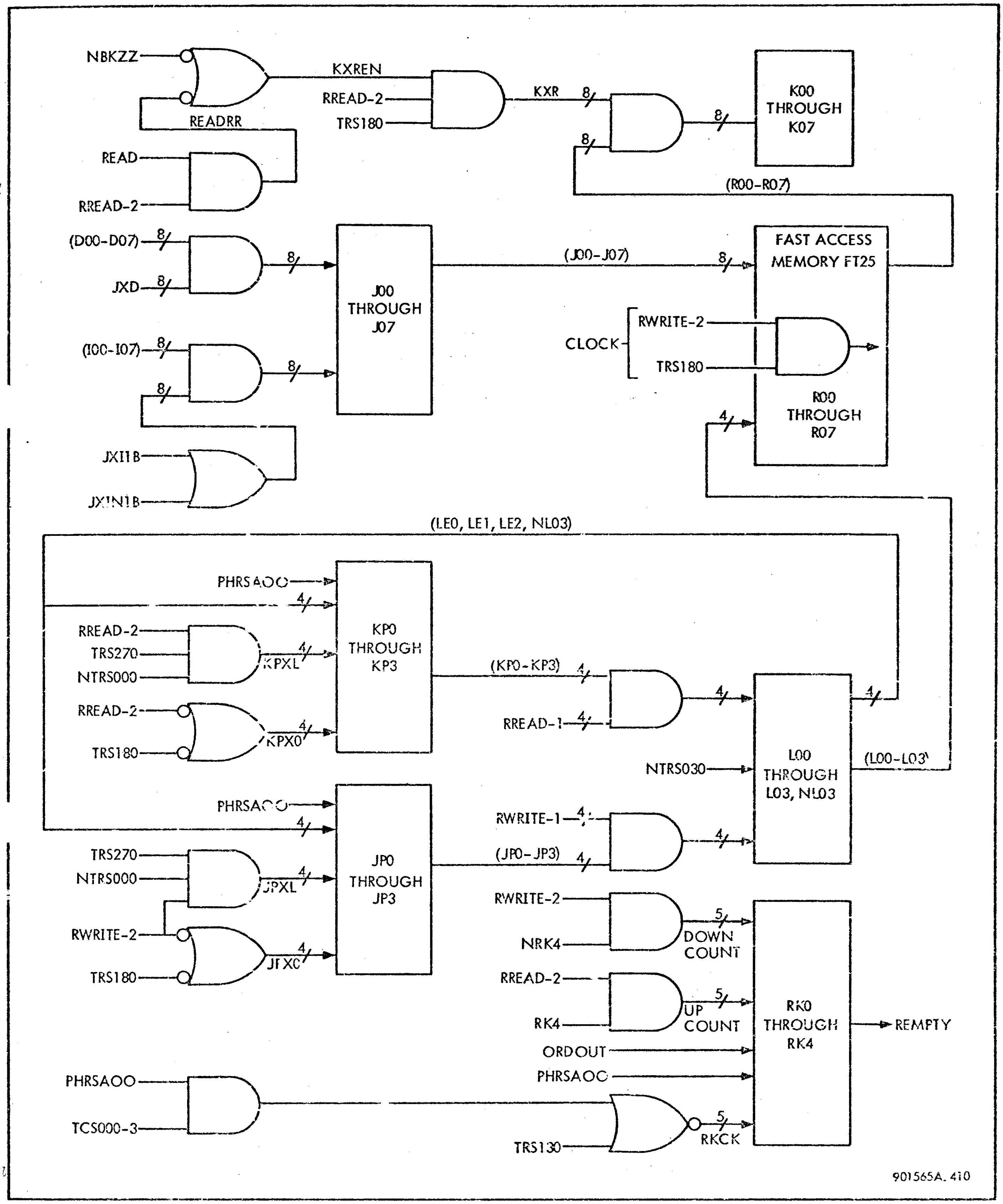


Figure 4-11. FAM Circuits, Simplified Logic Diagram

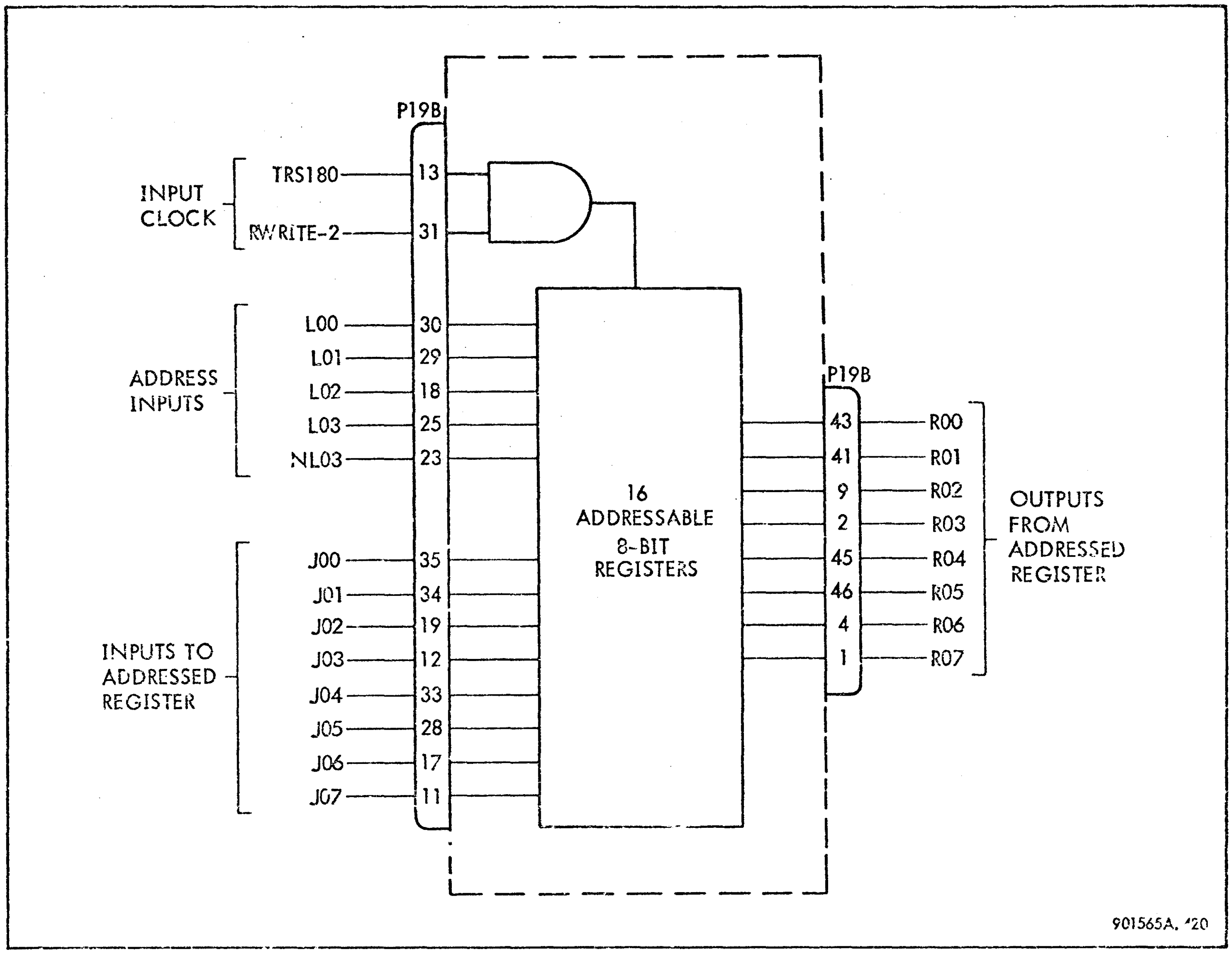


Figure 4-12. FAM Module, Block Diagram

start a new TRL delay line cycle until the previous cycle is complete.

SWRITE = NTRS130 RK0 (CYCLER JFI NTRS000 + ...)

SREAD = NTRS130 NREMPTY (CYCLER NTRS000 NKFI SREADEN + CYCLER NTRS000 NFKI READ + ...)

After a 300-ns delay, CYCLER becomes true and is latched, allowing the SREAD (or SWRITE) signal to start the delay line if required.

CYCLER = NTRS030 (TRS300 + CYCLER + ...)

The SWRITE signal cannot be true unless the J-register-filled signal JFI is true. Signal JFI is true after data has been stored in the J-register. When the FAM module is full, flip-flop RK0 is set and the SWRITE signal is inhibited, preventing any additional FAM write cycles. The SREAD signal cannot be true unless the K-register-filled signal KFI is false. Signal KFI is true after data has been stored in the K-register and is not false until the data has been transferred from the K-register during execution of an order. When the RK-counter indicates that all active bytes have been read from the FAM module, a true REMPTY signal inhibits the SREAD signal, preventing any additional FAM read cycles.

During execution of a read order, write order, or check-write order, FAM write cycles and FAM read cycles may occur in any sequence, under control of signals KFI and JFI. When signal JFI is true and signal KFI is false, signal SWRITE and signal SREAD are both true. When CYCLER comes true at the end of a FAM write cycle or FAM read

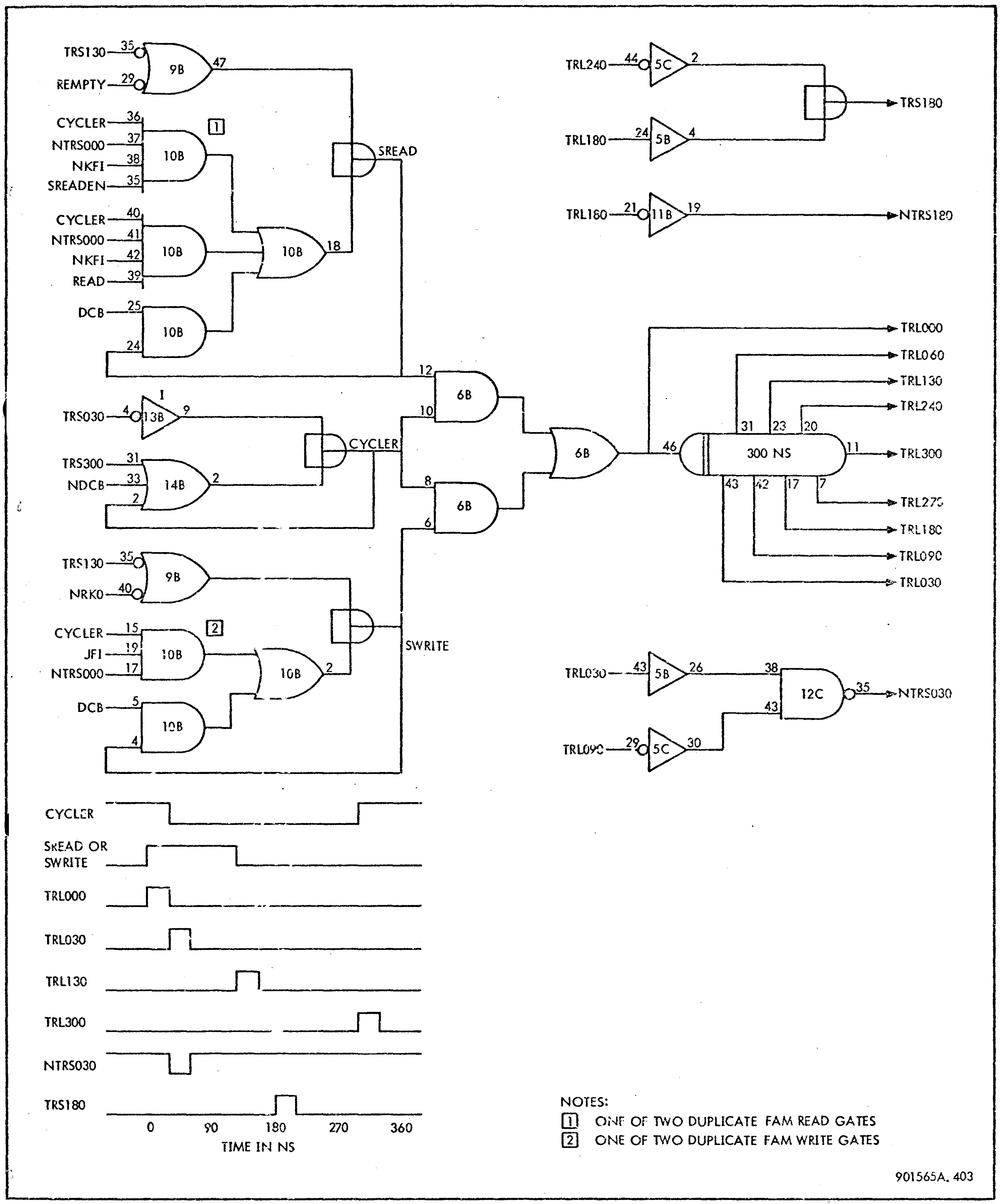


Figure 4-13. TRL Delay Line, Logic and Timing Diagram

cycle, the TRL delay line is started by both signals. However, either a FAM write cycle or a FAM read cycle can occur, but not both. Priority is established by signals which detect the type of order being executed. If a write order or checkwrite order is being executed, signal WCHW is true and data transfers from the FAM module to the K-register have priority; therefore, a FAM read cycle must take precedence over a FAM write cycle. If a read order is being executed, signal READ is true and data transfers from the J-register to the FAM module have priority; therefore, a FAM write cycle must take precedence over a FAM read cycle.

The following signals control operations during a FAM write cycle.

RWRITE-1 = N(SREAD WCHW) (SWRITE TRS030 + RWRITE-1 NTRS000) NTRS130

RWRITE-2 = N(SREAD WCHW) (SWRITE TRS030 + RWRITE-2 NTRS000)

RWRITE-N4 = RWRITE-2 NRK4

The following signals control operations during a FAM read cycle.

RREAD-1 = N(READ SWRITE)(SREAD TRS030 + RREAD-1 NTRS000) NTRS130

RREAD-2 = N(READ SWRITE)(SREAD TRS030 + RREAD-2 NTRS000)

RREAD-4 = RREAD-2 RK4

If both SWRITE and SREAD are true, only one of these two sets of signals are valid. If signal WCHW is true, a FAM read cycle occurs because the factor N(SREAD WCHW) is false. If signal READ is true, a FAM write cycle occurs because the factor N(READ SWRITE) is false.

4-42 RK-Counter

During execution of a read order, write order, or checkwrite order, a data byte is transferred from the J-register into an addressed location in the FAM module during a FAM write cycle, or read from the FAM module into the K-register (or the I-register) during a FAM read cycle. The RK-counter, which consists of flip-flops RK0 through RK4 and associated logic elements, keeps track of the number of active bytes in the FAM module.

During phase RSA of an order out service cycle, RK0 through RK3 are set and RK4 is direct set. Clocking takes place at the rising edge of TCL delay line signal TCS000-3.

M/RK4 = PHRSAOO

PHRSAOO = PHRSA ORDOUT

(S/RK0-S/RK3) = ORDOUT

(C/RK0-C/RK3) = RKCK

RKCK = N(PHRSAOO TCS000-3 + ...)

For service cycles other than order out, clocking for all flip-flops takes place at the rising edge of TRL delay line signal TRS130.

(C/RK0-C/RK4) = RKCK

RKCK = N(TRS130 + ...)

Flip-flops RK0 through RK3 form an up/down counter clocked by signal RKCK and controlled by flip-flop RK4. Flip-flop RK4 changes state at each clock and controls all read count gates through signal RREAD-4 and controls all write count gates through signal RWRITE-N4.

S/RK4 = NRK4

R/RK4 = ...

RREAD-4 = RREAD-2 RK4

RWRITE-N4 = RWRITE-2 NRK4

Therefore, read count gates are enabled during a FAM read cycle, and write count gates are enabled during a FAM write cycle.

If signal RREAD-4 is true when the flip-flops are clocked, the flip-flops count up, as indicated in table 4-3.

S/RK0 = RREAD-4 NRK0 RK1 RK2 RK3 + ...

R/RK0 = RREAD-4 RK1 RK2 RK3 + ...

S/RK1 = RREAD-4 NRK1 RK2 RK3 + ...

R/RK1 = RREAD-4 RK2 RK3 + ...

S/RK2 = RREAD-4 NRK2 RK3 + ...

R/RK2 = RREAD-4 RK3 + ...

S/RK3 = RREAD-4 NRK3 + ...

R/RK3 = RREAD-4 + ...

If signal RWRITE-N4 is true when the flip-flops are clocked, the flip-flops count down, as indicated in table 4-3.

S/RK0 = RWRITE-N4 NRK0 NRK1 NRK2 NRK3 +...

R/RK0 = RWRITE-N4 NRK1 NRK2 NRK3 + ...

S/RK1 = RWRITE-N4 NRK1 NRK2 NRK3 + ...

R/RK1 = RWRITE-N4 NRK2 NRK3 + ...

S/RK2 = RWRITE-N4 NRK2 NRK3 + ...

R/RK2 = RWRITE-N4 NRK3 + ...

S/RK3 = RWRITE-N4 NRK3 + ...

R/RK3 = RWRITE-N4 + ...

Signals indicating the state of the RK-counter provide inputs to the TRL delay line (paragraph 4-41), the service call logic (paragraph 4-32), and the end data and end service logic (paragraph 4-35). At the start of a data out or a data in service cycle, the RK-counter (RK0 RK1 RK2 RK3 RK4) is in state (1 1111). For either type of service cycle, data bytes are first written into the FAM module, causing a countdown for each byte written. As a byte is read from the FAM module, a countup occurs. If the RK-counter reaches state (0 1111), 16 active bytes are stored in the FAM module and the SWRITE signal is inhibited, preventing any additional FAM write cycles until an active byte is read from the FAM module.

SWRITE = NTRS130 RK0 (DCB SWRITE + ...)

Table 4-3. Operation of the RK-Counter

PRESENT STATE					NEXT STATE									
					If RWRITE-N4 Is True					If RREAD-4 Is True				
RK0	RK1	RK2	RK3	RK4	RK0	RK1	RK2	RK3	RK4	RK0	RK1	RK2	RK3	RK4
1	0	0	0	0	0	1	1	1	1	1	0	0	0	1
1	0	0	0	1	1	0	0	0	0	1	0	0	1	0
1	0	0	1	0	1	0	0	0	1	1	0	0	1	1
1	0	0	1	1	1	0	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	0	1	1	1	0	1	0	1
1	0	1	0	1	1	0	1	0	0	1	0	1	1	0
1	0	1	1	0	1	0	1	0	1	1	0	1	1	1
1	0	1	1	1	1	0	1	1	0	1	1	0	0	0
1	1	0	0	0	1	0	1	1	1	1	1	0	0	1
1	1	0	0	1	1	1	0	0	0	1	1	0	1	0
1	1	0	1	0	1	1	0	0	1	1	1	0	1	1
1	1	0	1	1	1	1	0	1	0	1	1	1	0	0
1	1	1	0	0	1	1	0	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	0	0	1	1	1	1	0
1	1	1	1	0	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	(Inhibited)				

Notes

1. The number of active bytes in the FAM module is indicated by the ones complement of the RK-counter state (1 1111 indicates 0 active bytes; 0 1111 indicates 16 active bytes)

2. Initial state (1 1111) can be followed only by a FAM write cycle; a subsequent state (1 1111) inhibits the FAM read cycle

If the RK-counter reaches state (1 1111) after bytes have been written into the FAM module, all active bytes have been read. Therefore, signal REMPTY becomes true, inhibiting the SREAD signal and preventing any additional FAM read cycles until a byte is written into the FAM module.

SREAD = NTRS130 NREMPTY (DCB SREAD + ...)

REMPTY = RK0 RK1 RK2 RK3 RK4

Flip-flop SCR is controlled by RK-counter signals, and in turn controls service call flip-flop SCN and end data flip-flop EDISET3. SCR is direct set during phase RSA of an order out service cycle.

M/SCR = PHRSAOO

During a data out or a data in service cycle, SCR is clocked by RKCK and changes state under control of RK-counter signals.

S/SCR = RREAD-2 SCRSET

SCRSET = NSCSET RK2 NRK3 NRK4

SCSET = WCHW RK1SCR + READ NRK1

RK1SCR = RK1 SCR

R/SCR = SCRSET

C/SCR = RKCK

If the controller is executing a write order or a checkwrite order (WCHW true), SCSET is true until RK1 is reset, so that SCRSET is false until RK1 is reset. Therefore, SCR will remain in the set state until the RK-counter is in state (1 0100), indicating that 11 active bytes are in the FAM module. If a FAM read cycle occurs at this time, RREAD-2 will come true and SCR will remain in the set state as the RK-counter goes to state (1 0101) to indicate that there are 10 active bytes in the FAM module. If a FAM write cycle occurs at this time, RREAD-2 will be false and SCR will be reset as the RK-counter goes to state (1 0011) to indicate that there are 12 active bytes in the FAM module.

If the controller is executing a read order (READ true), SCSET is false until RK1 is reset, so that SCRSET becomes true when the RK-counter is in state (1 1100), indicating that there are three active bytes in the FAM module. If a FAM read cycle occurs at this time, RREAD-2 will come true and SCR will remain in the set state as the RK-counter goes to state (1 1101) to indicate that there are two active bytes in the FAM module. If a FAM write cycle occurs at this time, RREAD-2 will be false and SCR will be reset as the RK-counter goes to state (1 1011) to indicate that there are four active bytes in the FAM module.

At the start of a data out service cycle following an order out service cycle, SCN is direct set. This action is caused by SCR, which is direct set during phase FS of the order out service cycle.

NSCNMEN1 = DATAOUT SCR + ...

The input/output operation begins with at least three service cycles, causing 12 bytes to be written into the FAM module before SCR is reset. Signal SCSET prevents reset of SCN during phase FSL, so that SCN is not reset until at least seven active bytes are in the FAM module.

S/SCN = SCNEN

SCNEN = SCN DATA EXT SCSET

SCSET = WCHW RK1SCR + ...

Since SCN is not reset until phase FSL, an additional service cycle of four bytes is in process and 12 bytes are written.

After the initial service cycles, SCR is set whenever there are 11 active bytes in the FAM module (1 0100), and a FAM read cycle occurs. After SCR is set, SCN is set again to request a service cycle. At the start of a data in service cycle following an order out service cycle, SCN is in the reset state. After four bytes have been written into the FAM module, SCR is reset and SCN is direct set.

NSCNMEN1 = READ RKID SCNREN + ...

SCNREN = NSCR + ...

Signal SCSET prevents reset of SCN during phase FSL, so that SCN is not reset if there are eight or more active bytes in the FAM module.

S/SCN = SCNEN

SCNEN = SCN DATA EXT SCSET

SCSET = READ NRK1 + ...

After the initial service calls, additional bytes are written into the FAM module. If a FAM read cycle takes place while there are three active bytes in the FAM module (1 1100), SCR is set, thereby inhibiting any service call when there are less than four bytes in the FAM module. For any other condition, SCR is reset and a service call may be requested.

An end service signal is generated during phase RSA of a data out service cycle if SCR is reset (12 or more active bytes in the FAM module).

S/EDISET3 = NSCR NEDIS3 + ...

NEDIS3 = PHRSADO (NRK3 + NBYT1ID)

For a multiple-byte interface, this flip-flop is set after 12 active bytes are in the FAM module (1 0011); for a single-byte interface, this flip-flop is set after 14 active bytes are in the FAM module (1 0001).

4-43 JP-Register

The J-pointer register (JP-register), which consists of buffered latches JP0 through JP3, stores the address of the next FAM location to be selected for writing data from the J-register. During a FAM write cycle, the address stored in the JP-register is placed in the L-register for addressing a location in the FAM module and a new address is accepted from outputs of the L-register. (See figure 4-14.)

During phase RSA of an order out service cycle, the address 1111 is stored in the JP-register. Therefore, the first FAM location addressed for writing is always location 1111.

JP0 = PHRSAOO + ...

PHRSAOO = PHRSA ORDOUT

JP1 = PHRSAOO + ...

JP2 = PHRSAOO + ...

JP3 = PHRSAOO + ...

During a FAM write cycle, the incremented value from the L-register output signals is stored in the JP-register. Refer to paragraph 4-45 for operation of the L-register.

JP0 = JPXL LE0 + ...

JPXL = RWRITE-2 TRS270 NTRS000

JP1 = JPXL LE1 + ...

JP2 = JPXL LE2 + ...

JP3 = JPXL NL03 + ...

An address stored in the JP-register during a FAM write cycle is retained while signal JPX0 is true.

JP0 = JP0 JPX0 + ...

JPX0 = N(RWRITE-2 TR180)

RWRITE-2 = N(SREAD WCHW) (SWRITE TRS030 + RWRITE-2 NTRS000)

JP1 = JP1 JPX0 + ...

JP2 = JP2 JPX0 + ...

JP3 = JP3 JPX0 + ...

Signal JPX0 goes false during a FAM write cycle just before the new address is transferred from the L-register. Consequently, the contents of the JP-register are 0000 before a new address is stored.

4-44 KP-Register

The K-pointer register (KP-register), which consists of buffered latches KP0 through KP3, stores the address of the next FAM location to be selected for reading data into the K-register (or I-register). During a FAM read cycle, the address stored in the KP-register is placed in the L-register for addressing a location in the FAM module, and a new address is accepted from outputs of the L-register. (See figure 4-15.)

During phase RSA of an order out service cycle, the address 1111 is stored in the KP-register. Therefore, the first FAM location addressed for writing is always location 1111.

KP0 = PHRSAOO + ...

PHRSAOO = PHRSA ORDOUT

KP1 = PHRSAOO + ...

KP2 = PHRSAOO + ...

KP3 = PHRSAOO + ...

During a FAM read cycle, the incremented value from the L-register output signals are stored in the KP-register. Refer to paragraph 4-45 for operation of the L-register.

KP0 = KPXL LE0 + ...

KPXL = RREAD-2 TRS270 NTRS000

KP1 = KPXL LE1 + ...

KP2 = KPXL LE2 + ...

KP3 = KPXL NL03 + ...

An address stored in the KP-register during a FAM read cycle is retained while signal KPX0 is true.

KP0 = KP0 KPX0 + ...

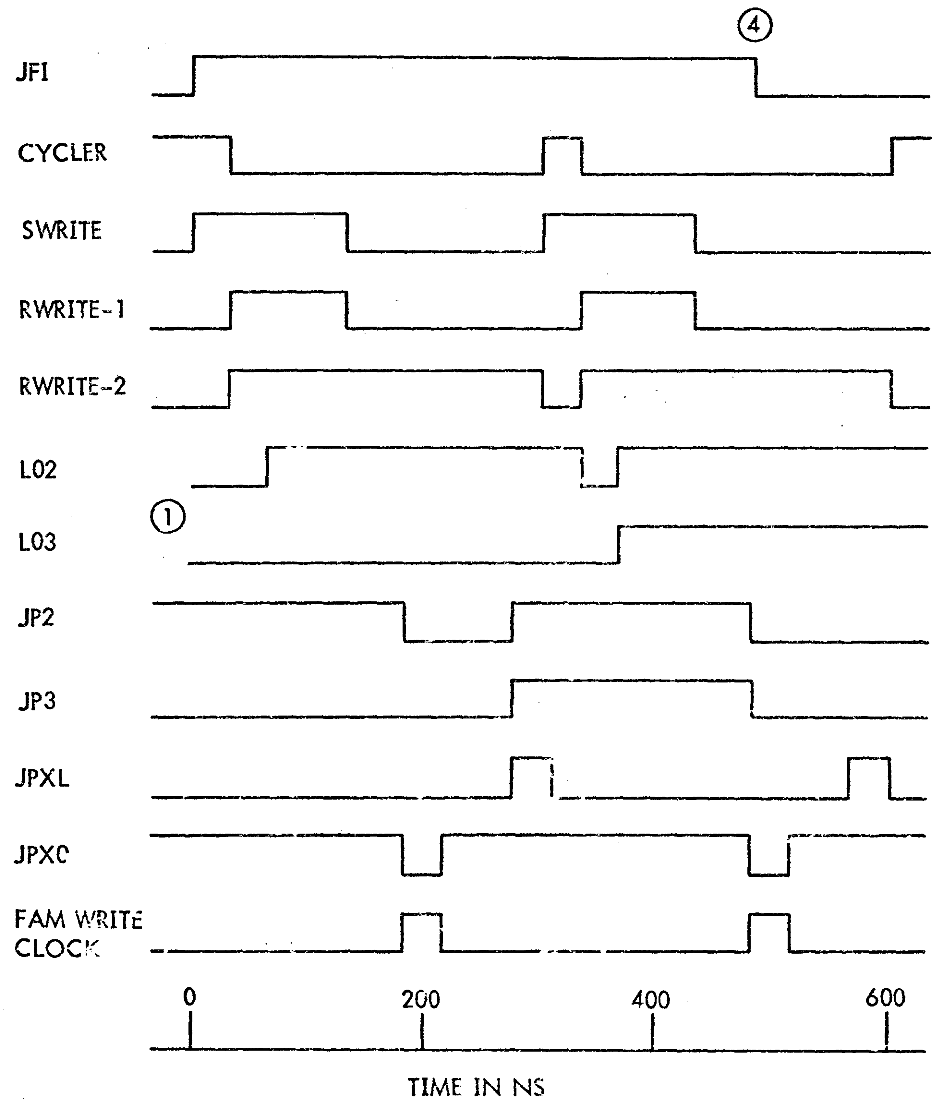
KPX0 = N(RREAD-2 TRS180)

RREAD-2 = N(READ SWRITE) (SREAD TRS030 + RREAD-2 NTRS000)

KP1 = KP1 KPX0 + ...

KP2 = KP2 KPX0 + ...

KP3 = KP3 KPX0 + ...

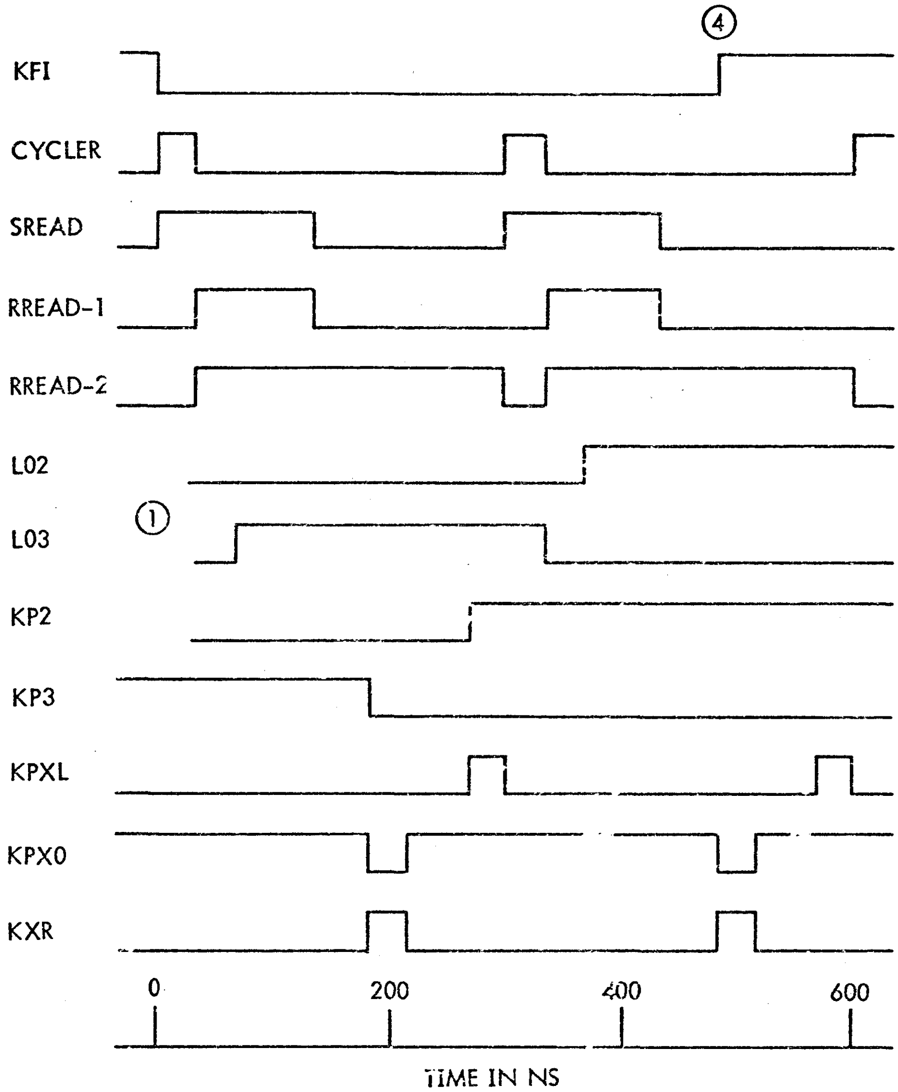


NOTES:

1. CONTENTS OF L02 AND L03 CLEARED BY NTRS030
2. RK-COUNTER INCREMENTED BY TPS130
3. DATA TRANSFERRED FROM J-REGISTER TO ADDRESSED LOCATION IN FAM MODULE BY FAM WRITE CLOCK
4. JFI LATCHED UNTIL JFIRESET TRUE

901641A.304

Figure 4-14. Sequence of FAM Write Cycles, Timing Diagram



NOTES:

1. CONTENTS OF L02 AND L03 CLEARED BY NTRS030
2. RK-COUNTER INCREMENTED BY TRS130
3. DATA TRANSFERRED FROM ADDRESSED LOCATION IN FAM MODULE TO K-REGISTER (OR I-REGISTER) BY KXR
4. KFI FALSE UNTIL KFISET TRUE, GENERATING KFIX1

901641A. 305

Figure 4-15. Sequence of FAM Read Cycles, Timing Diagram

Signal KPX0 goes false during a FAM read cycle just before the new address is transferred from the L-register, so that the contents of the KP-register are 0000 before a new address is stored.

4-45 L-Register

The L-register consists of buffered latches L00 through L03 and buffered latch NL03 which stores the bit complementary to the bit stored in L03. The L-register provides a four-bit address input to the FAM module during either a FAM read cycle or a FAM write cycle. Outputs of the L-register provide inputs to the KP-register or to the JP-register and store an incremented address in these registers, as summarized in table 4-4. Refer to paragraph 4-43 for operation of the JP-register and to paragraph 4-44 for operation of the KP-register.

During a FAM write cycle, the contents of the JP-register are stored in the L-register while signal RWRITE-1 is true. Signal RWRITE-1 is latched until a data byte is stored in the addressed FAM location, and an incremented address is stored in the JP-register. (See figure 4-13.)

L00 = JP0 RWRITE-1 + ...

RWRITE-1 = N(READ WCHW) (SWRITE TRS030 + RWRITE-1 NTRS000) NTRS130

L01 = JP1 RWRITE-1 + ...

L02 = JP2 RWRITE-1 + ...

L03 = JP3 RWRITE-1 + ...

NL03 = NJP3 RWRITE-1 + ...

During a FAM read cycle, the contents of the KP-register are stored in the L-register while signal RREAD-1 is true.

Table 4-4. Relation Between State and Output of the L-Register

STATE				SIGNALS					OUTPUT TO JP-REGISTER OR KP-REGISTER
L00	L01	L02	L03	LE0	LE1	LE2	L23	L123	
0	0	0	0	0	0	0	0	0	0 0 0 1
0	0	0	1	0	0	1	0	0	0 0 1 0
0	0	1	0	0	0	1	0	0	0 0 1 1
0	0	1	1	0	1	0	1	0	0 1 0 0
0	1	0	0	0	1	0	0	0	0 1 0 1
0	1	0	1	0	1	1	0	0	0 1 1 0
0	1	1	0	0	1	1	0	0	0 1 1 1
0	1	1	1	1	0	0	1	1	1 0 0 0
1	0	0	0	1	0	0	0	0	1 0 0 1
1	0	0	1	1	0	1	0	0	1 0 1 0
1	0	1	0	1	0	1	0	0	1 0 1 1
1	0	1	1	1	1	0	1	0	1 1 0 0
1	1	0	0	1	1	0	0	0	1 1 0 1
1	1	0	1	1	1	1	0	0	1 1 1 0
1	1	1	0	1	1	1	0	0	1 1 1 1
1	1	1	1	0	0	0	1	1	0 0 0 0

Signal RREAD-1 is latched until a data byte is read from the addressed FAM location and an incremented address is stored in the KP-register. (See figure 4-14.)

L00 = KP0 RREAD-1 + ...

RREAD-1 = N(READ SWRITE)(SREAD TRS030 + RREAD-2 NTRS000) NTRS130

L01 = KP1 RREAD-1 + ...

L02 = KP2 RREAD-1 + ...

L03 = KP3 RREAD-1 + ...

NL03 = NKP3 RREAD-1 + ...

The incremented value of the input to the L-register is generated by a set of exclusive OR gates for the most significant bits of the address.

LEC = (L00 + L123) N(L00 L123)

L123 = L01 L23

L23 = L02 L03

LE1 = (L01 + L23) N(L01 L23)

LE2 = (L02 + L03) N(L02 L03)

During a FAM write cycle, the incremented address is placed in the JP-register; during a FAM read cycle, the incremented address is placed in the KP-register.

The L-register is cleared 30 ns after starting the TRL delay line, so the address from the KP-register or JP-register can be read at address outputs L00 through L03 and NL03.

L00 = L00 NTRS030 + ...

L01 = L01 NTRS030 + ...

L02 = L02 NTRS030 + ...

L03 = L03 NTRS030 + ...

NL03 = NL03 NTRS030 + ...

After the L-register is cleared by signal NTRS030 and is loaded as previously described, signal NTRS030 acts as a latch control until a new value is loaded.

4-46 Operation of FAM Circuits During the Write Sequence

While the controller is executing a write order or a check-write order, data is transferred from the I-register to the D-register through the FAM circuits. (See figure 4-11.) Data accepted from the IOP passes through the I-register, the J-register, the FAM module, the K-register, and the D-register to the addressed selection unit. For a write sequence, data transfers from the FAM module to the K-register have priority over data transfers from the J-register to the FAM module. This priority assures that the D-register will have data for transfer to the selection unit.

Data transfer from the IOP is controlled by the phase control circuit as described in paragraph 4-20. Data from the IOP is requested during phase RSA. As the IOP responds, the TCL delay line is started, IOP data is stored in the I-register, and phase RS is entered.

DCL = CYCLE/C PHRSA RSAU + ...

IXD = PHRSADO TCS000-3

New data cannot be requested until phase RSA is entered from phase RS. This change of phase cannot occur until all previously accepted data has been transferred to the FAM module and the J-register is empty (JFI false).

DCL = CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART2 = WCHW PHRS NJFI + ...

The J-register is cleared after its contents have been transferred to the FAM module.

NJX0 = PHRSDO TCS000-1

Data transfers from the FAM circuits to the selection unit are controlled by the selection unit interface circuits as described in paragraph 4-53. Data transfers from the FAM module to the K-register are controlled by the TRL delay line. Data transfers from the K-register to the D-register take place at eight-bit intervals until the postamble is written (POST true).

DXK = WRITE NPOST BIT7RWE + ...

The function of the FAM circuits is to process data transfers between the IOP and the addressed selection unit, providing data to the selection unit at the required rate for an IOP-to-controller interface of one byte, two bytes, or four bytes.

4-47 ONE-BYTE INTERFACE. For a one-byte interface with the IOP, signal BYT1ID is true, the byte counter is not used, and the data path from the IOP is through the most significant byte of the I-register (I00-I07) to the J-register, then to the addressed location in the FAM module. (See figure 4-11.)

When IOP data is first stored in the I-register, signal JFI is false. Therefore, the data is transferred to the J-register as the TCL delay line is started during phase RS, and JFI is raised and latched at the true level.

JXI1B = IOP BYT1ID PHRSDO TCS000-2

JFI = N(JFIRESET RWRITE-2 TRS180)(JFIX1 + JFI NPHRSAOO + ...)

JFIX1 = PHRSDO TCS000-2

The controller can accept data from the IOP but cannot start the TCL delay line during phase RS until JFI is false.

The TRL delay line is started by JFI through signal SWRITE.

SWRITE = (CYCLER JFI NTRS000 + ...) NTRS130 RK0

During the FAM write cycle that is started by this signal, the following events take place:

a. The L-register is cleared.

b. The contents of the JP-register are read through outputs of the L-register to the FAM module.

c. The contents of the J-register are transferred in parallel to the FAM module location addressed by the L-register outputs.

d. The decremented value of the contents of the JP-register is read from the L-register outputs into the JP-register.

e. The RK-counter is decremented.

These events are controlled by the following equations:

L00 = L00 NTRS030 + ...

JPX0 = N(RWRITE-2 TRS180)

(FAM write clock) = RWRITE-2 TRS180

JPXL = RWRITE-2 TRS270 NTRS000

RKCK = N(TRS130 + ...)

RWRITE-N4 = RWRITE-2 NRK4

Signal JFI goes false as the contents of the J-register are stored in the FAM module, and a transfer from phase RS to phase RSA is enabled.

JFI = N(JFIRESET RWRITE-2 TRS180) (JFI NPHRSAOO + ...)

Data may be accepted from the IOP until the FAM module is filled. FAM read cycles transfer data from the FAM module to the K-register after the preamble has been written, enabling the TRL delay line to be started by an SREAD signal.

SREAD = (CYCLER NTRS000 NKFI SREADEN + ...) NTRS130 NREMPTY

SREADEN = NPOST NRWE NRWP NWPRE

When data is first stored in the FAM module, signal KFI is false. Therefore, the data is transferred to the K-register as soon as the preamble has been written because FAM read cycles have priority over FAM write cycles.

KFI = KX0 (KFIX1 + KFI NPHRSAOO)

KFIX1 = KFISET RREAD-2 TRS180

During the FAM read cycle that is started by this signal, the following events take place:

a. The L-register is cleared.

b. The contents of the KP-register are read through outputs of the L-register to the FAM module.

c. The contents of the FAM module location addressed by the L-register outputs are transferred to the K-register (or the I-register).

d. The incremented value of the contents of the KP-register is read from the L-register outputs into the KP-register.

e. The RK-counter is incremented.

These events are controlled by the following equations:

L00 = KP0 RREAD-1 + ...

KPXL = RREAD-2 TRS270 NTRS000

KPX0 = N(RREAD-2 TRS180)

KXR = KXREN RREAD-2 TRS180

KXREN = BKZZ + ...

RKCK = N(TRS130 + ...)

RREAD-4 = RREAD-2 RK4

Signal KFI is raised and latched as the contents of the FAM module are transferred to the K-register. Signal KFI remains true until the K-register is cleared following transfer of its contents to the D-register.

NKX0 = WCHW TDT2 + ...

This sequence of acceptance of data from the IOP, transfer of data to the FAM module, and reading data from the FAM module to the selection unit continues under mutual control of phase control circuits, FAM circuits, and selection unit interface circuits. When the FAM module is filled, requests for IOP data are inhibited because flip-flops RK0 is reset, inhibiting FAM write cycles, and JFI is held true, inhibiting transfer from phase RS to phase RSA. When the FAM module is empty, FAM read cycles are inhibited because signal REMPTY is true. Any attempt to write into the FAM module when it is full or to read from the FAM module when it is empty causes a rate error, as described in paragraph 4-78.

4-48 MULTIPLE-BYTE INTERFACE. For a two- or four-byte interface with the IOP, signal NBYT1ID is true, the byte counter is used to control data transfer from the I-register to the J-register, and the data path from the IOP is to the I-register, to the most significant byte of the I-register (I00-I07), to the J-register, then to the addressed location in the FAM module. (See figure 4-11.) The rest of the paragraph emphasizes the differences between write operations for a one-byte interface and for a multiple-byte interface.

When IOP data is stored in the I-register, signal JFIX1 comes true and causes JFI to be raised and latched similar to a one-byte sequence. However, JFI remains latched until all bytes accepted from the IOP have been transferred to the J-register. Data transfer from the I-register is controlled by timing signals of the TRL delay line (instead of the TCL delay line). Data transfers take place within the I-register so that all transfers from the J-register are from the most significant latches of the I-register (I00-I07). The multiple-byte interface data path from the J-register through the FAM circuits to the D-register is identical to the one-byte interface data path.

Signal JFI remains latched at the true level following acceptance of IOP data because a false JFIRESET signal takes control from signal JFIX1. Once JFI is raised by JFIX1, JFI remains latched until JFIRESET is true during a FAM write cycle.

```
JFI          = N(JFIRESET RWRITE-2 TRS180)
               (JFIX1 + JFI NPHRSAOO
               + ...)

   JFIX1     = PHRSDO TCS000-2

   NJFIRESET = WCHW NBYT1ID BK1 (Two- and
                                 four-byte
                                 interface)
               + WCHW BYT4ID BK0 (Four-byte
                                 interface)
```

The byte counter (BK0, BK1) is direct set to state (1, 1) each time JFIX1 is true and clocked during each FAM write cycle. (See paragraph 4-33.)

```
BKX1         = NBKX1EN + ...

   NBKX1EN   = WCHW JFIX1 + ...

NBKCK        = BKCKEN TRS270 + ...

   BKCKEN    = NBYT1ID(WCHW RWRITE-1 + ...)
```

For a two-byte interface, two FAM write cycles take place before signal JFI goes false to enable a transfer to phase RSA to request additional data from the IOP. During the first FAM write cycle, data is transferred from latches (I00-I07) of the I-register to the J-register, the contents of (I08-I15) are transferred to (I00-I07), and the byte counter goes to state (1, 0) so that signal BKZW is true.

```
JXIN1B   = NBYT1ID IOP DATAOUT RWRITE-2
           TRS060

IXI-1    = IXEN RWRITEDO BKZZ

   IXEN  = NBYT1ID TRL180 NTRL240
```

During the second FAM write cycle, data is transferred from latches (I00-I07) of the I-register to the J-register as before. However, since JFIRESET is now true, JFI goes false during the FAM write cycle.

For a four-byte interface, four FAM write cycles take place before signal JFI goes false to enable a transfer to phase RSA to request additional data from the IOP. During the first FAM write cycle, data is transferred as for the two-byte interface. During the second FAM write cycle, data is transferred from latches (I00-I07) of the I-register to the J-register, the contents of (I16-I23) are transferred to (I00-I07), and the byte counter goes from state (1, 0) to state (0, 1) so that signal BKWZ is true.

```
IXI-2 = IXEN RWRITEDO BKZW
```

During the third FAM write cycle, data is transferred from latches (I00-I07) of the I-register to the J-register, the contents of (I24-I31) are transferred to (I00-I07), and the byte counter goes from state (0, 1) to state (0, 0) so that signal BKWW is true.

```
IXI-3 = IXEN RWRITEDO BKWZ
```

During the fourth FAM write cycle, data is transferred from latches (I00-I07) of the I-register to the J-register as before. However, since JFIRESET is now true, JFI goes false during the FAM write cycle. Therefore, for a multiple-byte interface, the phase control circuits cannot request additional data from the IOP until previously accepted data has been written into the FAM module. However, FAM read cycles may occur during this interval to maintain the data rate to the addressed selection unit. For a multiple-byte interface, data transfer from the FAM module to the K-register is enabled by a false READRR signal (instead of a true BKZZ signal).

```
KXR        = KXREN RREAD-2 TRS180

   KXREN   = NREADRR + BKZZ

   READRR  = READ RREAD-2
```

4-49 Operation of FAM Circuits During the Read Sequence

While the controller is executing a read order, data is transferred from the D-register to the O-register through the FAM circuits. (See figure 4-11.) Data accepted from the selection unit passes through the D-register, the J-register, the FAM module, the K-register (or the I-register), and the O-register, to the IOP. For a read sequence, data transfers from the J-register to the FAM module have priority over data transfers from the FAM module to the K-register (or to the I-register). This priority order assures that a data in the D-register will be stored in the FAM module as it comes from the selection unit.

Data transfer from the selection unit is controlled by the selection unit interface circuits as described in paragraph 4-53. Following detection of the preamble, data bytes are transferred from the D-register to the J-register at eight-bit intervals as described in paragraph 4-54.

JXD = READ NPRE TDT2

A FAM write cycle is enabled each time signal JXD comes true.

SWRITE = (CYCLER JFI NTRS000 + ...) NTRS130 NRK0

JFI = N(JFIRESET RWRITE-2 TRS180)(JXD + JFI NPHRSA00 + ...)

FAM read cycles are allowed after read/write enable flip-flop RWE is set, as described in paragraph 4-62.

SREAD = (SREADEN NKFI CYCLER NTRS000 + READ NKFI CYCLER NTRS000 + ...) NREMPTY NTRS180

SREADEN = NPOST RWE NRWP NWPRE

While the phase control circuits are in phase RSA, the IOP accepts data stored in the O-register and enables a transfer to phase RS.

DCL = CYCLE/C PHRSA RSAU + ...

Unless end data signal ED is true, new data is transferred from the K-register (or from the K-register and the I-register) into the O-register while the phase control circuits are in phase RS.

OXK = OXKEN TCS000-2

OXKEN = PHRS DATAIN NED

However, the TCL delay line cannot be started to permit this data until additional data has been stored in the K-register (or K-register and I-register) as indicated by a true KFID signal.

DCL = CYCLE/C DCLSTART2 NRSAU + ...

DCLSTART2 = PHRS READ KFID + ...

The function of the FAM circuits during a read sequence is to control data transfers from the FAM module to the K-register (or K-register and I-register) so that data may be stored in the O-register for transfer to the IOP on a one-, two-, or four-byte interface.

4-50 ONE-BYTE INTERFACE. For a one-byte interface with the IOP, signal BYT1ID is true, the byte counter is not used, and the data path from the addressed location in the FAM module is first to the K-register then to the most significant latches of the O-register (O00-O07). (See figure 4-11.)

Each time selection unit data is transferred from the D-register to the J-register, signal JFI is raised and latched. The TRL delay line is started, and since a FAM write cycle has priority over a FAM read cycle, a FAM write cycle takes place.

During the FAM write cycle that is started by this signal, the following events take place:

a. The L-register is cleared.

b. The contents of the JP-register are read through outputs of the L-register to the FAM module.

c. The contents of the J-register are transferred in parallel to the FAM module location addressed by the L-register outputs.

d. The decremented value of the contents of the JP-register is read from the L-register outputs into the JP-register.

e. The RK-counter is decremented.

These events are controlled by the following equations:

L00 = L00 NTRS030 + ...

JPX0 = N(RWRITE-2 TRS180)

(FAM write clock) = RWRITE-2 TRS180

JPXL = RWRITE-2 TRS270 NTRS000

RKCK = N(TRS130 + ...)

RWRITE-N4 = RWRITE-2 NRK4

Signal JFI goes false as the contents of the J-register are stored in the FAM module. When data is first stored in the FAM module, signal KFI is false. Therefore, the data can be transferred to the K-register any time after a false REMPTY signal indicates that data is available, provided that no FAM write cycle takes priority.

SREAD = (CYCLER NTRS000 NFKI READ + ...) NTRS130 NREMPTY

KFI = KX0 (KFIX1 + KFI NPHRSAOO)

KFIX1 = KFISET RREAD-2 TRS180

During the FAM read cycle that is started by this signal, the following events take place:

a. The L-register is cleared.

b. The contents of the KP-register are read through outputs of the L-register to the FAM module.

c. The contents of the FAM module location addressed by the L-register outputs are transferred to the K-register (or the I-register).

d. The incremented value of the contents of the KP-register is read from the L-register outputs into the KP-register.

e. The RK-counter is incremented.

These events are controlled by the following equations:

L00 = L00 NTRS030 + ...

L00 = KP0 RREAD-1 + ...

KPXL = RREAD-2 TRS270 NTRS000

KPX0 = N(RREAD-2 TRS180)

RKCK = N(TRS130 + ...)

RREAD-4 = RREAD-2 RK4

KXR = KXREN RREAD-2 TRS180

KXREN = BKZZ + ...

Signal KFI is raised and latched as the contents of the FAM module are transferred to the K-register and KFI remains true until the K-register is cleared following the transfer of its contents to the O-register.

NKX0 = KX0EN + ...

KX0EN = OXKEN TCS100-3

OXKEN = PHRS DATAIN NED

This sequence of accepting data from the addressed selection unit, transferring data to the FAM module, and reading data from the FAM module into the O-register for transfer to the IOP continues under mutual control of phase control circuits, FAM circuits, and selection unit interface circuits. Data transfer to the IOP must continue at a high enough rate so that there is always space in the FAM module for new data which is accepted at a constant rate. Request strobes for the IOP cannot be generated unless there is data available for transfer. Any attempt to write into a full FAM module or to read from the FAM module when it has insufficient data causes a rate error as described in paragraph 4-78.

4-51 MULTIPLE-BYTE INTERFACE. For a two- or four-byte interface with the IOP, signal NBYT1ID is true, the byte counter is used to control data transfer from the addressed location in the FAM module to the K-register and I-register, and the data path from the FAM module to the O-register is through the K-register and lower-order latches of the I-register. (See figure 4-11.) This paragraph emphasizes the differences between a read sequence for a one-byte interface and for a multiple-byte interface.

When selection unit data is stored in the J-register, signal JXD comes true and causes JFI to be raised and latched as for a one-byte sequence. Data transfers from the J-register to the FAM module take place under control of signal JXD. FAM write cycles and FAM read cycles cause the same sequence of events as for a one-byte interface. However, signal KFID cannot come true until sufficient data bytes have been stored in the K-register and I-register.

The byte counter (BK0, BK1) is direct set to state (1, 1) by signal BKX1 each time signal KX0EN is true. At this time, data is transferred to the O-register from the K-register and I-register, both of which are then cleared. Refer to paragraphs 4-33, 4-37, 4-38, and 4-57 for details.

NKX0 = KX0EN + ...

BKX1 = NBKX1EN + ...

NBKX1EN = READ KX0EN + ...

Once signal SREADEN is true, FAM read cycles, controlled primarily by signal KFI, may take place whenever the FAM module contains data bytes. Signals RREAD-1 and RREAD-2, which control the priority of FAM read cycles over FAM write cycles, become true during a FAM read cycle. Data transfers occur as described for a one-byte interface. As the byte counter is clocked, it passes from state (1, 1) to (1, 0) to (0, 1) to (0, 0), as required.

NBKCK = BKCKEN TRS270 + ...

PKCKEN = NBYT1ID (READRR RREAD-1 + ...)

READRR = READ RREAD-2

For a two-byte interface, two FAM read cycles must take place before signal KFID goes true. When true, KFID enables a transfer to phase RSA and enables a request for the IOP to accept data that has been stored in the O-register. During the first FAM read cycle, data is transferred from the addressed location in the FAM module to the K-register, and the byte counter goes to state (1, 0) so that signal BKZW becomes true.

KXR = KXREN RREAD-2 TRS180

KXREN = BKZZ + ...

Signal KFI does not latch true because signal KFIX1 is held false by a false KFISET signal.

KFI = KX0 (KFIX1 + KFI NPHRSAOO)

KFIX1 = KFISET RREAD-2 TRS180

NKFISET = READRR NBYT1ID BK1
+ READRR BYT4ID BK0

During the second FAM read cycle, data is transferred from the addressed location in the FAM module to the I-register latches I07 through I15, and the byte counter goes to state (0, 1).

IXR-1 = IXEN READRR BKZW

IXEN = NBYT1ID TRL180 NTRL240

Signal KFI latches during the second FAM read cycle because KFISET is true. (BK1 is false, and BYT4ID is false.) Because KFI latches, KFID goes true and is latched until the data transfer is made to the O-register.

KFID = KX0(KFID + KFIDX1)

KFIDX1 = KFI TRS270

When the data transfer is made, the byte counter is set to state (1, 1).

For a four-byte interface, four FAM read cycles must take place before signal KFID goes true. The first two FAM read cycles are controlled as for a two-byte interface. However, after the second FAM read cycle, KFISET remains false since the byte counter is in state (1, 0) and BYT4ID is true. Therefore, KFI does not latch true, and a byte is read from the FAM module into I-register latches I16 through I23.

IXR-2 = IXEN READRR BKWZ

During the third FAM read cycle, the byte counter goes to state (0, 0). Therefore, during the fourth FAM read cycle, a byte is read into I-register latches I24 through I31.

IXR-3 = IXEN READRR BKWW

During this FAM read cycle, KFISET is true, KFI latches, and KFID is latched until the data transfer to the O-register is made. When the data transfer is made, the byte counter is set to state (1, 1).

4-52 Operation of the TRL Delay Line for a Seek Order

During execution of a seek order, the contents of the I-register must be transferred to the J-register, and the contents of the J-register must be transferred to the T-register or S-register in two successive data out service cycles.

Data transfer from the IOP is controlled by the phase control circuits as described in paragraph 4-20. Data from the IOP is requested during phase RSA. As the IOP responds, the TCL delay line is started, IOP data is stored in the I-register, the byte counter goes from state (1, 1) to state (1, 0), and phase RS is entered.

DCL = CYCLE/C PHRSA RSAU + ...

NBKCK = PHRSA SEKSEND TCS000-3

IXD = PHRSADO TCS000-3

New data is accepted after phase RSA is entered from phase RS. This change of phase is enabled immediately after phase RS is entered, if the request strobe acknowledge signal is false.

DCL = CYCLE/C DCLSTART2 NRSAU
+ ...

DCLSTART2 = PHRS SEKSEND + ...

SEKSEND = SEEK NPHRSAOO + ...

Data transfers from the I-register to the J-register must take place before new data is accepted from the IOP. The data transfer is enabled by the TCL delay line.

JXI1B = IOP PHRSADO TCS000-2 BYT1ID

Signal BYT1ID is true even if the controller is operating with a two-byte or four-byte IOP interface. As indicated in figure 4-21, byte width signals are true only during execution of read orders, write orders, or checkwrite orders for which signal WRCH is true.

For any IOP interface width, data transfers from the J-register to the T-register or to the S-register are enabled by the TRL delay line and are controlled by byte counter signals. The byte counter is clocked during phase RSA. (See paragraph 4-33.)

NBKCK = PHRSA SEKSEND TCS000-3

Therefore, when phase RS is first entered, signal BKWZ is true, and data is transferred from the J-register to the T-register after the TRL delay line is started.

TXJ = SEEK RWRITEDO BKZW TRS130

RWRITEDO = DATAOUT RWRITE-2

While the controller is in phase RSA a second time, the byte counter is clocked again, causing signal BKWZ to be true. After the second byte is accepted and stored in the J-register, bits 0 through 3 are transferred to the T-register and bits 4 through 7 are transferred to the S-register. (See paragraphs 4-25, 4-39, and 4-68 for details.)

TXJ = SEEK RWRITEDO BKWZ TRS130

SXJ = SEEK RWRITEDO BKWZ TRS130

4-53 SELECTION UNIT INTERFACE CIRCUITS

The selection unit interface circuits control exchange of signals between the controller and the selection units. When the controller is executing an order, an 11-bit track address is sent to the addressed selection unit during intersector gap time. (Two bits of the 11-bit address should always be zeros.) Angular position signals from the selection unit identify the sector under the read/write heads. When the angular position signals match the sector address register signals, data transfer can begin. Data is written on the addressed track for a valid write order; data is read from the addressed track for a valid read order or checkwrite order.

During execution of a write order, bits are written on the track by the Manchester encoding method, using the clock signals of a 3-MHz oscillator in the controller. A counter controls the shifting of the track address and the writing of the five-byte preamble, the 1024 data bytes, the two-byte checksum, and the single byte of zeros. The five-byte preamble is generated at inputs to the K-register. The data bytes are accepted from the FAM circuits into the K-register. Data from the K-register is transferred to the D-register in parallel and is shifted in series from the D-register to the selection unit. After all data bytes have been written, zeros are stored in the K-register (if necessary) to complete 1024 data bytes per sector, then the two-byte checksum is transferred from the P-register to the K-register. After the checksum is written, a byte of zeros is written before the read/write heads are disabled.

During execution of a read order, clocking is initially controlled by the oscillator in the controller. During this initial period, the addressed selection unit develops a clock signal from the Manchester-encoded data. After an interval established by logic circuits, clock control is transferred to a data strobe clock signal developed in the addressed selection unit. When the preamble synchronization pattern is detected, the data is accepted serially in eight-bit bytes into the D-register and is transferred in parallel to the J-register. From the J-register, the data passes to the FAM circuits. After the 1024 data bytes have been read, the two-byte checksum read from the addressed selection unit is compared with a checksum developed during execution of the read order. After the checksum comparison is made, no additional data is accepted from the addressed selection unit.

During execution of a checkwrite order, clocking is initially controlled by the oscillator in the controller, then by the data strobe clock. The preamble synchronization pattern indicates the start of data, as for a read order. Data from the IOP is moved as far as the D-register. As IOP data is shifted serially from the D-register, the data is compared with data accepted from the addressed selection unit. This comparison is made for 1024 data bytes and for the two-byte checksum developed by controller logic. Thus, the checkwrite order involves operations similar to those for execution of a write order (but does not include writing data) and includes operations similar to those for execution of a read order (but does not include transferring data to the IOP).

4-54 TDL Delay Line

The TDL delay line, which includes control flip-flop TDT and associated logic elements, generates timing signals to enable data transfer in the selection unit interface circuits. (See figure 4-16.)

Whenever flip-flop TDT is set, the TDL delay line is started. After 40 ns, TDT is direct reset. After 60 ns, the input to the delay line is inhibited, so a new cycle cannot be started until the previous pulse has passed.

TDL000 = TDTSET NTDL060

E/TDT = TDL040

The delay line provides pulses of nominal 40-ns duration at intervals of 20, 40, 60, 80, and 100 ns. Signal TDT1 is equivalent to TDL020; signal TDT2 is equivalent to TDL080.

Flip-flop TDT, which is clocked by read/write clock signal RWCK, is set whenever TDTSET is true and is reset whenever TDTSET is false.

S/TDT = TDTSET

R/TDT = ...

C/TDT = RWCK

Signal TDTSET is controlled by signals generated by the B-counter and by the selection unit interface logic. During execution of a write order, signal TDTSET comes true at eight-bit intervals to enable the transfer from the K-register to the D-register of the five-byte preamble, the 1024 data bytes, and the two-byte postamble.

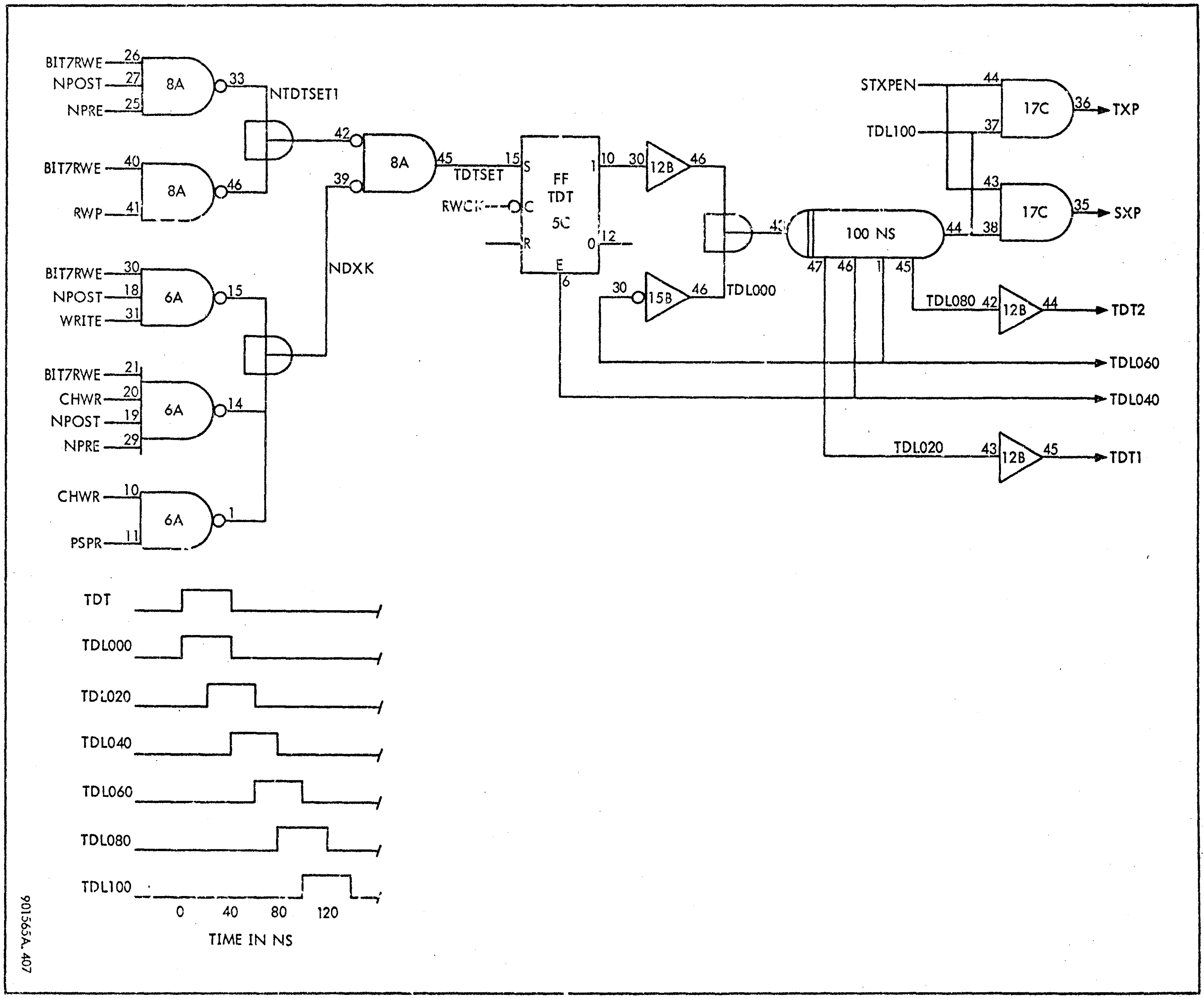


Figure 4-16. TDL Delay Line, Logic and Timing Diagram

TDTSET = DXK + ...

DXK = WRITE NPOST BIT7RWE + ...

BIT7RWE = B10 B11 B12 RWE

During execution of a read order, no transfer of data from the K-register to the D-register takes place, and the preamble synchronization pattern is used to identify the start of the data bytes. Once the data bytes are available, the TDL delay line is started at eight-bit intervals to enable a transfer of data from the D-register to the J-register.

TDTSET = TDTSET1 + ...

TDTSET1 = BIT7RWE NPOST NPRE + ...

JXD = NPRE READ TDT2

During execution of a checkwrite order, transfer of data from the K-register to the D-register takes place, and the preamble synchronization pattern is used to identify the start of the data bytes. When the preamble synchronization pattern is recognized (PSPR true), the next bit received from the selection unit will be the first data bit. Therefore, the TDL delay line is started to enable the first data byte received from the IOP (and in the K-register) to be transferred to the D-register and compared bit by bit with the first data byte received from the selection unit.

TDTSET = DXK + ...

DXK = CHWR PSPR + ...

PSPR = NDAR ND00 D01 D02 PSPBREND

PSPBREND = PSPB REND

PSPB = B07 B08 PRE RWE

REND = RWE RCHW

Subsequent data bytes from the IOP are transferred from the K-register to the D-register at eight-bit intervals.

TDTSET = DXK + ...

DXK = CHWR NPOST NPRE BIT7RWE + ...

Data bytes are received until postamble time (POST false).

For either read orders, write orders, or checkwrite orders, the TDL delay line is started at eight-bit intervals while flip-flops RWP and RWE are in the set state.

TDTSET = TDTSET1 + ...

TDTSET1 = RWP BIT7RWE + ...

4-55 Interface Clocking

The clock signals controlling the selection unit interface circuits are controlled by an internal 3-MHz oscillator having an output signal designated CLK3MH, flip-flops DSE and CLK, and control signals EXT and DSR. The read/write clock signal, which is designated RWCK, is generated by four identical circuits.

(RWCK-1 - RWCK-4) = RWCK

RWCK	= CLK3MH NEXT CLK	(1.5 MHz write clock, not extended performance)
	+ CLK3MH EXT NDSE	(3.0 MHz write clock, extended performance)
	+ DSE DSR	(Read clock)

During execution of any order, the read/write clock is generated by the internal clock at the start of a sector. During this period, the controller is either writing the preamble or counting locally generated clocks in a search for the preamble synchronization pattern.

RWCK = CLK3MH EXT NDSE + ...

For a write order, this equation generates the read/write clock throughout the sector. For a read order, the read/write clock is controlled by the selection unit data strobe after DSE is set, as described in paragraph 4-59.

RWCK = DSE DSR + ...

DSR = /DS/

When signal EXT is false (as described in paragraph 4-82), the read/write clock frequency is reduced by a factor of two, using flip-flop CLK as a frequency divider.

RWCK = CLK3MH NEXT CLK + ...

S/CLK = NCLK NDSE

R/CLK = ...

C/CLK = CLK3MH

When control of the read/write clock is transferred to the data strobe, the reduced frequency clock is read from the signal as for an EP RAD selection unit.

4-56 B-Counter

The bit and byte counter (B-counter) consists of flip-flops B00 through B12 and associated logic elements. These flip-flops, which have no reset inputs, are set by a clock signal if the set input is true and are reset by a clock signal if the set input is false. All logic equations for the B-counter are written with the following simplifications:

(RWCK-1 - RWCK-4)	=	RWCK
PRE-1	=	PRE
BX0-1	=	BX0
NBX0-1	=	NBX0
(△073)	=	B05
(△075)	=	B03 B04 B05
(△077)	=	B12
(△079)	=	B10 B11 B12

The functions of the B-counter are:

a. To count bits transmitted to the addressed selection unit or received from the addressed selection unit, in serial order

b. To control data transfers within the controller so that eight-bit bytes are transferred between registers

c. To control writing of the five-byte preamble during execution of a write order

d. To enable search for the four-bit preamble synchronization pattern during execution of a read order or checkwrite order

e. To identify the postamble during execution of a read order, write order, or checkwrite order

Bits are counted by flip-flops B10, B11, and B12; bytes are counted by flip-flops B00 through B09. The description of the B-counter operation is related to the sequences described in paragraph 4-59.

At the beginning of each intersector gap, flip-flop PRE, RWP, and BCE are in the reset state, and signals BX0 and SECP are false. Read/write clock signal RWCK is generated from a source internal to the controller. When a sector pulse or index pulse is detected, a true SECP signal clears flip-flops B00 through B05.

(E/B00-E/B05)	=	SECP
SECP	=	SPR + IPR
SPR	=	/SP/
IPR	=	/IP/

The next read/write clock sets TSE and generates a true BX0 signal that resets flip-flops B06 through B12 because set inputs to each of these flip-flops are false.

(C/B06-C/B11)	=	BX0 RWCK + ...
BX0	=	PXS + ...
PXS	=	NRWP TSE
C/B12	=	RWCK + ...
S/B06	=	NB06 NBX0 + ...
.		.
.		.
.		.
S/B12	=	NB12 NBX0 + ...

During execution of a write order, flip-flops B06 through B12 count subsequent read/write clocks in binary sequence from 0 000 000 to 1 110 111 (decimal 119). Flip-flop PRE is set when the B-counter is in state 1 001 000 (decimal 72). Flip-flop RWE is set when the B-counter is in state 1 001 100 (decimal 76), provided the sector compare signal is true and no errors are detected. Flip-flop RWP is reset when the B-counter is in state 1 010 000 (decimal 80). Flip-flop BCE is set when the B-counter is in state 1 110 000 (decimal 112). When the B-counter reaches a count of 1 110 111 (decimal 119), signal BX0 is true, resetting flip-flops B06 through B12 as before and causing PRE to be reset.

BX0	=	PSP WRITE BIT7RWE + ...
PSPB	=	B07 B08 PRE RWE
BIT7RWE	=	B10 B11 B12 RWE
R/PRE	=	BX0
C/PRE	=	RWCK

Flip-flop BCE is reset one clock time later when PSPB is false.

S/BCE	=	PSPB
R/BCE	=	...
C/BCE	=	RWCK

While PRE is set and BCE is reset, signal WPRE causes the five-byte preamble to be stored in the K-register for transfer to the D-register. At counts 79, 87, 95, and 103, the pattern 0101 0101 is stored in the K-register. At count 111, the pattern 0011 0101 is stored in the K-register. (See paragraph 4-57.)

KXPRE = WPRE BIT7RWE (Counts 79, 87, 95, 103, 111)

WPRE = PRE WRITE NBCE (Counts 73 through 112)

PSPWEN = B07 B09 (Counts 104 through 111)

As BCE is reset, the B-counter is placed in state 0 000 000 001 000 and begins a binary count to state 1 111 111 111 111.

S/B00 = NB00 NPRE + ...

.　　.
.　　.
.　　.

S/B06 = NB06 NPRE + ...

C/B00 = B05CK B05 B04 B03 B02 B01 + ...

B05CK = B06 NBCE

C/B01 = B05CK B05 B04 B03 B02 + ...

C/B02 = B05CK B05 B04 B03 + ...

C/B03 = B05CK B05 B04 + ...

C/B04 = B05CK B05 + ...

C/B05 = B05CK

C/B06 = RWCK B12 B11 B10 B09 B08 B07+...

S/B07 = NB07 NBX0 + ...

S/B08 = NB08 NBX0 + ...

S/B09 = B09X1 NBX0 + ...

B09X1 = WCHW RWE

S/B10 = NB10 NBX0 + ...

S/B11 = NB11 NBX0 + ...

S/B12 = NB12 NBX0 + ...

C/B07 = RWCK B12 B11 B10 B09 B08 + ...

C/B08 = RWCK B12 B11 B10 B09 + ...

C/B09 = RWCK B12 B11 B10 + ...

C/B10 = RWCK B12 B11 + ...

C/B11 = RWCK B12 + ...

C/B12 = RWCK

When the B-counter reaches its maximum count, it is cleared by the next clock signal and POST is set.

S/POST = NPOST NPRE

C/POST = B00 B01 B02 B03 B04 B05 B05CK + ...

The B-counter then counts 32 bits (count 0 000 000 011 111) and causes RWE to be reset, disabling the read/write heads.

R/RWE = RWERST

RWERST = POSTB89 BIT7RWE

POSTB89 = POST B08 B09

BIT7RWE = B10 B11 B12 RWE

C/RWE = RWCK

The B-counter is cleared at the start of the new sector, as described above. During execution of a read order, the B-counter is cleared by a sector pulse or index pulse and counts in binary sequence. At a count of 76, RWP is reset and DSE is direct set to transfer clock control to the data strobe of the addressed selection unit.

R/RWP = RWPRST

RWPRST = B06 B08 + ...

M/DSE = DSEM

DSEM = NRWP REND

REND = RWE RCHW

Preamble flip-flop PRE may be reset during any of the 16 clock times from count 112 to count 127 if the preamble synchronization pattern is recognized (PSPR true).

R/PRE = BX0

BX0 = PSPR + ...

PSPR = NDAR ND00 D01 D02 PSPBREND

PSPBREND = PSPB REND

PSPB = B07 B08 PRE RWE

C/PRE = RWCK

When PSPB is true, BCE is set. While PSPB is true, BCE remains in the set state; after PRE is reset, BCE remains in the set state for one clock time and clears the B-counter, as for the write order.

During execution of a read order, the B-counter is preset to 0 000 000 000 000 (instead of 0 000 000 001 000, as for a write order). The B-counter then advances to state 1 111 111 111 111, is cleared, and counts to 0 000 000 011 111, similar to a write order.

During execution of a checkwrite order, the B-counter operates as it does for a read order, first transferring clock control to the addressed selection unit, then searching for the preamble synchronization pattern, counting data bytes, and counting preamble bits.

4-57 K-Register

The K-register, which consists of buffered latches K00 through K07, stores data during execution of read orders, write orders, or checkwrite orders. Data stored in the K-register while signal KX0 is true is retained until KX0 is false.

K00 = K00 KX0 + ...

. .
. .
. .

K07 = K07 KX0 + ...

The K-register is cleared during phase RSA of an order out service cycle when a sense order is executed, when data is transferred from the K-register to the O-register, and after the TDT delay line is started during execution of a write order or checkwrite order.

NKX0 = PHRSAOO + SENSE + KX0EN + WCHW TDT2

KX0EN = OXKEN 1CS100-3

During execution of a sense order, two bytes of data are transferred through the K-register latches to the O-register under control of the byte counter. For byte 2 of a sense order (BKZW true), four bits of the track address are accepted from the T-register, and the four-bit sector address is accepted from the S-register.

K00 = T07 KXSENSE1 + ...		Part of track address
KXSENSE1 = SENSE BKZW		
K01 = T08 KXSENSE1 + ...		
K02 = T09 KXSENSE1 + ...		
K03 = T10 KXSENSE1 + ...		
K04 = S00 KXSENSE1 + ...		Sector Address
K05 = S01 KXSENSE1 + ...		
K06 = S02 KXSENSE1 + ...		
K07 = S03 KXSENSE1 + ...		

For byte 3 of a sense order (BKWZ true), the address for the sector currently under the read/write heads of the disc file (angular position) passes through K04, K05, K06, and K07 of the K-register.

K04 = AN0R KXSENSE2 + ...

KXSENSE2 = SENSE BKWZ

K05 = AN1R KXSENSE2 + ...

K06 = AN2R KXSENSE2 + ...

K07 = AN3R KXSENSE2 + ...

During execution of a write order, the bytes of the preamble are stored in the K-register while signal KXPRE is true. When signal PSPWEN is false, the bit sequence (0101 0101) is stored in the K-register; when signal PSPWEN is true, the bit sequence (0011 0101) is stored in the K-register. The preamble consists of four bytes of (0101 0101) followed by the preamble synchronization pattern of (0011 0101). This pattern is noted in the order K00, K01, K02, ... K07. In all cases the signal level for K00, K04, and K06 is false, and the signal level for K03, K05, and K07 is true. Signals KXPRE and PSPWEN are controlled by the B-counter and are defined in paragraph 4-56.

K01 = KXPRE NPSPWEN + ...

K02 = KXPRE PSPWEN + ...

K03 = KXPRE + ...

K05 = KXPRE + ...

K07 = KXPRE + ...

While the controller is executing a read order, write order, or checkwrite order, data bytes are transferred from the addressed location of the FAM module to the K-register under control of the TRL delay line. (See paragraph 4-41.)

K00 = R00 KXR + ...

KXR = KXREN RREAD-2 TRS180

KXREN = BKZZ + NREADRR

K01 = R01 KXR + ...

.
.
.

K07 = R07 KXR + ...

4-58 D-Register

The D-register, which is the temporary storage register for data passing between the controller and the selection unit, consists of flip-flops D00 through D07 and associated logic elements. During execution of a write order or a checkwrite order, the D-register accepts data in parallel from the K-register and shifts the data serially to the selection unit before accepting a new byte. At the start of a write order or checkwrite order, the D-register accepts the five-byte preamble from the K-register; at the end of a write order or checkwrite order, the D-register accepts the two-byte checksum from the P-register. During execution of a read order, the D-register accepts data serially from flip-flop DAR in eight-bit bytes and transfers the byte in parallel to the J-register before the next serial bit is accepted. The preamble and the checksum are read into the D-register but are not transferred to the J-register. During execution of a checkwrite order, IOP data transferred serially from the D-register (as in a write order) is compared with selection unit data transferred serially from the flip-flop DAR (as in a read order). If a mismatch occurs, an error signal is generated. The 1024 data bytes and the two-byte checksum are compared bit by bit during a checkwrite order. During the intersector gap time, part of the D-register is used for track address incrementing.

The D-register is clocked by read/write clock signal RWCK, and reset inputs are always true.

(C/D00-C/D07) = RWCK

(R/D00-R/D07) = ...

Therefore, each time RWCK goes false, each flip-flop in the D-register is set if its set input is true and reset if its set input is false. When signal DXK is true, the contents of the K-register are transferred to the D-register.

S/D00 = K00 DXK + ...

. .
. .
. .

S/D07 = K07 DXK + ...

After read/write enable flip-flop RWE is set during execution of a write order, DXK enables data transfer. Eight bits are accepted by the D-register each time signal DXK is true. This operation is inhibited during postamble time, during which time the checksum and single byte of zeros are stored.

DXK = WRITE NPOST BIT7RWE + ...

During execution of a checkwrite order, the preamble synchronization pattern must be recognized (PSPR true) before any data transfers are made. A data byte from the IOP is in the K-register while a search for the pattern is conducted, and the byte is transferred when PSPR is true.

DXK = CHWR PSPR + ...

After this initial byte is transferred, bytes are transferred at eight-bit intervals until postamble time is reached.

DXK = CHWR BIT7RWE NPRE NPOST + ...

When signal DXP is true, the contents of P-register bits 7 through 14 (checksum bits) are transferred to the D-register.

S/D00 = DXP P07 + ...

. .
. .
. .

S/D07 = DXP P14 + ...

This transfer is made for two byte times during postamble time (POST true).

DXP = POST BIT7RWE

During the intersector gap time, flip-flop DSL is set and enables a shift in four flip-flops of the D-register.

S/D04 = D05 DSL + ... (Not used)

S/D05 = D06 DSL + ... (Not used)

S/D06 = D07 DSL + ... (Not used)

S/D07 = D07SET DSL + ... (Track address increment)

The new data shifted in from signal D07SET is used during track address increment, as described in paragraph 4-70.

During execution of a read order or checkwrite order, the contents of the D-register are shifted right, and new data is stored from flip-flop DAR. Flip-flop DAR accepts data from the selection unit.

S/DAR = DAIR REND

DAIR = /DAI/

REND = RCHW RWE

R/DAR = ...

C/DAR = RWCK

S/D00 = DXSR DAR + ...

S/D01 = DXSR D00 + ...

. .
. .
. .

S/D07 = DXSR D06 + ...

After eight bits have been stored, the byte is transferred to the J-register.

Signal DXSR is true when all other signals controlling D-register flip-flop inputs are false.

DXSR = NDSL NDXK NDXP

Therefore, signal DXSR comes true during execution of read orders or checkwrite orders to enable acceptance of data from the addressed selection unit. In each case, read/write clock signal RWCK is controlled by a local oscillator until the preamble synchronization pattern is detected. After this event, RWCK is controlled by the data strobe signal extracted from data written on the track. During execution of a checkwrite order, the serial output from D07 of the D-register is compared with the serial output from DAR for all 1024 data bytes and for the two checksum bytes.

CHWER = CHWEREN (DAR + D07)
N(DAR D07)

CHWEREN = CHWR NPOSTB89 NPRE RWE

4-59 Interface Control Circuits

The selection unit interface is controlled by flip-flops that synchronize data transfer, detect the preamble and post-amble, control interface clocking, and control incrementing and transferring the track address.

Flip-Flop	Function
BCE	B-counter enable
DSE	Data strobe enable
DSL	D-register shift left enable (used only for track and sector incrementing)
PRE	Preamble detect
POST	Postamble detect
RWE	Read/write enable
RWP	Read/write possible
TSE	Track shift enable
SECPD	Sector pulse or index pulse detect

4-60 TRACK SHIFT SEQUENCE. (See figure 4-17.) While a read order, write order, or checkwrite order is being executed, the track address is incremented during the inter-sector gap time, and the incremented track address is transmitted serially to the addressed selection unit.

At the beginning of the intersector gap time, flip-flops SECPD and POST are in the set state and flip-flops TSE, DSL, and RWP are in the reset state. Read/write clock signal RWCK is generated by the local oscillator, as described in paragraph 4-55. SECPD is reset at the falling edge of sector pulse signal SPR or index pulse signal IPR.

S/SECPD = GND

R/SECPD = ...

C/SECPD = SECP

SECP = SPR + IPR

SPR = /SP/

IPR = /IP/

After SECPD is reset, TSE is set. Signal DSL is then direct set.

S/TSE = NRWP NSECPD

C/TSE = RWCK

M/DSL = TSE

Signal PXS comes true, enables a data transfer from the S-register to the P-register and from the T-register to the P-register, and clears the B-counter. (This data is the incremented track address and sector address.)

BX0 = PXS + ...

PXS = NRWP TSE

PXT = NRWP TSE

At the next clock signal, RWP is set, causing PXS to become false, and SECPD to be direct set.

S/RWP = PXS NRWE

C/RWP = RWCK

M/SECPD = SECPDM

SECPDM = RWP + ...

For the next 11 clock times, TSE is in the set state, and clock signal SC1D enables the 11-bit track address to be shifted out of the P-register to the selection unit. (Refer to paragraph 4-60.)

/SC1/ = SC1D

NSC1D = TSE RWP RWCK

/TRK/ = P11

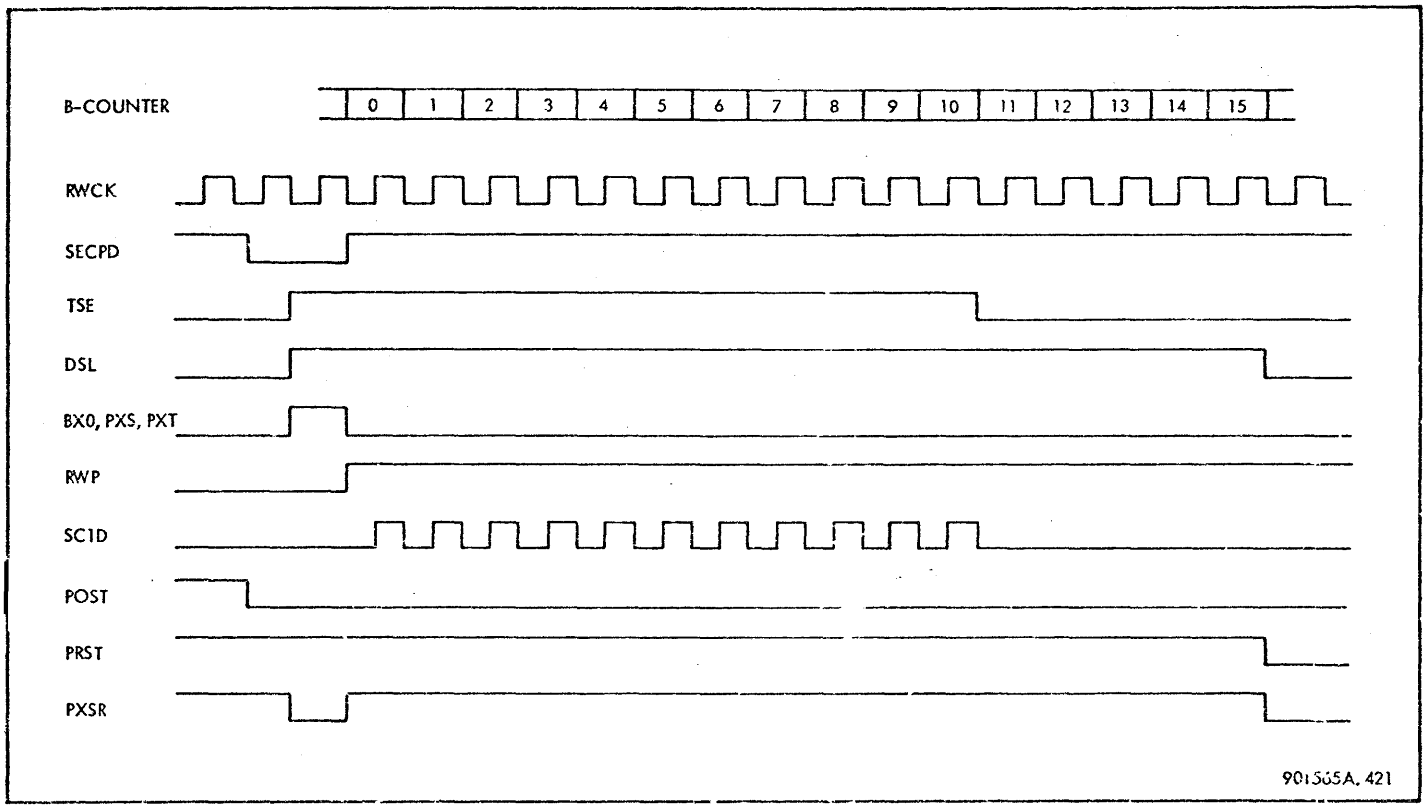


Figure 4-17. Track Shift Sequence, Timing Diagram

Flip-flop TSE is reset as the last track shift enable clock is generated.

R/TSE = TSERST

TSERST = B09 B11 + ...

C/TSE = RWCK

After the track address has been shifted, the sequence of operations depends on the type of order being executed.

4-61 <u>WRITE ORDER SEQUENCE</u>. If a write order is being executed, the B-counter is cleared, the track address is shifted, and RWP is set as described in paragraph 4-60. After the B-counter is cleared, it counts read/write clocks in binary sequence, as described in paragraph 4-56.

When the B-counter reaches a count of 72, PRE is set. (See figure 4-18.)

S/PRE = PRESET WRCH

PRESET = RWP B06 B09 NB10 NB11 (NPET + ...)

C/PRE = RWCK

While PRE is set (B-counter states 73 through 119), the five-byte preamble is written. (See paragraph 4-56.)

WPRE = WRITE PRE NBCE

When the B-counter reaches a count of 76, RWE is set if the sector under the read/write heads is the sector searched for (SECOMPR true) and if no errors have been detected. Refer to paragraph 4-72 for a description of error flip-flop operation.

S/RWE = PRE RWESET

RWESET = B10 SECOMPR NUNE NFAULT

NFAULT = NRER NSEN NWPV

C/RWE = RWCK

After RWE has been set, the read/write heads in the addressed selection unit are enabled by signal /WEN/, so that data signal /DAT/ and clock signal /SC2/ are validated.

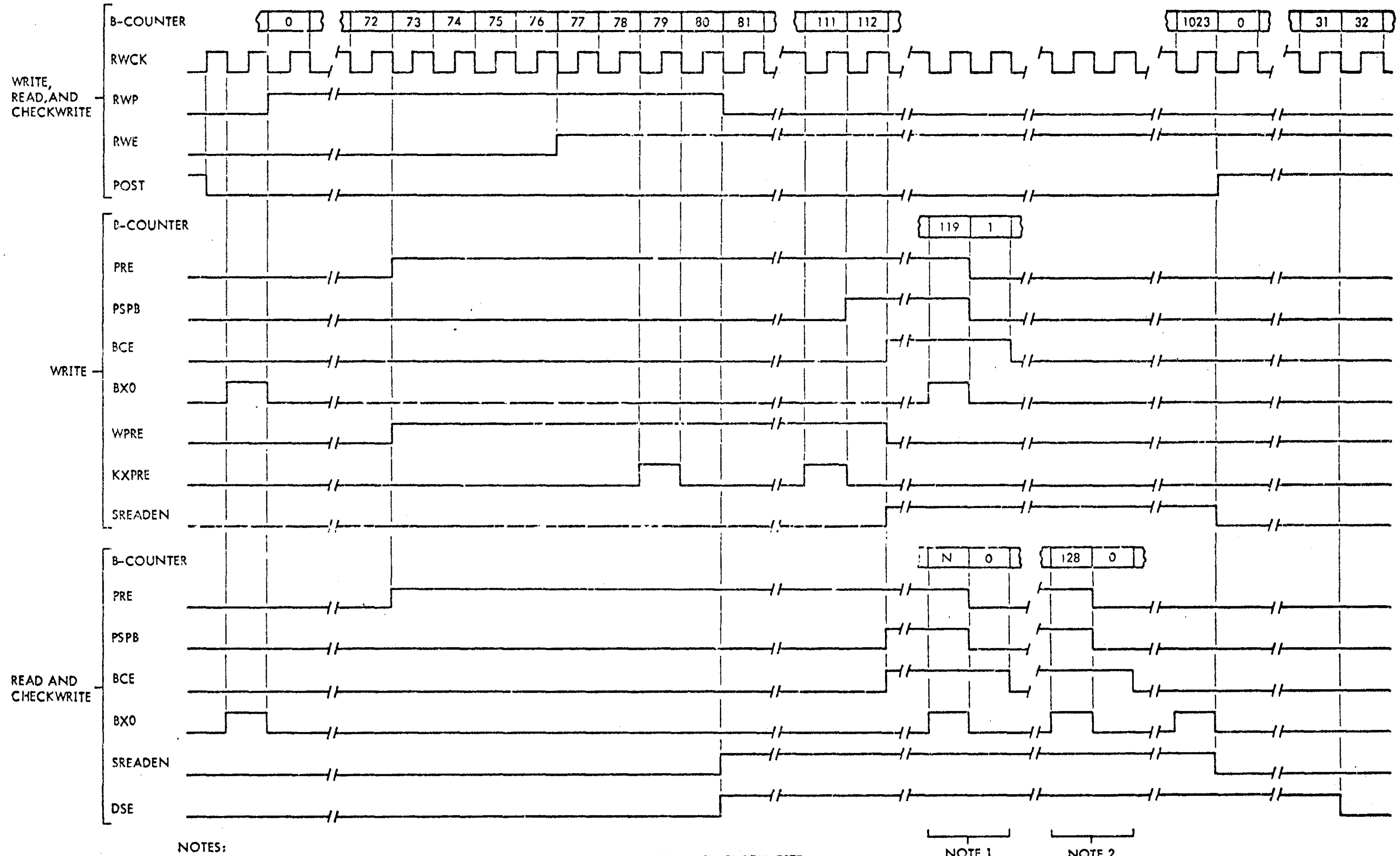
/WEN/ = WEND

WEND = WRITE RWE

/SC2/ = SC2D

SC2D = WRITE CLK3MH

/DAT/ = D07



NOTES:

1. FOR WRITE ORDER, FLIP-FLOP PRE RESET AT COUNT 119. FOR READ ORDER OR CHECKWRITE ORDER, FLIP-FLOP PRE RESET WHEN PREAMBLE SYNCHRONIZATION PATTERN RECOGNIZED, WHICH MAY TAKE PLACE WHILE COUNT (N) IS BETWEEN 112 AND 127
2. IF PREAMBLE SYNCHRONIZATION PATTERN IS MISSED DURING EXECUTION OF READ ORDER OR CHECKWRITE ORDER, FLIP-FLOP PRE RESET AT COUNT 128

901641A. 306

Figure 4-18. Interface Control Circuits, Timing Diagram

Flip-flop RWP is reset when the B-counter reaches 80.

R/RWP = RWPRST

RWPRST = B06 B08 + ...

C/RWP = RWCK

After the preamble is written, PRE is reset, BCE remains in the set state for one clock time, and the B-counter is preset to (0 000 000 001 000).

R/PRE = BX0

BX0 = PSPB WRITE BIT7RWE

PSPB = B07 B08 PRE RWE

BIT7RWE = B10 B11 B12 RWE

C/PRE = RWCK

S/BCE = PSPB

R/BCE = ...

C/BCE = RWCK

S/B09 = B09X1 BX0 + ...

B09X1 = WCHW RWE

When the B-counter reaches a maximum count (1 111 111 111 111), POST is set to identify the time for writing the postamble.

S/POST = NPOST NPRE

C/POST = B00 B01 B03 B04 B05 B05CK + ...

B05CK = B06 NBCE + ...

After the postamble has been written (32 bits), RWE is reset.

R/RWE = RWERST

RWERST = POSTB89 BIT7RWE

POSTB89 = POST B08 B09

BIT7RWE = B10 B11 B12 RWE

C/RWE = RWCK

The interface control circuits are now in the initial states, ready for sector pulse or index pulse and track address shifting, as before.

4-62 <u>READ ORDER SEQUENCE</u>. This paragraph emphasizes the difference in operation between the write order sequence described in paragraph 4-61, and the read order sequence.

If a read order is being executed, the B-counter is cleared, the track address is shifted, and RWP is set as described in paragraph 4-60. After the B-counter is cleared, it counts read/write clocks in binary sequence, as described in paragraph 4-56. When the B-counter reaches a count of 72, PRE is set, similar to a write order sequence. When the B-counter reaches a count of 76, RWE is set, similar to a write order sequence.

For a read order, the interface control circuits must search for the preamble synchronization pattern (0011), rather than write the preamble. The state of the B-counter when the pattern is detected may not be the same as the state of the B-counter when the pattern was written. Therefore, a search is conducted for the synchronization pattern for two byte times (16 bits). Furthermore, since data must be read from the selection unit, the data strobe signal must be allowed to control the read/write clock at some time during execution of the read order.

When the B-counter reaches a count of 80, RWP is reset as for a write order, and DSE is direct set, enabling read/write clock signal RWCK to be controlled by the data strobe signal.

M/DSE = DSEM

DSEM = NRWP REND

REND = RWE RCHW

RWCK = DSR DSE + ...

DSR = /DS/

Once set, DSE remains in the set state until RWE is reset at the end of the postamble.

S/DSE = DSE RWE

R/DSE = ...

C/DSE = RWCK

Preamble flip-flop PRE may be reset during any of the 16 clock times from count 112 of the B-counter to count 128 of the B-counter (PSPB true).

R/PRE = BX0

BX0 = PSPR + ...

PSPR = NDAR ND00 D01 D02 PSPBREND

PSPBREND = PSPB REND

PSPB = B07 B08 PRE RWE

C/PRE = RWCK

Signal PSPR is true when the preamble synchronization pattern (0011) has three bits in the D-register and one bit in data flip-flop DAR. If the preamble is missed, PSPB is true at count 127 and error flip-flop CER is set. (See paragraph 4-76.)

PSPM = B09 BIT7RWE NRWP PSPBREND

BIT7RWE = B10 B11 B12 RWE

For the read order, flip-flop BCE is set at count 112 to prevent a search for the preamble beyond count 127. If the preamble synchronization pattern is recognized, PRE is reset, and BCE is reset on the following clock, similar to a write operation.

S/BCE = PSPB

R/BCE = ...

C/BCE = RWCK

If the preamble synchronization pattern is not recognized, BCE remains in the set state, and a true BX0 signal is generated after B06 is reset at count 127.

BX0 = PRE NB06. ...

After BX0 is true, PRE is reset, then BCE is reset.

While BCE is set, the most significant flip-flops of the B-counter cannot be clocked.

(C/B00-C/B04) = PRE B05CK

B05CK = B06 NBCE

C/B05 = B05CK

After BCE is reset, the B-counter is cleared.

For the read order sequence, signal B09X1 is not true, and the B-counter begins counting data bytes with a count of (0 000 000 000 000). Thus the count of the B-counter is one less than the data byte being read, as in the following examples:

Data Byte	Write Order State	Read Order State
1	0 000 000 001 XXX	0 000 000 000 XXX
2	0 000 000 010 XXX	0 000 000 001 XXX
27	0 000 011 011 XXX	0 000 011 010 XXX
1023	1 111 111 111 XXX	1 111 111 110 XXX
1024	0 000 000 000 XXX	1 111 111 111 XXX

The least significant bits of the B-counter count the eight bits of each byte. During execution of a write order, the B-counter is cleared just before the last data byte is to be written.

Data accepted from the addressed selection unit is read by data flip-flop DAR after read/write enable flip-flop RWE is set.

S/DAR = DAIR REND

DAIR = /DAI/

REND = RWE RCHW

R/DAR = ...

C/DAR = RWCK

4-63 CHECKWRITE ORDER SEQUENCE. This paragraph emphasizes the differences in operation between the write order sequence described in paragraph 4-61, the read order sequence described in paragraph 4-62, and the checkwrite order sequence. If a checkwrite order is being executed, the B-counter is cleared, the track address is shifted, and RWP is set as described in paragraph 4-60. After the B-counter is cleared, it counts read/write clocks in binary sequence, as described in paragraph 4-56. When the B-counter reaches a count of 72, PRE is set, as for a write order sequence. For a checkwrite order, the interface control circuits must search for the preamble synchronization pattern (0011), as in the read order, rather than write the preamble. Since data must be read from the selection unit, the data strobe signal must be allowed to control read/write clock RWCK at some time during execution of the checkwrite order. Therefore, data strobe enable flip-flop is set, PRE is reset when the preamble synchronization pattern is recognized, and data flip-flop DAR reads data from the selection unit, similar to a read operation.

M/DSE = DSEM

DSEM = NRWP REND

REND = RWE RCHW

RWCK = DSR DSE + ...

DSR = /DS/

R/PRE = BX0

BX0 = PSPR + ...

PSPR = NDAR ND00 D01 D02 PSPBREND

S/DAR = DAIR REND

DAIR = /DAI/

R/DAR = ...

C/DAR = RWCK

4-64 SENSE ORDER SEQUENCE. During execution of a sense order, the interface control logic inhibits data transfer until the period of the intersector gap time following the transfer of the track address. This restriction guarantees that data accumulated for the sense order (figure 3-5) identifies the next sector for which a full 1024 data bytes can be processed. During the order out service cycle and after the sense order code is stored, service call signal SCD cannot be raised until flip-flop SEN is set and flip-flop TSE is reset.

M/SCN = DCB PHFS CYCLE/C N(NSCNMEN)

N(NSCNMEN) = NCDN SCNMEN1 + ...

SCNMEN1 = SEN NTSE + ...

Flip-flop SEN is not set until the previously incremented track address and sector address have been transferred from the T-register and the S-register to the P-register. (See paragraph 4-70.)

S/SEN = PXS SENSE

PXS = TSE NRWP

C/SEN = RWCK

Flip-flop TSE is reset by the following read/write clock. (See paragraph 4-60.) Once SEN is set, it cannot be reset until the order in service cycle is entered, causing NDATA to be true. (See paragraph 4-29.)

R/SEN = NDATA

Therefore, for a sense order, the data in service cycle for the first byte cannot begin until SEN is set, after which a transfer from phase FS to phase FSZ is possible. Flip-flop SCN is direct set during phase FS. When CDN is set, the direct set equation is inhibited and the order in service cycle follows.

4-65 ADDRESSING CIRCUITS

4-66 P-Register

The P-register, which consists of flip-flops P00 through P15 and associated logic elements, is clocked by read/write clock signal RWCK. Refer to paragraph 4-55 for a description of the read/write clock. A flip-flop of the P-register is reset if the reset input is true and if the set input is false. If the set input is true, the flip-flop is set regardless of the level of the reset input. Equations for the P-register are written with the following simplifications.

PXSR-1 = PXSR-2 = PXSR (P-register shift right)

PRST-1 = PRST-2 = PRST (Preset P-register)

(RWCK-1-RWCK-4) = RWCK (Read/write clock)

Reset inputs to the P-register are true when a D-register shift left is enabled (DSL true) and during the intersector gap time when data cannot be read from, or transmitted to, the addressed selection unit (NRWP true).

(R/P00-R/P15) = PRST

PRST = DSL + NRWP

For one clock time during the intersector gap time, signal PXT is true, causing the track overflow bit TOF and the contents of the T-register to be transferred to the P-register. (See figure 4-17.)

S/P00 = PXT TOF + ...

PXT = TSE NRWP

S/P01 = PXT T00 + ...

. .
. .
. .

S/P11 = PXT T10 + ...

At the same time, a sector address is stored in flip-flops P12 through P15.

S/P12 = PXS S00 + ...

PXS = TSE NRWP

S/P13 = PXS P13LD + ...

P13LD = P13LDEN + S01

P13LDEN = S03 S02 S00 EXT

S/P14 = PXS S02 + ...

S/P15 = PXS S03 + ...

For all sector addresses from 0000 through 1010, the contents of the S-register are transferred unchanged. Therefore, during the incrementing process described in paragraph 4-70, the normal binary sequence will be followed until a count of 1011 is reached. For this count, a value of 1111 will be transferred to the P-register if an EP RAD storage unit is connected (signal EXT true). In this case, the incrementing process generates an address of 0000, so that a sector match occurs for sector 0000 of the next track. (The track address is incremented in normal binary sequence each time that the sector address changes from 1111 to 0000.)

Just before preamble time, the incremented track address is returned to the T-register and the incremented sector address is returned to the S-register. During preamble time (PRE true), the P-register is preset to all ones in preparation for generation of the checksum. When signal PXSR is true, the contents of the P-register are shifted right, while new data is stored in flip-flop P00.

S/P00 = PXSR P00SET

PXSR = PRST NPXS

S/P01 = PXSR P00 + ...

. .
. .
. .

S/P15 = PXSR P14 + ...

The new information is used to generate the checksum while data is processed, as described in paragraph 4-71.

4-67 S-Register

The S-register, which consists of buffered latches S00 through S03 and associated logic elements, stores the address of the sector at which a read sequence or write sequence will begin when executed. During execution of a seek order, the S-register is loaded from the J-register under control of the byte counter and the TRL delay line, as described in paragraph 4-97.

S00 = J04 SXJ + ...

SXJ = SEEK RWRITEDO BKWZ TRS130

S01 = J05 SXJ + ...

S02 = J06 SXJ + ...

S03 = J07 SXJ + ...

Signal SX0 is used to clear the S-register before storage of new data and to retain the stored data.

S00 = S00 SX0 + ...

. .
. .
. .

S03 = S03 SX0 + ...

During phase RS of an order out service cycle, the S-register is cleared if a seek order is to be executed, so that a new address can be stored.

NSX0 = PHRS ORDOUT SEEK + ...

At the beginning of each sector, the S-register is cleared just before the incremented value is transferred from the P-register if a read order, write order, or checkwrite order is being executed.

NSX0 = RWP TDL020 + ...

S00 = SXP P12 + ...

SXP = STXPEN TDL100

STXPEN = SXPEN RWP

SXPEN = NPET + ...

S01 = SXP P13 + ...

S02 = SXP P14 + ...

S03 = SXP P15 + ...

Sector compare signal SECOMPR is controlled by a comparison between the contents of the S-register and the angular position signals from the addressed selection unit.

SECOMPR = (AN0R + NS00) N(AN0R NS00)
(AN1R + NS01) N(AN1R NS01)
(AN2R + NS02) N(AN2R NS02)
(AN3R + NS03) N(AN3R NS03)

AN0R = /AN0/

AN1R = /AN1/

AN2R = /AN2/

AN3R = /AN3/

4-68 T-Register

The T-register, which consists of buffered latches T00 through T10 and associated logic elements, stores the address of the track from which data will be read or into which data will be written. During execution of a seek order, the T-register is loaded from the J-register under control of the byte counter and the TRL delay line, as described in paragraph 4-97. The 11 bits (two of which should always be zeros) are stored in two consecutive bytes.

T00 = J01 TXJ + ...

TXJ = SEEK RWRITEDO BKZW TRS130

T01 = J02 TXJ + ...

. .
. .
. .

T06 = J07 TXJ + ...

The bits of the second byte are transferred from the J-register to both the T-register and the S-register.

T07 = J00 SXJ + ...

SXJ = SEEK RWRITEDO BKWZ TRS130

T08 = J01 SXJ + ...

T09 = J02 SXJ + ...

T10 = J03 SXJ + ...

Signal TX0 is used to clear the T-register before storage of new data and to retain the stored data.

T00 = T00 TX0 + ...

.
.
.

T10 = T10 TX0 + ...

During phase RS of an order out service cycle, the T-register is cleared if a seek order is to be executed, so that a new address can be stored.

TX0 = SX0

NSX0 = PHRS ORDOUT SEEK + ...

At the beginning of each sector, the T-register is cleared just before the incremented value is transferred from the P-register if a read order, write order, or checkwrite order is being executed.

TX0 = SX0

NSX0 = RWP TDL020 + ...

T00 = TXP P01 + ...

TXP = STXPEN TDL100

STXPEN = SXPEN RWP

SXPEN = NPET + ...

T01 = TXP P02 + ...

.
.
.

T10 = TXP P11 + ...

4-69 U-Register

The U-register, which consists of flip-flops U0, U1, and U2 and associated logic elements, stores the address of the EP RAD storage unit addressed for an input/output operation. The set input signals to the U-register come true and are latched during phase FSL of a response to an IOP command. Data is clocked into the U-register only when device controller busy flip-flop DCB is set when a new input/output operation is started.

(C/U0-C/U2) = DCBSET

DCBSET = PHFSL SIOPOSS OPER

SIOPOSS = SIOU NDCB NCIL

(R/U0-R/U2) = ...

S/U0 = SU0D

SU0D = DA5R IOP + PHFSL SU0D + ...

S/U1 = SU1D

SU1D = DA6R IOP + PHFSL SU1D + ...

S/U2 = SU2D

SU2D = DA7R IOP + PHFSL SU2D + ...

During phase FSL of any input/output sequence, the contents of the U-register are compared with the contents of IOP data lines /DA5/ through /DA7/. Signal DVSEL is true if the two sets of signals are identical.

DVSEL = (SU0D + NU0) N(SU0D NU0) (SU1D + NU1) N(SU1D NU1) (SU2D + NU2) N(SU2D NU2)

The contents of the U-register control address signals to the EP RAD storage units.

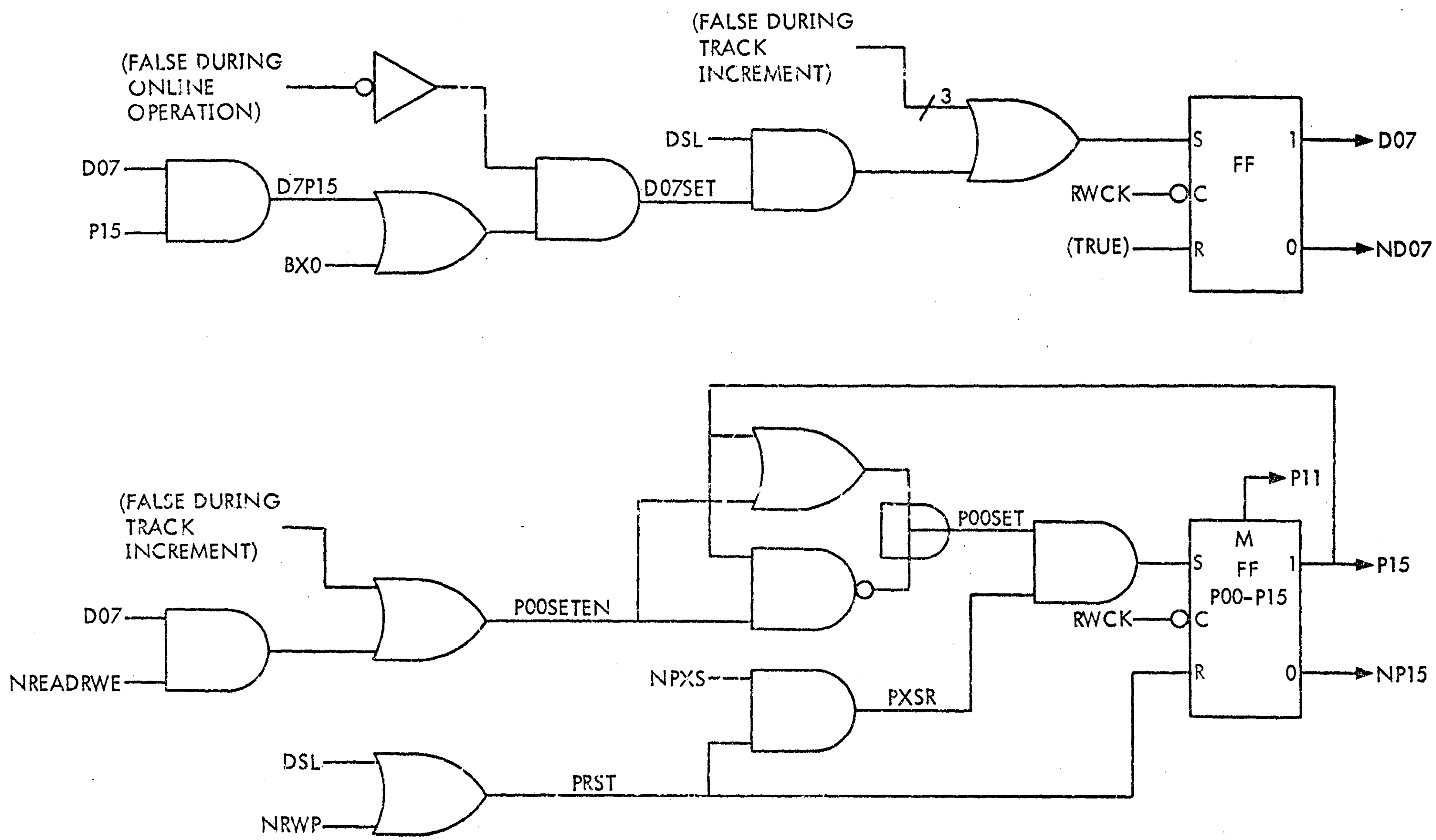
/ID0/ = SU0D

/ID1/ = SU1D

/ID2/ = SU2D

4-70 Address Incrementation

The initial track address and sector address are loaded by a seek order, as described in paragraph 4-97. During execution of a read order, write order, or checkwrite order, two operations must take place during the intersector gap time. First, the sector address must be incremented so that a true sector compare signal SECOMPR can be generated for the next sector in sequence. Second, if the sector address changes from 1011 (binary 11) to 0000, the track address must be incremented, so that the next track address in sequence can be selected. These operations are controlled by the P-register and flip-flop D07 of the D-register. (See figure 4-19.)



901565A. 423

Figure 4-19. Address Incrementation, Simplified Logic Diagram

During the intersector gap time, the contents of the T-register and S-register are transferred to the P-register when PXS and PXT are true. (See figure 4-17.) Flip-flop D07 is set at the same time.

S/D07 = D07SET DSL + ...

D07SET = BX0 + ...

For the next 16 clock times, the contents of the P-register are shifted right (from P00 toward P15) while new data is stored in P00. For 11 of the 16 clock times, the 11-bit track address is transmitted to the addressed selection unit.

/SC1/ = SC1D (Clock)

/TRK/ = P11 (Track address bits)

Flip-flop D07 acts as the carry flip-flop for a serial addition of one of the contents of the P-register. After the one preset in D07 is added to the least significant bit (P15) of the P-register, D07 remains in the set state if a carry is generated.

S/D07 = D07SET DSL + ...

D07SET = D07 P15

As the serial addition process continues, the incremented address is shifted into P00, and the more significant bits of the previous address are shifted into P15. When no carry is generated, D07 is reset and the bits of the previous address are shifted unchanged.

S/P00 = PXSR P00SET

P00SET = (P00SETEN + P15) N(P00SETEN P15)

P00SETEN = D07 NREADRWE + ...

Therefore, as a track address is transmitted to the addressed selection unit, a new track address is generated and stored in the P-register. Just before flip-flop RWP is reset, the new track address and sector address are transferred to the T-register and the S-register.

TXP = STXPEN TDL100

STXPEN = SXPEN RWP

SXPEN = NPET + ...

SXP = STXPEN TDL100

Circuits of the P-register store a code of 1111 in flip-flops P12 through P15 if the code in the S-register is 1011. Thus, when the address incrementation process takes place, the new sector address is 0000 and the track address is incremented in normal binary sequence.

4-71 Checksum Generation

The checksum is generated in the P-register during the execution of a write order, read order, or checkwrite order. In all cases, the 16-bit checksum is transferred to the D-register one byte at a time after the 1024 bytes of the sector have been processed. For a write order, the checksum is written on the disc file in the sector for which the checksum was generated. For a read order or checkwrite order, the checksum generated during execution of the order is compared bit-for-bit with the checksum read from the disc file. (See figure 4-20.)

After flip-flop PRE is set and RWP is reset (figure 4-18), the P-register is loaded with all ones.

S/P00 = PRE NRWP + ...

After the preamble has been written during execution of a write order or detected during execution of a read order or checkwrite order, PRE is reset and the process of generating the checksum begins. Because signal PRST is true, the contents of the P-register are continually shifted right (from P00 toward P15) and new data is entered in P00.

S/P00 = PXSR P00SET + ...

PXSR = PRST NPXS

PRST = NRWP + ...

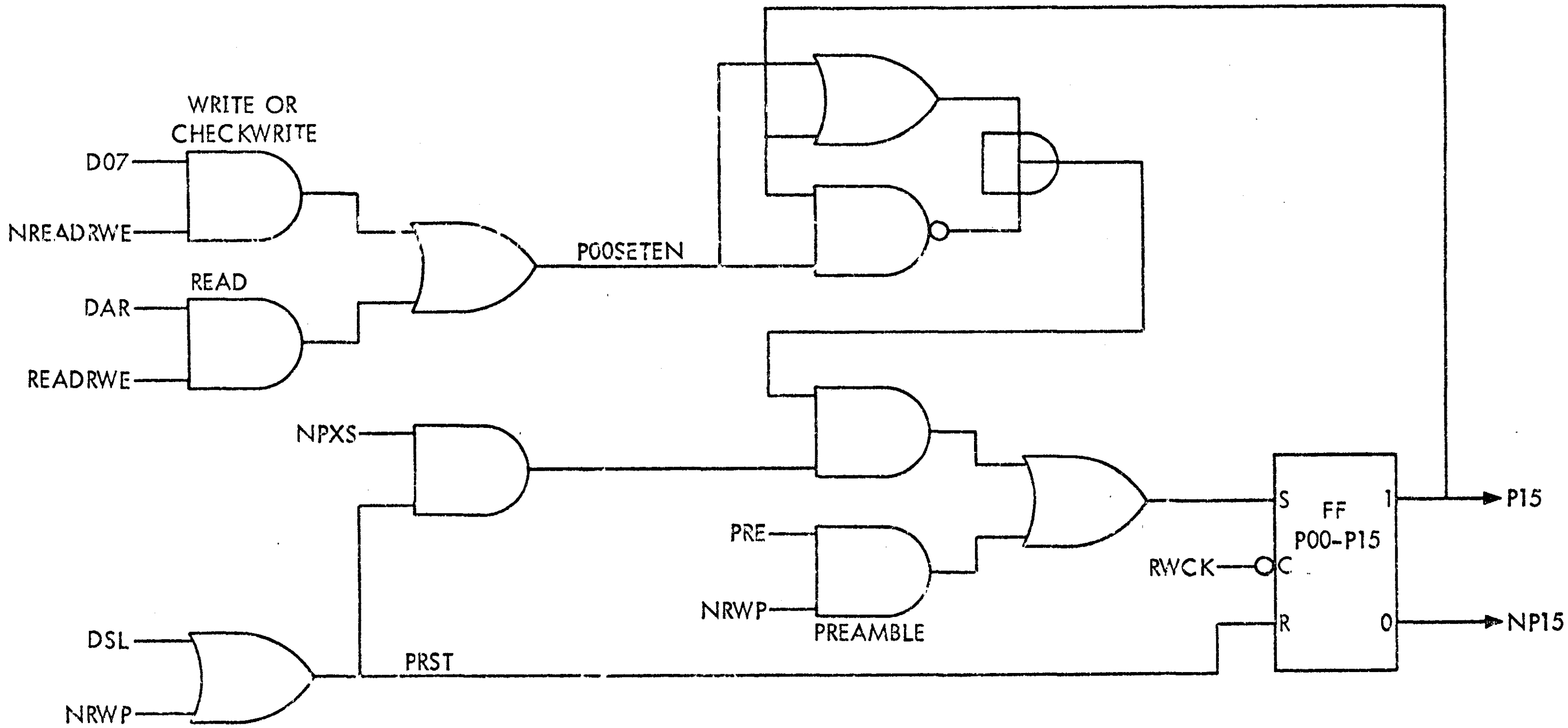
During execution of a write order or checkwrite order (NREADRWE true), P15 and D07 generate the new data; during execution of a read order (READRWE true), P15 and DAR generate the new data.

P00SET = (P00SETEN + P15) N(P00SETEN P15)

P00SETEN = READRWE DAR + NREADRWE D07

READRWE = READ RWE

In either case, an exclusive OR operation is performed on the content of the P-register and the new data, as indicated in figure 4-20, for execution of a write order or checkwrite order. Data bytes are stored in the D-register and read serially as data is circulated in the P-register. In the example of figure 4-20, a byte of 1011 0010 in the D-register, when processed with the 1111 1111 initially in the P-register, produces a byte of 0100 1101, which is stored in the P-register. The second data byte of the example, when processed with the 1111 1111 initially stored in the second half of the P-register, produces a byte of 1010 1100. In a similar manner, after these bytes are processed with additional data bytes, the P-register contains (from P15 to P00) the bits 0000 1111 0101 1010, which will be processed with the next data bytes received. The 16 bits stored in the P-register after 1024 data bytes are processed (including any bytes of all zeros) become the



BYTE NO.	1	2	3	4	5	6
D-REGISTER (READ FROM D07)	D07 — D00	D07 — D00	D07 — D00	D07 — D00	D07 — D00	D07 — D00
	1011 0010	0101 0011	0100 0010	1111 0110	---- ----	---- ----
P-REGISTER (READ FROM P15)	1111 1111	1111 1111	0100 1101	1010 1100	0000 1111	0101 1010
	P15 ———— P00		P15 ———— P00		P15 ———— P00	

NOTES:

1. BYTES 1 AND 2 REPRESENT INITIAL CONTENTS OF P-REGISTER
2. P-REGISTER BYTES 3-6 ARE GENERATED FROM CONTENTS OF D-REGISTER AND P-REGISTER

901565A. 424

Figure 4-20. Checksum Generation, Simplified Logic Diagram checksum stored on the disc file. When data is read serially from the disc file at the output of flip-flop DAR, the checksum generated should be identical to the checksum read from the disc file following the 1024 data bytes. The process is identical whether POOSETEN is controlled by D07 or DAR.

4-72 ERROR CIRCUITS

The error circuits of the controller consist of the flip-flops listed in table 4-5 and of the associated logic elements. These flip-flops and the signals controlled by them provide information to the IOP concerning error conditions that occur during execution of orders or as a result of power failure or from programming errors. Error signals are provided during the order in service cycle of an input/output operation. Program response to these error conditions may cause data to be provided by execution of additional commands (TDV, AIO, TIO, HIO, or SIO), as summarized in table 4-5.

4-73 Unusual End Logic

Unusual end flip-flop UNE may be direct set during phase FS of any service cycle other than an order out service cycle.

M/UNE = UNEM

UNEM = CYCLE/C DCB NORDOUT PHFS (CER + UNEM1 + DRESET)

UNEM1 = RER + SUN + WPV + NFKI ORDO PER REMPTY + NORD2 NORD3 NORD4 + ORDIN PER + ORD1 SENSE + NDVOR

DVOR = /DVO/

DRESET = PWRMONR

PWRMONR = /PWRMON/

Order Unavailable Write Protect Violation

Direct set of UNE takes place if error flip-flop CER, RER, SUN, or WPV is set. Signal /DVO/ is controlled by the addressed selection unit and is true if the addressed device is not operational, as described in paragraph 4-104. Signal /PWRMON/ is controlled by circuits which detect power failure, as described in paragraph 4-7. Of the 32 possible order codes, eight are interpreted as seek orders (X XX11), eight as read orders (X XX10), four as write orders (X X001), and four as checkwrite orders (X X101).

Table 4-5. Summary of Error Flip-Flops and Signals

FLIP-FLOP	FUNCTION	IOP INTERFACE SIGNALS CONTROLLED: TDV*	TSH†	AIO*	Order In**
CER	Checkwrite error	-	-	-	/DA0/
INL	Incorrect length	-	-	-	/DA1/
PER	Parity error (checksum)	-	-	-	/DA0/
RER	Rate error	/FR0/ /IOR/	-	/DA0/ /IOR/	/DA0/
SUN	Sector unavailable	/FR2/ /IOR/	-	/DA2/ /IOR/	-
UNE	Unusual end	-	/FR4/	-	/DA4/
WPV	Write protect violation	/FR3/ /IOR/	-	/DA3/ /IOR/	-

*/IOR/ controlled by FAULT = RER + SUN + WPV

†TSH = TIO + SIO + HIO

**/DA0/ controlled by TER = CER + PER + RER

Of the remaining eight, four are illegal (X X000). Of the possible forms of the sense order (X X100), two are illegal (X 1100). Any one of the six illegal order codes causes UNE to be direct set.

UNEM1 = NORD2 NORD3 NORD4 + ORD1 SENSE + ...

SENSE = ORD2 NORD3 NORD4

Parity error flip-flop PER, which can be set only during execution of a read order, causes UNE to be set for two different conditions. For a read record order (0 XX10), UNE is set during the order in service cycle, after a count done terminal order has indicated that the entire record has been read.

UNEM1 = ORDIN PER + ...

For a read sector order (1 XX10), UNE is set if an error occurs while data is read from any sector. End of sector is indicated by an empty K-register (NKFI true) and an empty FAM module (REMPTY true).

UNEM1 = ORD0 PER NKFI REMPTY + ...

If UNE is direct set for any reason, flip-flops (DATA, IN) will be placed in the (0, 1) state, as described in paragraph 4-32, because signal DATASET will be false.

NDATASET = UNE + ...

Therefore, an order in service cycle will occur if UNE is set during any input/output operation. The order in service cycle is begun after phase FS is entered. Flip-flop UNE may be set by the IOP during terminal order operations, as described in paragraph 4-34. If UNE is set by a terminal order, the sequence of operations is identical to that caused by a direct set signal. Once set, UNE must be reset by either a RESET signal or a MANRST signal.

R/UNE = RESET

C/UNE = NTCS000

E/UNE = MANRST

MANRST = NPET RSTR

RSTR = /RST/

4-74 Parity Error Logic

Parity error flip-flop PER can be set only during execution of a read order and then only while the checksum is being read from the addressed selection unit. The checksum read from the addressed selection unit through signal DAR is compared with the checksum generated in the P-register during execution of the read order and read from P15. If the two checksums are not identical, PER is set.

S/PER = PEREN P0OSET

PEREN = READRWE POST NB08

P0OSET = (P0OSETEN + P15) N(P0OSETEN P15)

P0OSETEN = READRWE DAR + ...

C/PER = RWCK

Once set, PER causes UNE to be direct set and can be reset only by a RESET signal.

R/PER = GND

E/PER = RESET

4-75 Write Protect Violation Logic

Write protect violation flip-flop WPV is set if a write order is attempted on a write protected track. Track-protected signal /TRP/ is generated within the addressed selection unit as described in paragraph 4-106.

S/WPV = PRE WPVSET

WPVSET = WRITE TRPR

TRPR = /TRP/

C/WPV = RWCK

If WPV is set during the preamble time, it causes UNE to be direct set and can be reset only by a RESET signal.

R/WPV = GND

E/WPV = RESET

4-76 Checkwrite Error Logic

Checkwrite error flip-flop CER can be direct set if an index pulse or sector pulse is received while RWE is set. This condition would occur if data strobes are missed during execution of a read order or checkwrite order. In that case, the B-counter value would be incorrect.

M/CER = CERM

CERM = RWE SECP

SECP = IPR + SPR

SPR = /SP/

IPR = /IP/

Flip-flop CER is set during execution of a checkwrite order if the checksum bits read from the disc file through flip-flop DAR do not match the checksum bits generated during execution of the checkwrite order. The checksum bits are read from D07 after transfer from the P-register. An exclusive OR gate is enabled by signal CHWEREN to make the comparison.

S/CER = CERSET

CERSET = CHWER + ...

CHWER = CHWEREN (DAR + D07) N(DAR D07)

CHWEREN = CHWR NPOST NPRE RWE

C/CER = RWCK

During execution of a read order or a checkwrite order, a search is conducted for the preamble synchronization pattern, as described in paragraph 4-56. If the preamble synchronization pattern is not detected, signal PSPM is true and CER is set.

S/CER = CERSET

CERSET = PSPM + ...

PSPM = PSPBREND NRWP BIT7RWE B09

PSPBREND = PSPB REND

PSPB = PRE RWE B07 B08

REND = RCHW RWE

C/CER = RWCK

If CER is set, it remains in the set state until signal RESET is true. Before RESET is true, CER causes UNE to be direct set.

R/CER = GND

E/CER = RESET

4-77 Sector Unavailable Logic

Sector unavailable flip-flop SUN may be set in the preamble time interval during which PRE is set and RWE is reset. (See figure 4-18.)

S/SUN = PRENRWE SUNSET

PRENRWE = PRE NRWE

SUNSET = S00 S01 EXT + T00 + T01 + T02 NTYP0R + T03 NTYP0R NTYP1R + ...

R/SUN = GND

C/SUN = RWCK

This interval follows the transfer of the incremented address from the P-register to the T-register and S-register, as described in paragraph 4-70. Therefore, SUN is set if a sector address stored in the S-register, or a track address stored in the T-register, represents a location which does not exist in the RAD storage unit. (Signals TYP0R, TYP1R, and EXT indicate the type of RAD storage unit, as described in paragraph 4-82.)

During execution of a seek order, the T-register is cleared and a new track address is stored. If the most significant bit of the new track address is a one, track overflow signal TOF comes true and is latched.

TOF = J00 TXJ + TOF TX0 + ...

TXJ = SEEK RWRITEDO BKZW TRS13C

TX0 = SX0

NSX0 = SEEK PHRS ORDOUT + ...

Because a track address with a most significant bit of one is invalid for any RAD storage unit, a true TOF signal causes direct set of SUN during phase TO of the data out service cycle.

M/SUN = SUNM

SUNM = NDATASET (PHTO TCS10C 3) (SEKSEND SUNSET)

NDATASET = CDN + ...

SEKSEND = SEEK NPHRSAOO + ...

SUNSET = TOF + T00 + T01 + T02 NTYP0R + T03 NTYP0R NTYP1R + S00 S01 EXT

Signal TOF becomes true and is latched if address incrementation causes the most significant bit of the track address to be true.

TOF = P00 TXP + TOF TX0 + ...

TXP = TDL100 STXPEN

A true TOF signal is not an error unless an attempt is made to read from, or to write into, the nonexistent addressed track. Therefore, for a sense order, a true TOF signal direct sets SUN to provide the unusual end data. The IOP is able to test for causes of unusual end.

M/SUN = SUNM

SUNM = NDATASET (PHTO TCS100-3) (SEKSEND SUNSET)

SEKSEND = SENSE NPHRSAOO + ...

If SUN is set, it remains in the set state until signal RESET is true. Before RESET is true, SUN causes UNE to be direct set.

E/SUN = RESET

4-78 Rate Error Logic

During execution of a write order or checkwrite order, data from the IOP must be provided in time for a transfer of data from the K-register to the D-register at the rate established by read/write clock signal RWCK. During execution of a read order, data must be accepted by the IOP before the FAM module is filled, and additional data must be stored in the FAM module at the rate established by read/write clock signal RWCK. Rate error flip-flop RER is set if either kind of rate is detected.

During execution of a read order, a rate error is detected if an attempt is made to transfer data from the D-register to the J-register (JXD true) when the FAM module is filled (NRKO true) and the IOP has not signalled count done (NCDN true). When all these conditions exist simultaneously, RER is direct set.

M/RER = RERM

RERM = JXD NRKO NCDN

During execution of a write order or a checkwrite order, a rate error is detected after the preamble has been written (NWPRE true) if an attempt is made to transfer data from the K-register to the D-register (DXK true) before the K-register has been filled (NKFICK true).

S/RER = REREN RERSET

REREN = DATA + JFI

RERSET = NWPRE DXK NKFICK

DXK = CHWR NPOST BIT7RWE NPRE + WRITE NPOST BIT7RWE + ...

C/RER = RWCK

When the K-register is filled from the FAM module, KFID comes true and is latched. Flip-flop KFICK is set by the following read/write clock and remains in the set state until the K-register is cleared following a K-register to D-register data transfer.

S/KFICK = KFID

KFID = KX0 (KFID + KFIDX1)

KFIDX1 = KFI TRS270

NKX0 = WCHW TDT2 + ...

R/KFICK = ...

C/KFICK = RWCK

Therefore, if a K-register to D-register transfer is attempted when KFICK is in the reset state, the K-register contains no new data.

A true JFI signal enables KFICK to set after the order in service cycle is in process. This signal is required for the multiple-byte interface, for which valid data may still be in the I-register after exit from the data out service cycle. (See paragraph 4-48.)

JFI = N(JFIRESET RWRITE-2 TRS180) (JFIX1 + ...)

Once RER is set, it can be reset only by signal RESET. Before signal RESET is true, RER causes an unusual end condition.

R/RER = GND

E/RER = RESET

4-79 Incorrect Length Logic

Incorrect length flip-flop INL is set for any one of three conditions:

a. The number of data bytes transferred during execution of a read order, write order, or checkwrite order is not an integral multiple of 1024.

b. The number of data bytes transferred during execution of a seek order is not 2.

c. The number of data bytes transferred during execution of a sense order is not 3.

Although these conditions are not necessarily errors, the information that INL was set may be required by a program. Therefore, although UNE is not set, a signal is returned to the IOP through signal /DA1/ during the order in service cycle.

/DA1/ = O01

O01 = OXORDIN INL + ...

Flip-flop INL is reset during any order out service cycle and is cleared following completion of any input/output operation.

R/INL = ORDOUT

C/INL = TCS100-3

E/INL = NDCB

Count done flip-flop CDN, which should be set after all data bytes have been transferred following execution of any order, controls signals related to setting flip-flop INL. During execution of a seek order or sense order, INL is set during the order in service cycle if CDN is not set.

S/INL = INLSET ORDIN

INLSET = INLEN SEKSEND + ...

SEKSEND = SEEK NPHRSAOO + SENSE NPHRSAOO

INLEN = NCDN + ...

During execution of a read order, INL is set during the order in service cycle if CDN is set and the K-register is still filled (KFI true). In this case, the byte transferred to the K-register is a byte of zeros which follows removal of all valid data bytes from the FAM module.

S/INL = INLSET ORDIN

INLSET = CDN READKFI + ...

READKFI = READ KFI

During execution of a write order or checkwrite order, INL is direct set if an attempt is made to transfer data from the K-register to the D-register (DXK true) after CDN has been set, the FAM module has been emptied (REMPTY true), and the preamble has been written (NWPRE true). These conditions exist after the last data byte has been stored in the [illegible]register following the removal of all valid data bytes from the FAM module and after a count done terminal order has been received from the IOP.

M/INL = INLM

INLM = CYCLER REMPTY CDN NWPRE DXK NKFID

4-80 INTERFACE TYPE LOGIC

4-81 Byte Width Logic

The data path between the IOP and the EP RAD controller may be one, two, or four bytes wide. For any byte width, data bytes are exchanged on a one-byte interface during execution of seek orders and sense orders. During execution of read orders, write orders, or checkwrite orders, data bytes may be transferred one, two, or four bytes at a time, depending on the states of signals /EDX2/ and /EDX4/ from the IOP. (See figure 4-21.) When the controller is service-connected (FSC true), signals /DX2/ and /DX4/ are sent to the IOP to indicate byte width, under control of signal WIDE which is true during execution of write orders, read orders, and checkwrite orders (WRCH true). Signals BYT1ID, BYT2ID, and BYT4ID are used internally during data transfers to control operations of the O-register, I-register, and related registers.

4-82 RAD Type Logic

Signals /TYP0/ and /TYP1/, which are accepted from the addressed RAD storage unit, indicate the storage capacity of the addressed RAD. For an EP RAD storage unit, both signals are true and signal EXT is true.

EXT = TYP0R TYP1R

TYP0R = /TYP0/

TYP1R = /TYP1/

Signal EXT controls operations within the controller. If EXT is true, read/write clock signal RWCK is nominally 3 MHz; if EXT is false, read/write clock signal RWCK is nominally 1.5 MHz. (See paragraph 4-55.)

For an EP RAD storage unit, the B-counter counts 1024 bytes per sector. (See paragraph 4-56.) For other types of RAD storage units, the B-counter is preset with a value of 1 010 011 000 XXX (decimal 664) and counts 360 bytes per sector.

S/B00 = PRE BX1MED + ...

BX1MED = RWE NEXT

S/B02 = PRE BX1MED + ...

S/B05 = PRE BX1MED + ...

S/B06 = PRE BX1MED + ...

For an EP RAD storage unit, there are 12 sectors per revolution; for other RAD storage units, there are 16 sectors per revolution. Therefore, signal LASTSECT is made true for a count of 1011, if EXT is true.

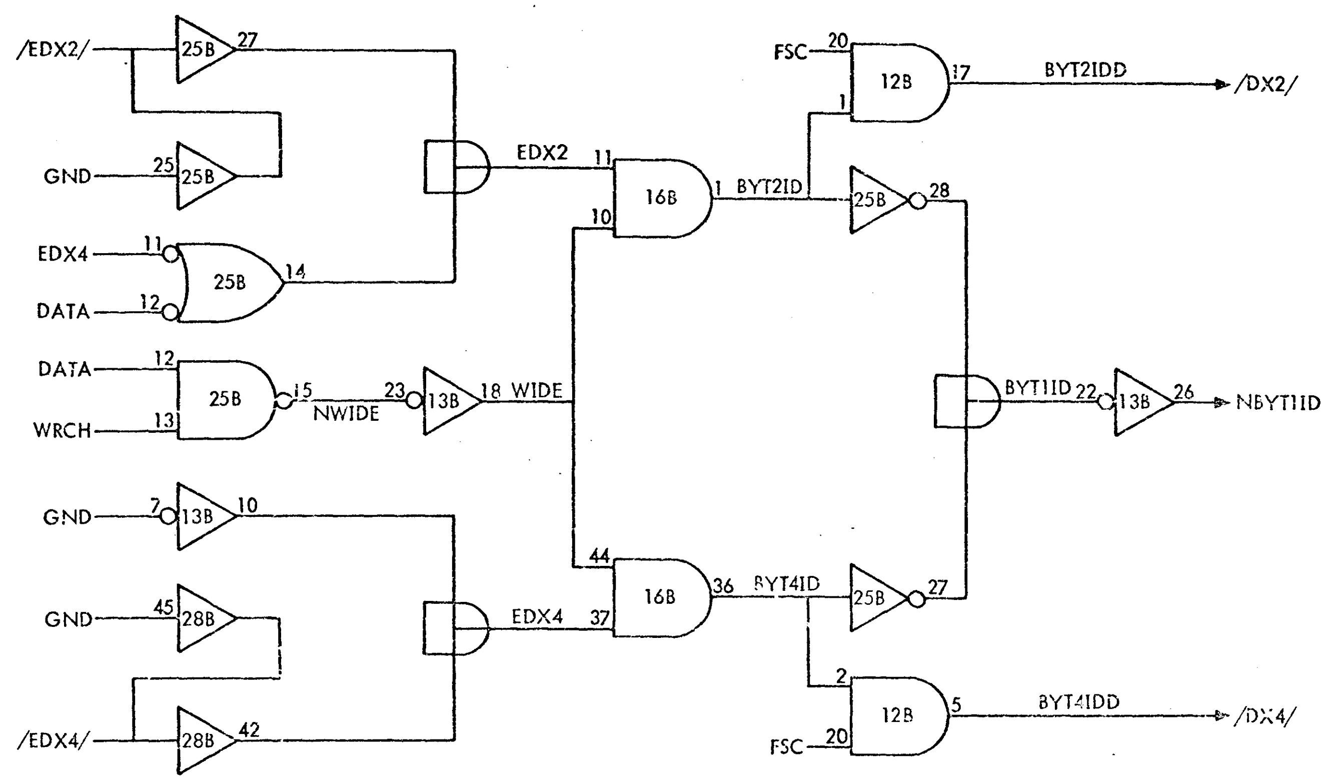
LASTSECT = AN0R AN1OTYP2 AN2R AN3R

AN1OTYP2 = AN1R + EXT

(Signal LASTSECT is used only by PET logic.)

4-83 OFFLINE OPERATION

Peripheral Equipment Tester Model 7901 (PET) can be used either to monitor operation of the EP RAD controller or to simulate IOP inputs to the EP RAD controller. In either



EDX2	EDX4	BYT1ID	BYT2ID (NOTE)	BYT4ID (NOTE)	DATA SIGNALS
0	0	1	0	0	/DA0/ - /DA7/
1	0	0	1	0	/DA0/ - /DA7/ /DB0/ - /DB7/
0	1	0	0	1	/DA0/ - /DA7/ /DB0/ - /DB7/ /DC0/ - /DC7/ /DD0/ - /DD7/

NOTE: BYT2ID OR BYT4ID TRUE ONLY WHEN WIDE IS TRUE

901565A. 425

Figure 4-21. Byte Width Circuits, Logic Diagram

case, the PET must be connected to the EP RAD controller through two cable connectors, as indicated in figure 7-5. When the PET is used to monitor operation of the controller, indicators on the PET panel read selected signals of the controller during online operation. When PET is used to simulate IOP inputs, no RAD storage unit attached to the controller is accessible to the IOP.

4-84 Online/Offline Control (See figure 4-22)

The EP RAD controller is placed in the online state by setting the switch on the LT25 module (location C23 in figure 7-5) to the 1 position. This action connects the PT18S signal to ground and energizes relays in the AT17 module (location C26 in figure 7-5). After these relays are energized, signal NINI is connected to ground and signal INI is disconnected from ground and allowed to go true. After signal INI is true, signal INC becomes true and signal NINC becomes false.

When the switch is placed in the 0 position, signal PT18S is open and two relays in the AT17 module are deenergized in sequence, causing signals INC and INI to go false in sequence and shorting signal AVI to signal AVO to complete the priority circuit to the next controller in sequence. When signal INI becomes false, the controller is effectively

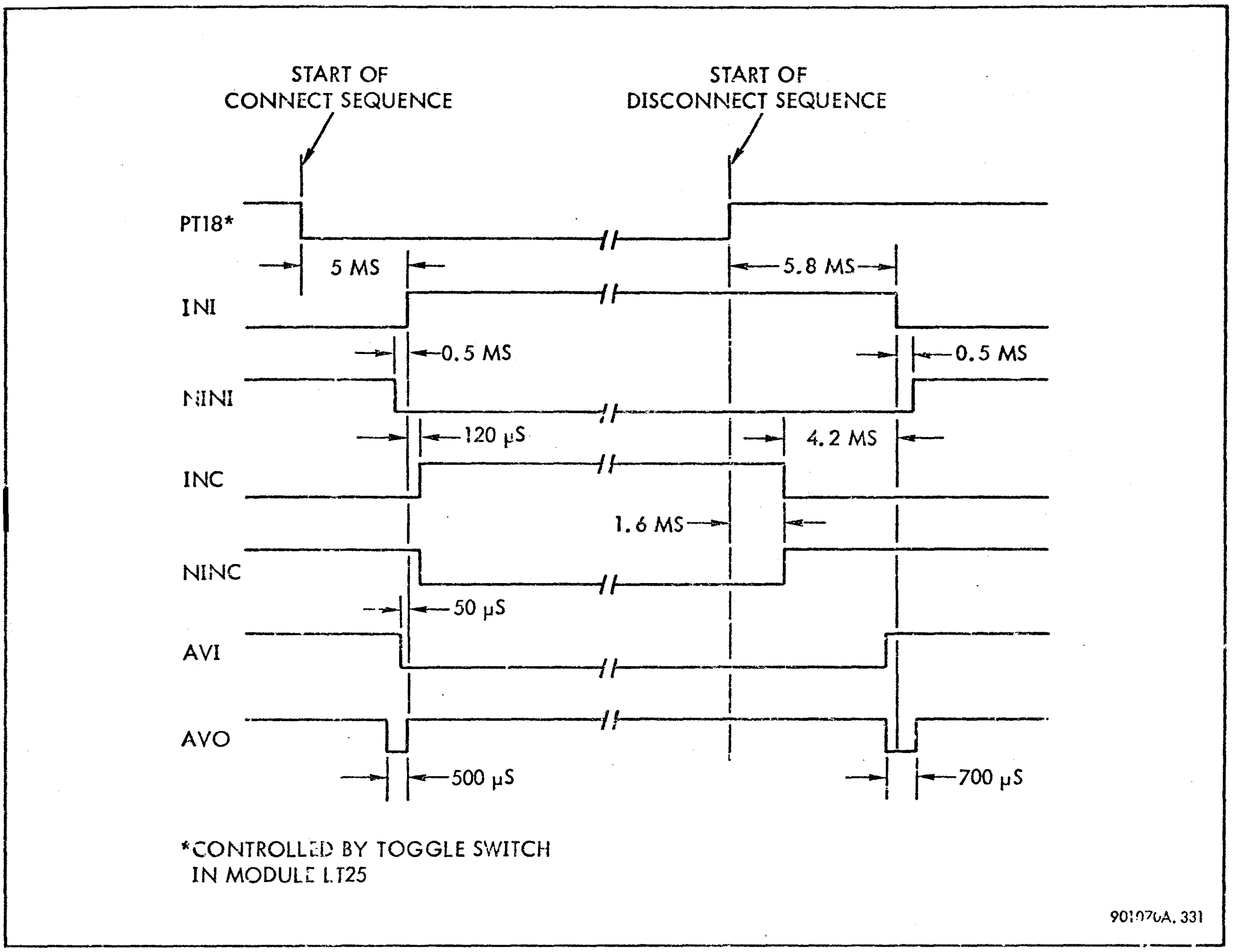


Figure 4-22. Connect-Disconnect Timing Diagram

disconnected from the IOP interface because signal INI grounds the following signals: AVOD, DCA, DORD, EDD, FR0D through FR7D, FSLD, HIPD, HPSD, ICD, IORD, O00 through O07, RSAR, RSD, NRSTR, and SCD.

Signal NINI, which is true, direct resets service connect flip-flop FSC.

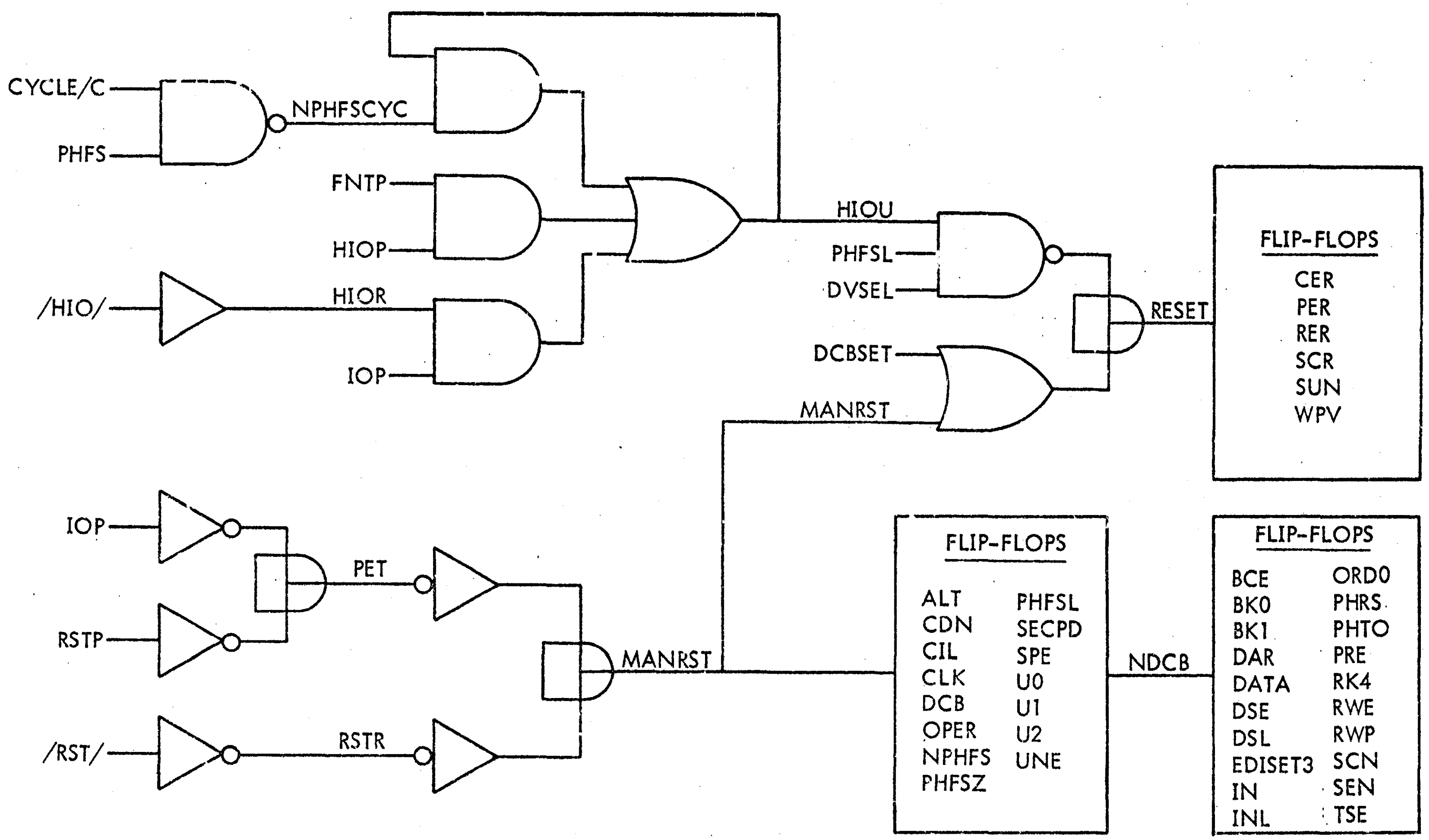
E/FSC = NINI + ...

4-85 Reset Control (See figure 4-23)

Control flip-flops of the EP RAD controller may be reset by manually-controlled signals or by computer-controlled signals. The error flip-flops (CER, PER, RER, SUN, and WPV) and SCR are reset by a halt input/output signal (HIOU), whether the HIO is controlled by the computer program or by an offline test. These flip-flops are also reset by DCBSET at the start of an input/output operation. At the end of an input/output operation, DCB is reset and causes one group of flip-flops to be reset. Computer-controlled signal RSTR, which can also be generated at a pushbutton on the computer control panel, generates a true MANRST signal. This signal resets the error flip-flops, flip-flop SCR, and a group of flip-flops that includes DCB. Therefore, signal RSTR resets all control flip-flops of the EP RAD controller. Signal MANRST is also controlled by the PET through PET reset signal RSTP. When the EP RAD controller is operating offline (PET true), MANRST is true whenever RSTP is true.

4-86 PET Operations

When the PET is connected to the controller, the signals listed in table 4-6 are available at the PET connectors. If the PET is used to monitor online operation of the controller,



901565A. 426

Figure 4-23. Reset Control, Simplified Logic Diagram

Table 4-6. PET Interface Control Signals

Signal	Source	Description
ALTP	32A-21	Alternate order control
CNTRCLKP	30A-14	Clock signal to the PET internal counter
DP00	30A-8	Simulated data byte stored in the J-register
DP01	30A-7	
DP02	30A-6	
DP03	30A-5	
DP04	30A-4	
DP05	30A-3	
DP06	30A-2	
DP07	30A-1	
ERSTOP	32A-20	Error stop signal that enables halt if error is detected
FSPS	32A-39	Function strobe simulation
HIOP	32A-26	Halt input/output function indicator simulation
INDUP	32A-19	Indicator signal control
IOP	32A-36	Online/offline control
ORDP1	32A-22	Order bit 1 simulation
ORDP2	32A-23	Order bit 2 simulation
ORDP3	32A-24	Order bit 3 simulation
ORDP4	32A-25	Order bit 4 simulation
REPEAT	32A-42	Continuous cycle control
RSTP	32A-40	Reset signal simulation
SGLPH	32A-18	Single-phase operation control
SGLPHCK	32A-43	Single-phase operation clock
SGLTRKP	32A-41	Single-track operation control
SIOP	32A-29	Start input/output function indicator simulation
TDVP	32A-27	Test device function indicator simulation
TIOP	32A-28	Test input/output function indicator simulation

(Continued)

Table 4-6. PET Interface Control Signals (Cont.)

Signal	Source	Description
TRKRST	30A-15	True when PET internal counter equals counter reset switch settings of PET panel
UAS0	30A-12	Storage unit address bit 0 simulation
UAS1	30A-11	Storage unit address bit 1 simulation
UAS2	30A-10	Storage unit address bit 2 simulation

signal IOP is true and signal INDUP, controlled from the PET panel, causes the signals listed in table 4-7 to be read. If the PET is used to control offline operation, signal IOP is false and signal PET is true, unless the PET reset signal RSTP is generated to reset the controller.

Signals DP00 through DP07 simulate data bytes and provide inputs to the J-register during data out service cycles (DATAOUT true).

```
J00       = DP00 JXDP + ...
     JXDP = DATAOUT RWRITE-2 TRS060 PET
J01       = DP01 JXDP + ...
 .            .
 .            .
 .            .
J07       = DP07 JXDP + ...
```

These signals replace IOP data for simulated write orders, checkwrite orders, and seek orders. For simulated sense orders and read orders, data is accepted from the disc file similar to online operation.

Signals ORDP1 through ORDP4 simulate bits of the order code and are accepted by the order register under control of alternate order signal ALTP and the alternate order circuits.

Signal UAS0 through UAS2 simulate storage unit address bits and are accepted by the U-register at the start of a simulated input/output operation.

```
SU0D          = UAS0 PET + ...
SU1D          = UAS2 PET + ...
(C/U0-C/U2)   = DCBSET
```

Signals HIOU, TIOU, TDVU, and SIOU can be controlled by signals HIOP, TIOP, TDVP, and SIOP to simulate commands from the IOP. The simulated function strobe signal from the PET is used to control operations.

```
HIOU          = FNTP HIOP
                + HIOU NPHFSCYC + ...
    FNTP      = FSP PET
    NPHFSCYC  = N(CYCLE/C PHFS)
TIOU          = FNTP TIOP
                + TIOU NPHFSCYC + ...
TDVU          = FNTP TDVP
                + TDVU NPHFSCYC + ...
SIOU          = FNTP SIOP
                + SIOU NPHFSCYC + ...
```

4-87 IOP SIMULATION. When the PET simulates IOP signals, the controller responds as if the IOP were providing the inputs. Inputs from the PET start the TCL delay line. (See figure 4-24.) Other operations follow in normal sequence, as described in paragraph 4-20.

When signal PET is true, device controller address signal DCAU is true to simulate a match of controller address and IOP address signals.

```
DCAU = PET + ...
```

The function strobe which starts execution of orders is controlled through signal FSU; the request strobe acknowledge signal from the IOP is simulated through signal RSAU; service connection is controlled through signal FSCU by service call flip-flop SCN. Function strobe signal FSU can be controlled by a pushbutton on the PET panel through signal FSPS or by a combination of PET signals and controller signals.

```
FSU    = PET NPHFSL (SCN + FSP)
    FSP = FSPS + ...
```

The function strobe is inhibited while the phase control logic is in phase FSL since signal NPHFSL becomes false. Additional service calls depend on the state of service call flip-flop SCN, which is controlled through signal CDNPET.

```
CDNPET = PET LASTSECT POSTB89 (TRKRST
         + SGLTRK) (EXT + ...)
```

Table 4-7. PET Interface Indication Signals

SIGNAL	SOURCE	DATA	
		If INDUP true	If INDUP false
IND01	19A-02	DCB	DCB
IND02	19A-01	READ	CIL
IND03	19A-39	WRITE	DVOR
IND04	19A-42	CHWR	RER
IND05	25A-42	UNE	PER
IND06	25A-39	T00	CER
IND07	25A-01	T01	WPV
IND08	25A-02	T02	SUN
IND09	25A-07	T03	DATA
IND10	25A-09	T04	IN
IND11	25A-46	T05	PHTO
IND12	25A-21	T06	PHRSA
IND13	25A-14	T07	PHRS
IND14	25A-12	T08	PHFSL
IND15	25A-27	T09	PHFSZ
IND16	25A-26	T10	PHFS

When the service call line is raised by SCN, the data in signals DP00 through DP07 are accepted for data out service cycles. For either data out or data in service cycles, request strobe acknowledge signal RSAU is simulated by signal RSAUEN.

RSAU = PET (BYT1ID + NJFI + NDATAOUT)

4-88 <u>SINGLE PHASE MODE</u>. The phase flip-flops described in paragraph 4-22 can be cycled through normal phase sequences one phase at a time if signal SGLPH is true. (See figure 4-24.) In this case, signal CYCLE/C, which controls start of the TCL delay line, is controlled through signal CYCEN (refer to paragraph 4-21 for a description of TCL delay line operation). Single phase enable flip-flop SPE is direct set whenever a TCL delay line cycle occurs. If signal SGLPH is true, CYCLE/C is inhibited by a false CYCEN signal until SPE is reset. Therefore, the TCL delay line cannot be started until SPE is reset. A true single phase clock signal SGLPHCK is generated by a PET panel pushbutton. As this signal goes false, SPE is reset and CYCLE/C is enabled. In this manner, the phases associated with any IOP command or any service cycle can be enabled one at a time.

4-89 <u>ALTERNATE ORDERS MODE</u>. The PET can cause the controller to either execute the order encoded by signals ORDP1 through ORDP4 or alternate execution of that order with execution of a write order. For execution of the order encoded in signals ORDP1 through ORDP4, signal ALTP is false and the PET order code is stored during phase RSA of the order out service cycle as for online operation.

M/ORD0 = ORDXPET

ORDXPET = PHRSA00 PET TCS000-3

ORD1 = ORDP1 ORDXPET + ...

ORD2 = ORDP2A ORDXPET + ...

ORDP2A = ORDP2 ALTORD

ALTORD = NALTP + ...

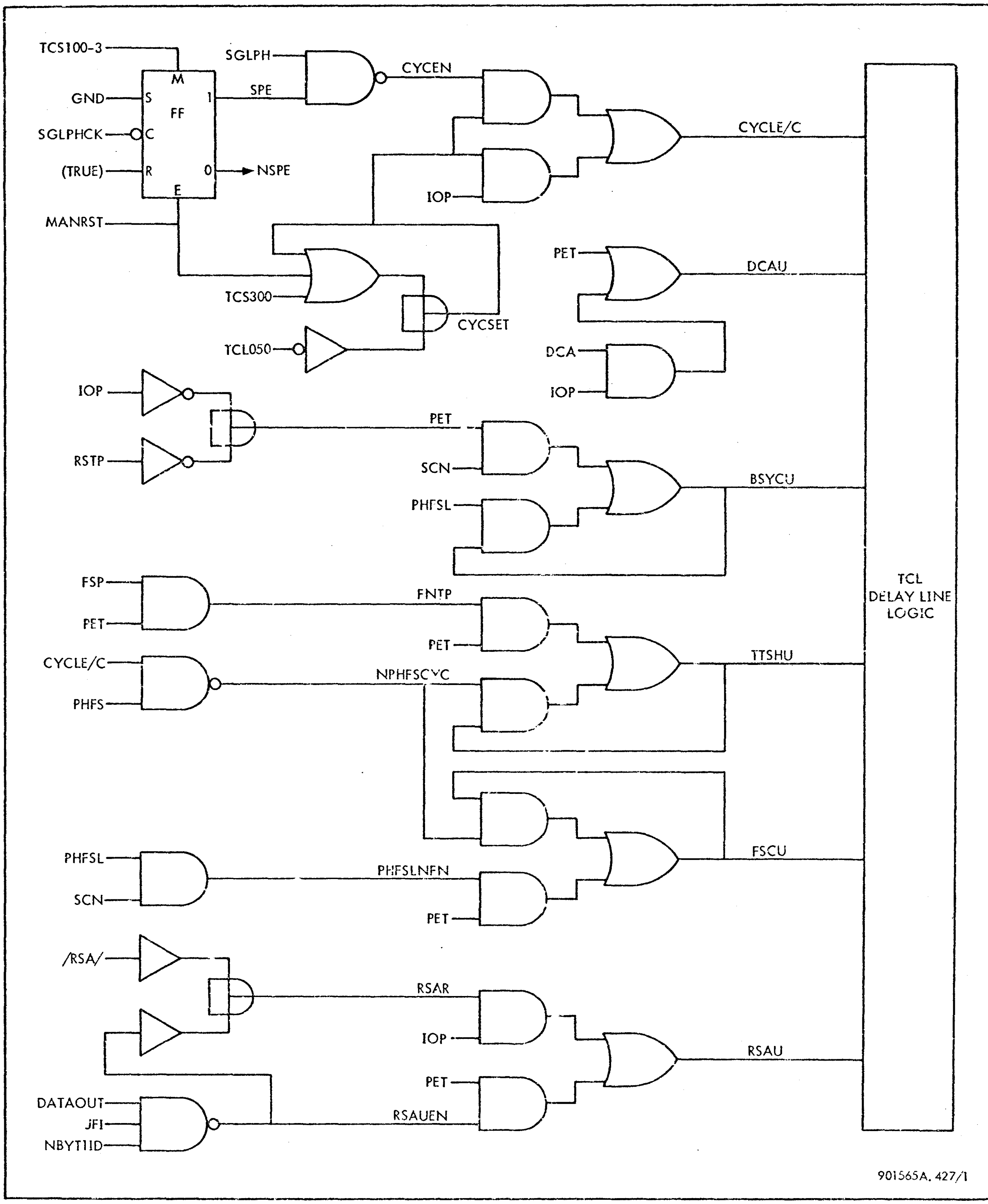


Figure 4-24. PET Interface Circuits, Simplified Logic Diagram (Sheet 1 of 2)

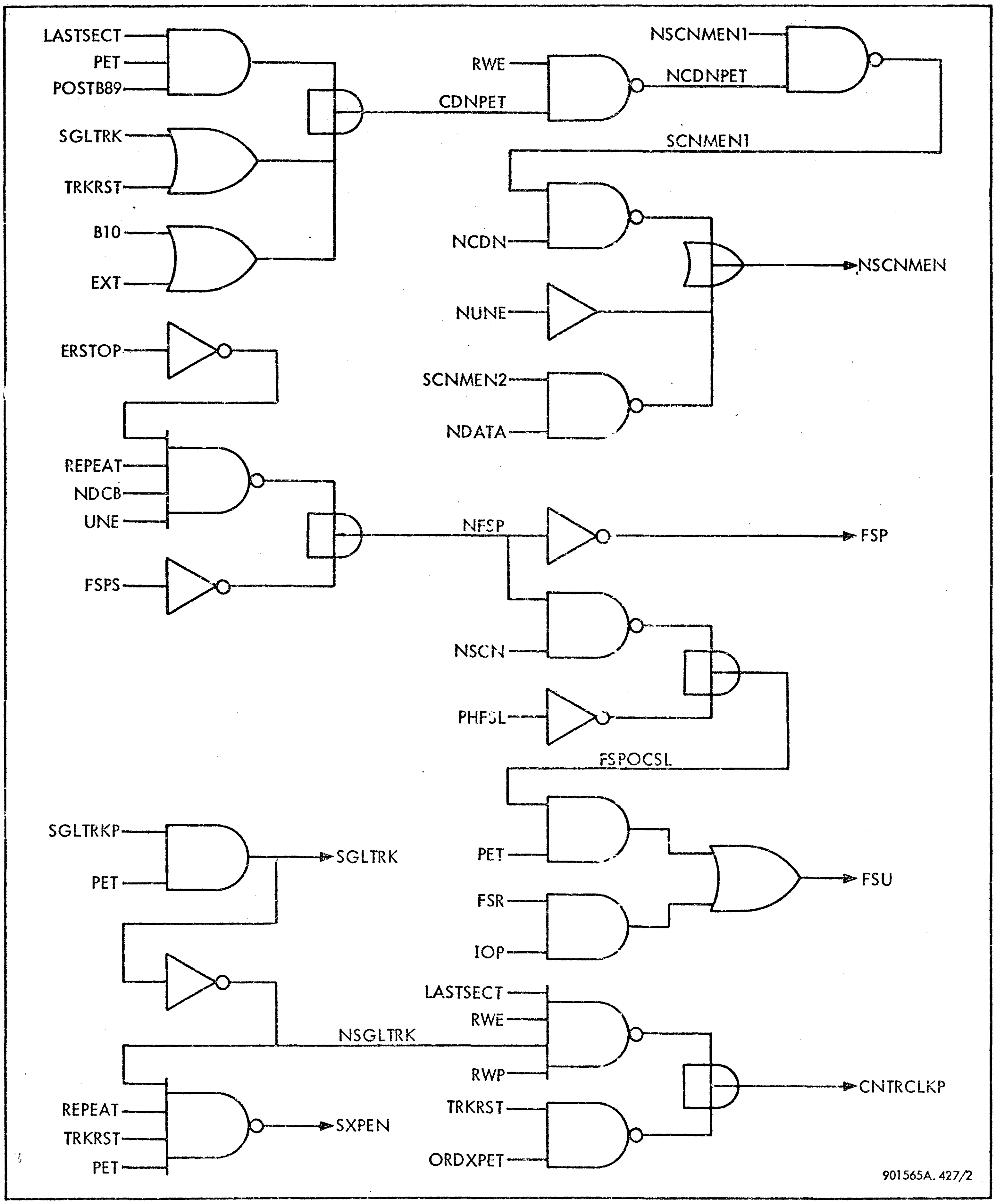


Figure 4-24. PET Interface Circuits, Simplified Logic Diagram (Sheet 2 of 2)

ORD3 = ORDP3A ORDXPET + ...

ORDP3A = ORDP3 ALTORD

ORD4 = ORDP4A ORDXPET + ...

ORDP4A = N(ALTORD NORDP4)

NORDP4 = N(ORDP4 PET)

For the alternate order mode of operation, signal ALTP is true and the PET order code is stored only when flip-flop ALTP is set.

ALTORD = ALT + ...

When ALT is in the reset state, a write order (1 X001) is stored. Flip-flop ALT changes state each time alternate order clock signal ALTCK goes false.

S/ALT = NALT

R/ALT = ...

C/ALT = ALTCK

Clock signal ALTCK is true during phase RSA of each order in service cycle if PET panel signal TRKRST is true.

ALTCK = ALTCKEN ALTP + . . .

ALTCKEN = ORDIN PHRSA TRKRST

Signal TRKRST is true when the PET internal counter state matches the track address and the sector address switch settings on the PET panel. Therefore, after each input/output operation, ALT changes state and alternates a write order with the order encoded on the PET panel switches after all data has been processed.

When signal ALTP is false, ALT is set by the first index pulse and remains in the set state.

ALTCK = NALTP IPR + ...

4-90 COUNT DONE SIMULATION. The address at which an input/output operation begins is established by a single phase seek order, during which a track address and a sector address are loaded. A read order, write order, or check-write order is terminated under control of signal TRKRST, which is generated by a counter in the controller.

CDNPET = LASTSECT PET POSTB89 (TRKRST + ...) (EXT + ...)

Signal TRKRST is true when the state of a PET counter matches a value set in PET panel switches. The counter is incremented by signal CNTRCLKP, which is sent to the PET.

NCNTRCLKP = LASTSECT RWE RWP NSGLTRK + ORDXPET TRKRST

Thus, the counter is incremented as the last sector of a track is processed and is cleared when a new order is stored after TRKRST is true.

4-91 SINGLE TRACK MODE. When the PET commands the single track mode of operation, an order is executed continually on a 12-sector track. For this mode of operation, the sequence of events which cause incrementation of the track address must be inhibited, but incrementation of the sector address must be allowed. (See paragraph 4-70.) Incrementation of the S-register is enabled through D07SET, as in normal operation, but incrementation of the T-register is inhibited by a true SGLTRKP signal.

ND07SET = B11 B12 SGLTRK NBX0 + ND7P15 NBX0

SGLTRK = SGLTRKP PET

That is, after four bits have been processed (B11, B12), the incrementing process is inhibited by forcing D07SET false.

Signal SXPEN, which enables a transfer of data from the P-register to the T-register and S-register, is inhibited by signal SGLTRK. (See figure 4-24.)

A count done signal is generated each time the last sector is detected.

CDNPET = LASTSECT PET POSTB89 (SGLTRK + ...)

Signal PRESET is inhibited if a write order is being executed so that writing is not allowed on alternate revolutions, thereby meeting read/write head duty cycle specifications.

PRESET = RWP NB11 B10 B09 B06 N(ALTYP2 PET SGLTRK WRITE)

4-92 ERROR STOP MODE. When signal REPEAT from the PET is true, the command chaining signal is true, causing repetition of the order set into PET switches.

CCH = N(IOP DA3R)(REPEAT PET + ...)

The function strobe is generated under control of signal ERSTOP from the PET. (See figure 4-24.) After the first function strobe is generated by a true FSPS signal, no function strobe is needed to continue service cycles, provided no unusual end occurs.

FSU = PET NPHFSL (REPEAT NDCB UNE NERSTOP + FSPS)

If signal ERSTOP from the PET is false, signal NERSTOP is true and an unusual end generates a new function strobe.

If signal ERSTOP from the PET is true, signal NERSTOP is false. When an unusual end occurs, DCB is reset as for online operation, and lack of a function strobe causes operation to stop. (The track address has been incremented.)

4-93 PHASE SEQUENCE CHARTS

The phase sequence charts describe the operation of the controller for normal online response to signals from the IOP. The emphasis is on the phase control circuits described in detail in paragraphs 4-20 through 4-35. Information is exchanged between the IOP and the controller as these circuits cycle through a sequence of six phases (FS, FSL, FSZ, RS, RSA, and TO), each of which is defined by a flip-flop.

At certain times during a sequence of the phase control circuit operations, signals are required from circuits asynchronous with the phase control circuits. The three asynchronous timing circuits of the controller are:

a. The TCL delay line, which controls transfer of information between the IOP and the controller

b. The TRL delay line, which controls transfer of data bytes to and from the FAM module

c. The TDT delay line, which controls transfer of data between the controller and the addressed storage unit

Data passing between the IOP and the addressed storage unit is controlled by all three timing circuits during the transfer process. Therefore, although details of operation of asynchronous circuits are not defined in the phase sequence charts, their relation to the operation of the phase control circuits cannot be ignored. Signals originating outside the phase control circuits, either in the IOP or in asynchronous circuits of the controller, are identified in the phase sequence charts.

For normal online operation, the controller is initially in the ready automatic state. When in this state, the controller responds to any IOP command (AIO, HIO, SIO, TIO, or TDV) by passing through phases FS, FSZ, and FSL, and then returning to phase FS. If the command is an SIO and if the SIO is accepted, the controller enters the busy automatic state and remains in this state until completion of one or more input/output operations or until an error occurs. Upon entering the busy automatic state, the controller requests an order out service cycle, during which the controller stores the order transmitted from the IOP. After the order is stored, the controller will request a sequence of data out service cycles or a sequence of data in service cycles. If no error occurs during these service cycles, a signal from the IOP indicates a count done after all data has been transferred, after which the controller requests an order in service cycle. During the order in service cycle, information is sent to the IOP. Following the order in service cycle, the controller may return to the ready automatic state or may start a new order in service cycle, as determined by terminal order information.

Each of the four service cycles (order out, data out, data in, and order in) is identified by the states of two flip-flops. For any service cycle, the controller passes through phases FS, FSZ, and FSL, followed by some sequence of phases RS and RSA, followed by phase TO. During any TO phase, the controller may receive information from the IOP which indicates than an interrupt has occurred, that all data has been transferred, or that the IOP has commanded an unusual end. If an error is detected by circuits of the controller, an order in service cycle will be requested during the next TO phase in sequence. During phase TO of an order in service cycle, the controller may receive a command chaining signal. This signal causes the controller to start a new order out service cycle, rather than return to the ready automatic state.

Therefore, operation of the controller consists of passing from the ready automatic state to the busy automatic state in response to IOP signals, processing data, and returning to the ready automatic state. For execution of seek orders, write orders, and checkwrite orders, data is transferred from the IOP in a succession of data out service cycles. For execution of sense orders or read orders, data is transferred to the IOP in a succession of data in service cycles. Each complete input/output operation begins with an order out service cycle and ends with an order in service cycle.

4-94 IOP Command Sequences

In response to an IOP command, the controller provides information on function response lines /FR0/ through /FR7/ and on data or order lines /DOR/ and /IOR. The information provided and the operations which take place within the controller depend upon the type of IOP command, as indicated in tables 4-8 through 4-12.

4-95 Order Out Sequence

Each input/output operation begins with an order out service cycle. An order out service cycle follows an accepted SIO command or an order in service cycle during which a command chaining signal is accepted from the IOP. During an order out service cycle, an order is read from IOP data lines /DA3/ through /DA7/ and stored in the order register (ORD0 through ORD4), as indicated in table 4-13. If the order indicates seek, write, or checkwrite, subsequent service cycles will be data out service cycles; if the order is sense or read, subsequent service cycles will be data in service cycles. Thus, order out service cycles normally begin with the (DATA, IN) flip-flops in state (0, 0) and end with these flip-flops in state (1, 0) or (1, 1). If the order is one of the illegal codes or if it is a write order which addresses a write-protected track, an error will be detected. The (DATA, IN) flip-flops will be placed in the (0, 1) state, and the error will be reported during the order in service cycle which follows.

Table 4-8. AIO Command, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
Interrupt Pending	Raise interrupt call line ICD when CIL set	ICD = LIL LIL = NAIOR CIL INC + AIOR INI LIL NRSTR	CIL set by terminal order and remains in set state until AIO response received from IOP
FS	Enable TCL delay line	DCL = CYCLE/C DCLSTART1 + ... CYCLE/C = IOP CYCSET + ... DCLSTART1 = FSU PHFS AIOC + ... AIOC = AIOM AIOR AVIR + ... AIOM = NHPIL LIL + ...	CYCSET latched true. Delay line input when AIOR signal received from IOP (only for device controller with LIL true)
	Reset CIL	R/CIL = CILRST CILRST = AIOC + ... C/CIL = NTCS000	
	Set NPHFS	S/NPHFS = PHFS C/NPHFS = TCS100-3	End phase FS
	Set PHFSZ	S/PHFSZ = PHFS C/PHFSZ = TCS100-3	Enter phase FSZ
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Reset PHFSZ	R/PHFSZ = ... C/PHFSZ = TCS100-3	End phase FSZ
		S/PHFSL = PHFSZ C/PHFSL = TCS100-3	Enter phase FSL OPER may be set, but no significance for AIO
FSL	Enable TCL delay line	DCL = CYCLE/C DCLSTART3 + ... DCLSTART3 = NFSU PHFSL + ...	TCL delay line enabled when function strobe false
	Enable function response signals	FR0D = BSYC SWA0 + ...	(FR0D-FR3D) contain device controller address

(Continued)

Figure 4-8. AIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)		BSYC = AVIR AIOR AIOM PHFSL-1 + ...	
		FR1D = BSYC SWA1 + ...	
		FR2D = BSYC SWA2 + ...	
		FR3D = BSYC SWA3 + ...	
		FR4D = BSYC GND + ...	FR4D always false
		FR5D = BSYC U0 + ...	(FR5D-FR7D) contain device address
		FR6D = BSYC U1 + ...	
		FR7D = BSYC U2 + ...	
	Enable status signals	DA0 = O00 + ...	RER, SUN, WPV indicate cause of interrupt
		O00 = OXAIOST RER + ...	
		OXAIOST = AIOC FSU	
		DA2 = O02 + ...	
		O02 = OXAIOST SUN + ...	
		DA3 = O03 + ...	
		O03 = OXAIOST WPV + ...	
	Enable condition code signals (IORD, DORD)	IORD = PHFSL IORDEN + ...	IORD true if all status signals false. Defines normal I/O interrupt
		IORDEN = NIORDEN1 + ...	
		NIORDEN1 = AIOC NFAULT + ...	
		NFAULT = NRER NSUN NWPV	
		DORD = DORDEN PHFSL + ...	DORD always true
		DORDEN = AIOC + ...	
	Reset PHFSL	R/PHFSL = ...	End phase FSL
		C/PHFSL = TCS100-3	
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS (service connect flip-flop FSC not in set state)
		PHFSET = NFSCU PHFSL-1	
		FSCU = FSC IOP + ...	
		C/NPHFS = TCS100-3	

Table 4-9. HIO Command, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
FS	CPU processes HIO instruction, and IOP generates true HIOR function indicator signal and true FSR function strobe		
	Enable TCL delay line	DCL = CYCLE/C DCLSTART1 + ...	
		CYCLE/C = CYCSET IOP + ...	CYCSET latched true. IOP true unless DC is offline
		DCLSTART1 = FSU PHFS TTSHU DCAU + ...	
		FSU = FSR IOP + ...	
		TTSHU = TTSH IOP + ...	
		TTSH = HIOR + ...	
		DCAU = DCA IOP + ...	DCA true if (SWA0-SWA3) matches (DA0R-DA3R)
	Reset	R/OPER = PHFS	Prepare to sample signal DVTR during phase FSZ
		C/OPER = NTCS080	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	Enter phase FSZ
		C/PHFSZ = TCS100-3	
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Sample DVTR signal from addressed selection unit	S/OPER = DVTR OPERSET	Set OPER if DVTR true, indicating RAD is operating
		OPERSET = TTSHU PHFSZ	
		C/OPER = NTCS080	
	Reset PHFSZ	R/PHFSZ = ...	End phase FSZ
		C/PHFSZ = TCS100-3	
	Set PHFSL	S/PHFSL = PHFSZ	Enter phase FSL
		C/PHFSL = TCS100-3	
FSL	Enable TCL delay line	DCL = CYCLE/C DCLSTART3 + ...	TCL delay line enabled at end of function strobe

(Continued)

Figure 4-9. HIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	Enable function response signals	FR0D = BFSD TSH CIL + ...	FR0D true if interrupt pending (CIL)
		BFSD = FSLD	
	FR1D FR2D	FSLD = TTSH DCA PHFSL-1	
	0 0 Device ready	PHFSL-1 = PHFSL	
	1 1 Device busy	FR1D = BFSD TSH DVBSY + ...	
	0 1 Device not operational	DVBSY = DCB DVSEL	DVSEL true if (U0-U2) matches (DA5R-DA7R), indicating device selected
		FR2D = BFSD TSH STSH02 + ...	
		STSH02 = DVBSY + NOPER	
		FR3D = BFSD TSH DVTR + ...	Device test (DVT)
	FR5D FR6D	FR4D = BFSD TSH UNE + ...	Unusual end (UNE)
	0 0 Device controller ready	FR5D = BFSD TSH DCB + ...	
		FR6D = BFSD TSH DCB + ...	
	1 1 Device controller busy	FR7D = BFSD TSH GND + ...	FR7D always false
	Enable condition code signals (IORD, DORD)	IORD = IORDEN PHFSL + ...	IORD true if addressed device is not busy (NDVBSY)
		IORDEN = NIORDEN1 + ...	
		NIORDEN1 = NDVBSY HIOU + ...	
		DORD = DORDEN PHFSL + ...	DORD true if addressed device is operating (OPER)
		DORDEN = OPER + ...	
	Clear flip-flops CER, PER, RER, SCR, SUN, and WPV	E/CER = RESET	
		RESET = DVSEL HIOU PHFSL + ...	DVSEL true if (U0-U2) matches (DA5R-DA7R)
		HIOU = HIOR IOP + ...	
		E/PER = RESET	
		E/RER = RESET	
		E/SCR = RESET	
		E/SUN = RESET	
	Reset DCB	E/WPV = RESET	

Table 4-9. HIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	Reset DCB	R/DCB = DCBRST DCBRST = RESET + ... C/DCB = NTCS080	
	Clear flip-flops DCE, BK0, BK1, DAR, DATA, DSE, DSL, EDISET3, IN, INL, ORD0, PHRS, PHRSA, PHTO, PRE, RWE, RWP, SCN, SEN, TSE		Flip-flops are direct reset by equation of form E/XXXX = NDCB
	Reset PHFSL	R/PHFSL = ... C/PHFSL = TCS100-3	End phase FSL
		R/NPHFS = PHFSET PHFSET = NFSCU PHFSL-1 FSCU = FSC IOP + ... C/NPHFS = TCS100-2	Enter phase FS (flip-flop FSC can be set only by SIO command)

Table 4-10. SIO Command, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
FS	CPU processes SIO instruction, and IOP generates true function indicator signal SIOR and function strobe signal FSR		
	Enable TCL delay line	DCL = CYCLE/C DCLSTART1 + ... CYCLE/C = CYCSET IOP + ... DCLSTART1 = FSU PHFS TTSHU DCAU + ... FSU = FSR IOP + ... DCAU = DCA IOP + ... TTSHU = TTSH IOP + ... TTSH = SIOR + ...	CYCSET latched true. DCA true if (SWA0-SWA3) matches (DA0R-DA3R). IOP true unless DC is offline
	Reset OPER	R/OPER = PHFS C/OPER = NTCS080	Prepare to sample signal DVTR during phase FSZ

(Continued)

Table 4-10. SIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FS (Cont.)	Set NPHFS	S/NPHFS = PHFS C/NPHFS = TCS100-3	End phase FS
	Set PHFSZ	S/PHFSZ = PHFS C/PHFSZ = TCS100-3	Enter phase FSZ
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Sample DVTR signal from selection unit	S/OPER = DVTR OPERSET OPERSET = TTSHU PHFSZ C/OPER = NTCS080	Set OPER if DVTR true, indicating RAD is operating
	Reset PHFSZ	R/PHFSZ = ... C/PHFSZ = TCS100-3	End phase FSZ
	Set PHFSL	S/PHFSL = PHFSZ C/PHFSL = TCS100-3	Enter phase FSL
	Enable TCL delay line	DCL = CYCLE/C DCLSTART3 + ... DCLSTART3 = PHFSL NFSU + ...	TCL delay line enabled at end of function strobe FSR
FSL	Enable function response signals	FROD = BFSD TSH CIL + ... BFSD = FSLD FSLD = TTSH DCA PHFSL-1 + ... TTSH = SIOR + ... TSH = DCA (SIOR + ...)	FROD true if interrupt pending (CIL)
	FR1D FR2D 0 0 Device ready 1 1 Device busy 0 1 Device not operational	FR1D = BFSD TSH DVBSY + ... DVBSY = DCB DVSEL FR2D = BFSD TSH STSH02 + ... STSH02 = DVBSY + NOPER	

(Continued)

Table 4-10. SIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)		FR3D = BFSD TSH DVTR	FR3D true if device test (DVTR) true;
		FR4D = BFSD TSH UNE + ...	FR4D true if unusual end (UNE) true
	<u>FR5D</u> <u>FR6D</u>	FR5D = BFSD TSH DCB + ...	
	0 0 Device controller ready	FR6D = BFSD TSH DCB + ...	
	1 1 Device controller busy	FR7D = BFSD TSH GND + ...	FR7D always false
	Enable condition code signals (IORD, DORD)	IORD = PHFSL IORDEN + ...	
	<u>IORD</u> <u>DORD</u>	IORDEN = DCBSET + ...	
		DCBSET = OPER SIOPOSS PHFSL	
	0 0 Not operational	SIOPOSS = NCIL NDCB SIOU	
	0 1 Interrupt pending or busy	DORD = PHFSL DORDEN + ...	
	1 1 SIO accepted	DORDEN = OPER + ...	
	If SIO accepted, set DCB	S/DCB = DCBSET	
		C/DCB = NTCS080	
	If DCBSET, clear flip-flops CER, PER, RER, SCR, SUN, and WPV	E/CER = RESET	
		RESET = DCBSET + ...	
		E/PER = RESET	
		E/RER = RESET	
		E/SCR = RESET	
		E/SUN = RESET	
		E/WPV = RESET	
	If DCBSET, store device address in (U0-U2) at end of phase FSL	S/U0 = SU0D	Device address retained in (U0-U2) during I/O operation
		SU0D = DA5R IOP + ...	
		SU1 = SU1D	
		SU1D = DA6R IOP + ...	
		S/U2 = DA7R IOP + ...	
		(C/U0-C/U2) = DCBSET	

(Continued)

Table 4-10. SIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	Reset PHFSL	R/PHFSL = ...	End phase FSL
		C/PHFSL = TCS100-3	
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS
		PHFSET = NFSCU PHFSL-1 + ...	
		C/NPHFS = TCS100-3	

Table 4-11. TDV Command, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
FS	CPU processes TDV instruction, and IOP generates true TDVR function indicator signal and true FSR function strobe.		
	Enable TCL delay line	DCL = CYCLE/C DCLSTART1 + ...	CYCSET latched true. IOP true unless DC is offline. DCA true if (SWA0-SWA3) matches (DA0R-DA3R)
		CYCLE/C = CYCSET IOP + ...	
		DCLSTART1 = FSU PHFS TTSHU DCAU + ...	
		FSU = FSR IOP + ...	
		DCAU = DCA IOP + ...	
		TTSHU = IOP TTSH + ...	
		TTSH = TDVR + ...	
	Reset OPER	R/OPER = PHFS	Prepare to sample signal DVTR during phase FSZ
		C/OPER = NTCS030	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	Enter phase FSZ
		C/PHFSZ = TCS100-3	
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Sample DVTR signal from selection unit	S/OPER = DVTR OPERSET	Set OPER if DVTR true, indicating RAD is operating
		OPERSET = TTSHU PHFSZ	

(Continued)

Table 4-11. TDV Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved		Comments
FSZ (Cont.)		C/OPER	= NTCS080	
	Reset PHFSZ	R/PHFSZ	= ...	End phase FSZ
		C/PHFSZ	= TCS100-3	
	Set PHFSL	S/PHFSL	= PHFSZ	Enter phase FSL
		C/PHFSL	= TCS100-3	
FSL	Enable TCL delay line	DCL	= CYCLE/C DCLSTART3 + ...	Delay line enabled at end of function strobe
		DCLSTART3	= PHFSL NFSU + ...	
	Enable function response signals	FROD	= (TDVR DCA FSD) RER + ...	FROD true for rate error
		(TDVR DCA FSD)	= DCA FSLD TDVR	
		FSLD	= PHFSL-1 TTSH DCA + ...	
		PHFSL-1	= PHFSL	
		FR2D	= (TDVR DCA FSD) SUN + ...	FR2D true if sector unavailable
		FR3D	= (TDVR DCA FSD) WPV + ...	FR3D true if write protection violation
	Enable condition code signals (IORD, DORD)	IORD	= PHFSL IORDEN + ...	IORD true if none of the error flip-flops in set state
		IORDEN	= NIORDEN1 + ...	
		NIORDEN1	= TDVU NFAULT	
		NFAULT	= NRER NSUN NWPV	
		DORD	= DORDEN PHFSL + ...	DORD true if device is operating
		DORDEN	= OPER + ...	
	Reset PHFSL	R/PHFSL	= ...	End phase PHFSL
		C/PHFSL	= TCS100-3	
	Reset NPHFS	R/NPHFS	= PHFSET	Enter phase PHFS if service connect flip-flop FSC not in set state
		PHFSET	= NFSCU PHFSL-1	
		FSCU	= FSC IOP + ...	
		C/NPHFS	= TCS100-3	

Table 4-12. TIO Command, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
FS	CPU processes TIO instruction, and IOP generates true TIOR signal and FSR signal		
	Enable TCL delay line	DCL = CYCLE/C DCLSTART1 + . . .	CYCSET latched true. IOP true unless DC is offline. DCA true if (SWA0-SWA3) matches (DA0R-DA3R)
		CYCLE/C = CYCSET IOP + . . .	
		DCLSTART1 = FSU PHFS TTSHU DCAU + . . .	
		FSU = FSR IOP + . . .	
		TTSHU = TTSH IOP + . . .	
		DCAU = DCA IOP + . . .	
		TTSH = TIOR + . . .	
	Reset OPER	R/OPER = PHFS	Prepare to sample signal DVTR during phase FSZ
		C/OPER = NTCS080	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	Enter phase FSZ
		C/PHFSZ = TCS100-3	
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Sample DVTR signal from addressed selection unit	S/OPER = DVTR OPERSET	Set OPER if DVTR true, indicating RAD is operating
		OPERSET = TTSHU PHFSZ	
		C/OPER = NTCS080	
	Reset PHFSZ	R/PHFSZ = ...	End phase FSZ
		C/PHFSZ = TCS100-3	
	Set PHFSL	S/PHFSL = PHFSZ	Enter phase FSL
		C/PHFSL = TCS100-3	
FSL	Enable TCL delay line	DCL = CYCLE/C DCLSTART3 + ...	TCL delay line enabled at end of function strobe
		DCLSTART3 = PHFSL NFSU + ...	

(Continued)

Table 4-12. TIO Command, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved		Comments
FSL (Cont.)	Enable function response signals	FROD	= BFSD TSH CIL + . . .	FROD true if interrupt pending (CIL)
		BFSD	= FSLD	
		FSLD	= TTSH DCA PHFSL-1	
		PHFSL-1	= PHFSL	
	FR1D FR2D			
	0 0 Device ready	FR1D	= BFSD TSH DVBSY + . . .	
	1 1 Device busy	DVBSY	= DCB DVSEL	
	0 1 Device not operational	FR2D	= BFSD TSH STSH02 + . . .	
		STSH02	= DVBSY + NOPER	
		FR3D	= BFSD TSH DVTR + . . .	Device test (DVTR)
		FR4D	= BFSD TSH UNE + . . .	Unusual end (UNE)
	FR5D FR6D	FR5D	= BFSD TSH DCB + . . .	
	0 0 Device controller ready	FR6D	= BFSD TSH DCB + . . .	
	1 1 Device controller busy			
		FR7D	= BFSD TSH GND + . . .	
	Enable condition code signals	IORD	= PHFSL IORDEN + . . .	IORD true if no interrupt, not busy, and device operating
		IORDEN	= NIORDEN1 + . . .	
	IORD DORD	NIORDEN1	= NCIL NDCB OPER TIOU + . . .	
	1 1 Ready for SIO			
	0 0 Device not operational	TIOU	= TIOR IOP + . . .	
		DORD	= DORDEN PHFSL + . . .	
	0 1 Interrupt pending or DC busy	DORDEN	= OPER + . . .	DORD true if device operating
	Reset PHFSL	R/PHFSL	= . . .	End phase FSL
		C/PHFSL	= TCS100-3	
	Reset NPHFS	R/NPHFS	= PHFSET	Enter phase FS
		PHFSET	= NFSCU PHFSL-1	
		FSCU	= FSC IOP + . . .	
		C/NPHFS	= TCS100-3	

Table 4-13. Order Out Service Cycle, Phase Sequence Chart

Phase	Function Performed	Signals Involved		Comments
	Device controller busy flip-flop DCB has been set by previously accepted SIO. Phase FS is entered following SIO or following order inservice cycle in which command chaining signal was received from IOP	ORDOUT	= NDATA NIN	Flip-flop NPHFS is reset following SIO or order in service cycle
FS	Direct set service call flip-flop SCN	M/SCN	= PHFS DCB CYCLE/C N(NSCNMEN)	CYCSET latched true
		CYCLE/C	= CYCSET IOP + ...	IOP true when controller is online
		N(NSCNMEN)	= NDATA NRWE NWCHW + ...	
	Raise service call line SCD	SCD	= LSL	Service call line held true until IOP responds with ASCR and FSR
		LSL	= NASCR SCN INC + ...	
	Start TCL delay line when ASCR and FSR true	DCL	= CYCLE/C DCLSTART1 + ...	
		DCLSTART1	= PHFS DCB BSYCU + ...	
		BSYCU	= BSYC IOP + ...	
		BSYC	= ASCM ASCR AVIR FSR + ...	
	Reset flip-flop CDN	R/CDN	= ORDOUT	CDN set during phase TO of last data transfer of previous order
		ORDOUT	= NDATA NIN	
		C/CDN	= NTCS000	
	Enable function response signals FR0D through FR7D	FR0D	= BSYC SWA0 + ...	(FR0D-FR3D) encode device controller address
		FR1D	= BSYC SWA1 + ...	
		FR2D	= BSYC SWA2 + ...	
		FR3D	= BSYC SWA3 + ...	
		FR4D	= BSYC GRD + ...	FR4D always false
		FR5D	= BSYC U0 + ...	(FR5D-FR7D) encode device address
		FR6D	= BSYC U1 + ...	
		FR7D	= BSYC U2 + ...	

(Continued)

Table 4-13. Order Out Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FS (Cont.)	Set service connect flip-flop FSC as function strobe FSR goes false	S/FSC = ASCB	FSC must be set before RSD raised in phase FSL
		ASCB = ASCM ASCR AVIR FSR (delayed NFSC)	
		C/FSC = NFSC FSR + ...	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	Enter phase FSZ
		C/PHFSZ = TCS100-3	
FSZ	Enable TCL delay line	DCL = CYCLE/C PHFSZ + ...	Phase FSZ functions not significant for order out service cycle
	Reset PHFSZ	R/PHFSZ = ...	End phase FSZ
	Set PHFSL	S/PHFSL = PHFSZ	Enter phase FSL
		C/PHFSL = TCS100-3	
FSL	Raise request strobe signal RSD	RSD = FSC NRSAR (FSCU RSD + NPHRSA RSET + ...)	RSD latches until request strobe acknowledge signal RSAR is true
		RSET = PHFSL NIN + ...	
		FSCU = FSC IOP + ...	
	Enable data or order signals, request order out service cycle	IORD = FSC NIN + ...	(DATA, IN) flip-flops in (0, 0) state at start of I/O or at end of order in service cycle
		DORD = FSC NDATA + ...	
	Start TCL delay line	DCL = CYCLE/C DCLSTART3 + ...	TCL delay line started
		DCLSTART3 = PHFSL NFSU + ...	
		FSU = FSR IOP + ...	
	Reset service call flip-flop SCN	R/SCN = SCNRST	SCN reset to prevent service call unless required
		SCNRST = PHFSL + ...	
		C/SCN = TCS100-3	
	Reset PHFSL	R/PHFSL = ...	End phase FSL

(Continued)

Table 4-13. Order Out Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	Set PHRSA	S/PHRSA = PHRSASET FSCU	Enter phase RSA
		PHRSASET = PHFSL NIN + ...	
		C/PHRSA = TCS100-3	
RSA	Wait for request strobe acknowledge signal RSAR from IOP		
	Start TCL delay line	DCL = CYCLE/C PHRSA RSAU + ...	
		RSAU = RSAR IOP + ...	
	Direct set SCR	M/SCR = PHRSAOO	Preset for control of FAM circuits
	Store order code	S/ORD0 = DA3R IOP	Order code retained until order has been executed
	(DA3R-DA7R)→(ORD0-ORD4)	C/ORD0 = ORDXIOP	
	(Order register bits) 0 1 2 3 4	ORDXIOP = IOP PHRSAOO TCS000-3	
	(IOP data lines) 3 4 5 6 7	PHRSAOO = ORDOUT PHRSA	
	Write order X X 0 0 1	ORDOUT = NDATA NIN	
	Read record order 0 X X 1 0	ORD1 = DA4R ORDXIOP + ...	
	Read sector order 1 X X 1 0	ORD2 = DA5R ORDXIOP + ...	
	Seek order X X X 1 1	ORD3 = DA6R ORDXIOP + ...	
	Sense order X 0 1 0 0	ORD4 = DA7R ORDXIOP + ...	
	Checkwrite order X X 1 0 1		
	Preset byte counter to (1, 1)	M/BK0 = BKX1	Preset required for multiple-byte IOP interface operations
		BKX1 = PHRSAOO + ...	
		M/BK1 = BKX1	
	Direct set flip-flop SCR	M/SCR = PHRSAOO	SCR and RK-counter preset for control of FAM circuits
	Preset RK-counter	(S/RK0-S/RK3) = ORDOUT	
		M/RK4 = PHRSAOO	
	Preset JP-register to 1111	(JP0-JP3) = PHRSAOO + ...	Presets determine FAM location for first FAM read cycle and first FAM write cycle
	Preset KP-register to 1111	(KP0-KP3) = PHRSAOO + ...	

(Continued)

Table 4-13. Order Out Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RSA (Cont.)	Reset PHRSA	R/PHRSA = ...	End phase RSA
	Set PHRS	S/PHRS = PHRSET FSCU PHRSET = PHRSA + ... C/PHRS = TCS100-3	Enter phase RS
RS	Start TCL delay line as RSAR goes false	DCL = CYCLE/C DCLSTART3 + ... DCLSTART3 = PHRS NDATA NRSAU + ...	
	Raise request strobe line RSD	RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)	
	Reset PHRS	R/PHRS = ...	End phase RS
	Set PHTO	S/PHTO = PHRS ED	Enter phase TO
		ED = EDSET TCS000-2 + ED FSCU + ...	End data signal set internally and latched
		EDI = EDI FSCU + EDSET1 NPHRSA + ... EDISET1 = NDATA + ... C/PHTO = TCS100-3	
TO	Start TCL delay line when request strobe acknowledge signal RSAR true	DCL = CYCLE/C DCLSTART1 + ... DCLSTART1 = PHTO RSAU + ...	
	Set DATA	S/DATA = DATASET NORDIN DATASET = NSKSBK NCDN NCDNPET NUNE ORDIN = NDATA IN C/DATA = PHFSTOD TCS100-3 PHFSTOD = PHTO + ...	DATA set regardless of order code stored
	If read order or sense order, set IN	S/IN = INSET NORDIN INSET = NORD4 + ... C/IN = PHFSTOD TCS100-3	IN set for orders requiring data transfer to computer through IOP

(Continued)

Table 4-13. Order Out Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
TO (Cont.)	Reset PHTO	R/PHTO = ...	End phase TO
	Reset NPHFS	R/NPHFS = PHFSET PHFSET = PHTO + ... C/NPHFS = TCS100-3	Enter phase FS
	Terminal order operations		Refer to table 4-19 for terminal order operations resulting in other than execution of order

4-96 Sense Order Sequence

The sense order is executed if the sense order code (0 0100) is stored in the order register during an order out service cycle. During execution of a sense order, three bytes of data are transferred to the O-register for transfer to the IOP. The first byte contains seven bits from the selection unit of the track address from the T-register and the track protect bit. The second byte contains four bits of the track address, and the four-bit sector address from the S-register. The third byte contains the four-bit address of the sector currently under the read/write heads of the selection unit. Equations controlling execution of the order are listed in table 4-14; a timing diagram is provided in figure 4-25.

Sense order data is transmitted one byte at a time regardless of the byte width of the IOP interface. The first byte is stored in the O-register as request strobe signal RSD is raised. The IOP delays, reads the data from the O-register, then delays before raising request strobe acknowledge signal RSAR. The second and third bytes are transferred through the K-register to the O-register. Transfer from the T-register and S-register to the K-register and from the K-register to the O-register is controlled by signals generated within the controller as the order is executed. The IOP accepts data from the O-register while signal RSD is true.

Table 4-14. Sense Order, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
	Order out service cycle follows accepted SIO or command chaining terminal order, after which:		For SIO sequence, refer to table 4-10
	a. (DATA, IN) in state (1, 1)	DATAIN = DATA IN	
	b. (BK0, BK1) in state (1, 1)	BKZZ = BK0 BK1	
	c. (ORD0-ORD4) store (0 0100)	SENSE = ORD2 NORD3 NORD4	For order out service cycle sequence, refer to table 4-13
	d. DCB in set state		
	e. FSC in set state		
	f. SCN in set state		

(Continued)

Table 4-14. Sense Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
	During preliminary phases (FS, FSZ, FSL) of data in service cycle, SEN is set, EP RAD controller address and EP RAD storage unit address are placed on function response lines (FR0D-FR7D), and (DORD, IORD) signals indicate data in service cycle request	IORD = FSC NIN + ... DORD = FSC NDATA + ... S/SEN = SENSE PXS PXS = TSE NRWP	
	At end of preliminary operations, enter phase RS	R/PHFSL = ...	Exit phase FSL
		S/PHRS = FSCU PHRSET PHRSET = PHFSL IN + ...	Enter phase RS
RS	(TRPR)→(O00)	OXSENSE1 = SENSE OXKEN BKZZ	TRPR is track protect bit from selection unit
	(T00-T06)→(O01-O07)	OXKEN = DATAIN NED PHRS	
	Start TCL delay line	DCL = CYCLE/C DCLSTART2 NRSAU + ... DCLSTART2 = PHRS SEKSEND + ... SEKSEND = SENSE NPHRSAOO + ... PHRSAOO = PHRSA ORDOUT	
	Reset flip-flop PHRS	R/PHRS = ...	Exit phase RS
	Set flip-flop PHRSA	S/PHRSA = FSCU PHRSASET PHRSASET = PHRSNED PHRSNED = PHRS NED	Enter phase RSA
	Raise request strobe signal RSD	RSD = FSC NRSAR (PHRS TCS000-2 + ...	Contents of O-register read into memory while RSD true
RSA	Decrement byte counter (BK0, BK1) to (1, 0)	NBKCK = PHRSA SEKSEND TCS000-3 + ... SEKSEND = SENSE NPHRSAOO + ... PHRSAOO = PHRSA ORDOUT BKZW = BK0 NBK1	

(Continued)

Table 4-14. Sense Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RSA (Cont.)	(T07-T10)→(K00-K03)	KXSENSE1 = SENSE BKZW	Prepare for transfer to O-register in phase RS
	(S00-S03)→(K04-K07)		
	Start TCL delay line	DCL = CYCLE/C PHRSA RSAU + ...	
	Reset flip-flop PHRSA	R/PHRSA = ...	Exit phase RSA
	Set flip-flop PHRS	S/PHRS = FSCU PHRSET	Enter phase RS
		PHRSET = PHRSA + ...	
RS	(K00-K07)→(O00-O07)	OXK = OXKEN TCS000-2	
		OXKEN = DATAIN NED PHRS	
	Raise request strobe signal RSD	RSD = FSC NRSAR (PHRS TCS000-2 + ...)	Contents of O-register read into memory while RSD true
	Start TCL delay line	DCL = CYCLE/C DCLSTART2 NRSAU + ...	
		DCLSTART2 = PHRS SEKSEND + ...	
		SEKSEND = SENSE NPHRSAOO + ...	
		PHRSAOO = PHRSA ORDOUT	
	Reset flip-flop PHRS	R/PHRS = ...	Exit phase RS
	Set flip-flop PHRSA	S/PHRSA = FSCU PHRSASET	Enter phase RSA
		PHRSASET = PHRSNED + ...	
		PHRSNED = PHRS NED	
RSA	Start TCL delay line	DCL = CYCLE/C PHRSA RSAU + ...	
	Decrement byte counter (BK0, BK1) to (0, 1)	NBKCK = PHRSA SEKSEND TCS000-3	
		SEKSEND = SENSE NPHRSAOO + ...	
		PHRSAOO = PHRSA ORDOUT	
		BKWZ = NBK0 BK1	
	(AN0R-AN3R)→(K04-K07)	KXSENSE2 = SENSE BKWZ	Prepare for transfer to O-register in phase RS

(Continued)

Table 4-14. Sense Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved		Comments
RSA (Cont.)	Reset flip-flop PHRSA	R/PHRSA	= ...	Exit phase RSA
	Set flip-flop PHRS	S/PHRS	= FSCU PHRSET	Enter phase RS
		PHRSET	= PHRSA + ...	
RS	Raise request strobe signal RSD	RSD	= FSC NRSAR (PHRS TCS000-2 + ...)	Contents of O-register read into memory while RSD true
	(K00-K07)→(O00-O07)	OXK	= OXKEN TCS000-2	
		OXKEN	= DATAIN NED PHRS	
	Raise end data signal ED internally	EDD	= EDI FSC	
		EDI	= EDISET1 NPHRSA + EDI FSCU + ...	
		EDISET1	= SENSE BKWZ + ...	
	Start TCL delay line	DCL	= CYCLE/C DCLSTART2 NRSAU + ...	
		DCLSTART2	= PHRS SEKSEND + ...	
		SEKSEND	= SENSE NPHRSAOO + ...	
		PHRSAOO	= PHRSA ORDOUT	
	Reset flip-flop PHRS	R/PHRS	= ...	Exit phase RS
	Set flip-flop PHTO	S/PHTO	= PHRS ED	Enter phase TO
TO	Terminal order operations			See table 4-19

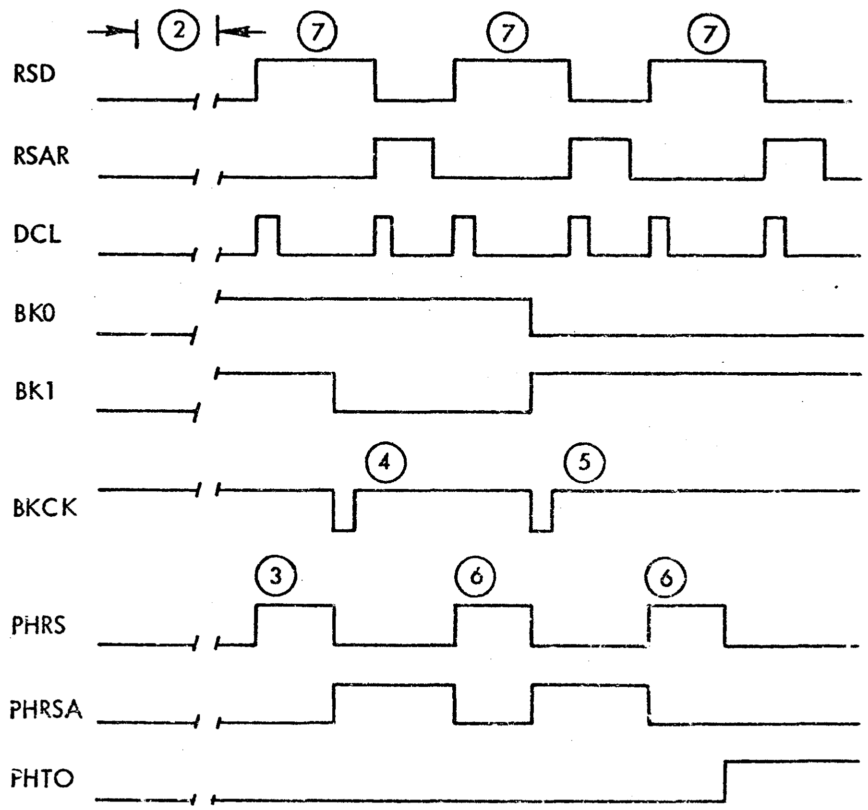
4-97 Seek Order Sequence

The seek order is executed if the seek order code (0 0011) is stored in the order register during an order out service cycle. During execution of a seek order, two bytes of data are accepted on the IOP data lines and are stored in registers of the controller. The first byte contains eight bits of the track address, which are stored in the T-register (three bits are not used). The second byte contains four additional bits of the track address, which are stored in the T-register, and the four-bit sector address, which is stored in the S-register. Equations controlling execution of the order are listed in table 4-15; a timing diagram is provided in figure 4-26.

Seek order data is transmitted one byte at a time, regardless of the byte width of the IOP interface. After the controller raises the request strobe signal RSD, the IOP delays, places output data on the data lines, then delays again before raising the request strobe acknowledge signal RSAR. The first byte is accepted into the I-register and is transferred to the J-register before the second byte is requested from the IOP. Transfer from the J-register to either the T-register or the S-register is controlled by signals generated within the controller as the order is executed.

4-98 Write Order Sequence

If a write order (X X001) is stored in the order register during an order out service cycle, the sequence outlined in table 4-16 follows. During execution of a write order, a sequence of data out service cycles is requested by the controller. During each data out service cycle, data bytes are accepted from the IOP, stored temporarily in registers of



NOTES:

1. NO TIME SCALE; SEQUENCE OF EVENTS ONLY
2. PRELIMINARY OPERATIONS: ORDER OUT SERVICE CYCLE AND PHASES FS, FSZ, FSL, OF DATA IN SERVICE CYCLE
3. (TRPR) ⟶ (O00)
(T00 - T06) ⟶ (O01-O07) } FIRST BYTE
4. (T07 - T10) ⟶ (K00 - K03)
(S00 - S03) ⟶ (K04 - K07) } SECOND BYTE
5. (AN0R-AN3R) ⟶ (K04 - K07) THIRD BYTE
6. (K00 - K07) ⟶ (O00-O07)
7. O-REGISTER READ WHILE RSD TRUE

901565A. 412

Figure 4-25. Data Transfer During Sense Order, Timing Diagram

Table 4-15. Seek Order, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
	Order out service cycle follows accepted SIO or command chaining terminal order, after which:		For SIO sequence, refer to table 4-10. For order out service cycle sequence, refer to table 4-13
	a. (DATA, IN) in state (1, 0)	DATAOUT = DATA NIN	
	b. (BK0, BK1) in state (1, 1)	BKZZ = BK0 BK1 SEEK = ORD3 ORD4	
	c. (ORD0-ORD4) store (0 0011)		
	d. DCB in set state		
	e. FSC in set state		
	f. SCN in set state		
	g. RSD true		
	During preliminary phases (FS, FSZ, FSL) of data out service cycle, EP RAD controller address and unit address on function response lines (FR0D-FR7D) and (DORD, IORD) signals indicate data out service cycle	IORD = FSC NIN + ... DORD = FSC NDATA + ...	
	Start delay line at end of function strobe	DCL = CYCLE/C DCLSTART3 + ... DCLSTART3 = PHFSL NFSU + ...	
	Reset flip-flop PHFSL	R/PHFSL = ...	Exit phase FSL
	Set flip-flop PHRSA	S/PHRSA = FSCU PHRSASET PHRSASET = PHFSL NIN + ...	Enter phase RSA
RSA	(DA0R-DA7R)→(I00-I07)	IXD-1 = PHRSADO TCS000-3 PHRSADO = PHRSA DATAOUT	Byte 1 (track No. bits 0-6)
	Decrement byte counter (BK0, BK1) to (1, 0)	NBKCK = PHRSA SEKSEND TCS000-3 SEKSEND = SEEK NPHRSAOO + ... PHRSAOO = PHRSA ORDOUT BKZW = BK0 NBK1	BKZW signal enables data transfer in phase RS

(Continued)

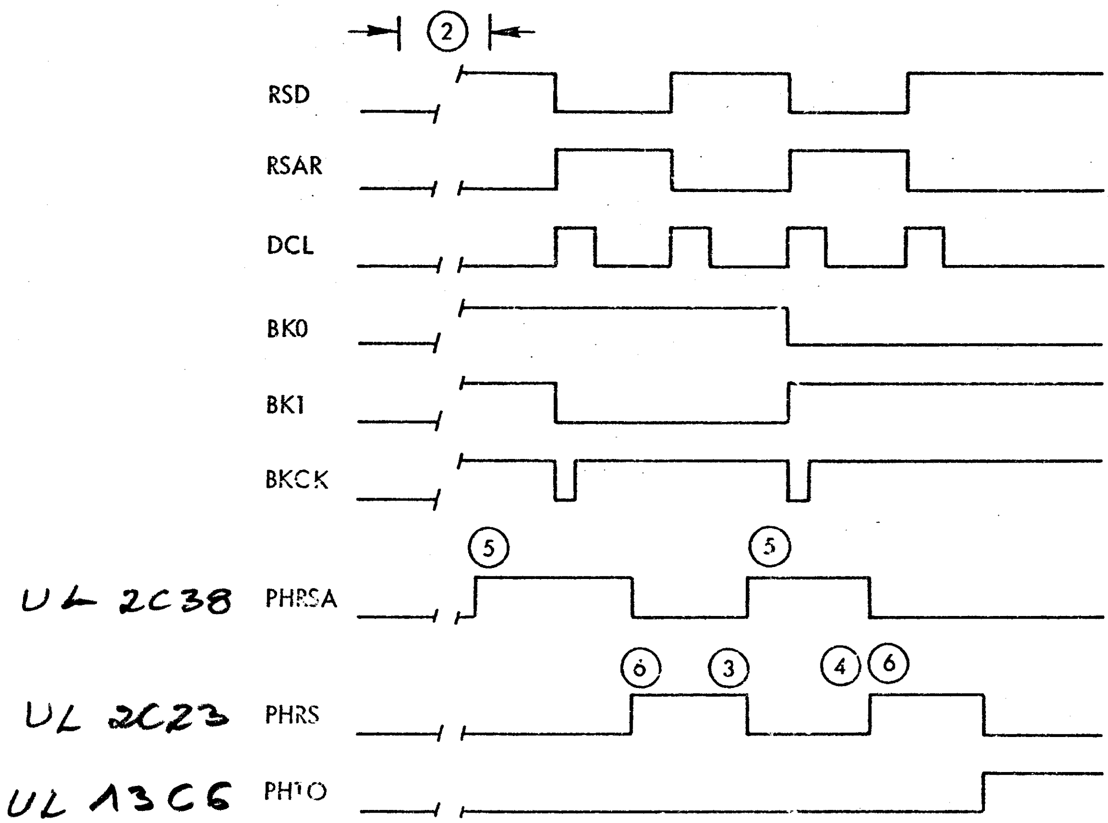
Table 4-15. Seek Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RSA (Cont.)	Start TCL delay line	DCL = CYCLE/C PHRSA RSAU + ...	
	Reset flip-flop PHRSA	R/PHRSA = ...	Exit phase RSA
	Set flip-flop PHRS	S/PHRS = FSCU PHRSET	Enter phase RS
		PHRSET = PHRSA + ...	
RS	(I00-I07)→(J00-J07)	If one-byte interface:	
		JXI1B = IOP PHRSDO TCS000-2 BYT1ID	
		PHRSDO = PHRS DATAOUT	
		If not one-byte interface:	
		JXIN1B = IOP DATAOUT TRS060 RWRITE-2 NBYT1ID	
	(J01-J07)→(T00-T06)	TXJ = SEEK RWRITEDO BKZW TRS130	
		RWRITEDO = RWRITE-2 DATAOUT	
	Raise request strobe signal RSD	RSD = FSC NRSAR (PHRS TCS000-2 + ...)	
	Raise end data signal ED internally	EDD = EDI FSC	
		EDI = EDISET1 NPHRSA + EDI FSCU + ...	
		EDISET1 = SEEK BKZW + ...	
	Start TCL delay line	DCL = CYCLE/C DCLSTART2 NRSAU + ...	
		DCLSTART2 = PHRS SEKSEND + ...	
		SEKSEND = SEEK NPHRSAOO + ...	
	Reset flip-flop PHRS	R/PHRS = ...	Exit phase RS
	Set flip-flop PHRSA	S/PHRSA = FSCU PHRSASET	Enter phase RSA
		PHRSASET = PHRSNED + ...	
		PHRSNED = PHRS NED	
RSA	(DA0R-DA7R)→(I00-I07)	IXD-1 = PHRSADO TCS000-3	Byte 2 (track No. bits 7-10; sector bits 0-3)
		PHRSADO = PHRSA DATAOUT	

(Continued)

Table 4-15. Seek Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RSA (Cont.)	Decrement byte counter (BK0, BK1) to (0, 1)	NBKCK = PHRSA SEKSEND TCS000-3 SEKSEND = SEEK NPHRSAOO + ... PHRSAOO = PHRSA ORDOUT BKWZ = NBK0 BK1	BKWZ signal enables data transfer in phase RS
	Start TCL delay line	DCL = CYCLE/C PHRSA RSAU + ...	
	Reset flip-flop PHRSA	R/PHRSA = ...	Exit phase RSA
	Set flip-flop PHRS	S/PHRS = FSCU PHRSET PHRSET = PHRSA + ...	Enter phase RS
RS	(I00-I07)→(J00-J07)	JXI1B = IOP PHRSADO TCS000-2 BYI1D PHRSADO = PHRS DATAOUT	
	Raise request strobe signal RSD	RSD = FSC NRSAR (PHRS TCS000-3 + ...)	
	(J00-J03)→(T07-T10)	TXJ = SEEK RWRITEDO BKWZ TRS130 RWRITEDO = DATAOUT RWRITE-2	
	(J04-J07)→(S00-S03)	SXJ = SEEK RWRITEDO BKWZ TRS130	
	Start TCL delay line	DCL = CYCLE/C DCLSTART2 NRSAU + ... DCLSTART2 = PHRS SEKSEND + ... SEKSEND = SEEK NPHRSAOO + ... PHRSAOO = PHRSA ORDOUT + ...	
	Reset flip-flop PHRS	R/PHRS = ...	Exit phase RS
	Set flip-flop PHTO	S/PHTO = PHRS ED	Enter phase TO
TO	Terminal order operations		See table 4-19



NOTES:

1. NO TIME SCALE: SEQUENCE OF EVENTS ONLY
2. PRELIMINARY OPERATIONS: ORDER OUT SERVICE CYCLE AND PHASES FS, FSZ, AND FSL OF DATA OUT SERVICE CYCLE
3. (J01 - J07) → (T00 - T06) FIRST BYTE
4. (J00 - J03) → (T07 - T10) } SECOND BYTE
   (J04 - J07) → (S00 - S03) }
5. (DA0R - DA7R) → (I00 - I07)
6. (I00 - I07) → (J00 - J07)

901565A. 411

Figure 4-26. Data Transfer During Seek Order, Timing Diagram

the controller, and transmitted to the addressed selection unit in serial form. The interface with the IOP may be one-, two-, or four-bytes wide. Data bytes are written starting at the track address and sector address indicated by the contents of the T-register and S-register. The contents of these registers are established by a seek order or by the contents remaining after execution of a previous order. The number of data bytes written is established by information available to the IOP. When the proper number of data bytes have been written, the IOP terminates execution of the write order with a count done terminal order, and an order in service cycle is requested by the controller.

Data transfers from the IOP to the FAM module proceed at a rate determined primarily by the IOP speed of response to requests from the controller. Data transfers from the FAM module to the selection unit must proceed at a rate determined by a clock signal internal to the controller.

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart

Phase	Function Performed	Signals Involved		Comments
	The write order or checkwrite order begins with an order out service cycle during which a write order code or a checkwrite order code is stored in the order register. The order out service cycle may follow an SIO command or an order in service cycle which ends with command chaining	WRITE	= NORD2 NORD3 ORD4	For both the write order and the checkwrite order, data bytes from the IOP pass through the FAM circuits to the selection unit interface circuits. No differences exist at the IOP interface
		CHWR	= ORD2 NORD3 ORD4	
		WCHW	= WRITE NPHRSAOO + CHWR NPHRSAOO	
		WRCH	= WRITE NPHRSAOO + RCHW NPHRSAOO	
		RCHW	= CHWR NPHRSAOO + ...	
		DATAOUT	= DATA NIN	
		BKZZ	= BK0 BK1	
FS	Direct set flip-flop SCN	M/SCN	= PHFS DCB CYCLE/C N(NSCNMEN)	CYCSET latched true. IOP true when controller is online. SCR preset during order out service cycle
		CYCLE/C	= CYCSET IOP + ...	
		N(NSCNMEN)	= NCDN DATAOUT SCR + ...	
	Raise service call line RSD	SCD	= LSL	Service call line held true until IOP responds with ASCR and FSR
		LSL	= NASCR SCN INC + ...	
	Start TCL delay line when ASCR and FSR true	DCL	= CYCLE/C DCLSTART1 + ...	
		DCLSTART1	= PHFS DCB BSYCU + ...	
		BSYCU	= BSYC IOP + ...	
		BSYC	= ASCM ASCR AVIR FSR + ...	
	Enable function response signals FR0D through FR7D	FR0D	= BSYC SWA0 + ...	(FR0D-FR3D) encode device controller address
		FR1D	= BSYC SWA1 + ...	
		FR2D	= BSYC SWA2 + ...	
		FR3D	= BSYC SWA3 + ...	
		FR4D	= BSYC GRD	FR4D always false
		FR5D	= BSYC U0 + ...	(FR5D-FR7D) encode device address

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved		Comments
FS (Cont.)		FR6D	= BSYC U1 + ...	
		FR7D	= BSYC U2 + ...	
	Set service connect flip-flop FSC as FSR goes false if previously reset by end service signal	S/FSC	= ASCB	FSC must be reset before RSD can be raised in phase FSL
		ASCB	= ASCM ASCR AVIR FSR (delayed NFSC)	
		C/FSC	= NFSC FSR + ...	
	Set NPHFS	S/NPHFS	= PHFS	End phase FS
		C/NPHFS	= TCS100-3	
	Set PHFSZ	S/PHFSZ	= PHFS	Enter phase FSZ
		C/PHFSZ	= TCS100-3	
FSZ	Start TCL delay line	DCL	= CYCLE/C PHFSZ + ...	Phase FSZ functions not significant for write order
	Reset PHFSZ	R/PHFSZ	= ...	End phase FSZ
		C/PHFSZ	= TCS100-3	
	Set PHFSL	S/PHFSL	= PHFSZ	Enter phase FSL
		C/PHFSL	= TCS100-3	
FSL	Raise request strobe signal RSD	RSD	= FSC NRSAR (FSCU RSD + NPHRSA RSET + ...)	RSD latches until RSAR raised by IOP
		RSET	= PHFSL NIN + ...	
	Enable data or order signals, and request data out service cycle	DORD	= FSC NDATA + ...	(DORD, IORD) is (0, 1)
		IORD	= FSC NIN + ...	
	Start TCL delay line	DCL	= CYCLE/C DCLSTART3 + ...	TCL delay line started when FSR goes false
		DCLSTART3	= PHFSL NFSU + ...	
		FSU	= FSR IOP + ...	
	If enough data bytes have been accepted, reset SCN; if additional data bytes are required, hold SCN in set state	S/SCN	= SCNEN	If SCN not in set state upon return to phase FS, service calls inhibited until SCR set
		SCNEN	= DATA SCN EXT SCSET	
		SCSET	= WCHW SCR RK1 + ...	

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)		R/SCN = SCNRST	
		SCNRST = PHFSL + ...	
		C/SCN = TCS100-3	
	Reset PHFSL	R/PHFSL = ...	End phase FSL
	Set PHRSA	S/PHRSA = PHRSASET FSCU	Enter phase RSA
		PHRSASET = PHFSL NIN + ...	
		C/PHRSA = TCS100-3	
RSA	Start TCL delay when IOP raises RSAR signal	DCL = CYCLE/C PHRSA RSAU + ...	
		RSAU = RSAR IOP + ...	
	Transfer data from IOP data lines to I-register		
	(DA0R-DA7R)→(I00-I07)	IXD = PHRSADO TCS000-3	
		PHRSADO = PHRSA DATAOUT	
	Reset SCR after sufficient bytes have been stored in FAM module	S/SCR = RREAD-2 SCRSET	SCR reset during FAM write cycle if SCRSET true
		SCRSET = NSCSET RK2 NRK3 NRK4	
		SCSET = WCHW RK1SCR + ...	
		RK1SCR = RK1 SCR	
		R/SCR = SCRSET	
		C/SCR = RKCK	
		NRKCK = TRS130 + ...	
		<u>If four-byte interface:</u>	
		M/EDISET3 = BYT4ID	
	Set EDISET3 to generate end data signal for use in phase RS	<u>If two-byte interface.</u>	
		S/EDISET3 = NSCR NEDIS3	
		NEDIS3 = PHRSADO NBYT1ID	

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RSA (Cont.)		If one-byte interface:	
		S/EDISET3 = NSCR NEDIS3	
		NEDIS3 = PHRSADO NRK3	
		C/EDISET3 = TCS100-3	
	Internally-generated end data signal	EDI = EDISET1 TCS000-2 + FSCU EDI + ...	
		EDISET1 = EDISET3 + ...	
	Reset PHRSA	R/PHRSA = ...	End phase RSA
	Set PHRS	S/PHRS = PHRSET FSCU	Enter phase RS
		PHRSET = PHRSA + ...	
		C/PHRS = TCS100-3	
RS	Raise request strobe signal RSD	RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)	RSD latches until RSAR raised by IOP
	Start TCL delay line as RSAR goes false	DCL = CYCLE/C DCLSTART2 NRSAU + ...	Signal JFI at false level
		DCLSTART2 = WCHW PHRS NJFI + ...	
	Preset signal JFI	JFI = N(JFIRESET RWRITE-2 TRS180) (JFIX1 + JFI NPHRSAOO + ...)	Signal JFI latched until data accepted from IOP has been transferred to J-register
		JFIX1 = PHRSDO TCS000-2	
		PHRSDO = PHRS DATAOUT	
	Mark byte counter	M/BK0 = BKX1	Byte counter direct set to (1, 1) during order out service cycle, but must be preset each time phase RS is entered from phase RSA
		BKX1 = NBKX1EN	
		BKX1EN = WCHW JFIX1 + ...	
		M/BK1 = BKX1	
	Clock byte counter	NBKCK = BKCKEN TRS270 + ...	For multiple-byte interface, byte counter is decremented as byte is transferred from J-register to FAM module
		BKCKEN = NBYT1ID (WCHW RWRITE-2 + BKCKEN NTRS030 + ...)	

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)		<u>If one-byte IOP interface:</u>	
	(I00-I07)→(J00-J07)	JXI1B = IOP PHRSDO BYT1ID TCS000-2	Data transfer occurs as soon as TCL delay line is started. Data transfer from J-register to FAM module controlled by TRL delay line
	Reset PHRS	R/PHRS = ...	End phase RS
	If end data, set PHTO	S/PHTO = PHRS ED ED = EDSET TCS000-2 + ED FSCU + ...	Enter phase TO. End data signal set internally during phase RSA and latched (or received from IOP)
		C/PHTO = TCS100-3	
	If not end data, set PHRSA	S/PHRSA = PHRSASET FSCU PHRSASET = PHRSNED	Enter phase RSA
		<u>If two-byte IOP interface:</u>	
	(I00-I07)→(J00-J07)	JXIN1B = IOP DATAOUT NBYT1ID RWRITE-2 TRS060	Data transfer occurs under control of TRL delay line
	(I08-I15)→(I00-I07)	IXI-1 = BKZZ RWRITEDO IXEN RWRITEDO = RWRITE-2 DATAOUT IXEN = NBYT1ID TRL180 NTRL240	For second data byte, data transfer occurs as part of first I-register to J-register transfer
	Decrement byte counter, causing BKZW to be true	BKZW = BK0 NBK1	
	(I00-I07)→(J00-J07)	JXIN1B = IOP DATAOUT NBYT1ID RWRITE-2 TRS060	Second data byte transferred to J-register
	Signal JFIRESET false causing JFI to be false	NJFIRESET = WCHW BK1 NBYT1ID + ...	As signal JFIRESET is false, latch is broken
	Reset PHRS, and set PHTO or PHRSA	DCL controlled by NJFI	
		<u>If four-byte IOP interface:</u>	
	(I00-I07)→(J00-J07)	JXIN1B = IOP DATAOUT NBYT1ID RWRITE-2 TRS060	Data transfer occurs under control of TRL delay line

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)	(I08-I15)→(I00-I07)	IXI-1 = BKZZ RWRITEDO IXEN RWRITEDO = RWRITE-2 DATAOUT IXEN = NBYT1ID TRL180 NTRL240	For second data byte, data transfer occurs as part of first I-register to J-register transfer
	Decrement byte counter, causing BKZW to be true		
	(I00-I07)→(J00-J07)	JXIN1B = IOP DATAOUT NBYT1ID RWRITE-2 TRS060	
	(I16-I23)→(I00-I07)	IXI-2 = BKZW RWRITEDO IXEN	As second data byte is transferred to J-register, third data byte is transferred to higher order byte of I-register
	Decrement byte counter, causing BKWZ to be true	BKWZ = NBK0 BK1	
	(I00-I07)→(J00-J07)	JXIN1B = IOP DATAOUT NBYT1ID RWRITE-2 TRS060	
	(I24-I31)→(I00-I07)	IXI-3 = BKWZ RWRITEDO IXEN	As third data byte is transferred to J-register, fourth data byte is transferred to higher order byte of I-register
	Decrement byte counter, causing BKWW to be true	BKWW = NBK0 NBK1	
	Signal JFIRESET false, causing JFI to be false	NJFIRESET = WCHW BK0 BYT4ID	As signal JFIRESET is false, JFI latch is broken
	Reset PHRS and set PHTO	DCL = CYCLE/C DCLSTART2 NRSAU + ... DCLSTART2 = WCHW PHRS NJFI + ...	Only one phase RS needed to accept four bytes from IOP
TO	Start TCL delay line when RSAR true	DCL = CYCLE/C DCLSTART1 + ... DCLSTART1 = PHTO RSAU + ...	
	If IOP transmits count done terminal order, set CDN	S/CDN = DA1R TORD TORD = IOP NES ED PHTO C/CDN = NTCS000	Refer to table 4-19 for terminal order operations other than count done
	If CDN, place (DATA, IN) flip-flops to (0, 1) state to request order in service cycle during next phase FS	S/DATA = DATASET NORDIN NDATASET = CDN + ... ORDIN = NDATA IN R/DATA = ...	If IOP does not transmit terminal order, data out service cycles continue following return to phase FS

(Continued)

Table 4-16. Write Order or Checkwrite Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
TO (Cont.)		C/DATA = PHFSTOD TCS100-3	
		PHFSTOD = PHTO + ...	
		S/IN = INSET NORDIN	
		INSET = NDATASET + ...	
		C/IN = PHFSTOD TCS100-3	
	Whether or not terminal order received from IOP:		
	Reset PHTO	R/PHTO = ...	End phase TO
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS
		PHFSET = PHTO + ...	

Thus data must be accepted from the IOP and written in the disc file at a predetermined rate so that all sectors are filled with the correct number of bytes. The FAM circuit provides a buffer between these two independently-controlled operations.

4-99 Read Order Sequence

If a read order (X XX10) is stored in the order register during an order out service cycle, the sequence outlined in table 4-17 follows. During execution of a read order, a sequence of data in service cycles is requested by the controller. During each data in service cycle, data bits are accepted serially from the addressed selection unit, assembled into eight-bit bytes, stored temporarily in registers of the controller, and transmitted to the IOP. The interface with the IOP may be one-, two-, or four-bytes wide. Data bits are read starting at the track address and the sector address indicated by the contents of the T-register and S-register. The contents of these registers are established by a seek order or by the contents remaining after execution of a previous order. The number of data bytes read is established by information available to the IOP. When the proper number of data bytes have been read, the IOP terminates execution of the read order with a count done terminal order, and an order in service cycle is requested by the controller.

Data transfers from the selection unit interface to the FAM circuits proceed at a rate determined primarily by the bit rate of the addressed selection unit. Data transfers from the FAM circuits to the IOP proceed at a rate determined primarily by the ability of the IOP to accept data. Thus, data must be accepted from the addressed selection unit at a rate established by a clock signal extracted from the Manchester-encoded data and must be accepted by the IOP at a rate established by the IOP speed of response to requests from the controller. The FAM circuits provide a buffer between these two independently-controlled operations.

4-100 Checkwrite Order Sequence

If a checkwrite order (X X101) is stored in the order register during an order out service cycle, the sequence outlined in table 4-16 follows. The checkwrite order combines operations of the write order with operations of the read order. Data bytes are accepted from the IOP on either a one-, two-, or four-byte interface. Data is read from the addressed selection unit, is assembled into eight-bit bytes, and is compared with the data accepted from the IOP. The data accepted from the IOP during the succession of data out service cycles must have been previously written into the addressed locations during execution of a write order, and the same number of bytes must be read during execution of the checkwrite order as were written during execution of the write order. Data is neither written nor read during execution of a checkwrite order.

4-101 Order In Service Cycle

Each input/output operation ends with an order in service cycle during which information is provided to the IOP, as indicated in table 4-18. During the terminal order phase of an order in service cycle, the command chaining bit is sampled. If the command chaining bit is true, an order out service cycle may follow the order in service cycle. If the command chaining bit is false, the controller returns to the ready automatic state and cannot accept new orders until an SIO command is transmitted from the IOP and is accepted by the controller.

Table 4-17. Read Order, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
	The read order begins with an order out service cycle during which a read order code is stored in the order register. The order out service cycle may follow an SIO command or an order in service cycle which ends with command chaining	READ = ORD3 NORD4	
		RCHW = READ NPHRSAOO + ...	
		WRCH = RCHW NPHRSAOO + ...	
		BKZZ = BK0 BK1	
		DATAIN = DATA IN	
FS	Wait until selection unit interface circuits transfer sufficient data to FAM circuits	S/SCR = RREAD-2 SCRSET	SCR preset during order out service cycle, reset when data in FAM module
		SCRSET = NSCSET RK2 NRK3 NRK4	
		SCSET = READ NRK1 + ...	
		R/SCR = SCRSET	
		C/SCR = RKCK	
		NRKCK = TRS130 + ...	
	Direct set SCN	M/SCN = PHFS DCB CYCLE/C N(NSCNMEN)	
		CYCLE/C = IOP CYCSET + ...	CYCSET latched true
		N(NSCNMEN) = NCON READ KFID NSCR + ...	IOP true when controller is online. KFID true when K-register filled and four bytes in FAM module
		KFID = KX0 (KFID + KFIDX1)	
		KFIDX1 = KFI TRS270	
	Raise service call line SCD	SCD = LSL	Service call line held true until IOP responds with ASCR and FSR
		LSL = NASCR SCN INC + ...	
	Start TCL delay line when ASCR and FSR true	DCL = CYCLE/C DCLSTART1 + ...	
		DCLSTART1 = PHFS DCB BSYCU + ...	
		BSYCU = BSYC IOP + ...	
		BSYC = ASCM ASCR AVIR FSR + ...	

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FS (Cont.)	Enable function response signals FR0D through FR7D	FR0D = BSYC SWA0 + ...	(FR0D-FR3D) encode device controller address
		FR1D = BSYC SWA1 + ...	
		FR2D = BSYC SWA2 + ...	
		FR3D = BSYC SWA3 + ...	
		FR4D = BSYC GRD + ...	FR4D always false
		FR5D = BSYC U0 + ...	(FR5D-FR7D) encode device address
		FR6D = BSYC U1 + ...	
		FR7D = BSYC U2 + ...	
	Set service connect flip-flop FSC as FSR goes false if FSC was previously reset by end service signal	S/FSC = ASCB ASCB = ASCM ASCR AVIR FSR (delayed NFSC)	FSC must be set before RSD can be raised
		C/FSC = NFSC FSR + ...	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	Enter phase FSZ
		C/PHFSZ = TCS100-3	
FSZ	Start TCL delay line	DCL = CYCLE/C PHFSZ + ...	Phase FSZ functions not significant for read order
	Reset PHFSZ	R/PHFSZ = ...	End phase FSZ
	Set PHFSL	S/PHFSL = PHFSZ	Enter phase FSL
		C/PHFSL = TCS100-3	
FSL	Enable data or order signals to request data in service cycle	DORD = FSC NDATA + ...	(DORD, IORD) are (0, 0)
		IORD = FSC NIN + ...	
	Start TCL delay line	DCL = CYCLE/C DCLSTART3 + ... DCLSTART3 = PHFSL NFSU + ... FSU = FSR IOP + ...	TCL delay line started when FSR goes false

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	If enough data bytes are available for transfer to IOP, hold SCN in set state; if additional data bytes are required for data in service cycle, reset SCN	S/SCN = SCNEN SCNEN = DATA SCN EXT SCSET SCSET = READ NRK1 + ... R/SCN = SCNRST SCNRST = PHFSL + ... C/SCN = TCS100-3	If SCN not in set state upon return to phase FS, service calls inhibited until SCR is reset
	Reset PHFSL	R/PHFSL = ...	End phase FSL
	Set PHRS	S/PHRS = PHRSET FSCU PHRSET = PHFSL IN + ... FSCU = FSC IOP + ... C/PHRS = TCS100-3	Enter phase RS
RS	Start TCL delay line when RSAR false	DCL = CYCLE/C DCLSTART2 NRSAU + ... DCLSTART2 = PHRS READ KFID + ... RSAU = RSAR IOP + ...	TCL delay line started when RSAU false, because KFID at true level
	Raise request strobe signal RSD	RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)	Signal RSD first raised in phase FSL, but must be raised each time phase RS is entered
	Transfer data from addressed location in FAM module to K-register (R00-R07)⟶(K00-K07) Transfer data from K-register to O-register (K00-K07)⟶(O00-O07)	KXR = KXREN RREAD-2 TRS180 KXREN = BKZZ + ... OXK = OXKEN TCS000-2 OXKEN = PHRS DATAIN NED	Transfer of data from addressed location in FAM module to K-register takes place under control of FAM circuits. This transfer must occur before exit from phase FSL to phase RS, and before TCL delay line is started in phase RS (KFID true)

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)	Transfer data from addressed location in FAM module to I-register, clock byte counter. Raise end data signal if sufficient data bytes are not stored in FAM module, preset KFI when K-register and I-register filled with data for O-register	If multiple-byte IOP interface	For multiple-byte IOP interface, additional bytes are taken from the FAM module to the I-register for transfer to O-register. Data transfer is controlled by the byte counter
	Mark byte counter	M/BK0 = BKX1 BKX1 = NBKX1EN NBKX1EN = KX0EN READ + ... KX0EN = OXKEN TCS100-3 M/BK1 = BKX1	Byte counter direct set to (1, 1) during order out service cycle, but must be preset each time data is transferred from K-register and I-register to O-register
	Clock byte counter	NBKCK = BKCKEN TRS270 + ... BKCKEN = NBYT1ID (READ-1 READRR + BKCKEN NTRS030 + ...)	For multiple-byte IOP interface, byte counter is incremented as the byte is transferred from the FAM module to the K-register or I-register
		If two-byte IOP interface:	
	First data byte transferred as for one-byte IOP interface		
	(R00-R07)→(K00-K07)	KXR = KXREN RREAD-2 TRS180 KXREN = READRR + ... READRR = READ RREAD-2	
	Decrement byte counter, causing signal BKZW to be true	BKZW = BK0 NBK1	
	Transfer second data byte from addressed location in FAM module		
	(R00-R07)→(I08-I15)	IXR-1 = IXEN READRR BKZW IXEN = NBYT1ID TRL180 NTRL240	

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)	As second data byte is stored, raise and latch KFI	KFI = KX0 (KFIX1 + KFI NPHRSAOO) NKX0 = KX0EN KX0EN = OXKEN TCS100-3 KFIX1 = KFISET RREAD-2 TRS180 NKFISET = NBYT1ID READRR BK1 + ...	During each FAM read cycle, RREAD-2 is true. When BK1 is false, KFISET is driven false, and KFIX1 raises KFI, which is latched until KX0 is false
	Raise and latch KFID	KFID = KX0 (KFID + KFIDX1) KFIDX1 = KFI TRS270	KFID enables TCL delay line to start in phase RS (next RSAR signal)
	Transfer data to O-register (K00-K07)→(O00-O07) (I08-I15)→(O08-O15)	 OXK = OXKEN TCS000-2 OXK = OXKEN TCS000-2	Transfer of data from K-register and I-register to O-register takes place at start of phase RS. Transfer of data from FAM module to K-register and I-register is independent of phase control timing, but data must be available before transfer to phase RS is allowed
	Mark byte counter	KX0EN = OXKEN TCS100-3	Prepare for next phase RS
		<u>If four-byte IOP interface:</u>	
	First data byte transferred as for one-byte IOP interface (R00-R07)→(K00-K07)	 KXR = KXREN RREAD-2 TRS180 KXREN = READRR + ... READRR = READ RREAD-2	
	Decrement byte counter, causing signal BKZW to be true	BKZW = BK0 NBK1	
	Transfer second data byte from addressed location in FAM module (R00-R07)→(I08-I15)	 IXR-1 = IXEN READRR BKZW IXEN = NBYT1ID TRL180 TRL240	

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)	Decrement byte counter, causing signal BKWZ to be true	BKWZ = NBK0 BK1	
	Transfer third data byte from addressed location in FAM module		
	(R00-R07)→(I16-I23)	IXR-2 = IXEN READRR BKWZ	
	Decrement byte counter, causing signal BKWW to be true	BKWW = NBK0 NBK1	
	Transfer fourth data byte from addressed location in FAM module	IXR-3 = IXEN READRR BKWW	
	As second data byte is stored, raise and latch KFI by driving KFISET false	KFI = KX0 (KFIX1 + KFI NPHRSA00) NKX0 = KX0EN + ... KX0EN = OXKEN TCS100-3 KFIX1 = KFISET RREAD-2 TRS180 NKFISET = BYT4ID READRR BK0 + ...	During each FAM read cycle, RREAD-2 is true. When BK0 false, KFISET driven false. KFIX1 raises KFI, which is latched until KX0 is false
	Raise and latch KFID	KFID = KX0 (KFID + KFIDX1) KFIDX1 = KFI TRS270	KFID enables TCL delay line to start in phase RS (next RSAR signal)
	Transfer data to O-register		Transfer of data from K-register and I-register to O-register takes place at start of phase RS. Transfer of data from FAM module to K-register and I-register is independent of phase control timing, but data must be available before transfer to phase RS is allowed
	(K00-K07)→(O00-O07)	OXK = OXKEN TCS000-2	
	(I08-I15)→(O08-O15)	OXK = OXKEN TCS000-2	
	(I16-I23)→(O16-O23)	OXK = OXKEN TCS000-2	
	(I24-I31)→(O24-O31)	OXK = OXKEN TCS000-2	
	Mark byte counter	KX0EN = OXKEN TCS100-3	Prepare for next phase RS
	End data signal raised and latched internally to control phase sequence	EDI = EDISET2 NPHRSA + EDI FSCU + ... EDISET2 = OXKEN KA8 KA8 = SCR REMPTY KFIDX1 + SCR KA8 KFID REMPTY = RK0 RK1 RK2 RK3 RK4	Signal KA8 raised and latched if FAM module empty when KFIDX1 true. If so, EDISET2 raised and latched

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS (Cont.)	Reset PHRS	R/PHRS = ...	End phase RS
	If end data, set PHTO	S/PHTO = PHRS ED	Enter phase TO
		C/PHTO = TCS100-3	
	If not end data, set PHRSA	S/PHRSA = PHRSASET FSCU	Enter phase RSA
		PHRSASET = PHRSNED	
		PHRSNED = PHRS NED	
		C/PHRSA = TCS100-3	
RSA	Start TCL delay line when IOP raises RSAR	DCL = CYCLE/C PHRSA RSAU + ...	O-register data accepted by IOP
		RSAU = RSAR IOP + ...	
	Reset PHRSA	R/PHRSA = ...	End phase RSA
	Set PHRS	S/PHRS = PHRSET FSCU	Enter phase RS
		PHRSET = PHRSA + ...	
TO	Start TCL delay line when RSAR true	DCL = CYCLE/C DCLSTART1 + ...	
		DCLSTART1 = PHTO RSAU + ...	
	If IOP transmits count done terminal order, set CDN	S/CDN = DA1R TORD	Refer to table 4-19 for terminal order operations other than count done
		TORD = IOP NES ED PHTO	
		C/CDN = NTCS000	
	If CDN, place (DATA, IN) flip-flops to (0, 1) state to request an order in service cycle during next phase FS	S/DATA = DATASET NORDIN	If IOP does not transmit terminal order, data in service cycles continue following return to phase FS
		NDATASET = CND + ...	
		ORDIN = NDATA IN	
		R/DATA = ...	
		C/DATA = PHFSTOD TCS100-3	
		PHFSTOD = PHTO + ...	
		S/IN = INSET NORDIN	
		INSET = NDATASET + ...	
		C/IN = PHFSTOD TCS100-3	

(Continued)

Table 4-17. Read Order, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
TO (Cont.)	Whether or not terminal order received from IOP:		
	Reset PHTO	R/PHTO = ...	End phase TO
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS
		PHFSET = PHTO + ...	

Table 4-18. Order In Service Cycle, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
FS	If phase FS follows count done terminal order or IOP unusual end, (DATA, IN) flip-flops are placed in state (0, 1) during previous phase TO:		Service call line held true until IOP responds with ASCR and FSR
	Raise service call line SCD	SCD = LSL	
		LSL = NASCR SCN INC + ...	
		M/SCN = PHFS DCB CYCLE/C N(NSCNMEN)	If DATA is not in reset state, previously existing conditions hold N(NSCNMEN) at true level
		N(NSCNMEN) = NDATA NRWE NWCHW + ...	
	Start TCL delay line when ASCR and FSR true	DCL = CYCLE/C DCLSTART1 + ...	
		DCLSTART1 = PHFS DCB BSYCU + ...	
		BSYCU = BSYC IOP + ...	
		BSYC = ASCM ASCR AVIR FSR + ...	
	Enable function response signals FR0D through FR7D	FR0D = BSYC SWA0 + ...	(FR0D-FR3D) encode device controller address
		FR1D = BSYC SWA1 + ...	
		FR2D = BSYC SWA2 + ...	
		FR3D = BSYC SWA3 + ...	
		FR4D = BSYC GRD + ...	FR4D always false
		FR5D = BSYC U0 + ...	(FR5D-FR7D) encode device address
		FR6D = BSYC U1 + ...	
		FR7D = BSYC U2 + ...	

(Continued)

Table 4-18. Order In Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FS (Cont.)	If phase FS follows detection of controller error, place (DATA, IN) flip-flops to (0, 1)	S/DATA = DATASET NORDIN	(DATA, IN) flip-flops must be in state (0, 1) to request order in service cycle
		DATASET = NCDN NCDNPET NUNE NSKSBK	
		ORDIN = NDATA IN	
		C/DATA = PHFSTOD TCS100-3	
		PHFSTOD = PHFS DATA	
		R/DATA = ...	
		S/IN = INSET NORDIN	
		INSET = NDATASET + ...	
		C/IN = PHFSTOD TCS100-3	
	Set NPHFS	S/NPHFS = PHFS	End phase FS
		C/NPHFS = TCS100-3	
	Set PHFSZ	S/PHFSZ = PHFS	
		C/PHFSZ = TCS100-3	Enter phase FSZ
FSZ	Start TCL delay line	DCL = CYCLE/C PHFSZ + ...	
	Reset PHFSZ	R/PHFSZ = ...	End phase FSZ
	Set PHFSL	S/PHFSL = PHFSZ	Enter phase FSL
		C/PHFSL = TCS100-3	
FSL	Start TCL delay line	DCL = CYCLE/C DCLSTART3 + ...	TCL delay line started when FSR goes false
		DCLSTART3 = PHFSL NFSU + ...	
		FSU = FSR IOP + ...	
	Reset service call flip-flop SCN	R/SCN = SCNRST	SCN reset to prevent additional service calls
		SCNRST = PHFSL + ...	
		C/SCN = TCS100-3	
	Reset PHFSL	R/PHFSL = ...	End phase FSL

(Continued)

Table 4-18. Order In Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
FSL (Cont.)	Set PHRS	S/PHRS = FSCU PHRSET	Enter phase RS
		PHRSET = PHFSL IN + ...	
		FSCU = FSC IOP + ...	
RS	Start TCL delay line	DCL = CYCLE/C DCLSTART3 + ...	
		DCLSTART3 = PHRS NDATA NRSAU + ...	
		RSAU = RSAR IOP + ...	
	Raise request strobe line RSD	RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-2 + ...)	RSD remains high until request strobe acknowledge signal received from IOP
	Load data into O-register	O00 = OXORDIN TER + ...	Contents of O-register on IOP data lines contains (XX01 X000), depending on state of flip-flops
	(TER, INL, 1, UNE)→(O00, O01, O03, O04)	OXORDIN = PHRSNED ORDIN	
		PHRSNED = PHRS NED	
		O01 = OXORDIN INL + ...	
		O03 = OXORDIN + ...	
		O04 = OXORDIN UNE + ...	
	Reset PHRS	R/PHRS = ...	End phase RS
	Set PHRSA	S/PHRSA = PHRSASET FSCU	Enter phase RSA
		PHRSASET = PHRSNED + ...	
		C/PHRSA = TCS100-3	
RSA	Start TCL delay line when request strobe acknowledge signal received from IOP	DCL = CYCLE/C PHRSA RSAU + ...	IOP accepts data in O-register
		RSAU = RSAR IOP + ...	
	Reset PHRSA	R/PHRSA = ...	End phase RSA
	Set PHRS	S/PHRS = PHRSET FSCU	Enter phase RS
		PHRSET = PHRSA + ...	
		C/PHRS = TCS100-3	

(Continued)

Table 4-18. Order In Service Cycle, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
RS	Start TCL delay line when request strobe acknowledge signal RSAR goes false	DCL = CYCLE/C DCLSTART3 + ...	
		DCLSTART3 = PHRS NDATA NRSAU + ...	
	Raise request strobe line RSD	RSD = FSC NRSAR (FSCU RSD + PHRS TCS000-3 + ...)	RSD remains high until RSAR received from IOP
	Reset PHRS	R/PHRS = ...	End phase RS
	Set PHTO	S/PHTO = PHRS ED	Enter phase TO
		ED = EDSET TCS000-2 + ED FSCU + ...	End data signal set internally and latched
		EDI = EDI FSCU + EDISET1 NPHRSA + ...	
		EDISET1 = NDATA + ...	
		C/PHTO = TCS100-3	
TO	Start TCL delay line when RSAR true	DCL = CYCLE/C DCLSTART1 + ...	
		DCLSTART1 = PHTO RSAU + ...	
	If end service, reset FSC	R/FSC = ESR FSC	
		C/FSC = FSC RSD + ...	
	If end service, reset DCB. If not end service, not unusual end, and command chaining is ordered by IOP, inhibit reset of DCB	R/DCB = DCBRST	
		DCBRST = DCBRST1 + ...	
		DCBRST1 = PHTO ORDIN DCBRSTEN	
		DCBRSTEN = N(CCH NES NUNE)	
		CCH = IOP DA2R NDA3R	
		C/DCB = NTCS080	
	Reset PHTO	R/PHTO = ...	End phase TO
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS
		PHFSET = PHTO + ...	
		C/NPHFS = TCS100-3	

4-102 Terminal Order Operations

Every service cycle ends with a terminal order phase during which a terminal order may be received from the IOP, as indicated in table 4-19. If no terminal order is received and no errors have occurred during data processing, the order in process continues. The count done terminal order that ends every errorless input/output operation is followed by an order in service cycle. Interrupt terminal orders and unusual end terminal orders are commanded by the IOP and may cause the data processing to stop. A command chaining terminal order can occur only during an order in service cycle and causes an order out service cycle to follow the order in service cycle. Controller errors are acted upon during the terminal order phase, regardless of when they occur.

Table 4-19. Terminal Order Operations, Phase Sequence Chart

Phase	Function Performed	Signals Involved	Comments
TO	Start TCL delay line	DCL = CYCLE/C DCLSTART1 + CYCLE/C DCLSTART2 + ...	
		DCLSTART1 = PHTO RSAU + ...	
		DCLSTART2 = PHTO ES + ...	
	IOP Signals		
	If count done, set CDN	S/CDN = DA1R TORD	Indicates all data has been transferred for read, write, or checkwrite operation. Reset during next order out service cycle
		TORD = IOP NES ED PHTO	
		C/CDN = NTCS000	
	If interrupt, set CIL	S/CIL = DA0R TORD	Reset by AIO command. New SIO cannot be accepted until CIL is reset. The order in process goes to completion
		C/CIL = NTCS000	
	If unusual end, set UNE	S/UNE = DA3R TORD	Reset by new SIO
		C/UNE = NTCS000	
	If UNE or CDN set, reset DATA and set IN to request order in service cycle upon return to phase FS	S/DATA = DATASET NORDIN	
		DATASET = NCDN NCDNPET NUNE NSKSBK	
		ORDIN = NDATA IN	
		C/DATA = PHFSTOD TCS100-3	
		PHFSTOD = PHTO + ...	
		S/IN = INSET NORDIN	
		INSET = NDATASET + ...	
		C/IN = PHFSTOD TCS100-3	

(Continued)

Table 4-19. Terminal Order Operations, Phase Sequence Chart (Cont.)

Phase	Function Performed	Signals Involved	Comments
TO (Cont.)	Reset PHTO	R/PHTO = ...	End phase TO
		C/PHTO = TCS100-3	
	Reset NPHFS	R/NPHFS = PHFSET	Enter phase FS
		PHFSET = PHTO + ...	
		C/NPHFS = TCS100-3	

4-103 EP RAD SELECTION UNIT

The EP RAD selection unit either accepts data signals and control signals from the EP RAD controller and writes Manchester-encoded data on the magnetic surfaces of the disc file, or reads Manchester-encoded data from the disc file and transmits data signals and control signals to the EP RAD controller. A maximum of eight EP RAD selection units may interface with one EP RAD controller. Each EP RAD selection unit interfaces with one disc file.

All EP RAD selection units of an EP RAD file are connected to the associated EP RAD controller by a common cable assembly, as indicated in figure 3-1. Interface signals common to the EP RAD controller and to all EP RAD selection units of an EP RAD file are listed in table 4-20. Signals generated by an EP RAD selection unit or received by an EP RAD selection unit are valid only if the EP RAD selection unit is addressed by the EP RAD controller.

4-104 ADDRESS CIRCUITS (See figure 6-5)

Signals ID0R, ID1R, and ID2R, which are transmitted from the U-register of the controller, provide inputs to all selection units. For one selection unit, the address encoded by the signal levels matches the address encoded by switch settings of the LT26 Switch Comparator module, causing signal SEL for the addressed selection unit to be true. If no power failure has occurred (NPDLY true), signal DVT is true, generating a true device test signal DVTD. In response to an accepted SIO command, the controller generates a true SLNR signal. As signal SLNR goes false, flip-flop USLA of the addressed selection unit (SEL true) is set. Once signal USLA is true, signals USLB, TYP0, TYP1, and DVOD are true, and interface signals for the addressed selection unit are valid.

4-105 TRACK REGISTER (See figure 6-6)

The track register, which consists of flip-flops TR0 through TR10, is cleared by a true PDLY signal.

(E/TR0-E/TR10) = PDLY

The track register is a serial register clocked by signal SC1R, which is generated by the controller. While the selection unit is addressed, the track register is loaded with an 11-bit track address during each intersector gap time. Signal SC1R is true 11 times, and the track address bits are accepted from the controller through signal TRKR. (The two most significant bits should always be zeros.)

S/TR0 = TRKR USLA

S/TR1 = TR0

⋮ ⋮

S/TR10 = TR9

(C/TR0-C/TR10) = SC1R

Outputs of the track register address one of the 512 read/write heads and permit reading from or writing into the track associated with the addressed read/write head. Signals from TR2 through TR5 are used in the memory protect circuits.

4-106 MEMORY PROTECT CIRCUITS (See figure 6-8)

The memory protect circuits accept output signals from the four most significant bits of the track register (TR2, TR3, TR4, and TR5) and generate 16 output signals, as summarized in table 4-21. For any possible combination of the four inputs, one of signals NGT01 through NGT16 is false. If the switch associated with the signal is closed, signal TRP is driven false. If the selection unit is addressed, signal USLA is true and a true TRPD signal is generated to indicate that the addressed track is write-protected. If an order other than write is being executed, signal TRPD does not affect operation of the controller. Tracks must be protected in groups of 32, as indicated in table 4-21 since the four most significant bits of any address cause all tracks in that range to be protected.

4-107 ANGLE REGISTER (See figure 6-9)

The angle register, which consists of flip-flops AN0 through AN3, is cleared to 0000 by index pulse IP.

(E/AN0-E/AN3) = IP

Table 4-20. EP RAD Selection Unit Interface Signals

Signal	Function
/AN0/-/AN3/	Sector address (angle) data to controller. A four-bit code which indicates the address of the sector currently under the read/write heads
/DAI/	Data signal to controller. Developed from Manchester-encoded data written on disc file
/DAT/	Data output to storage unit from D07 of controller
/DS/	Data strobe to controller. Developed from Manchester-encoded data. Provides the clock signal associated with /DAI/
/DVT/	Device test signal to controller
/DVO/	Device operational signal to controller
/ID0/-/ID2/	Device address signals from controller. The selection unit controls signal levels on the common cable assembly only if the device address signals match the address set in the module
/IP/	Index pulse to controller. Generated once per revolution of the disc
/NMNRST/	Manual reset signal from controller. Developed by signal NPWRMON
/PWRMON/	Signal to controller. True when power circuits operating properly
/SAI/	Sector amplified enable signal from controller. True after track address has been shifted from controller to addressed selection unit during intersector gap time
/SC1/	Track and sector shift clock. True 11 times during intersector gap time to permit output of TRKR to be stored in track register
/SC2/	Data clock from controller. True during execution of write order to enable Manchester-encoded data to be stored on disc
/SLN/	Select now signal from controller. True when an SIO command is accepted
/SP/	Sector pulse signal to controller. True 11 times for each revolution of the disc
/TRK/	Track address bits from controller. Read under control of signal /SC1/
/TRP/	Track protect signal to controller. True when controller attempts to write in a write-protected track
/TYP0/-/TYP1/	Storage unit type signals to controller. For EP RAD storage unit, both signals are true
/WEN/	Write enable signal from controller. True during execution of write order, after read/write enable flip-flop in controller is set

Table 4-21. Memory Protect Signals

TRACK REGISTER OUTPUTS				TRACKS PROTECTED	OUTPUT SIGNAL
TR2	TR3	TR4	TR5		
0	0	0	0	0-31	NTG01
0	0	0	1	32-63	NTG02
0	0	1	0	64-95	NTG03
0	0	1	1	96-127	NTG04
0	1	0	0	128-159	NTG05
0	1	0	1	160-191	NTG06
0	1	1	0	192-223	NTG07
0	1	1	1	224-255	NTG08
1	0	0	0	256-287	NTG09
1	0	0	1	288-319	NTG10
1	0	1	0	320-351	NTG11
1	0	1	1	352-383	NTG12
1	1	0	0	384-415	NTG13
1	1	0	1	416-447	NTG14
1	1	1	0	448-479	NTG15
1	1	1	1	480-511	NTG16

The reset input to each flip-flop is its complement, so a flip-flop goes from the set state to the reset state on the falling edge of a clock signal.

S/AN0 = NAN0

S/AN1 = NAN1

S/AN2 = NAN2

S/AN3 = NAN3

The clock signal for flip-flop AN3 is the complement of sector pulse SP, so that it changes state on the rising edge of each sector pulse SP. The clock signal for other flip-flops is the complement of sector pulse SP gated with outputs of other flip-flops.

C/AN3 = NSP

C/AN2 = NSP AN3

C/AN1 = NSP AN3 AN2

C/AN0 = NSP AN3 AN2 AN1

Therefore, the angle register changes state at the rising edge of each sector pulse, counting in binary sequence from 0000 to 1011, in which AN3 represents the least significant bit and AN0 represents the most significant bit. After the angle register reaches 1011, the index pulse clears it to 0000.

4-108 HEAD SELECTION MATRIX

Selection of a read/write head is controlled by outputs of the track register which select a read/write head through the LT76 Read/Write Coupler modules and the RT18 Y-Select modules. (See figure 4-27.) The selected read/write head either provides inputs to the LT76 module for transmission to the controller or accepts signals from the controller which enable writing data on the disc file.

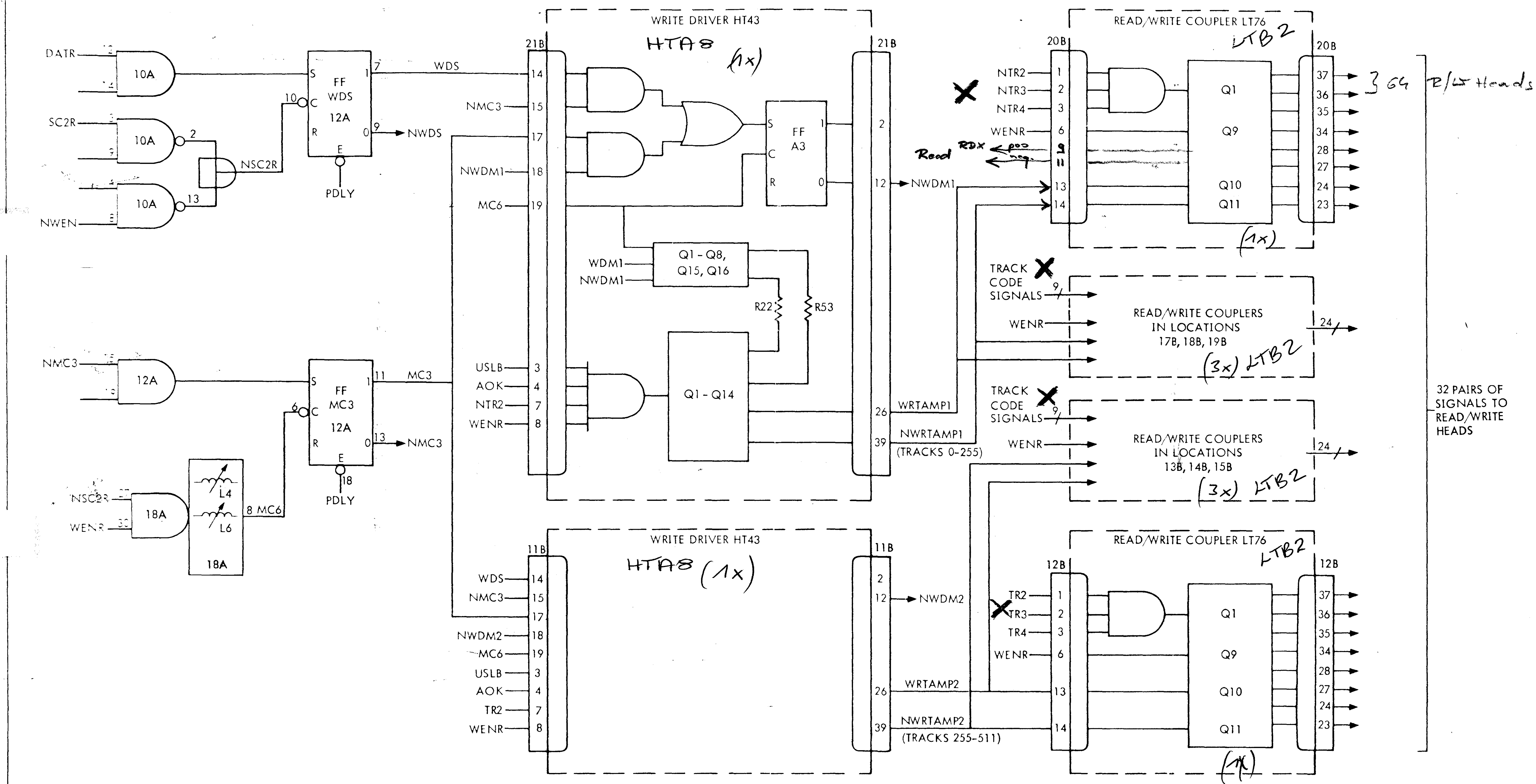


Figure 4-28. Write Channel, Schematic Diagram

901565A.405

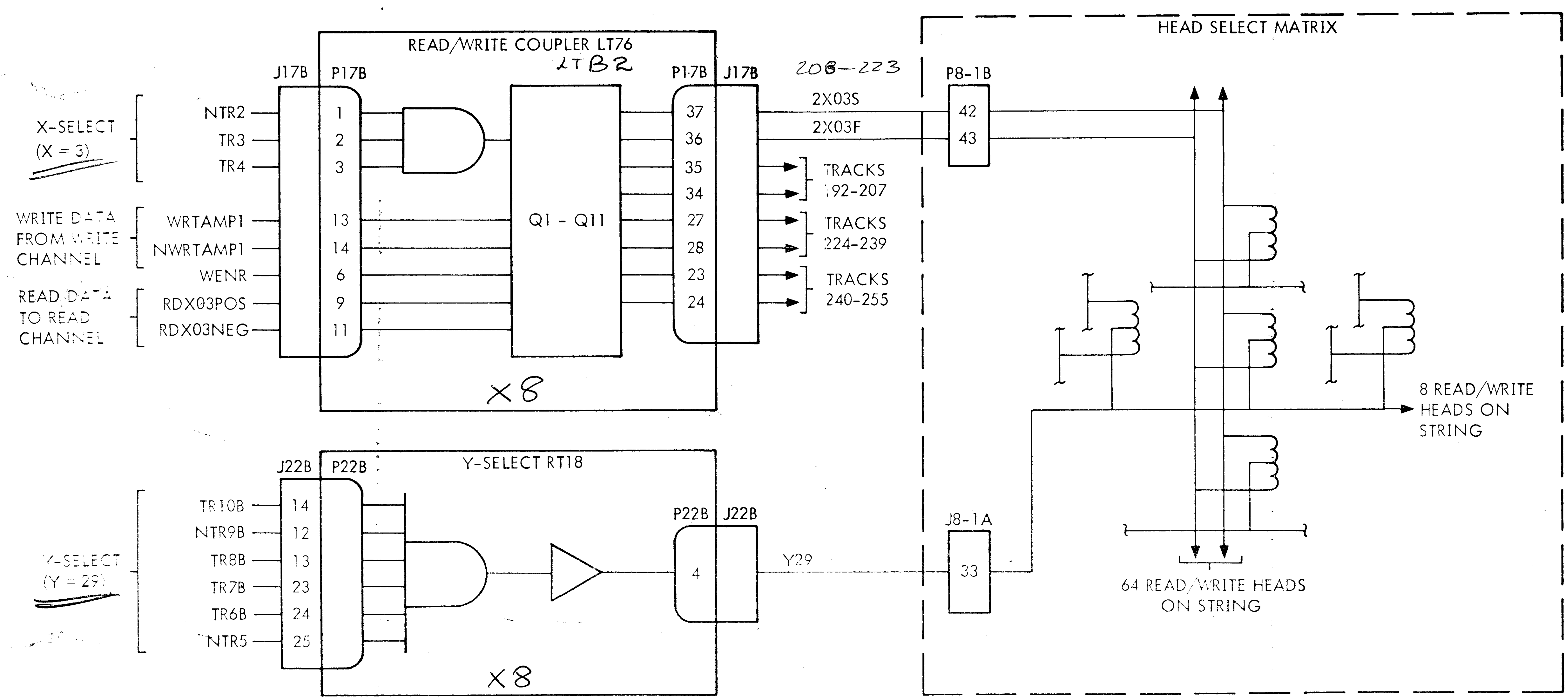


Figure 4-29. Part of Head Selection Matrix (Track 221), Schematic Diagram

901565A. 429

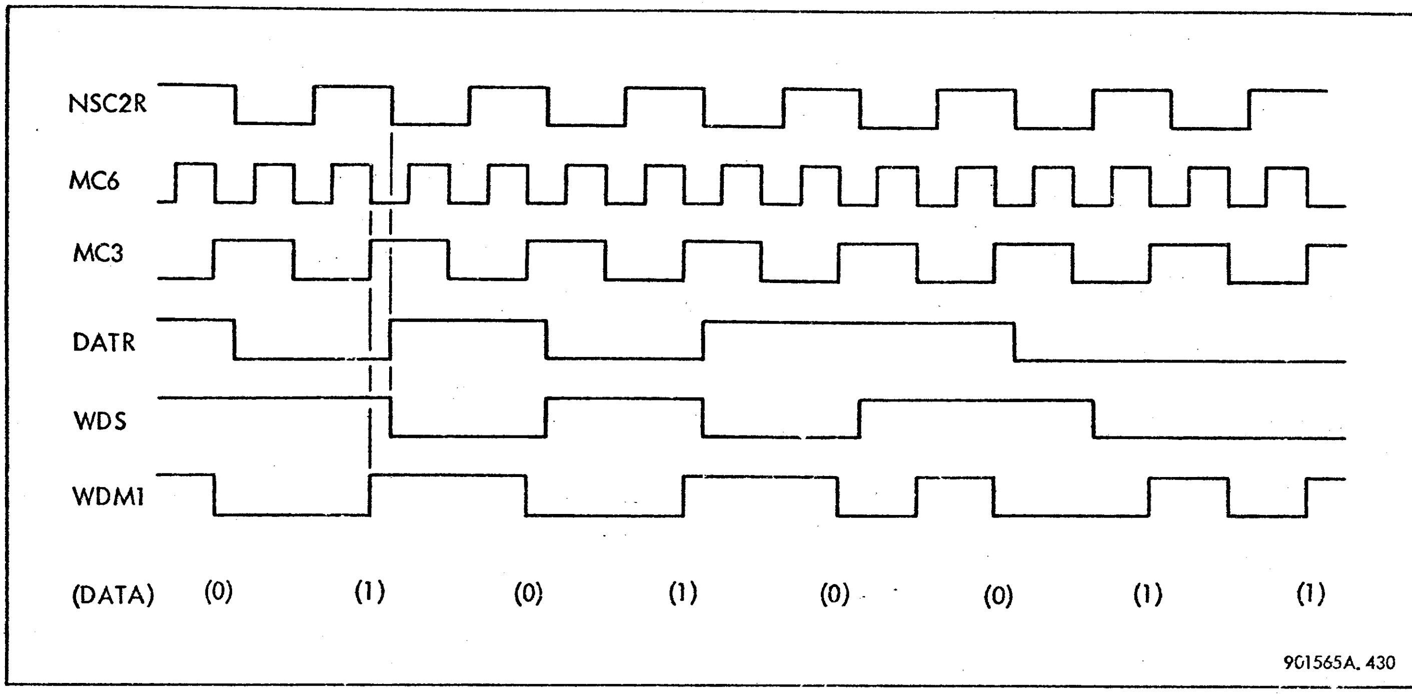


Figure 4-30. Write Signals, Timing Diagram

4-111 LOGICAL SPARING CIRCUITS

The logical sparing circuits (figure 4-33) consist of two BT12 Binary-to-Octal Decoder modules, eight LT105 Spares Selector modules, one RT18 Y-Select module, and associated logic elements. These circuits control the selection of one of the 64 spare read/write heads in place of a XDS-assigned read/write head. Signals TRM1X2, TRM1X3, and TRM1X4 select one of eight LT76 Read/Write Coupler modules, as described in paragraph 4-108. When logical sparing is used, signals SPSEL, SP0, SP1, and SP2 cause one of signals YSP0 through YSP7 to be true, providing a Y-select signal which activates a spare read/write head.

Figures 6-10 through 6-13 indicate the correspondence between the 512 read/write heads and the 512 track addresses as assigned at XDS. If a read/write head fails or if the circuits between the LT76 module and the read/write head fails, one of the 64 spare read/write heads can be assigned to the track address by changing wiring on one of the eight LT105 Spares Selector modules.

If logical sparing is not used, signals NSPSEL, NXSP2, NXSP3, and NXSP4 are true, and signals TRM1X2, TRM1X3, and TRM1X4 are controlled by outputs of track address register flip-flops TR2, TR3, and TR4. Also, a false SPSEL signal inhibits gates in the RT18 module used in the spares select logic, so that all Y-select signals for the spare read/write heads are false. If logical sparing is used, signal SPSEL is true and one of the spare read/write heads is addressed in place of the normally assigned read/write head.

The BT12 modules provide 24 signals which represent all track address register signals in octal notation. Signals X0 through X7 represent the most significant (sixty-fours) digit; signals YM0 through YM7 represent the next most significant (eights) digit; signals YL0 through YL7 represent the least significant (units) digit. A track address for which a spare read/write head is assigned is detected by an LT105 module (figure 4-34).

If logical sparing is not used, each of the eight input gates of the LT105 module is connected to ground, so that signals NSP0, NSP1, NSP2, NSPSEL, and the module identification signal (NMOD1 through NMOD8) are true. When logic sparing is to be used, the ground connection is removed from one input gate, and the address of the track to be spared is encoded at the input gate disconnected from ground. When that track is not addressed, the output signals are all true. When that track is addressed, the signals to the assigned input gates are true, the output of the assigned gate is false, and the LT105 module output signals are as indicated in figure 4-34. Signals NSPSEL, NSP0, NSP1, and NSP2 cause one output of the RT18 module to be true, providing a Y-select signal. The module identification signal generates a combination of signals NXSP2, NXSP3, and NXSP4 that selects one of the LT76 modules. Therefore, one of the 64 spare read/write heads is addressed in place of the initially assigned read/write head. Figure 4-35 illustrates the logic elements involved for sparing track address 221 (octal 335).

4-112 TYPICAL OPERATIONS

Table 4-22 outlines the sequence of EP RAD file operations in response to an SIO command, followed by a sense order, a seek order, and a write order. This sequence of operations is typical. The sense order detects the sector currently

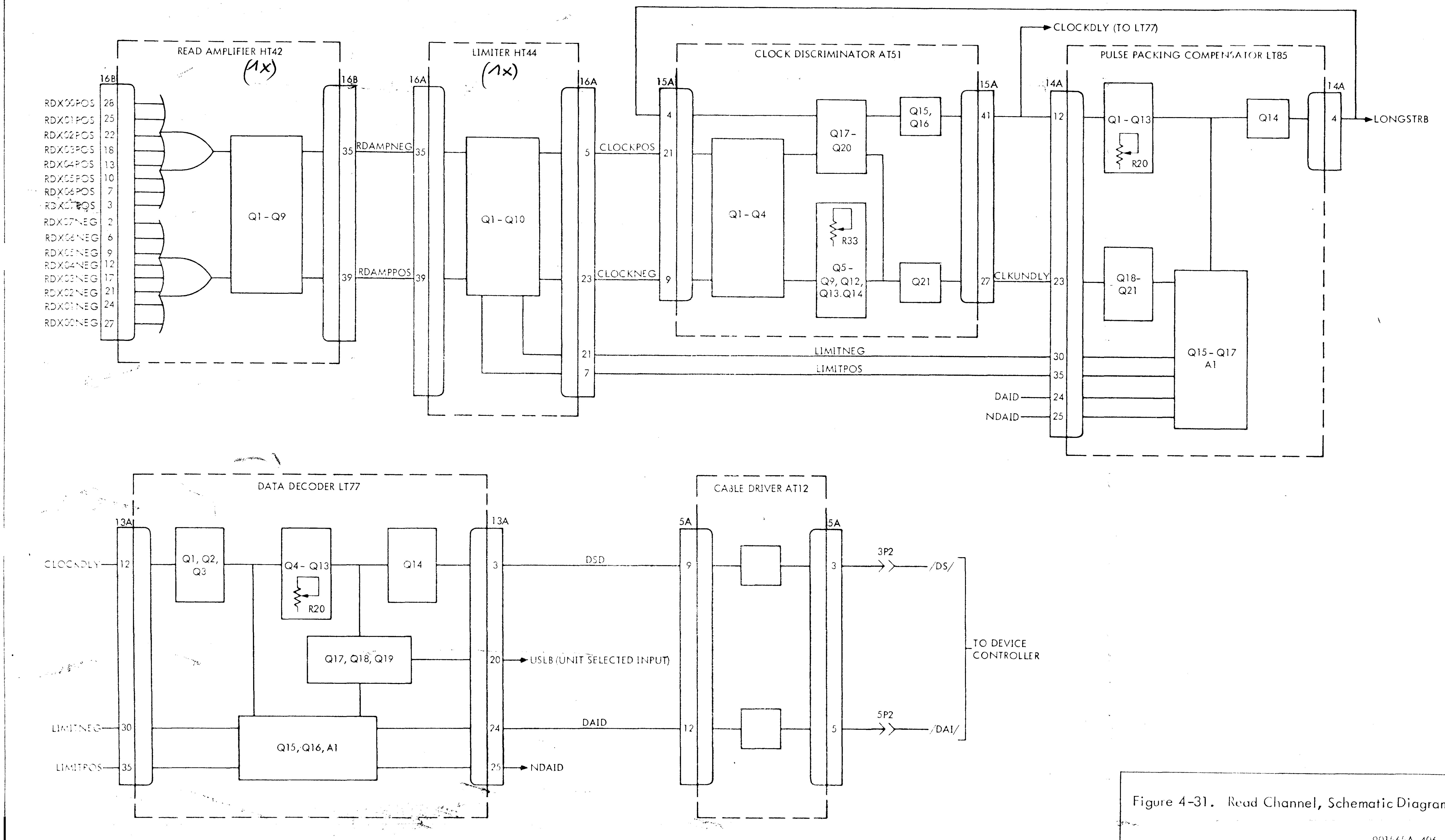


Figure 4-31. Read Channel, Schematic Diagram

901565A. 406

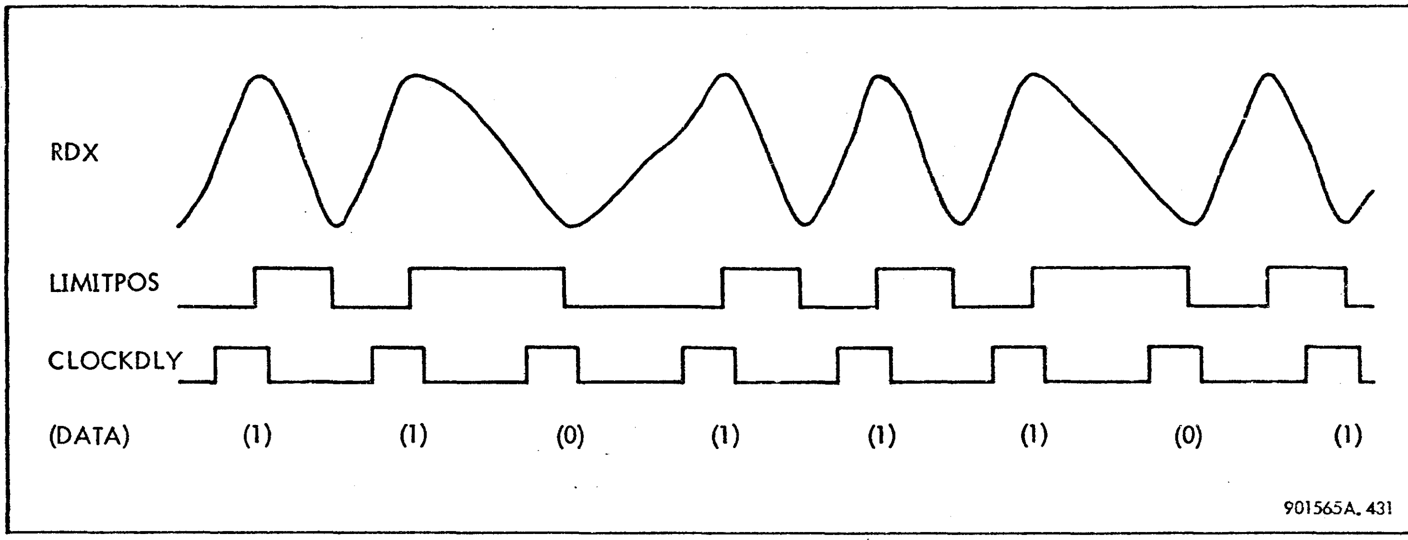


Figure 4-32. Read Signals, Timing Diagram

under the read/write heads of the EP RAD storage unit. The seek order provides a track number and sector number at which execution of the following order is to begin. (A program using this sequence assures minimum delay while waiting for an addressed sector because the available sector is addressed in constructing the seek order.) The write order follows the order which stored the addressed location. The table provides references to paragraphs, phase sequence charts, and illustrations which provide details of the operations outlined. Figure 4-36 shows major elements of the EP RAD controller and can be used with other reference material to review operation.

Table 4-22. Typical Operations of the EP RAD File

Operation	References
The IOP address an SIO command to the EP RAD controller and one of eight (maximum) EP RAD storage units. The SIO command is accepted if: a. The EP RAD controller has priority b. The EP RAD controller and EP RAD storage unit are ready c. No interrupt is pending	Function strobe and function indicators (par. 4-10 and table 4-1) SIO function indicator (par. 4-17) Phase control circuits (par. 4-22) Phase sequence chart (table 4-10) Flow diagram (fig. 4-8)
During the order out service cycle, the sense order code is stored in the order register	Phase sequence chart (table 4-10) Order register (par. 4-31) Order signals (table 4-2) Flow diagram (fig. 4-8) Phase control circuits (par. 4-24)
During the following three data in service cycles, data is transferred to the IOP	Data path (fig. 3-5) Timing diagram (fig. 4-25)

(Continued)

Table 4-22. Typical Operations of the EP RAD File (Cont.)

Operation	References
a. Write protect bit from selection unit and five track address bits from T-register b. Four track address bits from T-register and four sector address bits from S-register c. Four current sector bits from selection unit	Phase sequence chart (table 4-14) Flow diagram (fig. 4-8) Byte counter (par. 4-33) O-register (par. 4-38) K-register (par. 4-57) T-register (par. 4-68) S-register (par. 4-67) Address circuits (par. 4-104) Memory protect circuits (par. 4-106)
During the order in service cycle, command chaining permits the order out service cycle to follow	Phase circuits (par. 4-29) Phase sequence chart (table 4-18) Flow diagram (fig. 4-8)
During the order out service cycle, the seek order code is stored in the order register	Phase sequence chart (table 4-13) Order register (par. 4-31) Order signals (table 4-2) Phase control circuits (par. 4-24) Flow diagram (fig. 4-8)
During the following two data out service cycles, data is transferred from the IOP a. Five bits of track address b. Four bits of track address and four-bit sector address	Data path (fig. 3-4) Timing diagram (fig. 4-26) Phase control circuits (par. 4-26) Flow diagram (fig. 4-8) Phase sequence chart (table 4-15) Byte counter (par. 4-33) I-register (par. 4-37) J-register (par. 4-39) T-register (par. 4-68) S-register (par. 4-67)

(Continued)

Table 4-22. Typical Operations of the EP RAD File (Cont.)

Operation	References
During the order in service cycle, command chaining permits the order out service cycle to follow	Phase circuits (par. 4-29) Phase sequence chart (table 4-18) Flow diagram (fig. 4-8)
During the order out service cycle, the write order code is stored in the order register	Phase sequence chart (table 4-13) Order register (par. 4-31) Order signals (table 4-2) Phase control circuits (par. 4-24) Flow diagram (fig. 4-8)
During execution of a write order, the number of data out service cycles depends upon the number of data bytes to be transmitted and the byte width of the IOP interface. After all data bytes have been transferred, the IOP transmits a count done terminal order	Data path (fig. 3-6) Phase control circuits (par. 4-27) Flow diagram (fig. 4-8) Phase sequence chart (table 4-16) I-register (par. 4-37) JP-register (par. 4-43) J-register (par. 4-39) FAM circuits (par. 4-46) L-register (par. 4-45) KP-register (par. 4-44) K-register (par. 4-57) D-register (par. 4-58) F-register (par. 4-66) Preamble (par. 4-61) Checksum (par. 4-71) Address increment (par. 4-70) Terminal order (table 4-19)
During the order in service cycle, the EP RAD controller disconnects from the IOP	Phase circuits (par. 4-29) Phase sequence chart (table 4-18) Terminal order (table 4-19) Flow diagram (fig. 4-8)

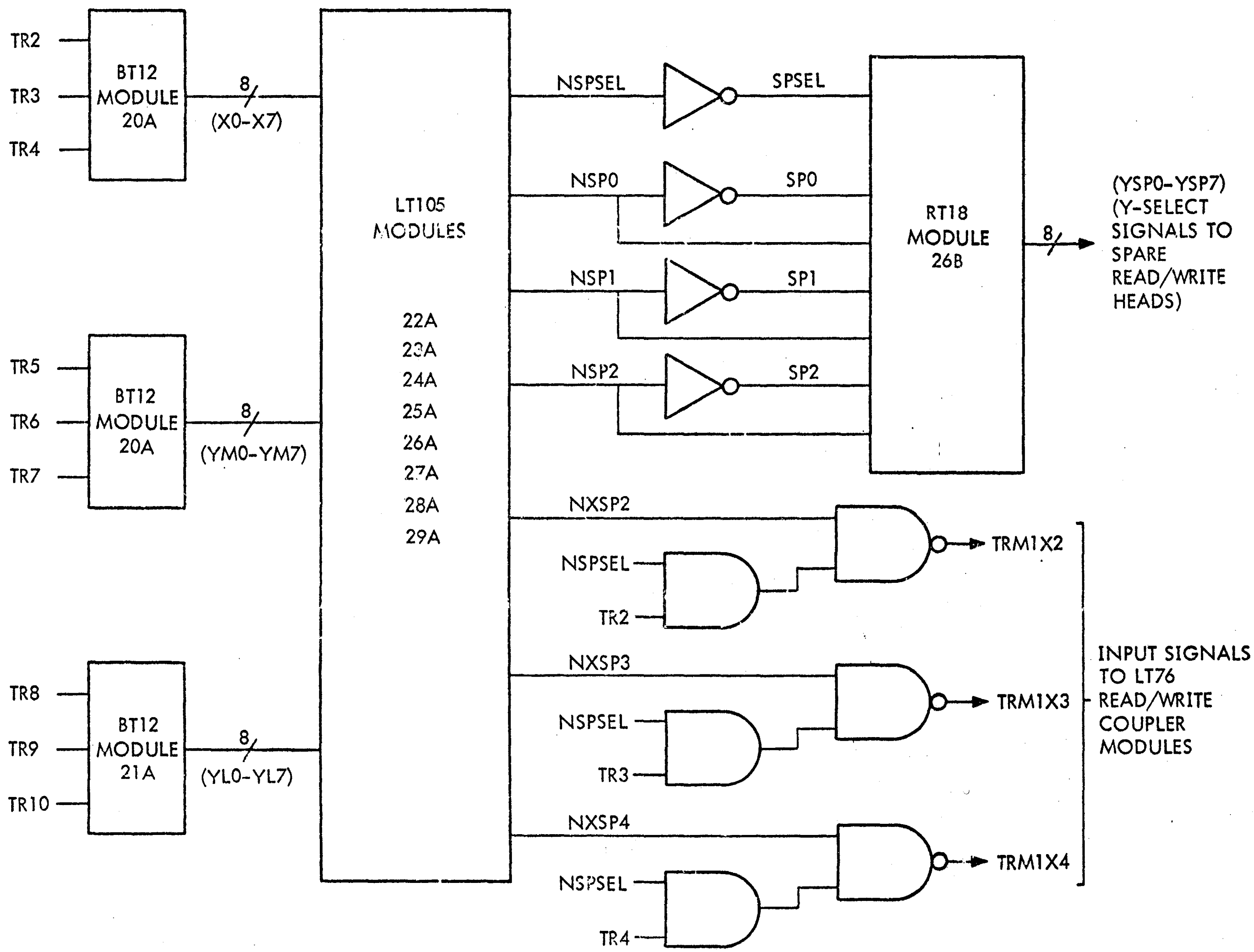
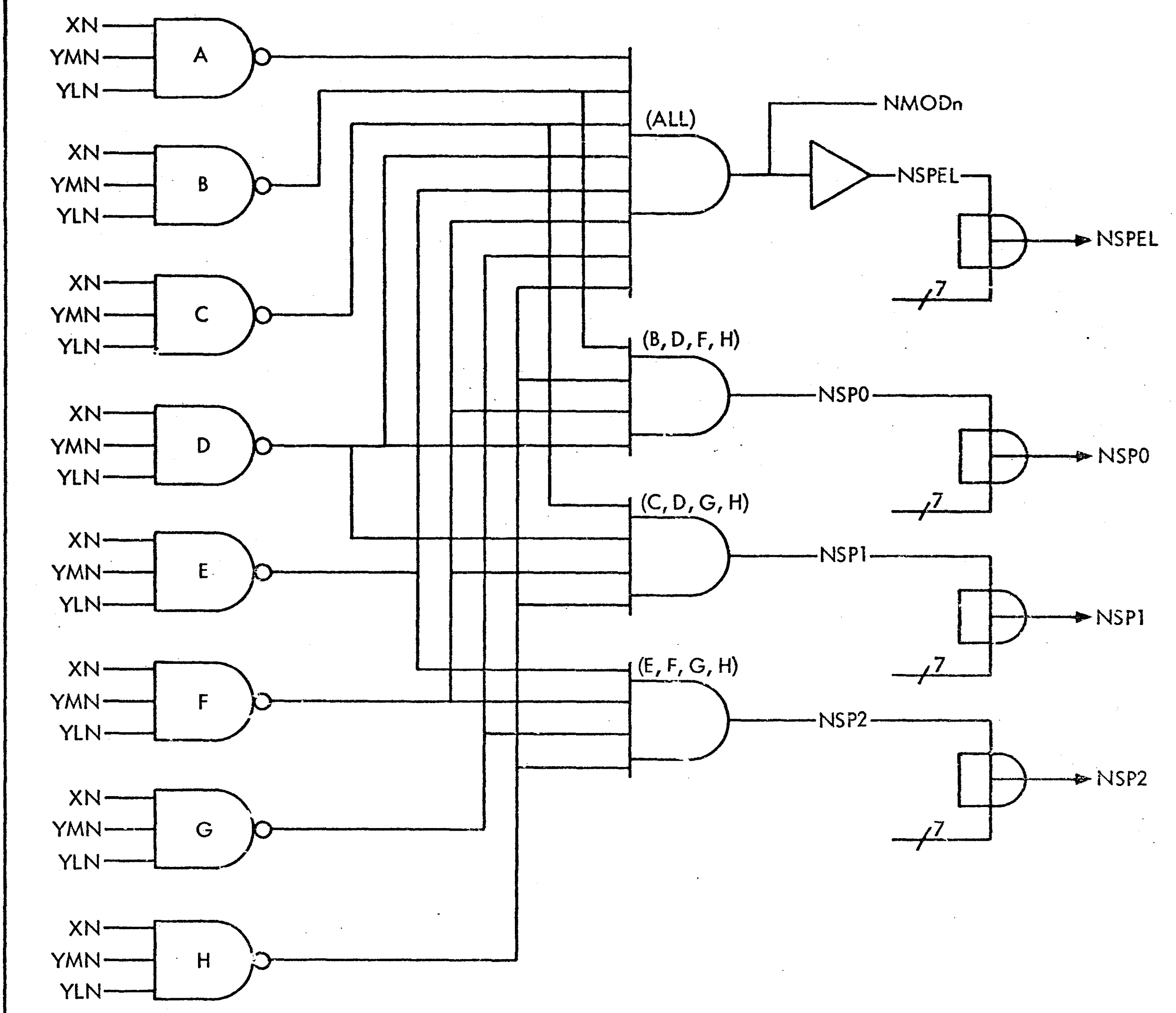


Figure 4-33. Logical Sparing Circuits, Block Diagram

901565A. 432



MODULE SIGNAL	NXSP2	NXSP3	NXSP4
NMOD1	0	0	0
NMOD2	0	0	1
NMOD3	0	1	0
NMOD4	0	1	1
NMOD5	1	0	0
NMOD6	1	0	1
NMOD7	1	1	0
NMOD8	1	1	1

INPUT GATE	NSP0	NSP1	NSP2
A	1	1	1
B	0	1	1
C	1	0	1
D	0	0	1
E	1	1	0
F	0	1	0
G	1	0	0
H	0	0	0

XN = N X 64
YMN = N X 8
YLN = N X 1

901565A. 433

Figure 4-34. LT105 Spares Selector Module, Simplified Logic Diagram

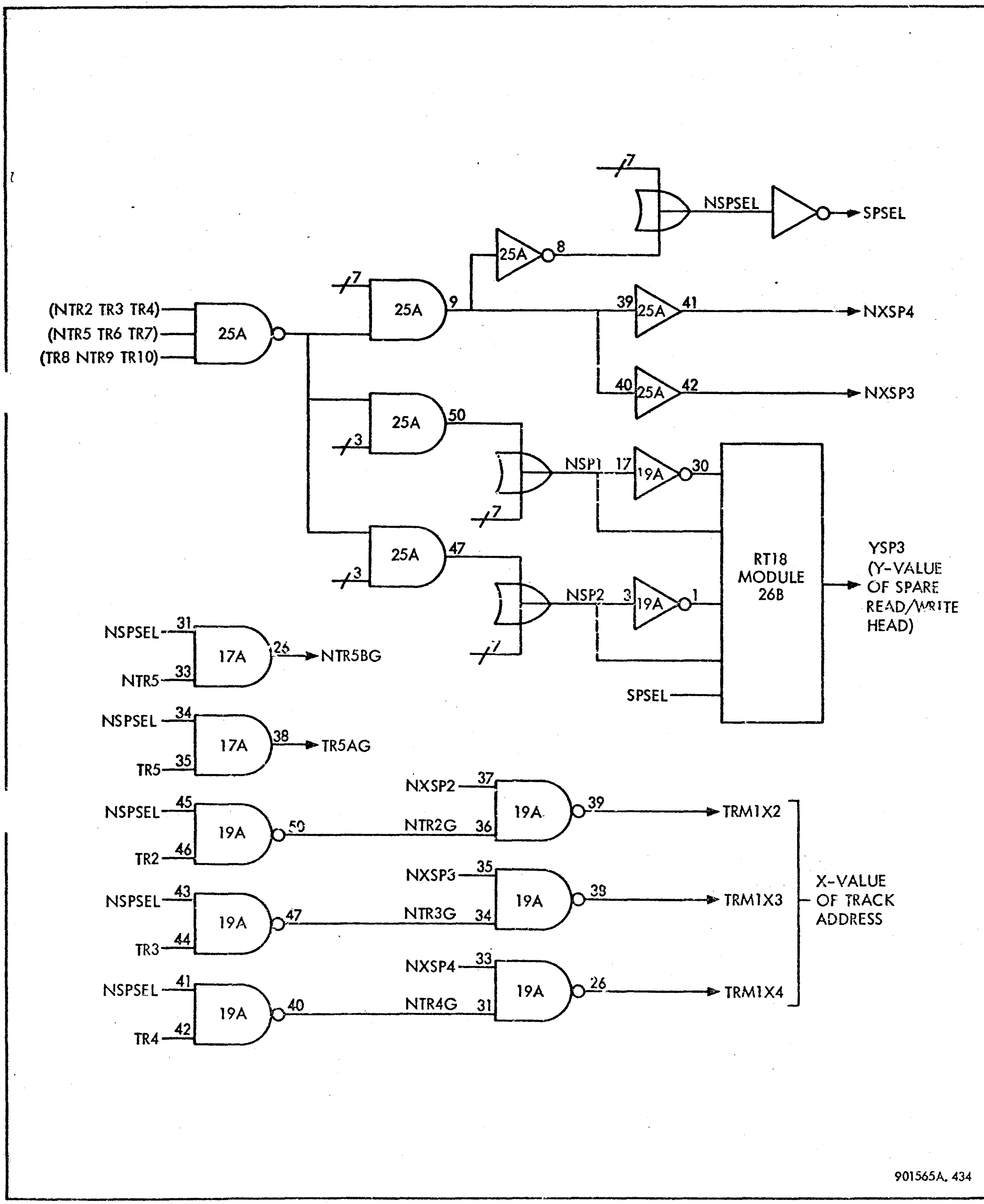


Figure 4-35. Logical Sparing Circuits for Track 221 (Octal 335), Simplified Logic Diagram

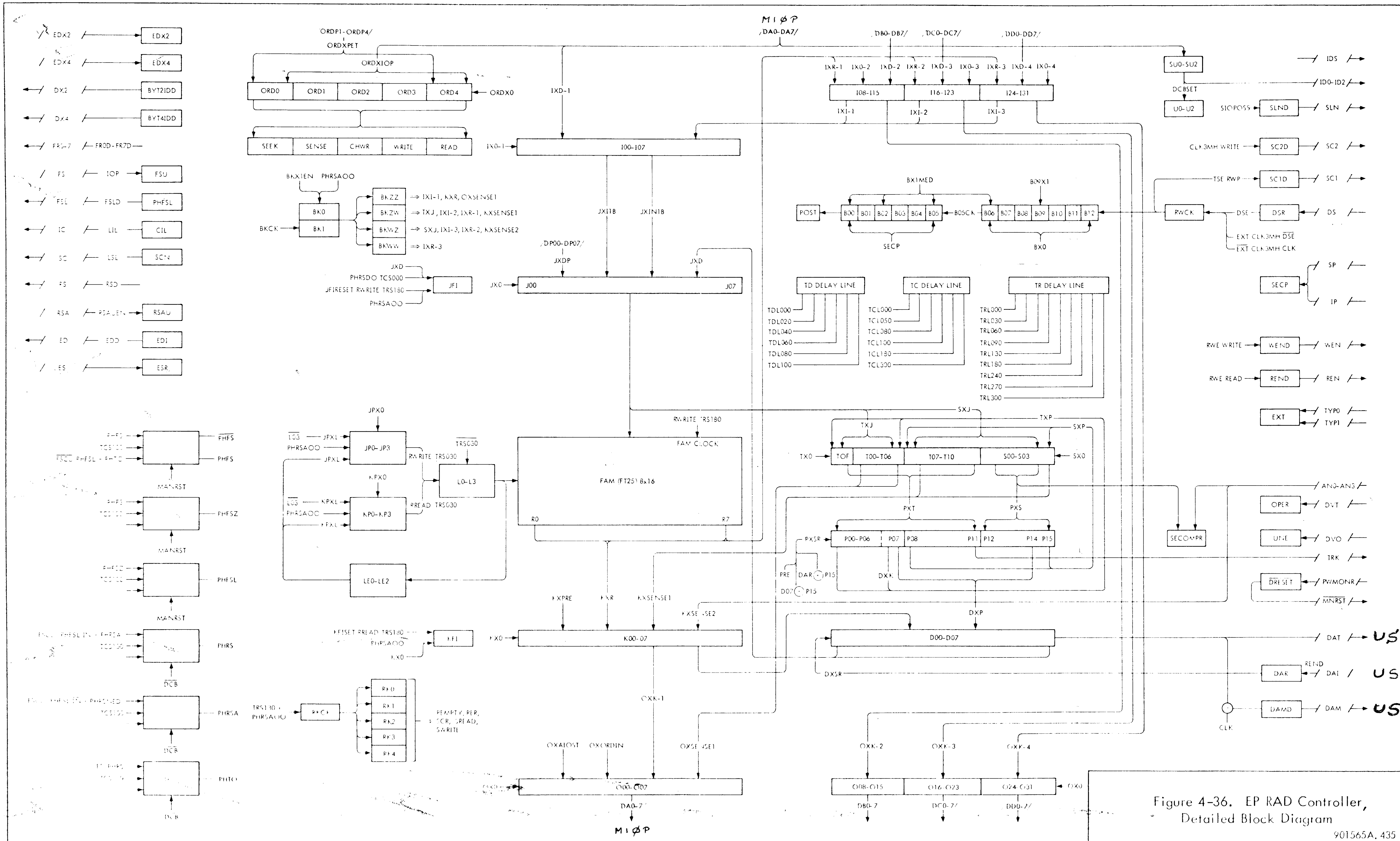


Figure 4-36. EP RAD Controller, Detailed Block Diagram

901565A. 435

SECTION V

LOGIC EQUATIONS AND GLOSSARIES

5-1 GLOSSARIES

Definitions of EP RAD file terms are contained in table 5-1. Table 5-2 contains a glossary of EP RAD controller signals and table 5-3 contains a glossary of EP RAD selection unit signals. All glossaries are in alphanumeric sequence.

5-2 LOGIC EQUATIONS (See tables 4-8 through 4-19.)

Table 5-1. Glossary of EP RAD File Terms

Term	Definition
B-counter	Flip-flops B00 through B12. Counts bits and bytes during execution of read order, write order, or checkwrite order
Byte counter	Flip-flops BK0 and BK1. Used during execution of all orders to count bytes of a service cycle
Condition code	A two-bit code transmitted from the EP RAD file which indicates the status of the EP RAD file to the IOP
Data in service cycle	A service cycle during which data bytes are transferred from the EP RAD file to the IOP
Data out service cycle	A service cycle during which data bytes are transferred from the IOP to the EP RAD file
D-register	Flip-flops D00 through D07. Used during execution of write order or checkwrite order to transform data format from parallel to serial. Used during execution of read order to transform data format from serial to parallel
End data signal	Signal ED, which may be generated by either the IOP or the EP RAD controller and which causes an end to data transfer
End service signal	Signal ES, which is generated only by the IOP and which causes an end of the input/output operation
Fast access memory (FAM) module	FT25 module which stores a maximum of 16 addressable bytes. Receives data inputs from J-register and address inputs from L-register. Outputs of addressed register are designated R00 through R07
FAM read cycle	A cycle of operation of the fast access memory (FAM) circuit, during which a byte is transferred from the addressed location in the FAM module to the K-register or the I-register
FAM write cycle	A cycle of operation of the fast access memory (FAM) circuit during which a byte is transferred from the J-register to the addressed location in the FAM module
Function indicator	A signal that indicates the type of function (AIO, ASC, HIO, TIO, TDV, or SIO)

(Continued)

Table 5-1. Glossary of EP RAD File Terms (Cont.)

Term	Definition
Function response signals	Signals FR0D through FR7D. Signals transmitted to the IOP in response to a function strobe (FSR) and a function indicator signal (AIOR, ASC, SIOR, TDVR, TIOR, HIOR)
Function strobe	A signal /FS/ generated by the IOP to indicate that a response is required of a controller
Indicator signals	Signals IND01 through IND16. Signals sent to the PET to indicate state of EP RAD controller during test
IOP byte signals	Signals DA0R through DA7R, DB0R through DB7R, DC0R through DC7R, and DD0R through DD7R. Transfer data between the controller and IOP. Signals DA0R through DA7R are also used for exchange of orders
I-register	Consists of basic I-register (I00 through I07) and extended I-register (I08 through I31). Stores data from either the FAM circuit or the IOP
JP-register	Buffered latches JP0 through JP3. J-pointer register establishes the FAM module location for input
J-register	Buffered latches J00 through J07. Accepts data from the I-register or D-register for transfer to the FAM circuit
KP-register	Buffered latches KP0 through KP3. K-pointer register, which establishes the FAM module location for output
K-register	Buffered latches K00 through K07. Accepts data from the FAM module for transfer to O-register, I-register, or D-register. During execution of sense order, accepts data from S-register and T-register for transfer to O-register
L-register	Buffered latches L00 through L03, and NL03. Addresses the FAM circuit and causes incrementing of KP-register or JP-register
Order code	A five-bit code indicating the type of order to be executed by the controller (read, write, checkwrite, seek, or sense)
Order in service cycle	A service cycle during which order information is transmitted from the controller to the IOP
Order out service cycle	A service cycle during which an order code is accepted from the IOP
Order register	Flip-flop ORD0 and buffered latches ORD1 through ORD4. Stores order code (seek, sense, read, write, or checkwrite) during execution of order
O-register	Consists of basic O-register (O00 through O07) and extended O-register (O08 through O31). Stores data for transfer to computer memory under control of IOP
PET	Peripheral Equipment Tester Model 7901

(Continued)

Table 5-1. Glossary of EP RAD File Terms (Cont.)

Term	Definition
PET data signals	Signals DP00 through DP07. Signals received from the PET to simulate signals DA0R through DA7R during offline test
Phase control circuits	Flip-flops NPHFS, PHFSZ, PHFSL, PHRS, PHRSA, and PHTO and associated circuits. Establish phase of controller and respond to subcontroller outputs and internal timing and control signals
P-register	Flip-flops P00 through P15. Used to generate checksum during execution of read order, write order, or checkwrite order, and to increment track address and sector address during intersector gap
Read sequence	The sequence of operations (service cycles, data transfers) that takes place during execution of a read order
Request strobe acknowledge signal	RSAR signal which is generated by the IOP to indicate that a data exchange has taken place in response to an RSD signal
Request strobe signal	RSD signal which is generated within the controller to request a data strobe from the IOP, causing a data transfer between the IOP and the controller
RK-counter	Flip-flops RK0 through RK4. Indicates the number of active bytes in the FAM module during execution of read order, write order, or checkwrite order
Sector address	A four-bit code which addresses one of the 12 sectors of each track
Service call signal	SCD signal which is generated by the controller when service is required for data transfer
Service connect	A state of the controller in which data transfers between the IOP and the controller may occur
Service cycle code	A two-bit code indicating the type of service cycle requested by the controller
S-register	Buffered latches S00 through S03, and NS03. Stores sector address
Subcontroller	A standard set of modules which form part of every device controller and which monitor and respond to IOP signals
Terminal order	An optional order following execution of a seek order, sense order, write order, read order, or checkwrite order, which indicates count done, interrupt, channel end, unusual end, or command chaining
Track address	An 11-bit code which addresses one of 512 tracks on the surfaces of the disc file. (Only 9 of the 11 bits are used)
T-register	Buffered latches T00 through T10. Stores track address

(Continued)

Table 5-1. Glossary of EP RAD File Terms (Cont.)

Term	Definition
Unit address	A three-bit code which addresses one of the eight (maximum) EP RAD storage units in an EP RAD file
U-register	Flip-flops U0 through U2. Stores address of EP RAD storage unit
Write sequence	The sequence of operations (service cycles, data transfers) that takes place during execution of a write order

Table 5-2. Glossary of EP RAD Controller Signals

Signal	Definition/Function
/AIO/	Acknowledge input/output function line. Causes highest priority device with interrupt call line raised to send status and address data. Transmitted from IOP to device controller
AIOC	Acknowledge I/O control Enables gating of status for AIO if controller is the highest priority device with interrupt call line raised
AIOM	Acknowledge I/O monitor. Indicates that controller has raised interrupt call line. Enables BSYC and AIOC if true, enables /AVO/ if false
AIOR	Acknowledge I/O receiver
ALT	Flip-flop which alternates a write order with the order encoded in the PET panel switches, and provides for skipping revolutions when writing in single track mode
ALTCK	ALT clock
ALTCKEN	ALT clock enable
ALTORD	PET-generated simulation of ALT
ALTYP2	ALT signal for extended performance (TYP2) use
/AN0/-/AN3/	Sector address (angle) data from selection unit
(AN0R-AN3R)	Sector address receivers
AN1OTYP2	Equivalent to AN1R or EXT
/ASC/	Acknowledge service call function line. Causes highest priority device with service call line raised to send address data
ASCB	Acknowledge service call buffer. Enables setting FSC if the controller is the highest priority device with service call line raised
ASCM	Acknowledge service call monitor. Indicates that the controller has raised a service call. Enables ASCB and BSYC if true; enables AVO if false
ASCR	Acknowledge service call receiver
/AVI/	Available input priority line. Driven by the IOP to the highest priority controller. Passed on by inactive controllers as signal AVO

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
AVIR	Available input receiver
/AVO/	Available output line
AVOD	Available output driver. Driven by any controller that is not addressed or that does not have priority for an interrupt or service call
(B00-B12)	B-counter: (B00-B09) for byte count, (B10-B12) for bit count
B05CK	B05 clock
B09X1	Store a one in B09
BCE	B-counter count enable. Permits (B00-B05) to be incremented by clock signals
BFSD	Buffered function strobe delayed. Gates TIO, SIO, and HIO status to FR0D through FR7D
BIT7RWE	Read/write enable and bit number 7 (binary 111). Times parallel transfer of (D00-D07) ⟶ (J00-J07) or (K00-K07) ⟶ (D00-D07)
BK0-BK1	Byte counter for seek, sense, and expanded interface byte handling
BKWW BKWZ BKZW BKZZ	Byte counter decodes: ZZ = (0, 0); ZW = (0, 1); WZ = (1, 0); WW = (1, 1)
BSYC	Busy control. Gates the address data to FR0D through FR7D for an ASC or AIO when priority recognized, thus defining the busy device for the IOP
BSYCU	Busy clamp latched from PHFSL to PHFS
BX0	Clear B-counter
BX1MED	Preset term for B-counter (used on 360-byte sector medium speed controller)
BYT1ID BYT2ID BYT4ID	Identify width of IOP interface (one, two, or four bytes)
CCH	Command chaining bit in terminal order from IOP
CDN	Count done flip-flop. Causes order in when set by IOP to indicate end of data transfer
CDNPET	PET simulation of CDN flip-flop
CER	Flip-flop set if checkwrite error or if preamble synchronization pattern missed
CERM	Mark flip-flop CER
CERSET	Set flip-flop CER

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
CHWER	Checkwrite error; set CER on noncomparison of disc file data and D-register output during checkwrite operation
CHWEREN	Checkwrite error enable
CIL	Interrupt call flip-flop may be set by IOP during terminal order
CILRST	Reset CIL, true for AIO function indicator
/CL1/	Clock 1 MHz. 1.024 MHz signal from the CPU via the IOP
CL1R	Clock 1 MHz receiver
CLIR	Clock signal from IOP
CLK	Clock divider flip-flop; creates a 1.5 MHz clock when controller is used as medium speed controller
CLK3MH	3 MHz clock
CNTRCLKP	Clock sent to PET to increment its internal counter
CSLI	Service call inhibit. A delay of 100 to 350 ns to allow control logic to settle between disconnecting a service cycle and raising a new service call
CYCEN	Control cycle enable term used in single-phase mode (PET)
CYCLE/C	Control cycle enable; indicates when a phase cycle is possible (TCL delay line)
CYCLER	FAM cycle enable; indicates when FAM cycle is possible (TRL delay line)
(D00-D07)	D-register; the register which shifts data between storage unit and controller
D07SET	Set D07; presets D07 when the T-register and the S-register are to be incremented
/DA0/-/DA7/	Bidirectional communication lines. Signals between the IOP and controller are transferred via these lines. The information carried includes device address, AIO status, orders, terminal orders, operational status bytes during order in, and data byte 1
(DA0D-DA7D)	Data line drivers
(DA0R-DA7R)	Data line receivers
/DAI/	Data signal from storage unit to controller
DAIR	Data receiver
/DAM/	Manchester-encoded data to medium speed RAD storage unit
DAMD	Medium-speed RAD data driver
DAR	Synchronized data flip-flop; set by DAIR and DSR

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
/DAT/	Data output to storage unit from D07
DATA	Data/order flip-flop; set for data, reset for order
DATAIN	Data in signal; true when data sent to IOP (read or sense)
DATAOUT	Data out signal; true when data accepted from IOP (seek, write, or checkwrite)
DATASET	Set flip-flop DATA
/DB0/-/DB7/	Data byte 2 lines (B-lines). Bidirectional lines that carry data for two- or four-byte interface
(DB0D-DB7D)	Data line drivers
(DB0R-DB7R)	Data line receivers
/DC0/-/DC7/	Data byte 3 lines (C-lines). Bidirectional lines carrying data for four-byte interface
(DC0D-DC7D)	Data line drivers
(DC0R-DC7R)	Data line receivers
DCA	Device controller address recognition. Compares (DA0R-DA3R) with (SWA0-SWA3) for address recognition
DCA47	Part of DCA controlled by bits 4 through 7 for single byte controllers. (Not used by EP RAD file)
DCB	Device controller busy flip-flop, set by successful SIO
DCBRST	Reset flip-flop DCB
DCBSET	Set flip-flop DCB
DCL	Start term for TCL delay line
/DD0/-/DD7/	Data byte 4 lines (D-lines). Bidirectional lines carrying data for four-byte interface
(DD0D-DD7D)	Data line drivers
(DD0R-DD7R)	Data line receivers
/DOR/	Data or order indicator line. If false during service cycle, indicates that A-lines contain data; if true during service cycle, indicates that A-lines contain orders. Indicates address recognition for all instructions
DORD	Data or order line driver
DORDEN	DORD enable
(DP00-DP07)	Data lines from PET
DRESET	Device reset, true when a power failure occurs

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
/DS/	Data strobe from selection unit
DSE	Data strobe enable. Gates DSR into RWCK during a read or checkwrite operation
DSEM	Mark flip-flop DSE
DSL	D-register shift left. Used when incrementing T-register and S-register
DSR	Data strobe received
DVBSY	Device busy
/DVO/	Selected device operational signal from selection unit
DVOR	Selected device operational signal receiver
DVSEL	Device selected
/DVT/	Device test signal from selection unit
DVTR	Device test signal receiver
/DX2/	Request for two-byte interface (transfer 16 bits in parallel). False for one- or four-byte interface
/DX4/	Request for four-byte interface (transfer 32 bits in parallel). False for one- or two-byte interface
DXK	Transfer contents of K-register to D-register; (K00-K07) ⟶ (D00-D07)
DXP	Transfer contents of P-register to D-register; (P07-P14) ⟶ (D00-D07)
DXSR	Shift contents of D-register to right
/ED/	End data line. Bidirectional line true when the last data byte is on the line
EDD	End data driver
EDI	EDD gating term, combines all conditions for end data
EDISET3	End data flip-flop
EDR	End data receiver
EDU	End data from IOP or PET
ERSTOP	Error stop switch signal from PET, halts operation on error
EXT	Extended performance operation
FAULT	A fault condition caused by SUN, WPV, or RER

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
FNTP	Simulated function strobe enabled by PET
/FR0/-/FR7/	Function response lines from IOP
(FR0D-FR7D)	Function response line drivers
(FR0R-FR7R)	Function response line receivers
/FS/	Function strobe line. The /FS/ signal from the IOP defines period during which the controller should respond to function indicator or acknowledge service call indicator if it recognizes its address or priority. Used as a clock term for setting or resetting device controller busy flip-flop DCB or for setting FSC
FSC	Service connect flip-flop. Defines the period during which data or orders may be requested and transferred
FSCU	FSC for IOP or PET
FSLD	Function strobe driver
FSP	Offline simulation of function strobe
FSPOCSL	Simulated CSL signal for offline operation
FSPS	Simulated function strobe from PET
FSR	Function strobe receiver
FSU	Function strobe, IOP or PET
GNDxxx	Ground connection (false level)
/HIO/	Halt I/O function line. Causes the controller to terminate the I/O sequence and to return to ready state
HIOP	PET simulation of HIO function indicator
HIOR	Halt I/O receiver
HIOU	HIO function indicator, PET or IOP
/HPI/	High priority interrupt line. When raised, overrides a higher priority device interrupt call. Not presently used in Sigma peripherals
HPID	High priority interrupt driver
HPIL	High priority interrupt latch. Inhibits AIOM, thus preventing a low priority interrupt from responding to an AIO instruction
HPIR	High priority interrupt received
/HPS/	High priority service call line. When raised, overrides any higher priority with a service call raised. Not presently used on Sigma peripherals
HPSD	High priority service call driver

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
HPSL	High priority service latch. Inhibits ASCM, thus preventing a low priority service call from responding to ASC
HPSR	High priority service receiver
(I00-I31)	Incoming data storage buffer (I-register)
/IC/	Interrupt call. Raised by the controller in response to an order modifier or a terminal order (zero byte count, channel end, or unusual end)
ICD	Interrupt call driver
/ID0/-/ID2/	Device address signals from controller to storage units
IN	Input/output control flip-flop; set for input, reset for output
INC	Inhibit calls. Prevents interrupt call or service call when the controller is offline or when controller dc power fails
(IND01-IND16)	Indicator drivers to PET
INDUP	PET indicator select switch signal. Selects upper or lower set of functions to be displayed by (IND01-IND16)
INI	Inhibit input. Permits signal /AVO/ to go true when required, but forces all other signals between IOP and controller false when the controller is offline or when the controller dc power fails
INL	Incorrect length flip-flop. Set if byte count is not a multiple of sector storage, if seek byte count is not two, or if sense byte count is not three
INLEN	Enable set of flip-flop INL
INLM	Mark flip-flop INL
INLSET	Set flip-flop INL
INSET	Set flip-flop IN
IOP	PET signal. True for online, false for offline (during test, IOP true enables monitor mode of PET)
/IOR/	Input/output request. Defines direction for communications on the data lines for service cycle. Defines status for instructions
IORD	Input/output request driver
IORDEN	Enable IORD
/IP/	Index pulse from storage unit
IPR	Index pulse receiver
(IX0-1 - IX0-4)	Clear I-register
IXD-1	Enable transfer of (DA0R-DA7R) ⟶ (I00-I07)

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
IXD-2	Enable transfer of (DB0R-DB7R) ⟶ (I08-I15)
IXD-3	Enable transfer of (DC0R-DC7R) ⟶ (I16-I23)
IXD-4	Enable transfer of (DD0R-DD7R) ⟶ (I24-I31)
IXEN	Extended interface option
IXI-1	Enable transfer of (I08-I15) ⟶ (I00-I07)
IXI-2	Enable transfer of (I16-I23) ⟶ (I00-I07)
IXI-3	Enable transfer of (I24-I31) ⟶ (I00-I07)
IXR-1	Enable transfer of (R00-R07) ⟶ (I08-I15)
IXR-2	Enable transfer of (R00-R07) ⟶ (I16-I23)
IXR-3	Enable transfer of (R00-R07) ⟶ (I24-I31)
(J00-J07)	J-register (input buffer for FAM module)
JFI	J-register filled latch
JFIRESET	Force JFI false
JFIX1	Force JFI true
(JP0-JP3)	J-pointer register (JP-register). Address register for data written into the FAM
JPX0	Clear the JP-register
JPXL	Load the incremented JP address into the JP-register (L00-L03) ⟶ (JP00-JP03)
JX0	Clear the J-register
JXD	Load the contents of the D-register into the J-register: (D00-D07) ⟶ (J00-J07)
JXDP	Load PET data into the J-register
JXI1B	Load contents of I-register into J-register (one-byte interface only)
JXIN1B	Load contents of I-register into J-register (not one-byte interface)
(K00-K07)	K-register. Provides sense data storage, preamble synchronization pattern generation, and functions as FAM module output buffer
KA8	Control latch indicating that FAM module is empty and last byte is in K-register
KFI	K-register filled latch
KFICK	KFI delay flip-flop used for setting rate error flip-flop RER

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
KFID	Latch signal that sets KFICK
KFIDX1	Force KFID true
KFISET	Selects condition for forcing KFI true
KFIX1	Force KFI true
(KP0-KP3)	KP-register (K-pointer register). Address register for data read from the FAM module
KPX0	Clear the KP-register
KPXL	Load the incremented KP address into the KP-register; (L00-L03) ⟶ (KP00-KP03)
KX0	Clear the K-register
KX0EN	Enable KX0
KXPRE	Load the preamble synchronization pattern into the K-register
KXR	Load the addressed FAM byte into the K-register; (R00-R07) ⟶ K00-K07)
KXREN	Enable KXR
KXSENSE1	Load second sense byte into the K-register; (T07-T10) ⟶ (K00-K03), (S00-S03) ⟶ (K04-K07)
KXSENSE2	Load third sense byte into the K-register; (AN0R-AN3R) ⟶ (K04-K07)
(L00-L03)	L-register; address register for FAM module
LASTSEC	PET decode of sector preceding index mark
(LE0-LE2)	Exclusive OR adder used to increment KP-register and KP-register
LIH	Latch interrupt high. Retains the fact that a high priority interrupt has been raised. Enables AIOM
LIL	Latch interrupt low. Retains the fact that a low priority interrupt has been raised. Enables AIOM
LSH	Latch service high. Retains the fact that a high priority service call has been issued. Enables ASCM
LSL	Latch service low. Retains the fact that a low priority service call has been issued. Enables ASCM
MANRST	Manual reset from RSTR (IOP) or from RSTP (PET)
/NMANRST/	Manual reset signal from controller to storage unit
(O00-O31)	O-register; data drivers to IOP
OPER	Device operational flip-flop

(Continued)

Table 5-2. Glossary of EP RAD Controller Signal (Cont.)

Signal	Definition/Function
(ORD0-ORD4)	Order register flip-flop and order register buffered latches
ORDIN	Order in signal
ORDOUT	Order out signal
(ORDP1-ORDP4)	PET order switch signals used to load order register
ORDX0	Clear the order register
ORDXIOP	Load the data line (IOP) into the order register; (DA3R-DA7R) ⟶ (ORD0-ORD4)
ORDXPET	Load the PET data lines into the order register latches; (ORDP1-ORDP4) ⟶ (ORD1-ORD4)
OSCJ	Oscillator jumper for 3 MHz operation
(OX0-1 - OX0-4)	Clear the O-register
OXAIOST	Enable status response to AIO; (RER, SUN, WPV) ⟶ (O00, O02, O03)
(OXK-1 - OXK-4)	Load contents of K-register into O-register (K00-K07) ⟶ (O00-O07) and contents of I-register into O-register. (I08-I31) ⟶ (O08-O31)
OXKEN	Enable OXK
OXORDIN	Enable status signals for order in; (TER, INL, 1, UNE) ⟶ (O00, O01, O03, O04)
OXSENSE1	Load first sense byte into O-register; (TRPR0) ⟶ (O00); (T00-T06) ⟶ (O01-O07)
(P00-P15)	P-register; a two-byte parity register used to generate parity for the storage unit and to increment the T-register and the S-register
P00SET	Set flip-flop P00
P00SETEN	Enable set flip-flop P00
P13LD	Increment sector number from 1011 to 0000
P13LDEN	Enable increment sector number
/PC/	Parity check. Bidirectional line which is raised whenever byte 0 parity (A-line parity) should be checked (not used by EP RAD file)
PCD	Parity check driver
PER	Parity error flip-flop (read operation)
PEREN	Enable set PER
PET	Inverted IOP signal; indicates offline operation

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
PHFS	NPHFS flip-flop in reset state; idle phase, indicates function strobe can be accepted
PHFSL	PHFSL flip-flop; indicates function strobe acknowledge sent to IOP
PHFSCYC	PHFS and CYCLE/C signal true
PHFSDAT	PHFS and DATA signal true
PHFSET	Set flip-flop NPHFS
PHFSLNFN	PHFSL and SCN true (service call)
PHFSTOD	Phase FS of data transfer (PHFSDAT) or phase TO (PHTO)
PHFSZ	PHFSZ flip-flop; delay phase for gathering status of storage unit
PHRS	PHRS flip-flop; RSD is sent to IOP, and FAM cycle is started for previously processed bytes
PHRSA	PHRSA flip-flop; request strobe acknowledge
PHRSADO	PHRSA and data out; (DATA, IN) = (1, 0)
PHRSAOO	PHRSA and order out; (DATA, IN) = (0, 0)
PHRSAORD	PHRSA and order (DATA = 0)
PHRSASET	Set phase flip-flop PHRSA
PHRSDO	Phase PHRS and data out; (DATA, IN) = (1, 0)
PHRSET	Set flip-flop PHRS
PHRSNED	Phase RS and not end data
PHTO	PHTO flip-flop; termination phase used to return to PHFS
POST	Control flip-flop that indicates parity check portion of sector
POSTB89	POST and B08 and B09
PRE	Control flip-flop that identifies preamble portion of sector
PRESET	Set flip-flop PRE
PRST-1, PRST-2	Reset term for P-register
PSPB	Preamble synchronization bytes; true for two byte times during search for preamble synchronization pattern
PSPM	Preamble synchronization pattern missed
PSPR	Preamble synchronization pattern recognized

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
PSPWEN	Preamble synchronization pattern write enable; generates the four-bit preamble synchronization pattern (1100)
PT18S	PT18 switched. Ground for K1 and K2 (INI and INC) on the AT17 module. This term is normally from the PT18 power supply, but may be chassis ground. It is fed via switch S1 (online/offline) on module LT25
/PWRMON/	Power monitor line from selection units
PWRMONR	Power monitor signal from selection unit; true when addressed storage unit power fails
PXS	Load contents of S-register into P-register; (S00-S03) ⟶ (P12-P15)
PXSR-1, PXSR-2	Shift contents of P-register to the right
PXT	Load contents of T-register into P-register; (TOF) ⟶ (P00); (T00-T10) ⟶ (P01-P11)
(R00-R07)	Output of addressed location in fast access memory (FAM) module
RCHW	Read order or checkwrite order
READ	Read order
READRR	Clock signal for FAM read cycle
REMPTY	FAM module (R-register) empty
REND	Read or checkwrite operation and read/write enable
REPEAT	PET continuous cycle switch signal
RER	Rate error flip-flop; indicates storage unit processed information faster than IOP
REREN	Enable set flip-flop RER
RERM	Mark flip-flop RER
RERSET	Set flip-flop RER
RESET	Reset EP RAD controller circuits
(RK0-RK4)	RK-counter; indicates number of active bytes in FAM module. Counts down from 1 1111 when data is written into FAM module; counts up when data is read from FAM module
RKCK	R-counter clock
RREAD-1, RREAD-2, RREAD-4	Control terms true when FAM read cycle has started

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
/RS/	Request strobe. Requests the transfer of data or orders while service connected. One byte, halfword, or word is transferred following each RS. May be used as a clock for gating data or orders into the controller or for changing state of control logic circuits
/RSA/	Request strobe acknowledge. Raised by the IOP to indicate that the data or order transfer is complete. Causes RS to go low
RSAR	Request strobe acknowledge receiver
RSARC	Request strobe acknowledge latch
RSAU	Request strobe acknowledge from IOP or PET
RSAUEN	Enable RSAU for PET
RSD	Request strobe driver
RSET	Request strobe in phase RS
/RST/	I/O reset. Normally resets all control logic in the controller and device. RST is generated by I/O RESET or SYSTEM RESET switches, by a programmable reset for the Sigma 5 or Sigma 7, by the RESET position of the INITIALIZE switch for the Sigma 2, or by the start term as power is applied to the Sigma 2, 5, or 7
RSTP	PET reset pushbutton signal
RWCK	Read/write clock (3 MHz oscillator or data strobe bit rate clock)
RWE	Read/write enable flip-flop; allows data transfer operations to begin
RWERST	Reset flip-flop RWE
RWP	Read/write possible flip-flop; indicates that a data transfer order can be accepted
RWPRST	Reset flip-flop RWP
RWRITE-1 RWRITE-2 RWRITE-4	Control terms true when FAM write cycle has started
(S00-S03)	S-register; contains address of next sector to be operated on by read order or checkwrite order
/SC/	Service call. Raised by the controller to start a data or order service cycle
/SC1/	Track and sector shift clock to storage unit
SC1D	Shift clock driver

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
/SC2/	Data clock to storage unit
SC2D	Data clock driver
SCD	Service call driver
SCN	Service call flip-flop; marked on when service is required and kept in set state when additional service required
SCNMEN	Enable mark flip-flop SCN
SCNREN	Enable reset flip-flop SCN
SCR	Read/write service flip-flop; set or reset when additional bytes can be stored in FAM module during execution of write order or checkwrite order, or read from FAM module during execution of read order
SCRSET	Set flip-flop SCR
SCSET	Inhibits SCRSET if true
SECOMPR	Sector compare; (AN0R-AN3R) matches (S00-S03)
SECP	Sector pulse or index pulse
SECPD	Sector pulse disable flip-flop
SECPDM	Mark flip-flop SECPD
SEEK	Seek order in process
SEKSEND	End signal for seek order or sense order
SEN	Sense flip-flop; indicates sense operation possible
SENSE	Sense order in process
SGLPH	PET single-phase switch signal
SGLPHCK	PET single-phase clock signal
SGLTRKP	PET single-track mode switch signal
/SIO/	Start I/O function indicator. Causes the device controller to go busy when accepted
SIOP	PET SIO function indicator switch signal
SIOPOSS	SIO possible
SIOR	Start input/output receiver
SIOU	SIOP or SIOR
SKSBK	Seek order or sense order with final byte count

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
/SLN/	Select now line to selection units
SLND	Strobe sent to storage unit to connect the storage unit addressed by (SU0D-SU2D)
/SP/	Sector pulse line to selection units
SPE	PET single-phase enable flip-flop
SPR	Sector pulse from storage unit
SREAD	Read cycle from FAM module is pending
SREADEN	Enable SREAD
STSH02	SIO, TIO, HIO status device not busy and operational
STXPEN	Enable SXP and TXP
(SU0D-SU2D)	Storage unit address signals
SUN	Sector unavailable flip-flop (error)
SUNM	Mark flip-flop SUN
SUNSET	Set flip-flop SUN
(SWA0-SWA3)	Device controller address switches located on LT25 module
SWRITE	Write cycle into FAM module is pending
SX0	Clear S-register
SXJ	Load contents of J-register into S-register: (J00-J03) ⟶ (T07-T10), (J04-J07) ⟶ (S00-S03)
SXP	Load contents of P-register into S-register: (P12-P15) ⟶ (S00-S03)
SXPEN	Enable SXP for PET
(T00-T10)	T-register; stores track address
TCLxyz	Phase delay line outputs (xyz = delay in nanoseconds)
TCSxyz	Phase delay line sensor outputs (xyz = delay in nanoseconds)
TDLxyz	D-register delay line outputs (xyz = delay in nanoseconds)
TDT	TDL delay line flip-flop
TDT1, TDT2	Buffered outputs of TDL delay line
TDTSET	Set flip-flop TDT
/TDV/	Test device function indicator line

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
TDVP	PET simulation of TDVR signal
TDVR	Test device receiver
TDVU	TDVR or TDVP
TER	Transmission error signal (CER, PER or RER)
/TIO/	Test I/O function indicator. Tests the I/O system. Status returned is the same as for the HIO and SIO commands
TIOP	PET simulation of TIOR signal
TIOR	Test I/O receiver
TIOU	TIOR or TIOP
TOF	Track overflow bit
TORD	Terminal order
/TRK/	Track address line to selection units
TRKRST	True when PET interval counter equals counter reset switch setting
TRLxyz	TRL delay line outputs (xyz = delay in nanoseconds)
/TRP/	Track protect switch signal from selection unit
TRPR	Track protect switch signal receiver
TRSxyz	TRS delay line sensor outputs (xyz = delay in nanoseconds)
TSE	Track shift enable flip-flop
TSH	Gating term that indicates TIO, SIO, or HIO is for this controller because of address recognized. Used to enable gating of status to (FR0D-FR7D)
TTSH	Gating term that defines the instruction being performed is a TIO, TDV, SIO, or HIO
TX0	Clear the T-register
TXJ	Transfer contents of J-register to T-register: (J01-J07) ⟶ (T00-T06)
TXP	Transfer contents of P-register to T-register: (P01-P07) ⟶ (T00-T06)
/TYP0/, /TYP1/	Storage unit type signals from selection unit
TYP0R, TYP1R	Storage unit type receivers
(U0-U2)	Storage unit address loaded by an SIO operation

(Continued)

Table 5-2. Glossary of EP RAD Controller Signals (Cont.)

Signal	Definition/Function
(UAS0-UAS2)	PET switch signals for storage unit address
UNE	Unusual end flip-flop
WCHW	Write order or checkwrite order in process
/WEN/	Write enable signal to storage unit
WEND	Write enable driver
WIDE	True when wide interface option (32 bits) is used and a write, read, or checkwrite operation is performed
WPRE	Write preamble
WPV	Write protection violation flip-flop (error)
WPVSET	Set flip-flop WPV
WRCH	Write, read, or checkwrite operation in process
WRITE	Write order in process

Table 5-3. Glossary of EP RAD Selection Unit Signals

Signal	Definition/Function
ACSENSE1, ACSENSE2	Power monitor ac inputs. Outputs of 30V transformer in power distribution panel
/AN0/-/AN3/	Sector address signals to EP RAD controller
(AN0D-AN3D)	Sector address signal drivers
AOK	Output of power monitor. When true, indicates that ac and dc power is on
CLKUNDLY	Undelayed clock discriminator output
CLOCKDLY	Delayed clock discriminator output. Used to clock read data flip-flop DAID
CLOCKNEG, CLOCKPOS	Inputs to clock discriminator
/DAI/	Data signal to controller
DAID	Read data flip-flop
/DAT/	Data signal from controller
DATR	Data receiver
/DS/	Data strobe to controller
DSD	Data strobe driver

(Continued)

Table 5-3. Glossary of EP RAD Selection Unit Signals (Cont.)

Signal	Definition/Function
/DVO/	Device operational signal to controller
DVOD	Device operational driver
/DVT/	Device test signal to controller
DVTD	Device test driver
/ID0/-/ID2/	Storage unit address signals from controller
(ID0R-ID2R)	Storage unit address signal receivers
/IP/	Index pulse signal to controller
IPD	Index pulse driver
LIMITNEG, LIMITPOS	Inputs to data decoder
LONGSTROB	Strobe output of pulse packing compensator. If true, extends duration of signal CLOCKDLY
/MANRST/	Manual reset signal from controller
MANRSTR	Manual reset signal receiver
MC3	3 MHz signal divided down from frequency doubler. Used to create Manchester-encoded data
MC6	6 MHz signal output of frequency doubler
(NMOD1-NMOD8)	Module location signals for LT105 Spares Selector modules
PDLY	Power on signal delayed 10 seconds
POS25SENSE	Sense +25V input
POWERON	Power on; indicates that all conditions necessary for operation are present
RDAMPNEG, RDAMPPOS	Outputs of read amplifier
RDX0dNEG, RDX0dPOS	Inputs to read amplifier from read/write couplers. (d = 0, 1, 2, 3, 4, 5, 6, 7)
SAE	Sector amplifier enable
/SC1/	Track address shift strobe. Consists of 11 pulses from controller during intersector gap time
/SC2/	Data strobe from controller

(Continued)

Table 5-3. Glossary of EP RAD Selection Unit Signals (Cont.)

Signal	Definition/Function
SC1R	Track address shift strobe receiver
SC2R	Data strobe receiver
SECT	Sector amplifier output
SECTNEG, SECTPOS	Sector track signals
SEL	Unit selected. True when (ID0-ID2) compare with address switch signals
/SLN/	Select now strobe from controller. Used to set unit select flip-flop USLA
SLNR	Select strobe receiver
/SP/	Sector pulse signal to controller
(SP0-SP2)	Three-bit code that enables read/write head selection signals (YSP0-YSP7) for spare Y-select value
SPD	Sector pulse driver
SPSEL	Spare select signal, true when spare read/write head is addressed
TGn	Outputs of track protect matrix (n = 00, 01, ... 15, 16)
(TR0-TR10)	Track address register
TR5AG, TR5BG	Track address register bit 5. Controls read/write head selection. Disabled when SPSEL is true
/TRK/	Track address bits from controller; read while SC1R is true
TRKR	Track address receiver
(TRM1X2-TRM1X4)	Track address register bits 2, 3, and 4. Represents X-value for selection of normal read/write head or spare read/write head
/TRP/	Track protect signal to controller
TRPD	Track protected signal driver
/TYP0/, /TYP1/	Storage unit type signals to controller
TYP0D, TYP1D	Storage unit type drivers
USLA	Unit select flip-flop. Set if storage unit has been addressed by (ID0-ID2) signals, and SLNR is true
USLB	USLA buffered
WDM1, WDM2	Write data flip-flops. Used to encode data in Manchester form

(Continued)

Table 5-3. Glossary of EP RAD Selection Unit Signals (Cont.)

Signal	Definition/Function
WDS	Synchronized write data flip-flops
/WEN/	Write enable signal from controller
WENR	Write enable signal receiver
WRTAMP1, WRTAMP2	Write amplifier outputs
(X0-X7)	Represents X-value (most significant actual digit of track address) of spared address
(X0B-X7B)	Buffered (X0-X7) signals
(NXSP2-NXSP4)	Represents X-value of selected spare read/write head. Controls (TRM1X2-TRM1X4) if SPSEL is true
(Y00-Y63)	Outputs of Y-select matrix
(YL0-YL7)	Represents least significant octal digit of spared track address (least significant octal digit of Y-value)
(YL0B-YL7B)	Buffered (YL0-YL7) signals
(YM0-YM7)	Represents middle octal digit of spared track address (most significant octal digit of Y-value)
(YM0B-YM7B)	Buffered (YM0-YM7) signals
(YSP0-YSP7)	Y-value of addressed spare read/write head, controlled by (SP0-SP2) and SPSEL

SECTION VI
DRAWINGS

6-1 SCOPE OF SECTION

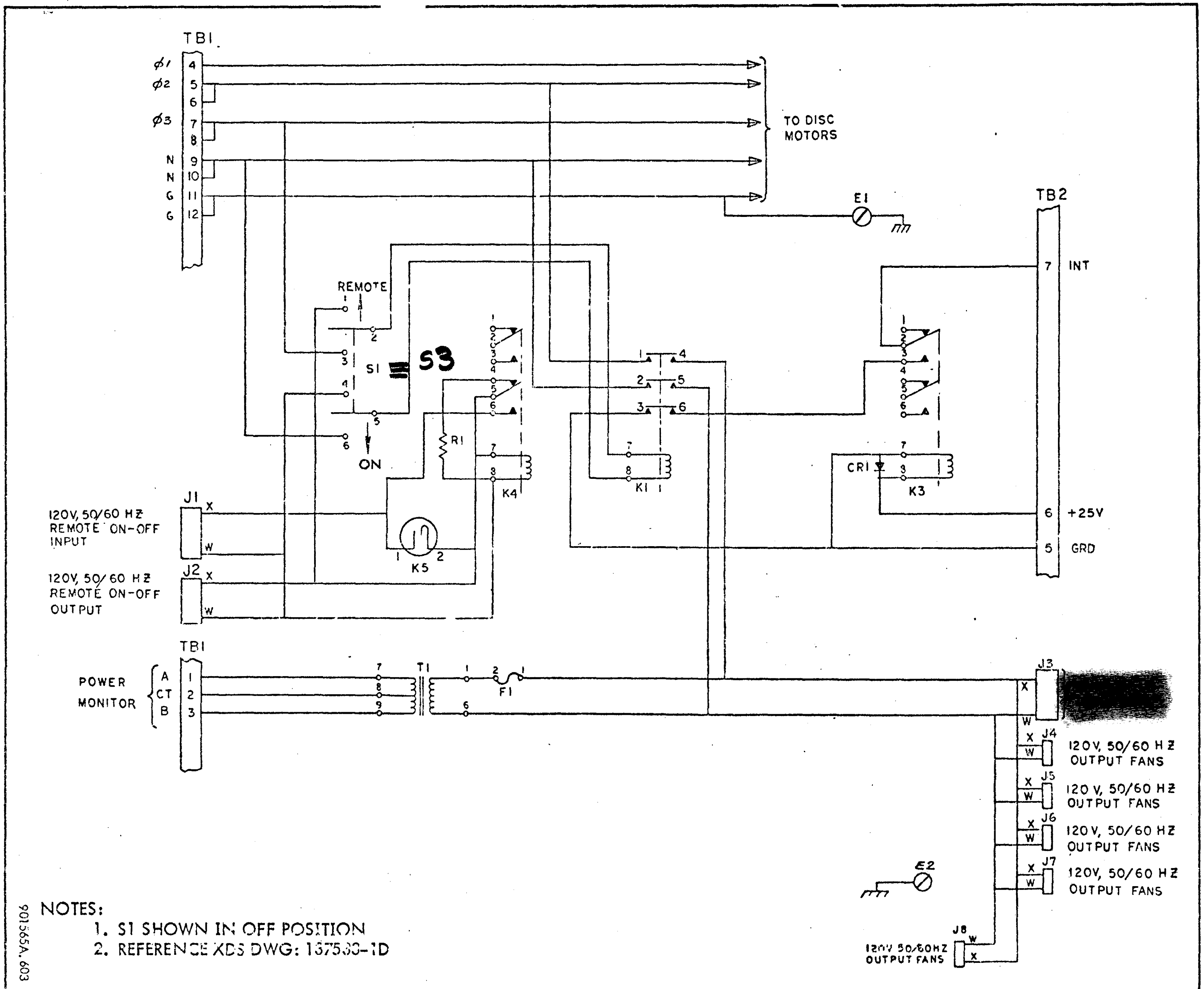
This section contains engineering drawings necessary to support the text of other sections and a list of related engineering data (table 6-1) necessary to maintain the EP RAD File.

6-2 LOCATION OF RELATED TEXT

Figures 6-1 through 6-3 are discussed in paragraphs 4-5. Figure 6-4 is discussed in paragraph 4-2. Figures 6-5 through 6-9, which are logic diagrams of the EP RAD selection unit, are discussed in paragraph 4-103. Figures 6-10 through 6-13, which provide detailed information concerning the read/write head selection matrix, are discussed in paragraph 4-103. Figure 6-14 is a schematic of a modified motor control assembly which is installed on some EP RAD storage units. Figures 6-15 through 6-22 are schematic diagrams of the EP RAD controller, showing differences introduced by the logical sparing option. Differences introduced by logical sparing circuits are discussed in paragraph 4-111.

Table 6-1. List of Related Engineering Data

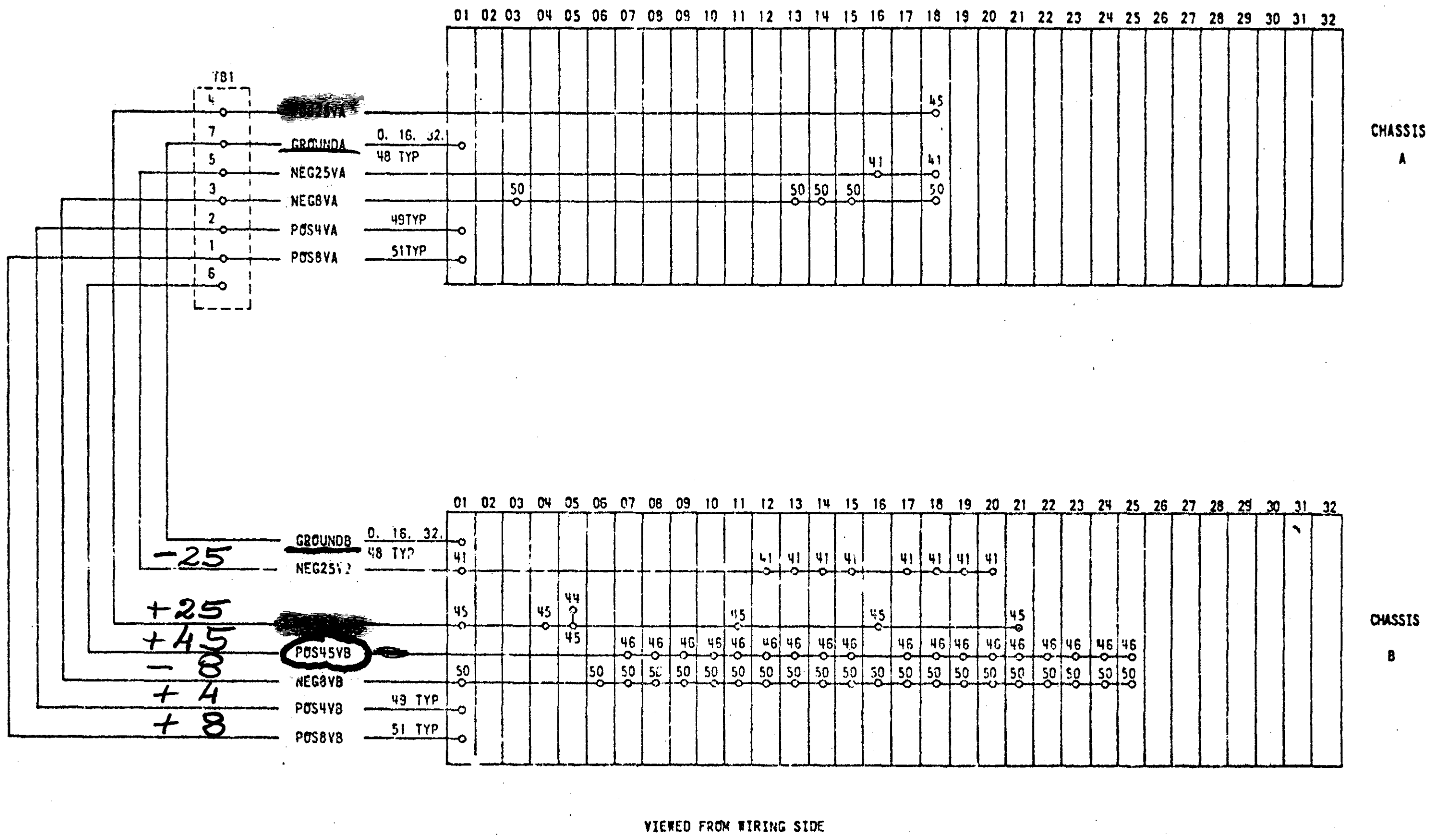
Drawing Number	Title/Content
134029	Wire list, motor control assembly
134293	JT18 operating procedure
137532	Wire list, power distribution panel
139812	Wire list, switch power and connector
139866-202	Wiring data, EP RAD selection unit
139866-502	Wiring data, EP RAD selection unit
139866-902	Wiring data, EP RAD selection unit
146883-002	Logic equations, EP RAD controller
146883-100	List, signal dictionary, EP RAD controller
146884-202	Wiring data, EP RAD controller
146884-502	Wiring data, EP RAD controller
146884-902	Wiring data, EP RAD controller
147608	Wire list, power, EP RAD controller
148784	Wire list, cabinet, power



NOTES:

1. S1 SHOWN IN OFF POSITION
2. REFERENCE XDS DWG: 137563-1D

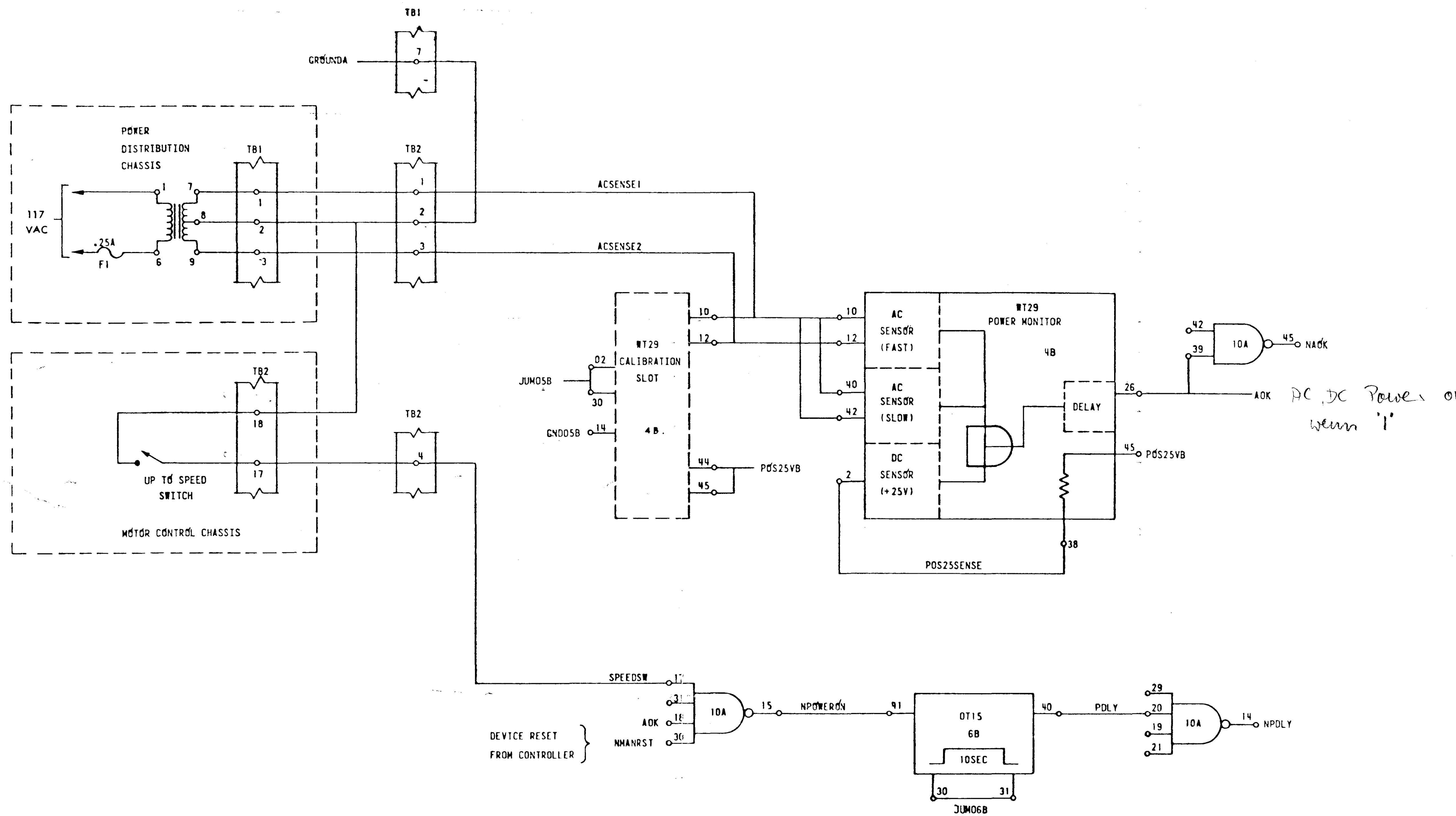
Figure 6-1. Power Distribution Panel, Schematic Diagram



NOTE: REFERENCE XDS DWG: 149337-16A

Figure 6-2. EP RAD Selection Unit, Power Distribution, Chassis Wiring Diagram

901565A.608



NOTE: REFERENCE XDS DWG: 149337-8A

Figure 6-3. EP RAD Selection Unit, Power Fail-Safe Circuits, Logic Diagram

901565A.601

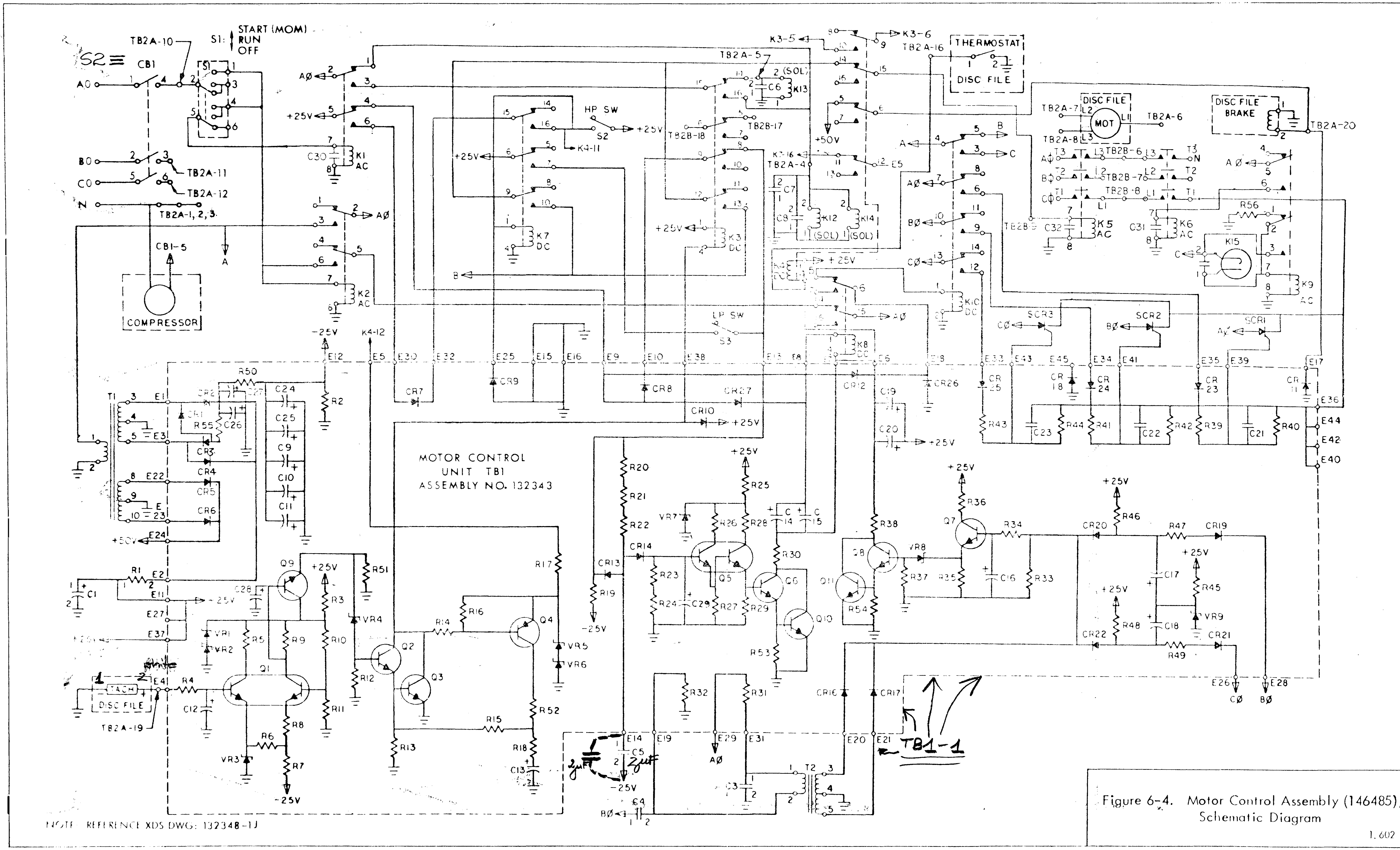
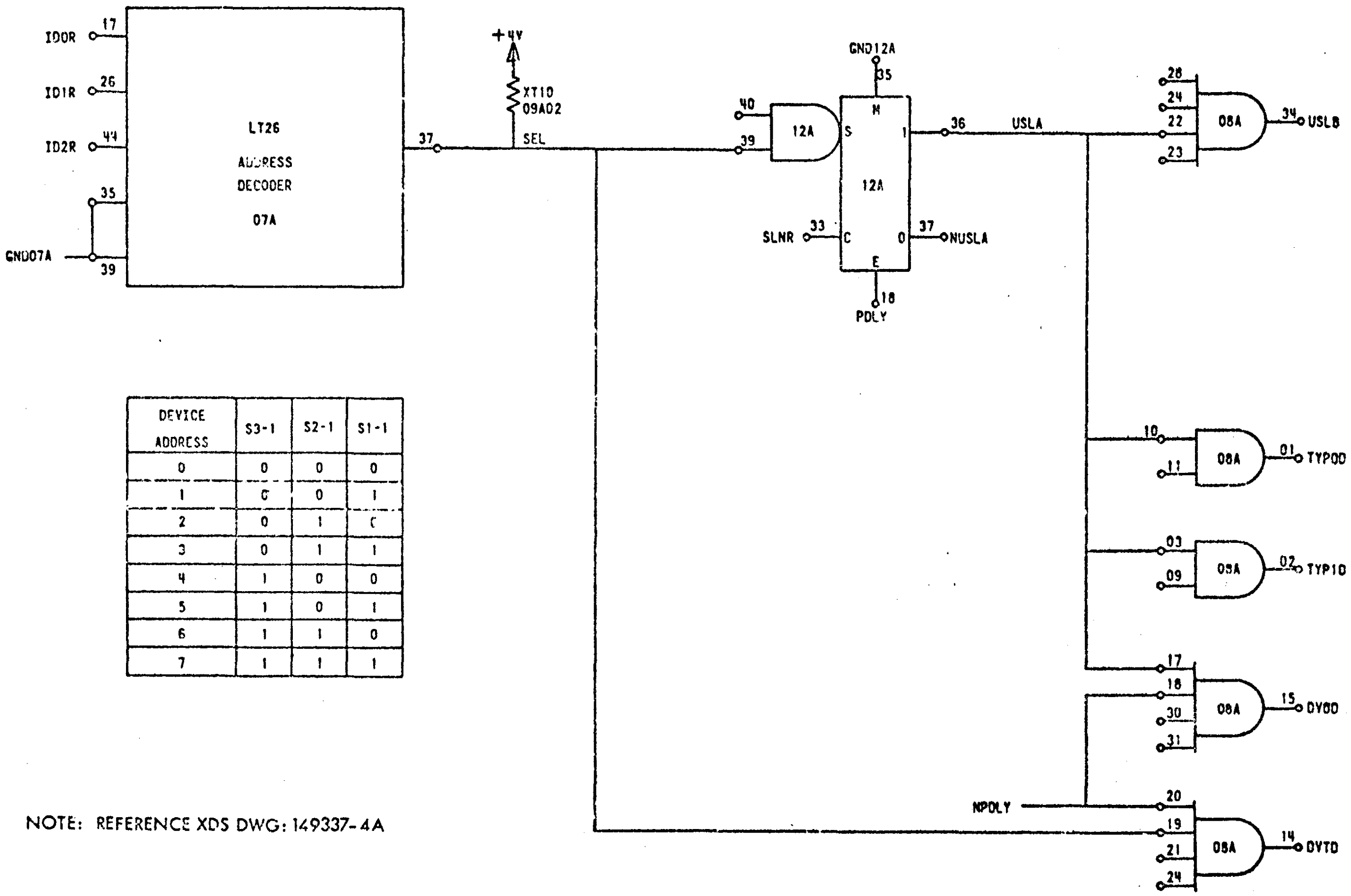


Figure 6-4. Motor Control Assembly (146485), Schematic Diagram

NOTE: REFERENCE XDS DWG: 132348-1J

1.602

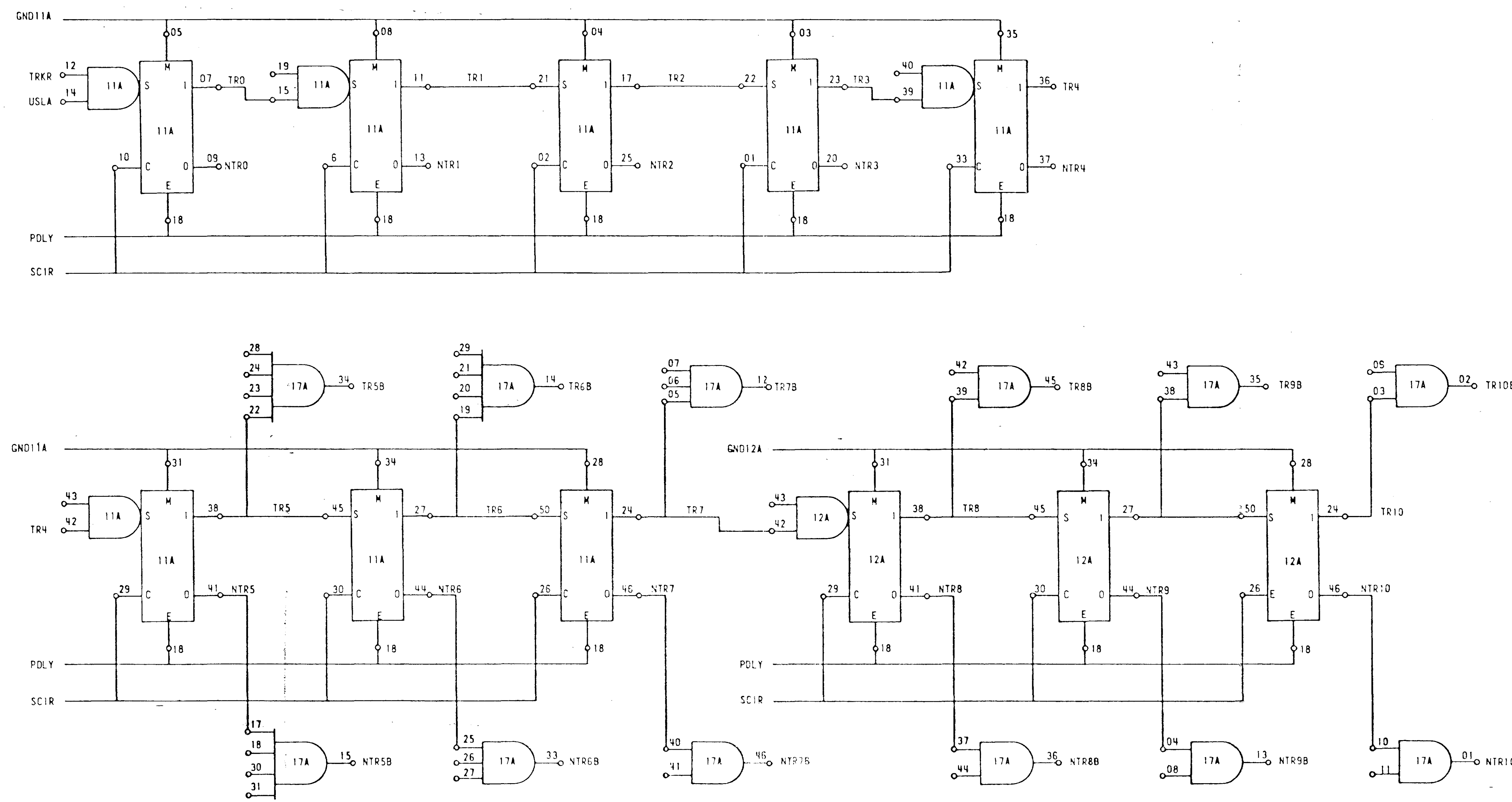


DEVICE ADDRESS	S3-1	S2-1	S1-1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

NOTE: REFERENCE XDS DWG: 149337-4A

901565A. 605

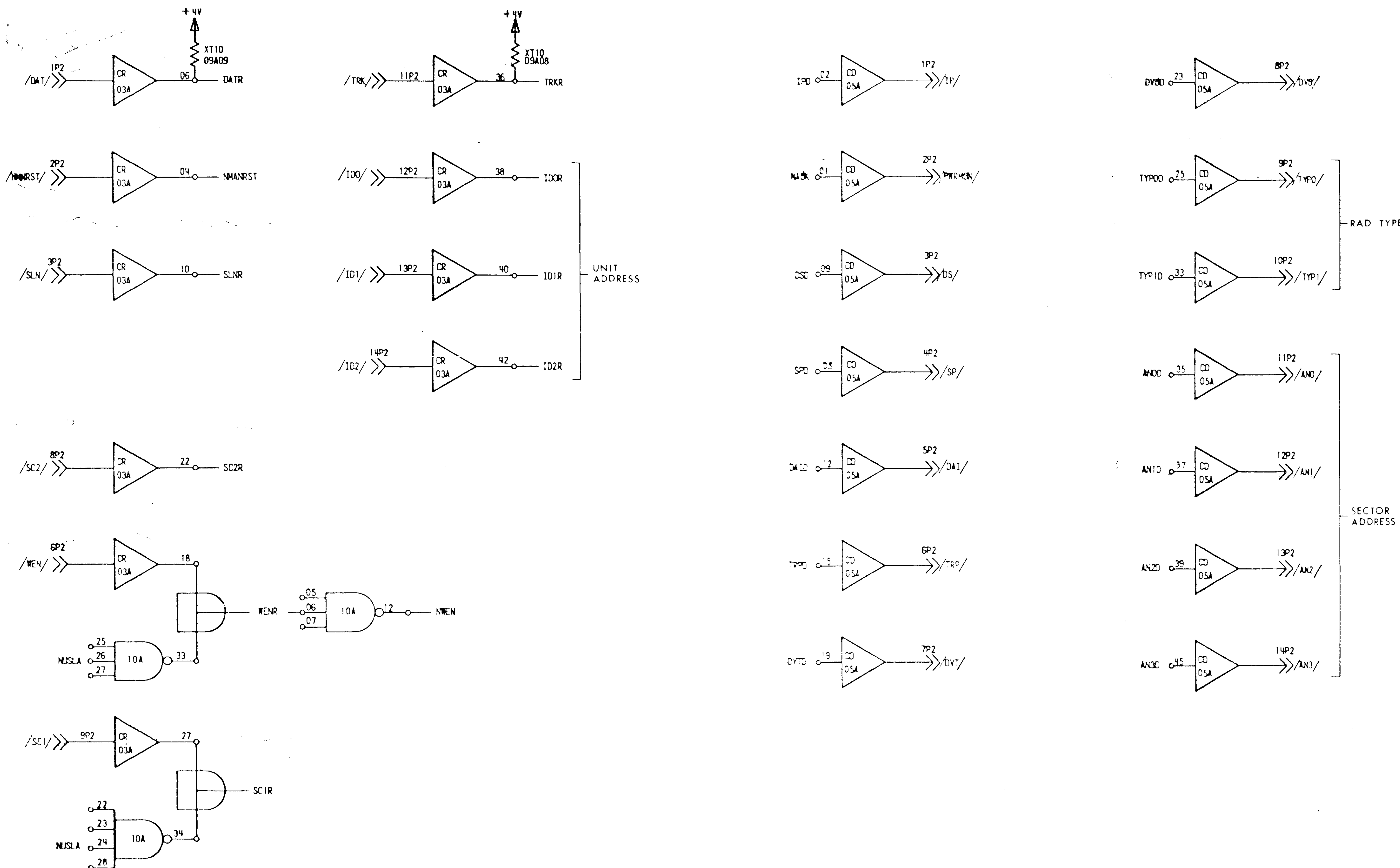
Figure 6-5. EP RAD Selection Unit, Address Circuits, Logic Diagram



NOTE: REFERENCE XDS DWG: 149337-7A

Figure 6-6. EP RAD Selection Unit, Track Register (Without Logical Sparing), Logic Diagram

901565A.606



NOTE: REFERENCE XDS DWG: 149337-3A

Figure 6-7. EP RAD Selection Unit, Input/Output Circuits, Logic Diagram

901565A.607

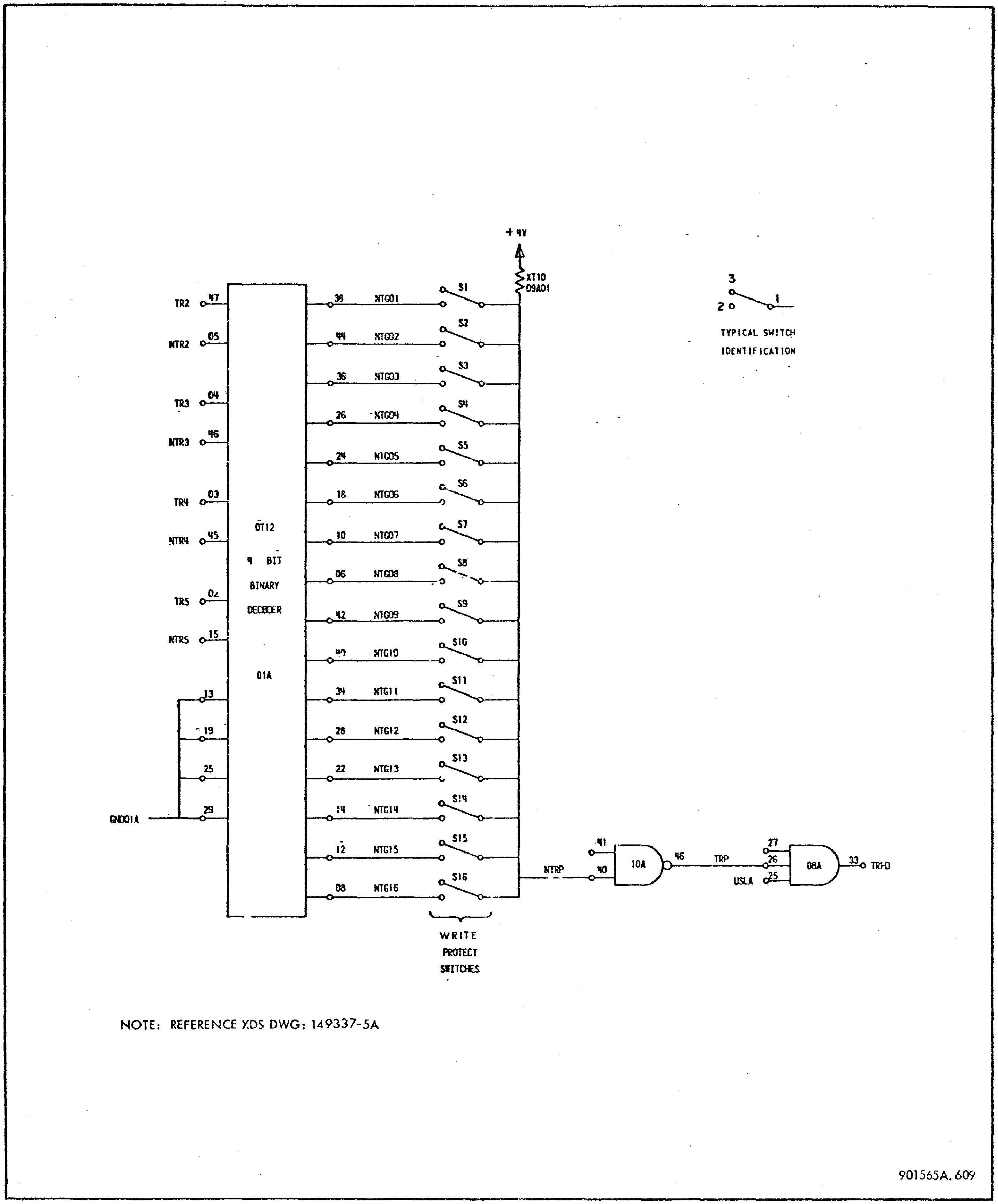
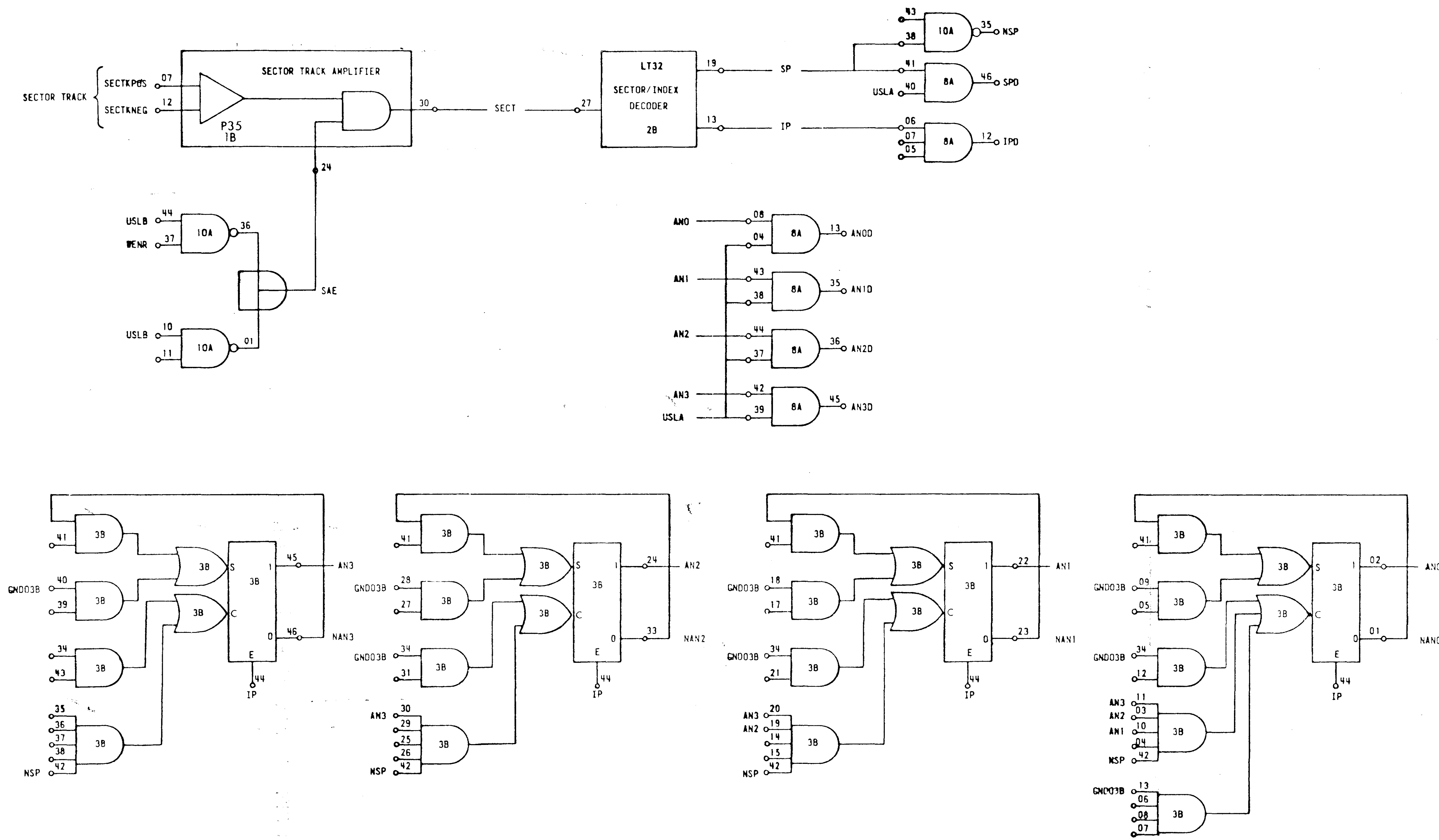


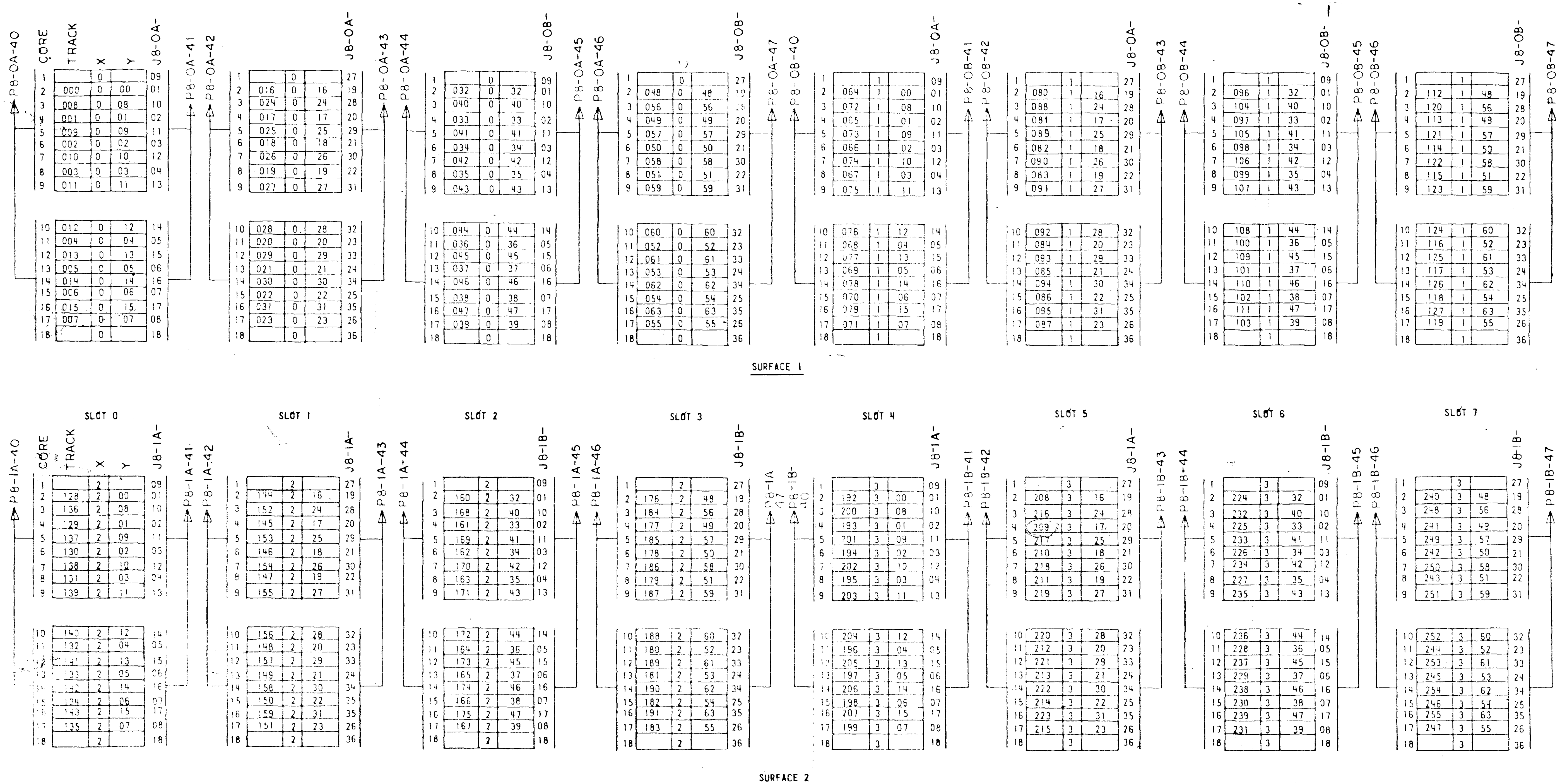
Figure 6-8. EP RAD Selection Unit, Memory Protect Circuits, Logic Diagram



NOTE: REFERENCE XDS DWG: 149337-6A

Figure 6-9. IP RAD Selection Unit, Angle Register, Logic Diagram

901565A.610



NOTE: REFERENCE XDS DWG: 149337-14A

Figure 6-10. Head Location Chart (Sheet 1 of 2)

901565A. 604/1

SURFACE 3

SLOT 0 (J8-2A-40, J8-2A-41)

CORE	TRACK	X	Y	J8-2A-
1		4		09
2	256	4	00	01
3	264	4	08	10
4	257	4	01	02
5	265	4	09	11
6	258	4	02	03
7	266	4	10	12
8	259	4	03	04
9	267	4	11	13
10	268	4	12	14
11	260	4	04	05
12	269	4	13	15
13	261	4	05	06
14	270	4	14	16
15	262	4	06	07
16	271	4	15	17
17	263	4	07	08
18		4		18

SLOT 1 (J8-2A-42, J8-2A-43)

CORE	TRACK	X	Y	J8-2A-
1		4		27
2	272	4	16	19
3	280	4	24	28
4	273	4	17	20
5	281	4	25	29
6	274	4	18	21
7	282	4	26	30
8	275	4	19	22
9	283	4	27	31
10	284	4	28	32
11	276	4	20	23
12	285	4	29	33
13	277	4	21	24
14	286	4	30	34
15	278	4	22	25
16	287	4	31	35
17	279	4	23	26
18		4		36

SLOT 2 (J8-2A-44, J8-2A-45)

CORE	TRACK	X	Y	J8-2B-
1		4		09
2	288	4	32	01
3	296	4	40	10
4	289	4	33	02
5	297	4	41	11
6	290	4	34	03
7	298	4	42	12
8	291	4	35	04
9	299	4	43	13
10	300	4	44	14
11	292	4	36	05
12	301	4	45	15
13	293	4	37	06
14	302	4	46	16
15	294	4	38	07
16	303	4	47	17
17	295	4	39	08
18		4		18

SLOT 3 (J8-2A-46, J8-2A-47)

CORE	TRACK	X	Y	J8-2B-
1		4		27
2	304	4	48	19
3	312	4	56	28
4	305	4	49	20
5	313	4	57	29
6	306	4	50	21
7	314	4	58	30
8	307	4	51	22
9	315	4	59	31
10	316	4	60	32
11	308	4	52	23
12	317	4	61	33
13	309	4	53	24
14	318	4	62	34
15	310	4	54	25
16	319	4	63	35
17	311	4	55	26
18		4		36

SLOT 4 (J8-2B-40, J8-2B-41)

CORE	TRACK	X	Y	J8-2A-
1		5		09
2	[illegible]	5	[illegible]	01
3	[illegible]	5	[illegible]	10
4	[illegible]	5	[illegible]	02
5	[illegible]	5	[illegible]	11
6	[illegible]	5	[illegible]	03
7	[illegible]	5	[illegible]	12
8	[illegible]	5	[illegible]	04
9	[illegible]	5	[illegible]	13
10	[illegible]	5	[illegible]	14
11	[illegible]	5	[illegible]	05
12	[illegible]	5	[illegible]	15
13	[illegible]	5	[illegible]	06
14	[illegible]	5	[illegible]	16
15	[illegible]	5	[illegible]	07
16	[illegible]	5	[illegible]	17
17	[illegible]	5	[illegible]	08
18		5		18

SLOT 5 (J8-2B-42, J8-2B-43)

CORE	TRACK	X	Y	J8-2A-
1		5		27
2	336	5	16	19
3	344	5	24	28
4	337	5	17	20
5	345	5	25	29
6	338	5	18	21
7	346	5	26	30
8	339	5	19	22
9	347	5	27	31
10	348	5	28	32
11	340	5	20	23
12	349	5	29	33
13	341	5	21	24
14	350	5	30	34
15	342	5	22	25
16	351	5	31	35
17	343	5	23	26
18		5		36

SLOT 6 (J8-2B-44, J8-2B-45)

CORE	TRACK	X	Y	J8-2B-
1		5		09
2	352	5	32	01
3	360	5	40	10
4	353	5	33	02
5	361	5	41	11
6	354	5	34	03
7	362	5	42	12
8	355	5	35	04
9	363	5	43	13
10	364	5	44	14
11	356	5	36	05
12	365	5	45	15
13	357	5	37	06
14	366	5	46	16
15	358	5	38	07
16	367	5	47	17
17	359	5	39	08
18		5		18

SLOT 7 (J8-2B-46, J8-2B-47)

CORE	TRACK	X	Y	J8-2B-
1		5		27
2	368	5	48	19
3	376	5	56	28
4	369	5	49	20
5	377	5	57	29
6	370	5	50	21
7	378	5	58	30
8	371	5	51	22
9	379	5	59	31
10	380	5	60	32
11	372	5	52	23
12	381	5	61	33
13	373	5	53	24
14	382	5	62	34
15	374	5	54	25
16	383	5	63	35
17	375	5	55	26
18		5		36

SURFACE 4

SLOT 0 (J8-3A-40, J8-3A-41)

CORE	TRACK	X	Y	J8-3A-
1		6		09
2	384	6	00	01
3	392	6	08	10
4	385	6	01	02
5	393	6	09	11
6	386	6	02	03
7	394	6	10	12
8	387	6	03	04
9	395	6	11	13
10	396	6	12	14
11	388	6	04	05
12	397	6	13	15
13	389	6	05	06
14	398	6	14	16
15	390	6	06	07
16	399	6	15	17
17	391	6	07	08
18		6		18

SLOT 1 (J8-3A-42, J8-3A-43)

CORE	TRACK	X	Y	J8-3A-
1		6		27
2	400	6	16	19
3	408	6	24	28
4	401	6	17	20
5	409	6	25	29
6	402	6	18	21
7	410	6	26	30
8	403	6	19	22
9	411	6	27	31
10	412	6	28	32
11	404	6	20	23
12	413	6	29	33
13	405	6	21	24
14	414	6	30	34
15	406	6	22	25
16	415	6	31	35
17	407	6	23	26
18		6		36

SLOT 2 (J8-3A-44, J8-3A-45)

CORE	TRACK	X	Y	J8-3B-
1		6		09
2	416	6	32	01
3	424	6	40	10
4	417	6	33	02
5	425	6	41	11
6	418	6	34	03
7	426	6	42	12
8	419	6	35	04
9	427	6	43	13
10	428	6	44	14
11	420	6	36	05
12	429	6	45	15
13	421	6	37	06
14	430	6	46	16
15	422	6	38	07
16	431	6	47	17
17	423	6	39	08
18		6		18

SLOT 3 (J8-3A-46, J8-3A-47)

CORE	TRACK	X	Y	J8-3B-
1		6		27
2	432	6	48	19
3	440	6	56	28
4	433	6	49	20
5	441	6	57	29
6	434	6	50	21
7	442	6	58	30
8	435	6	51	22
9	443	6	59	31
10	444	6	60	32
11	436	6	52	23
12	445	6	61	33
13	437	6	53	24
14	446	6	62	34
15	438	6	54	25
16	447	6	63	35
17	439	6	55	26
18		6		36

SLOT 4 (J8-3B-40, J8-3B-41)

CORE	TRACK	X	Y	J8-3A-
1		7		09
2	[illegible]	7	[illegible]	01
3	[illegible]	7	[illegible]	10
4	[illegible]	7	[illegible]	02
5	[illegible]	7	[illegible]	[illegible]
6	[illegible]	7	[illegible]	03
7	[illegible]	7	[illegible]	12
8	[illegible]	7	[illegible]	04
9	[illegible]	7	[illegible]	13
10	[illegible]	7	[illegible]	14
11	[illegible]	7	[illegible]	05
12	[illegible]	7	[illegible]	15
13	[illegible]	7	[illegible]	06
14	[illegible]	7	[illegible]	16
15	[illegible]	7	[illegible]	07
16	[illegible]	7	[illegible]	17
17	[illegible]	7	[illegible]	08
18		7		18

SLOT 5 (J8-3B-42, J8-3B-43)

CORE	TRACK	X	Y	J8-3A-
1		7		27
2	464	7	16	19
3	472	7	24	28
4	465	7	17	20
5	473	7	25	29
6	466	7	18	21
7	474	7	26	30
8	467	7	19	22
9	475	7	27	31
10	476	7	28	32
11	468	7	20	23
12	477	7	29	33
13	469	7	21	24
14	478	7	30	34
15	470	7	22	25
16	479	7	31	35
17	471	7	23	26
18		7		36

SLOT 6 (J8-3B-44, J8-3B-45)

CORE	TRACK	X	Y	J8-3B-
1		7		09
2	480	7	32	01
3	488	7	40	10
4	481	7	33	02
5	489	7	41	11
6	482	7	34	03
7	490	7	42	12
8	483	7	35	04
9	491	7	43	13
10	492	7	44	14
11	484	7	36	05
12	493	7	45	15
13	485	7	37	06
14	494	7	46	16
15	486	7	38	07
16	495	7	47	17
17	487	7	39	08
18		7		18

SLOT 7 (J8-3B-46, J8-3B-47)

CORE	TRACK	X	Y	J8-3B-
1		7		27
2	496	7	48	19
3	504	7	56	28
4	497	7	49	20
5	505	7	57	29
6	498	7	50	21
7	506	7	58	30
8	499	7	51	22
9	507	7	59	31
10	508	7	60	32
11	500	7	52	23
12	509	7	61	33
13	501	7	53	24
14	510	7	62	34
15	502	7	54	25
16	511	7	63	35
17	503	7	55	26
18		7		36

NOTE: REFERENCE XDS DWG: 149337-A15

Figure 6-10. Head Location Chart (Sheet 2 of 2)

901565A.604/2

TRACK

Y SELECT	00 - 31 / 64 - 95	128 - 159 / 192 - 223	256 - 287 / 320 - 351	384 - 415 / 448 - 479
Y00	0A - 01	1A - 01	2A - 01	3A - 01
Y01	- 02	- 02	- 02	- 02
Y02	- 03	- 03	- 03	- 03
Y03	- 04	- 04	- 04	- 04
Y04	- 05	- 05	- 05	- 05
Y05	- 06	- 06	- 06	- 06
Y06	- 07	- 07	- 07	- 07
Y07	- 08	- 08	- 08	- 08
Y08	- 10	- 10	- 10	- 10
Y09	- 11	- 11	- 11	- 11
Y10	- 12	- 12	- 12	- 12
Y11	- 13	- 13	- 13	- 13
Y12	- 14	- 14	- 14	- 14
Y13	- 15	- 15	- 15	- 15
Y14	- 16	- 16	- 16	- 16
Y15	- 17	- 17	- 17	- 17
Y16	- 19	- 19	- 19	- 19
Y17	- 20	- 20	- 20	- 20
Y18	- 21	- 21	- 21	- 21
Y19	- 22	- 22	- 22	- 22
Y20	- 23	- 23	- 23	- 23
Y21	- 24	- 24	- 24	- 24
Y22	- 25	- 25	- 25	- 25
Y23	- 26	- 26	- 26	- 26
Y24	- 28	- 28	- 28	- 28
Y25	- 29	- 29	- 29	- 29
Y26	- 30	- 30	- 30	- 30
Y27	- 31	- 31	- 31	- 31
Y28	- 32	- 32	- 32	- 32
Y29	- 33	- 33	- 33	- 33
Y30	- 34	- 34	- 34	- 34
Y31	0A - 35	1A - 35	2A - 35	3A - 35

TRACK

Y SELECT	32 - 63 / 96 - 127	160 - 191 / 224 - 255	288 - 319 / 352 - 383	416 - 447 / 480 - 511
Y32	0B - 01	1B - 01	2B - 01	3B - 01
Y33	- 02	- 02	- 02	- 02
Y34	- 03	- 03	- 03	- 03
Y35	- 04	- 04	- 04	- 04
Y36	- 05	- 05	- 05	- 05
Y37	- 06	- 06	- 06	- 06
Y38	- 07	- 07	- 07	- 07
Y39	- 08	- 08	- 08	- 08
Y40	- 10	- 10	- 10	- 10
Y41	- 11	- 11	- 11	- 11
Y42	- 12	- 12	- 12	- 12
Y43	- 13	- 13	- 13	- 13
Y44	- 14	- 14	- 14	- 14
Y45	- 15	- 15	- 15	- 15
Y46	- 16	- 16	- 16	- 16
Y47	- 17	- 17	- 17	- 17
Y48	- 19	- 19	- 19	- 19
Y49	- 20	- 20	- 20	- 20
Y50	- 21	- 21	- 21	- 21
Y51	- 22	- 22	- 22	- 22
Y52	- 23	- 23	- 23	- 23
Y53	- 24	- 24	- 24	- 24
Y54	- 25	- 25	- 25	- 25
Y55	- 26	- 26	- 26	- 26
Y56	- 28	- 28	- 28	- 28
Y57	- 29	- 29	- 29	- 29
Y58	- 30	- 30	- 30	- 30
Y59	- 31	- 31	- 31	- 31
Y60	- 32	- 32	- 32	- 32
Y61	- 33	- 33	- 33	- 33
Y62	- 34	- 34	- 34	- 34
Y63	0B - 35	1B - 35	2B - 35	3B - 35

SPARE CENTER TAPS

TRACKS 00-127	0A - 09, - 18, - 27, 0A - 36
	0B - 09, - 18, - 27, 0B - 36
TRACKS 128-255	1A - 09, - 18, - 27, 1A - 36
	1B - 09, - 18, - 27, 1B - 36
TRACKS 256-383	2A - 09, - 18, - 27, 2A - 35
	2B - 09, - 18, - 27, 2B - 36
TRACKS 384-511	3A - 09, - 18, - 27, 3A - 36
	3B - 09, - 18, - 27, 3B - 36

NOTE: REFERENCE XDS DWG: 149337-12A

901565A.611

Figure 6-11. Head Centertap Chart

INPUT

PIN	25B	24B	23B	22B	10B	09B	08B	07B	Gate
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10	36
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9	
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10	05
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9	
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR5B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10	38
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9	
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10	06
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9	
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10	35
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9	
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10	04
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9	
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10	37
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9	
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10	07
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9	
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8	
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7	
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6	
25	NTR5B	NTR5B	NTR5B	NTR5	TR5B	TR5B	TR5B	TR5	

OUTPUT

Gate	25B	24B	23B	22B	10B	09B	08B	07B
36	Y00	Y08	Y16	Y24	Y32	Y40	Y48	Y56
05	Y01	Y09	Y17	Y25	Y33	Y41	Y49	Y57
38	Y02	Y10	Y18	Y26	Y34	Y42	Y50	Y58
06	Y03	Y11	Y19	Y27	Y35	Y43	Y51	Y59
35	Y04	Y12	Y20	Y28	Y36	Y44	Y52	Y60
04	Y05	Y13	Y21	Y29	Y37	Y45	Y53	Y51
37	Y06	Y14	Y22	Y30	Y38	Y46	Y54	Y62
07	Y07	Y15	Y23	Y31	Y39	Y47	Y55	Y53

NOTE: REFERENCE XDS DWG: 149337-11A

901565A.612

Figure 6-12. Y-Select Location Chart (Without Logical Sparing)

LTB2

LT76 MODULE	SELECT INPUT	SELECT PIN	WRITE AMP PIN	WRITE AMP INPUT	READ OUTPUT	READ PIN	START/FINISH PIN	START/FINISH OUTPUT	TRACK	CONNECTOR PIN
20B	NTR2 NTR3 NTR4 WENR	01 02 03 06	13 14	WRTAMP1 NWRTAMP1	RDX00POS RDX00NEG	09 11	35 34 37 36 27 28 23 24	1X00S 1X00F 2X00S 2X00F 3X00S 3X00F 4X00S 4X00F	00-15 16-31 32-47 48-63	P8-0A-40 41 42 43 44 45 46 P8-0A-47
19B	NTR2 NTR3 TR4 WENR	01 02 03 06	13 14	WRTAMP1 NWRTAMP1	RDX01POS RDX01NEG	09 11	35 34 37 36 27 28 23 24	1X01S 1X01F 2X01S 2X01F 3X01S 3X01F 4X01S 4X01F	64-79 80-95 96-111 112-127	P8-0B-40 -41 -42 -43 -44 -45 -46 P8-0B-47
18B	NTR2 TR3 NTR4 WENR	01 02 03 06	13 14	WRTAMP1 NWRTAMP1	RDX02POS RDX02NEG	09 11	35 34 37 36 27 28 23 24	1X02S 1X02F 2X02S 2X02F 3X02S 3X02F 4X02S 4X02F	128-143 144-159 160-175 176-191	P8-1A-40 -41 -42 -43 -44 -45 -46 P8-1A-47
17B	NTR2 TR3 TR4 WENR	01 02 03 06	13 14	WRTAMP1 NWRTAMP1	RDX03POS RDX03NEG	09 11	35 34 37 36 27 28 23 24	1X03S 1X03F 2X03S 2X03F 3X03S 3X03F 4X03S 4X03F	192-207 208-223 224-239 240-255	P8-1B-40 -41 -42 -43 -44 -45 -46 P8-1B-47
15B	TR2 NTR3 NTR4 WENR	01 02 03 06	13 14	WRTAMP2 NWRTAMP2	RDX04POS RDX04NEG	09 11	35 34 37 36 27 28 23 24	1X04S 1X04F 2X04S 2X04F 3X04S 3X04F 4X04S 4X04F	256-271 272-287 288-303 304-319	P8-2A-40 -41 -42 -43 -44 -45 -46 P8-2A-47
14B	TR2 NTR3 TR4 WENR	01 02 03 06	13 14	WRTAMP2 NWRTAMP2	RDX05POS RDX05NEG	09 11	35 34 37 36 27 28 23 24	1X05S 1X05F 2X05S 2X05F 3X05S 3X05F 4X05S 4X05F	320-335 336-351 352-367 368-383	P8-2B-40 -41 -42 -43 -44 -45 -46 P8-2B-47
13B	TR2 TR3 NTR4 WENR	01 02 03 06	13 14	WRTAMP2 NWRTAMP2	RDX06POS RDX06NEG	09 11	35 34 37 36 27 28 23 24	1X06S 1X06F 2X06S 2X06F 3X06S 3X06F 4X06S 4X06F	384-399 400-415 416-431 432-447	P8-3A-40 -41 -42 -43 -44 -45 -46 P8-3A-47
12B	TR2 TR3 TR4 WENR	01 02 03 06	13 14	WRTAMP2 NWRTAMP2	RDX07POS RDX07NEG	09 11	35 34 37 36 27 28 23 24	1X07S 1X07F 2X07S 2X07F 3X07S 3X07F 4X07S 4X07F	448-463 464-479 480-495 496-511	P8-3B-40 -41 -42 -43 -44 -45 -46 P8-3B-47

NOTE: REFERENCE XDS DWG: 149337-13A

901565A.613

Figure 6-13. Input/Output and Start/Finish Location Chart (Without Logical Sparing)

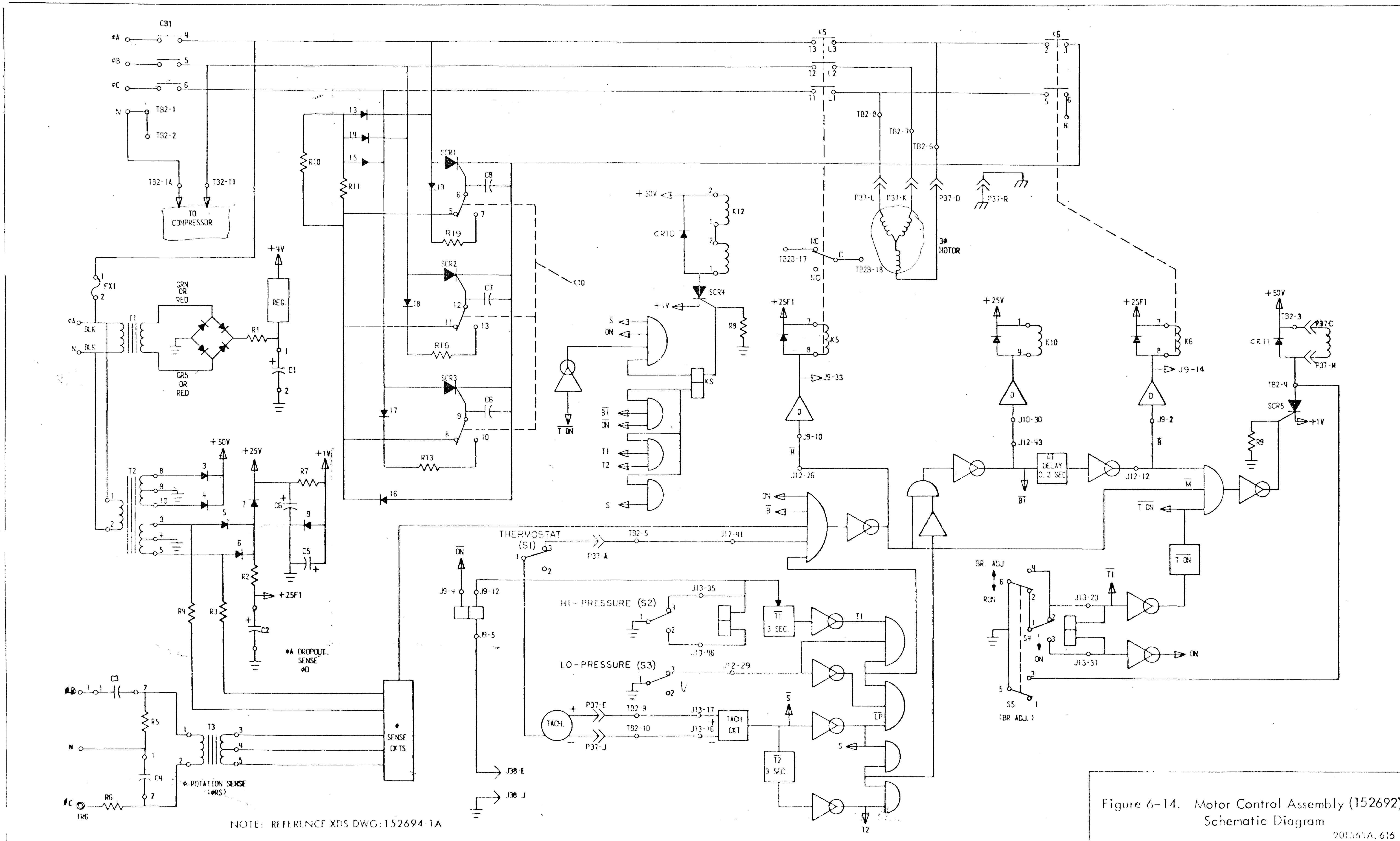
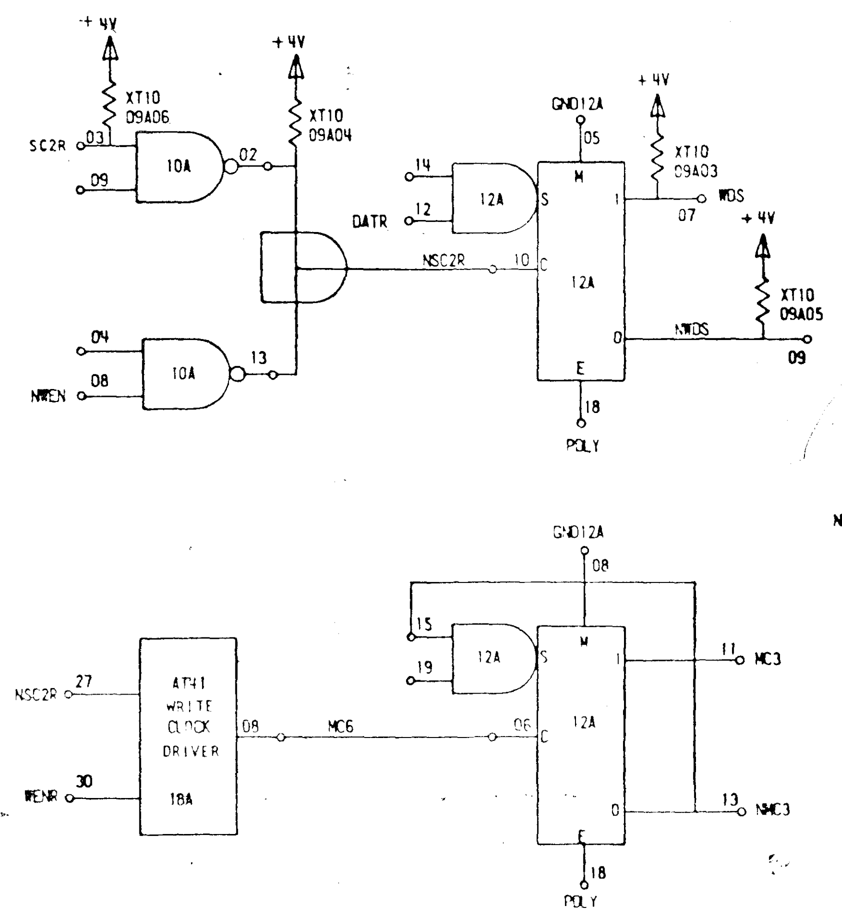


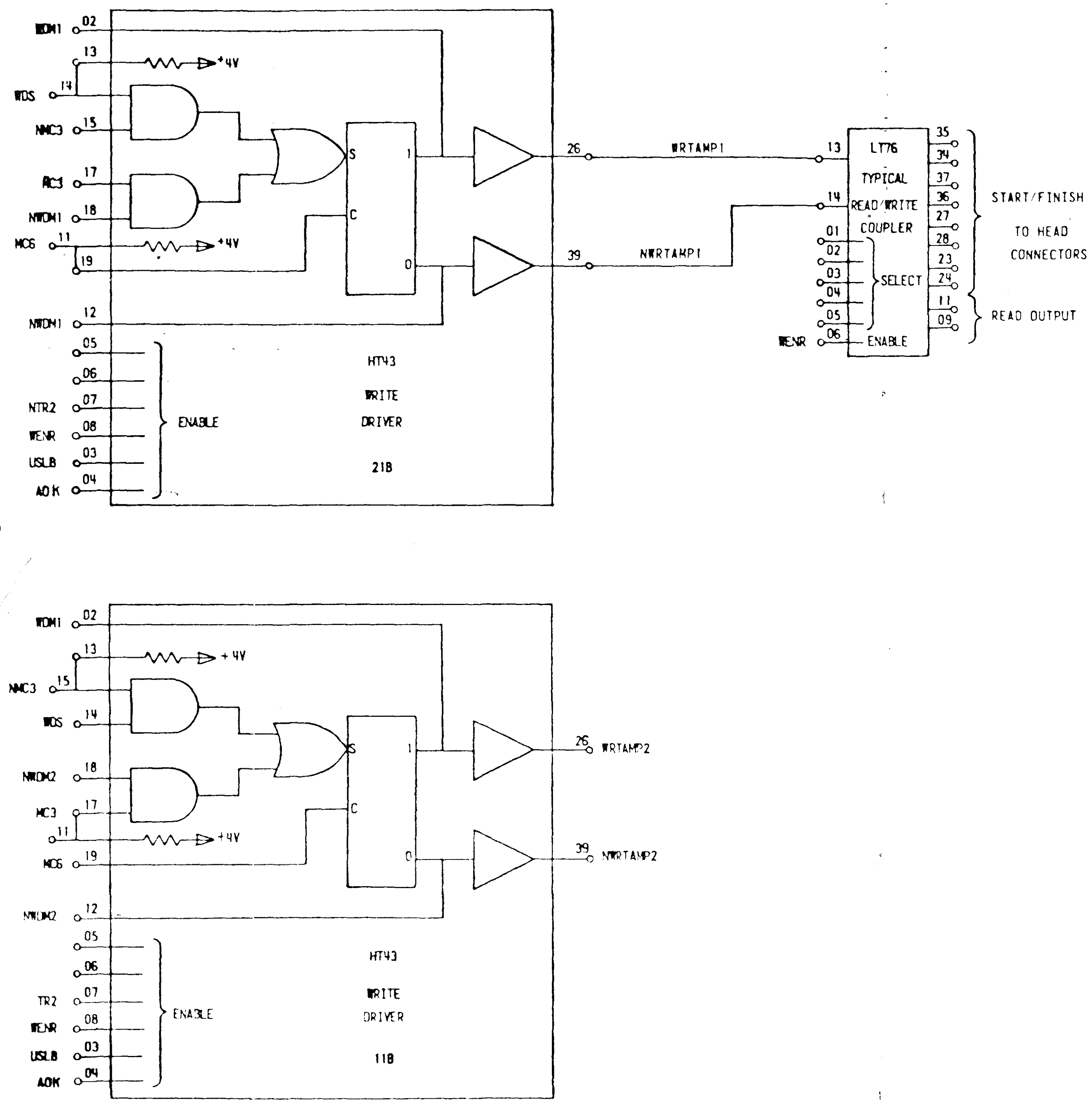
Figure 6-14. Motor Control Assembly (152692), Schematic Diagram

901565A.616

MODULE LOCATION CHART

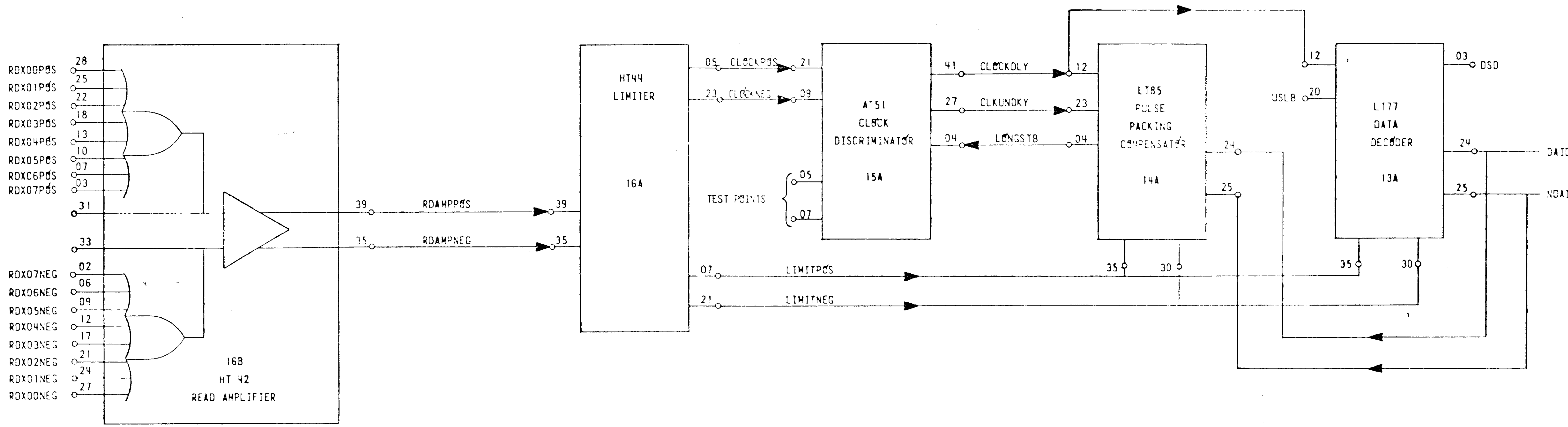
TRACK ADDRESS	LT76	HT43
00 - 63	20B	21B
64 - 127	19B	
128 - 191	18B	
192 - 255	17B	
256 - 319	15B	11B
320 - 383	14B	
384 - 447	13B	
448 - 511	12B	





NOTE: REFERENCE XDS DWG: 149337-9A

Figure 6-15. EP RAD Selection Unit, Write Channel (Without Logical Sparing), Schematic Diagram 901565A.614



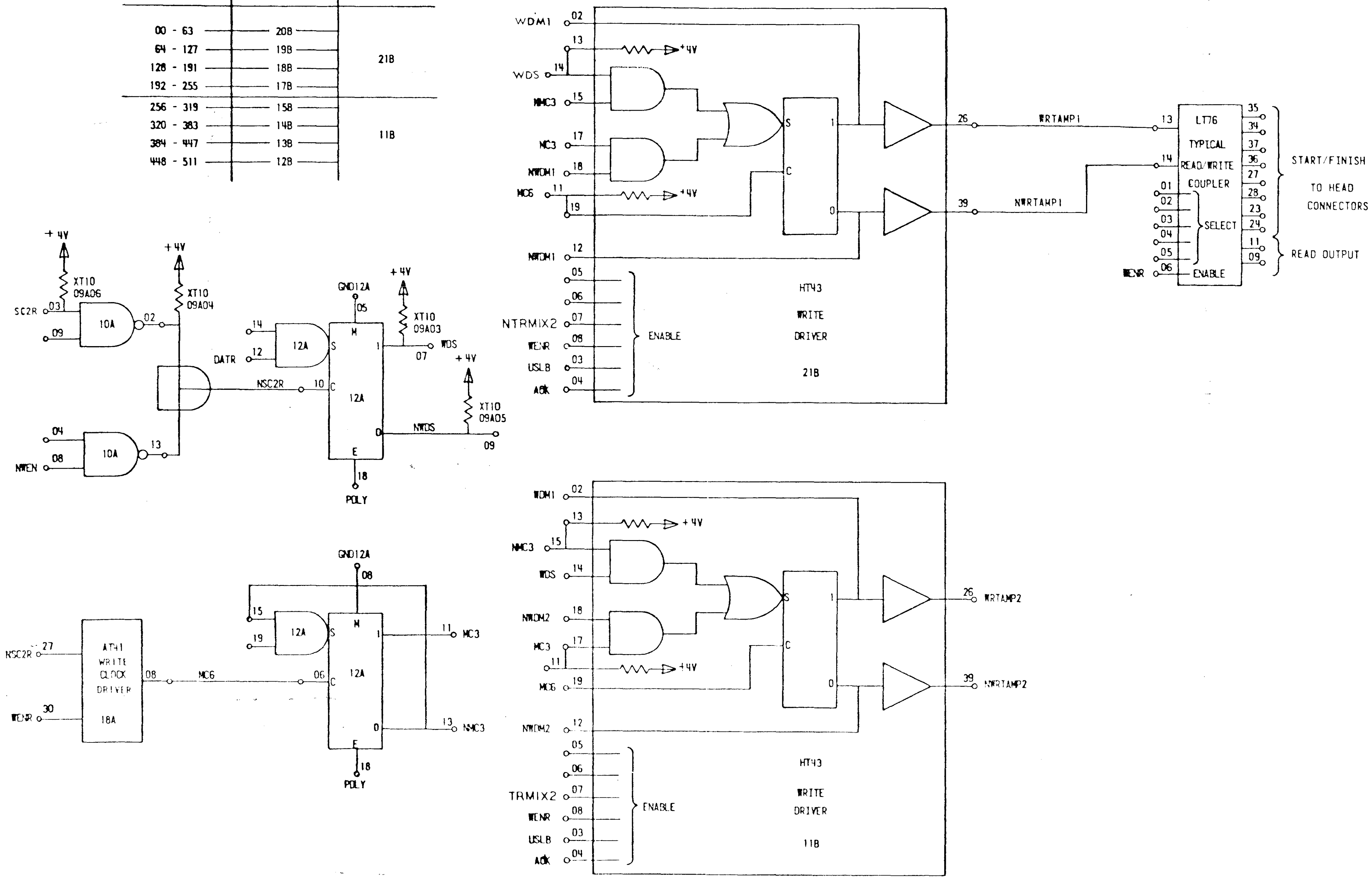
NOTE: REFERENCE XDS DWG: 149337-10A

Figure 6-16. EP RAD Selection Unit, Read Channel, Schematic Diagram

901565A.615

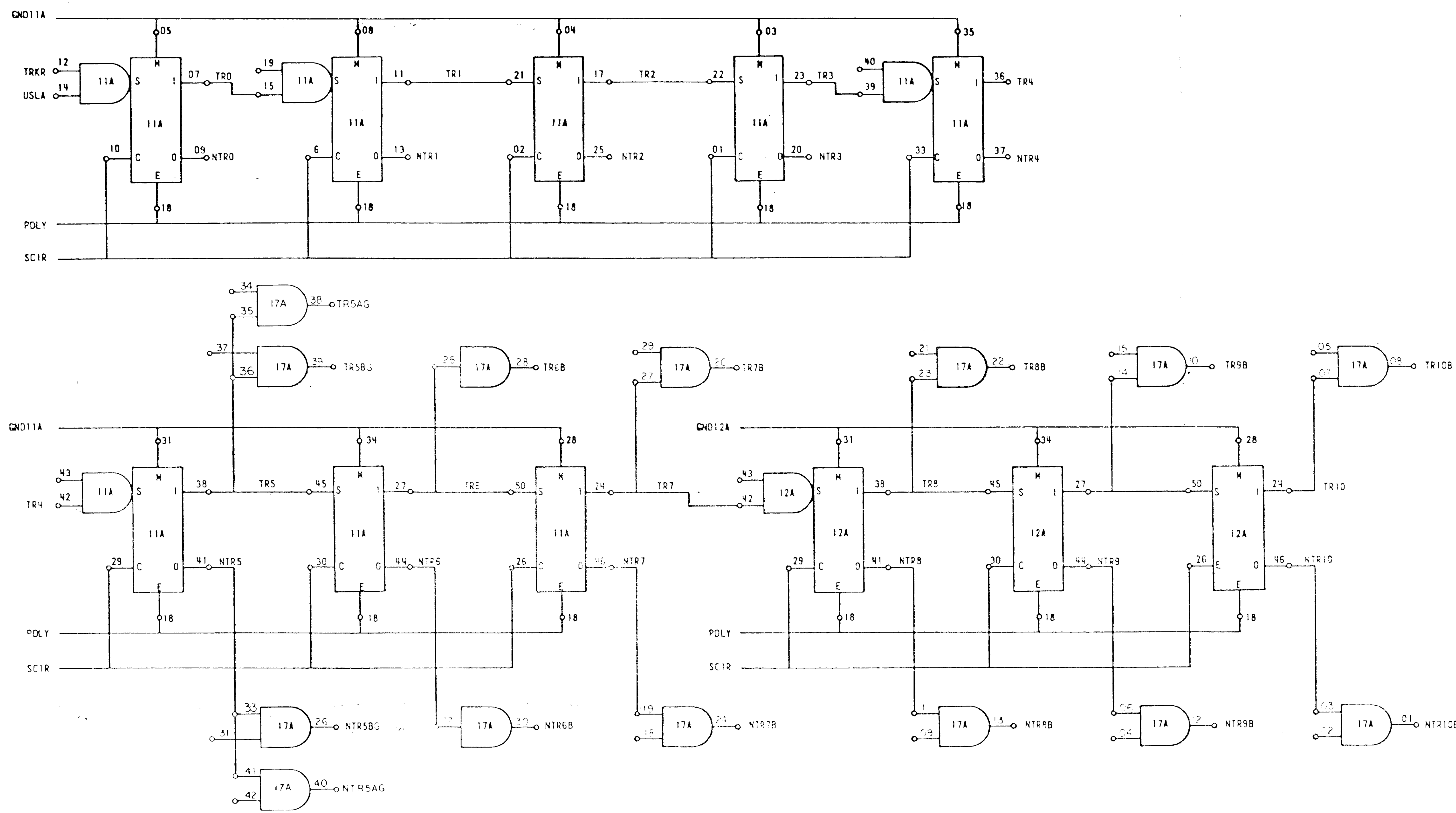
MODULE LOCATION CHART

TRACK ADDRESS	LT76	HT43
00 - 63	20B	21B
64 - 127	19B	
128 - 191	18B	
192 - 255	17B	
256 - 319	15B	11B
320 - 383	14B	
384 - 447	13B	
448 - 511	12B	



NOTE: REFERENCE XDS DWG:149339-9B

Figure 6-17. LP RAD Selection Unit, Write Channel (With Logical Sparing), Schematic Diagram 901565A.617



NOTE: REFERENCE XDS DWG 149337-19B

Figure 6-18. EP RAD Selection Unit, Track Register (With Logical Sparing), Schematic Diagram 901565A.618

LT76

INPUT/OUTPUT AND START/FINISH LOCATION CHART

LT76 MODULE	SELECT INPUT	SELECT PIN	WRITE AMP PIN	WRITE AMP INPUT	READ OUTPUT	READ PIN	START/FINISH PIN	START/FINISH OUTPUT	TRACK	CONNECTOR PIN
20B	NTRMIX2	01	13	WRTAMP1	RDX00POS	09	35 / 34	1X00S / 1X00F	00-15	P8-0A-40 / 41
	NTRMIX3	02	14	NWRTAMP1	RDX00NEG	11	37 / 36	2X00S / 2X00F	16-31	42 / 43
	NTRMIX4	03					27 / 28	3X00S / 3X00F	32-47	44 / 45
	WENR	06					23 / 24	4X00S / 4X00F	48-63	46 / P8-0A-47
19B	NTRMIX2	01	13	WRTAMP1	RDX01POS	09	35 / 34	1X01S / 1X01F	64-79	P8-0B-40 / -41
	NTRMIX3	02	14	NWRTAMP1	RDX01NEG	11	37 / 36	2X01S / 2X01F	80-95	-42 / -43
	TRMIX4	03					27 / 28	3X01S / 3X01F	96-111	-44 / -45
	WENR	06					23 / 24	4X01S / 4X01F	112-127	-46 / P8-0B-47
18B	NTRMIX2	01	13	WRTAMP1	RDX02POS	09	35 / 34	1X02S / 1X02F	128-143	P8-1A-40 / -41
	TRMIX3	02	14	NWRTAMP1	RDX02NEG	11	37 / 36	2X02S / 2X02F	144-159	-42 / -43
	NTRMIX4	03					27 / 28	3X02S / 3X02F	160-175	-44 / -45
	WENR	06					23 / 24	4X02S / 4X02F	176-191	-46 / P8-1A-47
17B	NTRMIX2	01	13	WRTAMP1	RDX03POS	09	35 / 34	1X03S / 1X03F	192-207	P8-1B-40 / -41
	TRMIX3	02	14	NWRTAMP1	RDX03NEG	11	37 / 36	2X03S / 2X03F	208-223	-42 / -43
	TRMIX4	03					27 / 28	3X03S / 3X03F	224-239	-44 / -45
	WENR	06					23 / 24	4X03S / 4X03F	240-255	-46 / P8-1B-47
15B	TRMIX2	01	13	WRTAMP2	RDX04POS	09	35 / 34	1X04S / 1X04F	256-271	P8-2A-40 / -41
	NTRMIX3	02	14	NWRTAMP2	RDX04NEG	11	37 / 36	2X04S / 2X04F	272-287	-42 / -43
	NTRMIX4	03					27 / 26	3X04S / 3X04F	288-303	-44 / -45
	WENR	06					23 / 24	4X04S / 4X04F	304-319	-46 / P8-2A-47
14B	TRMIX2	01	13	WRTAMP2	RDX05POS	09	35 / 34	1X05S / 1X05F	320-335	P8-2B-40 / -41
	NTRMIX3	02	14	NWRTAMP2	RDX05NEG	11	37 / 36	2X05S / 2X05F	336-351	-42 / -43
	TRMIX4	03					27 / 28	3X05S / 3X05F	352-367	-44 / -45
	WENR	06					23 / 24	4X05S / 4X05F	368-383	-46 / P8-2B-47
13B	TRMIX2	01	13	WRTAMP2	RDX06POS	09	35 / 34	1X06S / 1X06F	384-399	P8-3A-40 / -41
	TRMIX3	02	14	NWRTAMP2	RDX06NEG	11	37 / 36	2X06S / 2X06F	400-415	-42 / -43
	NTRMIX4	03					27 / 28	3X06S / 3X06F	416-431	-44 / -45
	WENR	06					23 / 24	4X06S / 4X06F	432-447	-46 / P8-3A-47
12B	TRMIX2	01	13	WRTAMP2	RDX07POS	09	35 / 34	1X07S / 1X07F	448-463	P8-3B-40 / -41
	TRMIX3	02	14	NWRTAMP2	RDX07NEG	11	37 / 36	2X07S / 2X07F	464-479	-42 / -43
	TRMIX4	03					27 / 28	3X07S / 3X07F	480-495	-44 / -45
	WENR	06					23 / 24	4X07S / 4X07F	496-511	-46 / P8-3B-47

NOTE: REFERENCE XDS DWG: 149337-18B

Figure 6-19. Input/Output and Start/Finish Location Chart (With Logical Sparing)

901565A.619

INPUT

MODULE

PIN	25B	24B	23B	22B	10B	09B	08B	07B
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9
22	NTR8B	NTR8B	NTR8B	NTR8B	NTR8	NTR8	NTR8	NTR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5A	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10
12	NTR9B	NTR9B	NTR9B	NTR9B	NTR9	NTR9	NTR9	NTR9
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
28	NTR10B	NTR10B	NTR10B	NTR10B	NTR10	NTR10	NTR10	NTR10
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG
14	TR10B	TR10B	TR10B	TR10B	TR10	TR10	TR10	TR10
27	TR9B	TR9B	TR9B	TR9B	TR9	TR9	TR9	TR9
13	TR8B	TR8B	TR8B	TR8B	TR8	TR8	TR8	TR8
23	NTR7B	TR7B	NTR7B	TR7B	NTR7	TR7	NTR7	TR7
24	NTR6B	NTR6B	TR6B	TR6B	NTR6	NTR6	TR6	TR6
25	NTR5BG	NTR5BG	NTR5AG	NTR5AG	TR5BG	TR5BG	TR5AG	TR5AG

OUTPUT

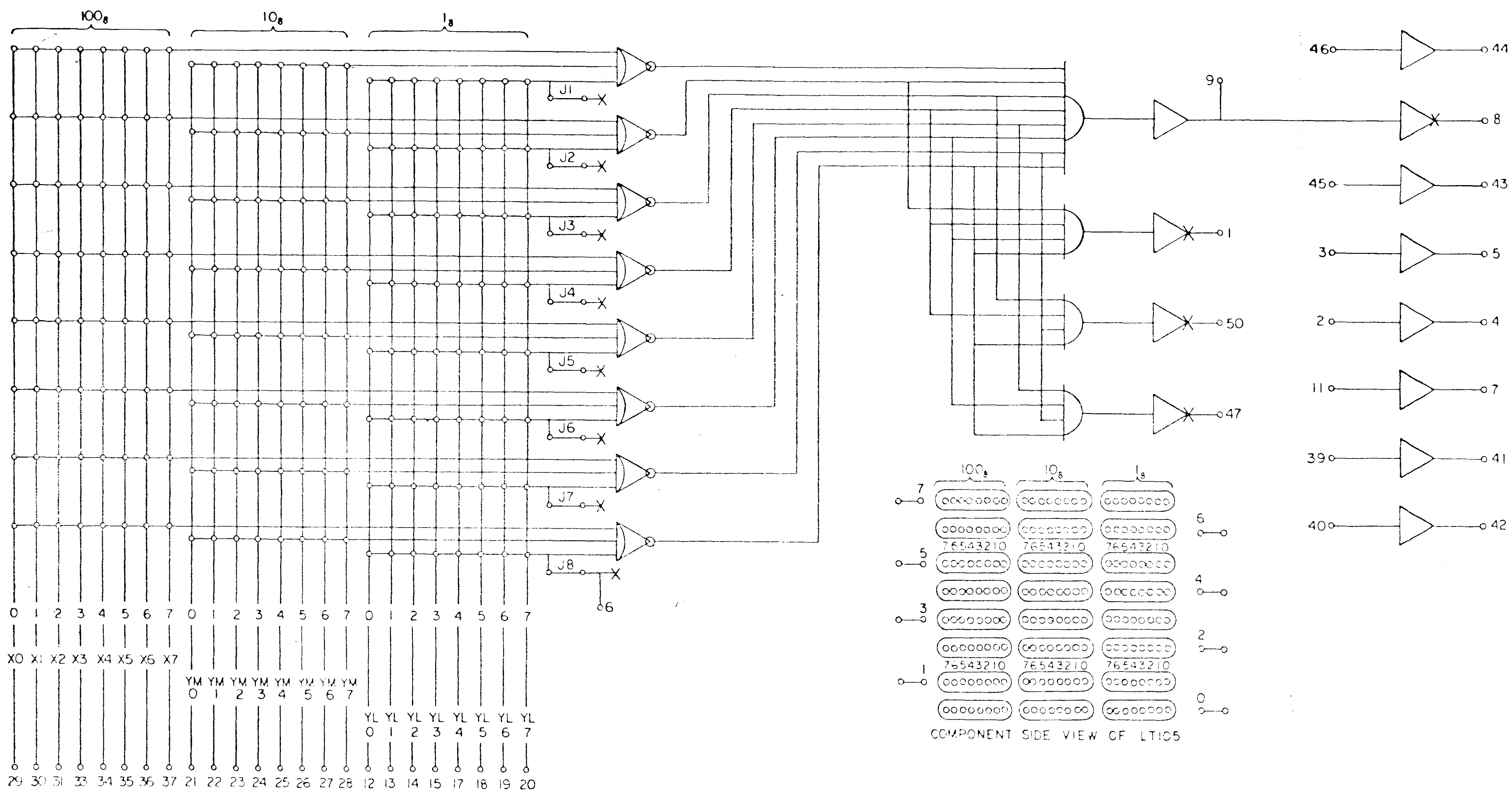
MODULE

Gate	25B	24B	23B	22B	10B	09B	08B	07B
36	Y00	Y08	Y16	Y24	Y32	Y40	Y48	Y56
05	Y01	Y09	Y17	Y25	Y33	Y41	Y49	Y57
38	Y02	Y10	Y18	Y26	Y34	Y42	Y50	Y58
06	Y03	Y11	Y19	Y27	Y35	Y43	Y51	Y59
35	Y04	Y12	Y20	Y28	Y36	Y44	Y52	Y60
04	Y05	Y13	Y21	Y29	Y37	Y45	Y53	Y61
37	Y06	Y14	Y22	Y30	Y38	Y46	Y54	Y62
07	Y07	Y15	Y23	Y31	Y39	Y47	Y55	Y63

NOTE: REFERENCE XDS DWG: 149337-17B

Figure 6-20. Y-Select Location Chart (With Logical Sparing)

901565A.620



TYPICAL LT105 LOGIC DIAGRAM

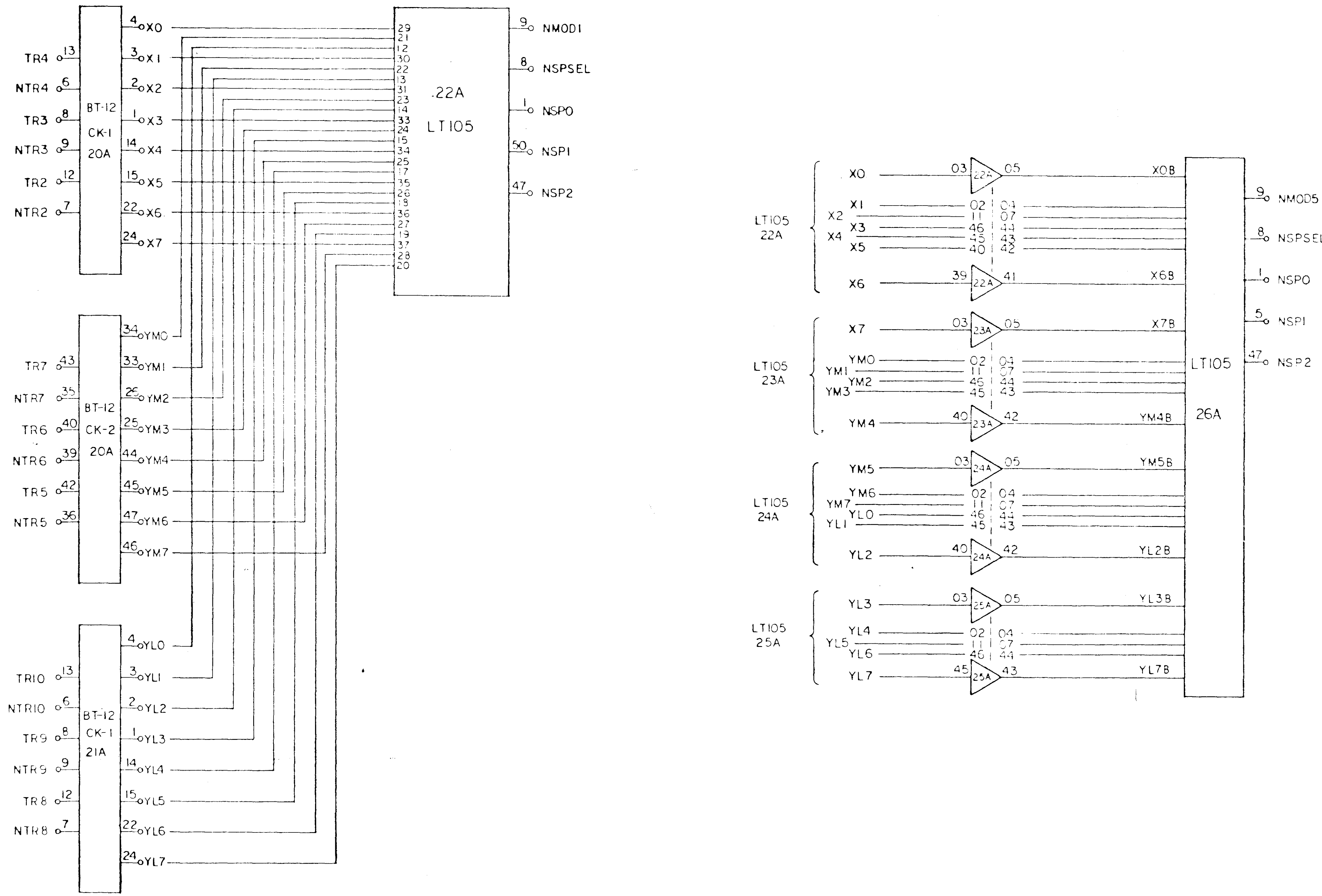
UNITS WITH LOGICAL SPARING

NOTES:

1. -⌖- ON 100_8, 10_8, & 1_8 INDICATES LOCATIONS AT WHICH SPARING JUMPERS CAN BE INSTALLED. NO SPARING JUMPERS ARE INSTALLED AT THIS TIME. SEE NOTES 2-7 FOR INSTALLATION PROCEDURE.
2. DECODE DECIMAL TRACK FAILING ADDRESS INTO AN OCTAL ADDRESS.
3. THIS OCTAL ADDRESS, THEN, IS XYZ; WHERE $X=100_8$, $Y=10_8$ & $Z=1$.
4. INSTALL L SHAPED JUMPER WIRES IN APPROPRIATE SLOTS FOR X, Y & Z.
5. SOLDER JUMPERS TO PADS ON COMPONENT SIDE (SEE REF DIA ABOVE), TURN BOARD OVER & SOLDER AND CUT LEADS TO SIZE.
6. REMOVE JUMPER FOR CIRCUIT SELECTED (J1, J2 … J8).
7. REINSTALL LT105.
8. REFERENCE XDS DWG: 149337-22B

Figure 6-21. LT105 Spares Selector Module, Logic Diagram

901565A.621

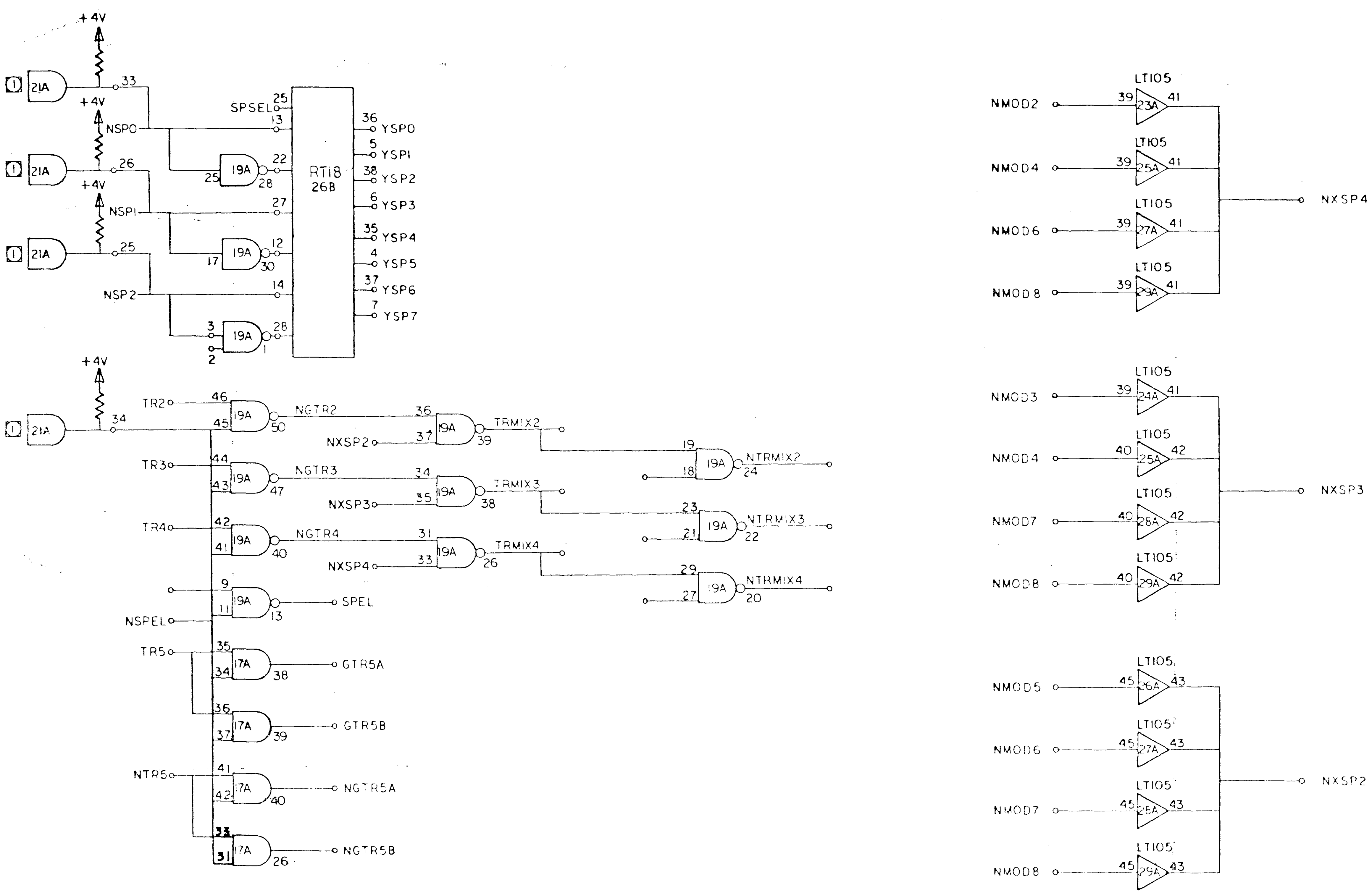


NOTES:

1. LT105-27A, LT105-28A, LT105-29A, SAME AS LT105-26A.
2. LT105-23A, LT105-24A, LT105-25A, SAME AS LT105-22A.
3. REFERENCE XDS DWG:149337 22A

Figure 6-22. EP RAD Selection Unit, Spares Select Circuits, Logic Diagram (Sheet 1 of 2)

901565A.622/1



NOTES:

1. ALL GATE INPUTS OF THIS ELEMENT ARE OPEN (TRUE)
2. REFERENCE XDS DWG: 149337-21B

Figure 6-22. EP RAD Selection Unit, Spares Select Circuits, Logic Diagram (Sheet 2 of 2) 901565A.622 2

SECTION VII
SPECIFICATIONS AND INSTALLATION DATA

7-1 SPECIFICATIONS

Specifications for the EP RAD storage unit are listed in table 7-1. An EP RAD file consists of a maximum of eight EP RAD storage units, one of which contains an EP RAD controller.

7-2 INSTALLATION

7-3 INSTALLATION REQUIREMENTS

Refer to figure 7-1 for overall space requirements of an EP RAD storage unit, including front and rear access areas for maintenance. Refer to figures 7-2 and 7-3 for cabling requirements.

Table 7-2 summarizes cable connections between an EP RAD controller and an IOP for various systems. The IOP equipment may be one of the following:

a. Multiplexing Input/Output Processor Model 8271 (Sigma 5)

b. Multiplexing Input/Output Processor Model 8471 (Sigma 7)

c. Four-byte MIOP Model 8273 (Sigma 5)

d. Four-byte MIOP Model 8473 (Sigma 7)

e. Selector Input/Output Processor Model 8285 (Sigma 5)

f. Selector Input/Output Processor Model 8485 (Sigma 7)

g. Integral IOP (Sigma 2)

h. Integral IOP (Sigma 5)

7-4 INSTALLATION PROCEDURE

The installation sequence indicated in table 7-3 may be used for installation of an EP RAD file as a subsystem of a complete computer installation or as an addition to a computer installation.

Table 7-1. EP RAD Storage Unit Specifications

Characteristic	Specification
Physical Characteristics	
Height	63-1/2 inches
Width	29-1/2 inches
Depth	35-1/2 inches
Weight	1200 lbs
Power Source Requirements	
Voltage	208 Vac ± 10%, three-phase, 60 ± 1/2 Hz
Current	
Starting (max)	57A
Running (max)	15A
Power Requirements	
EP RAD storage unit	3000W

(Continued)

Table 7-1. EP RAD Storage Unit Specifications (Cont.)

Characteristic	Specification
Power Requirements (Cont.)	
EP RAD controller	300W
EP RAD file (maximum size)	24,300W
Operational Characteristics	
Disc file speed	1774 rpm
Period of revolution	33.8 ms
Period per sector	2.81 ms
Intersector gap time	100 μs
Effective data transfer rates	
Bits/second	3,070,000
Bytes/second	354,000
Words/second	88,500
Environmental Characteristics	
Ambient room temperature	10°C to 40°C (50°F to 104°F)
Relative humidity	10% to 90%

Table 7-2. Connections Between EP RAD Controller and IOP

EP RAD CONTROLLER MODULE AND LOCATION	IOP MODULE AND LOCATION			
	SIOP	MIOP	Sigma 2 Integral IOP	Sigma 5 Integral IOP
AT17 26C ✓	AT11 9E	AT11 ✓ 1D	AT11 7C	AT11 9E
AT10 28C ✓	AT12 11E	AT12 ✓ 14C	AT12 1C	AT12 9F
AT11 30C ✓	AT11 21E	AT11 ✓ 32A	AT11 3C	AT11 8L
AT12 32C ✓	AT10 14E	AT10 ✓ 14B	AT11 5C	AT10 10L
AT11* 28B	AT11* 19E	AT11** 29A		
AT11† 31B	AT11† 17E	AT11** 19C		

* Used only for two- or four-byte IOP interface (Models 8285/8485)
† Used only for four-byte IOP interface (Models 8285/8485)
**Used only for four-byte IOP interface (Models 8273/8473)

Table 7-3. Installation Procedure Checkoff List

Item	Operation
1	Visually inspect crated equipment for obvious signs of damage during shipment
2	Check that each item of the Installation Material List (IML) is included in the shipment
3	Check that maintenance documents specified in the IML are included in the shipment
4	Check that revision level of maintenance documents agrees with revision level of equipment*
5	Check that revision level of diagnostic program documents agrees with revision level of media CAUTION Do not tilt EP RAD storage unit more than 15 degrees from vertical during uncrating Note Inspect equipment for damage during uncrating
6	Uncrate equipment using following tools: a. Claw hammer b. 12-inch crescent wrench c. 1-1/8-inch socket wrench with 18-inch ratchet d. Four metal plates to prevent floor damage by EP RAD storage unit feet
7	Locate equipment according to Installation Floor Plan Note Do not move EP RAD storage unit after it has been installed and is operating
8	Before connecting power cables or control cables, check that all circuit breakers and switches of primary power source are off

*Revision level of maintenance documents is indicated by change letter. Revision level of modules is indicated by change letter on mother board. Revision level of automated wire lists is indicated by letter suffix of part number. Revision level of equipment is indicated on attached sticker

(Continued)

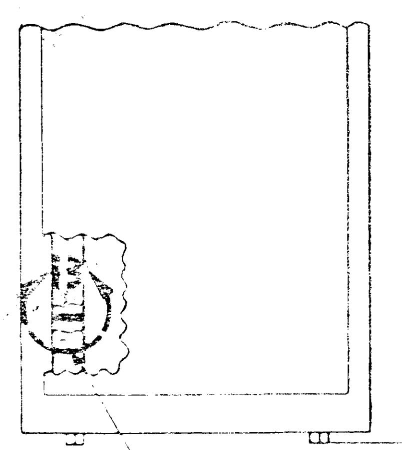
Table 7-3. Installation Procedure Checkoff List (Cont.)

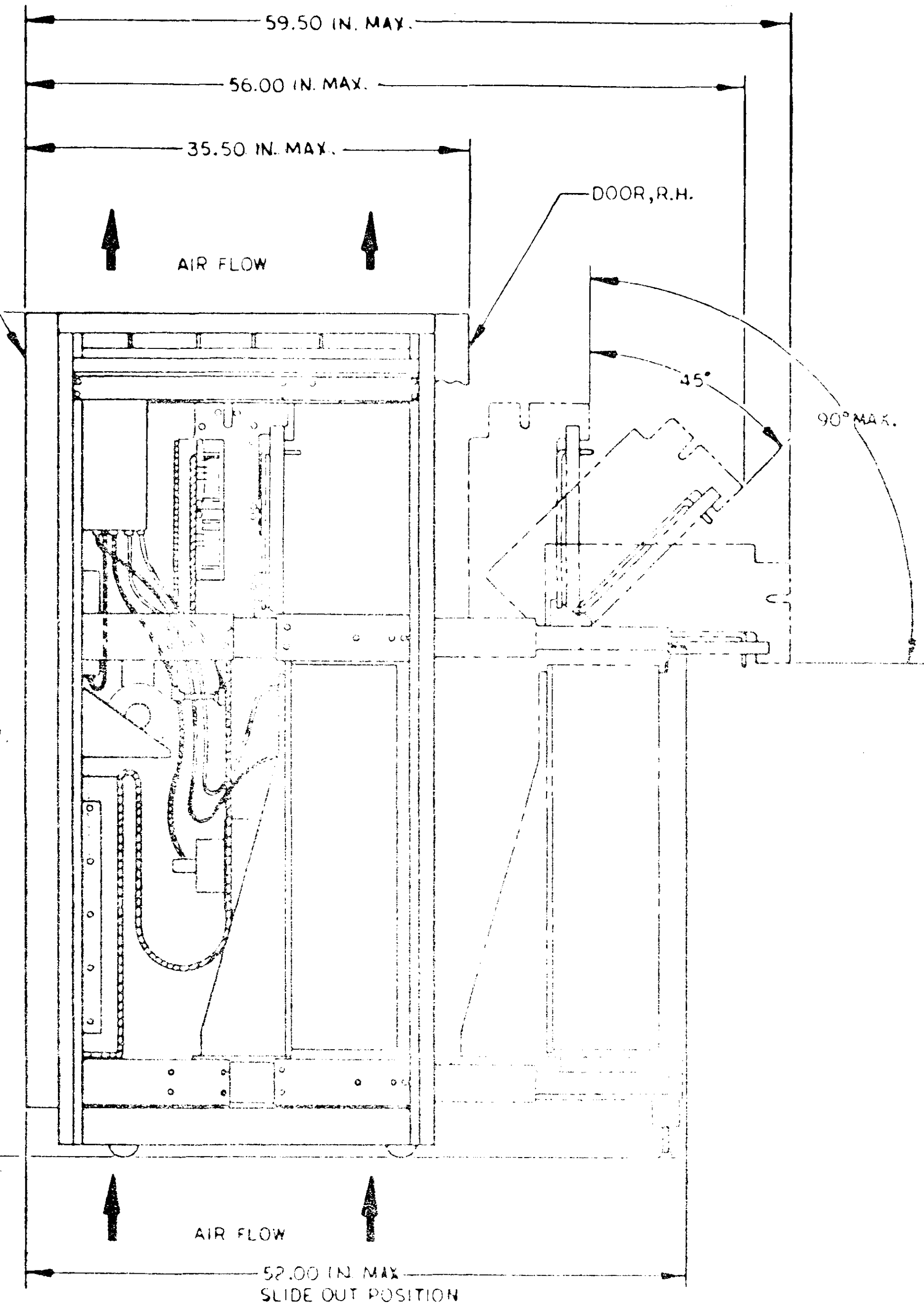
Item	Operation
9	Check power supplies (PT16, PT17, PT18, PT19, and PT20) for loose connections
10	Check that all power supplies have circuit breakers set to ON and MARGIN switches set to N (normal)
11	Check power distribution boxes (PT14 and PT15) for loose connections
12	Check that items connected to the primary power source are distributed among all three phases as evenly as possible
13	Check primary power source outlets for proper wiring of each phase and neutral to ground
14	Check primary power cables for short circuits
15	Check power buses on side of each frame for short circuits and loose connections
16	Connect control cables according to Installation Cable List, noting the following features: a. Port expander cables are connected upside down b. All terminated cables have 16 ohms impedance to ground c. Major assemblies of computer are located as indicated in Computer Assembly Chart d. Cables for add-on installations labelled end-for-end (A, B, C, ...), so that corresponding ends can be identified after cables are beneath flooring
17	Check that modules of EP RAD selection units are installed as indicated in figure 7-4 Note Optional modules in EP RAD controller are dependent on use of one-, two-, or four-byte interface with IOP
18	Check that modules of EP RAD controller are installed as indicated in figure 7-5
19	Connect primary power cabling according to Installation Power Chart
20	Turn on circuit breakers and switches of primary power source

(Continued)

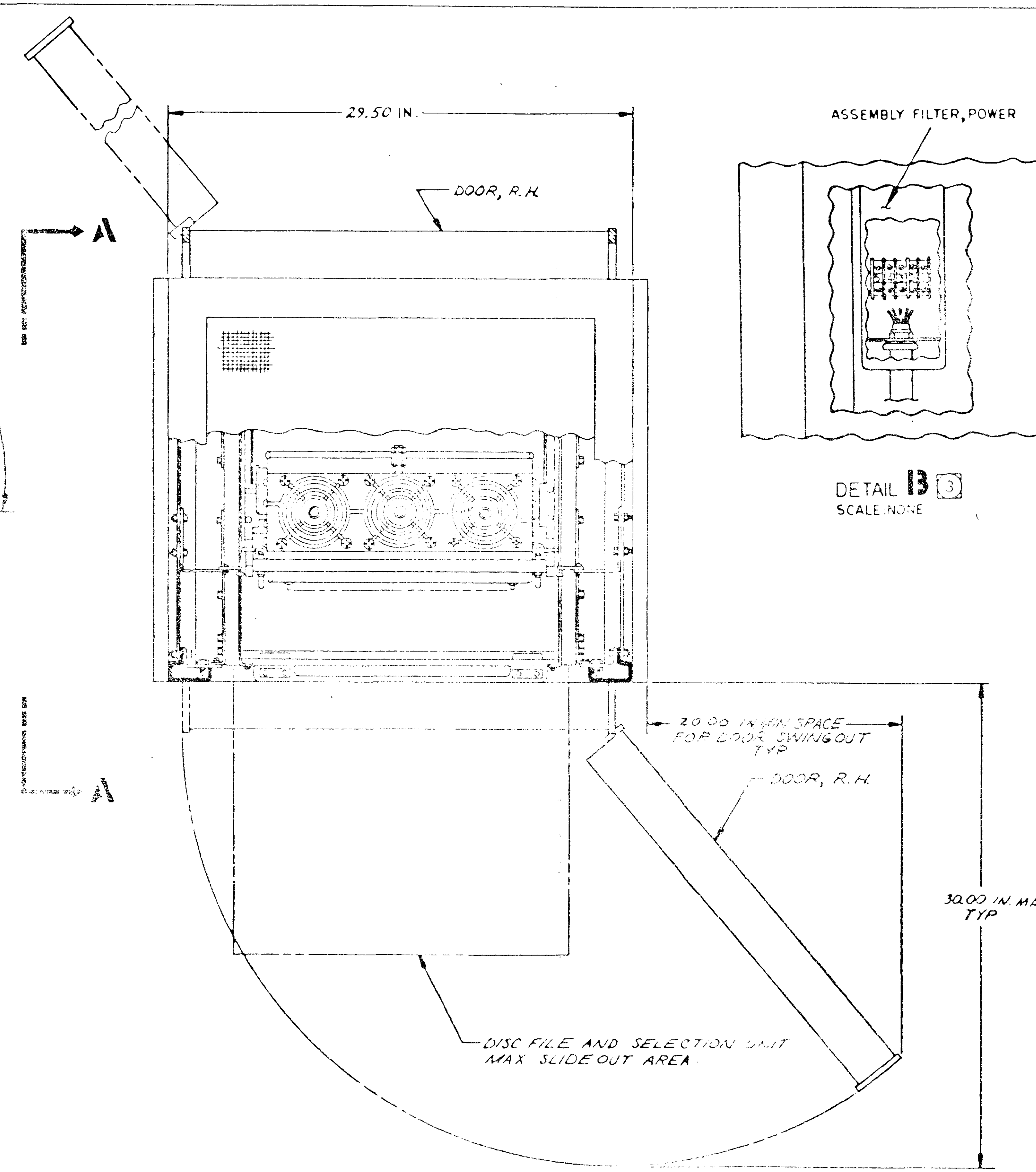
Table 7-3. Installation Procedure Checkoff List (Cont.)

Item	Operation
21	Check that all fans are operating Note EP RAD storage units are checked before shipment; however, the procedure of paragraph 8-4 may be used as required during installation
22	Use turn-on procedure for each item of computer installation (computer, memory, IOP, peripherals)
23	Exercise each item of installation with its diagnostic
24	Exercise systems evaluation and test program (SEVA)





VIEW A-A
SCALE: NONE
(ROTATED 90° CCW)
SIDE PANEL REMOVED FOR CLARITY



NOTES:

1. ADJUSTMENT OF LEVELING SCREWS IS 6 IN. MAX.
2. POWER REQUIREMENTS.
   208V, 60 ± 0.5 HZ, 3 PHASE WYE INPUT.
   POWER FILTER

PHASE	START	RUN
TB1-1	16A	2A
TB-2	25A	11A
TB-3	16A	2A

3. INPUT POWER CONNECTION.
   IF THERE IS MORE THAN ONE STORAGE UNIT, BALANCE LOAD BETWEEN PHASES AS FOLLOWS,

POWER FILTER	UNIT 1 & 4	UNIT 2	UNIT 3
TB1-1	Ø 1	Ø 2	Ø 3
TB1-2	Ø 2	Ø 3	Ø 1
TB1-3	Ø 3	Ø 1	Ø 2
TB1-4	NEUTRAL		
TB1-5	GROUND		

4. REFERENCE XDS DWG 149338 1A, 2A

Figure 7-1. RAD Storage Unit, Installation Drawing

901565A.705

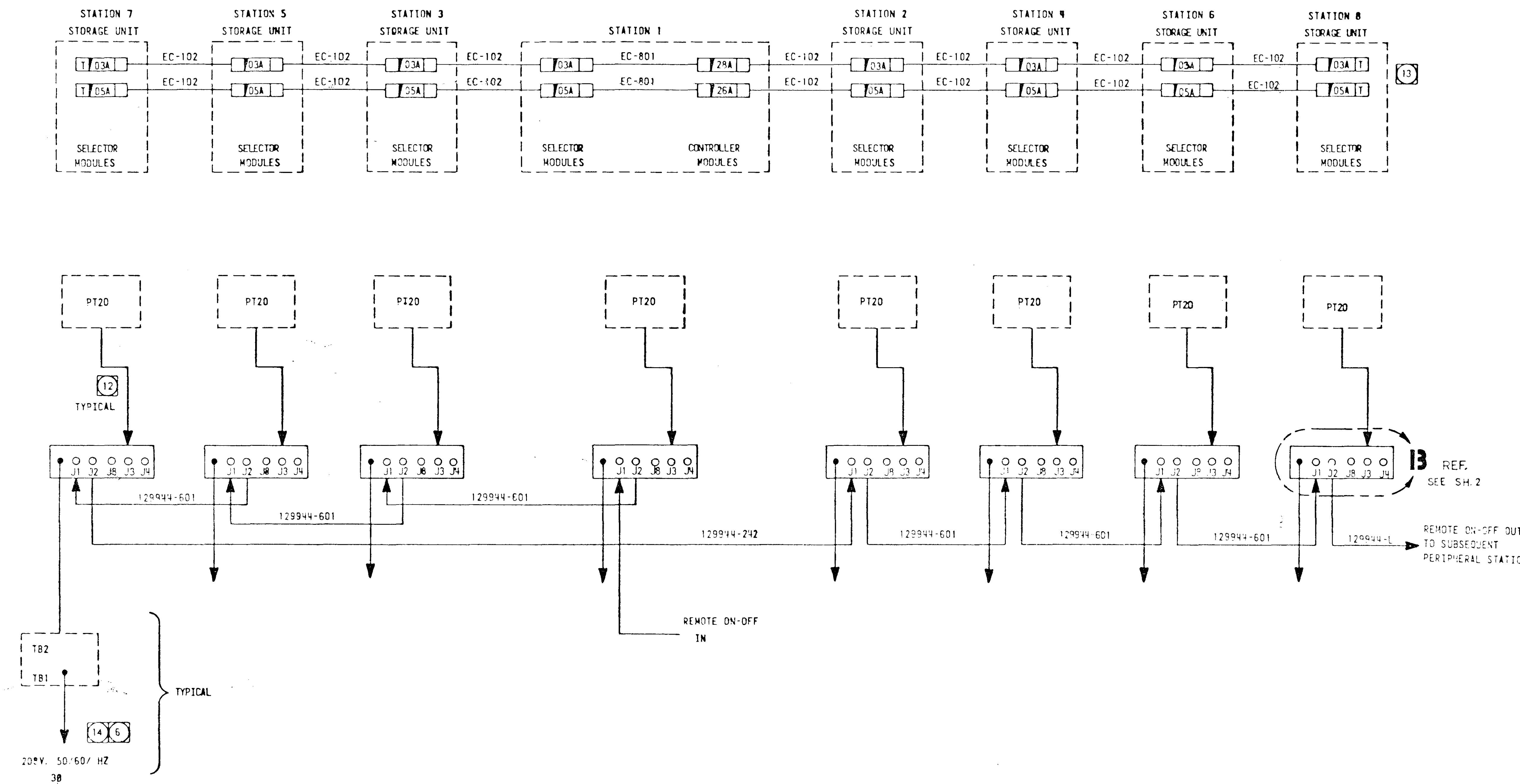


Figure 7-2. EP RAD File, Cabling Diagram (Sheet 1 of 2)

901565A.701/1

NOTES, UNLESS OTHERWISE SPECIFIED

1. REFERENCE DRAWINGS,
   - A. INSTALLATION DRAWING, SIGMA SYSTEM POWER INTERCONNECTIONS - 133273
   - B. INSTALLATION DRAWING, RAD MEMORY - 126657
   - C. INSTALLATION DRAWING, RAD MEMORY - 132841
   - D. INSTALLATION DRAWING, RAD CONTROLLER - 135747
   - E. INSTALLATION DRAWING, SINGLE BAY CABINET - 131417
   - F. INSTALLATION DRAWING, DISC MEMORY - 135345
   - G. PROCEDURE, INSTALLATION RAD INTERCONNECTIONS - 134124
   - H. INSTALLATION DRAWING, STORAGE UNIT-137534
   - I. INSTALLATION DRAWING, CONTROLLER-137506
   - J. INSTALLATION DRAWING PT20-137209
   - K. INSTALLATION DRAWING STORAGE UNIT-149338
   - L. INSTALLATION DRAWING CONTROLLER 149333

2. AN EP RAD FILE MAY BE EXPANDED BY ADDING STATIONS TO EITHER SIDE OF THE STATION CONTAINING THE RAD CONTROLLER. FOR EFFICIENCY A NUMERICAL BALANCE OF ADDED STATIONS MUST BE MAINTAINED TO THE LEFT AND RIGHT OF THE CABINET CONTAINING THE RAD CONTROLLER.

3. INSTALL SIDE PANELS TO EP RAD STORAGE UNITS AT EXTREME ENDS OF EP RAD FILE

4. INCOMING REMOTE ON-OFF POWER CABLE CONNECTS TO "120V, 50/60 HZ INPUT, REMOTE ON-OFF" (J3) OF THE POWER DISTRIBUTION PANEL LOCATED IN THE CONTROLLER CABINET (STATION NO. 1). THE "120V, 50/60 HZ OUTPUT, REMOTE ON-OFF" (J4) OF THE LAST STATION IS AVAILABLE FOR CONNECTION TO SUBSEQUENT PHERIPHERAL STATIONS.

5. INTERCONNECTING POWER CABLES ARE CONNECTED IN SEQUENCE FROM STATION NO. 1 TO NO. 3 TO NO. 2 TO NO. 4 AS SHOWN. (ALL CABLES BETWEEN STATION NO. 2 & NO. 3 ARE 12 FT.). IF THE SUBSYSTEM CONTAINS ONLY TWO STATIONS (NO. 1 & NO. 2), INTERCONNECTING POWER CABLES BETWEEN NO. 1 & 2 WILL BE 6 FT.

6. INPUT POWER (208V, 3Ø, 50/60 HZ), INPUT POWER CABLES, AND 30 AMP. CIRCUIT BREAKERS FOR EACH RAD STATION TO BE PROVIDED BY THE CUSTOMER.

7. FOR CONNECTIONS OF SIGNAL AND PRIORITY CABLE CHAIN FROM THE RAD CONTROLLER TO THE IOP INTERFACE OR DEVICE CONTROLLER SEE, INSTALLATION DRAWING, PERIPHERAL DEVICE AND CONTROL PANEL INTERCONNECTION SYSTEM-137113.

8. ROUTE INTERCONNECTING SIGNAL CABLES ALONG HINGE SIDE OF FRAMES.

9. ROUTE STATION TO STATION INTERCONNECTING SIGNAL CABLES ALONG CABLE TROUGHS PROVIDED AT THE TOP OF CABINETS.

10. ROUTE AND HARNESS ALL CABLES AS REQUIRED USING CABLE STRAP - 124712.

11. RAD SUBSYSTEM TO BE ASSEMBLED WITH ALL CABINETS ADJACENT TO EACH OTHER.

12. AC CORDS FURNISHED WITH PT20 POWER SUPPLY.

13. MAXIMUM SIGNAL CABLE LENGTH FROM CONTROLLER TO LAST STORAGE UNIT IS FORTY FEET.

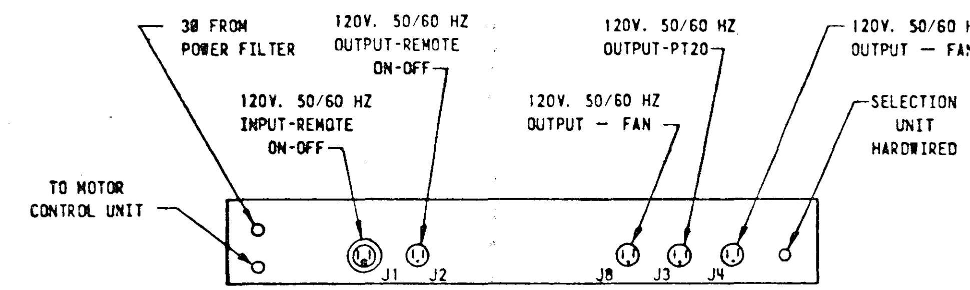
14. 3 PHASE POWER INPUT IS TO BE ALTERNATED ONTO TB-1 AT POWER FILTER TO PROVIDE EQUAL LOAD DISTRIBUTION AS FOLLOWS,

PWR FILTER	UNITS 1,4,7	UNITS 2,5,8	UNITS 3,6
TB1-1	Ø1	Ø2	Ø3
TB1-2	Ø2	Ø3	Ø1
TB1-3	Ø3	Ø1	Ø2
TB1-4	NEUTRAL		
TB1-5	GROUND		

15. MAXIMUM NUMBER OF STORAGE UNITS PER EP RAD FILE IS EIGHT(8).

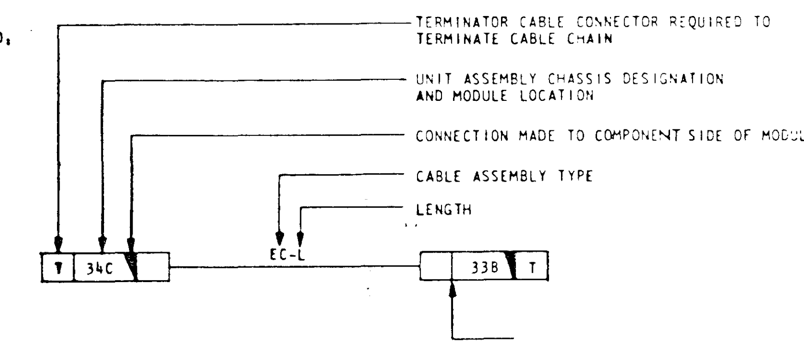
16 REFERENCE XDS DWG: 137115-1C, 4C

DETAIL B



LEGEND,

A.



B.

CODE	DESCRIPTION	PART NO.
EC-L	ETCHED TO COMPONENT CABLE ASSEMBLY	127314-CHARTED
T	TERMINATOR	127315

C.

SYMBOL	FUNCTION
•———	HARDWIRED CABLE
---T[ ]	TERMINATE WITH 127315 TERMINATOR IF CABLE CHAIN SHOULD END AT THIS POINT.

Figure 7-2. EP RAD File, Cabling Diagram (Sheet 2 of 2)

901565A.701/2

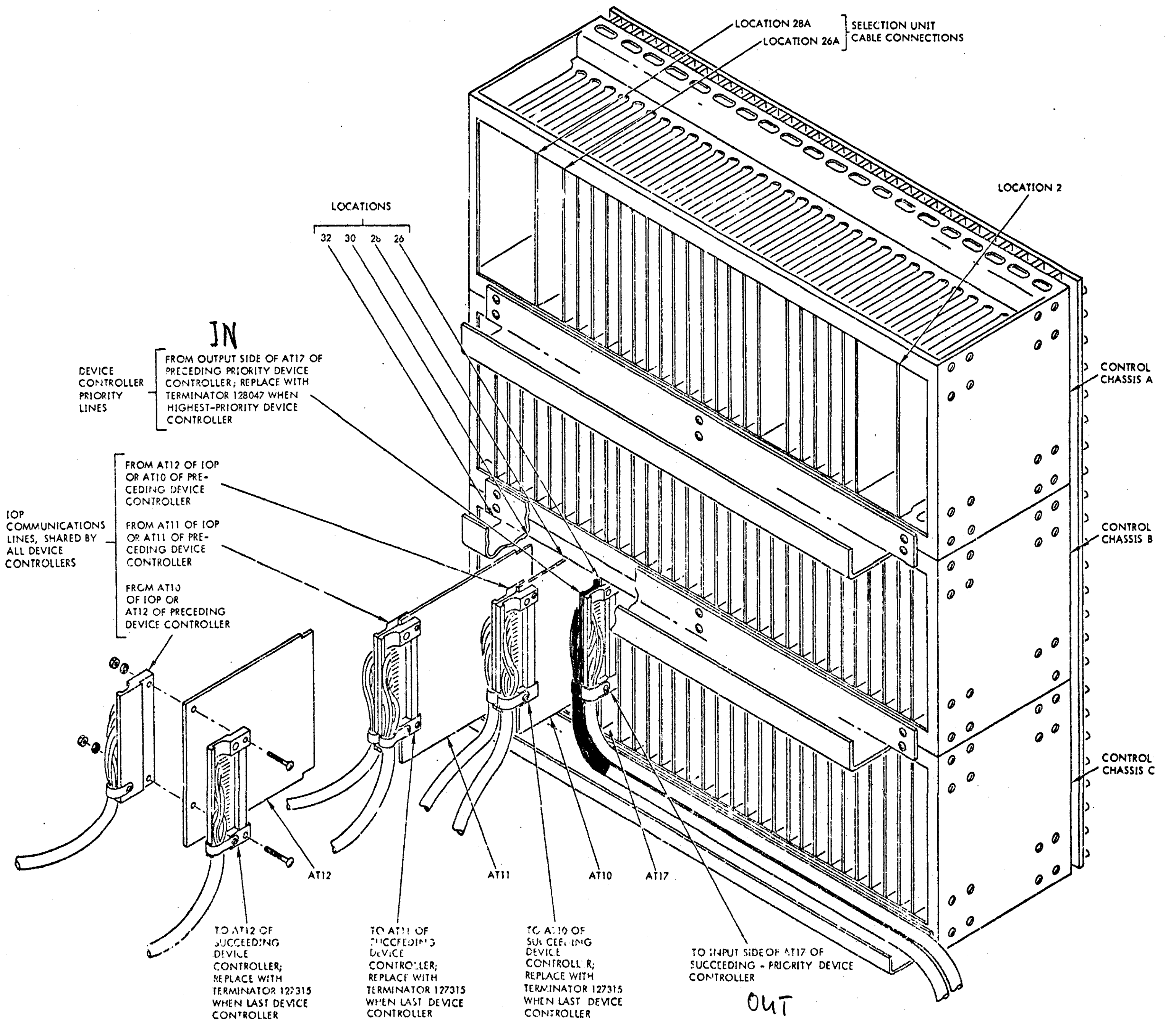


Figure 7-3. EP RAD Controller, Cable Connections

US

CHASSIS A

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
			LT 105	LT 105	LT 105	LT 105	LT 105	LT 105	LT 105	LT 105	BT 12	BT 12	IT 11	AT 41	BT 31	HT 44	AT 51	LT 85	LT 77	FT 12	FT 12	IT 11	XT 10	BT 11	LT 26		AT 12		AT 10		CT 12

Brackets: note 1 spans A19 through A29 and A17; note 3 spans A22 through A25; note 2 spans A22 through A29.

CHASSIS B

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
						RT 18	RT 18	RT 18	RT 18	RT 18	HT 43	LT 76	LT 76	LT 76	LT 76	HT 42	LT 76	LT 76	LT 76	LT 76	HT 43	RT 18	RT 18	RT 18	RT 18	OT 15		WT 29	FT 11	LT 32	P 35

Bracket: note 1 spans B26.

NOTES:

1. MODULES IN LOCATIONS A17, B26, AND A19 THROUGH A29 ARE LOGICAL SPARING CIRCUITS
2. LT105 MODULES IN LOCATIONS A22 THROUGH A29 NEED NOT BE INSERTED UNLESS LOGICAL SPARING IS REQUIRED
3. LT105 MODULES MUST BE INSERTED IN LOCATIONS A22 THROUGH A25 BEFORE ANY LT105 MODULES CAN BE INSERTED IN LOCATIONS A26 THROUGH A29

901565A. 702

Figure 7-4. EP RAD Selection Unit, Module Location Chart

UL

CHASSIS A

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
J 181		J 183		AT 12		AT 10	FT 27	FT 41	FT 41	FT 41	XT 10	LT 71	FT 27	FT 27	LT 58	LT 58	BT 11	FT 10	BT 11	IT 13		BT 10	BT 13	IT 11	BT 11	IT 11	FT 10			CT 10	

PET (locations 32–30)

CHASSIS B

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	AT 11	FT 27	FT 27	AT 11	FT 27	FT 27	IT 15	AT 24	FT 26	FT 26	XT 10	FT 26	FT 25 *	BT 15	FT 27	BT 11	IT 16	FT 27	IT 15	BT 16	HT 15	AT 16	IT 24	IT 11	BT 11	DT 14	HT 15	DT 14	FT 18	FT 12	XT 10
	32	32	32	16 32	16 32	16 32	16 32														16 32										

Locations 31–29: ②; locations 28–25: ① ②; location 11: ① ②

CHASSIS C

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AT 12	LT 43	AT 11	LT 41	AT 10	LT 24	AT 17		LT 26	LT 25	XT 10		FT 26	FT 27	IT 11	BT 11	FT 27	IT 13	BT 11	FT 10	IT 11		BT 11	IT 11	IT 15	BT 15	FT 27	LT 29	BT 22	FT 12	FT 10	

SUBCONTROLLER (locations 32–22)

OIL

NOTES:

1. MODULES IN LOCATIONS 11B AND 25B THROUGH 28B MUST BE INSERTED WHEN 16-BIT DATA PATH OPTION IS INSTALLED
2. MODULES IN LOCATIONS 11B AND 25B THROUGH 31B MUST BE INSERTED WHEN 32-BIT DATA PATH OPTION IS INSTALLED
3. PET CONNECTIONS USED ONLY DURING OFFLINE TEST OR FOR MONITORING ONLINE OPERATION

901565A. 703

Figure 7-5. EP RAD Controller, Module Location Chart

SECTION VIII
MAINTENANCE

8-1 SCOPE OF SECTION

The EP RAD file maintenance procedures in this section are for use following installation. However, the basic checks and adjustments of paragraph 8-4 can be used during installation, if required. For any operation requiring relocation of an EP RAD storage unit, refer to section VII.

8-2 GENERAL MAINTENANCE

All assembly and maintenance documents should be available at the installation that includes the EP RAD file. These documents should accurately reflect the change level of the EP RAD file.

External surfaces of the EP RAD file must be kept clean and dust free. Doors and panels must close completely and be in reasonable alignment. The tops of cabinets must remain clear to allow free intake and exhaust of air.

The interiors of the EP RAD file must be kept free of wire cuttings, dust, spare parts, and other foreign matter. No clip leads or push-on jumpers should be in use during normal operation, and all cables must be neatly dressed by clamps or routing. All chassis and frames must be properly bolted down, with all hardware in place. Air filters should be checked periodically for cleanliness and replaced if dirty.

8-3 DIAGNOSTIC TEST PROGRAMS

Diagnostic test programs should be run at frequent intervals as the primary preventive maintenance method for the EP RAD file. Programs should be run with the MARGIN switch of the PT20 power supply set at N (normal), L (low), and H (high).

Note

Before using a diagnostic test, check that documentation and media are for the same revision level.

The following documents are required for diagnostic testing:

Title	XDS Publication No.
Sigma 5 and 7 Extended Performance Rapid Access Data (RAD) File, Program No. 704978B, Diagnostic Program Manual	901540
Diagnostic Control Program for Sigma 5 and Sigma 7 Computer Peripheral Device, Reference Manual	900712
Sigma 5 and 7 Relocatable Diagnostic Program Loader, Diagnostic Program Manual	900972
Sigma 2 Relocatable Diagnostic Program Loader, Diagnostic Program Manual	901128
Sigma 2 High Capacity, Rapid Access Data (RAD) File Test, Diagnostic Program Manual	901538

Any failures that cannot be isolated using the diagnostic test programs may be isolated using one or more of the off-line tests.

8-4 BASIC CHECKS AND ADJUSTMENTS

CAUTION

During adjustment procedures, it will be often necessary to remove a module, insert the card extender (XDS part No. 117306), and adjust components of the module. Before removing a module, shut down dc power from the PT20 power supply by setting the circuit breaker to OFF. After inserting the card extender and the module, set the circuit breaker to ON.

8-5 PRELIMINARY OPERATIONS

a. Check that ac power is not connected to the EP RAD storage unit.

b. Check that all cables are installed. (See figures 7-2 and 7-3.)

c. Inspect controller and selection unit for loose wires, bent pins, or other obvious mechanical defects.

d. At the power distribution panel, check that the REMOTE-OFF-ON switch is in the OFF (center) position.

Note

For normal operation, the EMERGENCY USE ONLY circuit breaker is left ON, so that power is always applied to the compressor. For installation or test, the circuit breaker may be set to OFF.

e. At the motor control assembly, check that the POWER switch is OFF, and that the circuit breaker (under the EMERGENCY USE ONLY cover) is OFF.

8-6 POWER TEST

a. Connect the EP RAD storage unit to the ac power source.

b. At the PT20 power supply, set the MARGIN switch to N (normal) and the circuit breaker to ON.

c. At the power distribution panel, set the REMOTE-OFF-ON switch to ON.

Note

If any of the voltages measured are not within ±2 percent of nominal value, adjust as necessary, using the test point of the selection unit as a reference. (Refer to XDS publication No. 901157 for adjustment procedure.)

d. Check the dc voltages of the controller and the selection unit as follows:

Voltage	Controller (UL)	Selection Unit (US)
+4.0	2A-49	20B-49
+8.0	2A-51	21B-51
-8.0	2A-50	20B-50
+25.0	-	20B-45 (21B45)
-25.0	-	20B-41
+45.0	-	21B-46

CAUTION

If the phase relations specified are not correct, the magnetic surface of the disc file and the flying heads may be damaged.

e. Check that the phase relation at TB1 of the power distribution panel is as follows:

Phase	Pin
A	TB-1
B	TB-2
C	TB-3

f. At the motor control assembly, set the circuit breaker (under EMERGENCY USE ONLY cover) to ON. Check that the compressor starts.

g. Set POWER toggle switch to ON. Check that the disc rotates clockwise.

8-7 ADJUSTMENT OF TIMING SIGNALS

a. While observing the output at test point A of the CT10 Clock Oscillator module (controller location 2A), adjust inductor L1 for peak signal amplitude. UL

b. Adjust pulse shape potentiometer R16 for positive pulse width of 140 ±10 ns at pin 2A-34. (See figure 8-1.)

c. Replace CT10 Clock Oscillator module and remove sector/index amplifier P35 from location 1B of the selection unit. Connect sector/index amplifier P35 through the card extender. US

d. Adjust R28 for waveshapes as illustrated in figure 8-2.

e. Synchronize on signal IP (pin 2B-13) and observe signals IP and SP (pin 2B-19). Check that there are 11 SP pulses for each IP pulse and that waveforms are as indicated in figure 8-3. US

Note

If there are not 11 SP pulses for each IP pulse, as indicated, the timing track must be re-recorded, as described in JT18 Operating Procedure, XDS Drawing No. 134293.

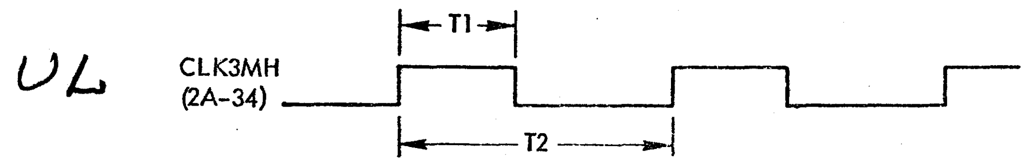
f. Replace sector/index amplifier P35.

8-8 POWER FAIL-SAFE TEST

a. Remove WT29 Power Monitor module from selection unit location 4B.

Note

If adjustment potentiometers of WT29 module have been sealed, skip to step l. If potentiometers have not been sealed, proceed with step b.

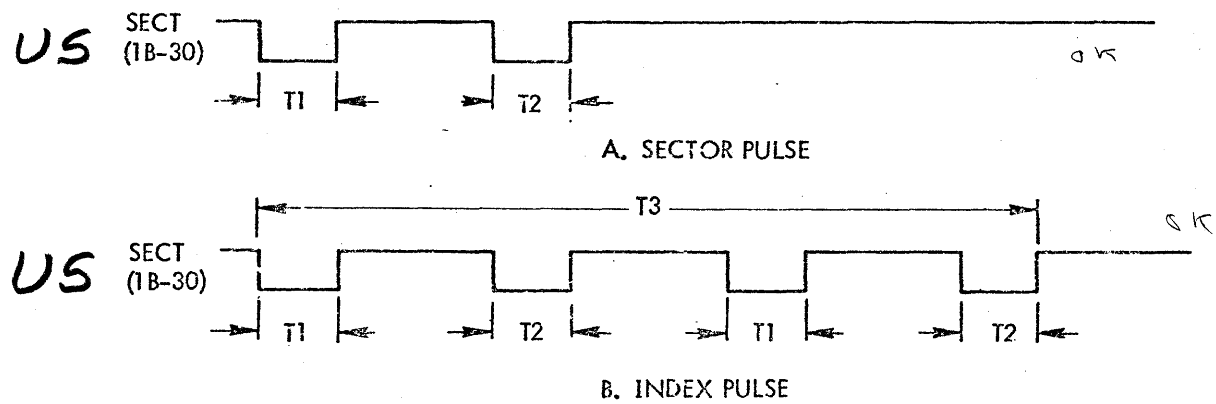


NOTES:

1. ITEMS IN PARENTHESES INDICATE LOCATION IN THE EP RAD CONTROLLER (MODULE - PIN NUMBER)
2. T1 IS 140 ± 10 NS
3. T2 IS 324 TO 336 NS

901565A.813

Figure 8-1. Signal CLK3MH, Timing Diagram



NOTES:

1. ITEMS IN PARENTHESES INDICATE LOCATION IN THE EP RAD SELECTION UNIT (MODULE - PIN NUMBER)
2. T1 IS 400 TO 750 NS
3. T2 IS 500 TO 2500 NS
4. T3 IS 9.5 µS MAXIMUM

901565A.812

Figure 8-2. Signal SECT, Timing Diagram

b. Connect the WT29 Power Monitor module through card extender.

c. Connect a clip lead from pin 4B-44 to pin 4B-45.

d. At the power distribution panel, remove fuse F1.

e. On the WT29 module, adjust R15 until signal AOK (pin 4B-26) just reaches 0.0V. (Normal voltage is +8.0 ±1.0V.)

f. Remove the clip lead installed in step b and replace fuse F1 (removed in step c).

g. Remove the WT29 module (with card extender from location 4B) and place in location 5B.

h. Check that output at pin 26 is normal (+8.0 ±1.9V).

i. Adjust R5 counterclockwise until output level falls to 0V; then adjust R5 slowly clockwise until output level returns to normal range and remains there.

j. Adjust R11 as described in step i for R5.

k. Adjust R19 as described in step i for R5.

l. Replace the WT29 module in location 4B.

m. Check that signal NPDLY (selection unit location 10A-14) is at +4V.

n. Temporarily connect selection unit pin 10A-31 to ground. Check that signal NPDLY falls to 0V.

Note

If 10-second delay is not attained after removal of ground connection in step o, adjust R10 on OT15 10-Second One-Shot module (selection unit location 6B). Use card extender during adjustment.

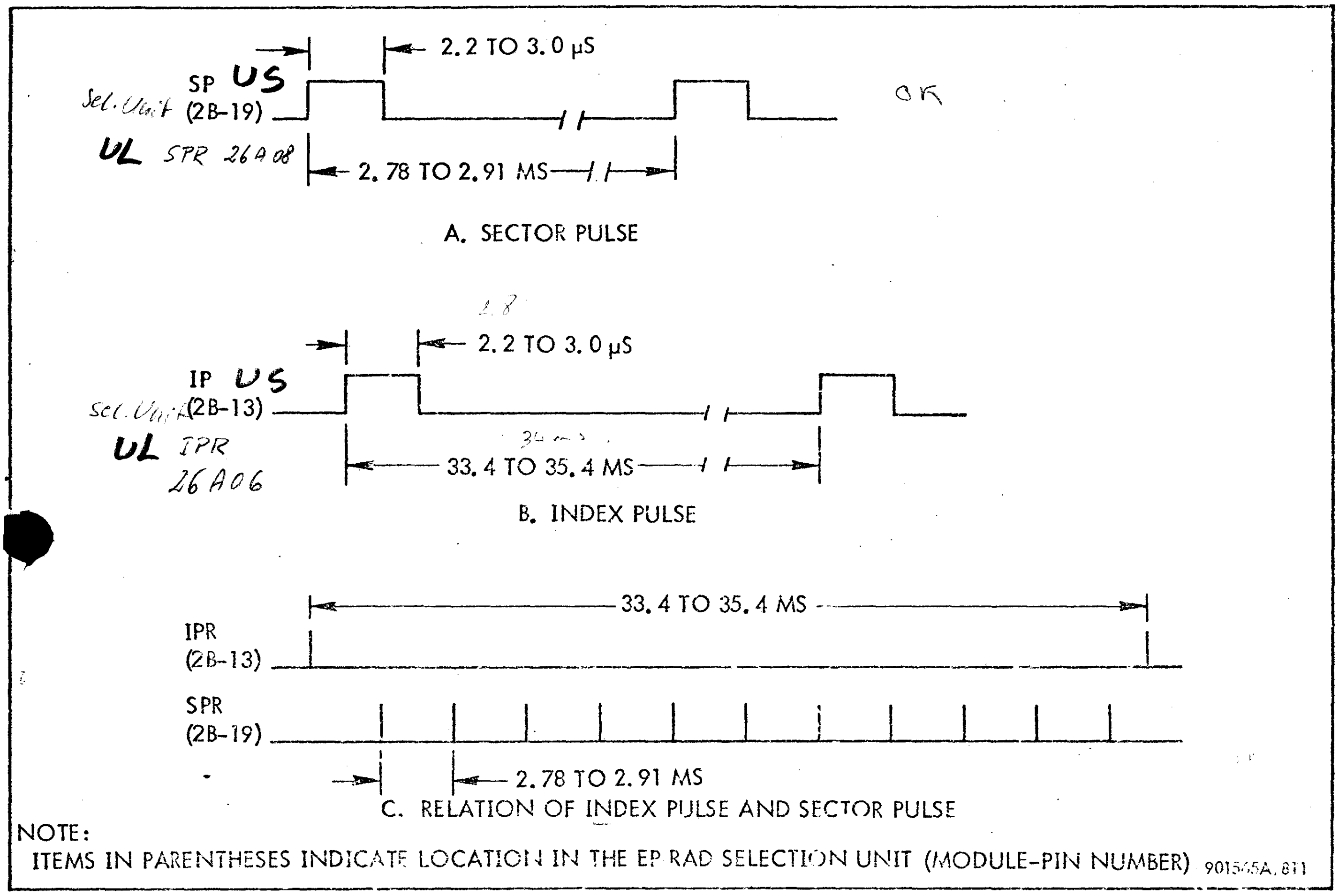


Figure 8-3. Signals SP and IP, Timing Diagram

o. Remove ground connected in step n. Check that NPDLY remains at 0V level for at least 10 seconds following removal of ground connection.

8-9 ADJUSTMENT OF AT41 WRITE CLOCK DRIVER

a. At the power distribution panel, check that the REMOTE-OFF-ON switch is OFF (center).

b. Insert PET connector P181 in controller location 32A.

c. Insert PET connector P183 in controller location 30A.

d. Check that all modules are inserted in controller (figure 7-5) and in selection unit (figure 7-4).

e. Place the PET panel overlay (figure 8-4) over the PET control panel.

f. Set the PET panel ADDRESS switches to the address of the EP RAD storage unit under test.

g. At the controller, place online/offline switch of LT25 Special Purpose Logic module (location 23C) in the 0 position (down). (See figure 2-2.)

h. At PET, place PET/MONITOR switch to PET, place three switches marked with arrows to position indicated by arrowhead, and place all other switches in down position.

i. Apply power to PET.

j. Apply power to the controller and selection unit.

k. Set the following switches in the up position: ORDER 1, SIO, REPEAT, and COUNTER RESET switches 1, 2, 4, 8, 16, and 32.

l. Press and release the RESET pushbutton.

m. Press and release the COUNTER INITIALIZE pushbutton.

n. Press and release the FS pushbutton. Note that the WRITE lamp is lighted, and that the TRACK lamps increment from TRACK lamp 10 lighted (000 0000 0001) to TRACK lamp 5 lighted (000 0010 0000), and repeat.

CAUTION

Remove dc power before removing modules.

o. At controller, remove BT11 Buffered AND Gate module from location 7A.

p. Connect a clip lead from ground to signal REND (pin 7A-1).

q. Connect a clip lead from signal RWCK-3 (pin 2A-10) to signal SC2D (pin 7A-35).

r. At selection unit, remove AT41 Write Clock Driver module from location 18A and connect through card extender.

s. Synchronize on, and display, signal NSC2R (18A-27).

t. Alternately adjust L4 and L6 for maximum sinusoidal amplitude at pin 18A-2.

Note

For jitter test, trigger the oscilloscope on the falling edge of signal MC6 (pin 18A-8). Adjust falling edge of signal MC6 for thinnest trace possible. Use the expanded scale to check the next two falling edges for jitter. Any jitter on these edges will seriously reduce the overall timing margin of the system.

u. Adjust R43 to place the falling edge of signal MC6 within 130 to 140 ns from falling edge of signal NSC2R, as indicated in figure 8-5.

v. If any jitter is observed on signal MC6, readjust L4 a maximum of 1/8 turn in either direction to remove jitter.

w. Recheck the sine wave at pin 18A-2 to check that the amplitude has not decreased.

x. Remove clip leads installed in steps p and q.

y. Replace AT41 module in location 18A.

z. Disconnect PET.

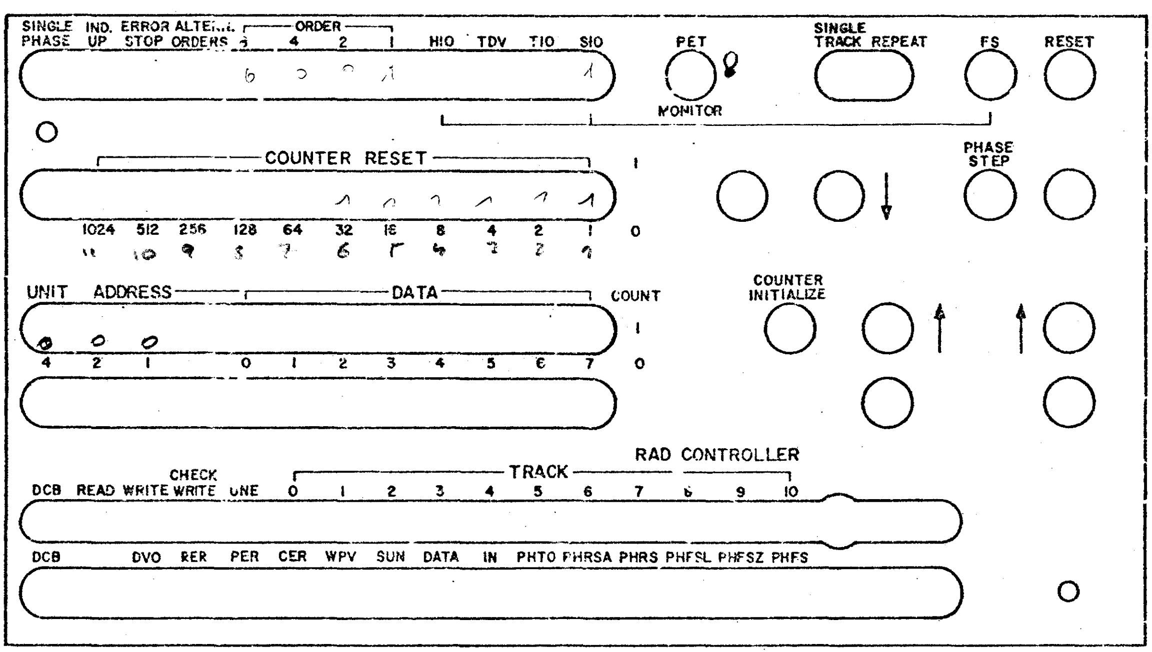
8-10 DATA PATH TIMING ADJUSTMENT

a. At the power distribution panel, check that the REMOTE-OFF-ON switch is OFF (center).

b. Insert PET connector P181 in controller location 32A.

c. Insert PET connector P183 in controller location 30A.

d. Check that all modules are inserted in controller (figure 7-5) and in selection unit (figure 7-4).



NOTE: REFERENCE XDS DWG: 147152-1A

901565A.801

Figure 8-4. PET Panel Overlay

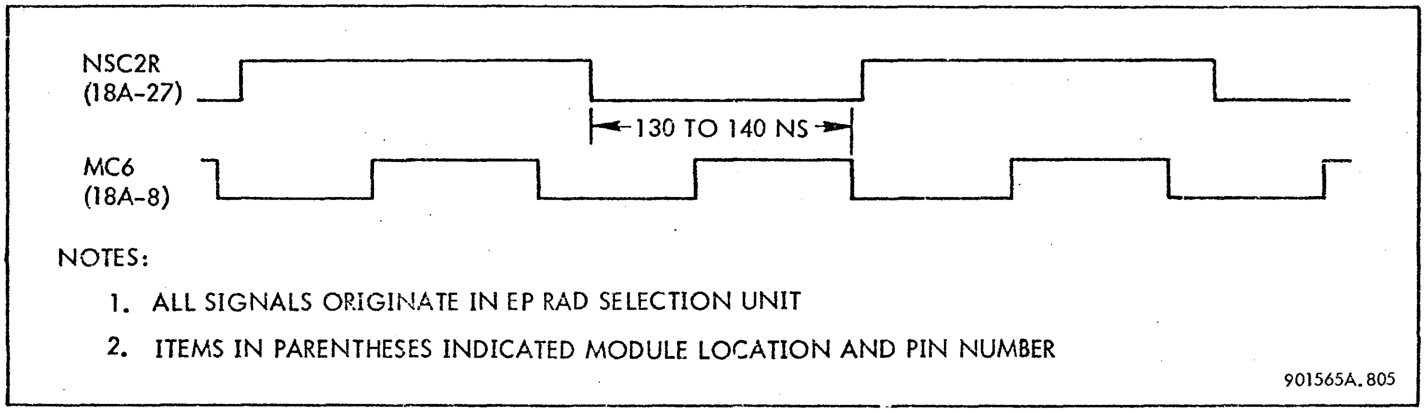


Figure 8-5. Data Clock Signals, Timing Diagram

e. Place PET panel overlay (figure 8-4) over the PET control panel.

f. Set the PET panel ADDRESS switches to the address of the EP RAD storage unit under test.

g. At the controller, place the online/offline switch of the LT25 Special Purpose Logic module (location 23C) in the 0 position (down). (See figure 2-2.)

h. At PET, place the PET/MONITOR switch to PET, place the three switches marked with arrows to the positions indicated by the arrowhead, and place all other switches in the down position.

i. Apply power to the PET.

j. Apply power to the controller and selection unit.

k. Set the following switches in the up position: ORDER 1, SIO, and DATA 1, 3, 5, and 7.

Note

Steps k, l, and m cause a 01010101 pattern to be written on the disc file.

l. Press and release the RESET pushbutton.

m. Press and release the FS pushbutton.

n. At the selection unit, remove the LT85 Pulse Packing Compensator module from location 14A.

Note

Do not replace the LT85 module at this time.

o. Set the following switches in the down position: ORDER 1 and all DATA switches.

p. Set the following switches in the up position: ORDER 2, SINGLE TRACK, REPEAT, and COUNTER RESET 1.

q. Press and release the RESET pushbutton.

r. Press and release the FS pushbutton. Check that the READ lamp is lighted.

Note

Disregard any error indicators.

s. Remove the AT51 Clock Discriminator module from location 15A.

t. Adjust R33 of the AT51 module to the center of its range (approximately 12 turns from either end).

u. Adjust R20 of the LT85 module fully counterclockwise.

v. Adjust the oscilloscope to trigger on signal SP (2B-19), using a timebase of 10 μs/cm.

w. Insert the AT51 module in place (location 15A) using the card extender.

x. Display the data test point (pin 15A-5) on the A-trace of the oscilloscope and trigger the A-trace timebase negative on the data test point signal.

Note

Operate the oscilloscope in the A-delayed-by-B mode, 100 ns/cm.

y. Display the clock test point signal (pin 15A-7). Adjust the delay multiplier of the oscilloscope to view the data pattern close to the preamble.

z. Adjust R33 on the AT51 module for a delay of 230 ±2 ns (A, figure 8-6). Use the expanded scale of the oscilloscope.

aa. Replace the AT51 module in location 15A and insert the LT85 module (location 14A) using the card extender.

ab. While viewing test points of the AT51 module (A, figure 8-6), adjust R20 on the LT85 module for a period of 270 ±2 ns.

ac. Synchronize negative on, and observe, signal DAIR (controller pin 26A-13). Observe signal DSR (controller pin 26A-10). Use an A-timebase of 100 ns/cm.

ad. At the selection unit, replace the LT85 module in location 14A and insert the LT77 Data Decoder module (location 13A), using the card extender.

ae. Adjust R20 on the LT77 module for delay time between signal DAIR and signal DSR (B, figure 8-6).

af. At the PET, set the REPEAT switch to the down position and write data on the entire disc.

ag. Read the contents of the disc. No errors should occur.

8-11 OFFLINE TESTS

Peripheral Equipment Tester Model 7901 (PET) is required to perform offline tests. Offline tests enable the PET to simulate IOP signals and cause the EP RAD file to respond as it would for actual IOP signals. Single-phase operation of the EP RAD file can be controlled from the PET. The PET may also be used to monitor online operation. The PET panel overlay (figure 8-4) is used with the PET during offline testing of the EP RAD file. The functions of switches marked by the PET panel overlay are indicated in table 8-1. Test equipment required for offline testing is listed in table 8-2.

8-12 PRELIMINARY OPERATIONS

a. At the power distribution panel, check that the REMOTE-OFF-ON switch is OFF (center).

b. Insert PET connector P181 in controller location 32A.

c. Insert PET connector P183 in controller location 30A.

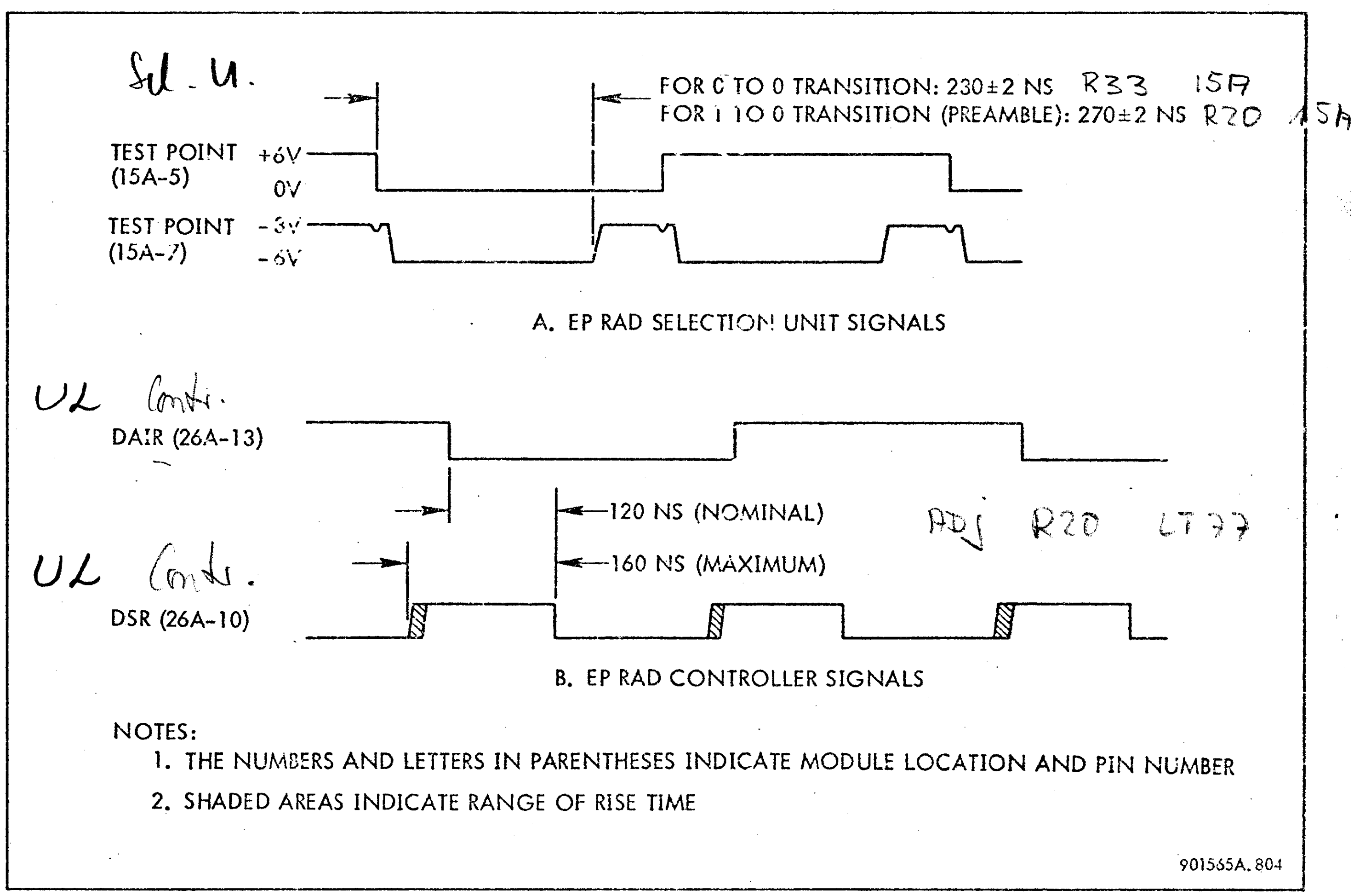


Figure 8-6. Data Synchronization Signals, Timing Diagram

Table 8-1. Functions of PET Panel Overlay Switch Designations

Switch Designation	Function
PET/MONITOR switch	When in PET position, transfers control of EP RAD controller to PET; when in MONITOR position, transfers control of EP RAD controller to IOP, but enables INDICATOR lamps to display state of controller as selected by IND. UP switch
RESET pushbutton	Resets EP RAD controller by generating a true RSTP signal
FS pushbutton	When pressed, simulates function strobe signal by generating a true FSP signal
HIO switch	Simulates function indicator HIOR
TDV switch	Simulates function indicator TDVR
TIO switch	Simulates function indicator TIOR
SIO switch	Simulates function indicator SIOR
SINGLE TRACK switch	Inhibits track register from incrementing by generating a true SGLTRKP signal
REPEAT switch	Permits continuous operation on tracks defined by the SINGLE TRACK switch
ORDER 1 switch ORDER 2 switch ORDER 4 switch ORDER 8 switch	Generate order codes as follows: Order — Switch 8 4 2 1 Write — 0 0 0 1 Seek — 0 0 1 1 Read — 0 0 1 0 Sense — 0 1 0 0 Checkwrite — 0 1 0 1
ALTERN. ORDERS switch	Provides a means of executing an automatic write operation before the order set into the ORDER switches is executed
ERROR STOP switch	Halts the operation being executed when a transmission error is received. When an error is detected, the failing track number is displayed and the sector counter is incremented by one
IND. UP switch	Selects the upper row or lower row of functions to be displayed by the 16 PET indicators
SINGLE PHASE switch	Enables the single phase mode of operation. Used with PHASE STEP pushbutton to progress through an operation one phase at a time
PHASE STEP pushbutton	Provides an enable pulse which generates one clock signal to cause a change of phase in the controller

(Continued)

Table 8-1. Functions of PET Panel Overlay Switch Designations (Cont.)

Switch Designation	Function
COUNTER RESET switches	Select the number of tracks to be operated on. Cause a reset term (RSTP) to be generated when the PET internal counter equals the value set in COUNTER RESET switches
COUNTER INITIALIZE pushbutton	Resets PET internal counter
DATA switches	Simulate IOP data
UNIT ADDRESS switches	Address one of eight storage units
INDICATOR lamps	Display one of two sets of 16 signals from EP RAD controller, depending on position of IND. UP switch
(Arrows)	Not used. Place each switch in position indicated by adjacent arrowhead

Table 8-2. Test Equipment Required for Offline Tests

Equipment	Part No.	Manufacturer
Card Extender	117306	XDS
Timing Track Recorder JT18	134046	XDS
Peripheral Equipment Tester (PET) Model 7901		XDS
PET Panel Overlay	147152	XDS
Oscilloscope	Model 543	Tektronix
Preamplifier	Model 1A1	Tektronix
Volt-ohm-milliammeter	Model 630A	Triplett

d. Check that all modules are inserted in the controller (figure 7-5) and in the selection unit (figure 7-4).

e. Place the PET panel overlay (figure 8-4) over the PET control panel.

f. Set the PET panel ADDRESS switches to the address of the EP RAD storage unit under test.

g. At the controller, place the online/offline switch on the LT25 Special Purpose Logic module (location 23C) in the 0 position (down). (See figure 2-2.)

h. At PET, place the PET/MONITOR switch to PET, place the three switches marked with arrows to the position indicated by the arrow, and place all other switches in the down position.

i. Apply power to the PET.

j. Apply power to the controller and selection unit.

k. Perform testing as required.

8-13 SINGLE PHASE SEQUENCES

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Place the HIO switch and the SINGLE PHASE switch in the up position.

c. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

d. Press and release the FS pushbutton. Note that the PHFS lamp goes off and that the PHFSZ lamp is lighted.

e. Press and release the PHASE STEP pushbutton. Note that the PHFSZ lamp goes off and that the PHFSL lamp is lighted.

f. Press and release the PHASE STEP pushbutton again. Note that the PHFSL lamp goes off, and that the PHFS lamp is lighted.

g. Place the HIO switch in the down position.

h. Place the TDV switch in the up position.

i. Repeat steps c through f.

j. Place the TDV switch in the down position.

k. Place the TIO switch in the up position.

l. Repeat steps c through f.

m. Perform additional testing as required.

8-14 ILLEGAL ORDER SEQUENCE

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Place the SIO switch and the SINGLE PHASE switch in the up position.

c. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

d. Press and release the FS pushbutton. Note that the PHFS lamp goes off and that the PHFSZ lamp is lighted.

e. Press and release the PHASE STEP pushbutton for each step of the following sequence:

Step	Lamps Lighted	Remarks
1	PHFSL	
2	PHFS, DCB, DVO	A successful SIO sets DCB. Order out service cycle (steps 2–7)
3	PHFSZ	
4	PHFSL	
5	PHRSA	
6	PHRS	
7	PHTO	
8	PHFS, DATA, IN	Data in service cycle. Data lamp off. Illegal order sets UNE (steps 8–11)
9	PHFSZ, UNE	
10	PHFSL	
11	PHRS	
12	PHRSA	Data in service cycle. Data lamp off. Illegal order sets UNE (steps 12–14)
13	PHRS	
14	PHTO	
15	PHFS, UNE	Order in service cycle. IN lamp goes off

f. Perform additional testing as required.

Note

Relation between DATA switch settings and bytes of seek order is as indicated in table 8-3.

Table 8-3. Data In Bytes of Seek Order

DATA Switch	Byte 0	Byte 1
0	TOF (track overflow bit)*	T07
1	(not used)* T00	T08
2	(not used)* T01	T09
3	T02	T10
4	T03	S00†
5	T04	S01†
6	T05	S02
7	T06	S03

*If TOF, T00, or T01 true, a sector unavailable error occurs

†If S00 and S01 are both true, a sector unavailable error occurs

8-15 SINGLE PHASE SEEK ORDER

a. Perform the preliminary operations described in paragraph 8-12 unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: SINGLE PHASE, ORDER 1, ORDER 2, SIO, PET.

c. Set DATA switches 3 through 7 to the center position.

d. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

UL

3C38 e. Press and release the FS pushbutton. Note that the PHFS lamp goes off and that the PHFSZ lamp is lighted.

f. Press and release the PHASE STEP pushbutton for each step of the following sequence.

	Step	Lamps Lighted	Remarks
3C17	1	PHFSL	SIO accepted
5C9	2	PHFS, DCB, DVO	
3C38	3	PHFSZ	Order out service cycle
3C17	4	PHFSL	
2C38	5	PHRSA	
2C23	6	PHRS	
13C6	7	PHTO	
5C9	8	PHFS, DATA	Byte one of seek order
3C38	9	PHFSZ	
3C17	10	PHFSL	
2C38	11	PHRSA	
2C23	12	PHRS	
2C38	13	PHRSA	

g. Place the IND. UP switch to the up position. Note that TRACK lamps 2, 3, 4, 5, and 6 are lighted.

h. Set DATA switches 0 through 4, 6, and 7 to the center position, and set DATA switch 5 to the down position.

i. Place the IND. UP switch to the down position.

j. Press and release the PHASE STEP pushbutton. Note that the PHRSA lamp goes off and the PHRS lamp is lighted.

k. Press and release the PHASE STEP pushbutton again. Note that the PHRS lamp goes off and the PHTO lamp is lighted.

l. Place the IND. UP switch to the up position. Note that all TRACK lamps are lighted.

1/1 Ind. UP switch to the down p.

m. Press and release the PHASE STEP pushbutton for each step of the following sequence.

Step	Lamps Lighted	Remarks
1	PHFS, IN	DATA lamp goes off. Order in service cycle
2	PHFSZ	
3	PHFSL	DATA lamp goes off. Order in service cycle
4	PHRS	
5	PHRSA	
6	PHRS	
7	PHTO	
8	PHFS	DCB lamp and IN lamp go off

n. Set DATA switches 0, 1, and 2 to down position; set DATA switches 4 and 5 to center position.

o. Repeat steps d through f. A new seek order with different byte is stored.

p. Repeat steps j, k, and m. Note that lamps SUN and UNE are lighted at step 1 of m. This indicates that a sector unavailable error was detected in the second byte (S00 and S01 both true).

q. Perform additional testing as required.

8-16 SINGLE PHASE SENSE ORDER (04)14C34

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up positions: SINGLE PHASE, ORDER 4, SIO, and PET.

c. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

d. Press and release the FS pushbutton. Note that the PHFS lamp goes off and that the PHFSZ lamp is lighted.

e. Press and release the PHASE STEP pushbutton for each step of the following sequence.

Step	Lamps Lighted	Remarks
1	PHFSL	SIO accepted
2	PHFS, DCB	Order out service cycle
3	PHFSZ	
4	PHFSL	
5	PHRSA	
6	PHRS	

Step	Lamps Lighted	Remarks
7	PHTO	Order out service cycle
8	PHFS, DATA, IN	Data in service cycle (three bytes of sense order)
9	PHFSZ	
10	PHFSL	
11	PHRS	
12	PHRSA	
13	PHRS	
14	PHRSA	
15	PHRS	
16	PHRSA	
17	PHRS	
18	PHTO	
19	PHFS	DATA lamp goes off. Order in service cycle
20	PHFSZ	
21	PHFSL	
22	PHRS	
23	PHRSA	
24	PHRS	
25	PHTO	
26	PHFS	DCB lamp and IN lamp go off

f. Perform additional testing as required.

8-17 REPEAT MODE SEEK ORDER

a. Perform preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: ORDER 2, ORDER 1, SIO, PET, and REPEAT.

c. Press and release the RESET pushbutton.

d. Press and release the FS pushbutton. Note that DCB lamp is lighted.

Note

During step d, the controller cycles continuously through the phases indicated in paragraph 8-15. All lamps listed will be lighted briefly and will appear to be dimly lit.

e. Set the REPEAT switch to the down position. Note that the PHFS lamp is lighted.

f. Set the REPEAT switch to the up position.

g. Press and release the FS pushbutton. Note that the DCB lamp is lighted and that the controller cycles as in step d.

h. Set the IND. UP switch to the up position.

i. Set each DATA switch, one at a time, in turn, to the up position. For each DATA switch, note that the corresponding TRACK lamp, as indicated in table 8-3, is lighted. For DATA switches 0, 1, and 2, note that UNE and SUN are lighted.

j. Perform additional testing as required.

8-18 SINGLE PHASE WRITE ORDER (01) 14C12

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: SINGLE PHASE, ORDER 1, SIO, and PET.

c. Connect a clip lead from ground to SECOMP signal (pin 20A-6) in the controller.

d. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

e. Press and release the FS pushbutton. Note that the PHFS lamp goes off and the PHFSZ lamp is lighted.

f. Press and release the PHASE STEP pushbutton for each step of the following sequence:

Step	Lamps Lighted	Remarks
1	PHFSL	
2	PHFS, DCB	SIO accepted. Order out service cycle, write order stored
3	PHFSZ	
4	PHFSL	

Step	Lamps Lighted	Remarks
5	PHRSA	SIO accepted. Order out service cycle, write order stored
6	PHRS, WRITE	
7	PHTO	
8	PHFS, DATA	Start at data out service cycle
9	PHFSZ	
10	PHFSL	
11	PHRSA	This sequence occurs 16 times to fill the FAM
12	PHRS	
13	PHTO	
14	PHFS	This service call is aborted because the FAM module is filled and no additional service calls are required for data
15	PHFSZ	
16	PHFSL	
17	PHFS	

g. Disconnect clip lead installed in step c.

h. Perform additional testing as required.

8-19 SECTOR COUNTER TEST

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: IND. UP, ORDER 4, SIO, PET, REPEAT, and COUNTER RESET switches 1, 2, 4, 8, 16, and 32.

c. Press and release the RESET pushbutton.

d. Press and release the COUNTER INITIALIZE pushbutton.

e. Press and release the FS pushbutton. Note that the WRITE lamp is lighted, and the TRACK lamps increment from TRACK lamp 10 lighted (000 0000 0001) to TRACK lamp 5 lighted (000 0010 0000).

f. Synchronize on, and display, signal AN0R (controller pin 20A-1).

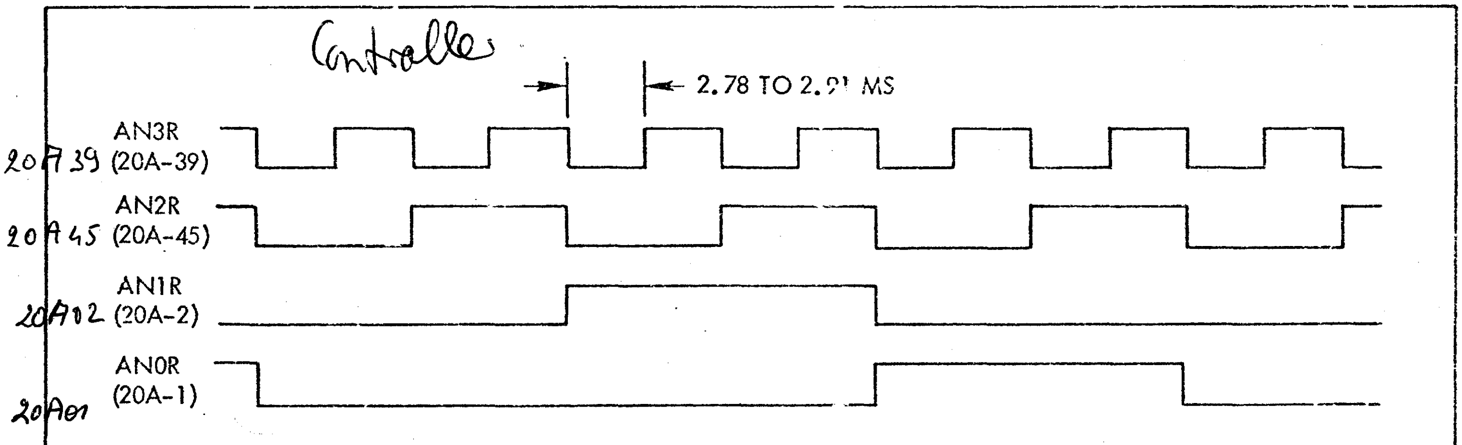
g. Observe signals AN0R through AN3R, as illustrated in figure 8-7.

h. Synchronize on, and display, signal TDT (controller pin 5C-10).

i. Observe signals TDT, TDT1, and TDT2, as illustrated in figure 8-8.

8-20 EXTENDED INTERFACE TEST (TWO-BYTE OPTION)

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

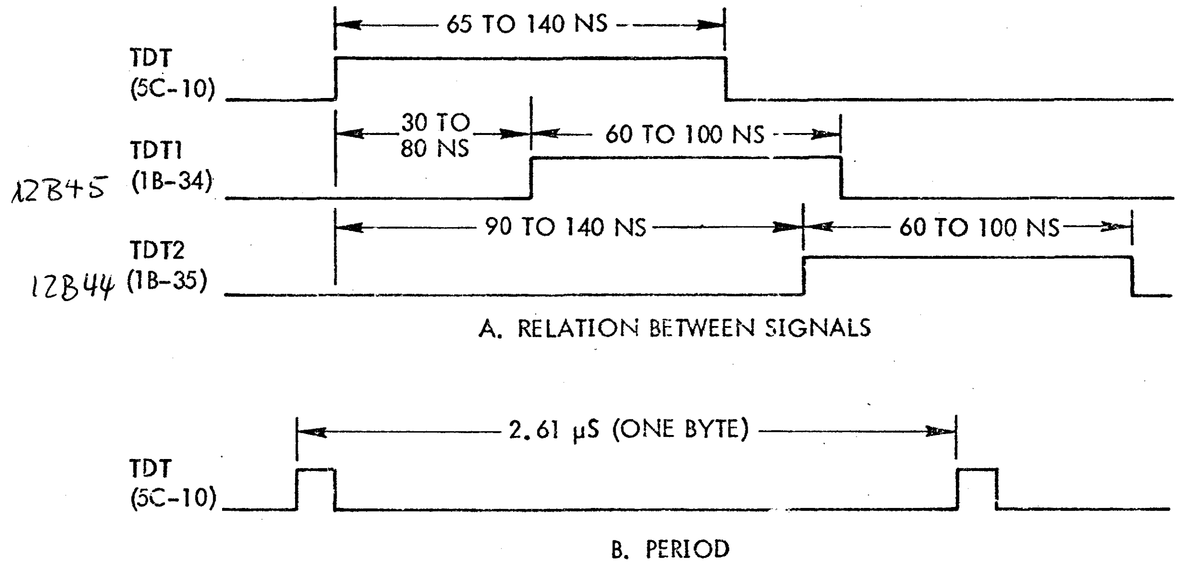


NOTES:

1. ALL SIGNALS ARE GENERATED IN THE EP RAD SELECTION UNIT, BUT ARE MEASURED AT THE INPUT TO THE EP RAD CONTROLLER
2. THE ITEMS IN PARENTHESES INDICATE MODULE LOCATION AND PIN NUMBER

901565A. 807

Figure 8-7. Sector Identification Signals, Timing Diagram



NOTES:

1. ALL SIGNALS ARE GENERATED IN THE EP RAD CONTROLLER
2. THE ITEMS IN PARENTHESES INDICATE MODULE LOCATION AND PIN NUMBER

901565A.806

Figure 8-8. TDL Delay Line Signals, Timing Diagram

b. Set the following switches in the up position: SINGLE PHASE, ORDER-1, SIO, and PET.

c. Connect a clip lead from ground to SECOMP signal (pin 20A-6) in the controller.

d. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

e. Press and release the FS pushbutton. Note that the PHFS lamp goes off and the PHFSZ lamp is lighted.

f. Press and release the PHASE STEP pushbutton for each step of the following sequence.

Step	Lamps Lighted	Remarks
1	PHFSL	
2	PHFS, DCB	
3	PHFSZ	SIO accepted. Order out service cycle, write order stored
4	PHFSL	
5	PHRSA	
6	PHRS, WRITE	SIO accepted. Order out service cycle, write order stored
7	PHTO	
8	PHFS, DATA	Start data out service cycle
9	PHFSZ	
10	PHFSL	
11	PHRSA	This sequence occurs eight times to fill the FAM module
12	PHRS	
13	PHTO	
14	PHFS	This service call is aborted because the FAM module is filled and no additional service calls are required for data
15	PHFSZ	
16	PHFSL	
17	PHFS	

g. Remove clip lead installed during step c.

h. Perform additional testing as required.

8-21 EXTENDED INTERFACE TEST (FOUR-BYTE OPTION)

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in the positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: SINGLE PHASE, ORDER 1, SIO, and PET.

c. Connect a clip lead from ground to SECOMP signal (pin 20A-6) in the controller.

d. Press and release the RESET pushbutton. Note that the PHFS lamp is lighted.

e. Press and release the FS pushbutton. Note that the PHFS lamp goes off and that the PHFSZ lamp is lighted.

Note

For a four-byte interface option, a new service call is requested for each group of four bytes transferred. Therefore, only one sequence of PHRSA, PHRS occurs during the data out service cycle.

f. Press and release the PHASE STEP pushbutton for each step of the following sequence:

Step	Lamps Lighted	Remarks
1	PHFSL	
2	PHFS, DCB	
3	PHFSZ	
4	PHFSL	SIO accepted. Order out service cycle, write order stored
5	PHRSA	
6	PHRS, WRITE	
7	PHTO	
8	PHFS, DATA	Start data out service cycle
9	PHFSZ	
10	PHFSL	
11	PHRSA	
12	PHRS	
13	PHTO	
14	PHFS	

g. Remove clip lead installed during step c.

h. Perform additional testing as required.

8-22 REPEAT MODE WRITE ORDER

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: IND. UP, ORDER 1, SIO, PET, REPEAT, and COUNTER RESET switches 1, 2, 4, 8, 16, and 32.

c. Press and release the RESET pushbutton.

d. Press and release the COUNTER INITIALIZE pushbutton.

e. Press and release the FS pushbutton. Note that the WRITE lamp is lighted and the TRACK lamps increment from TRACK lamp 10 lighted (000 0000 0001) to TRACK lamp 5 lighted (000 0010 0000).

f. Set the REPEAT switch down, then up. Note that TRACK lamp 5 through 10 are lighted (000 0011 1111).

g. Set the REPEAT switch to the up position.

h. Set the SINGLE TRACK switch to the up position.

i. Press and release the FS pushbutton. Note that the WRITE lamp is lighted and that the track register does not count.

j. Set the SINGLE TRACK switch to the down position. Note that the track register increments as in step e.

k. Set the SINGLE TRACK switch to the up position.

l. Set the REPEAT switch to the down position. Note that the track register does not count.

m. Press and release the FS pushbutton. Note that the track displayed is written once, and the operation halts.

n. Perform additional testing as required.

8-23 Y-SELECT TEST

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: IND. UP, ORDER 1, SIO, PET, REPEAT, and COUNTER RESET switches 1, 2, 4, 8, 16, and 32.

c. Press and release the RESET pushbutton.

d. Press and release the COUNTER INITIALIZE pushbutton.

e. Press and release the FS pushbutton. Note that the WRITE lamp is lighted, and the TRACK lamps increment from TRACK lamp 10 lighted (000 0000 0001) to TRACK lamp 5 lighted (000 0010 0000), then repeat.

f. At the selection unit, synchronize oscilloscope negative on signal Y00 (pin 25B-36).

g. Check the outputs of the Y-select drivers at the locations indicated in table 8-4. Outputs should be low (0 to 1V) when selected and high (+45V ±10%) when not selected, as indicated in figure 8-9. Check that the Y-select outputs are low in proper sequence and that only one output is low at any time.

8-24 TCL DELAY LINE TEST

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that

Table 8-4. Locations of Y-Select Output Signals

PIN NO.	MODULE LOCATION							
	25B	24B	23B	22B	10B	9B	8B	7B
36	Y00	Y08	Y16	Y24	Y32	Y40	Y48	Y56
5	Y01	Y09	Y17	Y25	Y33	Y41	Y49	Y57
38	Y02	Y10	Y18	Y26	Y34	Y42	Y50	Y58
6	Y03	Y11	Y19	Y27	Y35	Y43	Y51	Y59
35	Y04	Y12	Y20	Y28	Y36	Y44	Y52	Y60
4	Y05	Y13	Y21	Y29	Y37	Y45	Y53	Y61
37	Y06	Y14	Y22	Y30	Y38	Y46	Y54	Y62
7	Y07	Y15	Y23	Y31	Y39	Y47	Y55	Y63

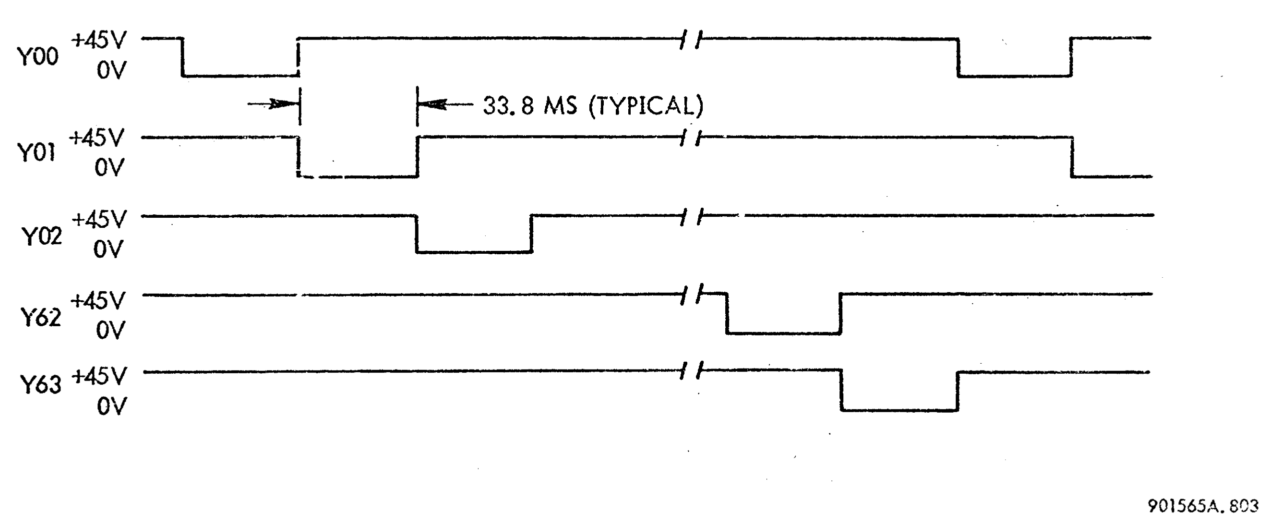


Figure 8-9. Head Select Signals, Timing Diagram

switches are in the positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: ORDER 1, ORDER 2, SIO, and REPEAT.

c. Press and release the RESET pushbutton.

Note

During step d, the controller cycles continuously through the phases indicated in paragraph 8-15. All lamps listed will be lighted briefly and will appear to be dimly lit.

d. Press and release the FS pushbutton. Note that the DCB lamp is lighted.

e. Synchronize on signal DCL (controller pin 4B-15).

f. Check that the phase control delay line timing is as indicated in figure 8-10.

g. Perform additional testing as required.

8-25 TRL DELAY LINE TEST

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: ORDER 1, ORDER 2, SIO, and REPEAT.

c. Press and release the RESET pushbutton.

Note

During step d, the controller cycles continuously through the phases indicated in paragraph 8-15. All lamps listed will be lighted briefly and will appear to be dimly lit.

d. Press and release the FS pushbutton. Note that the DCB lamp is lighted.

e. Set the REPEAT switch to the down position. Note that the PHFS lamp is lighted.

f. Set the IND. UP switch to the up position.

g. Select track 12, sector 3, by setting DATA switches 0 through 7 to positions 1100 0011 (table 8-3).

h. Set the ORDER 2 switch to the down position.

i. Set the following switches to the up position: REPEAT and COUNTER RESET switches 1, 2, 4, 8, 16, and 32.

j. Press and release the RESET pushbutton.

k. Press and release the COUNTER INITIALIZE pushbutton.

l. Press and release the FS pushbutton. Note that the WRITE lamp is lighted, and that the TRACK lamps increment from TRACK lamp 10 lighted (000 0000 0001) to TRACK lamp 5 lighted (000 0010 0000), then repeat the sequence.

m. Synchronize on signal SWRITE (controller pin 10B-2).

n. Check that the TRL delay line is as indicated in figure 8-11.

o. Perform additional testing as required.

8-26 WRITE AMPLIFIER TEST

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches to the up position: ORDER 1, ORDER 2, SIO, and REPEAT.

c. Press and release the RESET pushbutton.

Note

During step d, the controller cycles continuously through the phases listed in paragraph 8-15. All lamps listed will be lighted briefly and will appear to be dimly lit.

d. Press and release the FS pushbutton. Note that the DCB lamp is lighted.

e. Set the REPEAT switch to the down position. Note that the PHFS lamp is lighted.

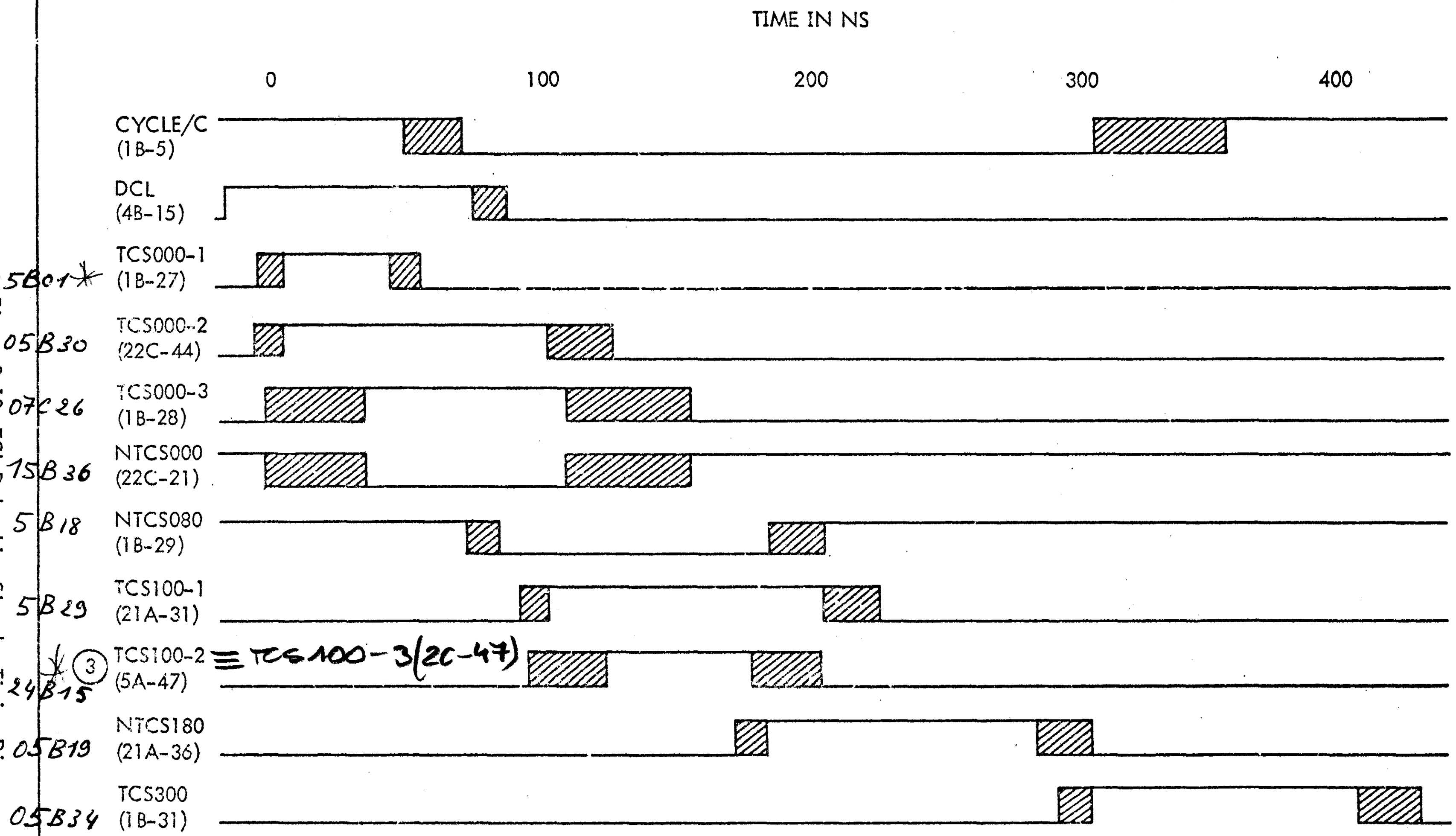
f. Set the ORDER 2 switch to the down position.

g. Set the REPEAT switch to the up position.

h. Set DATA switches 1, 3, 5, and 7 to the center position.

i. Press and release the RESET pushbutton.

j. Press and release the COUNTER INITIALIZE pushbutton.

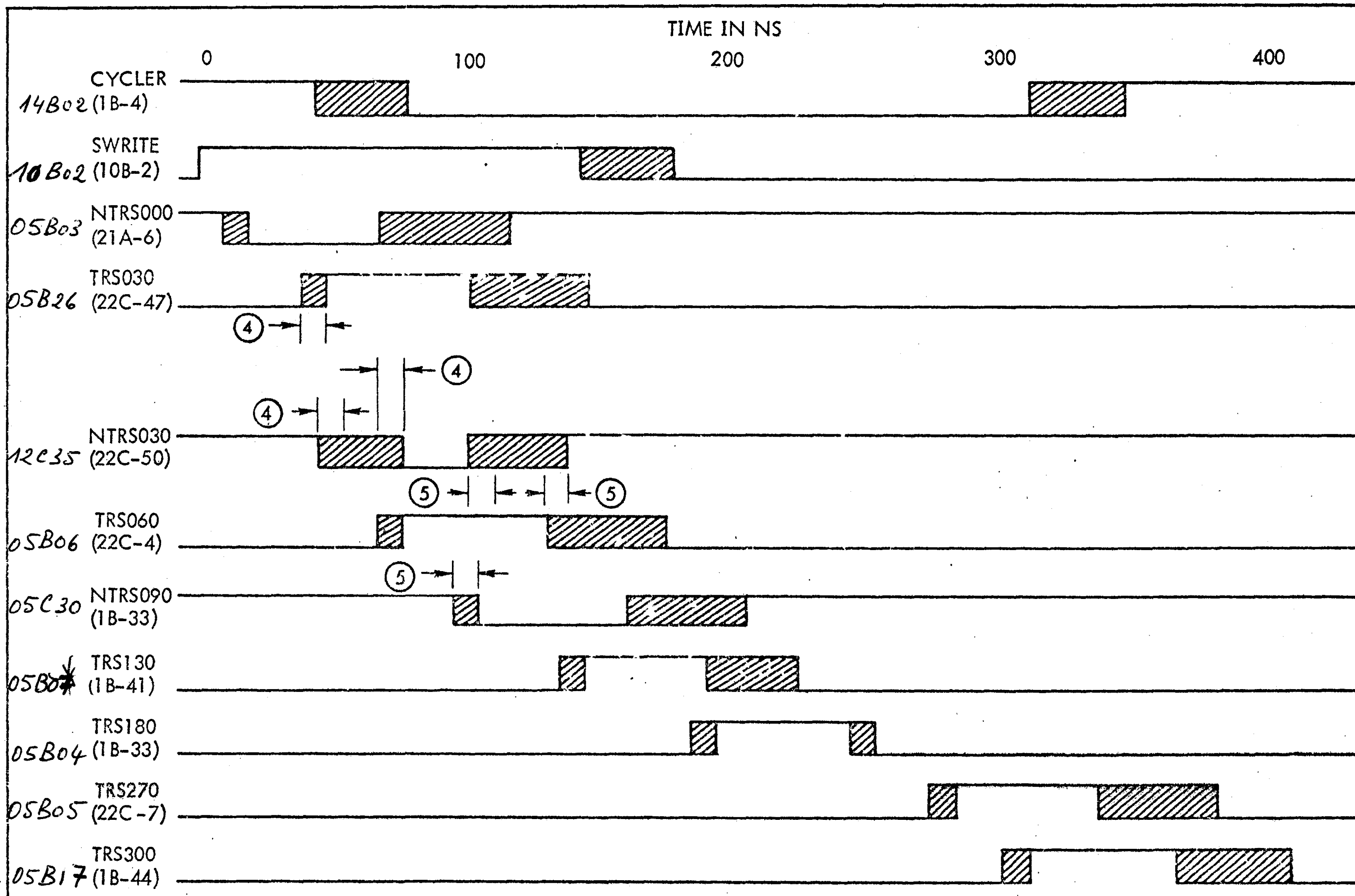


NOTES:

1. THE ITEMS IN PARENTHESES INDICATE MODULE LOCATION AND PIN NUMBER
2. ALL SIGNALS ORIGINATE IN THE EP RAD CONTROLLER
3. SIGNAL TCS100-3 IS IDENTICAL TO SIGNAL TCS100-2, AND CAN BE TESTED AT (2C-47)
4. SHADED AREAS REPRESENT RANGE OF RISE TIME OR FALL TIME

901565A. 808

Figure 8-10. TCL Delay Line Signals, Timing Diagram



NOTES:

1. THE ITEMS IN PARENTHESES INDICATE MODULE LOCATION AND PIN NUMBER
2. SHADED AREAS REPRESENT THE RANGE OF RISE TIME OR FALL TIME
3. ALL SIGNALS ORGINATE IN THE EP RAD CONTROLLER
4. NTRS030 FALL TIME RANGE CORRESPONDS TO TRS030 RISE TIME RANGE PLUS DELAY
5. NTRS030 RISE TIME RANGE CORRESPONDS TO NTRS090 FALL TIME RANGE PLUS DELAY

901565A.809

Figure 8-11. TRL Delay Line Signals, Timing Diagram

k. Press and release the FS pushbutton.

l. Synchronize delayed on signal PSPB (controller pin 7A-34).

m. Synchronize internally on signal WRTAMP1 (selection unit pin 21B-26) and signal NWRTAMP1 (selection unit pin 21B-39) and display the signals. Check that these signals are complements of one another and that WRTAMP1 is as indicated in figure 8-12.

n. Set the REPEAT switch to the down position.

o. Set the ORDER 2 switch to the up position.

p. Set DATA switches 0 through 7 to the center position.

q. Repeat steps c through f.

r. Set DATA switches 0, 2, 4, and 6 to the down position.

s. Repeat steps i through l.

t. Synchronize internally on signal WRTAMP2 (selection unit pin 11B-26) and signal NWRTAMP2 (selection unit pin 11B-39) and display the signals. Check that these signals are complements of one another and that WRTAMP2 is as indicated in figure 8-12.

u. Display signal BIT7RWE (controller pin 13A-14) with signal DATR (selection unit pin 3A-6).

Note

Check that DATA switch 7 changes the data at bit time 0, DATA switch 6 changes the data at bit time 1, and so forth until DATA switch 0 changes the data at bit time 7.

v. Change each DATA switch in turn, and check that each switch controls one bit of information per byte, as shown in figure 8-13.

w. Perform additional testing as required.

8-27 CHECKWRITE TEST

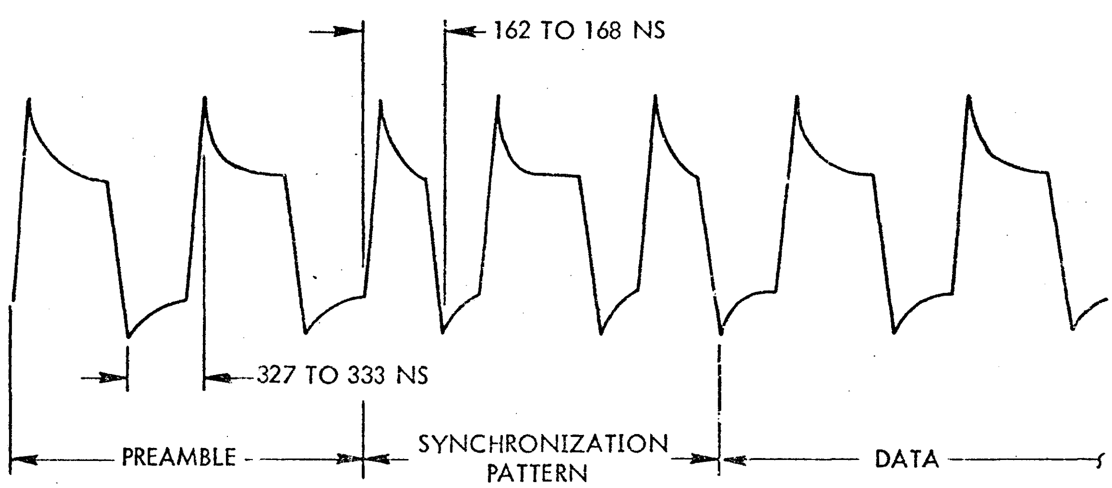
a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches in the up position: ORDER 1, ORDER 2, SIO, and REPEAT.

c. Press and release the RESET pushbutton.

Note

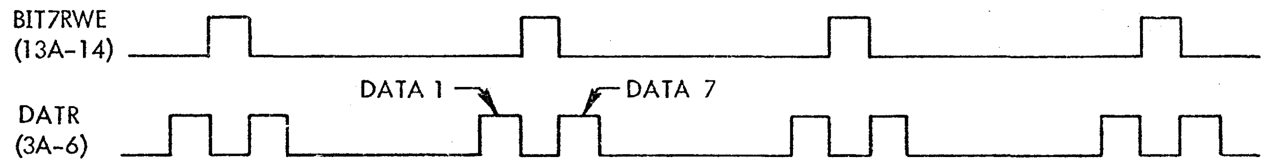
During step d, the controller cycles continuously through the phases listed in paragraph 8-15. All lamps listed will be lighted briefly and will appear to be dimly lit.



NOTE:
PEAK-TO-PEAK VOLTAGE IS 20 TO 30V

901565A.802

Figure 8-12. Write Amplifier Output Signals, Timing Diagram



NOTES:

1. BIT7RWE IS GENERATED IN THE EP RAD CONTROLLER
2. DATR IS GENERATED IN THE EP RAD SELECTION UNIT
3. THE ITEMS IN PARENTHESES INDICATE THE MODULE LOCATION AND PIN NUMBER

901565A.810

Figure 8-13. Data Path Timing Signals, Timing Diagram

d. Press and release the FS pushbutton. Note that the DCB lamp is lighted.

e. Set the REPEAT switch to the down position. Note that the PHFS lamp is lighted.

f. Set DATA switches 0, 1, 4, and 5 to the center position.

g. Set the following switches to the up position: IND. UP, REPEAT, and COUNTER RESET switches 1, 2, 4, 8, 16, 32, 64, 128, and 256.

h. Set the ORDER 2 switch to the down position.

i. Press and release the RESET pushbutton.

j. Press and release the COUNTER INITIALIZE pushbutton.

k. Press and release the FS pushbutton. Note that the WRITE lamp is lighted and that TRACK lamps increment from all off lamps to all lighted lamps, and repeat.

l. Set the REPEAT switch to the down position. Note that the PHFS lamp is lighted. +IND. DOWN

m. Set the ORDER 2 switch to the up position.

n. Set the REPEAT switch to the up position.

o. Repeat steps c through e.

p. Set the ORDER 2 switch to the down position.

q. Set the ORDER 4 switch to the up position.

r. Set the REPEAT switch to the up position.

s. Repeat steps i through k. The CHECKWRITE lamp is lighted, the TRACK lamps increment, and no error lamps are lighted. +IND. UP

t. After the entire disc has been checked (approximately 16 seconds) set the REPEAT switch to the down position. Note that the PHFS lamp is lighted.

u. Set DATA switch 4 to the down position.

v. Set the REPEAT switch to the up position.

w. Repeat steps i through k. Lamps CER and UNE are lighted, indicating a checkwrite error and an unusual end.

x. Perform additional testing as required.

8-28 ALTERNATE ORDERS MODE, REPEATED OPERATION

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the following switches to the up position: IND. UP, ALTERN. ORDERS, ORDER 4, ORDER 1, SIO and REPEAT.

c. Set the ERROR STOP switch in the up position, unless reset at error detection is desired.

d. Set the DATA switches to the eight-bit pattern selected for writing.

e. Set the COUNTER RESET switches to the number of the highest track into which data is to be written.

f. Press and release the RESET pushbutton.

g. Press and release the COUNTER INITIALIZE pushbutton.

Note

Following step h, a write order will be executed (WRITE lamp lighted) and the pattern established in step d will be written in track 0. After the write order is executed, a checkwrite order will be executed (CHECKWRITE lamp lighted). If the ERROR STOP switch is up, detection of errors will cause reset of the track register and automatic rewriting of data on the disc. If the ERROR STOP switch is down, the track register will be reset at the track address established in step d, and the operation will repeat from track 0.

h. Press and release the FS pushbutton.

i. Perform additional testing as required.

8-29 ALTERNATE ORDERS MODE, SINGLE TRACK OPERATION

a. Perform the preliminary operations described in paragraph 8-12, unless previously done. Check that switches are in positions noted in steps e through h of paragraph 8-12.

b. Set the COUNTER RESET switches to the track number to be tested.

c. Set the following switches in the up position: ORDER 1, SIO, REPEAT, and IND. UP.

d. Press and release the COUNTER INITIALIZE pushbutton.

e. Press and release the RESET pushbutton.

f. Press and release the FS pushbutton. Note that the operation halts with the track number selected in step b displayed on the TRACK lamps.

g. Set the DATA switches to any eight-bit pattern.

h. Set all COUNTER RESET switches to the down position.

i. Set the following switches in the up position: ORDER 4, ERROR STOP, ALTERN. ORDERS, and SINGLE TRACK.

Note

Do not press RESET pushbutton.

j. Press the FS pushbutton. Note that the WRITE lamp and the CHECKWRITE lamp are lighted and that the TRACK lamps do not increment.

k. Perform additional testing as required.

8-30 CPU MODE TESTS

The following machine language programs can be used to [test] the EP RAD file.

8-31 SIGMA 5 OR SIGMA 7 MACHINE LANGUAGE TEST PROGRAM

Table 8-5 defines a simple machine language program that can be used for basic troubleshooting of the EP RAD controller. When run, the program causes a continual start of an input/output operation (SIO), followed by a halt of the input/output operation (HIO) after a controlled delay. Signals of the EP RAD controller may be read continually as the program repeats.

8-32 SIGMA 2 MACHINE LANGUAGE TEST PROGRAM

Table 8-6 defines a simple machine language program that can be used for basic troubleshooting of the EP RAD file. When run, the program seeks sector 0, track 0, writes 360 bytes, then seeks sector 0, track 0 again and checkwrites 360 bytes. The starting address is 0100 (hexadecimal). The instructions used are described in table 8-7. For more detailed information, refer to XDS publication No. 900964. The program of table 8-6 will be run once. To cause continual recycling, change the contents of the last address as indicated.

8-33 REPAIRS, REPLACEMENTS, AND ADJUSTMENTS
8-33A. Tachometer OUTPUT VOLTAGE TEST Programm (Page 8-22A)
8-34 REPLACEMENT OF THE DRIVE MOTOR STATOR

Replace the drive motor stator as follows:

CAUTION

Study the entire procedure before attempting replacement. Do not loosen any bolts or screws on the RAD bulkhead because this will cause severe damage to the disc file.

a. At the motor control assembly, set the POWER switch to OFF.

b. After the disc has come to a complete halt, set the circuit breaker under the EMERGENCY USE ONLY cover to OFF.

c. Pull the bulkhead assembly forward and drop the front legs down to support the extended bulkhead assembly (figure 7-1).

d. Loosen and remove the four Allen screws that secure the brake and tachometer assembly to the end of the motor housing (see section IX). Remove the brake and tachometer assembly from the motor housing, leaving the stator wires attached.

e. Loosen and remove the four Allen screws that secure the stator to the motor housing and the motor housing to the spindle housing. Remove the motor housing and stator from the spindle housing with the brake and spindle

INSTRUCTIONS (Cont.)

8-32A TACHOMETER OUTPUT VOLTAGE TEST PROCEDURE

The tachometer generates an output of seven volts per 1000 rpm. The normal output at RAD operating speed is approximately 12 vdc and should not drop below 10 vdc. Voltages lower than 10 vdc can cause problems during start-up. Noise spikes greater than 10 vdc can cause data errors.

The tachometer output voltage should be checked on a monthly basis as follows:

a. Connect the oscilloscope ground probe to the white wire on the tachometer and the signal probe to the blue wire on the tachometer.

b. At RAD operating speed any tachometer with an output of less than 10 vdc or with noise spikes greater than 10 vdc should be replaced. There will be some ripple, which is normal. If there is no output, inspect the tachometer shaft coupling for possible failure.

CAUTION

During the replacement of a tachometer, use care when removing the three No. 2 screws (XDS part No. 123054-104) that attach the adapter plate to the tachometer. These screw heads can be easily damaged due to the torque required to overcome the Loctite applied to their threads. The application of Loctite has now been discontinued, therefore it should not be used when installing the adapter plate on a new tachometer. (See figure 9-5 for assembly drawing).

Table 8-5. EP RAD File Program for Continuous Test (Sigma 5 or Sigma 7)

Memory Location*	Contents*	Remarks
0008	2200 0100	Load immediate (LI). The value 0000 0100, which is the address of the first half of the command doubleword, is stored in general register 0. (For doubleword addressing, 0200 is addressed as 0100)
0009	2220 XXXX	Load immediate (LI). The value 0000 XXXX, which controls the number of counts in the delay introduced by the BDR instruction, is stored in general register 2. (A typical value for XXXX is 0200)
000A	4C00 0YYY	Start input/output operation (SIO). The value YYY must address the EP RAD controller
000B	6420 000B	Branch on decrementing register (BDR). The value in general register 2 is reduced by one. If the value is then positive, the BDR instruction is repeated (location 000B). When the value is zero, the instruction in location 000C is executed
000C	4F00 0YYY	Halt input/output operation (HIO). The operation started by the instruction in location 000A is halted
000D	6800 0009	Branch on conditions reset (BCR). The logical product of the R-field of this instruction (0) and the condition code, which is always zero, causes the instruction in memory location 0009 to be executed
0200	OOXM MMMM	First half of command doubleword. Character X has no significance. Characters M MMMM represent the memory byte address at which the SIO instruction will start processing information. Characters OO represent one of six EP RAD file order codes, as follows: Code — Order X'01' — Write X'02' — Read record X'12' — Read sector X'03' — Sense X'04' — Seek X'05' — Checkwrite
0201	FFXX BBBB	Second half of command doubleword. Characters XX have no significance. Characters BBBB represent the byte count (number of bytes to be written, read, or checked by write order, read order, or checkwrite order). Characters FF represent flag codes, but may be set to 00 for this test. (Refer to XDS publication No. 900950 and 900959 for flag codes in normal operation)

* Memory location and contents are in hexadecimal notation

Table 8-6. Sigma 2 Machine Language Test Program for EP RAD File

Memory Location*	Contents*	Mnemonic	Remarks
0000	400A	B	Branch to first instruction
0001	0003	WD	Order byte for seek
0002	0001	WD	Order byte for write
0003	0005	WD	Order byte for checkwrite
0004	0169	WD	Byte count for write and checkwrite
0005	0003	WD	Byte count for seek
0006	00FD	WD	Starting address for seek
0007	00FF	WD	Starting address for write and checkwrite
0008	0000	WD	Track to sector
0009	0090	WD	RAD device number (90)
000A	8006	LDA	Load seek starting address
000B	000A	WD	Load starting address in I/O register A
000C	8005	LDA	Load seek byte count
000D	000B	WD	Store byte count in I/O register B
000E	8001	LDA	Load order byte for seek
000F	E0FD	STA	Store order byte in table I/O for starting address
0010	8009	LDA	Load RAD device number
0011	1041	RD	Start seek operation (SIO)
0012	1042	RD	Test for comparison (TIO)
0013	6202	BNC	Branch if complete (address +2)
0014	49FE	B	Branch back if not complete (address -2)
0015	8007	LDA	Load write starting address
0016	000A	WD	Load starting address in I/O register A
0017	8004	LDA	Load byte count
0018	000B	WD	Store byte count in I/O register B
0019	8002	LDA	Load write order byte
001A	E0FF	STA	Store order byte in I/O table starting address

* Memory locations and contents are in hexadecimal notation

(Continued)

Table 8-6. Sigma 2 Machine Language Test Program for EP RAD File (Cont.)

Memory Location*	Contents*	Mnemonic	Remarks
001B	8009	LDA	Load RAD device number
001C	1041	RD	Start write (SIO)
001D	1042	RD	Test for comparison (TIO)
001E	6202	BNC	Branch if complete (address +2)
001F	49FE	B	Branch back if not complete (address -2)
0020	8007	LDA	Load starting address for checkwrite
0021	000A	WD	Store starting address in I/O register A
0022	8004	LDA	Load byte count
0023	000B	WD	Store byte count in I/O register
0024	8003	LDA	Load order byte for checkwrite
0025	E0FF	STA	Store order byte in table I/O starting address
0026	8009	LDA	Load RAD device number
0027	1041	RD	Start checkwrite (SIO)
0028	1042	RD	Test for comparison (TIO)
0029	6202	BNC	Branch if checkwrite complete (address +2)
002A	49FE	B	Branch back if checkwrite not complete (address -2)
002B†	00D0	WD	End of program

* Memory locations and contents are in hexadecimal notation

† To cause the program to recycle continually, change the contents of memory location 002B to 400A. This commands a branch to the first instruction as in memory location 0000

Table 8-7. Instructions Used in Sigma 2 Test Program

Mnemonic	Operation
B	BRANCH. The effective address is loaded into the program address register (general register 1). The next instruction is accessed from the location pointed to by the effective address of the branch instruction
BNC	BRANCH IF NO CARRY. The branch condition is true only if the carry indicator is reset (0)
LDA	LOAD ACCUMULATOR. The effective word is loaded into the accumulator (general register 7)
RD	READ DIRECT. The contents of the effective location are interpreted by mode (bits 0 through 3) and function (bits 4 through 15) for read direct operations

(Continued)

Table 8-7. Instructions Used in Sigma 2 Test Program (Cont.)

Mnemonic	Operation
STA	STORE ACCUMULATOR. The contents of the accumulator (general register 7) are stored into the effective location
WD	WRITE DIRECT. The contents of the effective location are interpreted by mode (bits 0 through 3) and function (bits 4 through 15) for write direct operations

attached. This removal may require some effort as the end of the motor housing is tightly fitted into a lip in the spindle housing.

f. Position the stator and motor housing on the spindle housing so that the four mounting holes in the stator are aligned with the four tapped holes in the spindle housing. Install and tighten the four Allen screws that were removed in step e.

g. Loosen and remove the three Allen screws that secure the tachometer to the brake and tachometer assembly. Remove the tachometer from the assembly.

h. Mount the brake and tachometer assembly on the end of the motor housing. Install and tighten the four Allen screws that were removed in step d.

Note

Make sure that the fork on the tachometer is properly inserted.

i. Mount the tachometer on the brake and tachometer assembly by first inserting the tachometer shaft into the shaft coupler and then aligning the three holes in the tachometer base with the three tapped holes in the brake and tachometer assembly. Install and tighten the three Allen screws that were removed in step g.

j. Push the bulkhead assembly back into the RAD storage unit and raise the front legs.

Note

If the RAD storage unit aborts following the turn-on procedure of steps k and l, check the coupling between the tachometer and the coupling shaft.

k. At the motor control assembly, set the circuit breaker under the EMERGENCY USE ONLY cover to ON.

l. Set the POWER switch to ON.

8-35 ADJUSTMENT OF THE DISC FILE BRAKE

a. At the motor control assembly, set switch S1 to OFF.

Note

Wait until the disc has stopped before proceeding.

b. Set the circuit breaker (under the EMERGENCY USE ONLY cover) to OFF.

c. Disconnect the EP RAD file from the 208V three-phase source.

CAUTION

Use the feet at the base of the disc file to support the file when it is in the extended position (figure 7-1). Place plates on the floor to protect the floor from the feet, if necessary.

d. Pull the disc file forward, and set the adjustable feet on the floor.

e. Remove relay K7 to prevent the application of power to the disc file motor.

f. Connect a jumper from the +4V connection on the selection unit (E2, E4, or E6) to terminal board TB1-E4.

WARNING

DO NOT REACH INTO THE MOTOR CONTROL ASSEMBLY AFTER POWER HAS BEEN CONNECTED.

g. Connect the EP RAD file to the 208V three-phase power source.

h. At the motor control assembly, set the circuit breaker to ON.

i. Set switch S1 to ON. Note that the disc file brake retracts.

j. Measure the gap between the armature and friction brake at all four cutouts in the brake collar. The gap should be 0.010 in. to 0.015 in. Adjust the gap as described in steps k and l.

0.25 mm

k. Loosen each of four slot-head screws two turns.

Note

The gap changes by 0.015 in. for each 1/4 turn of the brake collar.

l. To increase the gap, rotate the brake collar clockwise; to decrease the gap, rotate the brake collar counterclockwise.

m. At the motor control assembly, set switch S1 to OFF.

n. Set the circuit breaker to OFF.

o. Disconnect the EP RAD file from the 208V three-phase source.

p. Replace relay K7 (removed in step e).

q. Remove the jumper connected in step f.

r. Connect the EP RAD file to the 208V three-phase source.

s. At the motor control assembly, set the circuit breaker to ON.

t. Set switch S1 to ON.

8-36 REPLACEMENT OF THE DISC FILE BRAKE LININGS

a. Remove the power from the EP RAD file and prepare for replacement by performing steps a through i of paragraph 8-35.

CAUTION

Do not attempt to remove the brake assembly with the power off.

b. Remove three Allen-head screws at the back of the brake assembly and remove the tachometer.

c. Remove four slot-head screws and remove the brake assembly.

Note

Replace the brake linings with XDS part number 147222-002 even if the part replaced has a different number. If necessary, adjust the brake collar to allow for increased thickness of the new lining.

d. Replace brake linings.

e. Measure and adjust the gap as described in steps k and l of paragraph 8-35.

CAUTION

Never remove power from the brake unless the four brake housing screws are secure.

f. Replace the brake assembly and tighten the four slot-head screws.

Note

Replace the tachometer coupling with XDS part number 149272, even if the part replaced has a different number.

g. Engage the slotted tachometer drive and coupling with the pin on the end of the motor shaft (see section IX).

h. Replace the tachometer and tighten the three Allen-head screws.

i. At the motor control assembly, set switch S1 to OFF.

Note

Wait until the disc has stopped before proceeding.

j. Perform steps n through t of paragraph 8-35.

8-37 RAD FILTER REPLACEMENT

These instructions are applicable to motor control unit, part number 146485 and to motor control unit, part number 152692.

The motor control unit, part number 146485 is equipped with three separate filters, two charcoal and one absolute, that must be replaced periodically. See table 8-7A.

The motor control unit, part number 152692, is equipped with two separate filters, one charcoal and one absolute, which must be replaced once a year. See table 8-7B.

In some cases the absolute filter, part number 158947, has an additional part number on the identifying label. It is assumed to be a vendor part number.

Always order the XDS part number.

Table 8-7A. Replacement Filter Part Numbers for Motor Control Unit, Part Number 146485

Item Number	Service Frequency	Number Required	Part	Part Number	Comments
1	90 Days	2	Charcoal Filter	132514	One gasket, item 2 should be installed with each filter every time it is replaced
2	90 Days	2	Gasket	132744	See Comment, Item 1
3	1 Year	1	Absolute Filter	158947	This item, which is to be used in place of assembly part number 129666, is a complete assembly

Table 8-7B. Replacement Filter Part Numbers for Motor Control Unit, Part Number 152692

Item Number	Service Frequency	Number Required	Part	Part Number	Comments
1	1 Year	1	Charcoal Filter	145527	This is a complete item
2	1 Year	1	Absolute Filter	158947	This is a complete item The number, 1024514, which may appear on the label, is assumed to be a vendor part number

8-38 RAD INTERFACE CONNECTOR CLEANING PROCEDURE

The RAD interface connectors, which are mounted on top of the disc file, are to be cleaned as follows:

CAUTION

Use only isopropyl alcohol (filtered) and a typewriter cleaning brush for this procedure. Any other materials may contaminate the connectors.

a. At the motor control assembly, set the POWER switch to OFF.

b. Check that the disc is not rotating and that the compressor is running.

Note

Do not dip the brush in the alcohol, as this action will contaminate the alcohol.

c. Pour sufficient alcohol over the brush to remove flux and other soluble contaminants from the brush.

d. Pour additional alcohol over the brush and shake out the excess by striking the brush handle against a sharp corner.

e. Brush both parts of the connector parallel to the long dimension of the connector.

f. Repeat steps c through e, so that the connector is cleaned with at least two applications of alcohol.

g. Remate the connectors as soon as possible after cleaning.

h. At the motor control assembly, place the POWER switch to ON. Check that the disc rotates.

8-39 SELECTION OF A SPARE WRITE CLOCK

When necessary, select a spare write clock as follows:

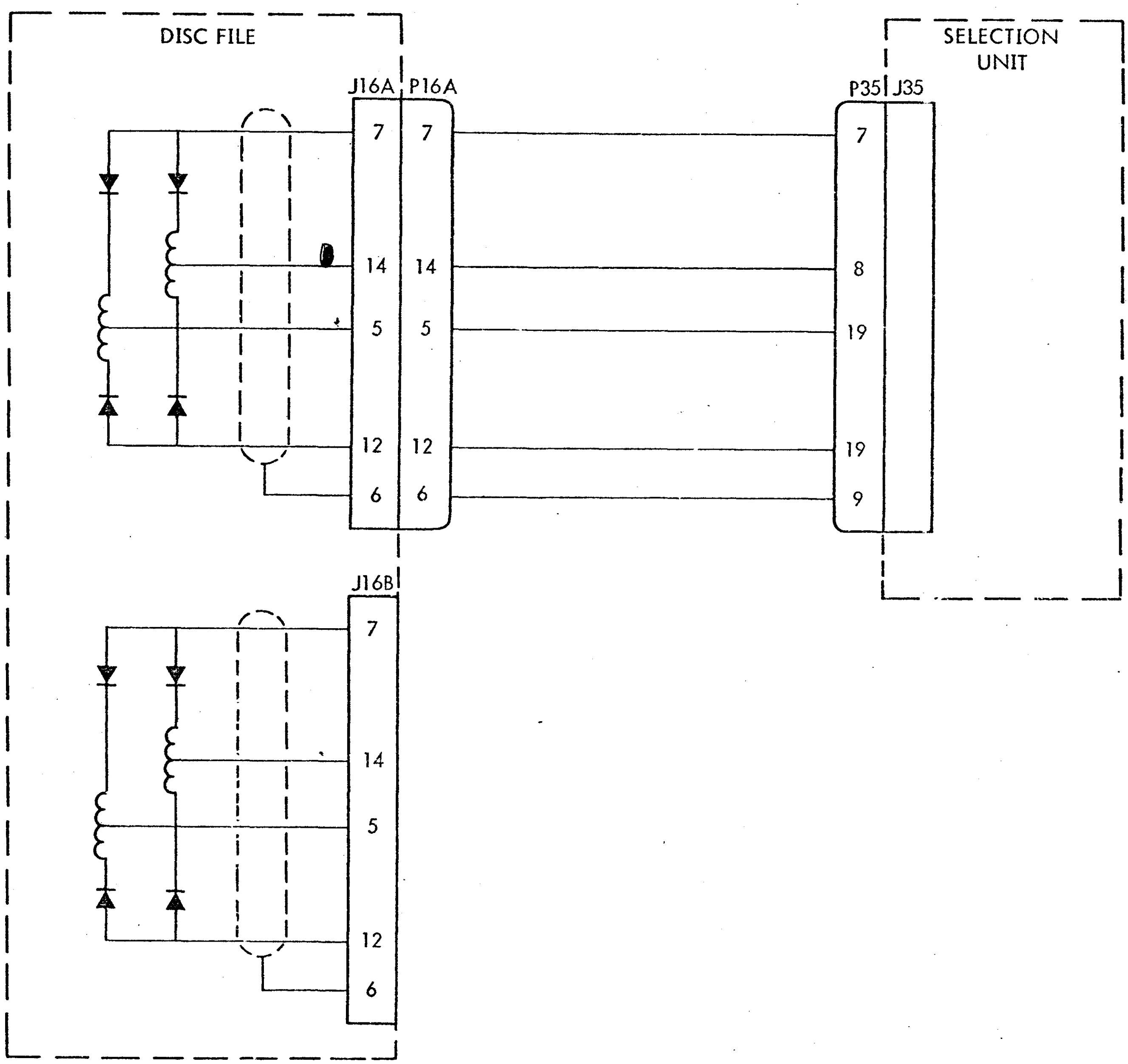
a. Check the maintenance log to determine if spare write clock sources are available.

b. At the motor control assembly, set the POWER switch to OFF.

c. Check that the disc is not rotating and that the compressor is running.

Note

Write clock signals are available from four heads, as indicated in figure 8-14.



NOTES:

1. J16A-14 IS ACTIVE WRITE CLOCK TRACK
2. J16A-5, J16B-14, AND J16B-5 ARE SPARE WRITE CLOCK TRACKS
3. WIRE FROM P16A-5 TO P35-19 MAY BE DISCONNECTED

901565A. 815

Figure 8-14. Write Clock Tracks, Schematic Diagram

d. If possible, select a spare write clock by disconnecting P16A from J16A and inserting it in J16B (or by disconnecting P16A from J16B and inserting it in J16A).

e. If necessary, rewire connector P16A to select the write clock signal from pin 5 instead of pin 14 (or pin 14 instead of pin 5).

f. If rewiring is necessary, insert P16A in J16A or J16B.

g. At the motor control assembly, place the POWER switch to ON. Check that the disc rotates.

8-40 LOGICAL SPARING OF READ/WRITE HEAD

Replace a failing read/write head circuit with a spare read/write head circuit as follows:

a. Express the track address of the failing read/write head circuit in three-digit octal notation. Example: Track address 221 (decimal) is track address 335 (octal).

Note

> An unused gate on any LT105 Spares Selector module may be used with the restriction that modules must be inserted in locations 22A, 23A, 24A, and 25A before modules can be inserted in locations 26A, 27A, 28A, or 29A. (See figure 7-4.)

b. Activate an unused gate on an LT105 Spares Selector module by removing the ground jumper from the gate input. (See figure 6-21.)

Note

> Each gate selects a spare read/write head circuit when activated. Therefore, do not provide identical inputs to two gates.

c. Connect jumpers from the octally coded track address signals to the inputs to the activated gate, as summarized in table 8-8. Example: To spare read/write head circuit 335 (octal), connect one gate input to signal X3 at pin 33, one gate input to signal YM3 at pin 24, and one gate input to signal YL5 at pin 18.

d. Solder the jumpers at both sides of the circuit board.

e. Record spared address and spare read/write head circuit used on the head wiring connection chart. (See figure 8-15.)

f. Insert the LT105 Spares Selector module in the selection unit.

8-41 SELECTION OF SPARE READ/WRITE HEADS

If a spare read/write head is needed, select it as indicated in the following example which substitutes a spare for track 221.

Note

> Decimal notation is used throughout this paragraph.

Table 8-8. Summary of Logical Sparing Signals

OCTAL DIGIT	X-VALUE		Y-VALUE			
	Most Significant Digit (100_8)		Middle Digit (10_8)		Least Significant Digit (1_8)	
	Signals	Pin	Signals	Pin	Signals	Pin
0	X0, X0B	29	YM0, YM0B	21	YL0, YL0B	12
1	X1, X1B	30	YM1, YM1B	22	YL1, YL1B	13
2	X2, X2B	31	YM2, YM2B	23	YL2, YL2B	14
3	X3, X3B	33	YM3, YM3B	24	YL3, YL3B	15
4	X4, X4B	34	YM4, YM4B	25	YL4, YL4B	17
5	X5, X5B	35	YM5, YM5B	26	YL5, YL5B	18
6	X6, X6B	36	YM6, YM6B	27	YL6, YL6B	19
7	X7, X7B	37	YM7, YM7B	28	YL7, YL7B	20

SPARE HEAD - S	HEAD CENTER TAP WIRING CHART	DISC FILE ASSY SERIAL NO.
FAULTY HEAD - 0		
USED SPARE - X		

	NO. 1								NO. 2								NO. 3								NO. 4								HEAD PLATE
HEAD NUMBER	0 & 4		1 & 5		2 & 6		3 & 7		0 & 4		1 & 5		2 & 6		3 & 7		0 & 4		1 & 5		2 & 6		3 & 7		0 & 4		1 & 5		2 & 6		3 & 7		SLOT NO.
1	9	S	27	S	9	S	27	S	9	S	27	S	9	S	27	S	9	S	27	S	9	S	27	S	9	S	27	S	9	S	27	S	
2	1		19		1		19		1		19		1		19		1		19		1		19		1		19		1		19		
3	10		28		10		28		10		28		10		28		10		28		10		28		10		28		10		28		
4	2		20		2		20		2		20		2		20		2		20		2		20		2		20		2		20		
5	11		29		11		29		11		29		11		29		11		29		11		29		11		29		11		29		
6	3		21		3		21		3		21		3		21		3		21		3		21		3		21		3		21		
7	12		30		12		30		12		30		12		30		12		30		12		30		12		30		12		30		
8	4		22		4		22		4		22		4		22		4		22		4		22		4		22		4		22		
9	13		31		13		31		13		31		13		31		13		31		13		31		13		31		13		31		CONNECTOR PIN NO.
10	14		32		14		32		14		32		14		32		14		32		14		32		14		32		14		32		
11	5		23		5		23		5		23		5		23		5		23		5		23		5		23		5		23		
12	15		33		15		33		15		33		15		33		15		33		15		33		15		33		15		33		
13	6		24		6		24		6		24		6		24		6		24		6		24		6		24		6		24		
14	16		34		16		34		16		34		16		34		16		34		16		34		16		34		16		34		
15	7		25		7		25		7		25		7		25		7		25		7		25		7		25		7		25		
16	17		35		17		35		17		35		17		35		17		35		17		35		17		35		17		35		
17	8		26		8		26		8		26		8		26		8		26		8		26		8		26		8		26		
18	18	S	36	S	18	S	36	S	18	S	36	S	18	S	36	S	18	S	36	S	18	S	36	S	18	S	36	S	18	S	36	S	
	J8 - 0A				J8 - 0B				J8 - 1A				J8 - 1B				J8 - 2A				J8 - 2B				J8 - 3A				J8 - 3B				CONNECTOR

NOTE: REFERENCE XDS DWG: 136588-1A

901565A. 814

Figure 8-15. Head Wiring Connection Chart

a. Find track 221 on the input/output and start/finish location chart (figure 6-13). Since track 221 is in the range (208-223), it has an X-value of 3 (NTR2 TR3 TR4) and is connected to the LT76 Read/Write Coupler module in location 17B through signals 2X03S and 2X03F (pins P8-1B-42 and P8-1B-43).

b. Find the X-values of 3 on the head location chart (figure 6-10, sheet 1 of 2). The read/write head for track 221 is on surface 2, slot 5, and is controlled by Y-select signal Y29.

c. Y-select signal Y29 is connected to the read/write head assembly at J8-1A-33.

d. A spare read/write head is available at J8-1A-36. (A read/write head is available at J8-1A-27, since this read/write head is connected to the same read/write coupler through P8-1B-42 and P8-1B-43.)

Note

Record any changes in wiring on the site documentation and on the head wiring connection chart of the EP RAD file (figure 8-15).

e. Disconnect the centertap wire from J8-1A-33 and connect it to the spare.

SECTION IX
ILLUSTRATED PARTS BREAKDOWN

9-1 GROUP ASSEMBLY PARTS LIST

The Group Assembly Parts List is a breakdown of all systems, assemblies, and subassemblies which can be disassembled, reassembled, or replaced and which are contained in the end article. The Group Assembly Parts List consists of columnar listings of parts related to illustrations. Parts are listed in order of disassembly sequence, except in cases where sequence of disassembly cannot be maintained. Attaching parts are listed below the related assembly or subassemblies. Items which are purchased in bulk form (for example, wire and insulating materials) are not listed.

Each parts list table is arranged in seven columns as follows:

a. The figure number of the part listed and the index number corresponding to the illustration reference

b. The XDS manufacturer's part number for the part

c. The vendor's part number for the part (if available)

d. A brief description of the part

e. The manufacturer's code for the part

f. The quantity of the part used per assembly

g. Usable on code column indicating that when a letter is used in the code column, the use of the coded part is restricted to the model identified by the code letter. (Where no letter symbol appears in this column, the part is used on all models of this configuration.)

How to use the Illustrated Parts Breakdown.

To obtain information about a part, the following steps should be taken:

a. Refer to the applicable assembly breakdown

b. Compare the part with the illustration until part is located.

c. Note the index number

d. Locate the index number in the corresponding Group Assembly Parts List

e. Find the part number and name of part opposite the Index number listed

9-2 NUMERICAL INDEX

This index is a listing of the items contained in the Group Assembly Parts List. The numerical order of the index (table 9-11) is determined by the XDS part number.

ILLUSTRATED PARTS BREAKDOWN CONTENTS

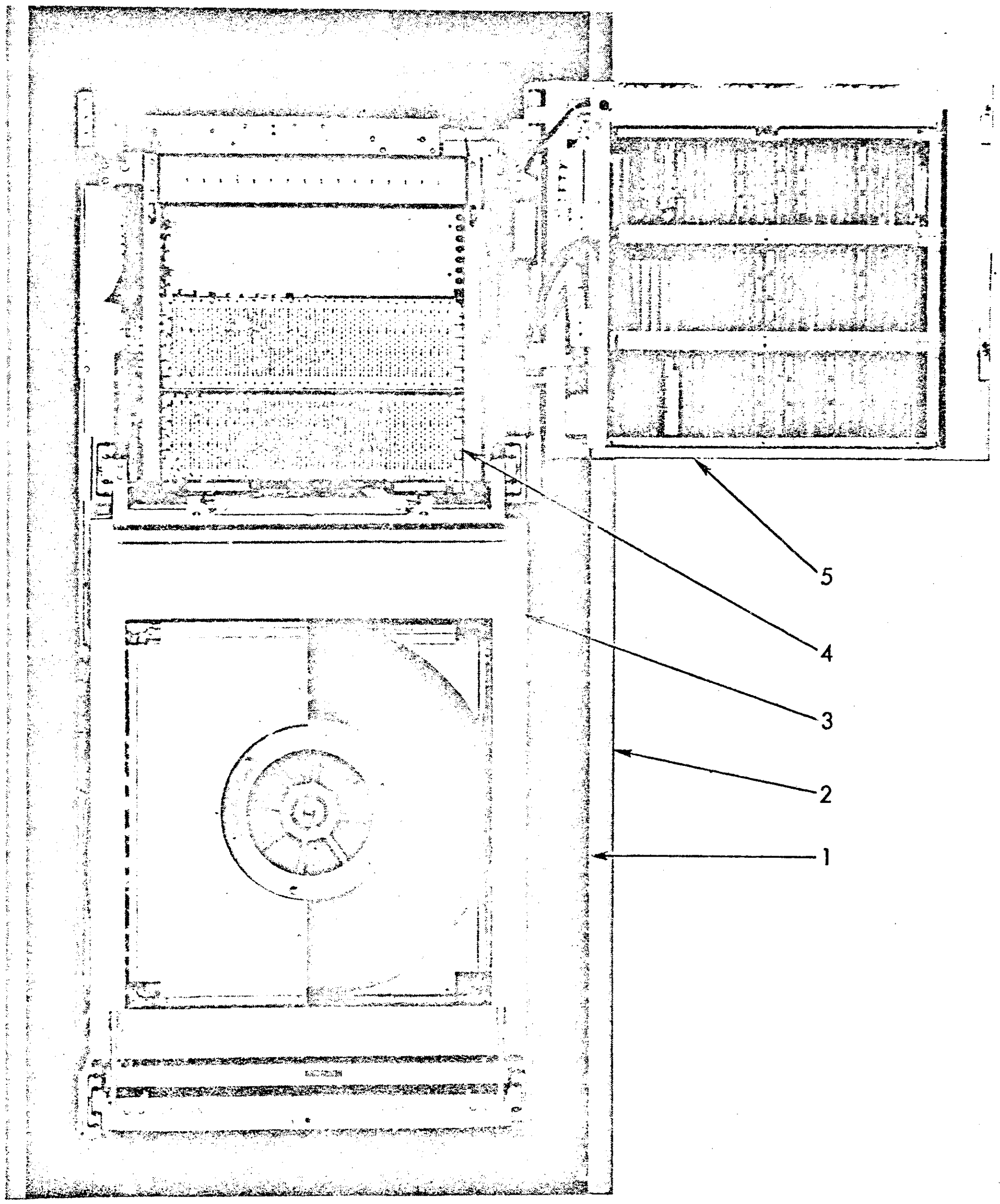


Figure 9-1. Extended Performance RAD Storage Unit and RAD Controller

Table 9-1. Extended Performance RAD Storage Unit

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-1-	139576 D		Extended Perf RAD Storage Unit (7232) (Fig 9-1)			
- 1	149763 C		. Storage Unit Cabinet Assy (Fig 9-2)		1	
	131419		. Cabinet Door Assy (Not shown)		2	
- 2	131410		. Cabinet Side Panel Assy		2	
- 3	139697 C		. Disc File Assy (Spindle and Drive) (Fig 9-5)		1	
- 4	139690 E		. Selection Unit Assy (Fig 9-3)		1	
- 5	149330 M		Extended Perf RAD Controller (7231) (Fig 9-9)		1	

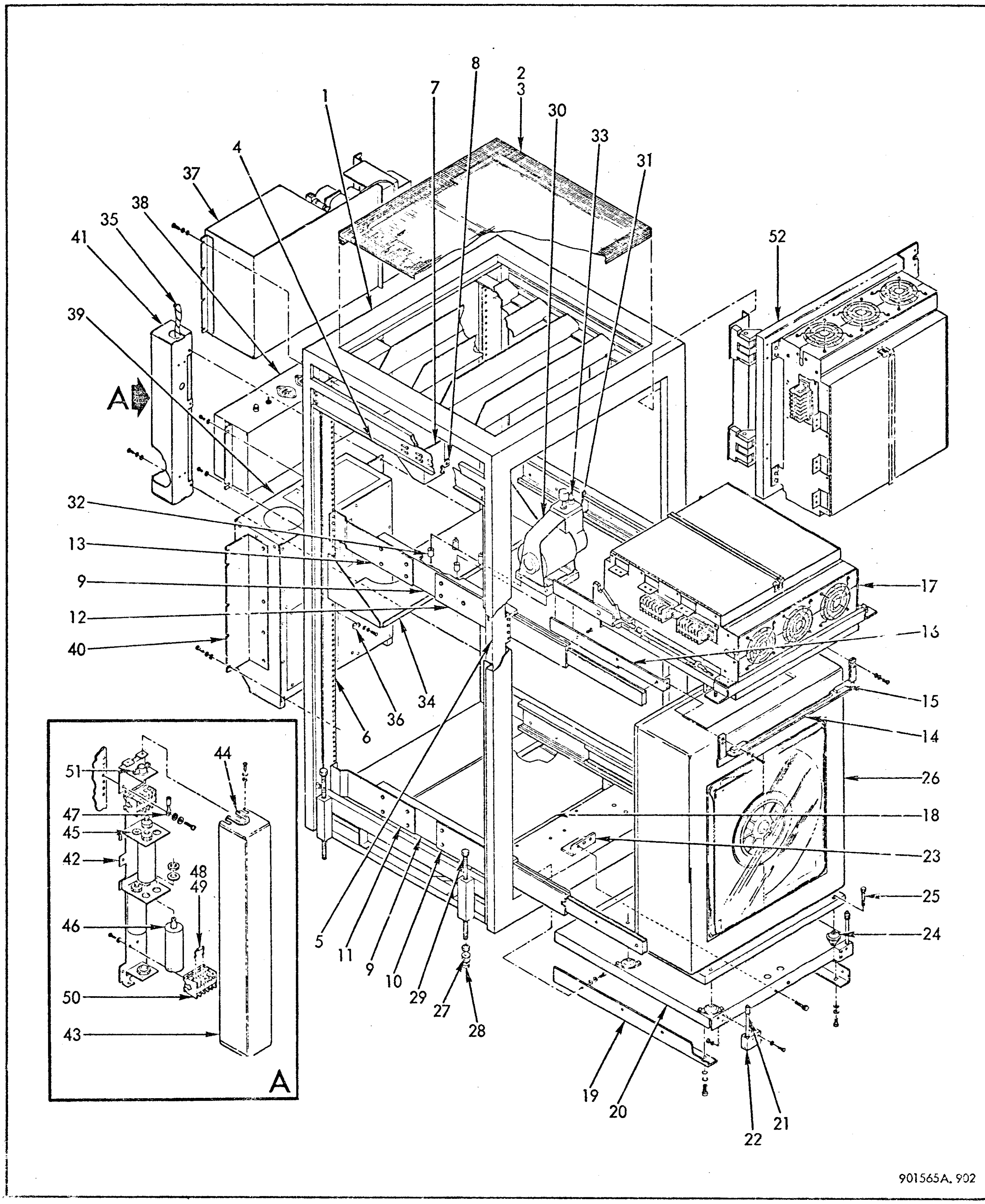


Figure 9-2. RAD Storage Unit Cabinet Assembly

Table 9-2. RAD Storage Unit Cabinet Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-	149763 C		. RAD Storage Unit Cabinet Assy		REF	
- 1	153320 A		. . Cabinet Basic Structure		1	
- 2	117424		. . Cap Cabinet Top		1	
- 3	139565-002		. . Clip, Speed U Type		2	
- 4	139814-001		. Bracket, Chassis Locking LH		1	
- 4	139814-002		. . Bracket, Chassis Locking RH		1	
			(Attaching Parts)			
-	101441-105		. . Screw, Cap Hex Hd		2	
-	101441-104		. . Screw, Cap Hex Hd		6	
-	100018-600		. . Washer, Flat		16	
-	100023-600		. . Washer, Lock Spring		8	
-	100008-600		. . Nut, Hex		8	
			- - - * - - -			
- 5	139994-001		. . Angle, Mtg LF (Retma)		1	
- 5	139994-002		. . Angle, Mtg RF (Retma)		1	
- 6	132019		. . Angle, Mtg Rear (Retma)		2	
			(Attaching Parts)			
-	101441-104		. . Screw, Cap Hex Hd		18	
-	100023-600		. . Washer, Lock Spring		18	
-	107311		. . Nut, Unistrut		18	
			- - - * - - -			
- 7	145412-001		. . Bracket, Latch Adjusting LH		1	
- 7	145412-002		. . Bracket, Latch Adjusting RH		1	

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-			(Attaching Parts)			
-	101441-104		. . Screw, Cap Hex Hd		8	
-	100018-600		. . Washer, Flat		8	
-	100023-600		. . Washer, Lock Spring		16	
-	100008-600		. . Nut, Hex		8	
			---*---			
- 8	111097		. . Bracket, Locking		2	
			(Attaching Parts)			
-	100012-610		. . Screw, Pan Head		4	
-	100018-600		. . Washer, Flat		8	
-	100023-600		. . Washer, Lock Spring		4	
-	100008-600		. . Nut, Hex		4	
			---*---			
- 9	129459		. . Slide, 20 inch (175 lb)		4	
-10	131354		. . Bracket Slide, Mtg Front		2	
-11	132088		. . Bracket Slide, Mtg Rear		2	
-12	139815-001		. . Bracket Slide, Sel Mtg RH Frt		1	
-12	139815-002		. . Bracket Slide, Sel Mtg LH Frt		1	
-13	139816-001		. . Bracket Slide, Sel Mtg RH Rear		1	
-13	139816-002		. . Bracket Slide, Sel Mtg LH Rear		1	
			(Attaching Parts)			
-	100039-510		. . Screw, Flat Head		28	
-	100018-500		. . Washer, Flat		28	
-	100024-500		. . Washer, Lock Int Tooth		28	
-	100008-500		. . Nut, Hex		28	
			---*---			

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-14	139858		. . Angle, Support Front		1	
			(Attaching Parts)			
-	100012-406		. . Screw, Pan Head		4	
-	100018-400		. . Washer, Flat		4	
-	100024-400		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-15	145698		. . Bumper, Rubber		4	
			(Attaching Parts)			
-	100018-307		. . Screw, Pan Head		8	
-	100018-300		. . Washer, Flat		8	
			- - - * - - -			
-16	147912-001		. . Bracket, Frame Mtg RH		1	
-16	147912-002		. . Bracket, Frame Mtg LH		1	
			(Attaching Parts)			
-	100039-609		. . Screw, Flat Head		6	
-	100012-505		. . Screw, Pan Head		6	
-	100024-500		. . Washer, Lock		6	
			- - - * - - -			
-17	139690		. . Selection Unit Assy (See Fig. 9-3)		REF	
-18	132646		. . Plate, Counter Balance		1	
-18	133155		. . Plate, Counter Balance		1	
			(Attaching Parts)			
-	101441-407		. . Screw, Cap Hex Head		6	
-	100018-600		. . Washer, Flat		6	
-	100023-600		. . Washer, Lock Spring		6	
			- - - * - - -			

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-19	145315-001		. . Angle, Spacer Slide RH		1	
-19	145315-002		. . Angle, Spacer Slide LH		1	
			(Attaching Parts)			
-	100039-609		. . Screw, Flat Head		8	
			- - - * - - -			
-20	131356		. . Plate, Drum Mounting		1	
			(Attaching Parts)			
-	100012-520		. . Screw, Pan Head		10	
-	100018-500		. . Washer, Flat		10	
-	100023-500		. . Washer, Lock Spring		10	
			- - - * - - -			
-21	132644		. . Leg Support Assy		2	
-22	131362		. . Bracket, Leg Support		2	
			(Attaching Parts)			
-	100012-500		. . Screw, Pan Head		6	
-	100018-500		. . Washer, Flat		12	
-	100024-500		. . Washer, Lock Int Tooth		6	
	100008-500		. . Nut, Hex Machine		6	
			- - - * - - -			
-23	131357		. . Bracket, Shipping		1	
			(Attaching Parts)			
-	101441-104		. . Screw, Cap Hex Head		2	
-	100018-600		. . Washer, Flat		2	
-	100023-600		. . Washer, Lock Spring		2	
	100008-600		. . Nut, Hex		2	
			- - - * - - -			

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-24	147931-006		. . Mount, Shock		4	
-25	129633-628		. . Screw, Cap Soc Hd		4	
			(Attaching Parts)			
-	100012-305		. . Screw, Pan Hd		8	
-	100018-300		. . Washer, Flat		8	
-	100024-300		. . Washer, Lock Int Tooth		8	
			--- * ---			
-26	139697		. . Disc File Assy (See Fig. 9-5)		REF	
-27	100008-410		. . Nut, Hex		8	
-28	100018-310		. . Washer, Flat		8	
-29	101918		. . Bolt		4	
-30	149960		. . Compressor Assy		1	
-31	111945		. . . Pump, Positive Pressure		1	
-32	117026-005		. . . Mount, Shear		4	
-33	132083-001		. . . Union, Tube Fitting		1	
-33	132570-001		. . . Terminal, Ins Ring Tongue		1	
			(Attaching Parts)			
-	100008-600		. . . Nut, Hex		4	
-	100018-600		. . . Washer, Flat		4	
-	100024-600		. . . Washer, Lock Int Tooth		4	
			--- * ---			
-34	146649		. . Bracket, Compressor Mounting		1	
			(Attaching Parts)			
-	100008-600		. . Nut, Hex		4	
-	100018-600		. . Washer, Flat		4	
-	100023-600		. . Washer, Lock Spring		4	
			--- * ---			

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-35	116701		. . Tubing, Pressure		A/R	
-35	101625-003		. . Tubing, Spirap		A/R	
-36	100657-003		. . Clamp, Nylon		2	
-36	100657-008		. . Clamp, Nylon		2	
			(Attaching Parts)			
-	100012-506		. . Screw, Pan Hd		2	
-	100018-500		. . Washer, Flat		2	
-	100024-500		. . Washer, Lock Int Tooth		2	
			- - - * - - -			
-37	146485		. . Motor Control Unit Assy (See Fig. 9-6)		1	
			(Attaching Parts)			
-	100012-506		. . Screw, Pan Hd		8	
-	100018-500		. . Washer, Flat		8	
-	100024-500		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
-38	137529		. . Power Distribution Panel Assy (See Fig. 9-8)		1	
			(Attaching Parts)			
-	100012-506		. . Screw, Pan Hd		6	
-	100018-500		. . Washer, Flat		6	
-	100024-500		. . Washer, Lock Int Tooth		6	
			- - - * - - -			
-39	136674		. . Power Supply Assy (PT20)		1	
-40	146488-001		. . Angle, Chassis Mounting RH		1	

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-40	146488-002		. . Angle, Chassis Mounting LH		1	
			(Attaching Parts)			
-	100012-504		. . Screw, Pan Hd		10	
-	100012-506		. . Screw, Pan Hd		10	
-	100018-500		. . Washer, Flat		10	
-	100024-500		. . Washer, Lock Int Tooth		10	
			- - - * - - -			
-41	139222		. . Power, Filter Assy		1	
			(Attaching Parts)			
-	100012-508		. . Screw, Pan Hd		3	
-	100018-500		. . Washer, Flat		3	
-	100024-500		. . Washer, Lock Int Tooth		3	
			- - - * - - -			
-42	139223		. . . Plate, Mounting		1	
-43	139224-002		. . . Cover, Filter		1	
			(Attaching Parts)			
-	100012-404		. . . Screw, Pan Hd		4	
-	100018-400		. . . Washer, Flat		4	
-	100024-400		. . . Washer, Lock Int Tooth		4	
			- - - * - - -			
-44	100840-001		. . . Grommet, Nylon		A/R	
-45	100840-003		. . . Grommet, Nylon		A/R	
-46	139175		. . . Filter, Power (C1 C2 C3 C4)		4	
-47	132570-004		. . . Terminal, Ring Tongue		9	
-48	110996-105		. . . Resistor Fixed Film 1W		4	
-49	100274-016		. . . Sleeve, Plastic		A/R	
-50	109432-001		. . . Block, Terminal Stack Type		10	

(Continued)

Table 9-2. RAD Storage Unit Cabinet Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-2-50	109432-005		. . . Clip, Retaining		4	
-50	109432-006		. . . Channel, Mounting		2	
-50	109432-008		. . . Plate, End		2	
-51	130191-002		. . . Clamp, Conduit		2	
			(Attaching Parts)			
-	100039-405		. . . Screw, Flat Hd		4	
-	100024-400		. . . Washer, Lock Int Tooth		4	
-	100008-400		. . . Nut, Hex		4	
			---*---			
-52	149330		. Extended RAD Controller (See Fig. 9-9)		REF	

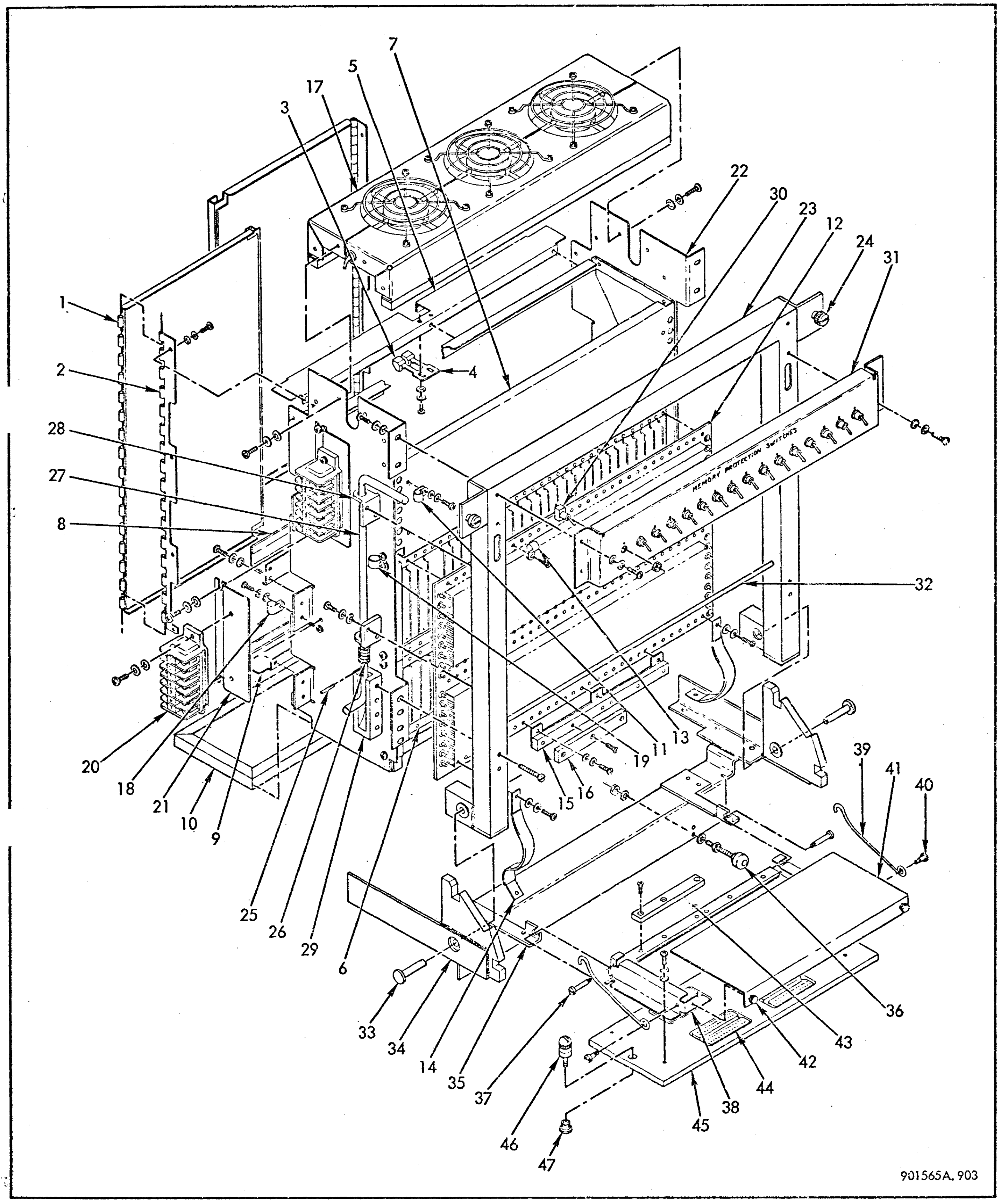


Figure 9-3. Selection Unit Assembly

Table 9-3. Selection Unit Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3-	139690		. Selection Unit Assy		REF	
- 1	131958		. . Door, Chassis		2	
- 2	131959		. . Hinge, Chassis Door		1	
- 2	131960		. . Hinge, Chassis Door		1	
			(Attaching Parts)			
-	100012-204		. . Screw, Pan Hd		8	
-	100018-200		. . Washer, Flat		8	
-	100024-200		. . Washer, Lock Int Tooth		8	
			- - - * - - -			
- 3	129554		. . Trigger, Door Latch		2	
			(Attaching Parts)			
-	100012-105		. . Screw, Pan Hd		2	
-	100024-100		. . Washer, Lock		2	
			- - - * - - -			
- 4	129540		. . Spring, Door Latch Mounting		1	
			(Attaching Parts)			
-	100012-304		. . Screw, Pan Hd		2	
-	100018-300		. . Washer, Flat		2	
-	100024-300		. . Washer, Lock Int Tooth		2	
			- - - * - - -			
- 5	130639		. . Bracket, Door Latch Mounting Support		1	
			(Attaching Parts)			
-	100012-203		. . Screw, Pan Hd		4	
-	100018-200		. . Washer, Flat		4	
-	100024-200		. . Washer, Lock Int Tooth		4	
			- - - * - - -			

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3-6	116231		. . Chassis, 32 Module (See Fig 9-4 for Mod Location)		2	
-6	129567-001		. . Nut, Strip Speed		4	
-7	129694		. . Panel, Blank		1	
			(Attaching Parts)			
-	100012-304		. . Screw, Pan Hd		19	
-	100018-400		. . Washer, Flat		19	
-	100024-400		. . Washer, Lock Int Tooth		19	
-	100008-400		. . Nut, Hex Mach		5	
			- - - * - - -			
- 8	116522		. . Channel, Cable Routing		1	
- 9	123940-001		. . Channel, Cable Routing		2	
			(Attaching Parts)			
-	100012-203		. . Screw, Pan Hd		12	
-	100018-200		. . Washer, Flat		12	
-	100024-200		. . Washer, Lock Int Tooth		12	
			- - - * - - -			
-10	117427		. . Filter, Air		1	
-11	100657-002		. . Clamp, Cable		2	
			(Attaching Parts)			
-	100012-407		. . Screw, Pan Hd		2	
-	100018-400		. . Washer, Flat		2	
-	100024-400		. . Washer, Lock Int Tooth		2	
-	100008-400		. . Nut, Hex Mach		2	
			- - - * - - -			
-12	139865		. . Backwiring Board Assy		1	
-13	100657-003		. . Clamp, Plastic		2	

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3-14	152673		. . Ground Strap Assy		2	
			(Attaching Parts)			
-	114538-214		. . Screw, Sheet Metal		36	
-	100008-300		. . Washer, Flat		36	
-	100024-300		. . Washer, Lock Int Tooth		36	
			---*---			
-15	139968		. . Strip Mounting, Wire Clamp		1	
			(Attaching Parts)			
-	100012-304		. . Screw, Pan Hd		3	
-	100018-300		. . Washer, Flat		3	
-	100024-300		. . Washer, Lock Int Tooth		3	
			---*---			
-16	139969		. . Block, Wire Clamping		2	
			(Attaching Parts)			
-	100039-310		. . Screw, Flat Hd		6	
			---*---			
-17	139637		. . Top Fan Assy		1	
			(Attaching Parts)			
-	100012-304		. . Screw, Pan Hd		8	
-	100018-300		. . Washer, Flat		8	
-	100024-300		. . Washer, Lock Int Tooth		8	
			---*---			
-18	100657-011		. . Clamp, Cable		2	

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3-19	100657-009		. . Clamp, Cable		2	
			(Attaching Parts)			
-	100012-407		. . Screw, Pan Hd		4	
-	100018-400		. . Washer, Flat		4	
-	100024-400		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-20	109432-001		. . Block, Terminal Stack Type		14	
-20	109432-011		. . End, Block		4	
-20	109432-008		. . End, Plate		2	
-20	109432-006		. . Channel, Mounting		2	
			(Attaching Parts)			
-	100012-310		. . Screw, Pan Hd		4	
-	100018-300		. . Washer, Flat		4	
-	100024-300		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-21	139967		. Bracket Mounting, Terminal Block (22-4 AWG)		2	
			(Attaching Parts)			
-	100012-405		. . Screw, Pan Hd		4	
-	100018-400		. . Washer, Flat		4	
-	100024-400		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-22	139634-001		. . Panel, Side Chassis RH		1	
-22	139634-002		. . Panel, Side Chassis LH		1	
-23	139635		. . Frame, Pivot Chassis Mounting		1	
			(Attaching Parts)			
-24	126340-010		. . Fastener, Captive		2	
			- - - * - - -			

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3-25	107199-308		. . Pin, Roll Corrosion		2	
-26	116722-003		. . Spring, Compression		2	
-27	145419-001		. . Rod, Latch		1	
-27	145419-002		. . Rod, Latch		1	
-28	145418		. . Guide, Rod		4	
			(Attaching Parts)			
-	100012-407		. . Screw, Pan Hd		8	
-	100018-400		. . Washer, Flat		8	
-	100024-400		. . Washer, Lock Int Tooth		8	
			--- * ---			
-29	145420-001		. . Block, Latch		1	
-29	145420-002		. . Block, Latch		1	
			(Attaching Parts)			
-	100039-520		. . Screw, Flat Hd		4	
-	100012-524		. . Screw, Pan Hd		4	
-	100018-500		. . Washer, Flat		4	
-	100024-500		. . Washer, Lock Int Tooth		4	
			--- * ---			
-30	107396		. . Switch, Toggle		16	
-31	145704		. . Panel, Switch Mounting		1	
			(Attaching Parts)			
-	100012-505		. . Screw, Pan Hd		8	
-	100018-500		. . Washer, Flat		8	
-	100024-500		. . Washer, Lock Int Tooth		8	
			--- * ---			
-32	147024		. . Rod Hanger, Interface Plate		1	
-33	139686		. . Pin, Hinge		2	

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3 -34	139636		. . Frame, Pivot Selection Unit Mtg		1	
-35	139892-002		. . Angle, Support		1	
-35	139892-001		. . Angle, Support			
			(Attaching Parts)			
-	100012-508		. . Screw, Pan Hd		4	
-	100018-500		. . Washer, Flat		4	
-	100024-500		. . Washer, Lock		4	
			- - - * - - -			
-36	109159-008		. . Bumper, Rubber		2	
			(Attaching Parts)			
-	100018-400		. . Washer, Flar		2	
-	100024-400		. . Washer, Lock Int Tooth		4	
-	100008-400		. . Nut, Hex Mach		6	
			- - - * - - -			
-37	113800-212		. . Screw, Shoulder Slotted		2	
-38	145515		. . Cover, Connector-Base Plate		1	
			(Attaching Parts)			
-	100012-205		. . Screw, Pan Hd		4	
-	100018-200		. . Washer, Flat		4	
-	100024-200		. . Washer, Lock Int Tooth		4	
			- - - * - - -			
-39	146673		. . Hanger		2	
-40	113800-204		. . Screw, Shoulder Slotted		2	
			- - - * - - -			
-41	145514		. . Cover, Connector		1	
-41	153709-001		. . Chart, Head Wiring		1	
-42	126340-002		. . Captive, Fastener		2	

(Continued)

Table 9-3. Selection Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-3 -43	139969		. . Block, Wire Clamping		2	
			(Attaching Parts)			
-	100039-307		. . Screw, Flat Hd		6	
			---*---			
-44	127489-002		. . Connector, 50 Pin		8	
			(Attaching Parts)			
-	100012-205		. . Screw, Pan Hd		16	
-	100024-200		. . Washer, Lock Int Tooth		16	
			---*---			
-45	127614		. . Plate Mtg, Connector Plug		1	
-46	152429-001		. . Screw, Captive		2	
-47	152429-002		. . Nut, Mtg		2	
			---*---			

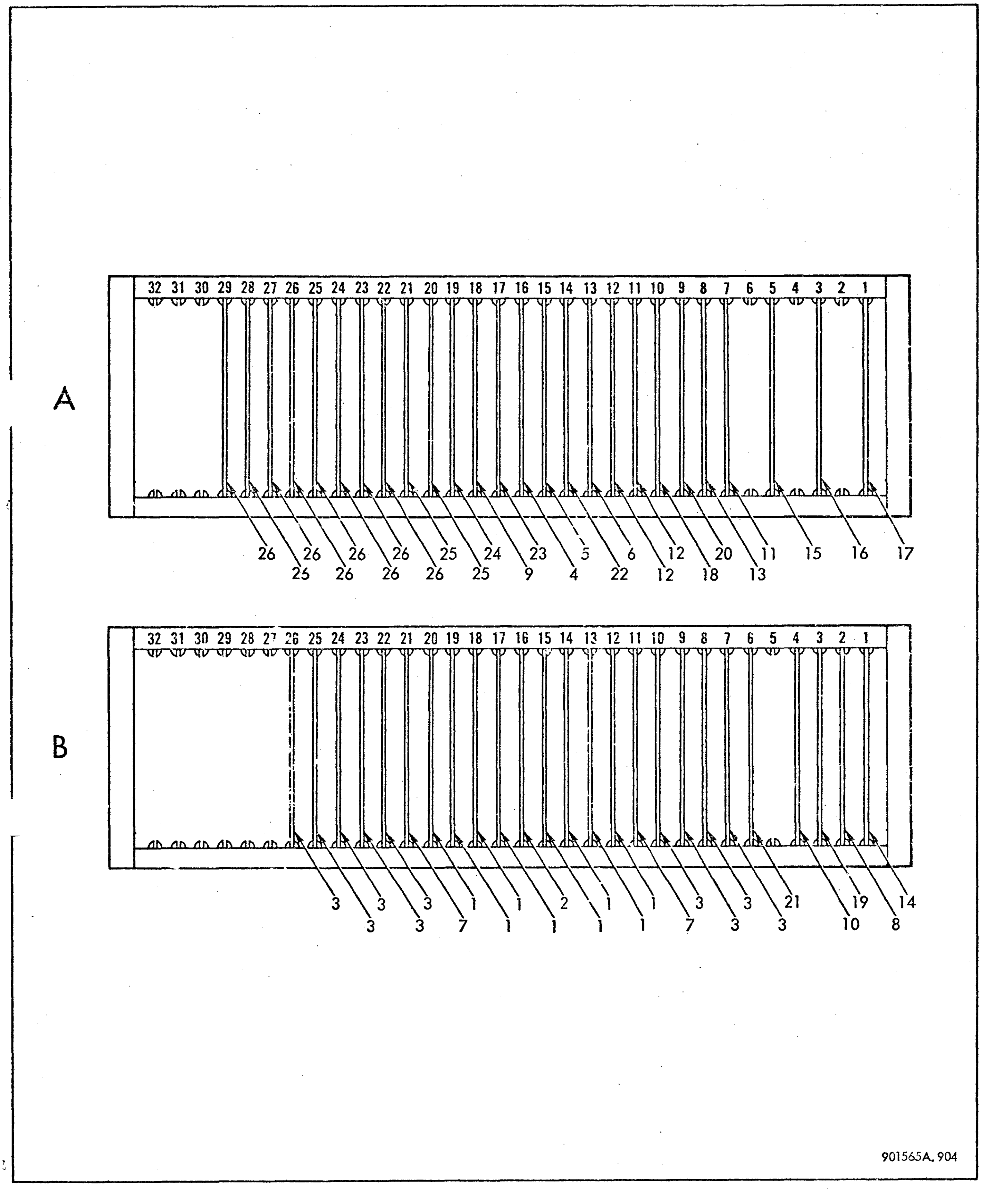


Figure 9-4. Module Location (Selection Unit Assembly)

Table 9-4. Module Locations (Selection Unit Assembly)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-4 -	149853 B		Module Kit Assy (Selection Unit Assy)		1	
-1	139418		. Module Assy, LT76 Read Write		8	
-2	139409		. Module Assy, HT42 Read AMP		1	
-3	139560		. Module Assy, RT18 Y Select		9	
-4	139714		. Module Assy, HT44 Limiter		1	
-5	147791		. Module Assy, AT51 Clock Discr		1	
-6	139716		. Module Assy, LT77 Data Decode		1	
-7	139792		. Module Assy, HT43 Write AMP		2	
-8	130747		. Module Assy, LT32 Sec Ind Dec		1	
-9	139570		. Module Assy, AT41 Write Clock		1	
-10	133500		. Module Assy, WT29 RAD Pwr Monitor		1	
-11	126982		. Module Assy, LT26 Switch Comp		1	
-12	117028		. Module Assy, FT12 Gated FF		2	
-13	116029		. Module Assy, BT11 BAND Gate		2	
-14	145221-001		. Module Assy, P35 Sector AMP		1	
-15	124629		. Module Assy, AT12 Cable Driver		1	
-16	123018		. Module Assy, AT10 Cable Rec		1	
-17	131572		. Module Assy, QT12 Lamp Dr Rec		1	
-18	116994		. Module Assy, IT11 Inverter Matrix		1	
-19	131572		. Module Assy, FT11 High Speed Ctr		1	
-20	116257		. Module Assy, XT10 Term Module		1	
-21	130689		. Module Assy, BT15 10 Sec 1st		1	
-22	147800		. Module Assy, LT85 Pul Puc Comp		1	
-23	145085		. Module Assy, BT31 BAND Gate		1	
-24	145095		. Module Assy, IT31 NAND Gate		1	
-25	115965		. Module Assy, BT12 Binary Decoder		2	
-26	164375		. Module Assy, LT105 Spare Selector		8	

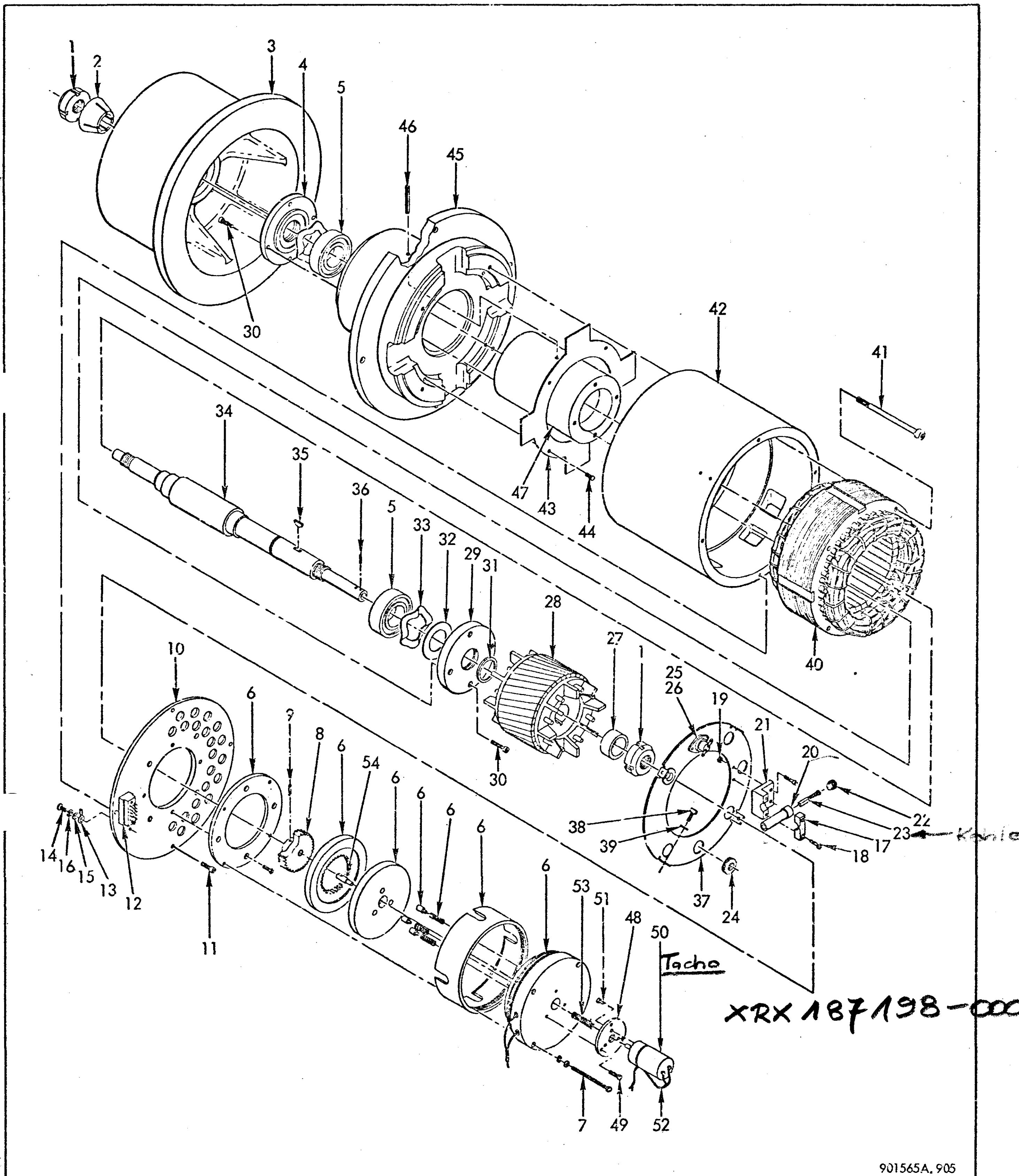


Figure 9-5. Spindle and Drive Assembly

Table 9-5. Spindle and Drive Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-5 -	139697 C		. Disc File Assy		REF	
9-5 -	148433 D		. . Bulk Hd Unit-(Disc File Assy)		1	
9-5 -	123455 R		. . . Spindle & Drive Assy		1	
-1	127387-001		. . . . Nut, Lock		2	
-2	127388		. . . . Washer, Hub Positioning		1	
-3	127389		. . . . Hub Assy		1	
-3	126716		. . . . . Disc, Hub		1	
-3	127054		. . . . . Insert, Hub		1	
-3	111468-502		. . . . . Insert, Thread		6	
-4	126623		. . . . Bearing, Retainer		1	
-5	123456		. . . . Bail, Bearing		2	
-6	147222-001		. . . . Brake, Magnetic		1	
			(Attaching Parts)			
-7	133079-406		. . . . Screw, Flat Hd		4	
			---*---			
-8	132086		. . . . Spline, Brake Drive		1	
-9	107199-413		. . . . Pin, Roll		1	
-10	131965		. . . . Cap, Motor Housing		1	
			(Attaching Parts)			
-11	113440-206		. . . . Screw, Cap Soc Hd		4	
			---*---			
-12	136561-001		. . . . Connector, Male 14 Pin (J37)		1	
-13	132570-002		. . . . Terminal, Ins Ring Tongue		1	
			(Attaching Parts)			
-14	100012-404		. . . . Screen, Pan Hd		1	
-15	100018-400		. . . . Washer, Flat		1	
-16	113221-400		. . . . Washer, Lock		1	
			---*---			

(Continued)

Table 9-5. Spindle and Drive Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-5 -17	149581		. . . . Clamp, Cartridge		1	
			(Attaching Parts)			
-18	129633-206		. . . . Screw, Cap Soc Hd		4	
-19	100008-200		. . . . Nut, Hex Mach		2	
			--- * ---			
-20	149479-001		. . . . Cartridge, Brush Holder		1	
-21	149580		. . . . Bracket, Cartridge		1	
-22	152008		. . . . Plug, Screw		1	
-23	149578-001	6[illegible]850.000	. . . . Brush, Metal Graphite		1	
-24	100720-006		. . . . Grommet, Rubber		2	
-25	128155-001		. . . . Thermostat, Overtemp		1	
			(Attaching Parts)			
-26	100012-104		. . . . Screw, Pan Hd		2	
-26	100018-100		. . . . Washer, Flat		2	
-26	100024-100		. . . . Washer, Lock		2	
-26	100008-100		. . . . Nut, Hex Mach		2	
			--- * ---			
-27	130777-001		. . . . Spacer, Rotor		1	
-28	131977-005		. . . . Motor, Rotor		1	
-29	131186		. . . . Cap, Load Spring Retaining		1	
			(Attaching Parts)			
-30	129633-508		. . . . Screw, Cap Soc Hd		4	
-30	129633-506		. . . . Screw, Cap Soc Hd		4	
			--- * ---			
-31	123460-021		. . . . "O" Ring, Teflon		2	
-32	127346-001		. . . . Shim, Retaining Bearing		A/R	
-32	127346-002		. . . . Shim, Retaining Bearing		A/R	

(Continued)

Table 9-5. Spindle and Drive Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-5 -32	127346-003		. . . . Shim, Retaining Bearing		A/R	
-33	128163-002		. . . . Washer, Spring		2	
-34	123458		. . . . Shaft, Spindle		1	
-35	126835-003		. . . . Woodruff, Key		1	
-36	107199-108		. . . . Roll, Pin		1	
-37	131964		. . . . Baffle, Motor Housing		1	
			(Attaching Parts)			
-38	129633-204		. . . . Screw, Cap Soc Hd		4	
-39	100018-200		. . . . Washer, Flat		4	
			- - - * - - -			
-40	131997-004		. . . . Motor, Elec Three Phase (Stator)		1	
			(Attaching Parts)			
-41	132103-001		. . . . Screw, Motor Housing Mtg		4	
			- - - * - - -			
-42	131963		. . . . Housing, Motor		1	
-43	129687		. . . . Baffle, Air Spindle & Drive		1	
			(Attaching Parts)			
-44	131530-103		. . . . Screw, Drive		4	
			- - - * - - -			
-45	127056		. . . . Spindle Housing Assy		1	
-46	107199-614		. . . . Pin, Roll Cres (3/16 Dia x 7/8 Lg)		3	
-47	126624		. . . . Liner, Spindle Housing		1	
-48	133080		. . . . Plate, Adaptor Tachometer		1	
			(Attaching Parts)			
-49	113440-206		. . . . Screw, Cap Soc Hd		3	
			- - - * - - -			

(Continued)

Table 9-5. Spindle and Drive Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-5 -50	132593 XRX 18718-0000		. . . . Generator, Tachometer		1	
			(Attaching Parts)			
-51	123054-104		. . . . Screw, Button Hd		3	
			---*---			
-52	133559-026		. . . . Wire, Twisted Pair		A/R	
-52	102066-001		. . . . Cord, Lacing		A/R	
-53	149272		. . . . Coupling, Shaft		1	
-54	132743		. . . . Shaft, Coupling-Tachometer		1	
			---*---			

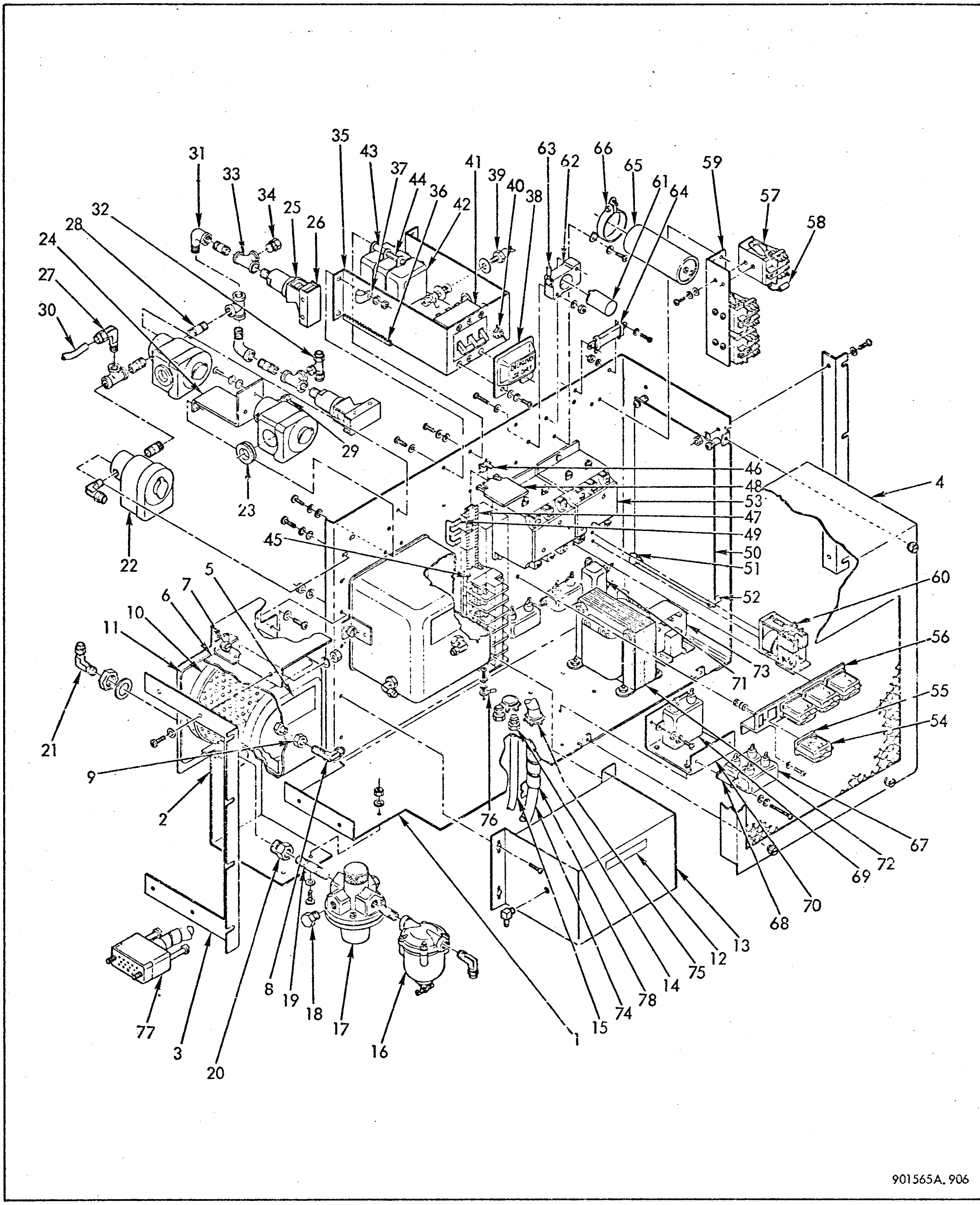


Figure 9-6. Motor Control Unit Assembly

Table 9-6. Motor Control Unit Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -	146485 J		. . Motor Control Unit Assy		REF	
-1	132175		. . . Chassis Motor Control Unit		1	
			(Attaching Parts)			
-	113526-006		. . . Nut, Self Clinching		10	
-	113526-012		. . . Nut, Self Clinching		5	
			- - - * - - -			
-2	146484		. . . Chassis, Filter Mtg Control Unit		1	
			(Attaching Parts)			
-	113526-012		. . . Nut, Self Clinching		2	
-	100012-508		. . . Screw, Pan Hd		5	
-	100018-500		. . . Washer, Flat		5	
-	113221-500		. . . Washer, Lock Spring		5	
-	100008-500		. . . Nut, Hex Mach		5	
			- - - * - - -			
-3	146487		. . . Angle, Mtg RH		1	
-3	146486		. . . Angle, Mtg LH		1	
			(Attaching Parts)			
-	100012-508		. . . Screw, Pan Hd		6	
-	100018-500		. . . Washer, Flat		6	
-	113221-500		. . . Washer, Lock Spring		6	
-	100008-500		. . . Nut, Hex Mach		6	
			- - - * - - -			
-4	132176		. . . Cover, Chassis (Motor Control Unit)		1	
-4	126340-012		. . . Fastener, Captive		4	
			- - - * - - -			
-5	147044-001		. . . Label, Filter		2	
-6	129731		. . . Filter, Container Assy		2	

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -6	127990		. . . . . Container, Filter-Charcoal		2	
-7	126440-012		. . . . . Fastener, Captive		4	
-8	116702-002		. . . . . Connector, Elbow		4	
-9	134844-001		. . . . . Nut, Lock		8	
-10	132514		. . . . Filter, Air Charcoal		2	
-11	132744		. . . . Gasket, Filter Mtg		2	
-12	147044-002		. . . . Label, Filter		1	
-13	158947		. . . . Absolute Filter Unit Assy		1	
			(Attaching Parts)			
-	100012-306		. . . . Screw, Pan Head		4	
			---*---			
-14	132084		. . . . Union, Bulkhead		2	
-15	116701		. . . . Tubing, Pressure		72	
-16	117226		. . . . Filter, Air		1	
-17	134993		. . . . Regulator, Pressure		1	
-18	133033-001		. . . . Plug, Pipe Hex Hd		1	
-19	132749-001		. . . . Nipple, Pipe Fitting		2	
-20	145646		. . . . Fitting, Adapter Bulkhead		1	
-21	116702-001		. . . . Connector, Elbow		2	
-22	132534		. . . . Valve, Solenoid (K12, K13, K14)		3	
			(Attaching Parts)			
-	100012-508		. . . . Screw, Pan Hd		6	
-	100018-500		. . . . Washer, Flat		6	
-	113221-500		. . . . Washer, Lock Spring			
			---*---			
-23	100720-009		. . . . Grommet, Rubber		3	

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -24	132359		. . . Bracket, Solenoid Mtg		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		2	
-	100018-300		. . . Washer, Flat		2	
-	113221-300		. . . Washer, Lock Spring		2	
			--- * ---			
-25	113707-002		. . . Switch, Pressure (S2, S3)		2	
-26	134843		. . . Cover, Protective		2	
-27	116702-002		. . . Connector, Elbow		2	
-28	132749-005		. . . Nipple-Pipe Fitting		5	
-29	132083-002		. . . Union, Tube Fitting (Male)		1	
-30	116701		. . . Tubing, Pressure		A/R	
-31	132532-002		. . . Elbow, Street		2	
-32	132528		. . . Tee, Tube Fitting		1	
-33	132529-001		. . . Tee, Female Pipe Fitting		4	
-34	133033-002		. . . Plug, Pipe Hex Hd		1	
-35	132178		. . . Bracket, Component Mtg		1	
-36	100840-002		. . . Grommet, Nylon		2	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		3	
-	100018-400		. . . Washer, Flat		3	
-	113221-400		. . . Washer, Lock Spring		3	
			--- * ---			
-37	100657-004		. . . Clamp, Cable Nylon		1	
			(Attaching Parts)			
-	100012-410		. . . Screw, Pan Hd		1	
-	100018-400		. . . Washer, Flat		1	
-	113221-400		. . . Washer, Lock Spring		1	
-	100008-400		. . . Nut, Hex Mach		1	
			--- * ---			

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -38	149710		. . . Cover, Protective		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		2	
-	100018-300		. . . Washer, Flat		2	
-	113221-300		. . . Washer, Lock Spring		2	
			- - - * - - -			
-39	132495		. . . Thyristor, (XDS 236) (SCR1, R2, R3)		3	
			(Attaching Parts)			
-	132570-005		. . . Terminal, Ins Ring Tongue		3	
-	113220-600		. . . Washer, Flat		3	
			- - - * - - -			
-40	113694		. . . Switch, Subminiature DPDT Toggle SI		1	
-41	133034-001		. . . Circuit, Breaker CB1		1	
			(Attaching Parts)			
-	100039-304		. . . Screw, Flat Head 100°		4	
			- - - * - - -			
-42	100992-003		. . . Capacitor, DV Oil/Paper (C30, 31, 32)		3	
-43	107132-003		. . . Spacer, Round		2	
-44	107018-314		. . . Standoff, Hex		2	
			(Attaching Parts)			
-	100012-320		. . . Screw, Pan Hd		2	
-	100012-307		. . . Screw, Pan Hd Recessed		2	
-	100018-300		. . . Washer, Flat		4	
-	100024-300		. . . Washer, Lock		4	
			- - - * - - -			
-45	109432-001		. . . Block, Terminal 18-8 AWS		20	
-46	109432-005		. . . Clip, Retaining		1	

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -47	109432-006		. . . Mounting, Channel		1	
-48	109432-008		. . . Plate, End		1	
-49	109432-012		. . . Jumper		2	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		4	
-	100018-400		. . . Washer, Flat		4	
-	113221-400		. . . Washer, Lock Spring		4	
-	100008-400		. . . Nut, Hex Mach		4	
			---*---			
-50	132343		. . . PW Assy, (TB1) (See Fig. 9-7)		1	
-51	100657-005		. . . Clamp, Cable Nylon		1	
-52	107018-308		. . . Standoff, Threaded		4	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		4	
-	100018-300		. . . Washer, Flat		4	
-	113221-300		. . . Washer, Lock Spring		4	
			---*---			
-53	130422-001		. . . Contactor, 3 Pole (K5, K6)		2	
			(Attaching Parts)			
-	100012-307		. . . Screw, Pan Hd Recessed		6	
-	100018-300		. . . Washer, Flat		6	
-	100024-300		. . . Washer, Lock		6	
-	100008-300		. . . Nut, Hex Mach		6	
			---*---			
-54	106994		. . . Relay, DC (K3, K4, K7, K8)		4	

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -55	106843		. . . Socket, Relay		4	
			(Attaching Parts)			
-	100012-207		. . . Screw, Pan Hd		4	
-	100018-200		. . . Washer, Flat		4	
-	113221-200		. . . Washer, Lock Spring		4	
-	100008-200		. . . Nut, Hex Mach		4	
			- - - * - - -			
-56	146260		. . . Bracket, Relay Mtg		1	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		2	
-	100018-400		. . . Washer, Flat		2	
-	113221-400		. . . Washer, Lock Spring		2	
-	100008-400		. . . Nut, Hex Mach		2	
			- - - * - - -			
-57	130132		. . . Relay, DPDT 10A (K1, K2, K9)		3	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		9	
-	100018-300		. . . Washer, Flat		9	
-	113221-300		. . . Washer, Lock Spring		9	
			- - - * - - -			
-58	110996-471		. . . Resistor, Film 1W (R56)		1	
-59	132179		. . . Bracket, Relay Mtg		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		4	
-	100018-300		. . . Washer, Flat		4	
-	113221-300		. . . Washer, Lock Spring		4	
			- - - * - - -			

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -60	130765		. . . Relay, 4 Form C 24VDC (K10)		1	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		1	
-	100018-400		. . . Washer, Flat		1	
-	113221-400		. . . Washer, Lock Spring		1	
			---*---			
-61	129681		. . . Relay, Time Delay (K15)		1	
-62	129682		. . . Socket, Time Delay		1	
-63	132570-001		. . . Terminal, Ins Ring Tongue		2	
			(Attaching Parts)			
-	100012-314		. . . Screw, Pan Hd Recessed		2	
-	100018-300		. . . Washer, Flat		2	
-	100024-300		. . . Washer, Lock		2	
-	100008-300		. . . Nut, Hex Mach		2	
			---*---			
-64	101155-150		. . . Resistor, Fixed WW (R1)		1	
			(Attaching Parts)			
-	100012-210		. . . Screw, Pan Hd		2	
-	100018-200		. . . Washer, Flat		2	
-	113221-200		. . . Washer, Lock Spring		2	
-	100008-200		. . . Nut, Hex Mach		2	
			---*---			
-65	108474		. . . Capacitor, JN Electrolytic (C1)		1	

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -66	126945-002		. . . Bracket, Capacitor Mtg		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		3	
-	100018-300		. . . Washer, Flat		4	
-	113221-300		. . . Washer, Lock Spring		2	
-	100008-300		. . . Nut, Hex Mach		3	
			- - - * - - -			
-67	100992-003		. . . Capacitor, DV Oil/Paper (C3, C4)		2	
-68	107132-005		. . . Spacer, Round LH		2	
-68	107132-006		. . . Spacer, Round RH		2	
			(Attaching Parts)			
-	100012-320		. . . Screw, Pan Hd		2	
-	113220-300		. . . Washer, Flat		2	
-	113221-300		. . . Washer, Lock Spring		2	
			- - - * - - -			
-69	100992-006		. . . Capacitor, DV Oil/Paper (C5)		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		2	
-	113220-300		. . . Washer, Flat		2	
-	113221-300		. . . Washer, Lock Spring		2	
			- - - * - - -			
-70	132177		. . . Bracket, Capacitor Mtg		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		4	
-	100018-300		. . . Washer, Flat		4	
-	113221-300		. . . Washer, Lock Spring		4	
			- - - * - - -			

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -71	100992-003		. . . Capacitor, DV Oil/Paper (C6, 7, 8)		3	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		6	
-	113220-300		. . . Washer, Flat		6	
-	113221-300		. . . Washer, Lock Spring		6	
			- - - * - - -			
-72	132369		. . . Transformer (T1)		1	
			(Attaching Parts)			
-	100012-508		. . . Screw, Pan Hd		4	
-	100018-500		. . . Washer, Flat		4	
-	113221-500		. . . Washer, Lock Spring		4	
-	100008-500		. . . Nut, Hex Mach		4	
			- - - * - - -			
-73	132492		. . . Transformer (T2)		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		4	
-	100018-300		. . . Washer, Flat		4	
-	113221-300		. . . Washer, Lock Spring		4	
			- - - * - - -			
-74	136179		. . . Cable, 4 Conductor (Grn Wire)		A/R	
-75	130191-001		. . . Connector, Cable Grip		2	
-76	132570-001		. . . Terminal, Ins Ring Tongue		1	
			(Attaching Parts)			
-	100012-306		. . . Screw, Pan Hd		1	
-	100018-300		. . . Washer, Flat		1	
-	113221-300		. . . Washer, Lock Spring		1	
-	100008-300		. . . Nut, Hex Mach		1	
			- - - * - - -			

(Continued)

Table 9-6. Motor Control Unit Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-6 -77	136560-002		. . . Connector, 14 Contact-Female		1	
-78	101625-003		. . . Tubing, Spiral		A/R	
			---*---			

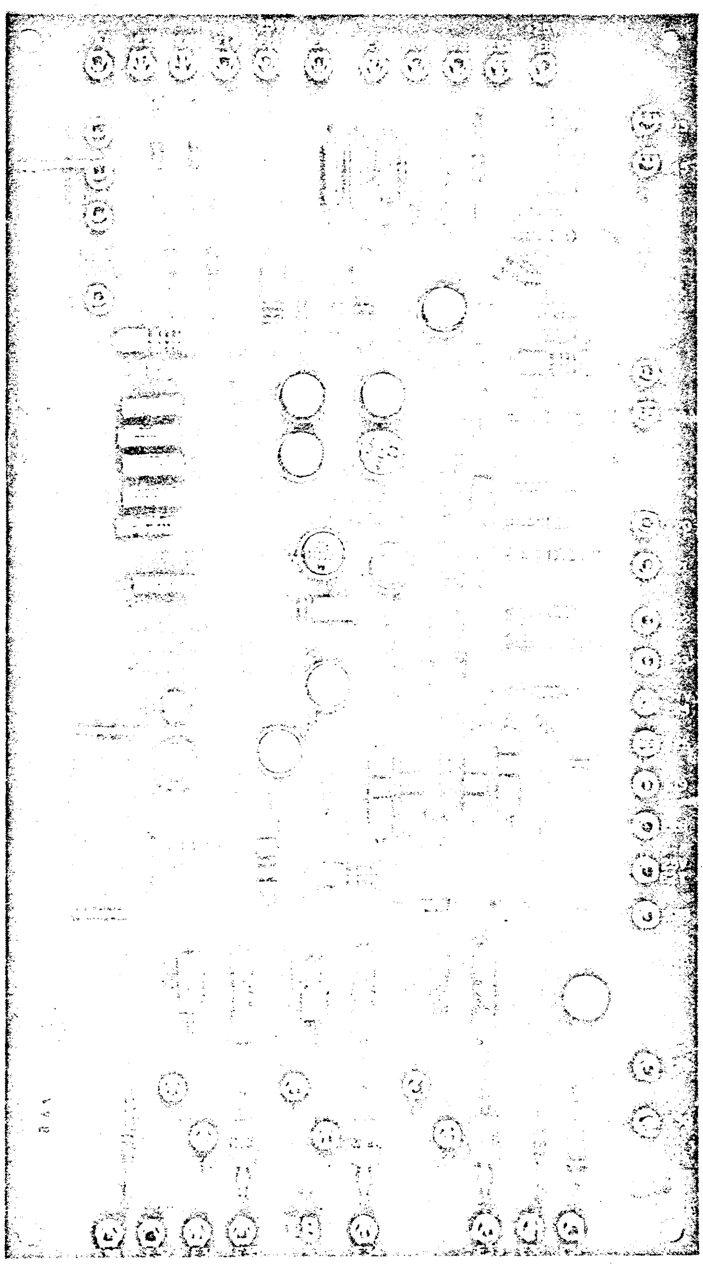


Figure 9-7. Printed Wiring Board (TB1)

Table 9-7. Printed Wiring Board TB1

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-7 -	132343		. . . PW Motor Control Unit (TB1)		1	
-	132344		. . . . Board, PW		1	
-	111530		. . . . . Transistor XDS 231, (Q1,5)		2	
-	100698		. . . . . Transistor XDS 210, (Q2,3,6,7, 8,10,11)		7	
-	102055		. . . . . Transistor XDS 214, (Q4)		1	
-	103242		. . . . . Transistor XDS 216, (Q9)		1	
-	124298		. . . . . Pad, Transistor (Q1 thru 8, 10, 11)		10	
-	100323		. . . . . Diode XDS 106 (VR1,2,5 thru 9)		7	
-	100025		. . . . . Diode XDS 101, (VR3,4)		2	
-	111516		. . . . . Diode XDS 123, (CR14)		1	
-	132494		. . . . . Diode XDS 135, (CR23,24,25)		3	
-	101154		. . . . . Diode XDS 113, (CR1 thru 13, 16, 17)(CR19 thru 22,26,27)		21	
-	123300-475		. . . . . Capacitor, Tantalum (C9 thru 12) (C14 thru 20, C24 thru 27)		15	
-	123300-126		. . . . . Capacitor, Tantalum (C13,22,23)		3	
-	110996-103		. . . . . Resistor, 1W (R2)		1	
-	110996-152		. . . . . Resistor, 1W (R3)		1	
-	110996-202		. . . . . Resistor, 1W (R25,45,50)		3	
-	110996-100		. . . . . Resistor, 1W (R18,30,38)		3	
-	110996-105		. . . . . Resistor, 1W (R20 thru 24)		5	
-	110996-622		. . . . . Resistor, 1W (R32)		1	
-	110996-473		. . . . . Resistor, 1W (R33)		1	
-	110996-273		. . . . . Resistor, 1W (R46 thru 49)		4	
-	130109-097		. . . . . Resistor, 1W (R39,41,43)		3	
-	110996-183		. . . . . Resistor, 1W (R31)		1	
-	123363-164		. . . . . Resistor, 1/8W (R37)		1	

(Continued)

Table 9-7. Printed Wiring Board TB1 (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-7 -	123362-243		. . . . . . Resistor, 1/8W (R4, 5, 9, 13, 35, 51, 10)		7	
-	123362-084		. . . . . . Resistor, 1/8W (R6, 8)		2	
-	123362-281		. . . . . . Resistor, 1/8W (R7)		1	
-	123362-147		. . . . . . Resistor, 1/8W (R28, 40, 42, 44, 53, 54)		6	
-	123362-197		. . . . . . Resistor, 1/8W (R12)		1	
-	123362-219		. . . . . . Resistor, 1/8W (R14)		1	
-	123362-176		. . . . . . Resistor, 1/8W (R17, 34, 11, 15, 29, 52)		6	
-	123362-212		. . . . . . Resistor, 1/8W (R26, 36)		2	
-	123362-339		. . . . . . Resistor, 1/8W (R19, 27)		2	
-	123362-172		. . . . . . Resistor, 1/8W (R16)		1	
-	110996-101		. . . . . . Resistor, 1W (R55)		1	
-	123300-124		. . . . . . Capacitor, Tantalum (C29)		1	
-	126297-001		. . . . . . Terminal, Bif Rivet (E1 thru 45)		45	
			- - - * - - -			

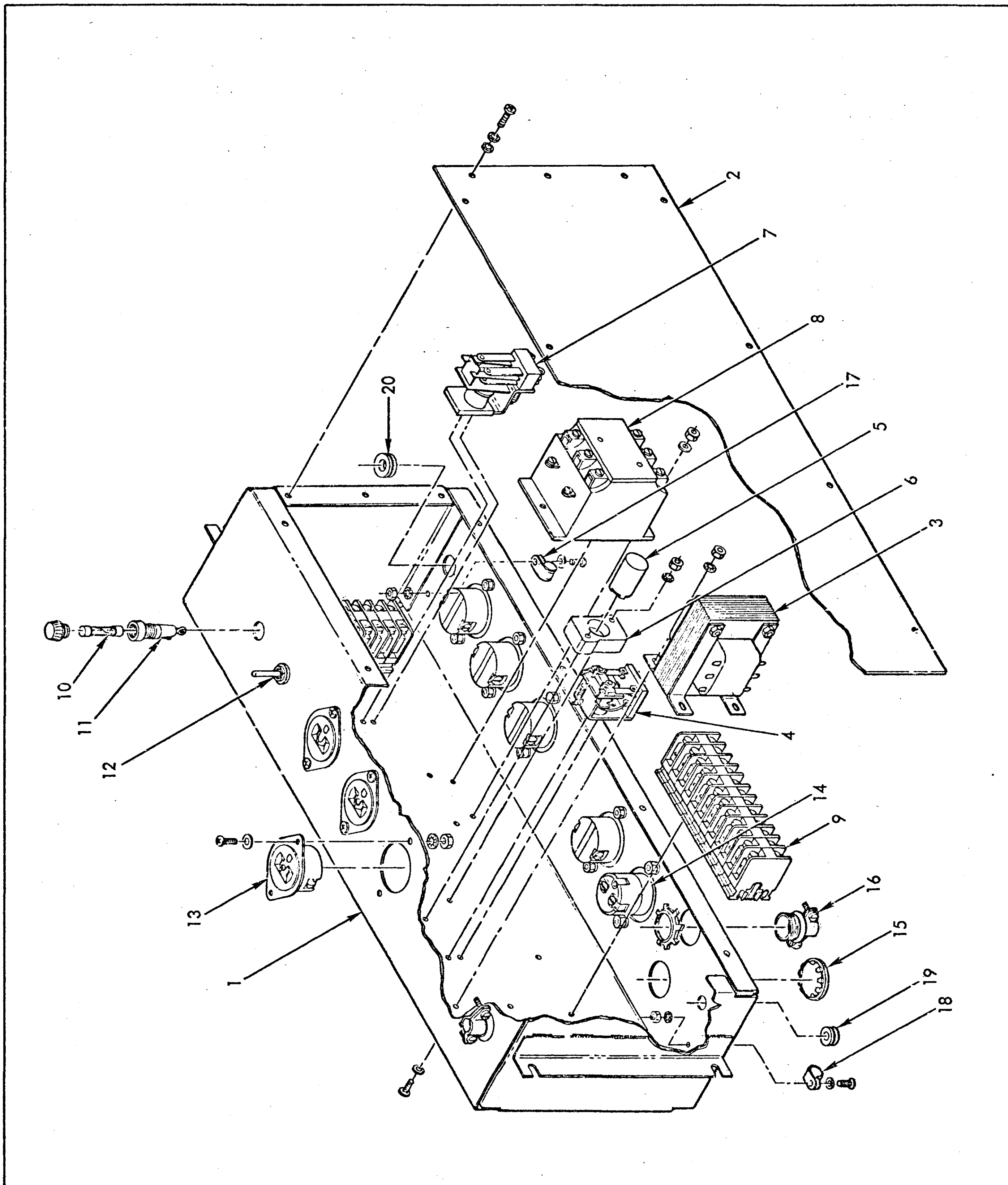


Figure 9-8. Power Distribution Panel Assembly

Table 9-8. Power Distribution Panel Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-8 -	137529 E		. . Power Distribution Panel Assy		REF	
-1	137530		. . . Chassis Distribution Panel		1	
-2	131326		. . . Cover, Distribution Panel		1	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		14	
-	100018-400		. . . Washer, Flat		14	
-	100024-400		. . . Washer, Lock		14	
			- - - * - - -			
-3	127055		. . . Transformer (T1)		1	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		4	
-	100018-400		. . . Washer, Flat		4	
-	100024-400		. . . Washer, Lock Int Tooth		4	
-	100008-400		. . . Nut, Hex Mach		4	
			- - - * - - -			
-4	130132		. . . Relay, DPDT 10A (K4)		1	
-4	110996-331		. . . Resistor, 330 1W (R1)		1	
			(Attaching Parts)			
-	100012-307		. . . Screw, Pan Hd		1	
-	100018-300		. . . Washer, Flat		1	
-	100024-300		. . . Washer, Lock Int Tooth		1	
			- - - * - - -			
-5	129681		. . . Relay, Time Delay Thermal (K5)		1	

(Continued)

Table 9-8. Power Distribution Panel Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-8 -5	129682		. . . Socket, Relay		1	
			(Attaching Parts)			
-	100012-316		. . . Screw, Pan Hd		2	
-	100018-300		. . . Washer, Flat		2	
-	100024-300		. . . Washer, Lock Int Tooth		2	
-	100008-300		. . . Nut, Hex Mach		2	
			- - - * - - -			
-6	130540		. . . Relay, DPDT 5A 24VDC Coil (K3)		1	
-6	101154		. . . Diode, XDS 113 (CR1)		1	
			(Attaching Parts)			
-	100012-406		. . . Screw, Pan Hd		1	
-	100018-400		. . . Washer, Flat		1	
-	100024-400		. . . Washer, Lock Int Tooth		1	
			- - - * - - -			
-7	130422-001		. . . Contactor, 3 Pole AC (K1)		1	
			(Attaching Parts)			
-	100012-414		. . . Screw, Pan Hd		3	
-	100018-400		. . . Washer, Flat		3	
-	100024-400		. . . Washer, Lock Int Tooth		3	
-	100008-400		. . . Nut, Hex Mach		3	
			- - - * - - -			
-8	109432-001		. . . Block (TB1, TB2)		22	
-8	109432-005		. . . Clip, Retaining		4	
-8	109432-006		. . . Mounting, Channel		2	
-8	109432-008		. . . Plate, End		2	

(Continued)

Table 9-8. Power Distribution Panel Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-8 -8	109432-012		. . . Jumper, Terminal		4	
			(Attaching Parts)			
-	100012-407		. . . Screw, Pan Hd		4	
-	100018-400		. . . Washer, Flat		4	
-	100024-400		. . . Washer, Lock Int Tooth		4	
-	100008-400		. . . Nut, Hex Mach		4	
-9	100653-006		. . . Fuse, .250 AMP 3AG (F1)		1	
-10	100331		. . . Holder, Fuse		1	
-11	130462		. . . Switch, Toggle DPDT (S1)		1	
-12	101430		. . . Receptacle, Female 3 Contact (J2 thru J8)		7	
-13	127675		. . . Receptacle, Male 3 Contact (J1)		1	
			(Attaching Parts)			
-	100012-307		. . . Screw, Pan Hd		16	
-	100018-300		. . . Washer, Flat		16	
-	100024-300		. . . Washer, Lock Int Tooth		16	
-	100008-300		. . . Nut, Hex Machine		16	
			- - - * - - -			
-14	109350-021		. . . Plug, Snap In		1	
-15	130191-002		. . . Clamp, Cable		2	
-16	100657-001		. . . Clamp, Cable		1	
-17	100657-005		. . . Clamp, Cable		1	
			(Attaching Parts)			
-	100012-307		. . . Screw, Pan Hd		2	
-	100018-300		. . . Washer, Flat		2	
-	100024-300		. . . Washer, Lock Int. Tooth		2	
-	100008-300		. . . Nut, Hex Mach		2	
			- - - * - - -			

(Continued)

Table 9-8. Power Distribution Panel Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-8 -18	100720-004		. . . Grommet, Rubber		1	
-19	100720-007		. . . Grommet, Rubber		1	
-	132570-004		. . . Terminal, Ins Ring Tongue		4	
-	132570-001		. . . Terminal, Ins Ring Tongue		49	
			--- * ---			

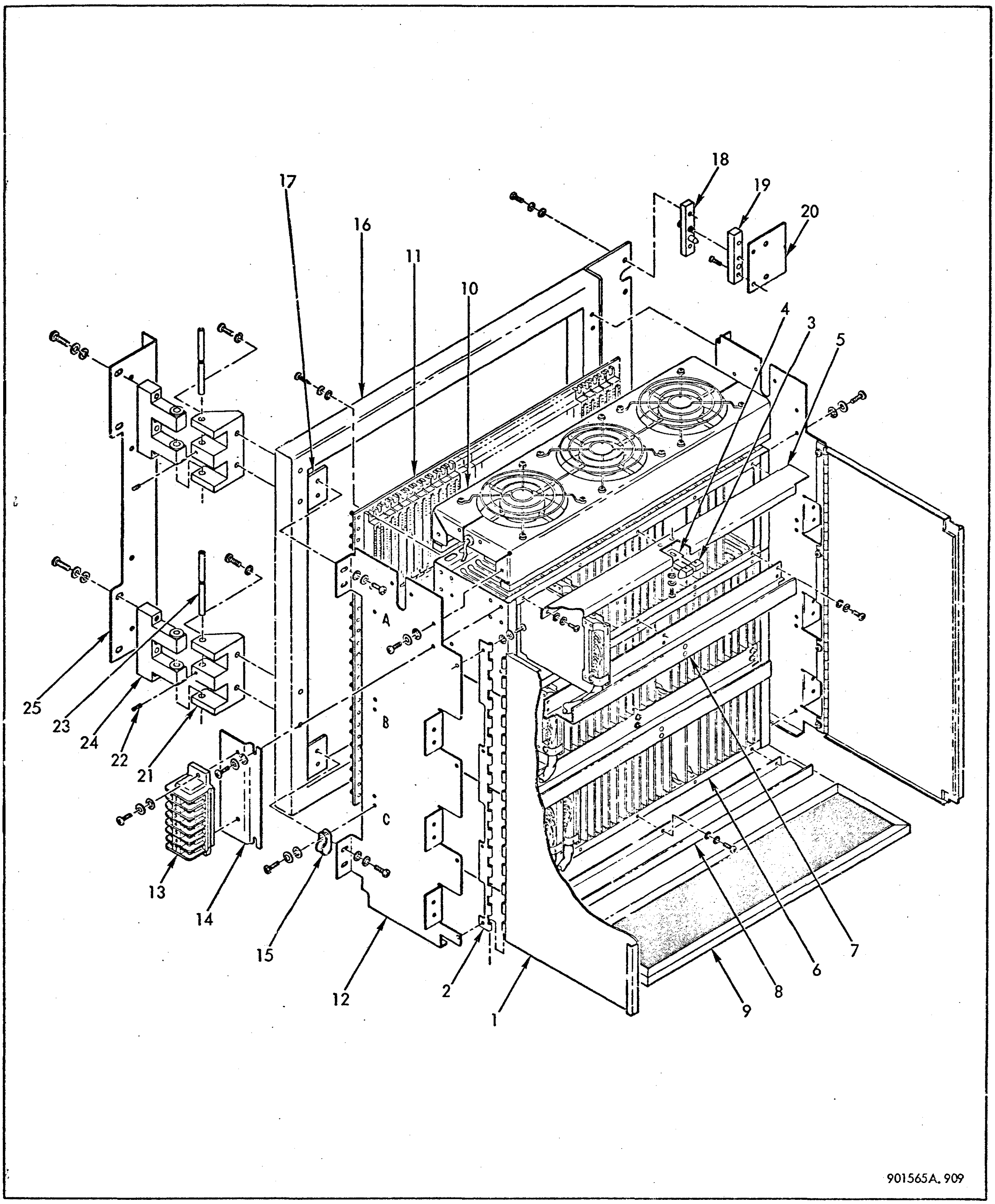


Figure 9-9. Extended Performance RAD Controller

Table 9-9. Extended Performance RAD Controller

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-9 -	149330 D		RAD Controller Assy (7231)		REF	
-1	131958		. Door, Chassis		2	
-2	131960		. Hinge, Chassis Door LH		1	
-2	131959		. Hinge, Chassis Door RH		1	
			(Attaching Parts)			
-	100012-204		. Screw, Pan Hd		8	
-	100018-200		. Washer, Flat		8	
-	100024-200		. Washer, Lock Int Tooth		8	
			- - - * - - -			
-3	129940		. Bracket, Door Latch Mtg		1	
			(Attaching Parts)			
-	100012-203		. Screw, Pan Hd		3	
-	100018-200		. Washer, Flat		3	
-	100024-200		. Washer, Lock Int Tooth		3	
			- - - * - - -			
-4	129554		. Trigger, Door Latch		2	
			(Attaching Parts)			
-	100012-105		. Screw, Pan Hd		2	
-	100018-100		. Washer, Flat		2	
			- - - * - - -			
-5	129540		. Spring, Door Latch		1	
			(Attaching Parts)			
-	100012-304		. Screw, Pan Hd		2	
-	100018-300		. Washer, Flat		2	
-	100024-300		. Washer, Lock Int Tooth		2	
			- - - * - - -			
-6	116231		. Chassis, 32 Module (See Fig. 9-10 for Module Locations)		3	

(Continued)

Table 9-9. Extended Performance RAD Controller (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-9 -6	129567-001		. Nut, Strip Speed		6	
			(Attaching Parts)			
-	100012-405		. Screw, Pan Hd		24	
-	100018-400		. Washer, Flat		24	
-	100024-400		. Washer, Lock Int Tooth		24	
			- - - * - - -			
-7	116522		. Channel, Cable Routing		2	
-8	123940-001		. Channel, Cable Routing		1	
			(Attaching Parts)			
-	100012-203		. Screw, Pan Hd		15	
-	100018-200		. Washer, Flat		15	
-	100024-200		. Washer, Lock Int Tooth		15	
			- - - * - - -			
-9	117427		. Filter, Air Panel		1	
-10	139637		. Top Fan Assy		1	
			(Attaching Parts)			
-	100012-304		. Screw, Pan Hd		8	
-	100018-300		. Washer, Flat		8	
-	100024-300		. Washer, Lock Int Tooth		8	
			- - - * - - -			
-11	139876 B		. Backwiring Board Assy		1	
			(Attaching Parts)			
-	114538-214		. Screw, Sheet Metal		54	
-	100018-300		. Washer, Flat		54	
-	100024-300		. Washer, Lock Int Tooth		54	
			- - - * - - -			
-12	145474-001		. Panel, Side Chassis Mtg LH		1	

(Continued)

Table 9-9. Extended Performance RAD Controller (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-9 -12	145475-002		. Panel, Side Chassis Mtg LH		1	
-13	109432-001		. Block, Terminal		7	
-13	109432-012		. Jumper, Terminal Block		1	
-13	109432-006		. Channel, Mtg (3.65 LG)		1	
-13	109432-008		. End, Plate		1	
-13	109432-011		. End, Anchor		2	
			(Attaching Parts)			
-	100012-304		. Screw, Pan Hd		2	
-	100018-300		. Washer, Flat		2	
-	100024-300		. Washer, Lock Int Tooth		2	
			- - - * - - -			
-14	139967		. Bracket, Mtg Terminal Block		1	
			(Attaching Parts)			
-	100012-410		. Screw, Pan Hd		2	
-	100018-400		. Washer, Flat		2	
-	100024-400		. Washer, Lock Int Tooth		2	
			- - - * - - -			
-15	100657-005		. Clamp, Cable Nylon		1	
-15	100657-007		. Clamp, Cable Nylon		2	
			(Attaching Parts)			
-	100012-405		. Screw, Pan Hd		1	
-	100018-400		. Washer, Flat		1	
-	100024-400		. Washer, Lock Int Tooth		1	
			- - - * - - -			
-16	147842		. Frame, Swing		1	

(Continued)

Table 9-9. Extended Performance RAD Controller (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-9 -17	147843		. Bracket, Mtg		1	
			(Attaching Parts)			
-	100012-506		. Screw, Pan Hd		4	
-	100018-500		. Washer, Flat		4	
-	100024-500		. Washer, Lock Int Tooth		4	
			- - - * - - -			
-18	139592		. Block, Shear Pin Mtg		2	
			(Attaching Parts)			
-	100012-508		. Screw, Pan Hd		2	
-	100018-500		. Washer, Flat		2	
			- - - * - - -			
-19	139593		. Block, Swing Frame Stop		2	
-20	149332		. Plate, Block Mtg		2	
			(Attaching Parts)			
-	100012-507		. Screw, Pan Hd		2	
-	100023-500		. Washer, Lock Spring		2	
			- - - * - - -			
-	149219		. . Hinge Assy		2	
			(Attaching Parts)			
-	108605-710		. . Screw, Cap Steel Soc Hd		4	
-	100023-700		. . Washer, Lock Spring		4	
			- - - * - - -			
-21	148498		. . . Bracket, Hinge		1	
-22	148499		. . . Bracket, Hinge Swing Frame		1	
-23	152051		. . . Pin, Hinge		1	
-24	132268-008		. . . Washer, Flat		2	

(Continued)

Table 9-9. Extended Performance RAD Controller (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-9 -25	149331		. . Angle, Swing Frame Mtg		1	
			(Attaching Parts)			
-	108605-712		. . Screw, Cap Steel Soc Hd		4	
-	100018-700		. . Washer, Flat		4	
-	100023-700		. . Washer, Lock Spring		4	

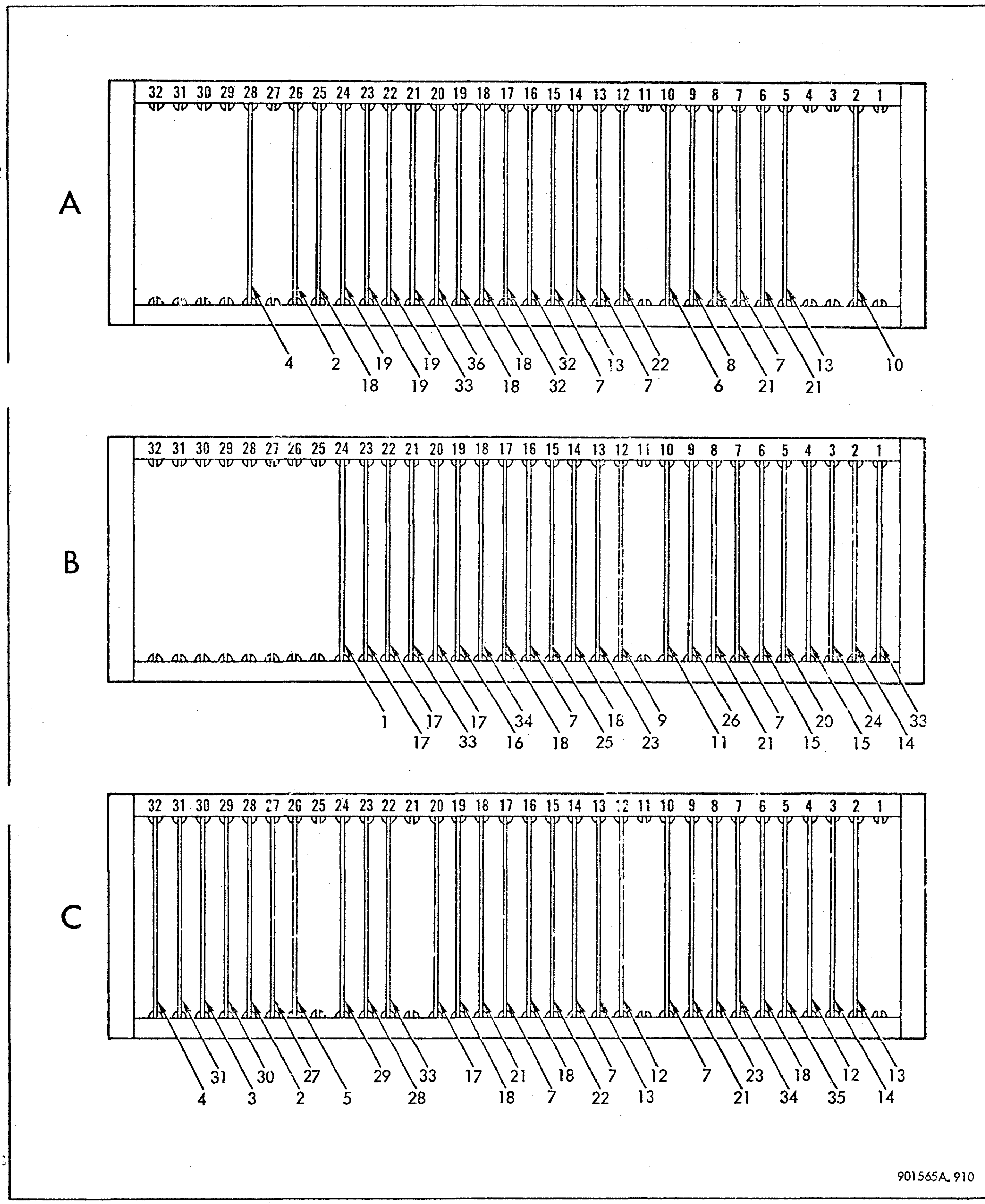


Figure 9-10. Module Location (RAD Controller)

Table 9-10. Module Locations (RAD Controller)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-10			(Module Locations) RAD Controller Assy			
9-10-1	128168		. Module Assy, AT24, Clock Driver #2		1	
-2	123018		. Module Assy, AT10 Cable Rec		2	
-3	123019		. Module Assy, AT11 Cable Dr/Rec		1	
-4	124629		. Module Assy, AT12 Cable Driver		2	
-5	126714		. Module Assy, AT17 Cable Dr/Rec		1	
-6	116056		. Module Assy, BT10 Buff AND/OR Gate		1	
-7	116029		. Module Assy, BT11 BAND Gate		8	
-8	116407		. Module Assy, BT13 Buff Matrix		1	
-9	125262		. Module Assy, BT16 Gated Buffer		1	
-10	123491		. Module Assy, CT10 Clock Oscillator		1	
-11	126611		. Module Assy, AT16 Rejection Gate		1	
-12	127393		. Module Assy, BT22 Fast Buffer		1	
-13	116380		. Module Assy, FT10 Basic Flip-Flop		4	
-14	117028		. Module Assy, FT12 Gated Flip-Flop		2	
-15	127319		. Module Assy, DT14 Delay Line		2	
-16	126743		. Module Assy, FT25 Fast Access Mem		1	
-17	126856		. Module Assy, FT26 Buff Latch No. 3		4	
-18	126986		. Module Assy, FT27 Buff Latch No. 2		8	
-19	133251		. Module Assy, FT41 Register FF		3	
-20	127391		. Module Assy, HT15 Delay/Line Sense		1	
-21	116994		. Module Assy, IT11 NAND Gate		6	
-22	117000		. Module Assy, IT13 Inverter Matrix		2	
-23	117375		. Module Assy, IT15 Gated Inverter		2	
-24	124634		. Module Assy, FT18 Counter Flip-Flop		1	
-25	125264		. Module Assy, IT16 Gated Inverter		1	
-26	128188		. Module Assy, IT24 NAND-NOR Gate		1	

(Continued)

Table 9-10. Module Locations (RAD Controller) (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
9-10-27	126710		. Module Assy, LT24 Logic Element		1	
-28	126712		. Module Assy, LT25 Logic Element		1	
-29	126982		. Module Assy, LT26 Switch Comp		1	
-30	133392		. Module Assy, LT41 Logic Element		1	
-31	133657		. Module Assy, LT43 Logic Element		1	
-32	134278		. Module Assy, LT58 Incr Decr		2	
-33	116257		. Module Assy, XT10 Term Module		4	
-34	117389		. Module Assy, BT15 Gated Buff No. 1		2	
-35	127643		. Module Assy, LT29 Clock Logic		1	
-36	136547		. Module Assy, LT71 Exclusive OR		1	

Table 9-11. Numerical Index

Fig. & Index No.	XDS Part Number	Description
	100008-100	Nut, Hex Mach
	100008-200	Nut, Hex Mach
	100008-300	Nut, Hex Mach
	100008-400	Nut, Hex Mach
2-27	100008-410	Nut, Hex
	100008-500	Nut, Hex Mach
	100008-600	Nut, Hex
	100012-104	Screw, Pan Hd
	100012-105	Screw, Pan Hd
	100012-203	Screw, Pan Hd
	100012-204	Screw, Pan Hd
	100012-205	Screw, Pan Hd
	100012-207	Screw, Pan Hd
	100012-210	Screw, Pan Hd
	100012-304	Screw, Pan Hd
	100012-305	Screw, Pan Hd
	100012-306	Screw, Pan Hd
	100012-307	Screw, Pan Hd
3-	100012-310	Screw, Pan Hd
	100012-314	Screw, Pan Hd
	100012-316	Screw, Pan Hd
	100012-320	Screw, Pan Hd
	100012-404	Screw, Pan Hd
	100012-405	Screw, Pan Hd
	100012-406	Screw, Pan Hd
	100012-407	Screw, Pan Hd
	100012-408	Screw, Pan Hd

Fig. & Index No.	XDS Part Number	Description
	100012-410	Screw, Pan Hd
	100012-414	Screw, Pan Hd
	100012-500	Screw, Pan Hd
	100012-504	Screw, Pan Hd
	100012-505	Screw, Pan Hd
	100012-506	Screw, Pan Hd
	100012-507	Screw, Pan Hd
	100012-508	Screw, Pan Hd
	100012-520	Screw, Pan Hd
	100012-610	Screw, Pan Hd
	100018-100	Washer, Flat
	100018-200	Washer, Flat
	100018-300	Washer, Flat
2-23	100018-310	Washer, Flat
	100018-400	Washer, Flat
	100018-500	Washer, Flat
	100018-600	Washer, Flat
	100023-500	Washer, Lock Spring
	100023-600	Washer, Lock Spring
	100023-700	Washer, Lock Spring
	100024-100	Washer, Lock Int Tooth
	100024-200	Washer, Lock Int Tooth
	100024-300	Washer, Lock Int Tooth
	100024-400	Washer, Lock Int Tooth
	100024-500	Washer, Lock Int Tooth
	100024-600	Washer, Lock Int Tooth
7-8	100025	Diode, XDS101 (VR3, 4)

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
	100039-307	Screw, Flat Hd
3-	100039-310	Screw, Flat Hd
	100039-405	Screw, Flat Hd
	100039-510	Screw, Flat Hd
3-	100039-520	Screw, Flat Hd
2-	100039-609	Screw, Flat Hd
2-49	100274-016	Sleeve, Plastic
7-7	100323	Diode, XDS106 (VR1, 2, 5 thru 9)
8-11	100331	Fuse, Holder
8-10	100653-006	Fuse, .250 AMP 3AG (F1)
8-17	100657-001	Clamp, Cable
3-11	100657-002	Clamp, Cable
2-36, 3-13	100657-003	Clamp, Cable
6-37, 8-19	100657-004	Clamp, Cable Nylon
6-51, 8-18	100657-005	Clamp, Cable
8-17	100657-007	Clamp, Cable Nylon
2-35	100657-008	Clamp, Nylon
3-19	100657-009	Clamp, Cable
3-18	100657-011	Clamp, Cable
7-3	100698	Transistor XDS210 (Q2, 3, 6, 7, 8, 10, 11)
8-18	100720-004	Grommet, Rubber
5-24	100720-006	Grommet, Rubber
8-20	100720-007	Grommet, Rubber
6-23	100720-009	Grommet, Rubber
2-44	100840-001	Grommet, Nylon
6-36	100840-002	Grommet, Nylon
2-45	100840-003	Grommet, Nylon
6-42, 67, 69	100992-003	Capacitor, DV Oil/Paper (C3, 4, 6, 7, 8, 30, 31, 32)
6-75	100992-006	Capacitor, DV Oil/Paper (C5)
7-11	101154	Diode, XDS113 (CR1 thru 13, 16, 17, 19 thru 22, 26, 27)
6-64	101155-150	Resistor, Fixed WW (R1)
8-13	101430	Receptacle, Female 3 Contact (J2, 3, 4, 5, 6, 7, 8)
2-	101441-104	Screw, Cap Hex Hd
2-	101441-105	Screw, Cap Hex Hd
2-	101441-407	Screw, Cap Hex Hd
6-78	101625-003	Tubing, Spirap
2-29	101918	Bolt
7-4	102055	Transistor XDS 214 (Q4)
5-52	102066-001	Cord, Lacing
7-5	103242	Transistor XDS 216 (Q9)
6-55	106843	Socket, Relay
6-54	106994	Relay DC (K3, 4, 7, 8)
6-52	107013-308	Standoff, Threaded
6-44	107018-314	Standoff, Hex
6-43	107132-003	Spacer, Round
6-68	107132-005	Spacer, Round LH
6-68	107132-006	Spacer, Round RH
9-22	107151-303	Screw, Set Socket
3-25	107199-308	Roll, Pin
5-9	107199-413	Roll, Pin

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
5-46	107199-614	Roll Pin, Cres (3/16 Dia x 7/8 Lg)
3-30	107396	Switch, Toggle
6-65	108474	Capacitor, JN Electrolytic (C1)
3-36	109159-008	Bumper, Rubber
8-15	109350-021	Plug, Snap In
3-20, 2-50, 6-45	109432-001	Block, Terminal Stack Type 8-18 AWG
2-50, 6-46	109432-005	Retaining Clip
3-20, 2-50, 6-47	109432-006	Mounting Channel
3-20, 2-50, 6-48	109432-008	End Plate
3-20	109432-011	End Anchor
6-49, 9-13	109432-012	Jumper, Terminal Block
7-18	110996-100	Resistor 1W (R18, 30, 38)
7-36	110996-101	Resistor 1W (R55)
7-15	110996-103	Resistor 1W (R2)
2-48	110996-105	Resistor 1W (R20 thru 24)
7-16	110996-152	Resistor 1W (R3)
7-24	110996-183	Resistor 1W (R31)
7-17	110996-202	Resistor 1W (R25, 45, 50)
7-22	110996-273	Resistor 1W (R46 thru 49)
8-4	110996-331	Resistor 1W (R1)
6-58	110996-471	Resistor 1W (R56)
7-21	110996-473	Resistor 1W (R33)
2-8	111097	Bracket, Locking
5-3	111468-502	Insert Thread
7-9	111516	Diode, XDS123 (CR14)
7-2	111530	Transistor, XDS231 (Q1, 5)
2-31	111945	Pump, Positive Pressure
6-	113220-300	Washer, Flat Light Series
6-	113220-600	Washer, Flat Light Series
6-	113221-200	Washer, Lock Spring
6-	113221-300	Washer, Lock Spring
6-	113221-400	Washer, Lock Spring
6-	113221-500	Washer, Lock Spring
5-11	113440-206	Screw, Cap Soc Hd
6-	113526-006	Nut, Self Clinching
6-	113526-012	Nut, Self Clinching
6-40	113694	Switch, Subminiature DPT Toggle (S1)
6-25	113707-002	Switch, Pressure (S2, 3)
3-40	113800-204	Screw, Shoulder Slotted
3-37	113800-212	Screw, Shoulder Slotted
3-	114538-214	Screw, Sheet Metal
7-14	115763-103	Capacitor Mylar (C21, 22, 23)
10-7	116029	Module Assy, BT11 BAND Gate
10-6	116056	Module Assy, BT10 Buff AND/OR Gate
3-6, 9-6	116231	Chassis, 32 Module (See Fig. 9-10 For Module Locations)
10-33	116257	Module Assy, XT10 Term Module
10-13	116380	Module Assy, FT10 Basic Flip-Flop
10-8	116407	Module Assy, BT13 Buff Matrix

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
3-8	116522	Channel, Cable Routing
2-35, 6-15, 30	116701	Tubing, Pressure
6-27	116702-001	Connector, Elbow
6-8, 6-21, 27	116702-002	Connector, Elbow
3-26	116722-003	Spring, Compression
10-21	116994	Module Assy, IT11 NAND Gate
10-22	117000	Module Assy, IT13 Inverted Matrix
2-32	117026-005	Mount, Shear
10-14	117028	Module Assy, FT12 Gated Flip-Flop
9-21	117136	Pivot, Hinge Swing Frame
9-24	117137	Block, Hinge Swing Frame
6-16	117226	Filter, Air
10-23	117375	Module Assy, IT15 Gated Inverter
10-34	117389	Module Assy, BT15 Gated Buffer No. 1
2-1	117419	Cabinet, Basic Structure
2-2	117424	Cap, Cabinet Top
3-10	117427	Filter, Air
10-2	123018	Module Assy, AT10 Cable Rec
10-3	123019	Module Assy, AT11 Cable Dr/Rec
5-51	123054-104	Screw, Button Hd
7-37	123300-124	Capacitor, Tantalum (C29)
7-13	123300-126	Capacitor, Tantalum (C13, 28)
7-12	123300-475	Capacitor, Tantalum (C9 thru 12)
7-27	123362-084	Resistor, 1/8W (R6, 8)
7-29	123362-147	Resistor, 1/8W (R28, 40, 42, 44, 53, 54)
7-25	123362-164	Resistor, 1/8W (R37)
7-35	123362-172	Resistor, 1/8W (R16)
7-32	123362-176	Resistor, 1/8W (R17, 34, 11, 15, 29, 52)
7-30	123362-197	Resistor, 1/8W (R12)
7-33	123362-212	Resistor, 1/8W (R26, 36)
7-31	123362-219	Resistor, 1/8W (R14)
7-26	123362-243	Resistor, 1/8W (R3, 5, 9, 10, 13, 35, 51)
7-28	123362-281	Resistor, 1/8W (R7)
7-34	123362-339	Resistor, 1/8W (R19, 27)
5-34	123450	Shaft, Spindle
5-	123455	Spindle & Drive Assy
5-5	123456	Ball Bearing
5-31	123460-021	"O" Ring Teflon
10-10	123491	Module Assy, CT10 Clock Oscillator
3-9, 9-8	123940	Channel, Cable Routing
7-6	124298	Pad, Transistor (Q1 thru 8, 10, 11 REF)
10-4	124629	Module Assy, AT12 Cable Driver
10-24	124634	Module Assy, FT18 Counter Flip-Flop
10-9	125262	Module Assy, BT16 Gated Buffer

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
10-25	125264	Module Assy, IT16 Gated Inverter
7-38	126297-001	Terminal Bif Rivet (E1 thru 45)
3-42, 6-4	126340-002	Fastener, Captive XDS
3-24	126340-010	Fastener, Captive XDS
6-7	126440-012	Fastener, Captive XDS
10-11	126611	Module Assy, AT16 Rejection Gate
5-4	126623	Bearing, Retainer
5-47	126624	Liner, Spindle Housing
10-27	126710	Module Assy, LT24 Logic Element
10-28	126712	Module Assy, LT25 Logic Element
10-5	126714	Module Assy, AT17 Cable Dr/Rec
5-3	126716	Disc, Hub
10-16	126743	Module Assy, FT25 Fast Access Memory
5-35	126835-003	Woodruff, Key
7-17	126856	Module Assy, FT26 Buff Latch No. 3
6-66	126945-002	Bracket, Capacitor Mtg
10-29	126982	Module Assy, LT26 Switch Comp
10-18	126986	Module Assy, FT27 Buff Latch No. 2
5-3	127054	Insert, Hub
8-3	127055	Transformer (T1)
5-45	127056	Spindle, Housing Assy
10-15	127319	Module Assy, DT14 Delay Line

Fig. & Index No.	XDS Part Number	Description
5-32	127346-001	Shim, Retaining Bearing
5-32	127346-002	Shim, Retaining Bearing
5-32	127346-003	Shim, Retaining Bearing
5-1	127387-001	Nut, Lock
5-2	127388	Washer, Hub Positioning
5-3	127389	Hub, Assy
10-20	127391	Module Assy, HT15 Delay/ Line Sense
10-12	127393	Module Assy, BT22 Fast Buffer
3-44	127489-002	Connector, 50 Pin
3-45	127614	Plate Mtg, Connector Plug
10-35	127643	Module Assy, LT29 Clock Logic
8-14	127675	Receptacle Male, 3 Contact (J1)
6-6	127990	Container, Filter-Charcoal
5-25	128155-001	Thermostat, Overtemp
5-33	128163-002	Washer, Spring
10-1	128168	Module Assy, AT24 Clock Driver #2
10-26	128188	Module Assy, IT24 NAND NOR Gate
2-9	129459	Slide, 20 Inch 175 Lb
3-4, 9-5	129540	Spring, Door Latch
3-3, 9-4	129554	Trigger, Door Latch
3-6, 9-6	129567	Nut, Strip Speed
5-38	129633-204	Screw, Cap Soc Hd
5-18	129633-206	Screw, Cap Soc Hd
5-30	129633-506	Screw, Cap Soc Hd

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
5-30	129633-508	Screw, Cap Soc Hd
2-25	129633-628	Screw, Cap Soc Hd
6-70	129645-002	Bracket Capacitor Mtg
6-61, 8-5	129681	Relay, Time Delay Thermal (K5, K15)
6-62, 8-6	129682	Socket, Time Delay
5-43	129687	Baffle, Air Spindle & Drive
3-7	129694	Panel, Blank
6-6	129731	Filter, Container Assy
9-3	129940	Bracket, Door Latch Mtg
7-23	130109-097	Resistor, 1W (R39, 41, 43)
6-57, 8-4	130132	Relay, DPDT 10A (K1, 2, 9)
6-75, 8-16	130191-001	Connector, Cable Grip
2-51, 8-15	130192-002	Clamp, Conduit
6-53, 8-8	130422-001	Contactor, 3 Pole St (K5, 6, 1)
8-12	130462	Switch, Toggle DPDT (S1)
8-7	130540	Relay, DPDT 5A 24VDC Coil (K3)
3-5	130639	Bracket, Door Latch Mtg Support
6-60	130765	Relay, 4 Form C 24VDC (K10)
5-27	130777-001	Spacer, Rotor
5-29	131186	Cap, Load Spring Retaining
8-2	131326	Cover, Distribution Panel
2-10	131354	Bracket, Slide Mtg Front
2-20	131356	Plate, Drum Mtg
2-23	131357	Bracket, Shipping

Fig. & Index No.	XDS Part Number	Description
2-22	131362	Bracket, Leg Support
5-44	131530-103	Screw, Drive
9-2	131950	Hinge, Chassis Door LH
3-1, 9-1	131958	Door, Chassis
3-2	131959	Hinge, Chassis Door
3-2, 9-2	131960	Hinge, Chassis Door RH
5-42	131963	Housing, Motor
5-37	131964	Baffle, Motor Housing
5-10	131965	Cap, Motor Housing
5-40	131977-004	Motor, Elec Three Phase (Stator)
5-28	131977-005	Motor, Rotor
2-6	132019	Angle, Mtg Rear (Retma)
2-33	132083-001	Union, Tube Fitting
6-29	132083-002	Union, Tube Fitting (Male Pipe to Plastic)
6-14	132084	Union, Bulkhead
5-8	132086	Spline, Brake Drive
2-11	132088	Bracket Slide, Mtg Rear
5-41	132103-001	Screw, Motor Housing
6-1	132175	Chassis, Motor Control Unit
6-4	132176	Cover, Chassis Motor Control Unit
6-70	132177	Bracket, Capacitor Mtg
6-35	132178	Bracket, Component Mtg
6-59	132179	Bracket, Relay Mtg
7-	132343	Printed Wiring, Motor Control Unit (TB1)
7-11	132344	Board, Printed Wiring

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
6-24	132359	Bracket, Solenoid Mtg
6-72	132369	Transformer (T1)
6-73	132492	Transformer (T2)
7-10	132494	Diode, XDS 135 (CR23, 24, 25)
6-39	132495	Thyristor, XDS 236 (SCR1, SCR2, SCR3)
6-10	132514	Filter, Air Charcoal
6-32	132528	Tee, Tube Fitting
6-33	132529-001	Tee, Female Pipe Fitting
6-31	132532-002	Elbow, Street
6-22	132534	Valve, Solenoid (K12, 13, 14)
3-45, 6-63	132570-001	Terminal, Ins Ring Tongue
5-13	132570-002	Terminal, Ins Ring Tongue
2-47	132570-004	Terminal, Ins Ring Tongue
6-	132570-005	Terminal, Ins Ring Tongue
5-50	132593	Generator, Tachometer
2-21	132644	Leg Support Assy
2-18	132646	Plate, Counter Balance
5-54	132743	Shaft, Coupling-Tachometer
6-11	132744	Gasket, Filter Mtg
6-19	132749-001	Nipple, Pipe Fitting
6-25	132749-002	Nipple, Pipe Fitting
6-28, 6-34	132749-005	Nipple, Pipe Fitting
6-18	133033-001	Plug, Pipe Hex Hd
6-34	133033-002	Plug, Pipe Hex Hd
6-41	133034-001	Circuit Breaker (CB1)
5-7	133079-406	Screw, Flat Hd

Fig. & Index No.	XDS Part Number	Description
5-48	133080	Plate, Adaptor Tachometer
2-18	133155	Plate, Counter Balance
10-19	133251	Module Assy, FT41 Register FF
10-30	133390	Module Assy, LT41 Logic Element
5-52	133559-026	Wire, Twisted Pair
10-31	133657	Module Assy, LT43 Logic Element
10-32	134279	Module Assy, LT58 Incr Decr
6-31	134843	Cover, Protective
6-26	134843	Cover, Protective
6-9	134844-001	Nut, Lock
9-23	134897	Pin, Hinge
6-17	134993	Regulator, Pressure
6-74	136179	Cable, 4 Conductor
10-36	136547	Module Assy, LT71 Exclusive OR
6-77	136560-002	Connector, 14 Contact Female
5-12	136561-001	Connector, Male 14 Pin (J37)
3-41	136588	Chart, Hd Wiring
2-39	136674	Power Supply Assy, PT20
2-38, 8-	137529	Power Distribution, Panel Assy
8-1	137530	Chassis, Distribution Panel
2-46	139175	Filter, Power (C1, 2, 3, 4)
2-41	139222	Power, Filter Assy
2-42	139223	Plate, Mtg
2-43	139224-002	Cover, Filter

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
4-1	139418	Module Assy, LT76 Read Write
2-3	139565-002	Clip, Speed U Type
1-	139576	Extended Performance, RAD Assy
9-18	139592	Block, Shear Pin Mtg
9-19	139593	Block, Swing Frame Stop
3-22	139634-001	Panel, Side Chassis RH
3-22	139634-002	Panel, Side Chassis LH
3-23	139635	Frame Pivot, Chassis Mtg
3-34	139636	Frame Pivot, Sel Unit Mtg
3-17, 9-10	139637	Top Fan Assy
3-33	139686	Pin, Hinge
2-17, 3-	139690	Selection Unit Assy
2-26, 5-	139697	Disc File Assy
4-6	139716	Module Assy, LT77 Data Decode
2-4	139814-001	Bracket, Chassis Locking LH
2-12	139815-001	Bracket, Slide Sel Mtg RH Front
2-12	139815-002	Bracket, Slide Sel Mtg LH Front
2-13	139816-001	Bracket, Slide Sel Mtg RH Rear
2-13	139816-002	Bracket, Slide Sel Mtg LH Rear
2-14	139858	Angle Support, Front
3-12	139865	Backwiring Board Assy
9-11	139876	Backwiring Board Assy
3-35	139892-001	Angle Support
3-35	139892-002	Angle Support

Fig. & Index No.	XDS Part Number	Description
9-14, 3-21	139967	Bracket Mtg Terminal Block
3-15	139968	Strip Mtg, Wire Clamp
3-16, 3-43	139969	Block, Wire Clamping
2-5	139994-001	Angle Mtg, RF (Retma)
2-5	139994-002	Angle Mtg, RF (Retma)
2-19	145315-001	Angle Spacer Slide, RH
2-19	145315-002	Angle Spacer Slice, LH
2-7	145412-001	Bracket, Latch Adjusting LH
2-7	145412-002	Bracket, Latch Adjusting RH
3-28	145418	Guide, Rod
3-27	145419-001	Rod, Latch
3-27	145419-002	Rod, Latch
3-29	145420-001	Block, Latch
3-29	145420-002	Block, Latch
9-12	145474-001	Panel, Side Chassis Mtg LH
9-12	145474-002	Panel, Side Chassis Mtg RH
3-41	145514	Cover, Connector
3-38	145515	Cover, Connector-Base Plate
6-20	145646	Fitting, Adapter Bulkhead
2-15	145698	Bumper, Rubber
3-31	145704	Panel, Switch Mtg
6-56	146260	Bracket, Relay Mtg
6-2	146484	Chassis, Filter Mtg Motor Control Unit
2-37, 6-	146485	Motor Control Unit Assy

(Continued)

Table 9-11. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
6-3	146486	Angle Mtg LH, Motor Control Unit
6-3	146487	Angle Mtg RH, Motor Control Unit
2-40	146488-001	Angle, Chassis Mtg RH
2-40	146488-002	Angle, Chassis Mtg LH
2-34	146649	Bracket, Component Mtg
3-39	146673	Hanger
3-32	147024	Rod Hanger, Interface
6-5	147044-001	Label, Filter
6-12	147044-002	Label, Filter
5-6	147222-001	Brake, Magnetic
4-5	147791	Module Assy, AT15 Clock Discr
9-16	147842	Frame, Swing
9-17	147843	Bracket, Mtg
2-16	147912-001	Bracket, Frame Mtg RH
2-16	147912-002	Bracket, Frame Mtg LH
2-24	147931-006	Mount, Shock
5-	148433	Bulkhead Unit-Disc File Assy
2-52, 9-	149330	7231 RAD Controller Assy
9-25	149331	Angle Swing Frame Mtg
9-20	149332	Plate, Block Mtg
5-23	149578-001	Brush, Metal Graphite
5-20	149579-001	Cartridge, Brush Holder
5-21	149580	Bracket, Cartridge
5-17	149581	Clamp, Cartridge
6-38	149710	Cover, Protective
2-	149763	RAD Storage, Unit Cabinet Assy
2-30	149960	Compressor, Assy
5-22	152008	Plug, Screw
3-46	152429-001	Screw, Captive
3-47	152429-002	Retainer, Insert Screw
3-14	152673	Ground Strap Assy
6-13	158947	Absolute Filter Unit Assy

XDS

Xerox Data Systems

PUBLICATION DATA QUICK

PDQ NO. 70-054

PUBLICATION NO. XDS 901565A-1

DATE 22 July 1970

TO: ALL HOLDERS OF XDS Extended Performance RAD File, Models 7231/7232

SUBJECT: TEMPORARY CHANGES TO TECHNICAL MANUAL

The following changes to Technical Manual 901565A-1 are necessary to reflect the latest technical information. The changes are released in this manner for purposes of expediency. The next scheduled revision to the manual will incorporate these changes formally.

PURPOSE: To add a monthly check of the tachometer output voltage to the maintenance section.

INSTRUCTIONS:

1. Make the following changes in the technical manual with pen and ink:
   a. Page 8-22, paragraph 8-33. Between last line of paragraph 8-33 and paragraph 8-34, write in:
      "8-33A TACHOMETER OUTPUT VOLTAGE TEST PROGRAM (see insert on attached page 8-22A)".
2. Insert pages of this PDQ into the technical manual as follows:
   a. Page 1 of this PDQ between cover and title page of the technical manual.
   b. Page 2 of this PDQ (marked page 8-22A) between pages 8-22 and 8-23.

Do not remove these pages until the above changes have been incorporated in a released revision or re-issue of the technical manual.

APPROVED: [signature]

MANAGER PUBLICATIONS DEVELOPMENT