systems engineering laboratories, incorporated

BULLETIN 9031

SEL 8500 SERIES MICROLOGIC MODULES





CONTENTS

1.	INTRODUCTION	
2.	SEL MICROLOGIC CIRCUIT MODULES	3
3.	CIRCUIT LOADING RULES	17
4.	TYPICAL CIRCUIT APPLICATIONS	19
5.	GROUNDING AND POWER DISTRIBUTION RULES	33
6.	SEL STANDARD LOGIC TRAYS AND PACKAGING ACCESSORIES	35

	NAME AND PART NO.	INPUT APPEARS AS	CIRCUITS PER CARD	OUTPUT WILL DRIVE	+3.6 VOLT POWER REQUIRED* PER CIRCUIT (TYPICAL)	SYMBOL AND PIN ASSIGNMENTS
	2-NOR 8522	I LOAD EACH INPUT	8	5 LOADS	9.0 ma	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
	3-NOR 8504	I LOAD EACH INPUT	6	5 LOADS	9.0 ma	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
	4-NOR 8526	i Load Each input	5	5 LOADS	9.0 ma	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
	J-K FLIP-FLOP 8524	TRIGGER-2 LOADS STEERING-1 LOAD RESET-1 LOAD	4	5 LOADS	18.6 ma	24 18 11 5 26
	3 J-K FLIP-FLOP 8528	TRIGGER-2 LOADS STEERING-1 LOAD RESET-1 LOAD	3	5 LOADS	18.6 ma	27 18 6 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7
	BUFFER 8501	2 LOADS	6	25 LOADS	17.4 ma	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
	HALF-ADDER 8523	1 LOAD EACH INPUT	4	OUTPUT E -4 LOADS OUTPUT F -5 LOADS	17.7 ma	27 26 27 27 28 27 28 28 27 28 28 28 28 28 28 28 28 28 28 28 28 28
	INVERTER 8525	I LOAD EACH INPUT	12	5 LOADS	9 ma	$25 - \bigcirc_{(1)} - 22 \qquad 26 - \bigcirc_{(2)} - 23 \qquad 27 - \bigcirc_{(3)} - 21 \qquad 24 - \bigcirc_{(4)} - 20 \qquad 17 - \bigcirc_{(5)} - 14 \qquad 19 - \bigcirc_{(5)} - 13$ $18 - \bigcirc_{(7)} - 12 \qquad 16 - \bigcirc_{(8)} - 15 \qquad 7 - \bigcirc_{(9)} - 4 \qquad 9 - \bigcirc_{(10)} - 3 \qquad 10 - \bigcirc_{(11)} - 5 \qquad 8 - \bigcirc_{(12)} - 6$
	2-NOR GATE 8527	1 LOAD EACH INDIVIDUAL INPUT 12 LOADS COMMON INPUT	12	5 LOADS	9 ma	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
	3-NOR EXPANDER 8531	I LOAD EACH INPUT	6	**	9 ma	27
2	4-NOR EXPANDER 8530	1 LOAD EACH INPUT	5		9 ma	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

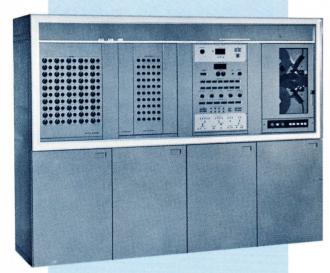
*POWER REQUIREMENTS SHOWN ARE BASED ON CIRCUIT IN MAXIMUM POWER CONSUMMATION STATUS

** DEPENDS UPON CONFIGURATION OF EXPANSION—SEE SPECIFICATION SHEET.





SEL 810 GENERAL PURPOSE DIGITAL COMPUTER

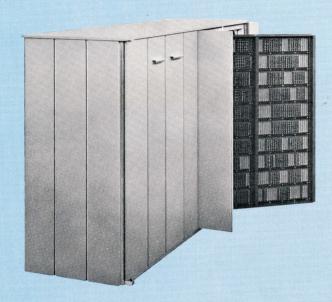


SEL 600 DATA ACQUISITION SYSTEM

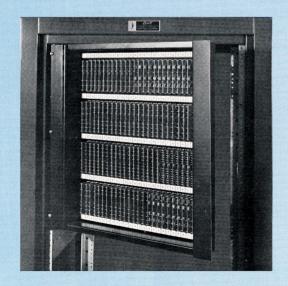
In the past few years, Systems Engineering Laboratories, Incorporated (SEL) has become a leader in the field of digital data acquisition and processing. SEL data acquisition and processing systems are at work all over the country serving the instrumentation and control needs of industry, the military, and government agencies. SEL direct data digital control systems have automated the production lines of some of the largest industrial plants.



4-ROW HORIZONTAL TRAY



SEL EXTENDED PAGE PLANE



MODULAR PANEL

SEL engineers are continually striving for new methods art techniques to improve accuracy, reliability, reduce cost, reduce size and increase speed and operating frequencies.

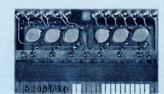
The basic element of all SEL logic units is the circuit modul. Advancing technology has now made possible the fabrication of super-small circuit modules.

SEL engineers have incorporated these micro-logic elements into SEL standard modules. These micrologic cards are directly compatible with all SEL standard packaging techniques ar are now being used in many SEL systems—especially in the digital computer line where accuracy, reliability, speed, and size are becoming increasingly more important.

The circuit card trays are designed around the physical properties of the cards (with several unique and convenient features). The card trays, files, and other packaging accessoridare standard products. Therefore, the circuit designer does not buy a packaging problem when he employs SEL micrologic circuit cards to implement his logic system.

This manual is devoted to acquainting the reader with the characteristics of SEL micrologic modules and their application. In addition, information is included on SEL packagin techniques. No attempt has been made to describe every micrologic circuit module SEL produces; however, a representative number of modules are described. Included are certa SEL design philosophy, descriptions of SEL circuit module, circuit loading rules, typical circuit applications, grounding and power distribution rules.





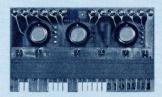














The SEL micrologic circuit design and packaging are derived from extensive experience and reflect the latest thinking in the industry. The circuits are highly versatile, thereby reducing the number of different types required.

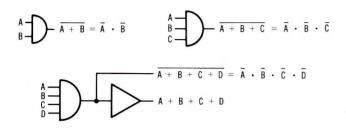
All circuit designs are based on "worst case" conditions. Simply stated, this philosophy requires that each circuit must operate properly when all power supply voltages, components and operating temperature are at their extreme limit or tolerance. MIL components and practices are used in all cases when applicable. Components are derated to less than 10 percent in most cases, and without exception, to less than 50 percent.

SEL micrologic cards are designed to eliminate the inter-connection problems inherent in breadboarding and system construction using micrologic elements. The cards are directly compatible with all SEL Standard Packaging techniques. By using the proven-in-use wire wrap technique for interconnection, any desired interconnections are readily mechanized.

Each logic element has an easily accessible test point located on the upper surface of the board. The elements presently in use are the Fairchild Industrial line of Micrologic. All elements have military counterparts; therefore, breadboarding of logic using these inexpensive devices will allow verification of logic design for military environments before fabrication of expensive high density packages.

All inputs and outputs are brought out to pins on the 29 Pin ELCO connector. Pins 1 and 29 are connected to \pm VC (3.6VDC). Pins 2 and 28 are connected to ground. Decoupling capacitors on each card minimize noise problems. These circuits are high speed devices and as such require careful handling of the ground and signal lines.

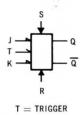
SEL has found it convenient to re-define the logic as NOR logic and revise the symbology to agree with presently used SEL symbols. In NOR terminology, the level closest to $\pm Vc$ will be defined as "1" and the level closest to ground will be defined as "0", or more compactly, a positive (\pm) input is a "1" and a negative (relatively) input is a "0". Using these definitions, and the SEL symbol sheet, the following definitions apply.



JK FLIP-FLOP TRUTH TABLE

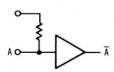
AT T=N			
j	K		
0	0		
0	1		
1	0		
1	1		

Q	Q
Q	Q
0	1
1	0
Q	Q



A "1" on the Reset (R) terminal resets the flip-flop to the state where the Q output is a "0" logic level. If this reset is present during a negative-going clock transition a "carry spike" will occur on the Q terminal, but the output will return to the reset state after it propagates.

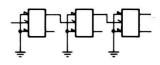
The digital buffer is primarily a fan-out multiplier, however, it can be used to form oscillators, one-shots, etc.



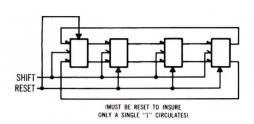
DIGITAL BUFFER

Obviously, the symbology used can be re-defined if desirable. For instance the R input on the J-K could be defined as a S, by "turning over" the symbol.

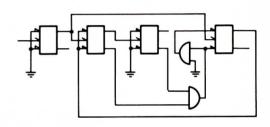
Some applications drawings are probably the easiest way to show inter-connection possibilities. A more complete treatment of circuit applications can be found in Section 4.



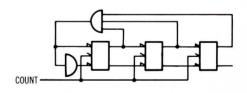
RIPPLE-THROUGH COUNTER



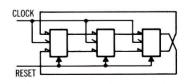
RING COUNTER



BCD RIPPLE-THROUGH COUNTER



SELF-MONITORED "RING" COUNTER 4 STATES



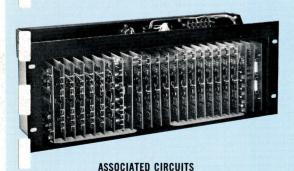
JOHNSON OR "WALKING CODE" COUNTER 6 STATE







STANDARD WIREWRAP TECHNIQUE



The mechanical considerations involved in the construction of a circuit card can play a very important part in the ultimate reliability of the circuits on the card. SEL logic circuits are packaged on epoxy glass fiber printed circuit cards. The circuit cards are printed on only one side to avoid problems concerned with feedthrough of printed circuit lands. Each component is mounted so that the leads are free to absorb stresses due to thermal expansion without endangering case seals and attachments. No evelets or plated-through holes are used. The printed circuit is never used as a contact surface. The size and shape of the cards minimize flexing which is often a primary cause of sudden "unexplained" solder joint failures. Each circuit on a card is provided with a conveniently located test point which eliminates the necessity of connecting test equipment probes to the component leads or to the connector pins. Self-guiding, self-supporting Elco Varicon connectors are used. These connectors make it impossible to insert the card incorrectly into the mating connector. All wiring connections to the mating connector are accomplished using the proven "wire wrap" technique. Stringent quality control is maintained throughout all phases of circuit card fabrication and testing.

PACKAGING

When you use SEL micrologic circuits in your system, you gain the option of including the same mechanical features used in systems built by Systems Engineering Laboratories, Incorporated. SEL has expended considerable effort and expense in designing and developing a complete line of versatile, rugged and easy to use slideout card trays. Naturally, SEL card trays are completely compatible with the SEL printed circuit modules in every respect; therefore, the mechanical design expense of your system can be greatly reduced by incorporating these "proven in use" card trays.

OTHER CIRCUITS AVAILABLE

In addition to the digital micrologic circuits described in this manual, Systems Engineering Laboratories, Incorporated also has available a complete line of associated circuits such as magnetic core memory driver circuits, digital tape record amplifiers, tape playback preamplifiers and translators. These associated circuits are also proven-reliable circuits which are presently being used in numerous SEL manufactured data acquisition and processing systems. Information on these and other special application circuits is available upon request.

MICROLOGIC CIRCUIT MODULES

The Micrologic Two-Input NOR circuit is a decision element which can perform all the functions required for any logical operation. It can be used for AND gates, OR gates, inverters, and DC controlled latches. Two inputs are provided. In logical functions the output will be positive when both inputs are at 0 volts. The circuit can be used with expander circuits to provide multi-input OR gates and AND gates. The reaction of the output (C) to the condition of the inputs (A and B) is shown in the Truth Table below.

TRUTH TABLE

А	В	С
1	0	0
0	1	0
1	1	ő
0	0	1

Where:
$$+V = \text{logical "1"}$$

$$0V = \text{logical "0"}$$

$$Then: \\ \underline{A+B} = \overline{C} \\ \overline{A \bullet B} = C$$

$$B \longrightarrow C$$





Two-NOR (8522)

SPECIFICATIONS

PART NUMBER	8522
OUTPUT CHARACTERISTICS	Propagation DelayAverage14 ns Maximum23 ns
	Turn-on Time
	Turn-off Time
INPUT REQUIREMENTS	Rise Time—Maximum AllowableNot Applicable Voltage Levels $ m "1"=1.3V \stackrel{+}{-} 2.3V$
	"0" = $0V \pm 0.6V$
LOAD CHARACTERISTICS	Inputs Appear As
MODULES PER CARD	4
CIRCUITS PER CARD	8
TEMPERATURE RANGE	15° to 55° C.
POWER REQUIREMENTS	3.6V ±10% Inputs HighTypical182 mw Maximum260 mw
	Inputs Low
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD. GRD.
	Din No. 1 20 2 28

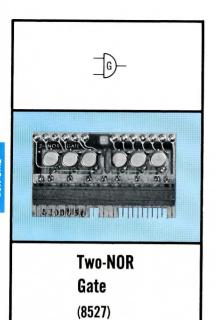
CIRCUIT CONFIGURATION

TYPICAL RESISTOR VALUES R₁ = 450 OHMS R₂ = 640 OHMS

LOGIC SYMBOL

SIGNAL CONNECTIONS

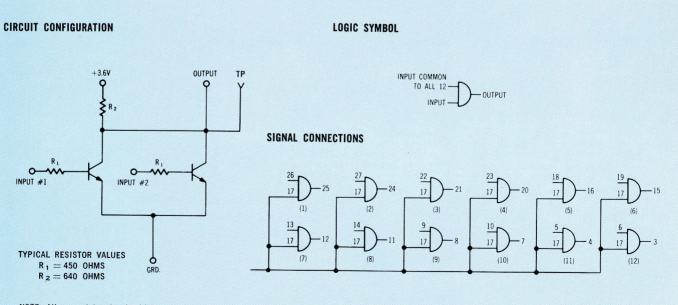
NOTE: All unused inputs should be wired to ground.



The Micrologic Two-NOR gate card provides twelve 2-input AND gates. One Input of each AND gate is tied to a common point and is available for use as a query (strobe) input to the 12 gates. The 2-NOR gate card can be used in any application where a common strobe is needed for up to 12 AND gates. Each 2-NOR circuit in the network may be paralleled with expander circuits to increase the number of inputs per gate. The input-output relationships are the same as those for the standard NOR circuits.

SPECIFICATIONS

PART NUMBER	8527
OUTPUT CHARACTERISTICS	Propagation DelayAverage14 ns
	Maximum23 ns
	Turn-on TimeAverage
	Maximum18 ns Turn-off TimeAverage15 ns
	Maximum28 ns
INPUT REQUIREMENTS	Rise Time—Maximum Allowable
LOAD CHARACTERISTICS	Inputs Appear As
	Output Capable of Driving5 Loads
MODULES PER CARD	6
CIRCUITS PER CARD	12
TEMPERATURE RANGE	15° to 55° C.
POWER REQUIREMENTS	$3.6V \pm 10\%$
	Inputs High
	Inputs LowTypical 72 mw Maximum
POWER CONNECTIONS	Voltage <u>+3.6V +3.6V GRD. GRD.</u>
	Pin Nc 1 29 2 28



The Micrologic Three-Input NOR circuit is a decision element which can perform all the functions required for any logical operation. Functionally the circuit is the same as the Two-NOR except for the additional input. It can be used for AND gates, OR gates, inverters, and DC controlled latches. It may also be used with expander circuits to provide multi-input gates. The Truth Table below shows the response of the output (D) to the conditions of the inputs (A, B, and C).

TRUTH TABLE

Α	В	С	D
0	0	0	1
AII Cor	Othe nbina		0

Where:	
+V = logical	"1"
0V = logical	"0"

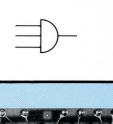
Then: $A + B + C = \overline{D}$ $\overline{A} \cdot \overline{B} \cdot \overline{C} = D$



SPECIFICATIONS

CIRCUIT CONFIGURATION

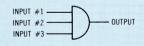
PART NUMBER	8504
OUTPUT CHARACTERISTICS	Propagation DelayAverage14 ns
	Maximum23 ns
	Turn-on TimeAverage13 ns
	Maximum18 ns
	Turn-off TimeAverage15 ns
	Maximum28 ns
INPUT REQUIREMENTS	Rise Time—Maximum AllowableNot Applicable
	Voltage Levels
	"0" = $0V \pm 0.6V$
LOAD CHARACTERISTICS	Inputs Appear As1 Load Per Input
	Output Capable of Driving5 Loads
MODULES PER CARD	3
CIRCUITS PER CARD	6
TEMPERATURE RANGE	15° to 55° C.
POWER REQUIREMENTS	3.6V ±10%
	Inputs HighTypical137 mw
	Maximum195 mw
	Inputs LowTypical
	Maximum 65 mw
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD. GRD.
No.	
	Pin No 1 29 2 28



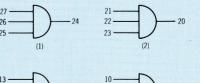


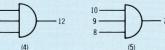
Three-NOR (8504)

LOGIC SYMBOL



SIGNAL CONNECTIONS







7. COS 1.

NOTE: All unused inputs should be wired to ground.

TYPICAL RESISTOR VALUES R $_1=450~\mathrm{OHMS}$ R $_2=640~\mathrm{OHMS}$

О ОПТРИТ



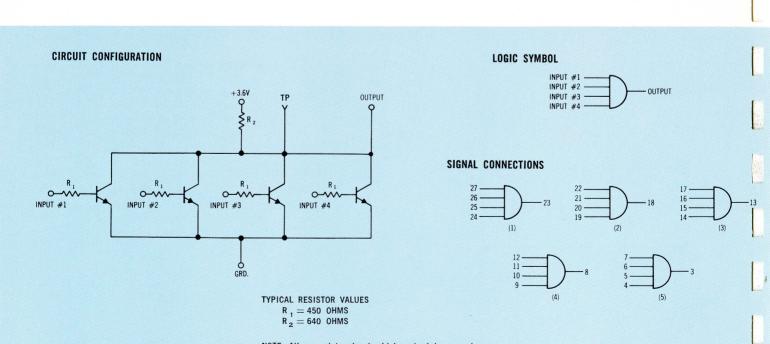
The Micrologic Four-Input NOR circuit is a decision element which can perform all the functions required for any logical operation. Functionally the circuit is the same as the Two-NOR and Three-NOR circuits except it has four inputs. It can be used for AND gates, OR gates, inverters, and DC controlled latches. The Four-Input NOR can also be used with three- or four-input expander circuits to provide larger configurations for AND or OR gating applications. The Truth Table below shows the response of the output (E) to the conditions of the inputs (A, B, C, and D).

+V = logical "1" 0V = logical "0" Then: $A+B+C+D = \overline{E}$ $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} = E$

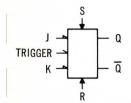


SPECIFICATIONS

PART NUMBER	8526
OUTPUT CHARACTERISTICS	Propagation DelayAverage14 ns
	Maximum23 ns
	Turn-on Time
	Maximum18 ns
	Turn-off Time
	Maximum28 ns
INPUT REQUIREMENTS	Rise Time—Maximum Allowable
	Voltage Levels"1" = 1.3V + 2.3V - 0.5V
	"0" = $0V \pm 0.6V$
LOAD CHARACTERISTICS	Inputs Appear As Load Per Input
	Output Capable of Driving
MODULES PER CARD	5
CIRCUITS PER CARD	5
TEMPERATURE RANGE	15° to 55° C.
POWER REQUIREMENTS	3.6V ±10%
	Inputs High114 mw
	Maximum162 mw
	Inputs Low
	Maximum 54 mw
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD GRD
TOTAL DOMELOTION	73.0V T3.0V GRD GRD
	Pin No 1 29 2 28



The Micrologic JK Flip-Flop is a storage element used in counters, shift registers, pulse shapers, sequencers, sequence control networks, and other networks requiring storage of an event after the information signal has expired. Simultaneous "0" steering inputs cause the output to toggle when the input is triggered. The trigger input responds to a negative-going edge thus enabling the circuit to count and to be used in other timing applications. The input-output relationships of the circuit are shown below.

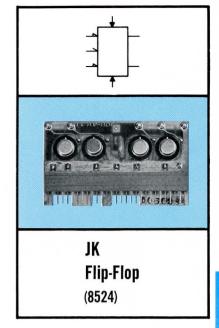


J	K	Q _{T+1}
1	1	Q
1	0	1
0	1	0
0	0	Q

S	R	Q	Q
0	1	0	1
1	0	1	0
1	1	1	1

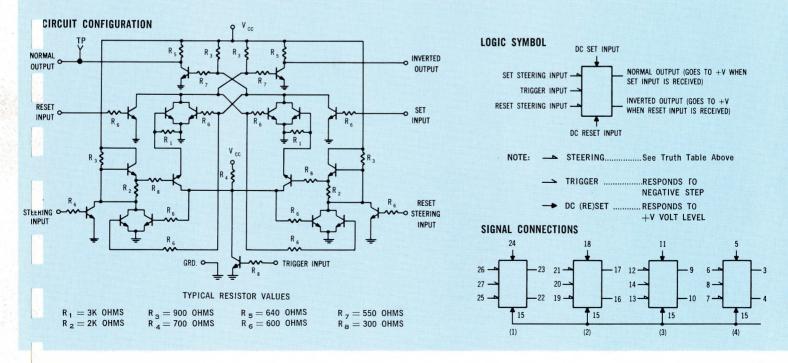
Where: logical "1" = +V logical "0" = 0V

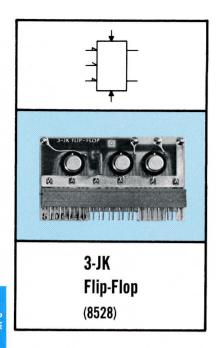
and Q_{T+1} is the status of the output one trigger pulse after the JK steering has been set up.



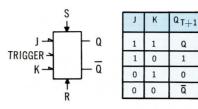
SPECIFICATIONS

PART NUMBER 8524 **OUTPUT CHARACTERISTICS** Propagation DelayAverage Maximum60 ns Average Maximum Turn-off TimeAverage Maximum INPUT REQUIREMENTS Maximum AC Clock Pulse Transition (neg) "0" = $0V \pm 0.6V$ Steering InputSet Up Time20 ns Release TimeSimultaneous with clock pulse LOAD CHARACTERISTICS Inputs Appear AsTrigger2 Loads Steering1 Load Reset1 Load Output Capable of Driving MODULES PER CARD CIRCUITS PER CARD TEMPERATURE RANGE 15° to 55° C. $3.6V \pm 10\%$ POWER REQUIREMENTS Typical POWER CONNECTIONS+3.6V +3.6V





The Micrologic 3-JK Flip-Flop is a storage element used in counters, shift registers, pulse shapers, sequencers, sequence control networks, and other networks requiring storage of an event after the information signal has expired. Simultaneous "0" steering inputs cause the output of the circuit to toggle when the input is triggered. The trigger input responds to a negative-going edge thus enabling the circuit to count and to be used in other timing applications. In the 3-JK Flip-Flop circuit, both set and reset DC inputs are made available individually. The input-output relationships of the circuit are shown below



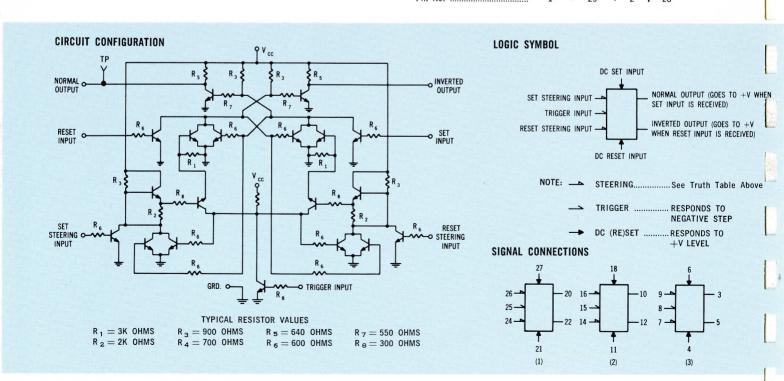
S	R	Q	ā
0	1	0	1
1	0	1	0
1	1	1	1

Where: logical "1" = +V logical "0" = 0V

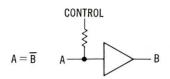
and Q_{T+1} is the status of the output one trigger pulse after the JK steering has been set up.

SPECIFICATIONS

PART NUMBER	8528				
OUTPUT CHARACTERISTICS	Propagation DelayAverage40 ns				
	Maximum60 ns				
	Turn-on TimeAverage40 ns				
	Maximum60 ns				
	Turn-off TimeAverage40 ns				
<u>.</u> ₩.	Maximum60 ns				
INPUT REQUIREMENTS	Maximum AC Clock Pulse				
	Transition (neg)200 ns				
	Voltage Levels"1" = 1.3V $\stackrel{+}{-}$ 2.3V $\stackrel{-}{-}$ 0.5V				
	"0" = $0V \pm 0.6V$				
	Steering InputSet Up Time20 ns				
	Release TimeSimultaneous with clock pu				
LOAD CHARACTERISTICS	Inputs Appear AsTrigger2 Loads				
	Steering1 Load				
	Reset 1 Load				
	Output Capable of Driving5 Loads				
MODULES PER CARD	3				
CIRCUITS PER CARD	3				
TEMPERATURE RANGE	15° to 55° C.				
POWER REQUIREMENTS	+3.6V ±10%				
	Typical				
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD. GRD.				
	Div No.				
	Pin No 1 29 2 28				

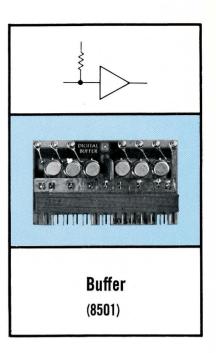


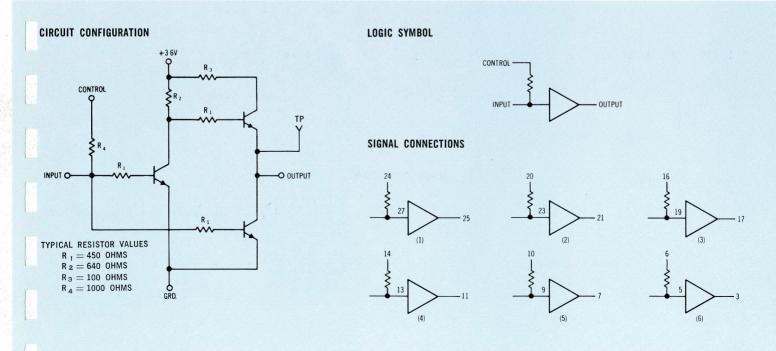
The Micrologic Buffer is a low impedance driver circuit. The buffer is used when the number of loads to be driven exceeds the number the source is capable of driving. It can also be used to minimize rise time deterioration due to capacitive loading in applications where the signal distribution is extensive. The circuit performs a logical inversion of the signal. The relation of the output to the input is shown below.

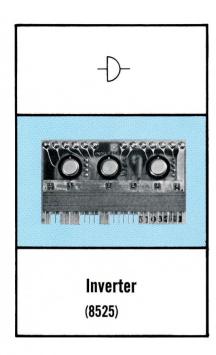


SPECIFICATIONS

	PART NUMBER	8501
	OUTPUT CHARACTERISTICS	Propagation DelayAverage
		Turn-on Time
in the		Turn-off Time
	INPUT REQUIREMENTS	Rise Time—Maximum Allowable
		$^{\prime\prime}0^{\prime\prime}=0$ V $\pm~0.6$ V
	LOAD CHARACTERISTICS	Inputs Appear As
	MODULES PER CARD	6
	CIRCUITS PER CARD	6
	TEMPERATURE RANGE	15° to 55° C.
	POWER REQUIREMENTS	3.6V ±10%
		Input HighTypical
		Input Low325 mw
	2"	Maximum375 mw
	POWER CONNECTIONS	Voltage <u>+3.6V +3.6V GRD. GRD.</u>
		Pin No 1 29 2 28





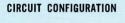


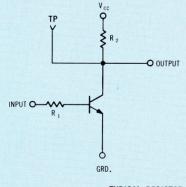
The Micrologic Inverter is a single input NOR primarily used for signal inversion. However, it can be used in other special applications—for example: Expanded Gates (used with expander circuits). The inverting action of this circuit is shown in the logical expression:

$$A = \overline{B}$$
 Where: $A - D - B$ $+V = logical "1" OV = logical "0"$

SPECIFICATIONS

PART NUMBER	8525
OUTPUT CHARACTERISTICS	Propagation DelayAverage14 ns
	Maximum 23 ns Turn-on Time Average 13 ns Maximum 18 ns
	Turn-off Time
INPUT REQUIREMENTS	Rise Time—Maximum Allowable
LOAD CHARACTERISTICS	Input Appears As
MODULES PER CARD	3
CIRCUITS PER CARD	12
TEMPERATURE RANGE	15° to 55° C.
POWER REQUIREMENTS	3.6V ± 10% Inputs High 275 mw Maximum 390 mw Inputs Low Typical 72 mw Maximum 130 mw
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD. GRD.
	Pin No 1 29 2 28



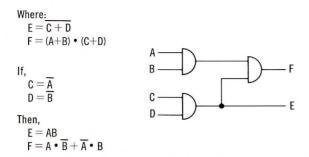


TYPICAL RESISTOR VALUES $\begin{array}{c} {\rm R}_{1} = 450 \ {\rm OHMS} \\ {\rm R}_{-} = 640 \ {\rm OHMS} \end{array}$

LOGIC SYMBOL

SIGNAL CONNECTIONS

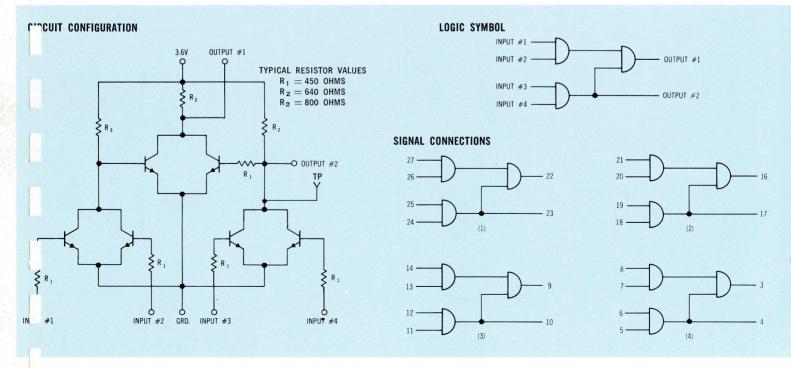
The Micrologic Half-Adder is a multipurpose combination of three 2-NOR circuits. The configuration can be used as a half-adder, an exclusive-OR gate, or any similar logic application. One output is a noninverting function of the four inputs. The second output may be considered as the output of one of the input Two-NORS. This is shown below with the logic relationships of the inputs to the outputs.

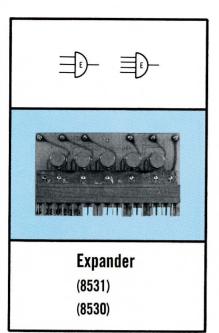


Half-Adder (8523)

SPECIFICATIONS

OI LUII IUNI IUNO		
	Output F	Output E
PART NUMBER	8523 (Exclusive OR)	(AND)
OUTPUT CHARACTERISTICS	Propagation DelayAverage28 ns	14 ns
	Maximum46 ns	23 ns
	Turn-on TimeAverage28 ns	13 ns
	Maximum46 ns	18 ns
	Turn-off TimeAverage28 ns	15 ns
	Maximum46 ns	28 ns
INPUT REQUIREMENTS	Rise Time—Maximum AllowableNot Applicable	
	Voltage Levels" "1" $= 1.3$ V $\stackrel{+}{-} 2.3$ V $\stackrel{-}{-} 0.5$ V	
	-0.5 V $^{\circ}$ '' = 0V ± 0.6 V	
	0 _ 0V <u> </u>	
LOAD CHARACTERISTICS	Inputs Appear As1 Load Per Input	
	Output Capable of DrivingOutput F5 Loads	
	Output E4 Loads	
MODULES PER CARD	4	
CIRCUITS PER CARD	4	
TEMPERATURE RANGE	15° to 55° C.	
POWER REQUIREMENTS	3.6V ±10%	
	Typical	
	Maximum255 mw	
POWER CONNECTIONS	Voltage +3.6V +3.6V GRD. GRD.	
	Pin No 1 29 2 28	





Micrologic Expander ciruits enable the use of multi-input (five or more) AND, OR gates without the necessity of adding inverters and several stages of gating. Logically, they are the same as their 3- and 4-NOR counterparts. They differ physically only in the power supplied to them. The collector input to the NOR circuit is connected to ± 3.6 volts. However, when the card is used as an expander, the collector voltage input is left open.

SPECIFICATIONS

PART NUMBER

3-NOR EXPANDER

8531

4-NOR EXPANDER

8530

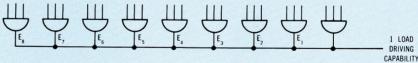
CHARACTERISTICS

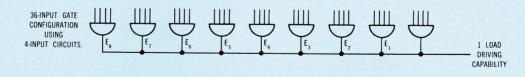
The specifications for these circuits are the same as for the standard 3- and 4-NOR circuits except the Expander circuits do not require any power.

Each Expander circuit appears as $\frac{1}{2}$ load to a standard NOR circuit and reduces the driving capability of the NOR accordingly. Since the standard NOR circuit is capable of driving five loads, the maximum number of Expanders that can be used with one NOR is eight and still drive one load. This, for example, allows construction of a 27-input OR gate capable of driving one load if one 3-input NOR and eight 3-input Expanders are used (illustrated below). A 4-input NOR expanded by eight 4-input Expanders will result in a 36-input gate (maximum) capable of driving one load (as illustrated below). Any combination of 3- and 4-input Expanders may be used as long as these loading rules are followed.

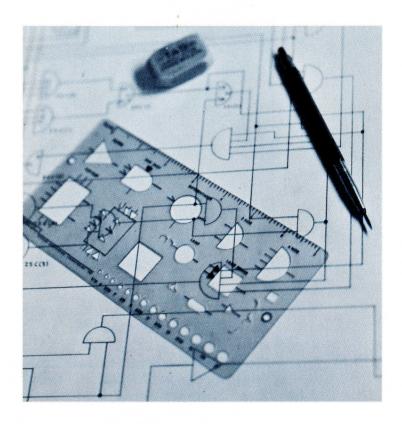
CIRCUIT CONFIGURATION

27-INPUT GATE CONFIGURATION HSING 3-INPUT CIRCUITS.



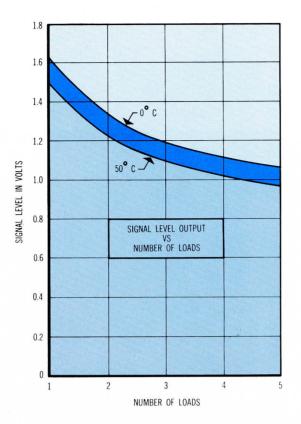


COMBINATION 3 AND 4-INPUT CIRCUITS SHOWING 31 INPUTS. 1 LOAD CAPABILITY



Systems using SEL micrologic modules can be designed with a minimum number of rules. Logic levels of 0 volts and \pm Vc are used with threshold of switching as low as 1 volt. The only consideration to circuit interconnections is the output driving capabilities of each circuit. The capabilities of the circuits are sufficient in most cases to perform logic without the use of buffer circuits. However, the digital buffer can be used where additional driving potential is required. In cases where the driving capability must be increased, the buffer circuit is serially connected into the signal line.

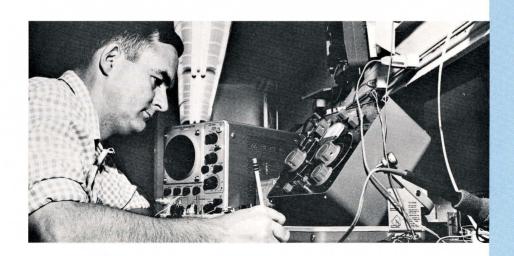
The SEL micrologic circuits presently operate up to speeds in excess of 5 megacycles. When high speed operating rates up in the RF region are used, it should be remembered that RF assembly techniques are applicable.

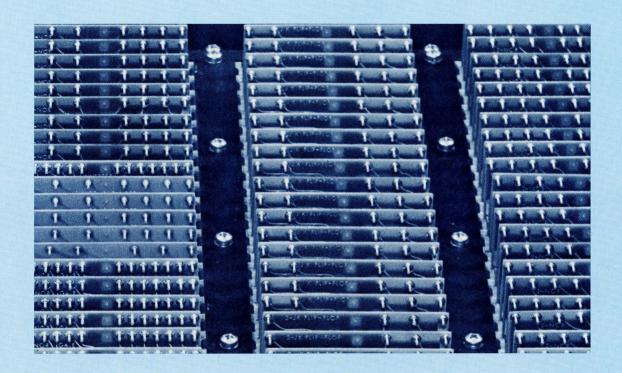


LOADING EFFECTS ON OUTPUT VOLTAGE

It is good practice to keep the length of interconnecting cables to a minimum. Grounding, shielding, lead inductance, etc. become increasingly severe problems as switching rates are increased.

The effects of loading must also be considered. The output voltage of the micrologic element is dependent on the number of driver loads added. As circuits are added, the output voltage decreases. The graph shows the effects of loading on the output voltage.





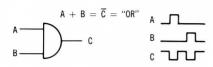
This section of the manual shows the wide application of SEL micrologic circuits. Their use as counters, registers, matrices, etc., and the performance of many different logic functions are diagrammed. SEL circuit applications are by no means limited to those shown on the following pages. Rather, we have prepared diagrams of what we feel are the most commonly required logic functions. The logic functions can be performed in ways other than as shown; however, the diagrams illustrate the circuit configurations which we have found yield the maximum efficiency, reliability and dollar savings.

NOR CIRCUIT APPLICATIONS

AND GATE



OR GATE

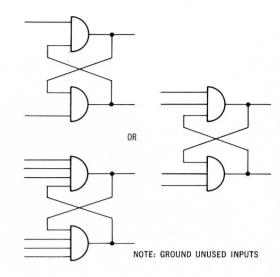


NOR TRUTH TABLE				
Α	В	С		
1	1	0		
1	0	0		
0	1	0		
0	0	1		

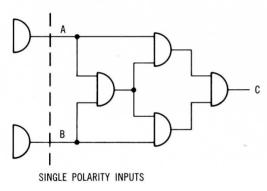
WHERE:

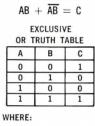
$$\begin{array}{c} +V = 1 \\ 0V = 0 \end{array}$$

NOR LATCH

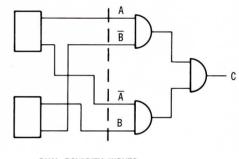


EXCLUSIVE OR



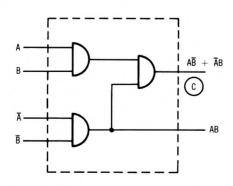


 $egin{array}{l} + V &= 1 \\ 0 V &= 0 \end{array}$



DUAL POLARITY INPUTS

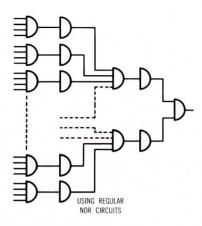
HALF ADDER



TR	UTH TAI	BLE
· A	В	С
0	0	0
0	1	1
1	0	1
1	1	0

NOR CIRCUIT APPLICATIONS (CONT'D)

GATE WITH MORE THAN 4 INPUTS

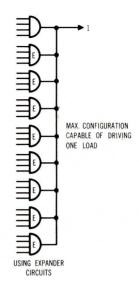


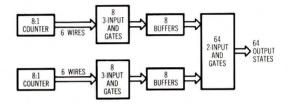
LARGE BANKS OF "AND" GATES - (MATRIX)

To derive all states of large counters without overly large individual AND gates and with a resultant savings in circuits used:

- (1) First divide into sub-counters.
- (2) Then matrix out each state of each counter and combine.

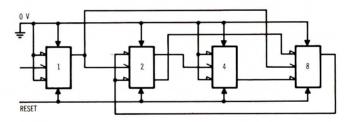
Example: A 64:1 counter using 64 six-input AND gates would require 64 3-NORS, 64 3-NOR expanders and 12 buffers (24 cards). If they are combined as shown only 64 two-input NORS, 16 3-input NORS, and 16 buffers would be required; for a total of only 14 cards, on which some spares would be available.





SPECIAL COUNTERS

BCD COUNTING 10:1 COUNTER



WAVEFORMS OF A BCD COUNTER

CYCLE 1 — CYCLE 2

0 1 2 3 4 5 6 7 8 9 0

2" (1)

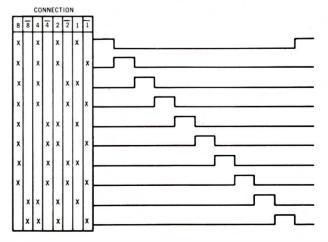
2" (2)

2' (2)

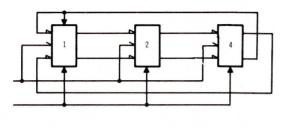
2' (4)

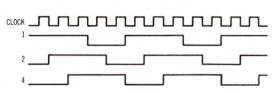
2* (8)

CONNECTION TO COUNTER AS SHOWN PROVIDES
OUTPUTS LIKE THESE BELOW (USING 4-NOR AND GATES)

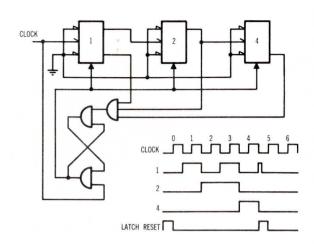


5:1 COUNTER

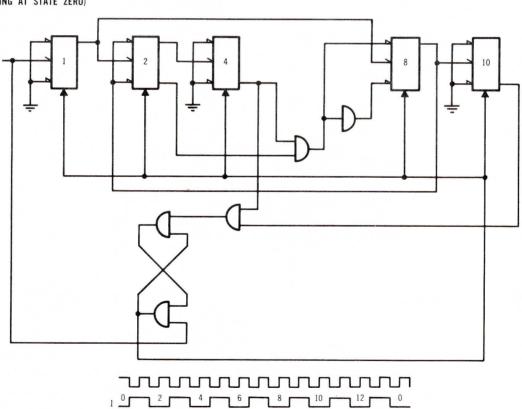




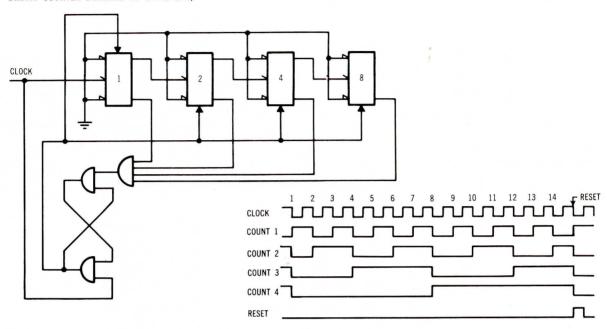
5:1 FORCED RESET COUNTER



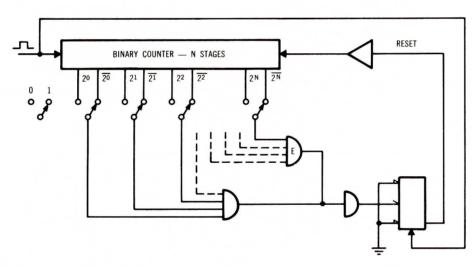
N:1 COUNTER BCD (EXAMPLE: 14-1 BCD COUNTER STARTING AT STATE ZERO)



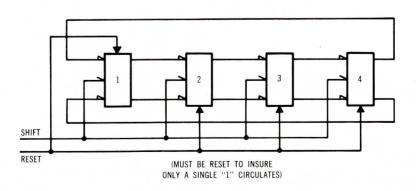
N:1 COUNTER—BINARY (EXAMPLE: 14-1 BINARY COUNTER STARTING AT STATE ONE)

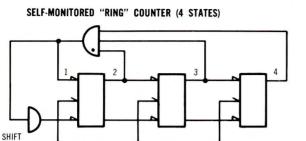


SELECTABLE COUNTDOWN COUNTER - BINARY

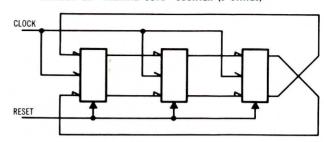


RING COUNTER

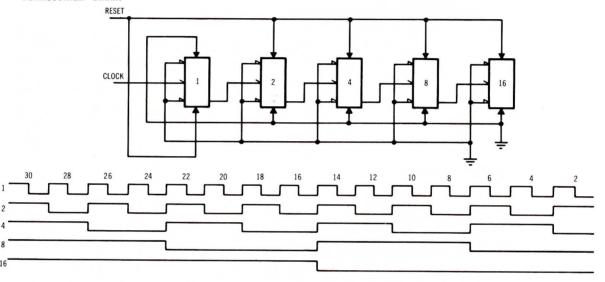




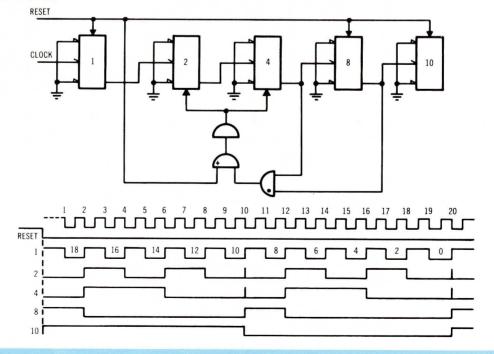
JOHNSON OR "WALKING CODE" COUNTER (6 STATES)



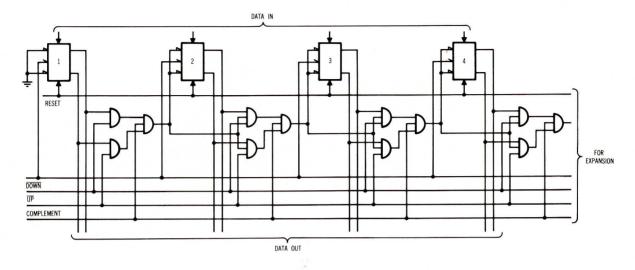




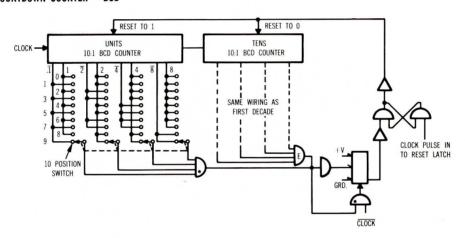
20:1 DOWNCOUNTER-BCD



UPCOUNTER, DOWNCOUNTER AND COMPLEMENT REGISTER

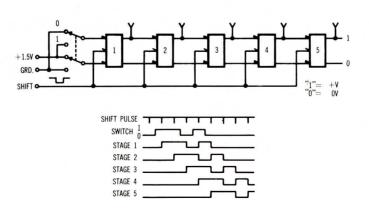


SELECTABLE COUNTDOWN COUNTER - BCD



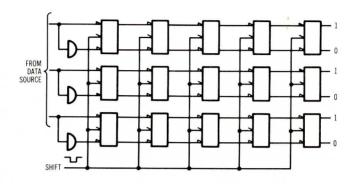
SHIFT REGISTERS

SERIAL SHIFT REGISTER

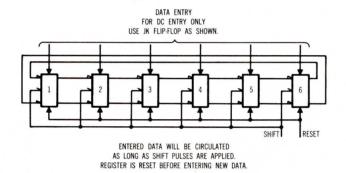


SHIFT REGISTERS (CONT'D)

PARALLEL SHIFT REGISTER (3 X 5) (A Multiple Stage Serial Shift Register)

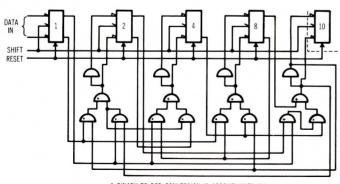


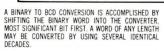
END CONNECTED (CIRCULATING) SHIFT REGISTER

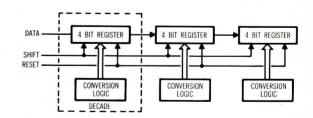


CONVERTERS

BINARY TO BCD CONVERTER (BIDEC)

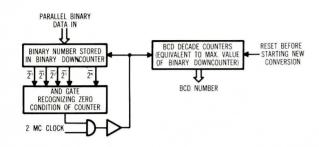




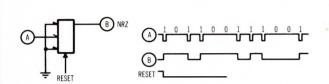


CONVERTERS (CONT'D)

BINARY TO BCD CONVERTER - COUNTING TYPE



PULSE TO NRZ CONVERTER



BCD TO BINARY CONVERTER - COUNTING TYPE

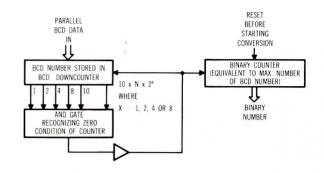
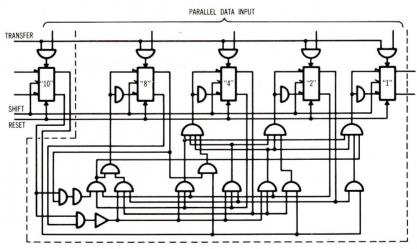


TABLE OF REQUIRED CONVERSION TIMES

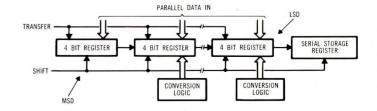
MAXIMUM	MAX. CONVERSION TIME			
BINARY NO.	1 MC CLOCK	2.5 MC CLOCK		
256	256 US	102.3 US		
512	512 US	205 US		
1024	1.024 MS	410 US		
2048	2.048 MS	820 US		
4096	4.096 MS	1.635 MS		
8192	8.192 MS	3.278 MS		

This circuit is used primarily for converting standard pulse coded data into the NRZ data form required for most computer input magnetic tape.

BCD TO BINARY CONVERTER (DECBI)



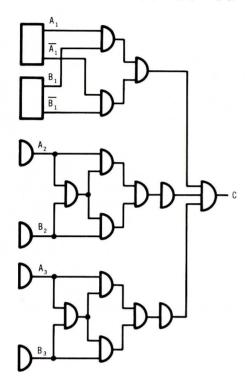
The BCD to binary conversion is accomplished by transfering the parallel BCD word into the converter, and shifting it out least significant bit first.



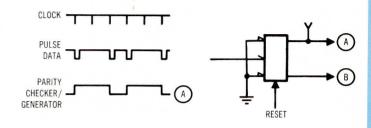
COMPARATORS

PARALLEL COMPARATOR

$$(A_1B_1 + \overline{A}_1\overline{B}_1) \cdot (A_2B_2 + \overline{A}_2\overline{B}_2) \cdot (A_3B_3 + \overline{A}_3\overline{B}_3) = C$$



SERIAL PARITY CHECKER/GENERATOR — PULSE DATA



NOTE:

IF + V LEVEL IS TAKEN AS AN IN-DICATION OF CORRECT PARITY FOR PARITY CHECKER OR "1" FOR PAR-ITY GENERATOR.

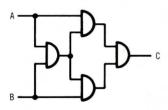
THEN: (A) IN EXAMPLE INDICATES:

- 1. PARITY ERROR FOR ODD PARITY CHECKER
- 2. CÓRRECT PARITY FOR EVEN PARITY CHECKER
- 3. PARITY BIT "O" FOR ODD PAR-
- ITY GENERATOR

 4. PARITY BIT "1" FOR EVEN PARITY GENERATOR

AND (B) IS THE INVERSE OF ABOVE.

SERIAL COMPARATOR

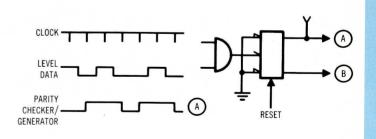


$$AB + \overline{AB} = C \text{ (EXCLUSIVE OR)}$$

$$A \longrightarrow B$$

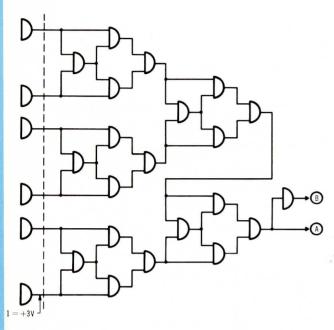
$$C \longrightarrow C$$

SERIAL PARITY CHECKER/GENERATOR — LEVEL DATA



SEE "SERIAL PARITY CHECKER/GENERATOR-PULSE DATA" FOR INTERPRETATION OF OUTPUTS () AND () $\$

PARALLEL PARITY CHECKER/GENERATOR



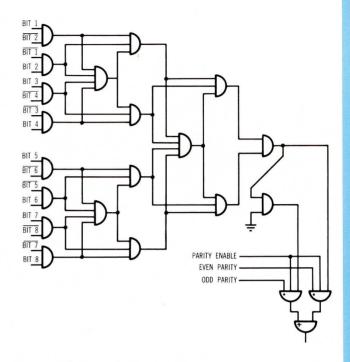
NOTE: IF + VOLT LEVEL IS TAKEN AS AN INDICATION OF CORRECT PARITY FOR PARITY CHECKER OR "1" FOR PARITY GENERATOR,

THEN: \bigoplus_{EVEN} is output to use for odd parity generator or even parity checker.

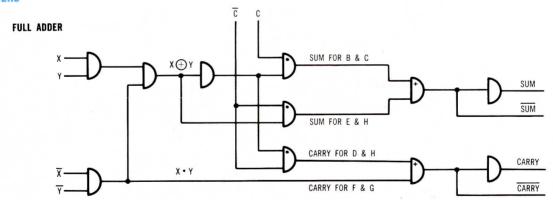
AND

 $\begin{picture}(60,0)\put(0,0){\line(0,0){10}}\put(0,0){\line(0,0){10}$

PARALLEL PARITY CHECKER



ADDERS



WHERE "1" = X

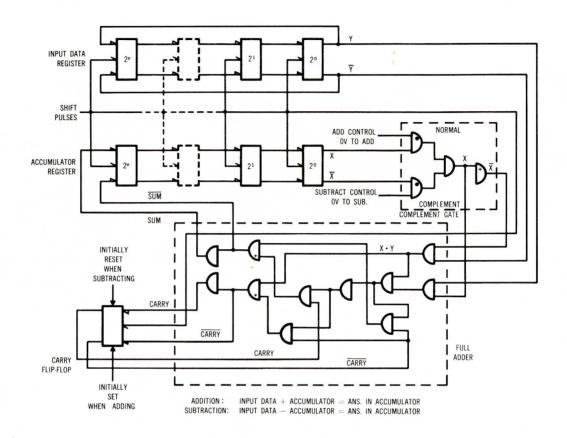
AND

$$\frac{x}{x} = +v$$

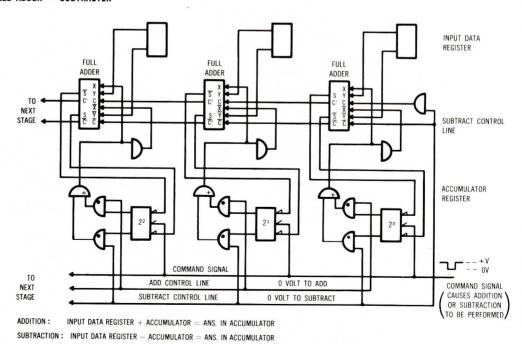
	х	Y	PREVIOUS CARRY	SUM	NEW CARRY
Α	0	0	0	0	0
В	1	0	0	1	0
С	0	1	0	1	0
D	1	1	0	0	1
D E	0	0	1	1	0
F	1	0	1	0	1
G	0	1	1	0	1
Н	1	1	1	1	1

ADDERS (CONT'D)

SERIAL ADDER - SUBTRACTER USING 2's COMPLEMENT



PARALLEL ADDER — SUBTRACTER

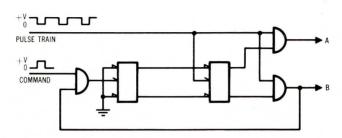


30

ANTI-COINCIDENCE LOGIC

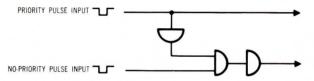
THE IDEAL ANTI-COINCIDENCE CIRCUIT CAN ONLY BE DETERMINED AFTER CONSIDERING THE EXACT SITUATION FOR WHICH IT IS REQUIRED. LISTED BELOW ARE THREE TYPICAL APPLICATIONS.

"PULSE PICKING"

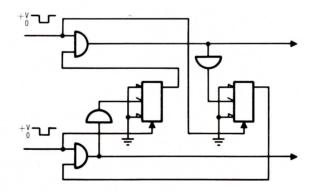


A WHOLE PULSE IS ELIMINATED FROM A PULSE TRAIN AT OUTPUT "A" WHEN THE COMMAND IS RECEIVED. IT WILL BE THE FIRST OR SECOND PULSE OF THE TRAIN AFTER THE COMMAND PULSE, DEPENDING ON WHEN THE COMMAND OCCURS RELATIVE TO THE PULSES OF THE TRAIN. THE SAME IS TRUE FOR OUTPUT "B" EXCEPT THE PULSE ELIMINATED FROM OUTPUT "A" WILL APPEAR AT OUTPUT "B".

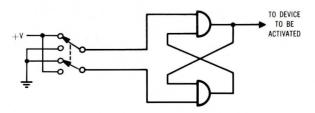
ASSIGNING PRIORITY TO ONE OF TWO PULSES

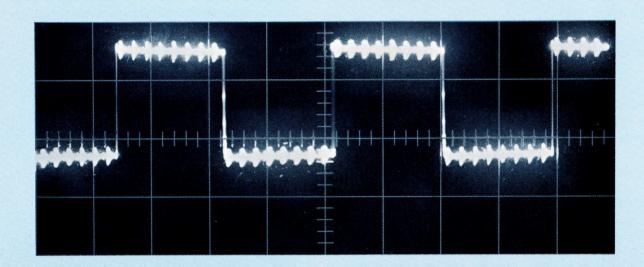


FIRST PULSE IN TO HAVE PRIORITY



PREVENTING SWITCH CONTACT SCRATCH (BOUNCE)





A significant percentage of logic system problems have been caused by some form of digital "noise." They require a good deal of time for correction due to their intermittent nature. The following discussion describes the techniques which will greatly reduce the probability of similar problems in your logic system.

DIGITAL GROUND SYSTEM

Most noise problems are a result of differences in potential between the various digital "grounds" within the system. These potential differences are generally in the form of "spikes" or "grass" and are the results of pulse current flowing in the ground structure. The logic system designer should observe the following rules to minimize noise problems.

All logic trays should have a 1-inch braid as the digital ground connection from the tray ground bus to the system digital ground bus.

The system digital ground bus should have a minimum crosssection equivalent to 1-inch braid. In most cases, a larger copper bar is mechanically most convenient. The ground terminals of the digital power supplies are considered as the origination of the bus. Every effort should be made to minimize the number of inter-tray logic connections required. These connections are the source of most of the high frequency current that flows in the ground structure.

System layout should be planned to make the digital ground system as compact as possible. Those trays which represent the largest loads should be placed closest to the power supply, if feasible. The ground braids from the trays should be connected together at the closest point. It is not advisable to run separate ground lines all the way to the power supplies from every tray.

Care should be taken to see that current returns from large pulse signals (such as that required to drive a long string of shift registers) do not flow in the main ground system. This is especially important when signals are being routed through cable retractors.

Equipment, such as tape transports, that have chassis and signal ground (or shield ground) in common requires some special attention. The head cable shields and the start-stop command are returned to chassis. It may be most convenient to lift these chassis connections, but it is also possible to eliminate most problems and retain the chassis grounds.

DC POWER DISTRIBUTION

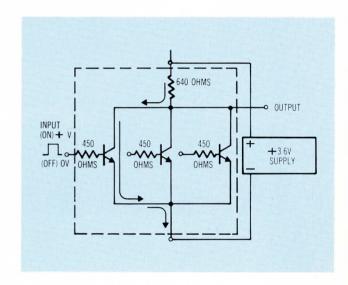
If the preceding rules on grounding are followed, power distribution problems are minimized. The following rules should also be observed for power distribution.

Power distribution to trays should be guided by the amount of current required by that tray. As a general rule of thumb, at least one #16 wire should be used for each 4 amperes drawn by the circuitry in the tray. If more than one #16 wire is required for the load the wires should be wired in parallel or a single equivalent wire used in their place.

DC POWER CONNECTIONS

A power supply source of +3.6 volts is required by all cir-

cuits except the expander circuits. The diagram shows a typical NOR circuit and illustrates the current flow. As shown in the illustration, a +3.6 volt source will meet all needs. An arrow shows the direction of conventional current flow.



AC POWER DISTRIBUTION

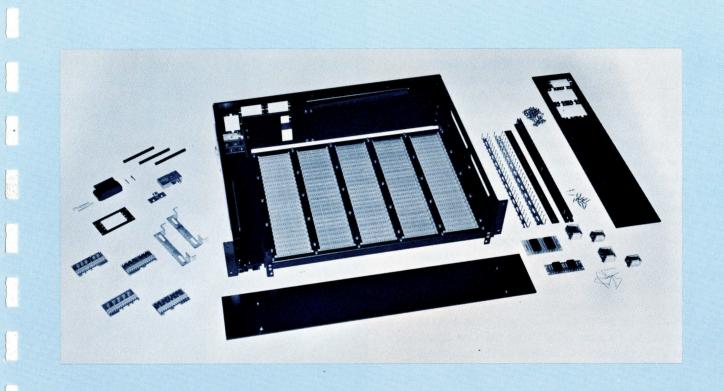
Many systems are operated from power lines that are extremely noisy. The following rules will reduce the associated problems.

Line filters should be installed on all systems. The Sprague Filterol series of filters has proven to be effective in reducing the noise problems created by noise in the power line. The cases of the filters should be insulated from ground and a separate return to "dirty earth" provided.

The AC power lines throughout the system should be routed so as to avoid coupling to either the ground system or the logic wiring.

AC neutral should not be connected to ground anywhere in the system.

SEL INTEGRATED LOGIC MODULAR PANEL, TRAYS AND PACKAGING ACCESSORIES



SEL offers three standard packaging modules for the integrated logic cards: a horizontally mounted tray, which contains four 25-card rows, a five-row vertically mounted tray (125 cards) and a hinged modular panel which is composed of as many 25-card mounting rows as may be required to a maximum of 15 rows. The trays and the modular panel each offer distinct advantages, depending upon your packaging requirements.

The trays are designed for housing functional logic systems which are independent within the tray.

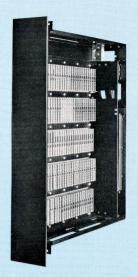
The modular panel is designed for fabrication of systems which require many functional assemblies that communicate with integrated circuit logic interfaces. The modular panel provides maximum convenience and maintenance. It provides optimum wiring configuration where circuit operating speeds make point-to-point wiring mandatory.

SEL standard logic trays include all the latest innovations in circuit-card packaging. Included are many exclusive features such as built-in power buses, a hinged cable retractor and insulated wire ducts. The trays are equipped with an integral chassis which mounts in a standard 19-inch equipment rack. The trays can be extended from the equipment rack with power applied, and when extended, all circuit test points, adjustments and circuit card pin connections are readily accessible. Each circuit card is mounted in an individual connector, and each connector can be easily keyed to a particular type of card. No supporting hardware is required to retain the cards in the connectors. The cable retractor is a hinged metal sleeve which encases all the wires between the slide-out mounting chassis. The insulated wire ducts in the trays are extruded vinyl channels with snap-on covers. They encase the wires between the individual rows of card connectors on the bottom of the tray. All wire connections to the card connectors are accomplished using the clean solderless "wire wrap" technique. All legends on SEL logic trays are silk screened.

MODULAR PANEL

The SEL modular panel for integrated logic cards is designed for hinge-mounting in standard 19-inch equipment cabinets. Frames can be mounted on both front and rear of your cabinet, and, if required, can fill the full height of the cabinet. Thus, an extremely high packing density can be achieved. A total of 750 logic cards can be accompodated in this configuration. The hinge mounting facilitates access to the wiring on the rear of the frame. When in the stored position, cabinet doors conceal the panel, thus protecting the logic cards as well as enhancing the appearance of the system.

The panel can contain from one to 15 horizontal rows of cards, as required. Each row mounts 25 cards. The simplified mechanical design of the frame makes modification extremely simple. The packaging accessories described on the following pages pertain to panel construction as well as trays, with exception of the paragraphs on tray panels and connectors.



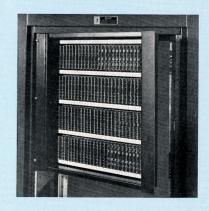
5-ROW VERTICAL TRAY



4-ROW HORIZONTAL TRAY



MODULAR PANEL



LIDE-OUT OPERATION

A closed tray is extended by momentarily applying light finger pressure on the face of the front panel. The pressure compresses a spring located in the cable retractor and releases a latch. When the pressure is removed, the spring eases the tray forward on the ball bearing slides. When the tray is fully extended, locks located on the slides engage autonatically. An extended tray is closed by manually releasing the slide locks.

TRAY PANELS

Front panels are made of quarter-inch aluminum with rounded front edges. These panels can be supplied unpainted or painted in accordance with your instructions. A chromate treat and zinc chromate primer are used to prepare the metal before paint is applied. Panels are mounted to the side members of the trays by threaded studs which are pressed into the rear face of the panel. No mounting hardware is visible from the front of the panel.

It should be mentioned, however, that when front panel mounted multi-wafer rotary switches are used, the amount of card space lost must be kept even in each row. For example, if a six-wafer rotary switch causes a three card setback in one card row, then three card spaces must be sacrificed in each of the remaining rows. Card setbacks cannot be staggered from row to row in the trays. This is necessary to preserve the lateral strength of the tray.

PANELS

Two basic styles of panels are available as follows:

5.25 in. by 19 in.

4-row horizontally mounted tray

4.75 in. by 28 in. 5-row vertically mounted tray

SPECIFICATIONS

4-ROW HORIZONTAL TRAY

Front Panel Width		19 Inches
Minimum Front Panel Height .		5.25 Inches
Cabinet Depth Required		25 Inches
Number of Rear Panel Connections		520 Maximum
Card Capacity		100 Maximum
Approximate Weight (Empty)		
Approximate Weight (Full)		30 Pounds

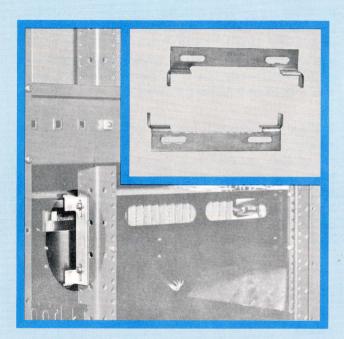
5-ROW VERTICAL TRAY

Minimum Front Panel Width		4.75 Inches
Front Panel Height	*	28 Inches
Cabinet Depth Required		25 Inches
Number of Rear Panel Connections		520 Maximum
Card Capacity	¥	125 Maximum
Approximate Weight (Empty)		34 Pounds
Approximate Weight (Full)	v.	42 Pounds

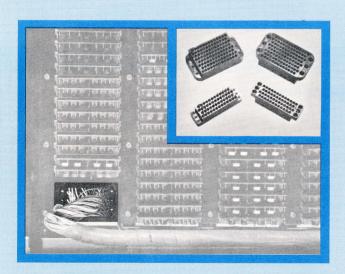
MODULAR PANEL

Width												18.25 Inches
Height .	•			÷								4 Inches Per Row
Cabinet Dep	oth	Requi	red									4 Inches
Number of	Card	l Row	S.									1 to 15
Number of	Car	ds Pe	r Ro	W								25
Approximate	e W	eight	of a	4	-Ro	W	Par	ıel	(En	npt	y)	13 Pounds
Approximate	e .W	eight	of a	4	-Ro	W	Pan	el	(Fu	II)		19 Pounds

NOTE: For mounting hardware and tray accessory part numbers, refer to the Parts List shown at end of this section.



TRAY HANGER (2 REQUIRED PER TRAY)



CONNECTOR MOUNTING PLATE

MOUNTING

The four-row horizontally mounted trays are supported in the equipment rack by two hangers near the rear of the chassi and four bolts located behind the front panel. The five-row vertically mounted card tray is supported by rigid cross members and four bolts behind the front panel.

All mounting hangers and cross members bolt directly to the mounting rails of the equipment rack. After the initial installation, any of the units can be removed from the rack be simply disconnecting the electrical connectors and removing the four mounting bolts behind the front panel. When the trays are in the stored position, all mounting hardware is concealed from view. All mounting hardware is supplied with the tray.

CONNECTORS

Separate Elco Varicon connectors are provided for each printed circuit card. This greatly increases the flexibility of the unit in that any number of connectors can be removed to provide room for mounting associated components. If components such as relays, patch panels, etc., are to be installed in place of the circuit card, flat mounting plates are easily installed in place of the connectors.

A quick-disconnect feature of SEL tray design allows from panels to be disconnected both mechanically and electrically in a matter of minutes. Either 50-pin or 104-pin connectors can be mounted in one of the card rows immediately behind the panel. All power to the panel is thus easily disconnected. The mounting plates for the 50-pin and 104-pin connectors bear SEL part numbers B0427 and B0429 respectively.

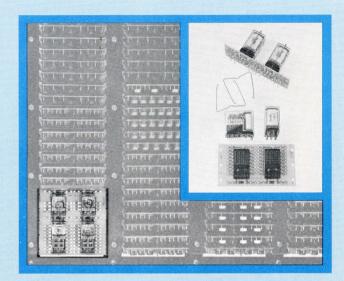
lighly reliable AMP quick-disconnect electrical connectors are used on the rear of the card trays. These connectors are of modular construction, accommodate many wire sizes, are asily keyed and use a reliable solderless crimp connection. Both 50- and 104-pin connectors are used, and different sizes may be used on the same tray. Both the 4-row horizontal tray not the 5-row vertical trays contain sufficient space for mounting up to five 104-pin connectors. Two types of pin contacts and contact receptacles are used in the connectors, ne which is used with #16-#18 wire and one which is used with #20 through #24 wire. These are packaged in kits of 10 pairs each. Contact crimping tools are required to crimp the ontacts to the wiring, and a pin extractor tool is used to emove the contacts from the connector blocks.

RELAY MOUNTING PLATES

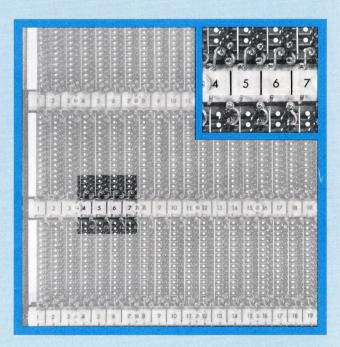
SEL relay mounting plates are available in two sizes. One accommodates two 2-pole Allied Control miniature relays. The larger plate can accommodate either two 4-pole Allied Control miniature relays, two 6-pole Allied Control miniature relays, or a combination of the two, depending on the relay sockets mounted on the plate.

POWER BUSES

Built-in power buses are provided on all SEL standard logic trays and modular panels. The power buses are located on the bottom of the tray and on the rear of the modular panels adjacent to each row of card connectors. Sufficient space is provided for six power buses along each row of card connectors.



RELAY MOUNTING PLATE



POWER BUSES

PARTS LIST FOR PACKAGING ACCESSORIES AND HARDWARE

NOMENCLATURE	SEL PART NO.	QTY/UNIT
Trays		
4-Row Horizontal	D12464	
5-Row Vertical	D12055	
Tray Hangers		
for 4-row horizontal tray	C0399-1A	2
for 5-row vertical tray	C0399-2A	2
for all other	specify dimensions and tray position in	
	cabinet	
Modular Panel (1 row)—	D12465-1	
Modular Panel (15 row)	D12465-15	
Front Panels		
$5.25^{\prime\prime}$ x $19^{\prime\prime}$ for 4-row horiz.	D12469	1
4.75" x 28" for 5-row vert.	D12470	1
Relay Mounting Plates		
for two 2-pole (2 Form C)		
miniature* relays	B12468-1	1
for two 4-pole		
miniature* relays	B12468-2	1
for two 6-pole	B12468-3	
miniature* relays for 4-pole, 6-pole	D12400-3	1
combination miniature* relays	B12468-4	1
Connector Mounting Plates	D104CC	
for 50-pin connector	B12466 B12467	
for 104-pin connector	D1240/	
Connector Housing		
for 50-pin	A10719	mated pair
for 104-pin	A10720	mated pair
Pin Contacts and Receptacles		
for #16-#18 wire	A10721	kits of 10 pair each
for #20-#24 wire	A10722	kits of 10 pair each
Special Tools		
Crimping tool	AMP #20	
	AMP #24	
Pin extractor	AMP #16-20, Type II	

^{*}Relays are Allied Control series TS-154-

OTHER SEL PRODUCTS

SEL LOW LEVEL MULTIPLEXERS have several patented features which provide the advantages of an amplifier-per-channel system at a fraction of the cost. Up to hundreds of input channels with random access programming, random addressable individual channels gains, channel displays, individual channel offset, and highest sampling rates are available.



SEL 600 DATA ACQUISITION SYSTEMS can handle from a few to hundreds of inputs from your transducers, digitize this information and produce digital tapes ready for processing in your computer. Special features include linearizing and scaling of data and complete conversion to engineering units.



SEL MAGNETIC CORE MEMORY SYSTEMS provide capacity ranges from 128 to 8192 words per basic unit, and word size according to customer requirement. Standard addressing types available are random access, sequential, sequential / interlace. Combinations of types are also available.



SEL DIGITAL LOGIC MODULES conventional solid-state circuit 8000 series and the latest techniques in the newly devel series. SEL modules are de...gr implement any logical requirement at the same time, provide depe and efficient operation.





SEL 900 SERIES INDUSTRIAL CONTROL SYSTEMS for Real Time On-Line Process Control, Supervisory/Optimizing Control and Pre-Set Control. SEL 810, 820 and 840 Series Computers provide all computation, comparison and stored program functions for these direct digital and hybrid control systems.



SEL ANALOG-TO-DIGITAL CONVERTERS provide low, medium or high speed conversions. Binary or BCD outputs, sample and hold, internal or external command, and display can be provided at customer option.



SEL INSTRUMENTATION AMPLIFIERS are designed for use where lowest noise and highest accuracy are required in amplification of wideband signals. Features include extremely low noise figure, high common-mode rejection, overload protection, high-input impedance, electronic chopper, manual or automatic gain programming, and plug-in bandpass filters.



SEL OPERATIONAL AMPLIFIER pletely solid state and provide tion previously available only ube models. Features include out ± 100 volts, overload protection, a input current without temperature pensation. Several card and configurations are available for packaging requirements.

AREA OFFICES:

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637 NORTH PARK AVENUE POMONA, CALIFORNIA 91767 AREA CODE 714-623-5235



SYSTEMS ENGINEERING LABORATORIES, INCORPORA