#### **GENERAL**

The minicomputer price/performance barrier established by traditional minicomputer architectures has been broken by SYSTEMS with the introduction of the CONCEPT 32/87. The CONCEPT 32/87 Computer is the industry's most powerful 32-bit minicomputer. Based on Emitter Coupled Logic technology, this new concept in minicomputer implementation delivers performance found before only on mainframe computers.

High level system throughput is possible due to the use of such big-machine features as an ECL-technology CPU with a 75 nanosecond cycle time, a four-way set associative cache memory, a hierarchial memory system, an alterable control storage, and a four-stage instruction pipeline.

System performance is enhanced through the use of the Input/Output Processor (IOP) with its Multipurpose bus. The IOP takes over most of the I/O related functions traditionally performed by a CPU, leaving the CPU free to handle more computational functions. Offloading the CPU provides greater system throughput from better use of the CPU's time and efficient handling of device-level I/O.

# **FEATURES**

The CONCEPT 32/87 Computer includes the following features and performance characteristics:

- · Mainframe architecture and performance
- · High system throughput
- Hierarchial memory system
- Cache memory
- Dual bus structure with separate I/O Processor
- Diagnostic Processor
- ECL-based CPU with integral Floating Point Processor
- Compatible with 32 SERIES machines under the MPX-32 operating system
- · High reliability design for superior uptime

# **PERFORMANCE**

The CONCEPT 32/87 is the highest performance computer yet offered by SYSTEMS. Its performance, as measured by Whetstone and R.T. Sim. benchmarks, is shown in Table 1. The configuration used for these benchmark runs was a CONCEPT 32/87 with one megabyte of Integrated Memory Modules, one 80 MB disc, MPX-32 Revision 1.4, and FORTRAN 77+ Revision 2.0

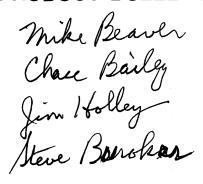
Table 1. Benchmark Results

Benchmark	CONCEPT 32/87 with 16 KB Cache	CONCEPT 32/87 with 32 KB Cache
Whetstone Single Precision Double Precision R.T. Sim.	3604 WHETS (x 1000) 2249 WHETS (x 1000) Not run	3604 WHETS (x 1000 2249 WHETS (x 1000) 22.4 sec.

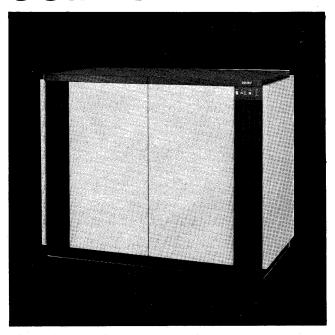
Since the Whetstone benchmark program is a relatively small program, the use of 32 KB cache does not improve Whetstone performance above the performance level attained using 16 KB cache. Of course, as task size, the number of tasks, and the number of users increase, the larger cache becomes a measurable advantage.

R.T. Sim. (Real-Time Simulation benchmark) is a mixed I/O -compute benchmark, designed to simulate a real-time environment where large arrays of data must be manipulated concurrently with large data transfers.

# PRODUCT BULLETIN



# CONCEPT 32/87 COMPUTER



Models 3810, 3820

- 3600 WHETS (x 1000)
- ECL based CPU
- 16 or 32 KB
   Cache Memory
- 32 SERIES Compatible



### **APPLICATIONS**

Due to its high performance and large memory capacity, the CONCEPT 32/87 allows significant expansion of applications without approaching the architectural limit of the machine.

The CONCEPT 32/87 is ideal for rigorous engineering applications where extremely high system performance and throughput are required. Some of the applications that the 32/87 is well suited for are:

- Laboratory and computational processing
- Scientific data processing
- · Large process control and monitoring
- Large-scale simulation
- · Program development

#### COMPATIBILITY

The CONCEPT 32/87 Computer is compatible with other computers offered by SYSTEMS. Since the instruction set of the CONCEPT 32/87 is a superset of other SYSTEMS computers instruction sets, programs developed on other SYSTEMS computers may be readily transported to the CONCEPT 32/87.

The CONCEPT 32/87 is supported by the MPX-32 operating system. Likewise, all SYSTEMS languages and utilities supported under MPX-32 are also supported on the CONCEPT 32/87 Computer.

The CONCEPT 32/87 can be linked into multiple CPU configurations with other SYSTEMS MPX-32 supported computers. A typical "shared memory" configuration would include a number of CPUs, each with its own private memory, and a common memory which can be accessed by all CPUs.

# SYSTEM ARCHITECTURE

The CONCEPT 32/87 is a powerful computer designed with features and performance found, until now, only on large machines. These include pipelined instruction execution, alterable (RAM based) control store, cache memory, integral Floating Point Processor and separate I/O and diagnostic processors.

#### **SelBUS**

The CONCEPT 32/87 system is built around a high-speed synchronous bus called the SelBUS that has a transfer rate of 26.67 million bytes per second (See Figure 1). All high-performance I/O devices, the I/O Processor, and main memory reside on the SelBUS.

#### MULTIPURPOSE BUS

The Multipurpose (MP) Bus is a medium speed asynchronous I/O bus that can transfer data at a rate of up to 1.5 million bytes per second under the control of the Input/ Output Processor. Up to 16 Device Controllers with a total of up to 124 I/O devices can exist on the MP BUS at a time.

#### CPU

The CPU is implemented with the proven 10,000 series Emitter Coupled Logic (ECL). ECL provides extremely fast gate switching times, which result in a faster CPU than can be implemented with traditional technologies. Functional units within the CPU are connected by internal busses which boast 75 nanosecond bus cycle times.

During each 75 nanosecond cycle four macro instructions are in various phases of execution. This pipelined method of operation increases the effective throughput of the CPU, and hence, the system.

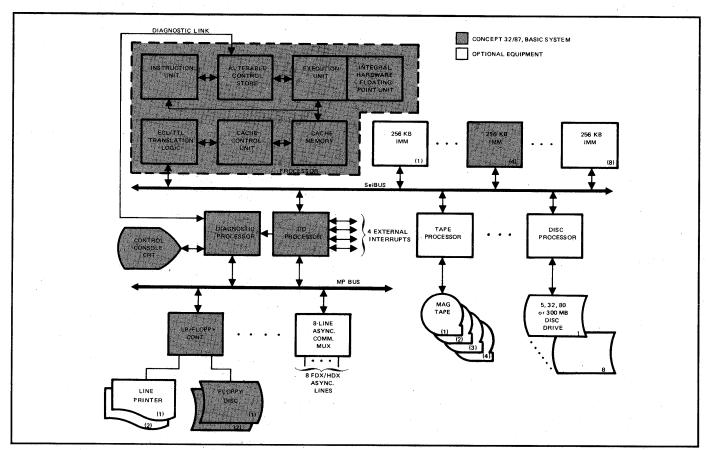


Figure 1. CONCEPT32/87 Block Diagram

#### Cache

Cache memory consists of 32 KB or 16 KB of very high-speed memory. It is integral to the CPU, and logically resides between the processor and main memory. (See Figure 1). Cache contains copies of sections of main memory, and can deliver that data to the processor in 75 nanoseconds, a fraction of the time required to fetch a word from main memory. Cache makes main memory appear to be significantly faster while being transparent to the user.

#### Instruction Repertoire

The functional classification and corresponding number of instructions for the CONCEPT 32/87 Computer are as follows:

Classification	Number
Fixed-Point Arithmetic	30
Floating-Point Arithmetic	20
Boolean	17
Load/Store	32
Bit Manipulation	8
Zero	5
Shift	13
Interrupt	11.
Compare	11
Branch	10
Register Transfer	14
Input/Output	12
Control	19
Hardware Memory Management	4
Total	206

Of particular significance are the Bit Manipulation instructions. The eight Bit Manipulation instructions provide the capability to selectively set, zero, add, or test any bit in memory or a register and also provide interprocessor semaphore capability in multiprocessor configurations.

Instructions are classified as either halfword instructions (16 bits) or word instructions (32 bits). The word instructions primarily reference memory locations; the halfword instructions primarily deal with register operands. System memory can be conserved by packing two consecutive halfword instructions into one memory location.

#### Privileged/Unprivileged Operations

The CPU is capable of both privileged and unprivileged operation. Privileged operation allows the CPU to perform control functions and I/O instructions. Unprivileged operation is the normal user program mode of the CPU. In this mode, memory protection is in effect and all privileged operations are prohibited. This prevents unprivileged users from interfering with each other or the system.

#### Floating Point Processor

The Floating Point Processor, an integral part of the CPU, is a high speed ECL based single and double-precision computational processor with 64-bit wide busses to achieve high speed floating point operations.

The CONCEPT 32/87 has a total of 20 floating point related instructions. This total includes eight instructions for addition, subtraction, multiplication, and division of words (single precision operands) and doublewords (double precision operands); eight register-to-register operations, and four fixed/floating point operand conversion instructions.

The twenty floating-point instructions are:

- Add (Word and Doubleword)
- Subtract (Word and Doubleword)
- Multiply (Word and Doubleword)
- Divide (Word and Doubleword)
- Add Register-to-Register (Word and Doubleword)
- Subtract Register-to-Register (Word and Doubleword)
- Multiply Register-to-Register (Word and Doubleword)
- Divide Register-to-Register (Word and Doubleword)
- Float Word
- Float Doubleword
- Fix Word
- Fix Doubleword

This wide selection of instructions permits the programmer to utilize the abilities of this very powerful computational force to the fullest.

#### Diagnostic Processor

The Diagnostic Processor takes up one MP BUS slot and has three main functions:

- Loading the CPU control store at power-up
- CPU Self-Test
- Diagnostic Tool

At power-up, the Diagnostic Processor loads the CPU microdiagnostics from a dedicated floppy disc to the control store RAM. It then performs CPU tests before loading the CPU microcode and system initialization. In a majority of cases, the tests point to the failing module.

Microdiagnostics for the CONCEPT 32/87 CPU are provided on floppy disc and are used to test the CPU data paths. The Diagnostic Processor communicates with the user through the control console. These built-in diagnostic features decrease system downtime and increase system availability.

#### **MEMORY**

A hierarchical memory system increases system performance by insuring that needed data is available for CPU usage in a very fast area of memory. Each level in figure 2 represents a level in the memory hierarchy. Each level is successively faster than the one below, with the CPU exchanging data with the system cache. Cache, with a greater than 90 percent hit ratio, combined with main memory that can provide a double-word fetch to the CPU and the cache in 1050 nanoseconds delivers words from main memory to the CPU in 94.5 to 153 nanoseconds.

The hit ratio and average system cycle time for any one program depends upon the size, structure, and program locality.

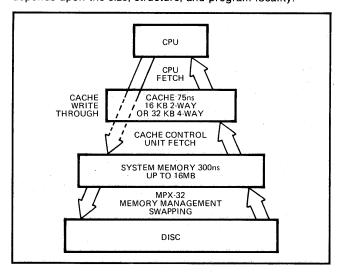


Figure 2. 32/87 Memory Hierachy

#### Cache

Two types of cache are available with the CONCEPT 32/87:

- 16K byte 2-way set associative cache
- 32K byte 4-way set associative cache

Both cache memories can provide two machine-level word instructions or four machine-level halfword instructions to the CPU in 75 nanoseconds. Both types of cache memory have a cache control unit. It fetchs data from main memory, monitors SelBUS activity, and monitors the relevance of the contents of cache memory.

The cache control unit loads the cache memory with data from main memory, (See Figure 2) and copies the memory address for that block of data into the cache index.

When the CPU reads a word, it sends the read address to the cache control unit. The cache control unit compares the most significant eleven bits of this read address with the addresses stored in the cache index. Greater than 90 percent of the time the word the CPU needs is in cache. The cache control unit sends the word to the processor over its 64-bit wide data path. If the needed word is not in cache, the cache control unit will fetch two words from main memory, send them to the processor, and store them in cache at the same time. Cache works well because computers tend to operate in loops.

Access and replacement of a block of data in cache is controlled by two accounting methods: Valid bits and Use bits. When an area of main memory is copied into cache, the valid bit is set. As long as only the CPU writes to that area of main memory, the cache is "valid", since the CPU alters both cache and main memory with a write-through. The cache control unit monitors the SelBUS for I/O transfers affecting that area in main memory. If the cache control unit detects an I/O write to the area of memory in question, the corresponding block of cache is marked "invalid" and must be updated.

The cache control unit uses a "Least Recently Used" algorithm to determine which block of data in cache can be replaced with new data from memory when the CPU requests data not in the cache. The use bits track usage for each block in cache.

A cache "write through" is done whenever the CPU writes data to memory. The CPU changes both the contents of cache and the corresponding contents of main memory, keeping the data current in both.

#### Main Memory

Main Memory in the CONCEPT 32/87 Computer interfaces directly to the SelBUS. The Integrated Memory Module is a high density memory subsystem implemented on a single board It includes 256 KB of dynamic MOS RAM, memory controller, error correction logic, and refresh circuitry. The IMM can overlap two read cycles, allowing reads to be initiated every 300 nanoseconds. A write can be initiated every 300 nanoseconds to a single IMM, but when more than one IMM is used, they can be interleaved and writes can then be initiated every 150 nanoseconds to the IMMs as a group.

The MOS Memory is organized in 39-bit words: 32 bits of data and 7 error Correction Code Bits (ECC). During write operations, the ECC bits are generated based on a modified Hamming code algorithm and stored in memory. When a read memory operation

takes place, the ECC bits are checked. If a 1-bit error is detected, the error is corrected. Two bit errors and multiple bit errors with an even number of bits wrong cause an error detection signal.

The CONCEPT 32/87 Computer supports up to 16 MB of physical memory. The chassis provided with the CONCEPT 32/87 supports 2 MB (8 IMMs) of memory. With the addition of a SeIBUS chassis, eight more IMMs can be added to the system. Memory requirements from 4 MB to 16 MB can be satisfied by Memory Support Packages.

#### Hardware Memory Management

The CONCEPT 32/87 Computer operates under the MPX-32 Operating System. MPX-32 is a mapped executive and has two ways to address memory; Mapped, Nonextended, and Mapped, Extended.

#### Mapped, Nonextended

Mapped, Nonextended addressing allows the CPU to address any instruction or operand (bit, byte, halfword, word, or doubleword) within a task's logical address space. This space consists of 512 KB of logical memory dispersed anywhere within the 16 MB physical memory in 2 KB blocks.

MPX-32 allows multiple logical address spaces. A user can access instructions and operands within the logical address space in which his task resides. Physical blocks of memory can be common to many logical address spaces; thus, tasks in different logical address spaces can share common blocks of physical memory.

#### Mapped, Extended

Mapped, Extended addressing provides all the capabilities of Mapped, Nonextended addressing plus access to a extended logical address space.

This space consists of 1.5 megabytes of memory beyond the primary logical address space. It allows the user additional memory space to store data (operands). Each extended logical address space can be 1.5 megabytes long, dispersed anywhere within 16 megabytes of physical memory. The combination of primary and extended logical address space supports programs up to two megabytes long. The executable code must lie within the primary logical address space but operands can be in either the primary logical or extended logical address space. Mapped, Extended addressing allows a task in the CONCEPT 32/87 to address a total of two megabytes.

#### **Memory Protect**

The Memory Protect system provides write protection for individual protection granules. A protection granule consists of 2 K bytes. Up to 256 granules (512 K bytes) can be protected at a time. The memory protect registers can be changed only by executing privileged instructions, providing a secure system.

In addition, memory management provides memory protection for each 2 KB map block of logical address space. One protect bit is associated with each 2 KB map block.

#### INPUT/OUTPUT SUBSYSTEM

The dual bus architecture of the CONCEPT 32/87 provides a choice of I/O prformance levels. SYSTEMS high performance I/O resides on the SelBUS, while medium performance I/O resides on the MP Bus. This two bus I/O structure allows great flexibility in system integration.

The MPX-32 operating system supports 16 Megabyte addressing, command chaining, and data chaining via extended I/O (XIO) protocols, to provide a powerful I/O system.

Modem support under MPX-32 adds to the scope of the I/O system, providing communications processing capabilities.

The CONCEPT 32/87 Computer has a total of 12 I/O instructions. Upon execution of a single instruction, an I/O Controller can be conditioned to transfer one or more blocks of data between an external device and memory. Once the transfer is initiated, the controller takes charge of the I/O operation, and the CPU is free to perform other tasks. When the transfer is completed, the I/O Controller can notify the CPU by an interrupt.

#### Input/Output Processor

The IOP is a powerful multiplexing channel for I/O operations. The IOP operates independently of and in parallel with the CPU. The result is increased CPU availability and improved system performance. Up to 16 Device Controllers supporting a total of up to 124 devices can be handled on a single MP BUS by a single IOP. Larger systems can use multiple IOP's and MP Busses, if required.

Four user-defined external interrupts for real-time sense and control, a 32-bit programmable timer, and a real-time clock are included in the IOP.

A Control Console Port on the IOP provides system control functions, eliminating the need for an operator's control panel.

#### Control Console

The traditional control panel functions have been combined with the operator's console functions on the Control Console CRT, which is connected to the Control Console Port.

The Control Console port can support modems, making remote control of the system possible over a telephone or private line.

The Control Console has three modes; Operator's Console mode, Control Panel mode, and Diagnostic mode. The operator can switch between the three modes at any time.

Operator's Console mode is the normal mode for the Control Console when the system is running. Job status, user status, and operator information are displayed. The operator can monitor and control the operation of the system. In the Operator's Console mode, the CRT can also function as a user terminal with all MPX-32 functions available.

Control Panel mode displays status and allows the operator to display and/or modify Machine State, General Purpose Register contents, and memory locations. Figure 3 outlines the display format

The system is in diagnostic mode when first powered up. CPU microdiagnostics can be run, single-stepped, and halted from the Control Console, which displays relevant information on the status of each diagnostic.

#### High Performance I/O

High performance, SelBUS-based I/O Interfaces include:

- High Speed Data Interface (HSD)
- Tape Processor
- High Speed Tape Processor
- Disc Processor II

The Model 9131 HSD II has a data transfer rate of 3.2 Megabytes per second. It is most useful in applications where a customer device has a very high maximum throughput. Interbus links between two SYSTEMS computers consist of two interconnected HSDs, one for each computer.

The Model 9020 Tape Processor supports up to four 800 bpi, 1600 bpi, or 800/1600 dual density drives at 45 or 75 ips. Drives having the same tape speed and different densities can be supported by the same Tape Processor.

The Model 8050 High Speed Tape Processor supports dualdensity (1600/6250 bpi) 75 and 125 inch-per-second and tridensity (800/1600/6250 bpi) 125 inch-per-second tape drives. Up to four drives of any type can be supported by a single High Speed Tape Processor.

Model 8055 Disc Processor II supports up to four 5, 32, 80 or 300 Megabyte discs. Up to eight discs can be optionally supported. A Dual Port Operation option is also available.

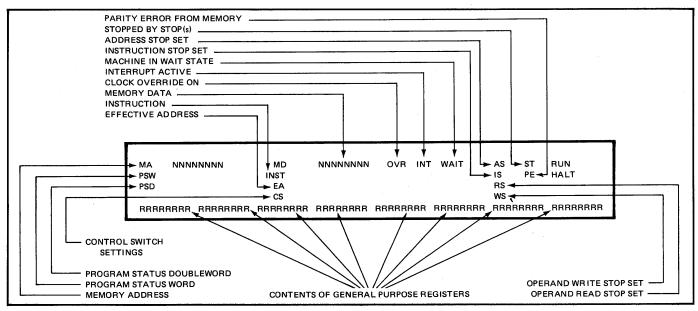


Figure 3. Control Panel Mode Display

#### Interrupts/Traps

The CONCEPT 32/87 Computer can accommodate up to 96 hardware priority interrupt levels used for I/O Controllers, and external signals. The interrupts associated with the I/O are provided by the I/O Controllers.

The IOP provides four external interrupt levels, a real-time clock, and a 32-bit programmable interval timer. Each uses one of the 96 interrupt levels.

Each interrupt level has an assigned dedicated memory location. All interrupt levels can be selectively enabled, disabled, activated, deactivated, and requested under software control. All Interrupt Control Instructions are privileged. Attempts at execution by unprivileged programs will yield a Privilege Violation Trap.

Users requiring more external interrupt lines than provided by their IOPs can add one or more Model 2345 Real-Time Option Modules. Each provides 16 external interrupt levels.

# **PACKAGING**

The CONCEPT 32/87 has been packaged in a way that is a major functional and asthetic departure from previous SYSTEMS computers. Low profile (55½") cabinet design combined with improved cooling and easy access to equipment make the CONCEPT 32/87 Computer easier to use and maintain. The CONCEPT 32/87 power system is UL listed.

Cabinets for peripherals and additional logic or memory are also available in the same design. The CONCEPT 32/87 CPU cabinet is shown in Figure 4.

The CPU cabinet contains two chassis: a CPU/Logic chassis and a MP BUS chassis. The CPU/Logic chassis has a total of 38 slots, including 21 CPU slots and 17 SelBUS slots. Twelve SelBUS slots are available for expansion beyond the CONCEPT 32/87 Basic System.

A Logic/Memory Support Package can be added to the CONCEPT 32/87. It provides 18 additional SelBUS slots, and can support up to eight IMMs and ten SelBUS-based modules, or combinations with more than ten SelBUS-based modules.

There are two chassis positions available for expansion of the CONCEPT 32/87. Any combination of Memory Support Packages and I/O Expansion Chassis can be put into these positions.

One Logic/Memory Support Package can be placed in one of the positions, leaving the other free for an I/O Expansion Chassis or a Memory Support Package.

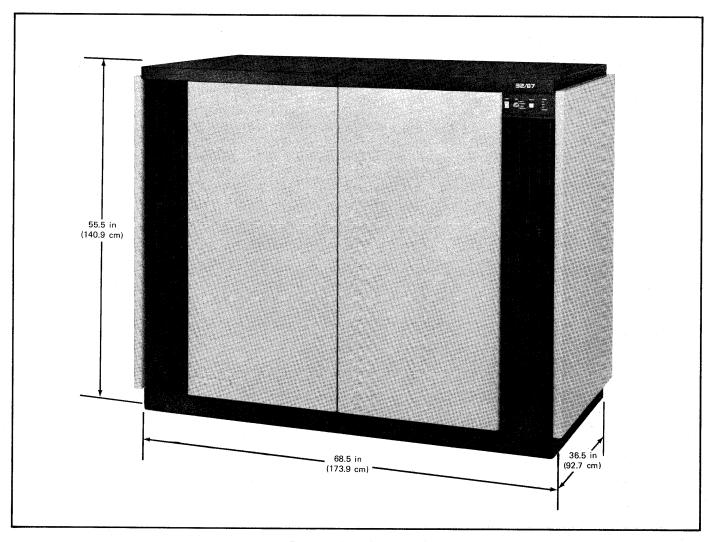


Figure 4. CPU Cabinet Pictorial

#### **MODEL NUMBERS**

# Model Number

# Nomenclature/Description

#### 3810

# CONCEPT 32/8710 COMPUTER BASIC

A 32-bit super minicomputer with 16 KB cache, based on ECL technology. The CONCEPT 32/87 includes:

- ECL-based 32-bit CPU
- 16 KB Cache Memory
- 1 Megabyte of Main Memory (4 IMMs)
- **Built-in Floating Point Processor**
- Input/Output Processor
- Diagnostic Processor
- Line Printer/Floppy Controller
- Two Floppy Disc Drives
- **CRT Control Console**
- 38-slot CPU Chassis with 17 SelBUS slots, (12 available) 21 CPU slots, and Power Supplies
- 8-slot I/O Chassis (MP BUS) with 6 available slots and required Power Supplies
- **Dual width Cabinet**
- AC Distribution Panel
- Firmware and Diagnostics on diskettes
- Manuals

#### 3810-1

## **CONCEPT 32/8710 COMPUTER BASIC**

Same as 3810 except 416/220 Vac, 50 Hz

power.

## 3820

3820-1

# **CONCEPT 32/8720 COMPUTER BASIC SYSTEM**

A 32-bit super minicomputer with 32 KB cache, based on ECL technology. The CONCEPT 32/87 includes:

- ECL-based 32-bit CPU
- 32 KB Cache Memory
- 1 Megabyte of Main Memory (4 IMMs)
- **Built-in Floating Point Processor**
- Input/Output Processor
- Diagnostic Processor
- Line Printer/Floppy Controller
- Two Floppy Disc Drives
- **CRT Control Console**
- 38-slot CPU Chassis with 17 SelBUS slots. (12 available) 21 CPU slots, and Power Supplies
- 8-slot I/O Chassis (MP BUS) with 6 available slots and required Power Supplies
- **Dual width Cabinet**
- **AC Distribution Panel**
- Firmware and Diagnostics on diskettes
- Manuals

# **CONCEPT 32/8720 COMPUTER BASIC**

SYSTEM

Same as 3820 except 416/220 Vac, 50 Hz

power.

# PERFORMANCE SPECIFICATIONS

#### **PROCESSOR**

Word Length

32 bits

**Data Sizes** 

1, 8, 16, 32, 64 bits

General Purpose Registers

8 (3 of which can be used

for indexing)

Additive Timing for Instruction Execution:

Indexing

None

Mapping

None

Instruction Repertoire

206 Instructions

Floating-Point Arithmetic

Integral Floating Point Processor in CPU.

Integrity Features

Memory Protect, Power Fail Safe, Memory ECC, Arithmetic Exception, Privilege Violation, Non-

present Memory

#### I/O SYSTEM

IOP Throughput

1.5 MB/second per IOP

I/O Mode

Block transfer

**SelBUS** 

Continuous Throughput

26.67 MB/second

# **MEMORY**

Medium

Dynamic MOS

Word Size

32 data bits plus 7 ECC bits

Cycle Time

300 ns effective

**Expansion Increments** 

256K bytes (64K words)

Capacity:

Inherent Capacity Maximum IMMs

2 Megabytes 4 Megabytes 16 Megabytes System Maximum

Interleaving

Standard (0-, 2- or 4-way)

Overlapping CACHE

Size

Organization

Standard

16 KB or 32 KB 2- Way or 4- Way Set Associative

Replacement Algorithm

Least Recently Used

# **INTERRUPTS**

**Priority Levels** 

96 Maximum

Real-Time Clock

60/120 Hz or 50/100 Hz (line frequency dependent)

Interval Timer

32-bit 300 ns resolution

# PHYSICAL/ENVIRONMENTAL

Operating

Temperature (°C) Relative Humidity

10° to 40° 5% to 95%

non-condensing

Storage

Temperature (°C) Relative Humidity -40° to 60° 2% to 95%

non-condensing

**DIMENSIONS** 

**CPU Cabinet** 

Height Width Depth

55.5 in (140.9 cm) 68.5 in (173.9 cm) 36.5 in (92.7 cm)

**ELECTRICAL** 

Models 3810

3820

3810-1

3280-1

Frequency

60 Hz

50 Hz

Voltage

115/208 Vac

416/220 Vac

Phases

3 Phase

3 Phase

Amps per Phase

50 Amps

50 Amps

Connection

Hardwired

Hardwired

Power Supplies:

**ECL** Logic

-5.2 Vdc @ 190 Amps 2.2 Vdc @ 200 Amps

TTL Logic

5 Vdc @ 300 Amps

Memory

5 Vdc @ 40 Amps 15 Vdc @ 11 Amps -15 @ 5 Amps

I/O Expansion

Chassis

5 Vdc @ 40 Amps -5 @ 7 Amps

15 Vdc @ 9 Amps

CORPORATE HEADQUARTERS

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