# INPUT/OUTPUT PROCESSOR (IOP) Model 8000 and 8001 USER INTERFACE MANUAL

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# WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to subpart J of part 15 of FCC rules, which are designated to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

#### CHAPTER 1

#### **FUNCTIONAL DESCRIPTION**

#### 1.1 General Information

The User Interface Manual supplies the necessary information to allow a designer to develop interfacing and protocol handling circuitry for the Input/Output Processor (IOP), Model 8000 and 8001.

The primary supporting documents for this user interface manual are the IOP Technical Manual, publication number 303-000170, the IOP Drawings Manual, publication number 304-000170, the IOP User Reference Manual, publication number 301-000170, and the CONCEPT/32 Circuit Registration Manual, publication number 313-000670.

The information contained in this manual is presented in the following order:

Chapter 1 - Functional Description
Chapter 2 - Operational Description
Chapter 3 - Electrical Specifications

Chapter 4 - Signal Cabling and Connections

The IOP consists of the following elements: a SelBUS interface, a multipurpose bus (MP Bus) interface, the IOP proper, and the system control panel (SCP) device dependent logic.

The SelBUS interface provides the communication path between the IOP and central processing unit (CPU), or IOP and memory.

The IOP proper has a control memory that contains the microprogram (firmware) for controlling the SelBUS and IOP interfaces.

The IOP interface circuits consist of control logic for operating the MP Bus, SCP interface, and receiver/drivers necessary to communicate with the I/O controllers.

For a more detailed description of the IOP hardware refer to the IOP Technical Manual.

Eight bit MP Bus controllers use Intel's 8291 general purpose instrument bus (GPIB) interface chip to simplify controller interface design and maintain a low interface IC count.

High performance controllers may be designed to transfer data 16 bits at a time and maintain a 1.5 MB throughput.

A minimum of one to a maximum of 16 controllers can be connected to the MP Bus. The controllers used in a particular system are distributed in any desired manner along the MP Bus. Each controller is allowed a maximum burst transfer time of 537 microseconds per burst.

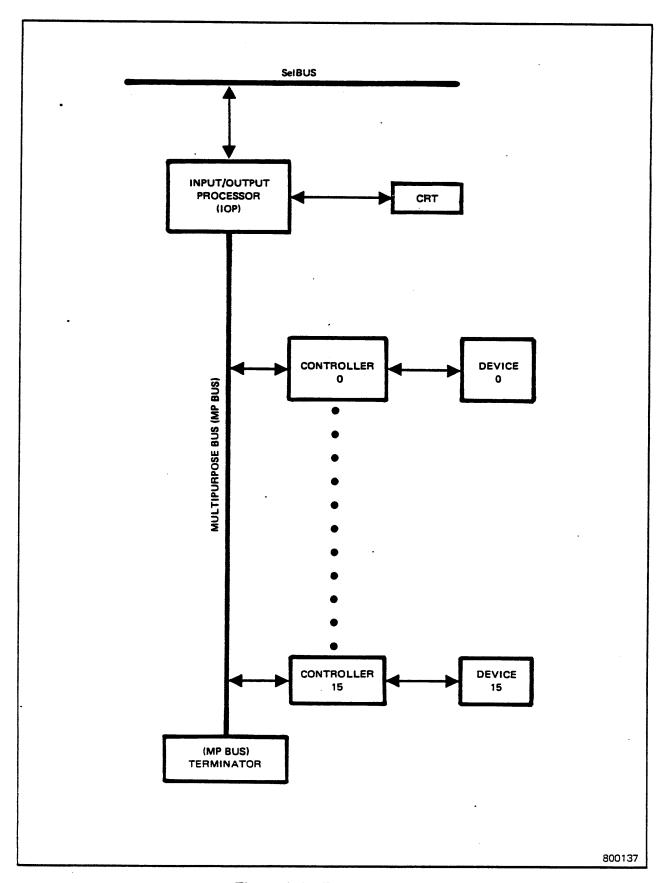


Figure 1-1. Typical System

The IOP is configured at one end of the MP Bus. The opposite end of the bus contains a MP Bus termination card. Controllers are connected within the I/O backplane using an interconnect bus. This backplane may be a part of the SelBUS chassis or a separate I/O chassis. The backplane is connected to the IOP using a 50 pin flat cable.

A minimum of one to a maximum of 16 devices can be connected to a controller. However, a maximum of 124 devices can be connected to one IOP.

A simplified block diagram of the IOP, in a typical system, is shown in Figure 1-1.

# 1.2 Multipurpose Bus (MP Bus) Description

The MP Bus is a highly efficient, cost effective, asynchronous bidirectional bus that functions at a maximum burst rate of 1.5 megabytes per second. The rate of data transfer is a function of the three wire handshake signals: data available (DAV), not ready for data (NRFD), and no data accepted (NDAC), and the operational speed of the individual controllers.

There are two basic protocols on the MP Bus: the service request (SRQ) protocol, (initiated by a device controller) and the IOP initiated protocol. The SRQ protocol notifies the IOP so that a particular controller can transfer status or data for the device specified in the state information. The IOP then initiates a parallel poll to determine which controller pair is requesting service. A serial poll is then used to determine which controller of the pair is requesting service. The state information (containing the device address) is passed to the IOP during the serial poll. The IOP initiated protocol notifies a controller that the IOP wants to initiate or terminate a transfer of information.

#### 1.2.1 Line Definition

The MP Bus interface connects the IOP to one or more (up to 16) controllers. The controllers are then connected to specific devices. A cable physically connects the IOP to the controller's backplane. This cable carries various signals to and from the IOP and controllers. The types of signals and direction of transfers carried on these lines are discussed in the following text. Note that the direction of the transfers is referenced from the IOP. Refer to Figure 3-2 for the location of the various signals discussed in the following text.

#### 1.2.1.1 I/O Data Lines

All of the I/O data lines are low true and are driven by open collector drivers on the IOP or controller. The I/O data lines are listed in Table 1-1.

#### 1.2.1.2 I/O Control Lines

All I/O control lines listed in Table 1-2 are low true and driven by open collector dirvers on the IOP or controller.

Table 1-1 I/O Data Lines

Name of I/O Data Line	MP Bus Connection	Uses
LDI00 LDI01 LDI02 LDI03 LDI04 LDI05 LDI06 LDI07 LDI08 LDI09 LDI10 LDI11 LDI12 LDI12 LDI13 LDI14 LDI15	Pin 20 Pin 21 Pin 23 Pin 24 Pin 26 Pin 27 Pin 29 Pin 30 Pin 32 Pin 33 Pin 35 Pin 36 Pin 38 Pin 38 Pin 39 Pin 41 Pin 42	These data lines (LDI00 through LDI15) carry data to or from the IOP from or to the devices, via the controllers.
LPARITY	Pin 10	The parity line carries odd parity information with all data transfers. Parity data is always low true.
LHALFWORD	Pin 14	The halfword line notifies the receiver that a 16 bit transfer is on the MP Bus.

Table 1-2 I/O Control Lines

Name of I/O Control Line	MP Bus Connection	Uses
LDAV	Pin 6	The data available line is controlled by the interface circuitry and driven true (low) each time data is placed on the MP Bus. The LDAV line can be driven by the IOP or any talking controller. Data must be valid whenever the LDAV line is low.
LNRFD	Pin 44	The not ready for data line is controlled by the receiving circuitry and remains true (low) until after the listeners data in register has been read. This signal prohibits the overrun of the last data byte in the interface. This signal is set high to indicate that the listener is ready for data, and set low to indicate that the listener can accept no more data. LDAV is not sent until this line is false (high).
LNDAC	Pin 46	The not data accepted line is controlled by the receiving circuitry and remains true (low) until after the listener has clocked the MP Bus data into it's data in register. The LNDAC signal is then set high (false). The LNDAC signal is set low after LDAV is again set high.
LEOI	Pin 8	The end or identify line is set true (low) by a controller to notify the IOP that the last byte of data, for the burst, is on the MP Bus. This signal is set low by the IOP to indicate that the last byte of a transfer is on the MP Bus. The LEOI signal is also used to notify a controller that it has exceeded the 537 microseconds allowed on the MP Bus and, as a result, the burst terminates. This signal is also used with LATN active low to initiate a parallel poll.

# 1.2.1.3 Output Control Lines

All output control lines listed in Table 1-3 are low true and are only driven by open collector drivers on the IOP.

# 1.2.1.4 Input Control Lines

All input control lines shown in Table 1-4 are low true and are only driven by open collector drivers on the controllers.

Table 1-3
Output Control Lines

Name of Output Control Line	MP Bus Connection	Uses
LATN	Pin 4	The attention line, driven by the IOP, causes all controllers on the MP Bus to respond with a handshake. This line is active low when the IOP wants to send commands, control signals, or addresses on the MP Bus. This signal is also used with LEOI active low to initiate a parallel poll.
LIFC	Pin 16	The interface clear line causes all MP Bus controllers and devices to go into a predetermined state. In this state the MP Bus controller will not drive any bus lines. This action represents a reset on the MP Bus. The LIFC signal does not require a handshake.

Table 1-4
Input Control Lines

Name of Input Control Line	MP Bus Connection	Uses
LSRQ	Pin 12	The service request line is set true (low) by any controller to notify the IOP that it is ready to transfer information (data or status). This signal does not require a handshake.
LINHIBIT	Pin 48	The inhibit line removes the IOP from control of the MP Bus. It also removes the drive of all control and data signals. The inhibit line may only be used as a static function and; therefore, can't be used while the controllers are operating. The L5.0688 MHz clock is not affected by the LINHIBIT line.

# 1.2.1.5 Output Timing Lines

The output timing lines shown in Table 1-5 are low true and driven by IOP open collector drivers.

# Table 1-5 Output Timing Lines

Name of Output Timing Line	MP Bus Connection	Uses
L150NSCLK	Pin 2	This bus clock line is used for all primary synchronization and may be used by high speed controllers as their basic clock.
L5.0688MHZ	Pin 18	This clock line may be used by communications controllers, generated by the IOP, and driven on the MP Bus as a freerunning clock. This line is not affected by the LINHIBIT line.

# 1.2.2 Multipurpose Bus Modes of Operation

The five modes of operation used by the IOP on the multipurpose bus (MP Bus) are listed below:

- 1. Address mode
  - a. Addresses controller
  - b. Identifies the controller as a talker or listener
- 2. Control signal mode
  - a. Transfers control information to the addressed controller
  - Transfers control information to all controllers
- 3. Parallel poll mode
  - a. Identifies which 2 of 16 controllers initiated an SRQ
  - b. Used for priority polling
- 4. Serial poll mode
  - a. Informs the IOP which one of two controllers (sharing priority) has requested service
  - b. Includes the address of the device
  - c. Decides whether status or data is ready
  - d. Indicates the type of transfer (byte/halfword) used
  - e. Indicates whether the controller has more data to input (incorrect length)
- 5. Data mode
  - a. Transfers data from talker to listener
  - b. Drives talker data and data available (DAV) lines
  - c. Receives listener data and drives the no data accepted (NDAC) and not ready for data (NRFD) lines

In the address mode, addresses identifying the controller as a talker or listener, are sent to the controller.

In the control signal mode, primary and secondary control signals are sent to the controllers and devices. Primary and secondary control signals are further divided into addressed and universal control signals. Addressed control signals are only recognized by the controller or addressed device. Universial control signals are recognized by all controllers on the MP Bus. Primary control signals are interpreted by the controllers.

Secondary control signals are an extension of the primary control signal field and must be immediately preceded by a primary control signal. The secondary control signals are used to send extended I/O commands and device addresses to the controllers. This procedure allows the controller to recognize the secondary control signal in only the addressed mode.

In the parallel poll mode 2, of a possible 16, controllers which initiated a SRQ are identified. This mode is used for priority polling. A method of priority polling is established and maintained in the following manner: Eight of the data lines (LDI00 through LDI07) on the MP Bus are assigned to two of the controllers. When parallel polling is initiated, the controllers set their assigned parallel poll data line true (low) if they need service. The IOP examines the lines and determines which controllers need service and which one to service first. The controller with the highest priority has the lowest address (e.g., the controller with highest priority is assigned address zero, next highest priority is assigned address one, etc.). Note that addresses zero and one share priority zero and addresses two and three share priority one, etc.

In serial poll mode, the IOP is informed of which one of the two controllers, sharing priorities, has requested service. The address of that device and the address of the controller requesting service is also included in the serial poll mode data. The IOP is also notified of status (for this particular device) and the type of transfer required (byte or halfword). The state information is in the output register as follows:

Bit 0, when set, indicates that status for the device requesting service is available in the data out register of the controller.

Bit 1, when set, informs the IOP that this controller has requested service.

Bit 2, when set, indicates that the controller is requesting byte transfers on the MP Bus. Bit 2, when not set, indicates that the controller is requesting a halfword transfer.

Bit 3, when set along with status ready (bit 0), indicates the controller has more data to transfer.

Bits 4 through 7 contain the hexadecimal address of the device on the controller requesting service.

The data mode transfers data on the MP Bus from talkers to listeners. The talker drives data and the data available signal onto the MP Bus. The listener receives data from the MP Bus and drives the no data accepted signal onto the MP Bus. Data must be driven to or from the IOP. No controller-to-controller communications are allowed on the MP Bus.

Commands, status, and data are placed onto the MP Bus via these modes using the following sequences. Because each of these modes requires a specified series of events on the MP Bus, they will also be referred to as sequences.

# 1.2.2.1 Command Transfer Sequence

The command transfer sequence is initiated by the IOP and is used to pass extended I/O commands to the controller. (For more detailed information see Chapter 2). Each mode

of this sequence requires the handshake sequence, as described in Chapter 2. The sequences of events are listed below:

Address sequence - listen.

Control signal sequence - execute secondary command (ESC).

Control signal sequence - extended I/O command most significant nibble (MSN).

Control signal sequence - extended I/O command least significant nibble (LSN).

Control signal sequence - device address.

Address sequence - unlisten.

# 1.2.2.2 Data Transfer Sequence

The data transfer sequence is initiated by a controller when it is ready to accept or output data from or to the IOP. The sequence is started by a controller pulling the SRQ line active (low). The sequence of events for a data transfer sequence are listed below:

Service request - SRQ low.

Parallel poll request - LEOI and LATN low.

Control signal sequence - serial poll enable (SPE).

Address sequence - talk XXX0.

Data sequence - state XXX0 (with RSV bit set if service is requested or 4.8 microsecond timeout if there is no controller at this address).

Address sequence - untalk.

Control signal sequence - serial poll enable (SPE).

Address sequence - talk XXX1 (only used if controller XXX0 didn't request the service).

Data sequence - state XXX1 (with the RSV bit set).

Address sequence - untalk.

Control sequence - serial poll disable (SPD).

Address sequence - talk or listen (determined by the extended I/O command).

Data sequence - data.

Data sequence - data.

Data sequence - data (etc).

Data sequence - data and end or identify (LEOI).

Address sequence - untalk or unlisten (determined by the extended I/O command).

# 1.2.2.3 End of Message Sequence

The end of message (EOM) sequence is used by the IOP to notify the controller that an I/O command's byte count has been exhausted and status is requested. The status transfer sequence will follow the EOM sequence. The sequence for this procedure is shown below:

Address sequence - listen.

Control signal sequence - EOM.

Control signal sequence - device address.

Address sequence - unlisten.

# 1.2.2.4 Status Transfer Sequence

The status transfer sequence is identical to the data transfer sequence, except the status ready (SR) bit in the state transfer is set. (For a more detailed discussion see Chapter 2). The status transfer sequence is shown below:

Service request - LSRQ low.

Parallel poll request - LEOI and LATN low.

Control signal sequence - serial poll enable (SPE).

Address sequence - talk XXX0.

Data sequence - state XXX0 (with SR and RSV bits set if service is requested or 4.8 microseconds timeout if there is no controller at this address).

Address sequence - untalk.

Control signal sequence - serial poll enable (SPE).

Address sequence - talk XXX1 (only used if controller XXX0 did not request service).

Data sequence - state XXX1 (with SR and RSV bits set).

Address sequence - untalk.

Control signal sequence - serial poll disable (SPD).

Address sequence - talk.

Data sequence - status.

Address sequence - untalk.

#### CHAPTER 2

# **OPERATIONAL DESCRIPTION**

#### 2.1 General Information

This chapter describes the multipurpose bus (MP Bus) software interface, interface sequences, general system considerations, and features of the input/output processor (IOP).

# 2.2 Multipurpose Bus Interface

The multipurpose bus (MP Bus) is a highly efficient, cost effective asynchronous, bidirectional bus that functions at a maximum burst transfer rate of 1.5 megabytes per second. The rate of data transfer is a function of the three wire handshake signals: data available (DAV), not ready for data (NRFD), and no data accepted (NDAC), and the operational speed of the individual controllers.

The IOP controls up to 16 device controllers via the MP Bus. There are five types of transfers performed by the IOP to the controller:

- 1. Command
- 2. Control signal
- 3. Reset
- 4. Data
- 5. Interface clear

The device controller on the MP Bus performs five types of transfers to the IOP:

- 1. Data
- 2. Status
- 3. State
- 4. Service request
- 5. Parallel poll priority

# 2.2.1 Extended I/O Commands

Each extended I/O command transfer requires two secondary address command transfers on the MP Bus following an execute secondary command. Extended I/O device commands are shown in Table 2-1.

Table 2-1
Extended I/O Device Commands

Command	First Secondary Command	Second Secondary Command
Sense Read Write Control	ММММ ММММ ММММ ММММ	0100 MM10 MM01 MM11
M is a modifi	er bit which is defined by each o	ontroller.

The last two bits in each secondary command has significance and determines the major command function.

# 2.2.1.1 Extended I/O Command Sequence

The extended I/O command sequence, which sends all extended I/O commands to the controller, is shown below:

- 1. An addressed listener sequence.
- 2. An addressed primary control signal sequence with an execute secondary command (ESC).
- 3. An addressed secondary command sequence with the four most significant bits (MSBs) of the extended I/O command as the least significant bits (LSBs) of the secondary command. Bit 4 is the MSB of the extended I/O command nibble.
- 4. An addressed secondary command sequence with the four LSBs of the extended I/O command as the LSBs of the secondary command. Bit 4 is the MSB of the extended I/O command nibble.
- 5. A device address sequence to pass the device address to the controller.
- 6. An unlisten sequence.

# 2.2.2 Extended I/O Status

Status transfers normally occur as a data transfer sequence, following the parallel poll, which is initiated by a SRQ from a controller. Status is read from the data out register on the controller when the status ready (SR) state bit is set. However, the software may obtain a device status report using the extended I/O sense command. Status available in the sense command is determined by controller implementation.

Status in the data out register is interpreted as shown in Table 2-2.

Table 2-2
Data Out Register Status

Bit	Meaning
0 1 2 3 4 5 6 7	Busy Status modifier Controller end Attention Channel end Device end Unit check Unit exception

Note: Bit 7 with bit 3 (unit exception with attention) may be used to signal an initial program load from this device. Exact interpretation of these status bits is left to the individual controller.

# **2.2.2.1** Busy Status

Busy status indicates that the device or controller cannot execute the command or I/O instruction because it is executing a previously initiated operation. If the busy condition applies to the controller, the status modifier bit is also set.

The busy signal indicates to the central processing unit (CPU) that the IOP cannot accept any CPU transfer requests for at least 20 microseconds. This signal is important to the advance read status transfer (ARSTX) and the advance interrupt control transfer (AICT) CPU bus transfers. When busy status is true, the CPU immediately terminates the macroinstruction with a condition code. This action indicates that the IOP is busy. Alternately, the CPU may retransmit the transfer request, at one microsecond intervals, for 20 microseconds.

# 2.2.2.2 Status Modifier Status

Status modifier status indicates that the controller cannot provide current status because it is busy, or that the normal sequence of the input/output command doublewords (IOCDs) is to be modified.

When status modifier status is stored, in response to an I/O instruction, all other status bits are zero. This condition indicates that the controller cannot execute the instruction, and it has not provided current status. Any pending interrupt conditions present in the controller or device are not cleared, and the status stored in memory will contain all zeros (except the status modifier status bit).

When the status modifier bit appears with the busy bit, it indicates that the condition pertains to the controller and the addressed device. The controller appears busy when executing operations that preclude the acceptance and execution of any command or I/O instruction, or contain a pending interrupt and status for a device other than the device addressed. By generating status modifier and attention status conditions, a device may request an initial program load from itself.

# 2.2.2.3 Controller End Status

Controller end status indicates that the controller has become available for use in another operation. Controller end status is only provided by a controller shared by multiple I/O devices and only when one or both of the following conditions have occurred:

- 1. The software previously caused the controller to be interrogated while the controller was in the busy state. The controller is defined as being in the busy state when a command or I/O instruction has been issued to a device on the controller and the controller has responded with a busy status modified in the status data.
- The controller detected an unusual condition during the operation after a channel end command was executed, but before a device end command. The unusual condition accompanies the controller end status.

If the controller remains busy after a channel end condition, but was not interrogated by the software, controller end status is not generated. The controller does not provide controller end status if the instruction was accepted.

When a temporary controller busy state occurs, controller end status is included with the busy and status modifier status even though the controller has not been freed. The busy condition is considered temporary if its duration does not exceed 50 microseconds.

Controller end status can be generated with a channel end or device end condition. It can also be generated between the two conditions. When a controller end status condition is generated, using an interrupt in the absence of any other condition, the controller can be identified by the subaddress provided in the status. Pending controller end status causes the controller to appear busy for the initiation of any new operations.

# 2.2.2.4 Attention Status

Attention status indicates that the device has detected a device dependent asynchronous condition. The device can generate attention status only when no operation is in process at the subchannel, controller, and device. The attention status accompanies a device end command upon completion of an operation. It can also be presented during the initiation of a new operation. Attention status accompanying a device end condition causes command chaining to be suppressed. Attention status alone may be generated when no operation is in process at the subchannel, controller, or device.

#### 2.2.2.5 Channel End Status

Channel end status is caused by the completion of the I/O operation involving data transfer or control information between the controller/device and the IOP. This status condition indicates that the subchannel has become available for use in another operation.

Each I/O operation causes a channel end status condition to be generated. When command chaining occurs only the channel end status condition of the last operation of the chain is reported to the software. Channel end status is unavailable to the software when a chain of commands is prematurely terminated because of an unusual condition, indicated with control unit end or device end status information or during the initiation of a command.

During control operations, channel end status is generated when the control information has been transferred to the device. For operations of short duration, channel end status may be delayed until the completion of the operation. Operations that cause no data to be transferred can generate a channel end condition during the initiation sequence of the command. A channel end condition pending in the controller causes the controller to appear busy for the initiation of a new operation.

# 2.2.2.6 Device End Status

Device end status is caused by the completion of an I/O operation at the device. On some devices, device end status is caused by manually changing the device from a not ready to a ready state. Device end status indicates that the device has become available for another operation.

Each I/O operation causes a device end status condition to be generated. When command chaining occurs, only the device end status of the last operation of the chain is reported to the software, unless an unusual condition is detected during the initiation of a command. If this condition occurs, the command is terminated without device end status.

Device end status associated with an I/O operation is generated either simultaneously with channel end status or at a later time. For control operations, device end status is generated at the completion of the operation of the device. The operation may be completed at the time channel end status is generated, or it may be completed at a later time.

When command chaining is specified in the subchannel, receipt of device end status, in the absence of any unusual conditions, causes the IOP to initiate a new I/O operation.

The presence of status modifier and device end status indicate that the normal command sequence must be modified. The handling of this set of bits by the IOP depends on the operation. If command chaining is specified in the current IOCD and no unusual conditions are present, status modifier and device end status cause the IOP to fetch and chain to the IOCD whose main memory address is 16 greater than that of the current IOCD. If command chaining is not specified or if any unusual conditions exists, the IOP takes no action, and status is saved in the status words.

#### 2.2.2.7 Unit Check Status

Unit check status indicates that the controller or device has detected an unusual condition that is detailed by the information available to a sense command. Unit check status may indicate that an IOP programming error has occurred, an equipment error has occurred, or a not ready state of the device has affected the execution of the command. Unit check status provides a summary indication of the conditions identified in the sense data.

An error condition causes unit check status only when it occurs during the execution of a command or during some activity associated with an I/O operation. Unless the error condition pertains to the activity initiated by a command, and is of immediate significance to the software, unit check status does not cause the software to be altered after the device end condition is cleared. A malfunction may cause the device to enter a not ready state.

Unit check status also indicates the existance of the not ready state, precluding the satisfactory execution of the command. The unit check status bit, in the absence of device end, channel end, or controller end conditions, indicates that the command was aborted before any action was attempted.

Unless the command is designed to cause a unit check indication, unit check status is not reported if the command is properly executed, even though the device entered a not ready state during the operation or as a result of the operation. Similarly, unit check status is not reported if the command can be executed with the device not ready. Selection of the device, in the not ready state, does not cause a unit check status indication when the sense command is issued, and whenever a controller interruption is pending for the addressed device.

Errors detected during the execution of a command are reported by a unit check status condition accompanied by a channel end, device end, or controller end status condition, depending upon when the condition was detected. Any errors associated with an operation, but detected after the device end status condition has been cleared, are indicated by generating unit check and attention status.

Termination of an operation with unit check status causes command chaining to be suppressed.

# 2.2.2.8 Unit Exception Status

Unit exception status is generated when the controller or device detects a condition that usually does not occur. It has only one meaning for any particular command and type of device.

Unit exception status can be generated when the device is executing an I/O operation, or when the device is involved with some activity associated with an I/O operation and the condition is of immediate significance to the software.

Unit exception status conditions are normally accompanied by channel end, device end, or controller end status, depending upon when the status was detected.

Termination of an operation with unit exception status causes command chaining to be suppressed.

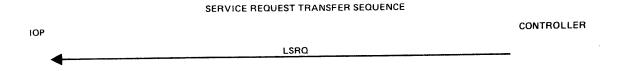
# 2.3 Interface Sequences

There are several interface sequences used by the input/output processor (IOP). These sequences are listed below:

Service request
Parallel poll
Handshake
Addressing
Control signal
Serial poll
Command transfer
Data transfer
Status transfer

#### 2.3.1 Service Request Sequence

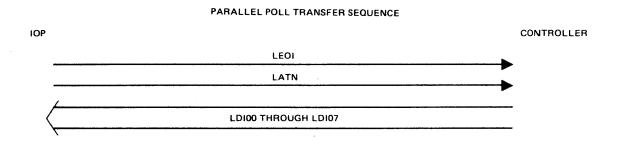
The controller loads the request for service (RSV) bit, status ready (SR) bit (if status is to be transferred), and the device address of the device requesting service into the controller's state register. The byte mode bit (bit 2) must be set if a status transfer is to occur. The multipurpose bus (MP Bus) service request (SRQ) line is then set low. Once the controller is recognized and an information transaction started, the controller is not allowed to set the SRQ line low until the IOP or controller has terminated the information transaction with an end of burst (end or identify) signal. If a status transfer is to occur, the controller loads the device status into the data out register after a serial poll disable (SPD) signal is detected by the controller. The SPD signal indicates the end of a serial poll sequence. A data transfer sequence is then used to obtain device status. The signal flow for the service request transfer sequence is shown below:



# 2.3.2 Parallel Polling Sequence

Parallel polling is used on the MP Bus as the IOPs response to an SRQ from one of the controllers. It determines which controller pair has requested service.

Parallel polling occurs when the controller requires data to be transferred for the input/output command doubleword (IOCD) in progress. The controller sets the MP Bus SRQ line low. The IOP recognizes the SRQ and sets the attention (ATN) and end or identify (EOI) lines low. This action is recognized by all the controllers as the start of the parallel poll operation. The signal flow for the parallel poll transfer sequence is shown below:



The controllers output their assigned priority onto the MP Bus within 300 nanoseconds. The controller's priority is the same as the most significant three bits of its address. The priority on the data lines is received by the IOP and examined as shown in Figure 2-1.

The IOP converts the parallel poll information into 2 of 16 possible controller addresses (the least significant bit of the address is ignored). These addresses are stored in the IOP. The IOP sets the attention and EOI lines high to terminate the parallel poll. Each controller must remove its priority from the MP Bus within 300 nanoseconds after the parallel poll is terminated.

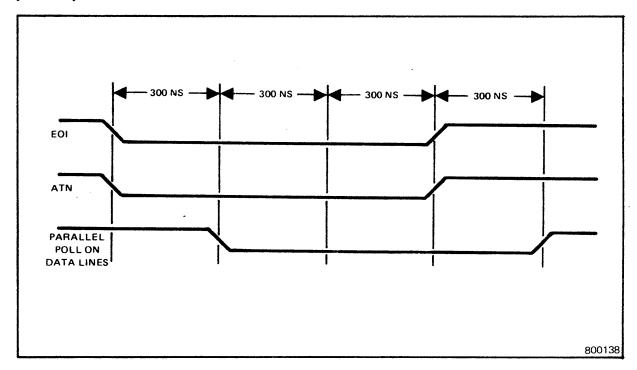


Figure 2-1. Parallel Poll Data Line Priority

# 2.3.3 Handshake Sequence

The handshake sequence is used for all transfers on the MP Bus except for service request (SRQ), parallel poll, and interface clear (IFC). The timing diagram of Figure 2-2 shows two cycles of the three wire handshake sequence. For further information, concerning the timing diagram, refer to the list of events for the handshake process. The signal flow for the three wire handshake sequence is shown below:

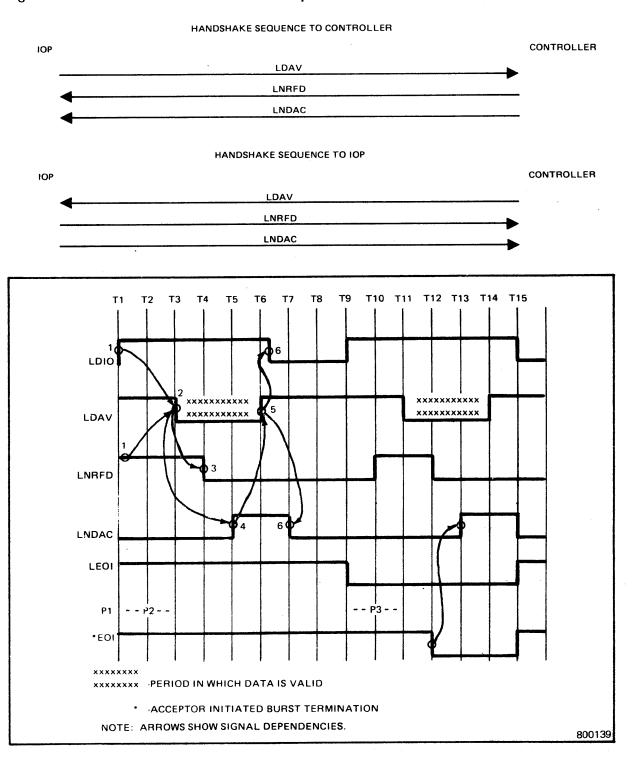


Figure 2-2. Three Wire Handshake Sequence

#### 2.3.3.1 List Of Events For Handshake Process

- P1 The source initializes the data available (DAV) line to high.
- P1 The acceptor initializes the not ready for data (NRFD) line high and sets the no data accepted (NDAC) line low in response to its listen address.
- T1 The source places a data byte on the DIO lines.
- P2 Source delays allowing the data to settle on the DIO lines. Data and parity are on the bus 38 nanoseconds before DAV is set low by the IOP.
- T3 When the data is valid, and the source has second the NRFD line high, the DAV line is set low. DAV must be low true for a minimum of 300 nanoseconds while data is on the MP Bus.
- T4 The acceptor sets the NRFD line low indicating that it is no longer ready. NRFD is low for at least 300 nanoseconds when the IOP has accepted the data.
- T5 The acceptor sets the NDAC line high indicating that it has accepted the data. NDAC must be high on the bus 300 nanoseconds before the IOP will accept the data.
- The source, having sensed that the NDAC line is high, sets the DAV line high. This action indicates to the acceptor that data on the DIO lines is no longer valid. Data remains on the bus 66 nanoseconds after DAV is set high on being outputted by the IOP. Upon completion of this step, one byte of data has been transferred. DAV must be low for 300 nanoseconds to transfer data to the IOP. The IOP examines the data 150 to 300 nanoseconds after DAV is driven low.
- T7 The acceptor, upon sensing the DAV line high, sets the NDAC line low in preparation for the next cycle.
- T9 The source places a new data byte on the DIO lines.
- P3 Source delays to allow the data to settle on the DIO lines.
- T10 The acceptor indicates that it is ready for the next data byte by setting the NRFD line high.
- T11 The source, upon sensing the NRFD line high, sets the DAV line low, thus indicating that data on the DIO lines is valid. The source indicates an end of burst transfer by setting the EOI line low.
- T12 The acceptor sets the NRFD line low indicating that it is no longer ready.
- T13 The acceptor sets the NDAC line high indicating that it has accepted the data. If the acceptor wishes to terminate the transfer it must set the EOI line low during this cycle. EOI should be examined by each controller on the leading edge of NDAC going high.
- T14 The source, having sensed that the NDAC line is high, sets the DAV line low and removes the data byte and EOI after a period of delay. EOI is sampled by the IOP 150 nanosecond after NDAC has gone high to determine if this is the last transfer.

T15 - The acceptor, upon sensing the DAV line high, sets the NDAC line low in preparation for the next cycle. The EOI line must be set high 75 nanoseconds before the next NDAC is set high.

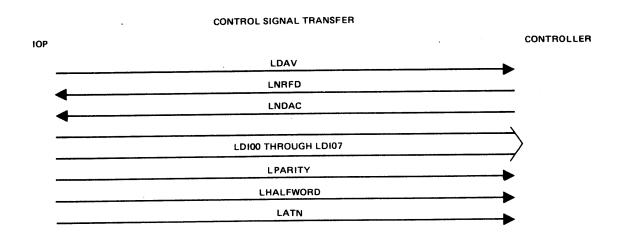
NOTE: All three handshake lines (DAV, NRFD, and NDAC) return to their initialized states. When a controller is not addressed it must not drive any handshake lines on the MP Bus; therefore, all lines are set high when the interface clear (IFC) signal is received.

# 2.3.4 Address Transfer Sequence

The address transfer sequences are listed below:

Addressed talk Addressed listen Untalk Unlisten

The signal flow for the control signal transfer used during an address transfer sequence is shown below:



#### 2.3.4.1 Addressed Talk Sequence

The addressed talk transfer sequence causes a particular controller to enter the transmit mode. After the address state change is recognized by the controller, data, along with the DAV signal, may be placed on the MP Bus.

To transmit data the controller must receive its talk address from the IOP. The talk address format is shown below:

Talk address=0100CCCC
Where CCCC equals the designated controller address.
Bit 4 is the most significant bit (MSB) of the controller address.

The IOP, acting as the talker, places the controller talk address on the MP Bus. The attention line is then set low. The controller receives the address using the three wire handshake sequence and enters the talk mode. The IOP then returns the attention line to the high state and enters the listen mode.

# 2.3.4.2 Addressed Listener Sequence

The addressed listen transfer sequence causes a particular controller to enter the receive mode. Data may be inputted to the controller when the DAV signal is on the MP Bus.

To receive data the controller must first receive its listen address from the IOP. The listen address format is shown below:

Listen address=0010CCCC
Where CCCC equals the designated controller address.
Bit 4 is the MSB of the controller address.

The IOP, acting as the talker, places the controller's listener address on the MP Bus and sets the attention line low. The controller receives the address using the three wire handshake sequence and enters the listen mode. The IOP then returns the attention line to the high state and proceeds to transmit data.

# 2.3.4.3 Untalk Sequence

The untalk transfer sequence removes all controllers on the MP Bus from the talk mode. This control signal, addresses a nonexistent controller to talk, thereby removing all talkers from the MP Bus. No controller should drive any handshake line on the MP Bus.

To terminate the talk mode, the controller must receive the untalk address. The untalk address format is shown below:

Untalk address=01011111 This address places all MP Bus talkers into the untalk mode.

The untalk address is placed on the MP Bus. The attention line is then set low. The controller receives the address using the three wire handshake sequence and stops driving data and handshake lines on the MP Bus. The IOP then sets the attention line high.

#### 2.3.4.4 Unlisten Sequence

The unlisten transfer sequence removes all controllers from the listen mode by adressing a nonexistent controller to listen. This control signal is the only listen signal that removes all listeners from the MP Bus. No controller should drive any handshake line on the MP Bus.

To terminate the listen mode the controller must first receive the unlisten address. The unlisten address format is shown below:

Unlisten address=00111111 This address places all MP Bus listeners in the unlisten mode.

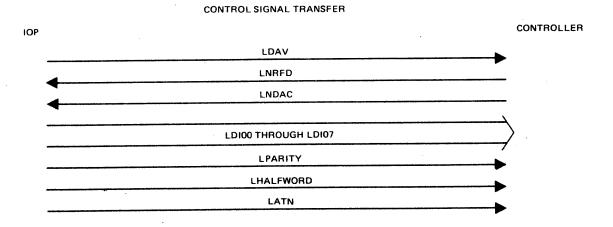
The IOP places the unlisten address on the MP Bus. The attention line is then set low. The controller receives the command using the three wire handshake sequence and no longer drives handshake signals to the MP Bus. The IOP then sets the attention line high. Data is not accepted into the controller after the unlisten sequence.

# 2.3.5 Control Signal Sequence

The control signal transfers are listed below:

Addressed primary control signal sequence Addressed secondary control signal sequence Device address control signal sequence Universal primary control signal sequence

The signal flow for the control signal transfer sequence is shown below:



# 2.3.5.1 Addressed Primary Control Signals

There are four addressed primary control signals used by the IOP:

- End of message (EOM) control signal = 00000000
- 2. Selected controller clear (SCC) control signal = 00000100
- 3. Device clear (DCR) control signal = 00001100
- 4. Execute secondary command (ESC) control signal = 00001111

The EOM sequence is used by the IOP to end a command. The EOM sequence informs a controller that the IOP has sent (output) or received (input) all the necessary data for the I/O operation. This information sent on the MP Bus indicates that the byte count is zero and no data chaining is specified.

The EOM control signal notifies the listening controller that no more data is to be transferred to or from this device. This control signal notifies the controller that SRQ is no longer required for this device. The EOM command signifies the end of an I/O command list (IOCL) for this device where command chaining is not specified.

The SCC control signal informs the controller that a read status transfer (RSTX) reset controller signal has been received by the IOP.

The SCC control signal places a selected controller, and all of its devices, into a predetermined idle state. This control signal provides an immediate clear of all devices on the addressed controller. The SCC control signal is issued in response to a reset controller command to the IOP. The controller is placed in an initialized state so that it will not drive any handshake line on the MP Bus.

The DCR control signal causes a particular device to be placed in a predetermined idle state. This control signal, in conjunction with a halt I/O command, causes an immediate clear of one device on the addressed controller.

The ESC control signal informs a controller that an IOCD command is ready to start for a particular device. Eight bit extended I/O commands are sent from the IOP to a controller as two successive transfers of eight bits (four bits of secondary command and four bits of command). Following the extended I/O command is the device address (four bits of secondary command and four bits of device address).

The ESC control signal notifies the controller that an extended I/O command follows. This mechanism passes all extended I/O commands to the controllers in three MP Bus transfers.

# 2.3.5.1.1 Addressed Primary Control Signal Sequence

The controller must be addressed as a listener to receive addressed primary control signals. Primary control signals are used to reset the controller or device, to terminate an IOCL, or to pass extended I/O commands.

The addressed primary control signal is placed on the MP Bus and the attention line is set low. The controller receives the information using the three wire handshake sequence. Secondary commands may now be sent or the IOP may terminate the control signal sequence. The IOP terminates the control signal mode by setting the attention line high.

# 2.3.5.2 Addressed Secondary Control Signal

The existence and definition of device control commands depends upon the type of devices that are used in the system and the device's specific requirements. These commands are specified by each controller and passed to the controller as addressed secondary control signals.

#### 2.3.5.2.1 Addressed Secondary Control Signal Sequence

Addressed secondary control signals are used to pass the extended I/O commands and device addresses to the addressed controllers. The addressed secondary control signals are decoded by the controller. The format for the addressed secondary control signal is shown below:

Addressed secondary control signal=0111NNNN Where NNNN is a nibble of the extended I/O command. Bit 4 is the MSB of the extended I/O command nibble.

This information is only recognized by the previously addressed controller. The IOP terminates the control signal mode by setting the attention line high.

# 2.3.5.3 Device Address Control Signal

All device addresses are sent to the controller as secondary addressed commands following a primary command.

# 2.3.5.3.1 Device Address Sequence

Since all device addresses are sent as addressed secondary control signals, they must be preceded by an addressed primary control signal. The IOP places the device address on to the MP Bus and sets the attention line low. The IOP terminates the control signal mode by setting the attention line high. The format for the device address is shown below:

Device address=0110AAAA
Where AAAA is the device address.
Bit 4 is the MSB of the device address.

Note that the device address is sent on the MP Bus following all extended I/O commands.

# 2.3.5.4 Universal Primary Control Signal

There are two universal primary control signals used by the IOP: serial poll enable and serial poll disable.

The serial poll enable control signal places all MP Bus controllers into the serial poll mode. Controller state information may then be passed to the IOP when the controller is addressed to talk.

The serial poll disable control signal removes all MP Bus controllers from the serial poll mode.

# 2.3.5.4.1 Universal Primary Control Signal Sequence

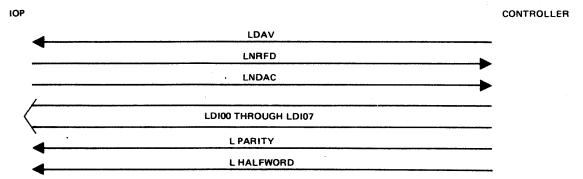
Universal primary control signals are recognized by all controllers on the MP Bus. The control signal is placed on to the MP Bus and the attention line is set low. The IOP terminates the control signal mode by setting the attention line high. These control signals are used to enter and exit the serial poll mode. The format for the universal primary control signals is shown below:

Serial poll enable (SPE) universal control signal=00011000 Serial poll disable (SPD) universal control signal=00011001

#### 2.3.6 Serial Poll Sequence

Serial polling, used by the MP Bus, determines which one, of two possible controllers, has requested service. The lowest addressed controller has priority during the serial poll. Serial polling also obtains the controller's device address and state information after a parallel poll. The signal flow for the state transfer sequence used during a serial poll sequence is shown as follows:

STATE TRANSFER SEQUENCE



# 2.3.6.1 Serial Polling

The serial poll determines which of the two possible controllers is requesting service. The address of the device requesting service is also passed to the IOP during this operation.

The IOP loads the SPE command into the output first-in-first-out (FIFO) buffer. It then places the SPE command on the MP Bus and sets the attention and DAV lines low. When the command is accepted, with the three wire handshake sequence, the controllers are placed into the serial poll mode.

The IOP then places the talk address of controller zero on the MP Bus with the attention and DAV lines set low.

In response to its address the controller places the contents of its state register onto the MP Bus. The contents are received by the IOP using the three wire handshake sequence.

The IOP examines the RSV bit (bit 1) in the controller's state register. If the RSV bit is set, the IOP terminates the serial poll. If the RSV bit is not set, the IOP continues the serial poll for controller one. The RSV bit indicates that this controller set the SRQ line low.

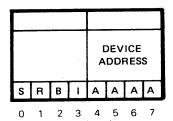
If the RSV bit was not set for controller zero, the IOP places the second controller's talk address on the MP Bus with the attention and DAV lines set low.

The second controller then places the contents of its state register on the MP Bus. The contents are received by the IOP using the three wire handshake sequence.

The IOP once again looks at the RSV bit in the second controller's state register. If the RSV bit is set, the IOP knows this controller has requested service. If the RSV bit is not set, the IOP recognizes that an error has occurred on the MP Bus and reports this error condition to software indicating a bus out status condition.

All controllers must respond with their state information within four microseconds or this information will be ignored. Also a possible bus out status condition may occur.

Controller state information is presented on the MP Bus in the following format:



Bit 0 (status ready) indicates that the controller is ready to present status in the data out register of the controller. Status cannot be loaded into the data out register until the serial poll is terminated.

Bit I (request for service) indicates that this controller has requested service by setting the SRQ line, on the MP Bus, low.

Bit 2 (byte mode) indicates that the transfer requests are to be one byte at a time on bits 0 through 7 of the MP Bus. When this bit is not set, it indicates that a halfword transfer on bits 0 through 15 is requested. Commands and termination status are always passed as bytes on bits 0 through 7. A controller may receive a byte on the last transfer in the halfword mode, if the IOCD contains an odd byte count.

Bit 3 (long block) indicates that more input data, in the controller, must be transferred. This indication, with status ready, causes incorrect length status to be posted.

Bits 4 through 7 (device address) are the address of the device on the controller that is requesting service. Bit 4 is the MSB.

The IOP outputs the untalk control signal along with the DAV signal to terminate the talk mode.

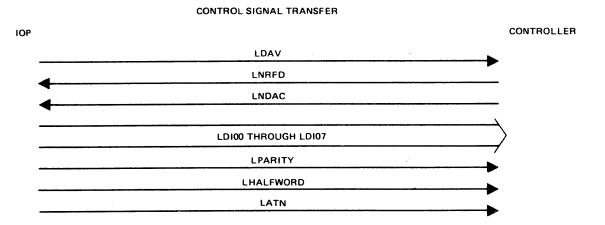
The IOP then loads the serial poll disable control signal into the MP Bus and sets the attention and DAV lines low. All controllers now exit the serial poll mode. The three wire handshake sequence is then completed.

# 2.3.7 Command Transfer Sequence

The command transfer sequences are listed below:

Addressed listen
Enable secondary command
Extended I/O command, most significant nibble (MSN)
Extended I/O command, least significant nibble (LSN)
Addressed device
Addressed unlisten

The signal flow for the control signal transfer used during the command transfer sequence is shown below:



# 2.3.7.1 Addressed Listen Sequence

To transfer a command the controller must receive its listen address from the IOP. The listen address format is shown below:

Listen address=0010CCCC

Where CCCC equals the designated controller address.

Bit 4 is the MSB of the controller address.

The IOP, acting as a listener, places the controller's listen address on the MP Bus and sets the attention line low. The controller receives the address, using the three wire handshake sequence, and enters the listen mode. The IOP then returns the attention line to the high state and enters the talk mode.

#### 2.3.7.2 Enable Secondary Command Sequence

The ESC control signal notifies the controller, via the three wire handshake sequence, that an extended I/O command follows. The ESC format is shown below:

ESC=00001111

This mechanism passes all extended I/O commands to the controllers.

# 2.3.7.3 Extended I/O Command Most Significant Nibble

The first nibble of the extended I/O command is sent to the addressed controller where it is decoded. The controller receives the extended I/O command using the three wire handshake sequence. The format for the extended I/O command most significant nibble (MSN) is shown below:

2-17

Extended I/O command MSN=0111NNNN Where NNNN is the MSN of the extended I/O command. Bit 4 is the MSB of the extended I/O command nibble.

# 2.3.7.4 Extended I/O Command Least Significant Nibble

The second nibble of the extended I/O command is sent to the addressed controller where it is decoded. The controller receives the extended I/O command using the three wire handshake sequence. The format for the extended I/O command least significant nibble (LSN) is shown below:

Extended I/O command LSN=0111NNNN
Where NNNN is the LSN of the extended I/O command.
Bit 4 is the MSB of the extended I/O command nibble.

This information is also recognized by the previously addressed controller.

# 2.3.7.5 Addressed Device Sequence

All device addresses are sent as addressed secondary control signals and, therefore, must be preceded by an addressed primary control signal. The IOP places the device address on the MP Bus and sets the attention line low. The format for the device address is shown below:

Device address=0110AAAA
Where AAAA is the device address.
Bit 4 is the MSB of the device address.

This address is then sent on the MP Bus following the extended I/O command LSN sequence.

# 2.3.7.6 Addressed Unlisten Sequence

To terminate the listen mode the controller must first receive the unlisten address. The format for the unlisten address is shown below:

Unlisten address=00111111
This address places all MP Bus listeners in the unlisten mode.

The IOP places the unlisten address onto the MP Bus and sets the attention line low. The controller receives the command using the three wire handshake sequence and no longer receives data from the MP Bus. The IOP then terminates the command mode by setting the attention line high. After the unlisten sequence is initiated, no controller is allowed to drive any of the handshake lines.

# 2.3.8 Data Transfers

A MP Bus transfer is initiated by the IOP using a primary control signal, or by the controller using a SRQ sequence and setting the attention status bit. Attention status is reported to the software by the IOP via a software interrupt. Software may then send a command to this device using a primary control signal transfer.

Data is transferred on the MP Bus by 'talkers' and 'listeners'. The talker drives data and the DAV signal on the MP Bus. The listener receives data from the MP Bus and drives the NRFD and NDAC signals onto the MP Bus to complete the three wire handshake sequence.

The previous step is repeated until the last byte of data in the burst is loaded on the MP Bus and accepted by the listener. Only one talker and one listener may access the bus at any one time.

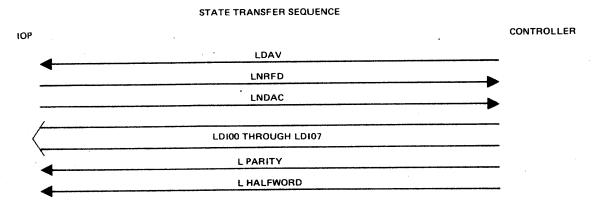
The last byte of data and the EOI indication is then placed on the MP Bus. The data is received using the three wire handshake sequence. The end of a burst data transfer sequence is normally indicated by the controller pulling the EOI line active with the last byte of data transferred, or by the IOP pulling the EOI line active when the byte transfer count is exhausted. The controller may also set the EOI line active to indicate an end of transfer when the currently controlled device abnormally goes out of service, or when a termination sequence is detected at the controller. The controller then accumulates the device status and sets the status ready bit (bit 0) in the controller state register. The SRQ line is then set and a status transfer occurs.

Data on the MP Bus, along with a low true parity bit (LPARITY) and a low true halfword (LHALFWORD) signal, is sent to the listening device. The LHALFWORD signal notifies the listening device that a halfword (16 bits) or a byte (8 bits) is on the MP Bus. The LPARITY signal is calculated from the number of bits driven on the IOP (8 bits if LHALFWORD is high or 16 bits if LHALFWORD is low). The LPARITY signal generates odd parity on the MP Bus. The signal flow for the data transfer sequence to the controller/IOP is shown below:

# DATA TRANSFER TO CONTROLLER IOP CONTROLLER LDAV LNRFD LNDAC LDI00 THROUGH LDI07 **OPTIONAL LDI08 THROUGH LDI15** LPARITY LHALFWORD LEOI (LAST TRANSFER ONLY) DATA TRANSFERS TO IOP IOP CONTROLLER LDAV LNRFD LNDAC LDI00 THROUGH LDI08 **OPTIONAL LDI08 THROUGH LDI15** LPARITY LHALFWORD LEOI (LAST TRANSFER ONLY)

# 2.3.9 Status Transfer Sequence

Status transfers normally occur as a data transfer sequence, following the parallel poll, which is initiated by a SRQ from a controller. Status is read from the data out register on the controller when the SR state bit is set in the serial state register. However, the software may obtain a device status report, using the extended I/O sense command from a controller supporting this command, and transferring the required status. The signal flow for the state transfer sequence used during the status transfer sequence is shown below:

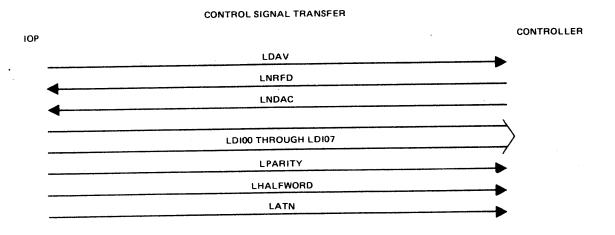


The state transfer sequence is followed by a data transfer sequence that contains device and status information.

# 2.3.10 Termination by End Of Message Sequence

The end of message (EOM) control signal is an addressed primary control signal that is sent when a SIO command has terminated. The IOP sends this command, along with the device address, to the controller.

The EOM control signal is placed onto the MP Bus and the attention line is set low. The controller receives the control signal using the three wire handshake sequence. The IOP then sets the attention line high. The signal flow for the control signal transfer used during the EOM sequence is shown below:



The EOM requests that the status transfer sequence be performed by the controller. The SQR sequence is then entered. The SR bit is sent to the IOP during the serial poll. The IOP then reads termination status from the controller. After the status transfer sequence is completed, the controller no longer sets the SRQ line low (for this particular device) until a new extended I/O command is received for that device. The EOM control sequence is shown below:

- 1. Addressed listen
- 2. EOM sequence
- 3. Addressed device
- 4. Addressed unlisten

A controller may also terminate a transfer by sending termination status to the IOP. The IOP responds by posting termination status to software.

#### 2.3.11 Reset

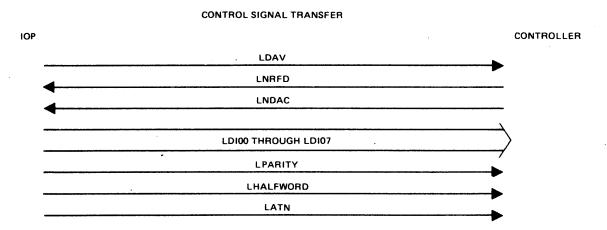
There are three types of resets used on the MP Bus: The selected controller clear (SCC), device clear (DCR), and interface clear (IFC).

## 2.3.11.1 Selected Controller Clear Sequence

The SCC sequence clears all devices on a particular controller by placing them in a predetermined idle state. This sequence is generated by software via a controller reset instruction. The selected controller no longer drives control signals or data on the MP Bus after the SCC sequence. The format for the SCC sequence is shown below:

- 1. The addressed listen sequence addresses the controller as a listener.
- 2. The addressed primary control signal sequence sends the SCC command.
- 3. The unlisten sequence removes this controller from the MP Bus.

The signal flow for the control signal transfer used during the SCC sequence is shown below:

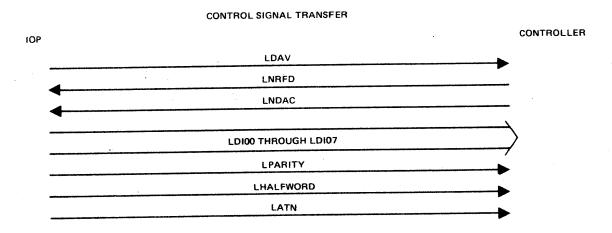


## 2.3.11.2 Device Clear Sequence

The DCR sequence clears any device, on any controller, on the MP Bus by placing it in a predetermined idle state. This sequence is generated by software via a halt I/O command. The format for the DCR sequence is shown below:

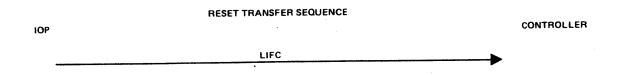
- 1. The addressed listen sequence addresses the controller as a listener.
- 2. The addressed primary control signal sends the device clear (DCR) command.
- 3. The addressed secondary command sequence sends the device address-0110AAAA, where AAAA is the device address.
- 4. The unlisten sequence removes this controller from the MP Bus.

The signal flow for the control signal transfer used during the DCR sequence is shown below:



## 2.3.11.3 Interface Clear Sequence

All controllers must recognize the interface clear (IFC) signal as the IOP reset signal. The IOP sets the IFC line active (low) during system reset. All controllers then clear their devices to a steady state condition. The IFC line is also set low when a hardware reset, a write data, or order transfer (WDOT) is detected on the SelBUS. The IFC line remains low for at least one microsecond. No controller drives data or control signals onto the MP Bus after this line is set low. The signal flow for the reset transfer sequence used during the IFC sequence is shown below:



### 2.4 General System Considerations

#### 2.4.1 Interface Timeout

The interface timeout timer is started at the beginning of the read/write burst, and reset by the end or identify (EOI) signal. If a burst is not completed within 537 microseconds, the timer initiates the highest level interrupt. This interrupt routine forces an EOI signal to the input/output processor (IOP) with the next data transfer, thus terminating the burst without loss of data. If the EOI signal does not clear the bus by the second timeout (another 537 microseconds), an interface clear (IFC) signal clears the bus and reports bus out status for the addressed subchannel to the software.

#### 2.4.2 Burst Length

A minimum of one transfer is required for each burst since the EOI signal can only be set with a data transfer. The maximum burst length is controlled by the interface timeout signal and the throughput of each controller. It is suggested that the burst length be as long as possible (at least 32 transfers) to minimize bus overhead and maximize data throughput. Transfers of smaller burst size will seriously affect the total bus throughput and may cause overruns.

## 2.4.3 Control Signal Timing

Each controller must respond to a serial poll within four microseconds or the serial poll is either ignored, or bus out check status is reported to the software. Tables 2-3 and 2-4 show the control signal pulse widths and IOP handshake timing pulse widths, respectively.

Table 2-3
Control Signal Pulse Widths

Control Signal	Pulse Widths		
DAV	≥ 300 ns		
NDAC	≥ 300 ns		
NRFD	≥ 300 ns		
IFC	≥ 1 µ s		

Table 2-4
IOP Handshake Timing Pulse Widths

IOP Handshake Timing	Direction of Transfer	Pulse Widths
DIO to DAV ↓	Out	≥38 ns
DAV † to DATA	Out	≥66 ns
NDAC † to DAV †	Out	≤240 ns
DAV ↓ to NDAC1	In	≤450 ns
DAV ↓ to NRFD ↓	In	≤575 ns
DAV to NDAC	In	≤375 ns
DAV I to DIO	In .	≤225 ns

#### Notes:

- 1. All signals are low true.
- 2. I indicates that the signal is going low.
- 3. † indicates that the signal is going high.
- 4. (Out) indicates that the signal is going out on the MP Bus.
- 5. (In) indicates that the signal is coming from the MP Bus.

## 2.5 Input/Output Processor Features

## 2.5.1 Parity Error Reporting

Data transferred from the controller to the input/output processor (IOP), via the multipurpose bus (MP Bus), is accompanied by a parity bit. Parity errors from the MP Bus cause interface check status to be sent to software within the eight bits of IOP status information. Data errors from the IOP, received by the controller, cause the unit check bit of the controller's status information to be set. This status is reported to the IOP during a status transfer on the MP Bus.

#### 2.5.2 Multipurpose Bus Timeout

The multipurpose bus (MP Bus) timeout insures that no one controller occupies the MP Bus for more than 537 microseconds. The MP Bus timer is initiated at the beginning of the read/write burst and is reset by the end or identify (EOI) signal. If an MP Bus data burst is not completed within 537 microseconds, an interrupt (of the highest level) is generated. This interrupt routine forces an EOI signal on the MP Bus with the next data transfer. A second timeout interrupt causes an interface clear (IFC) sequence to be initiated and bus out check status to be transferred to the software. The IFC sequence clears the MP Bus and returns all controllers to an idle state. Note that all I/O operations must be restarted after an IFC sequence.

#### 2.5.3 IOP Inhibit

The IOP inhibit feature allows another device to access the MP Bus without using the IOP. When the inhibit line is set low, the IOP is removed from controlling the MP Bus. However, the IOP will receive data from the MP Bus. This line must only be used as a static access to the MP Bus (i.e., no controller can be operating at the time that the inhibit line is pulled low).

## 2.5.4 Halfword or Byte Transfer

The halfword or byte transfer feature notifies the receiver that a halfword or byte data transfer is on the MP Bus. This feature is activated via the LHALFWORD I/O data line. When this line is high a byte (eight bits) transfer is on the MP Bus. A low signifies that a halfword (16 bits) is on the MP Bus. Parity is generated and checked according to this line. Eight bit odd parity is generated when the line is high and 16 bit odd parity is generated when the line is low.

## 2.5.5 Timing Signals

The IOP utilizes two timing signals: 150 nanosecond and 5.0688 megahertz. The 150 nanosecond timing signal is used for all primary synchronization. The 5.0688 megahertz timing signal is generated by the IOP, used by the communications controllers, and driven onto the MP Bus. Note that the 5.0688 megahertz signal is not removed from the MP Bus by the inhibit line.

#### **CHAPTER 3**

#### **ELECTRICAL SPECIFICATIONS**

## 3.1 Physical Requirements

There can be a maximum of 16 controllers on the multipurpose bus (MP Bus). Each controller can have up to 16 devices, provided the total number of devices per MP Bus does not exceed 124. These controllers can be located up to 20 feet away from the IOP. Each MP Bus must be terminated by a bus terminator (part number 160-103449). The maximum throughput rate is 1.5 megabyte.

## 3.2 Electrical Requirements

A 4 milliampere per line load is allowed on the MP Bus. MP Bus drivers must supply 300 mA at 5 volts and provide an interface to an open collector bus. The 75453 or equivalent line drivers are suggested for the MP Bus.

The electrical characteristics for the 75453 bus drivers are shown in Figure 3-1.

## 3.2.1 Cable Type

The IOP requires a 50 pin flat ribbon cable (part number 144-103045) not to exceed 20 feet in length. The MP Bus cable has two flat ribbon cable connectors (one on each end). Cable signals are specified under cable requirements.

# 3.2.2 Terminating Networks

The IOP is terminated using a terminating board with 240 ohm pull-up and 360 ohm pull-down resistors. The 240 ohm pull-up resistors are connected up to +5 volts and the 360 ohm pull-down resistors are connected to ground. The terminator board must be connected to the end controller slot on the MP Bus. Only one terminator board is used per MP Bus.

# 3.3 Interface Circuit Requirements

The MP Bus uses Schottky TTL, TTL, or LSTTL receivers and 75453 drivers. Other receivers or drivers may be used if they meet the threshold and switching time requirements specified in the electrical requirements section.

## 3.4 Typical Interfacing Circuit

An example of a typical interfacing circuit for Z80 controllers is shown in Figure 3-2.

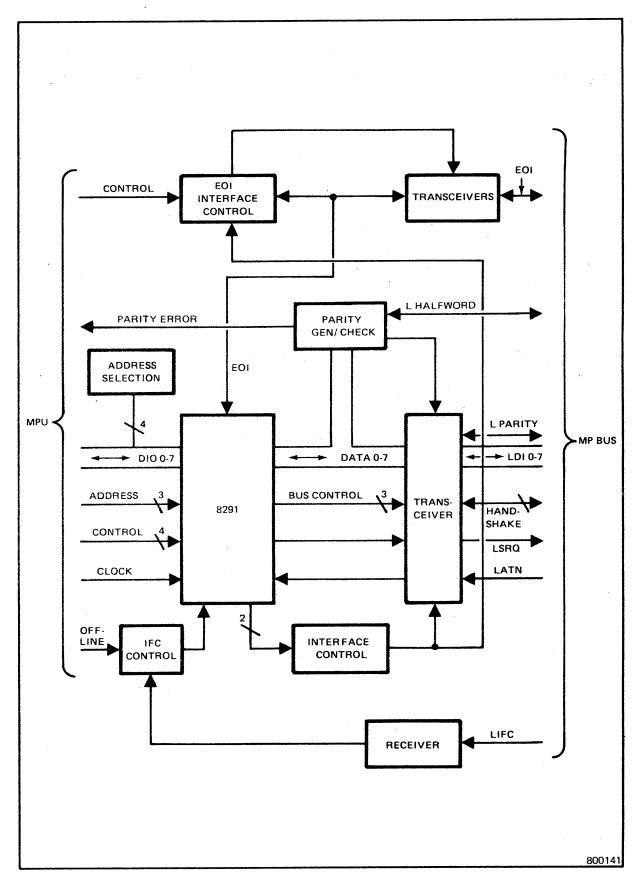


Figure 3-1. 75453 Electrical Characteristics

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted).

Supply voltage, V <sub>CC</sub> (see Note 1)	7∨
Input voltage	5.5V
Inter-emitter voltage (see Note 2)	5.5V
Output voltage (see Note 3)	30V
Output current (see Note 4)	300mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	800mW
Operating free-air temperature range.	0 to 70°C
Storage temperature	-65 to 150°C
Load temperature 1/16 inch from case for 10 seconds	260°C

#### NOTES:

- Voltage values are with respect to network ground terminal unless otherwise specified.
- This is the voltage between two emitters of a multiple-emitter transistor.
- This is the maximum voltage which should be applied to any output when it is in the off state.
- Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
- This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air R CA, of not more that 95°C/W.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IH</sub>	High-level input voltage			2			٧
VIL	Low-level input voltage					0.8	>
v <sub>i</sub>	Input clamp voltage	V <sub>CC</sub> = 4.75	I <sub>1</sub> = -12mA			1.5	٧
Юн	High-level output current	V <sub>CC</sub> = 4.75V V <sub>DH</sub> = 30V	V <sub>IH</sub> = 2V			100	μΑ
<b>v</b> oL	Low-level output voltage	V <sub>CC</sub> = 4.75V i <sub>OL</sub> = 100mA	V <sub>IL</sub> = 0.8V		0.25	0.4	v
		V <sub>CC</sub> = 4. 75	V <sub>1L</sub> = 0.8V		0.5	0.7	V
	Input current at max. input voltage	V <sub>CC</sub> = 5.25V	V <sub>I</sub> = 5.5V			1	mA
i <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5.25V	V <sub>1</sub> = 2.4V			40	μА
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = 5.25V	V <sub>I</sub> = 0.4V		-1	-1.6	mA
ССН	Supply current, outputs high	V <sub>CC</sub> = 5.25V	v <sub>1</sub> = 5V		8	11	mA
CCL	Supply current, outputs low	V <sub>CC</sub> = 5.25V	V <sub>I</sub> = 0		54	68	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

800140

Figure 3-2. Simplified Block Diagram of a Typical IOP Interface Circuit for Z80 Controllers

### **CHAPTER 4**

## SIGNAL CABLING AND CONNECTIONS

# 4.1 Cable Requirements

The multipurpose bus (MP Bus) cable connections are shown in Table 4-1. This cable is the 50 pin cable specified in Chapter 3.

Table 4-1 MP Bus Cable Connections

J9-MP Bus Connection	Controller Backplane Connection	Signal	J9-MP Bus Connection	Controller Backplane Connection	Signal
J9-01 J9-02 J9-03 J9-04 J9-05 J9-06 J9-07 J9-08 J9-09 J9-10 J9-11 J9-12 J9-13 J9-14 J9-15 J9-16 J9-17 J9-18 J9-17 J9-18 J9-19 J9-20 J9-21 J9-22 J9-23 J9-24	P1-143 P1-144 P1-145 P1-146 P1-147 P1-148 P1-149 P1-150 P1-151 P1-152 P1-153 P1-155 P1-155 P1-156 P1-157 P1-158 P1-159 P1-160 P1-161 P1-162 P1-163 P1-163 P1-164 P1-165	GND L150NSCLK GND LATN GND LDAV GND LEOI GND LPARITY GND LSRQ GND LHALFWORD GND LIFC GND L5.0688MHZ GND LDI00 LDI01 GND LDI02 LDI03	J9-26 J9-27 J9-28 J9-29 J9-30 J9-31 J9-32 J9-33 J9-34 J9-35 J9-36 J9-37 J9-38 J9-39 J9-40 J9-41 J9-42 J9-43 J9-42 J9-43 J9-44 J9-45 J9-46 J9-47 J9-48 J9-49	P1-168 P1-169 P1-170 P1-171 P1-172 P1-173 P1-175 P1-176 P1-177 P1-178 P1-179 P1-180 P1-181 P1-182 P1-183 P1-184 P1-185 P1-186 P1-187 P1-188 P1-189 P1-190 P1-191	LDI04 LDI05 GND LDI06 LDI07 GND LDI08 LDI09 GND LDI11 GND LDI12 LDI13 GND LDI14 LDI15 GND LNRFD GND LNRFD GND LNRFD GND LNHIBIT GND
J9-25	P1-167	GND	J9-50	P1-192	SPARE

#### APPENDIX A

#### **GLOSSARY**

AAAA (device address) - The address of a specific device used with the IOP.

AICT (advance interrupt control transfer) - One of the bus transfer signals.

ARSTX (advance read status transfer) - One of the bus transfer signals.

ATN (attention) - This output signal, driven by the IOP, causes all controllers on the MP Bus to listen. The ATN signal is active low when the IOP wants to send addresses, commands, or control signals. It is also used with EOI active low to initiate a parallel poll.

B (byte mode) - See BM.

BM (byte mode) - This bit of data is state transfer information indicating that a transfer is requested in the eight-bit mode.

CCCC (controller address) - A designated controller address.

DAC (data accepted) - This signal is driven true (high) each time data is accepted from the MP Bus. The DAC signal may be driven by the IOP or any listening controller.

DAV (data available) - This signal is controlled by the interface circuitry and driven true (low) each time data is placed on the MP Bus. The DAV signal may be driven by the IOP or any talking controller.

DCR (device clear) - This control signal places a particular device, on a particular controller, into a predetermined idle state.

EOI (end or identify) - This signal is set true (low) by the IOP or a controller to notify the listener that the last byte of data for the burst is on the MP Bus. It may be set by the IOP or a controller that is in the talk or listen mode. It is also used to notify a controller that it has exceeded the 537 microsecond time allowed on the MP Bus and, as a result, the burst terminates.

EOM (end of message) - This IOP control signal terminates an IOCD. A status transfer is requested following this control signal.

ESC (enable secondary command) - This IOP control signal notifies the controller that the next two bytes of information on the MP Bus are extended I/O commands. The third byte of data is the device address of the specified command.

GPIB (general purpose instrument bus) - An interface chip used to simplify controller interface design, maintain low IC count, and employ a well established bus protocol.

I (incorrect length) - This signal indicates that more input data in the controller must be transferred. This signal, along with status ready, cause incorrect length status to be posted.

IFC (interface clear) - This signal causes all MP Bus controllers and devices to go into a predetermined state.

IOCD (input/output command doubleword) - A doubleword generated by the CPU firmware to command a device controller.

IOCL (input/output command list) - One or more IOCDs arranged in sequential order.

IOP (input/output processor) - A unit that can command the MP Bus functions that connect to the SelBUS.

LATN (low true attention) - See ATN.

LCLK (150 ns clock) - This bus clock signal is used for all primary synchronization.

LDAV (low true data available) - See DAV.

LDIXX (low true device interface XX) - The device interface bus, data, address, and command lines.

LEOI (low true end or identify) - See EOI.

LHALFWORD (low true halfword) - This signal notifies the receiver, on the MP Bus, that a 16 bit transfer is on the MP Bus.

LINHIBIT (low true inhibit) - This signal removes the IOP from control of the MP Bus.

LIFC (low true interface clear) - See IFC.

LNDAC (low true no data accepted) - See NDAC.

LNRFD (low true not ready for data) - See NRFD.

LPARITY (low true parity) - A signal sent with all data transfers on the MP Bus. Parity is always odd, low true, generated, and checked on either 8 or 16 bits, depending upon the state of the LHALFWORD signal.

M (modifier) - A bit which is defined by each controller.

MP Bus (multipurpose bus) - An element of the IOP.

NDAC (no data accepted) - This signal is controlled by the receiving circuitry and remains true (low) until after the listener has clocked the MP Bus data into its data in register.

NNNN (nibble) - A nibble of the extended I/O command.

NRFD (not ready for data) - This signal is controlled by the receiving circuitry and remains true (low) until after the listeners data in register has been cleared. This signal prohibits the overrun of the last data byte in the interface.

R (request for service) - See RSV.

RSTX (read status transfer) - One of the bus transfer signals.

RSV (request for service) - Controller state information indicating that a particular controller has requested service by pulling the SRQ line low on the MP Bus.

S (status ready) - See SR.

SCC (selected controller clear) - This control signal places a controller and all of its devices into a predetermined IOP state.

SCP (system control panel) - An element of the IOP.

SPD (serial poll disable) - A universal primary control signal used to exit the serial poll mode.

SPE (serial poll enable) - A universal primary control signal used to enter the serial poll mode.

SR (status ready) - Bit 0 in the state register which informs the IOP, during a serial poll, that a device has status for the IOP.

SRQ (service request) - This signal is set true (low) by any controller to notify the IOP that the controller is ready to transfer information.

WDOT (write data or order transfer) - A command used to initiate or halt operations within the IOP.

5.0688 MHz clock - This clock signal is used by communications controllers, generated by the IOP, and driven onto the MP Bus. The inhibit line does not effect this freerunning clock.

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