SHUGART ASSOCIATES

ENGINEERING SPECIFICATION

CODE	PART NO.	REV EC
ES	30127-0	

SHEET 1 OF 24

TITLE SA 1000 CONTROLLER

SHUGART SA1400 CONTROLLER

TABLE OF CONTENTS

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1.0 Introduction

The SA-1400 Controller consists of a microprocessor based controller with on-board data separator logic able to control up to four drives. The drives can be any combination of Shugart SA-1000 fixed disk drives and SA-850 floppy disk drives. The SA-1400 can be mounted on the SA-1000 drive.

Commands are issued to the controller over a bidirectional bus connected to the host computer. The data separator/ "serdes" logic serializes bytes and converts to MFM data, and deserializes MFM data into 8 bit bytes.

Due to the microprogrammed approach utilized in the controller, extensive diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media imperfections up to 4 bit burst error.

2.0 SA-1400 Controller

2.1 Features

2.1.1 The capabilities supplied as standard with the SA-1400 are listed below:

Overlapped Seek ** In multiple drive configurations the host

can issue seeks to different drives without waiting for the first drive to complete its seek.

Automatic Seek and verify ** A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.

Fault Detection ** Two classes of faults are flagged to improve error handling.

* Controller faults
* Disk faults

Automatic Head and Cylinder Switching ** If during a multi-block data transfer the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.

Data Error Sensing and Correction ** If a data error is detected during a disk data transfer, the controller indicates whether or not it is correctable. If correctable, a pointer and mask can be

requested by the host for applying the correction or the error can be automatically corrected.

Logical to Physical Drive Correlation	** Logical Unit Number (LUN's) are independent of physical port numbers. All accesses specify LUN's.
On Board Sector Buffer	** A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.
Efficient Host Interface Protocol	** A bidirectional bus between the controller and host provides a simple yet effecient communication path. In addition, a high level command set permits effective command initiation.
Sector Interleave	** Sector interleaveing is programable with up to 16 way interleave.
Odd Parity	** The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
Fixed Sector Size	** The sector size is fixed at 256 bytes.

Number of Drives

** The controller will connect to a maximum of two (2) (optionally) drives. The drives can be any combination of SA-1ØØØ's and/or SA-85Ø's.

2.1.2 The capibilities available as options are listed below:

Multiple Host

** Up to 7 host computers may be connected to the controller.

Micro Diagnostics

** An on board set of diagnostics are initiated by a set of switches on the controller. A loopback cable is available to facilitate off line testing of the controller. A complete set of drive diagnostics is also available.

Variable Sector Size

** Sector sizes other than 256 bytes are available.

Additional Drive Poarts

** Up to four (4) drive(s) can be attached to the SA-1400.

2.2 System Configuration

The controller and data separator comprise a single PCB that can be mounted onto the SA-1000 drive. Up to

four drives may be connected as shown in fig. 2.1.

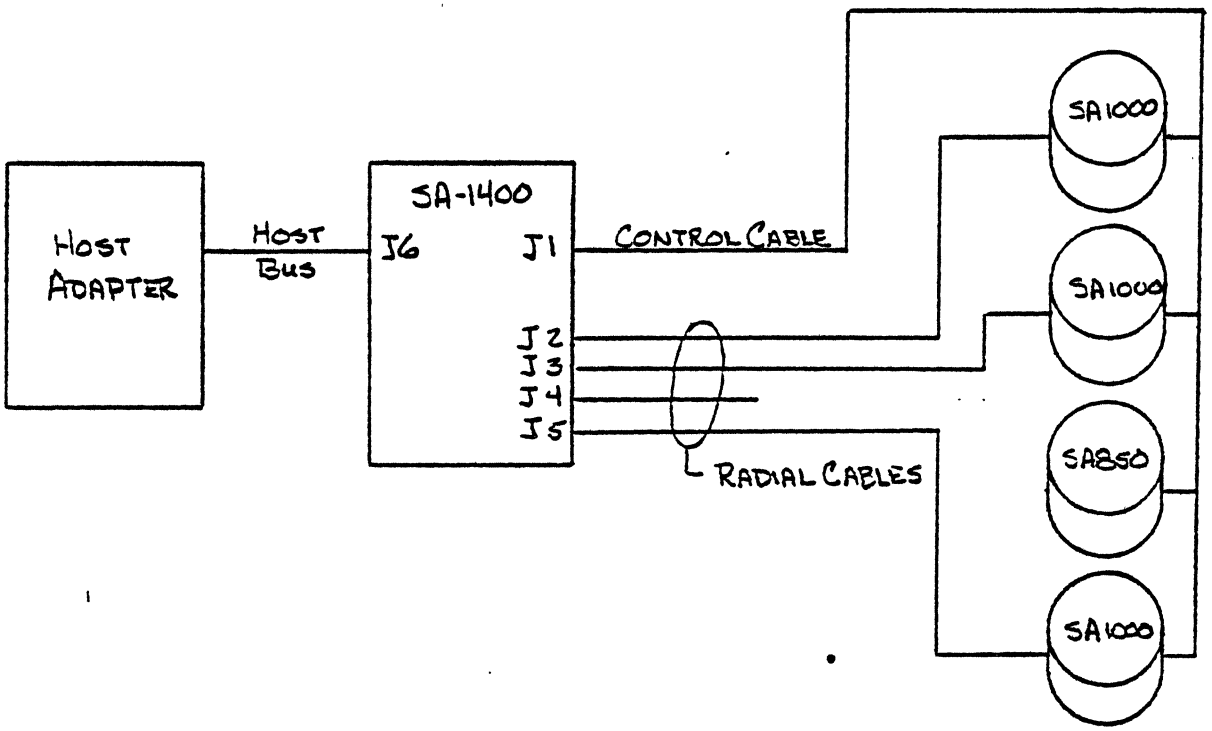


Fig. 2.1

2.3 Theory of Operation

Disk commands are issued to the SA-1400 via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (command structure is described in 4.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command the controller will send completion status to the host. (Further delineation of the completion status may be requested by issuing the appropriate sense commands.)

Odd parity is generated by the SA-1400 for all information that it puts on the I/O bus. If enabled, the SA-1400 flaggs all information that it recieves with bad parity.

2.3.1 Electrical Interface

The electrical interface to the SA-1000 will conform to the specification described in the SA-1000 interface specification.

3.0 Bus

The electrical interface to the SA-1400 host bus is shown in Fig. 3.1.

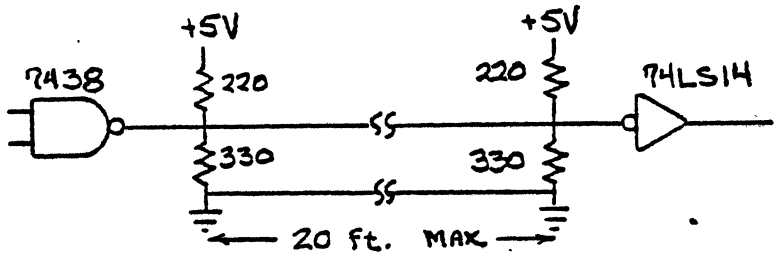


FIGURE 3.1

The bus consists of data and control lines and is designed to accomadate a multi-host and multi-controller enviroment. The data lines are bidirectional and nine bits wide. (8 bits data and 1 bit parity) Control of the bus is achieved by a simple algorithm described below. Bus transactions take place under control of a simple Request/Acknowledge protcol which uses the data "direction" and "type" lines. The bus is released after a transaction is completed. The signals on the bus when asserted are at ØVDC to Ø.4VDC and when deasserted or inactive at 2.5VDC to 5.25VDC.

3.1 Bus Signal Definations

I/O Bus direction control line. (assert=input into host adaptor, deassert=output from host adaptor.)

C/D Specify the type of data (assert = control deassert = data) on the bus.

REQ Request for data transfer. Driven by controller.

ACK Acknowledge byte transfer complete. Driven by host adaptor.

BSY Bus busy. When asserted means that the bus is in use and not available.

MSG Message. Command is complete.

RST Reset the controller.

SEL Selects the controller. Driven by the host adaptor.

DB(7-Ø,P) Nine bidirectional lines. Eight data lines and one parity. the parity is optional and need not be checked.

3.2 Theory of Operation (for a single-host system)

Whenever the host adaptor has a command for the controller it performs a selection sequence to gain the attention of the controller. The sequence is as follows:

The host adaptor causes the SEL line and the controller address bit (DB-Ø) on the host bus to become asserted. The host adaptor then waits

for the controller to respond with BSY. After the controller asserts BSY it (the controller) then asserts C/D (to indicate control mode transfer) and deasserts I/O (to indicate output from the host adaptor) to transfer the command bytes to the controller. The command bytes are transfered over the host bus with the REQ/ACK handshake protocol. The last REQ/ACK handshaking is done and all bytes of the command have been transferred to the controller.

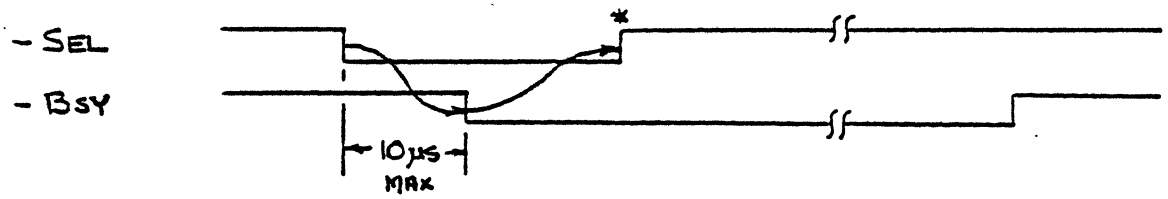
For data transfer the controller deasserts the the C/D line to indicate data. Depending on the command type (read/write disk) the I/O bit on the host bus is asserted or deasserted by the controller, and the data is transferred (a byte at a time) with a Request/Acknowledge interlocked handshake protocol. After all the data has been transferred, the completion status is placed on the bus by the controller, C/D an I/O are asserted. REQ is asserted and the controller waits for ACK from the host adaptor. After the status byte transfer the controller places zeros on the bus and asserts C/D, I/O and MSG along with REQ to indicate to the host that the command is complete. After the message is

transferred the controller deasserts BSY and all other lines. This completes the command execution and the controller is now ready to be selected for the next command.

3.2.1 Timing Diagrams for Device Selection

Note that the signals on the host bus are low true. Hence the wave forms are drawn as low true signals.

* SEL must be deasserted before assertion of REQ, I/O and C/D.



3.2.2 Timing Diagram for Data Transfer Protocol

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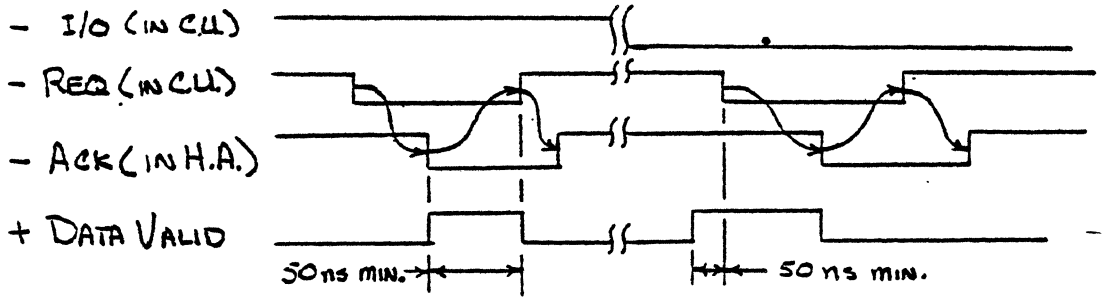


When the data transfer is to the controller, the controller will wait 50ns or more after

ACK and then takes the data on the host bus. Data will remain valid until REQ is deasserted. When the data transfer is to the host adaptor, the controller shall guarantee that the data to the host is valid 50ns before REQ is asserted and remains valid until ACK is asserted.

4.0 Commands

An I/O request to a disk drive is performed by passing a Command Descriptor Block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, number of blocks to transfer or the destination device ID. The controller performs an implied seek and verify when required to access a block.

Commands are categorized into three classes as indicated:

Class Ø - Non-data transfer, data transfer and status commands

Class 1 - Disk copy commands

Class 2-6 - Unused

Class 7 - Diagnostic commands

The command descriptor blocks incommand class Ø and 7 are 6 bytes long and those in class 1 are 10 bytes long.

Command Description (Class Ø)

Opcode (Hex)	Description
00	Test Drive Ready - Selects the drive and verifies drive ready.
01	Recalibrate. Positions the R/W arm to track 00, clears possible error status in the drive.
02	Request Syndrome. Returns 2 bytes of offset and syndrome for data error correction. The two bytes are as follows:

BYTE Ø	M.S. BIT OFFSET (8)		
BYTE 1	L.S. BIT OFFSET (3)	Ø	SYNDROME (4)

The bit offset is relative from the 1st data bit. ie., bit 7 of byte Ø.

03	Request Sense. Returns 4 bytes of drive and controller sense for the specified LUN. (refer to 4.2.2 and copy block for an execption.) Request Sense must be issued immediately after an error to be valid.

04 Format Drive. Formats all blocks with ID field according to interleave factor and data fields. The data field contains 6C HEX.

05 Check Track Format. Check format on the specified track for correct ID and interleave. Does not read the data field.

06 Format Track. Formats the specified track with bad block flag cleared in all blocks of that track. Writes 6C HEX in the data fields.

07 Format Bad Track (bad block flag). Formats the specified track with bad block flag set in the ID fields. Writes 6C in the data fields.

08 Read. Reads the specified number of blocks starting from initial block address given in the CDB.

0A Write. Writes the specified number of blocks starting from initial block address given in the CDB.

0B	Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drives capable of overlap seek.

Command Description (Class 1)

Opcode (HEX)	Description
00	Copy Block. Copies a specified number of blocks from the source LUN to the destination LUN. Completion status will indicate the source LUN. Request sense is issued to the source LUN ~~nad~~ will indicate erroring LUN in the sense bytes.

Command Description (Class 7)

Opcode	Description
00	RAM Diagnostic. Performs a data pattern test on the RAM buffer.
01	Write ECC. Displaces data on the disk by three bytes so that the ECC bytes can be written from the data specified. Used to verify the ECC logic.

02 Read ID. Transfers the cylinder, head, sector and 3 ECC bytes for the specified block ID field.

03 Drive Diagnostic Ø. Performs a drive diagnostic. Reads sector Ø on all cylinders sequentially. Reads sector Ø on 256 random cylinders.

4.1 Command Format

4.1.1 Class Ø & 7 Commands

byte #	7	6	5	4	3	2	1	0
0	0	0	0	opcode				
1	LUN			logical adr2				
2	logical adrl							
3	logical adr0							
4	number of blocks *							
5	control							

*Interleave factor for format and check track commands.

The control field is defined as follows:

7	6	5	4	3	2	1	0

spare (set to zero)

disable overlap

disable data error correction

disable retry

Commands in this group

a) NOP
b) Format Drive
c) Check Format
d) Request Sense
e) Request Syndrome
f) Recalibrate
g) Read Block(s)
h) Read ID
i) Write Block(s)
j) Format Track
k) Format Track (bad track flag)
l) Seek
m) RAM Diag.
n) Drive Diag.
o) Write ECC

4.1.2 Class 1 Commands

byte #	7	6	5	4	3	2	1	0
0	0	0	1	opcode				
1	LUN/s			logical adr2/s				
2	logical adr1/s							
3	logical adr0/s							
4	number of blocks							
5	LUN/d			logical adr2/d				
6	logical adr1/d							
7	logical adr0/d							
8	spare							
9	control							

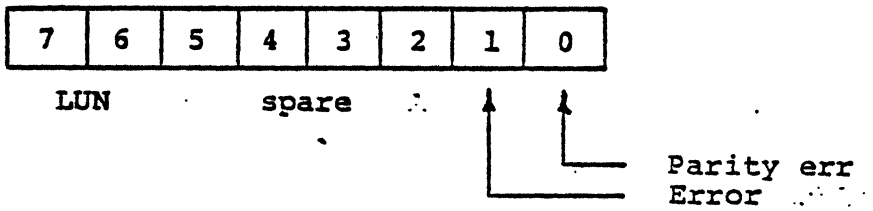
where 's' indicates the source device and
'd' indicates the destination device.

Commands in this group

a) Copy Block

4.2 Status Format

4.2.1 Completion Status Byte



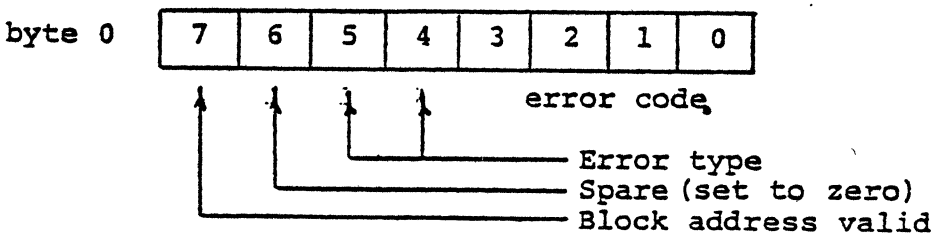
Bit 0 Parity error during transfer from host to controller

Bit 1 Error occured during command

Bit 2-4 Spare (set to zero)

Bit 5-7 Logical unit number of the drive

4.2.2 Drive and Controller Sense



byte #	7	6	5	4	3	2	1	0
1	LUN			logical adr2				
2	logical adr1							
3	logical adr0							

Type 0 (Drive) Error Codes

0	No Status
1	No Index Signal
2	No Seek Complete
3	Write fault
4	Drive not Ready
5	Drive not Selected (SA-1000 only)
6	No Track 00

Type 1 (Controller) Error Codes

0	ID Read Error. ECC error in the ID field
1	Uncorrectable data error during a read.
2	ID address mark not found
3	Data address mark not found
4	Record not found. Found correct CYL & HD but not sector.
5	Seek Error. R/W head positioned on a cylinder and/or selected a wrong head
6	DMA data time out error no acknowledge within 256 bytes.
7	Write protected. (SA-850) only)
8	Correctable data field error.
9	Bad block found.
A	Format Error

Type 2 (command) Error Codes

0	Invalid command recieved form the host.
1	Illegal Disk Address. Address is beyond the maximun address.

Type 3 (misc) Error Codes

0 RAM Error. Data error detected during sector buffer RAM diagnostic

5.0 Electrical/Mechanical Specification

Physical Parameters

Width	8.5 inches
Length	13.5 inches
Height	0.49 inches
Weight	1.12 lbs.

Enviromental Parameters

	Operating	Storage
Temp. (degree) F/C	32/0 to 131/55	-40/-40 to 167/75
Relitive Humidity (@ 40° F, wet bulb temp no condensation)	10% to 95%	10% to 95%
Altitude	Sea level to 10K feet	Sea level to 15K feet

Power Requirements

Voltage @ Current	+5 VDC @ 4.6A (max)
	-5 VDC @ 500mA (max)
	+24 VDC @ 100mA (max)

6.0 Diagnostic Philosophy

6.1 Board Resident Microdiagnostic

A. Power Up Microdiagnostic

The nucleus of the controller is the microprocessor. It consists of the following major blocks: ALU, JUMP, CONTROL, RAM, ROM and associated data paths. Whenever a reset is sent to the controller the microdiagnostics are executed.

B. Fault Isolation Microdiagnostic

The remaining portion of the controller can be checked out by initiating explicit microdiagnostic routines. The routinges are initiated by a set of control switches. Errors will be displayed in a set of LED's. Each microdiagnostic checks the fuctionality of a particular section of the controller and is able to isolate failures in the following major categories:

- Host Interface
- Disk Drive Interface
- Disk Drive Cables
- On-board Failure

Fault-isolation techniques can be concentrated on the failing section.

6.2 Error message and fault isolation microdiagnostic operation procedure (to be provided).

7.0 SA1000 Sector Format

The track layout for the SA1000 (typical for 32 sectors) is shown below.

13 bytes 00's	am	FE	cyl	*hd	sec	ecc	00	00	13 bytes 00's	am	F8	256 bytes data	ecc	00	00	15 bytes 4E's

am, FE, cyl, hd, sec, 00, F8 = 1 byte

ecc = 3 bytes

Track Capacity = 10416 +/- 3.5%, i.e. +/- 365 bytes

10048	= 314 X 32
16	= Index Gap (4E)
352	= Speed Tolerance Gap (4E)
10416	

314 bytes/sector

Last Gap = 352 bytes

* Bit 7 of head byte when set indicates bad sector.

8.0 Host I/O Connector Pin Assignment

The Host I/O Bus uses a 50-pin connector (AMP P/N 2-87227-5 or equivalent). The unused signal pins are considered to be spares for future use. The pin assignments are as follows:

Signal	Pin Number
DB(0)	2
DB(1)	4

Signal	Pin Number	
DB(2)	6	
DB(3)	8	
DB(4)	10	
DB(5)	12	
DB(6)	14	
DB(7)	16	
DB(8)	18	
----	20	-------
----	22	A
----	24	
----	26	for
----	28	future
----	30	usage
----	32	V
----	34	------
BSY	36	
ACK	38	
RST	40	
MSG	42	
SEL	44	
C/D	46	
REQ	48	
I/O	50	

NOTE:
All signals are negative true and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5V and 330 ohms to ground at each end of the bus.