REFERENCE MANUAL

SHUGART 706/712
HARD DISK

Silicon Valley Computer
(408)288-8837

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ABBREVIATIONS/MNEMONICS

BKPC	Background Port C
bpi	Bits per Inch
CRC	Cyclic Redundancy Check
D	Prompt Character
fci	Flux Change per Inch
ID	Identification
I/O	Input/Output
IP	Inspect Phase
LED	Light Emitting Diode
LSI	Large Scale Integration
MFM	Modified FM
MLC	Machine Language Code
PCB	Printed Circuit Board
PP	Print Parameters
PWM	Pulse Width Modulation
RCFLG	Recalibrate Flag
R/W	Read/Write
SEL	Select
tpi	Tracks per Inch
TRK	Track

NOTICE TO USERS

This manual, P/N 39402-0, supersedes, replaces, and incorporates the OEM manual, P/N 39252-1, published April, 1983, and further includes the Publication Change Notice No. 1 dated August 18, 1983, and Publication Change Notice No. 2 dated February 20, 1984. All technical changes have been indicated with a change bar in the text margin or a star symbol in the illustration. While every effort has been made to ensure that the information provided herein is correct, please notify us in the event of an error or inconsistency. Direct any comments on the form at the back of this manual to:

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SECTION I
INTRODUCTION

1.1 PURPOSE

This publication is designed as a reference source for OEM engineers, system integrators, service and maintenance technicians, and knowledgeable end users. It is assumed that the reading audience is sufficiently versed in the state-of-the-art with respect to rigid disk drives.

1.2 GENERAL DESCRIPTION

The Shugart 706/712 Disk Drives are random access 5.25 inch (130 mm) Winchester storage devices with one (706) or two (712) non-removable disks as storage media. Each disk surface employs one movable head to service 320 data tracks. These drive are available in half-height or full height configurations.

Low cost and high reliability are acheived through the use of a unique rotary band actuator design, a self-contained microcomputer, and custom LSI circuitry.

The 706/712 interface is either ST506 or ST412 compatible, allowing easy integration into existing systems. Some of the key features of this series are as follows:

a. Microprocessor-based electronics.

b. Three custom LSI devices for reliability.

c. Built-in diagnostics.

d. Jumper selected exercise routines.

e. Dedicated landing zone.

f. Single track seek time is less than latency.

g. Read/write pre-amp on head arm.

h. 3370 head flexure design.

i. Brushless dc spindle motor.

j. Winchester design reliability in a half-height or full-height package.

k. Improved shock and vibration characteristics.

1.3 SPECIFICATIONS SUMMARY

1.3.1 Performance Specifications

	706	712
Capacity		
Unformatted		
Per Drive	6.4 Mbytes	12.7 Mbytes
Per Surface	3.2 Mbytes	3.2 Mbytes
Per Track	10,416 bytes	10,416 bytes
Formatted (33 sectors/track)		
Per Drive	5.2 Mbytes	10.3 Mbytes
Per Surface	2.6 Mbytes	2.6 Mbytes
Per Track	8.4 kbytes	8.4 kbytes
Per Sector	256 bytes	256 bytes
Formatted (32 sectors/track)		
Per Drive	5.0 Mbytes	10.0 Mbytes
Per Surface	2.5 Mbytes	2.5 Mbytes
Per Track	8.2 kbytes	8.2 kbytes
Per Sector	256 bytes	256 bytes
Transfer Rate	5.0 Mbits/sec	5.0 Mbits/sec
Access Time (includes settling time)		
Track to Track	16.2 msec	16.2 msec
Average	85 msec	85 msec
Maximum	175 msec	175 msec
Average Latency	8.37 msec	8.37 msec
Start Up Time (typical)	12 sec	12 sec

1.3.2 Functional Specifications

Read/Write Heads	2	4
Disks	1	2
Cylinders	320	320
Data Tracks	640	1,280
Index/Revolution	1	
Rotational Speed	3,600 (±0,-72) rpm	
Recording Density	9,036 bpi	
Flux Density	9,036 fci	
Track Density	360 tpi	
Data Encode Method	MFM	
Write Precompensation	12 (± 2) nsec	
Reduced Write Current	Automatic	
Shipping Zone (track number)	353	

1.3.3 Physical Specifications

Mechanical Dimensions without Faceplate (nominal):

Height = 1.63 in (4.14 cm)
Width = 5.75 in (14.61 cm)
Depth = 8.00 in (20.32 cm)
Weight = 3.0 lbs (1.36 kg)/706
3.6 lbs (1.63 kg)/712

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3.6 lbs (1.63 kg)/712

Environmental Limits:

Host Ambient Temperature:
Operating — 41° to 113°F (5° to 45°C)
Non-operating — -40° to 140°F (-40° to 60°C)

Temperature Gradient:
Operating — 10°F (5.5°C) per ½ hour
Non-operating — 212°F (100°C) per hour non-condensing

Relative Humidity:
Operating — 8% to 80%
Non-operating — 1% to 95%
Maximum Wet Bulb:
Operating — 78°F (25.6°C) non-condensing
Non-operating — Non-condensing

Elevation:
Operating — 0 to 10,000 ft (0 to 3048 m)
Non-operating — -1,000 to 30,000 ft (-305 to 9144 m)

Acoustic Noise: Less than 50 dbA at 3.3 ft (1.0 m)

Shock:
Operating — 10 G max (11 msec half sine wave)
Non-operating — 40 G max (11 msec half sine wave)

Vibration:
Operating:
5 — 17 Hz = 0.036 in
17 — 150 Hz = 0.55 G
200 — 500 Hz = 0.25 G
Non-operating:
5 — 22 Hz = 0.50 G
44 — 500 Hz = 2.00 G

DC Voltage Requirements:
±12 Vdc ± 5% .75 A typical (3.9 A max starting for 10 sec) (2.7 A max starting with low power option)
± 5 Vdc ± 5% 1.6 A typical (2.4 A max)

Heat Dissipation = 86 BTU/hr typical (18.4 watts)

1.3.4 Reliability Specifications

Mean Time Between Failure:	20,000 Power-on Hours typical usage
Preventive Maintenance:	None Required
Mean Time to Repair:	12 minutes (PCB only)
Component Life:	5 years

1.4 FUNCTIONAL CHARACTERISTICS

1.4.1 General Operation

The 706/712 fixed disk drives consist of read/write heads, read/write and control electronics, track positioning mechanisms, media, and air filtration systems. These components perform the following functions:

a. Interpret and generate control signals.

b. Position the heads over the selected track.

c. Read and write data.

d. Provide a contaminant-free environment.

1.4.2 Read/Write and Control Electronics

The standard microprocessor and electronics are packaged on one printed circuit board containing the following circuits:

a. Index Generator Circuit

b. Head Position Actuation Drivers

c. Read/Write Amplifiers

d. Drive (READY) up to Speed Circuit

e. Drive Select Circuit

f. Write Fault Detection Circuit

g. Read/Write Head Select Circuit

h. Ramped (Buffered) Stepper Circuit

i. Track 00 Indicator

j. Brushless Spindle Motor Control Circuits

1.4.3 Drive Mechanism

The brushless dc drive motor rotates the spindle at 3,600 (±0, -72) revolutions per minute.

1.4.4 Positioning Mechanism

The read/write heads are mounted on an arm which is positioned by a Fasflex™ IV rotary actuator. A stepper motor is used to precisely position the rotary actuator utilizing a unique metal band/capstan concept. Figure 1-2 illustrates this positioning mechanism.

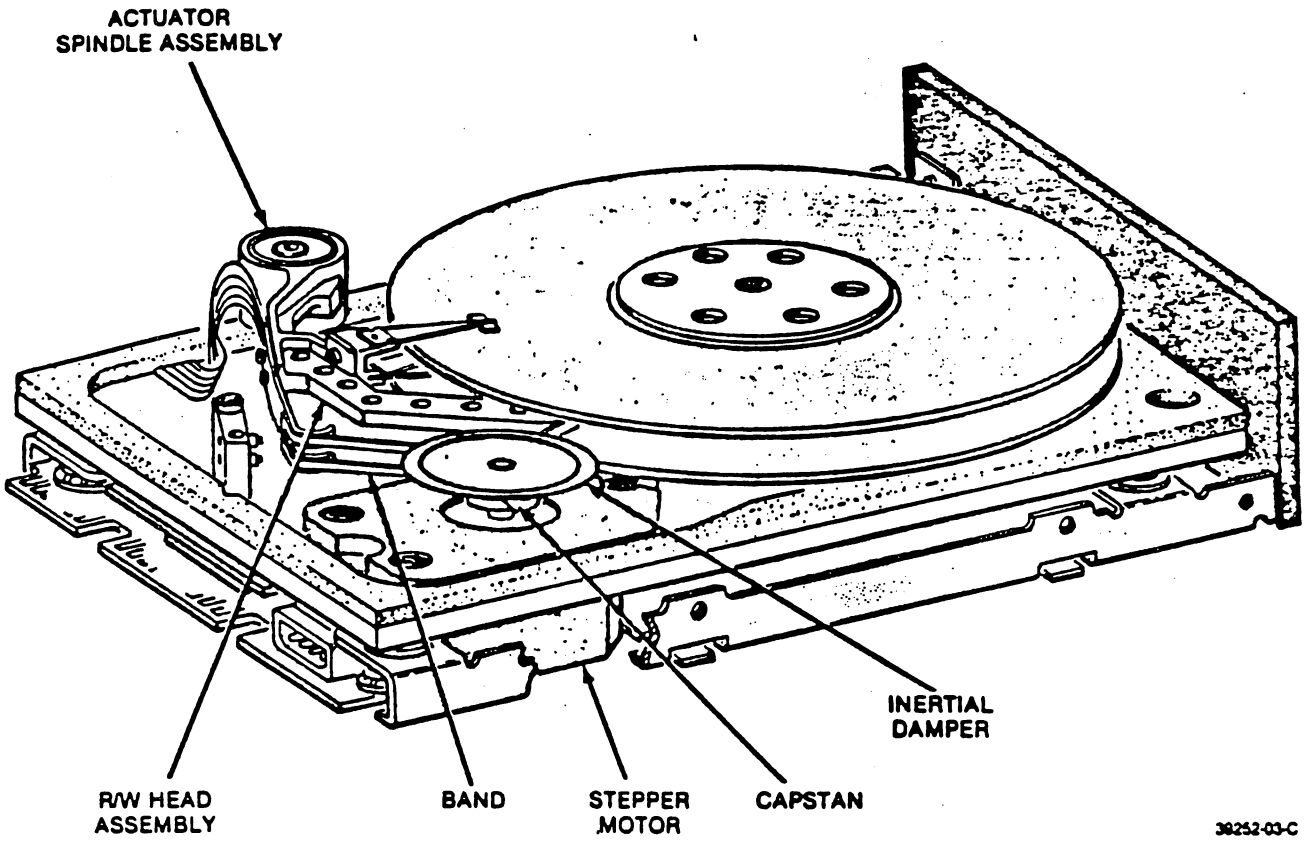
1.4.5 Read/Write Heads and Disk(s)

The recording media consists of a thin, lubricated, magnetic oxide coating on a 130 millimeter diameter aluminum substrate. This coating formulation, together with the low load force/low mass Winchester-type flying heads, permits reliable contact start/stop operation.

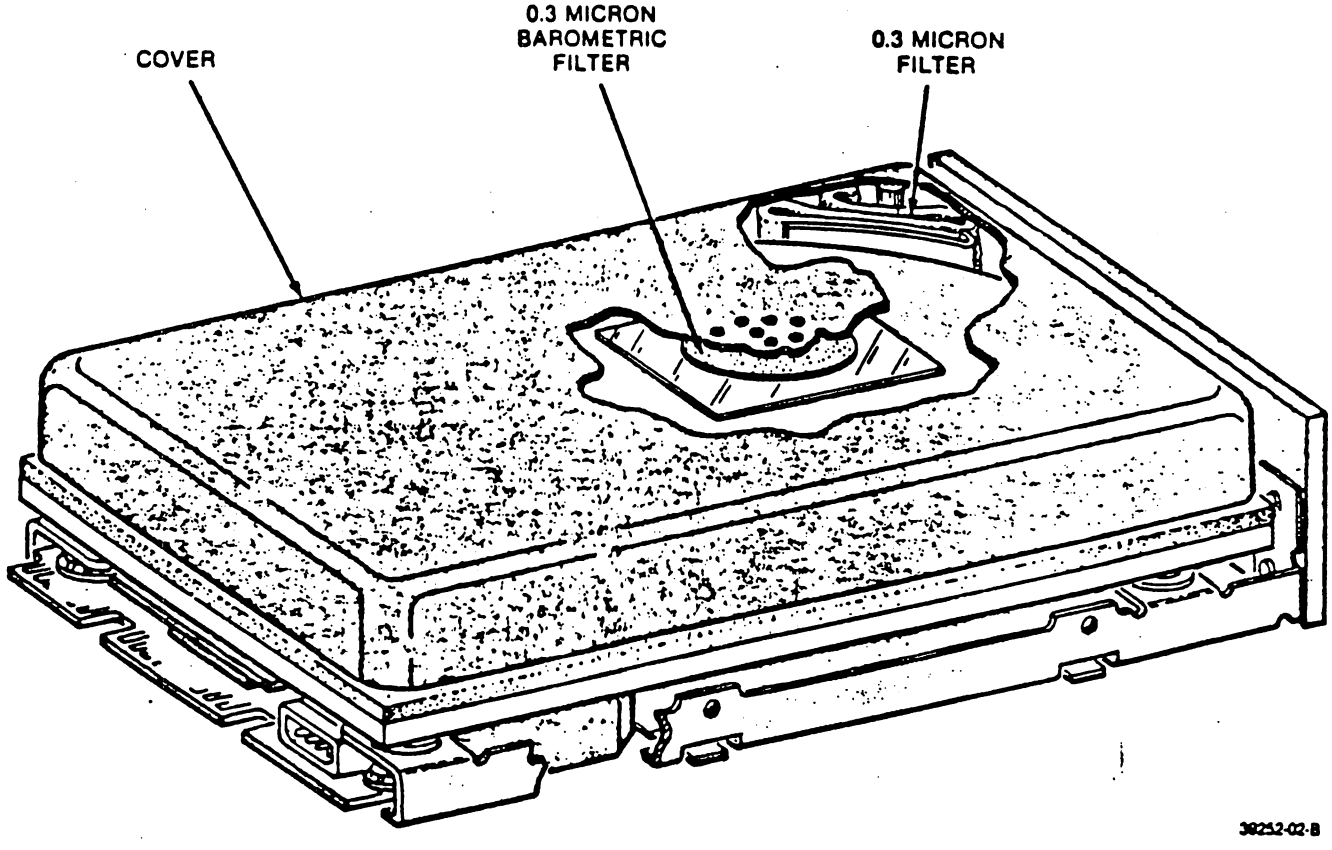
Data on each disk surface are read by one read/write head, each of which accesses 320 data tracks. The drive is available in two basic configurations: one disk with two read/write heads (706) or two disks with four read/write heads (712). The heads should be positioned at cylinder 353 via software prior to power down in order to minimize the potential for damage to the recorded data on portable systems. Refer to paragraph 1.4.8.

1.4.6 Air Filtration System

The disk(s) and read/write heads are fully encased in a protective cover using an integral recirculating air system, with a recirculating filter, to maintain a contaminant-free environment. A separate absolute breather filter allows pressure equalization within the envelope to the ambient air without contamination. See figure 1-3.



☆ FIGURE 1-2. READ/WRITE HEAD POSITIONING MECHANISM



☆ FIGURE 1-3. AIR FILTRATION SYSTEM

1.4.7 Spindle Lock and Brake

These drives are provided with an integral fail-safe spindle lock and brake. This solenoid operated, mechanical brake is actuated when dc power is applied to the drive, allowing the spindle to rotate. When the drive is powered off, the solenoid is deactivated allowing the brake to engage the spindle. This prevents the possibility of disk movement during shipping or movement of the drive. During spin down, the brake decelerates the spinning disks quickly to reduce the amount of time that the heads are in unstable flight. See figure 1-4.

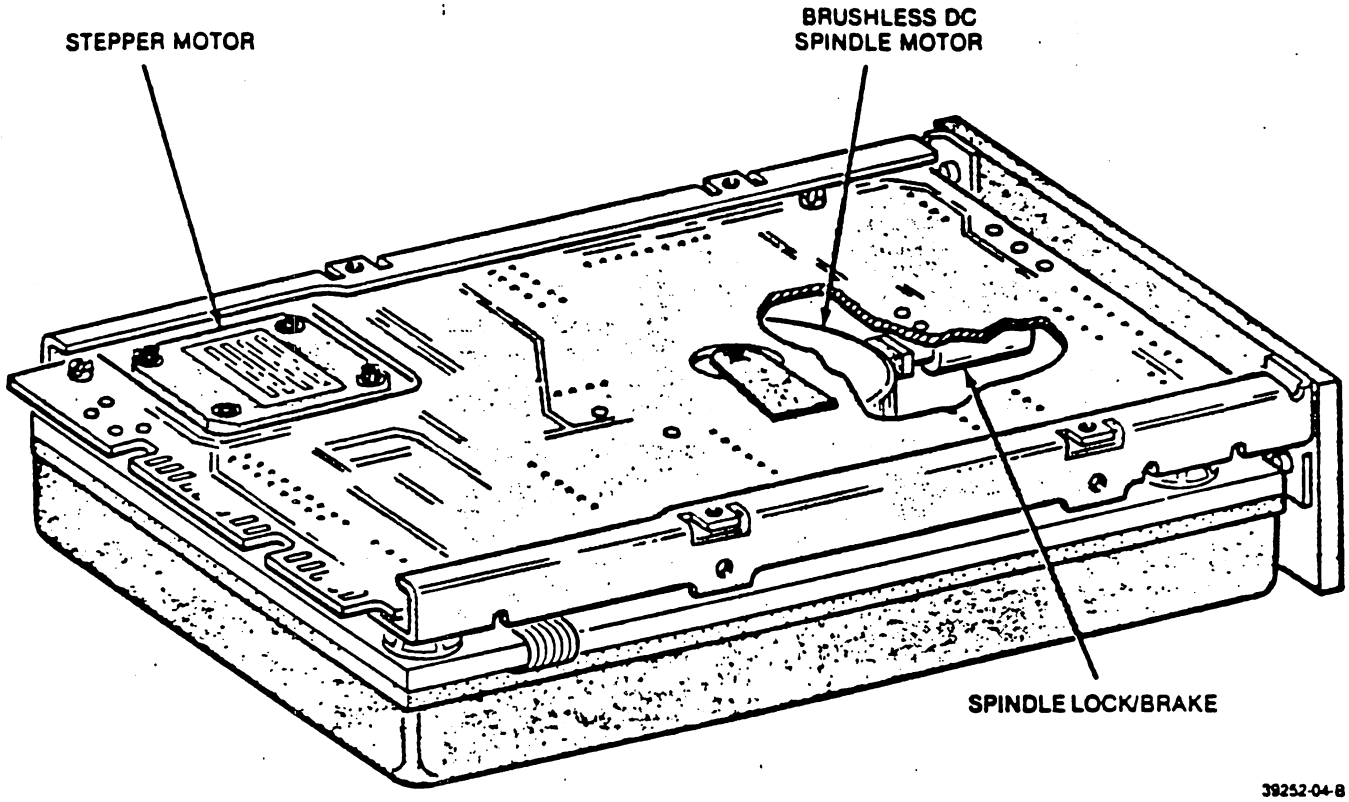


FIGURE 1-4. SPINDLE LOCK

1.4.8 Read/Write Head Shipping Zone

The unused area of the disk surface, inside the data bands, is designated as a "shipping zone." The heads should be positioned to this area via software before the drive is powered off, prior to moving or shipping the drive. This ensures that if the drive is exposed to severe handling (shock), the data storage area of the disk surface will not be damaged by heads movement on the disk(s). See figure 1-5.

1.5 FUNCTIONAL OPERATIONS

1.5.1 Power Sequencing

The required power-on sequence for early production units (i.e., 706/712 that are MLC 4 or less) is that both the 5 and 12 volts supplies be "on" within 20 seconds of each other. The order is not important.

No power-on sequence is required for MLC 5 and above. All drives have a speed sense circuit to prevent stepping until the disk is rotating at the proper speed (3,600 rpm). A READY signal will be presented to the controller interface once the disk is up to its normal rotational speed (± 2%) for two seconds. At READY time, after an initial power-up, the drive will recalibrate itself to track 00. When the recalibration procedure is complete, SEEK COMPLETE will go true. Normal seek and read functions can now begin. Refer to paragraph 2.6.

1.5.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the drive appropriately jumpered will respond to the input signals, and the output signals of that drive are then gated to the controller.

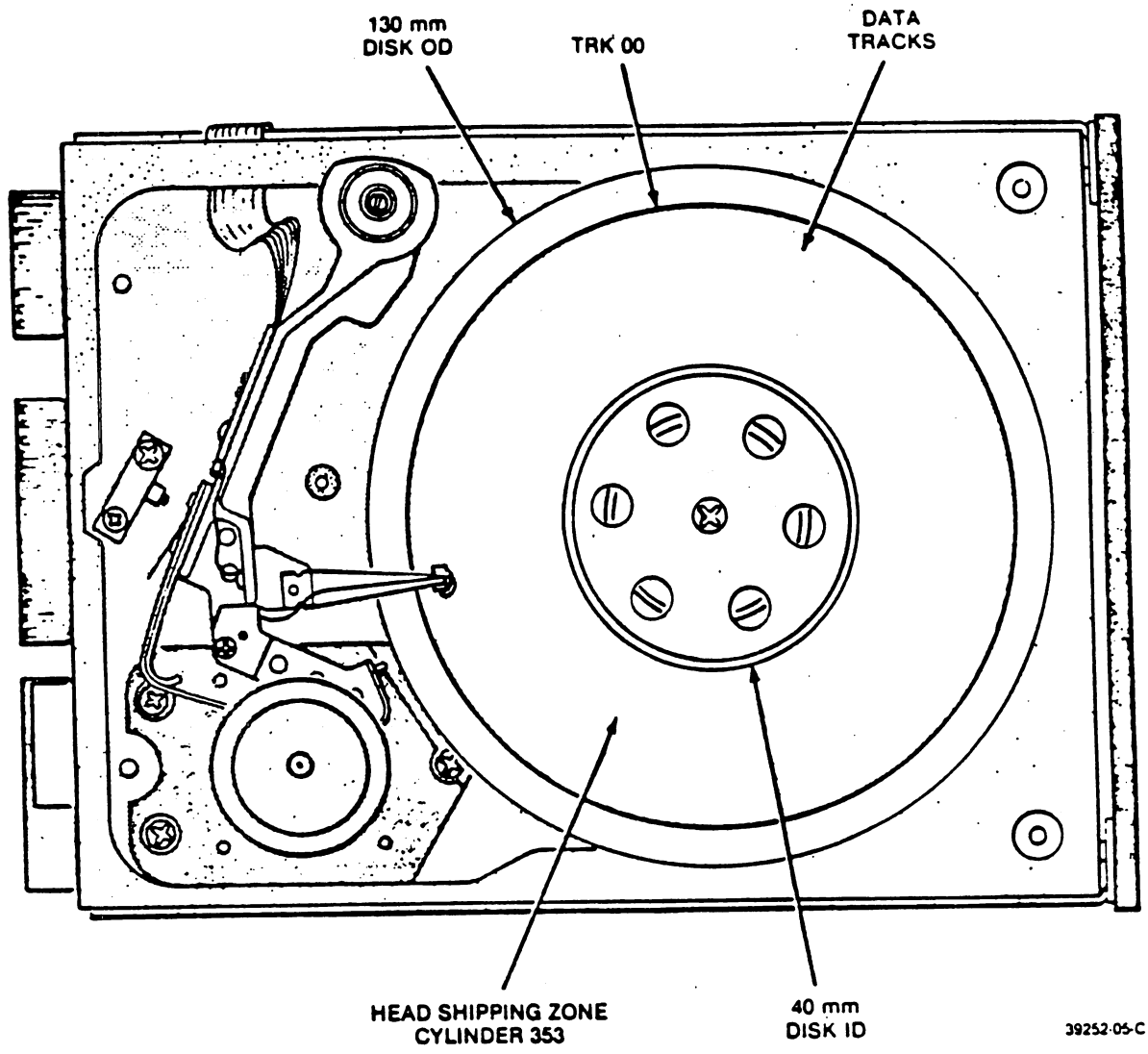


FIGURE 1-5. SHIPPING ZONE

1.5.3 Track Accessing

Read/write head positioning is accomplished by:

a. Deactivating the WRITE GATE.

b. Activating the appropriate DRIVE SELECT line.

c. Being in the READY condition with SEEK COMPLETE true.

d. Selecting the appropriate direction.

e. Pulsing the STEP line.

f. Checking for the edge of the -SEEK COMPLETE line (changing from false to true).

Stepping can occur at either the normal or buffered rate. During normal stepping, the heads are repositioned at the rate of incoming step pulses. In the case of buffered stepping, incoming step pulses are received at a high rate and are buffered into counters. When all of the steps have been received, they are issued to the stepper drivers at a ramped stepping rate.

Each pulse will cause the heads to move either one track in or one track out, depending on the level of the DIRECTION IN line. A true on the DIRECTION IN line will cause an inward seek; a false will result in an outward seek toward track 00.

1.5.4 Read Operation

Reading data from the disk is accomplished by:

a. Deactivating the WRITE GATE line.

b. Activating the appropriate DRIVE SELECT line.

c. Assuring that the drive is READY.

d. Selecting the appropriate head.

1.5.5 Write Operation

Writing data onto the disk is accomplished by:

a. Activating the appropriate DRIVE SELECT line.

b. Assuring that the drive is READY.

c. Clearing any write fault conditions (if thet exist), by reselecting the drive.

d. Selecting the proper head.

e. Activating the WRITE GATE and placing data on the WRITE DATA line.

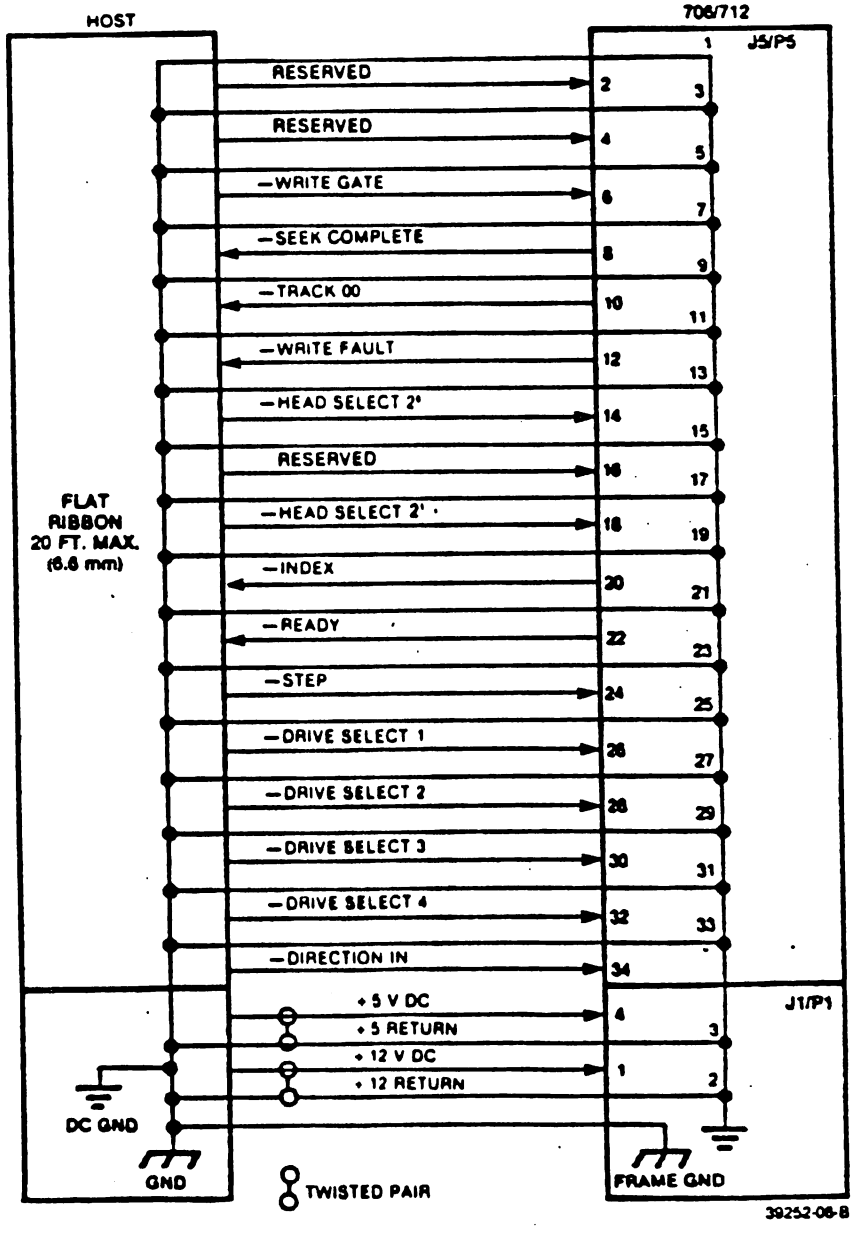
1.5.6 Head Selection

Any of the two to four possible heads can be selected by placing the binary address of that head on the two HEAD SELECT lines.

SECTION II
ELECTRICAL INTERFACE

2.1 INTRODUCTION

The interface for a 706/712 has drive control signal pin assignments per industry standards. See figure 2-1 for the pin assignments.



☆ FIGURE 2-1. J5 INTERFACE AND J1 POWER CONNECTIONS

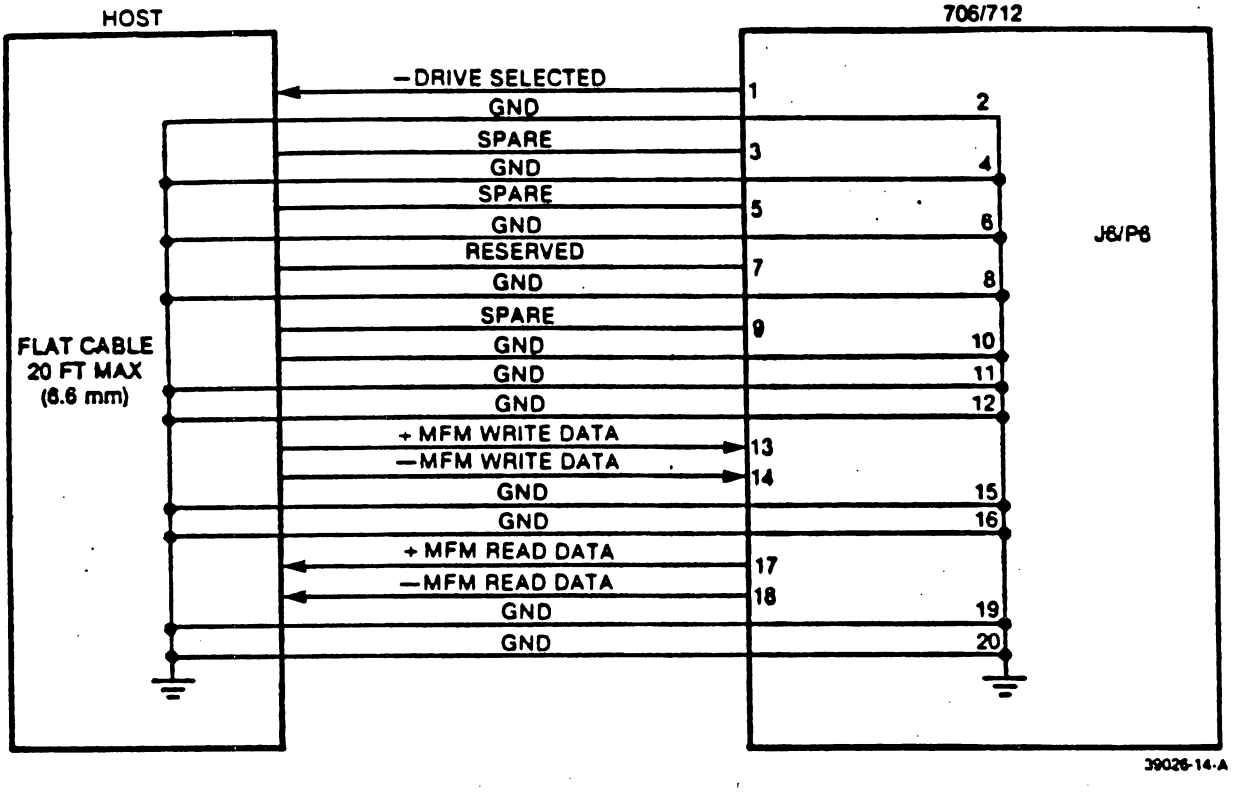
The signal interface consists of three categories:

a. Control Input Lines

b. Control Output Lines

c. Data Transfer Lines

All control lines are digital in nature and either provide signals to the drive (input) or provide signals to the host (output) via the interface connector J5/P5. The data transfer signals are differential in nature. They provide data either to or from the drive, via J6/P6. See figure 2-2 for the J6/P6 pin assignments.



☆ FIGURE 2-2. J6 INTERFACE CONNECTION

2.2 CONTROL INPUT LINES

The control input signals are of two types; those intended for multiplexing in a multiple drive system, and those intended to control the multiplexing. The control input signals to be multiplexed are:

a. The STEP signal

b. The DIRECTION SELECT signal

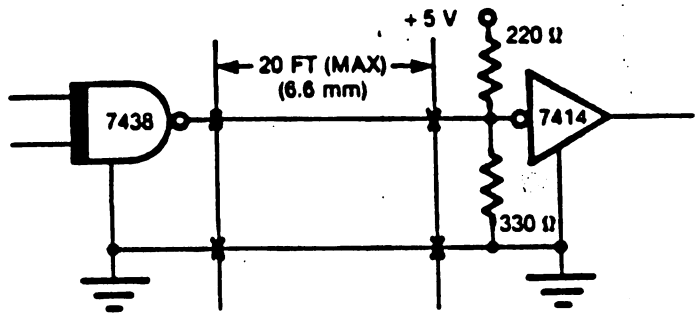
c. The HEAD SELECT 2^0 and 2^1 signals

d. The WRITE GATE signal

The signals which are intended to control the multiplexing are DRIVE SELECT 1 through DRIVE SELECT 4.

The control input lines have the following electrical specifications. See figure 2-3 for the recommended circuit.

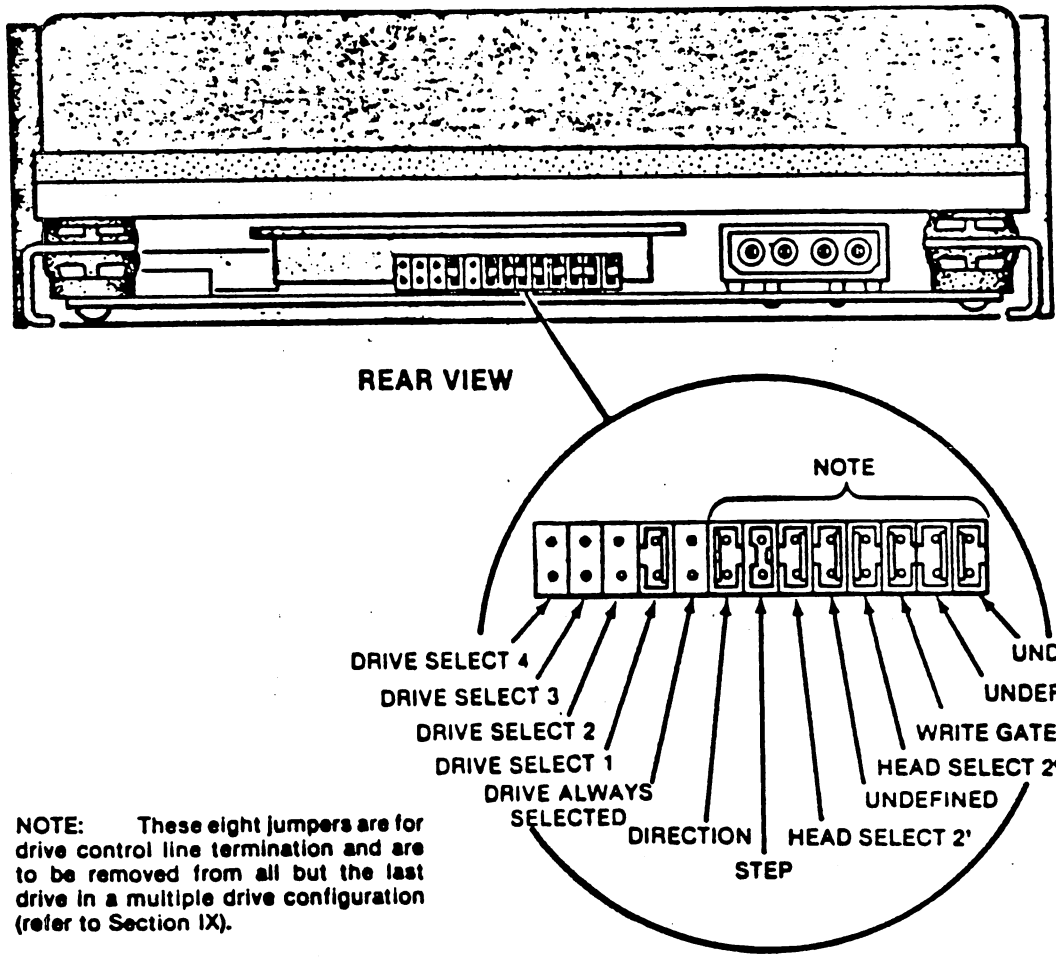
Only one drive in the system should be terminated. It should be located at the end of the cable and terminated with a 220/330 ohm resistor pack. This resistor pack can be disabled by removing the jumper block located near the P5 connector. See figure 2-4 for the location.



True = 0.0 to 0.4 V dc @ Iin = 40 mA (max)
False = 2.5 to 5.25 V dc @ Iin = 0 mA (open)

39026-06-A

FIGURE 2-3. CONTROL INPUT DRIVER/RECEIVER COMBINATION



NOTE: These eight jumpers are for drive control line termination and are to be removed from all but the last drive in a multiple drive configuration (refer to Section IX).

39252-07-A

☆ FIGURE 2-4. JUMPER LOCATIONS

2.2.1 Drive Select 1–4

DRIVE SELECT, when logically true, connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time.

Jumper options DS1-4 are used to choose which DRIVE SELECT line will activate the interface for that unique drive. See figure 2-4 for the jumper locations.

2.2.2 Direction In

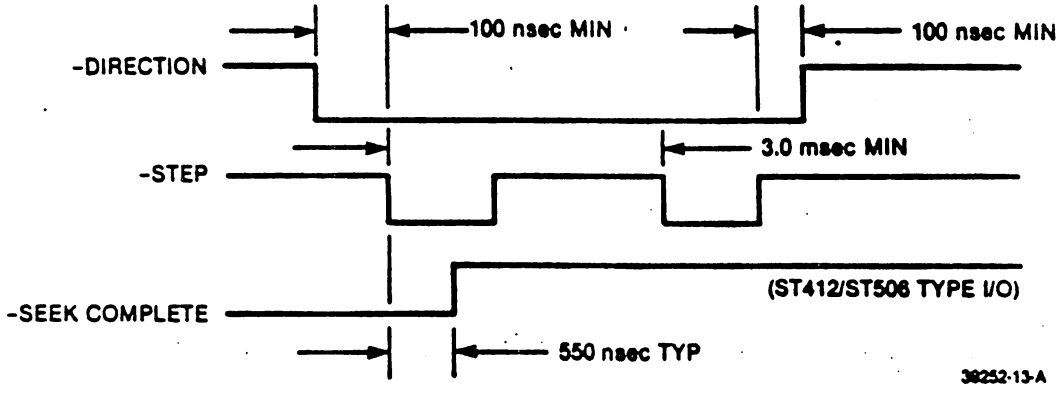
This signal defines the direction of motion of the read/write heads when the STEP line is pulsed. An open circuit, or logical false, defines the direction as "out" and a pulse applied to the STEP line will move the R/W head away from the center of the disk. If the input is shorted to ground (logical true) and a pulse is applied, the heads will move toward the center of the disk, i.e. "in."

2.2.3 Step

This line causes the read/write heads to move in the direction defined by the DIRECTION IN line. The motion is initiated at each logical true-to-false transition. Any change in the DIRECTION IN line must be made before the leading edge of the STEP pulse. Stepping can be performed in either the normal or buffered mode:

Normal Step Mode

In this mode, the read/write heads will move at the rate of the incoming STEP pulses. The minimum time between successive steps is 3.0 msec, with a minimum pulse width of 500 nsec. See figure 2-5.



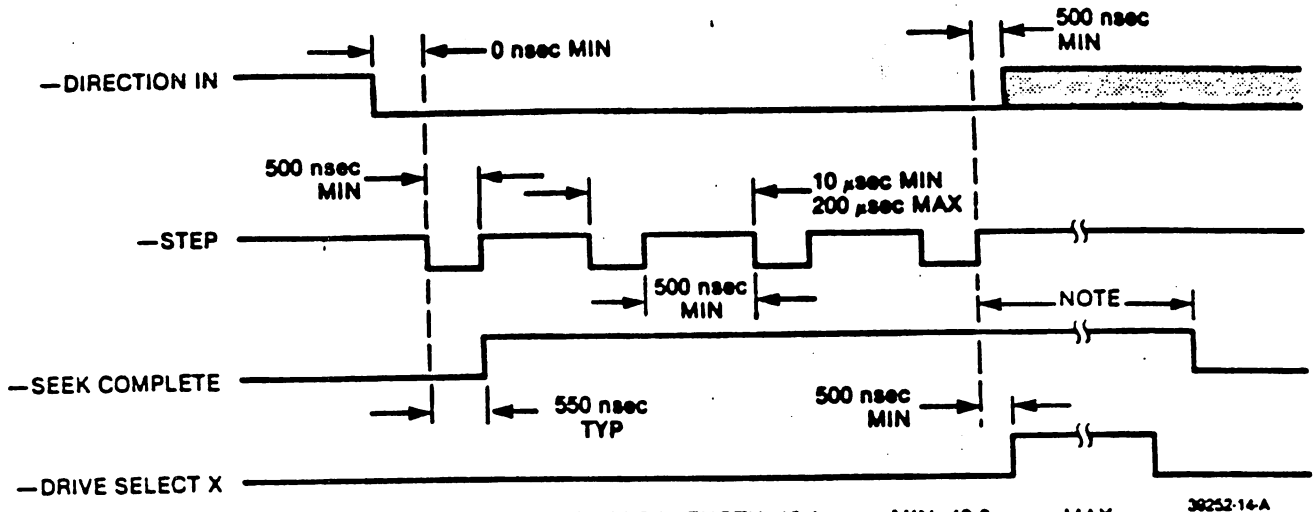
☆ FIGURE 2-5. NORMAL STEP MODE

Buffered Step Mode

In this mode, the STEP pulses are received at a high rate and buffered into a counter. After the last STEP pulse, the read/write heads will begin stepping the desired number of cylinders and SEEK COMPLETE (refer to paragraph 2.4.5) will go true after the heads settle on the cylinders. This mode of operation is automatically selected when the time between STEP pulses is less than 200 μsec.

The DRIVE SELECT line may be dropped and a different drive selected 500 nsec after the last STEP pulse has been sent to the drive.

The maximum time between steps is 200 μsec, with a minimum pulse width of 3.0 μsec. See figure 2-6.



NOTE: VARIES WITH SEEK LENGTH. 16.4 msec MIN, 40.0 msec MAX.

FIGURE 2-6. BUFFERED STEP MODE

Shipping Zone

The read/write heads can be accessed to the shipping zone by doing a seek to cylinder 353.

NOTE

STEP pulses with periods between 200 µsec and 3.0 msec are not permitted. Seek accuracy is not guaranteed if this timing requirement is violated.

2.2.4 Head Select 2^0 and 2^1

These two lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. When all HEAD SELECT lines are false, head 0 will be selected. Table 2-1 shows the HEAD SELECT sequence and model variations for the HEAD SELECT lines. See figure 2-7 for the timing sequences.

TABLE 2-1. HEAD SELECT (1 = FALSE, 0 = TRUE)

HEAD SELECT LINE 2^0	HEAD SELECT LINE 2^1	HEAD SELECTED 706	HEAD SELECTED 712
1	1	0	0
0	1	1	1
1	0	IMPROPER SELECT	2
0	0	IMPROPER SELECT	3

39252-06-B

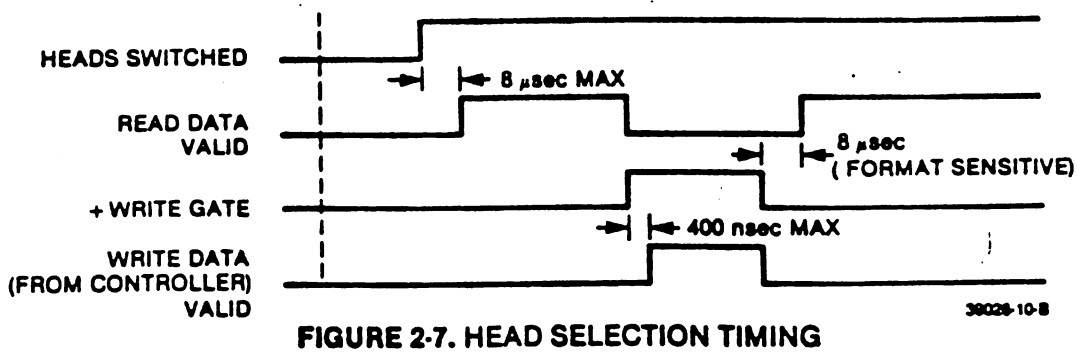


FIGURE 2-7. HEAD SELECTION TIMING

2.2.5 Write Gate

The active state of this signal (logical 0 level) enables WRITE DATA to be written onto the disk. The inactive state of the signal (logical 1 level) enables data to be transferred from the drive and STEP pulses to reposition the head arm. See figure 2-7 for the timing sequences.

2.2.6 Reduced Write Current and Precompensation

The 706/712 provides for automatic reduced write current switching. Optimum precompensation is 12 nsec and should be used on cylinders 128 through 320.

2.3 CONTROL OUTPUT LINES

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 mA at logical 0 (true), with a maximum voltage of 0.4 V measured at the driver. When the line driver is at logical 1 (false), the driver transitor is off and the collector cut-off current is a maximum of 250 μA.

All J5 output lines are enabled by their respective DRIVE SELECT lines.

Figure 2-3 shows the recommended control signal driver/receiver combination.

2.3.1 Track 00

This interface signal indicates a true state (logical 0) only when the read/write heads of the selected drive are at track 00 (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. This signal is false (logical 1) when the read/write heads of the selected drive are not at track 00. The state of this line is undefined when SEEK COMPLETE is false.

2.3.2 Index

The drive provides this interface signal once every revolution (16.74 msec typical) to indicate the beginning of the track. Normally this signal is a logical 1 (false) and makes the transition to logical 0 (true) for a period of approximately 200 μsec once each revolution (see figure 2-8).

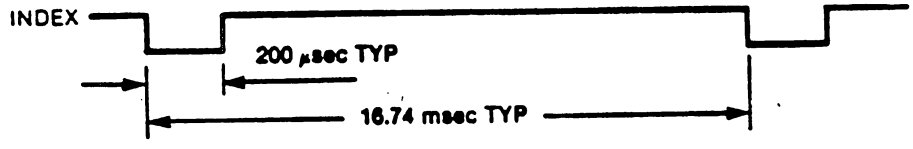


FIGURE 2-8. INDEX TIMING

2.3.3 Ready

This interface level, when true (logical 0), together with SEEK COMPLETE, indicates the drive is ready to read, write, or seek, and that the signals are valid. When this line is false (logical 1), all seeking and writing is inhibited at the drive.

READY will be true after the drive is up to speed (± 2%) for two seconds. The typical time for READY to become true after power-on is 12 seconds(21 seconds when the low power option has been utilized). After the automatic actuator recalibration process, typically six seconds, SEEK COMPLETE will also become true. It is now safe to seek the drive, but an additional two minutes should be allowed for thermal expansion to stabilize before any write operations are performed.

2.3.4 Write Fault

This signal, when active (logical 0), is issued to indicate a condition exists at the drive that could cause improper writing on the disk. A WRITE FAULT occurs whenever one of three conditions occurs:

a. The read/write heads are improperly selected.

b. The dc voltage is more than 25 percent out of tolerance.

c. The actuator or spindle control system is faulted.

To reset the WRITE FAULT line, deselect the drive for at least 500 nsec.

NOTE

The WRITE FAULT line will not reset if the fault condition still exists after deselection of the drive.

2.3.5 Seek Complete

The SEEK COMPLETE signal will go true (logical 0) when the read/write heads have settled on the final track at the completion of a seek. Reading or writing should not be attempted until SEEK COMPLETE is true.

The SEEK COMPLETE will go false in two cases:

a. A recalibration sequence is initiated (by the drive logic) at power-on if the read/write heads are not over track 00. Refer to paragraph 2.7.

b. After the leading edge of a STEP pulse (550 nsec typical) or the first of a series of Step pulses.

2.4 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host are differential in nature and may not be multiplexed. These two pairs of balanced signals are:

a. MFM WRITE DATA

b. MFM READ DATA

These signals are provided at the J6/P6 connector on all drives. Figure 2-9 illustrates the driver/receiver combination. See figure 2-2 for the J6/P6 interface connection.

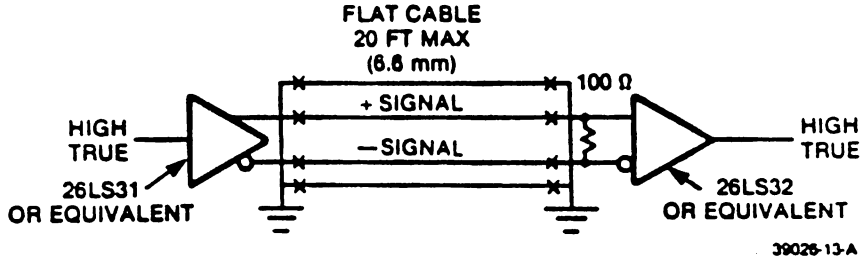


FIGURE 2-9. DATA TRANSFER LINE DRIVER/RECEIVER COMBINATION

2.4.1 MFM Write Data

This pair of signals defines the transitions (bits) to be written on the disk. +MFM WRITE DATA going more positive than -MFM WRITE DATA will cause a flux reversal on the track under the selected head providing WRITE GATE is active. This signal must be driven to an inactive state (+MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in the read mode. Figure 2-10 shows the timing for MFM WRITE DATA.

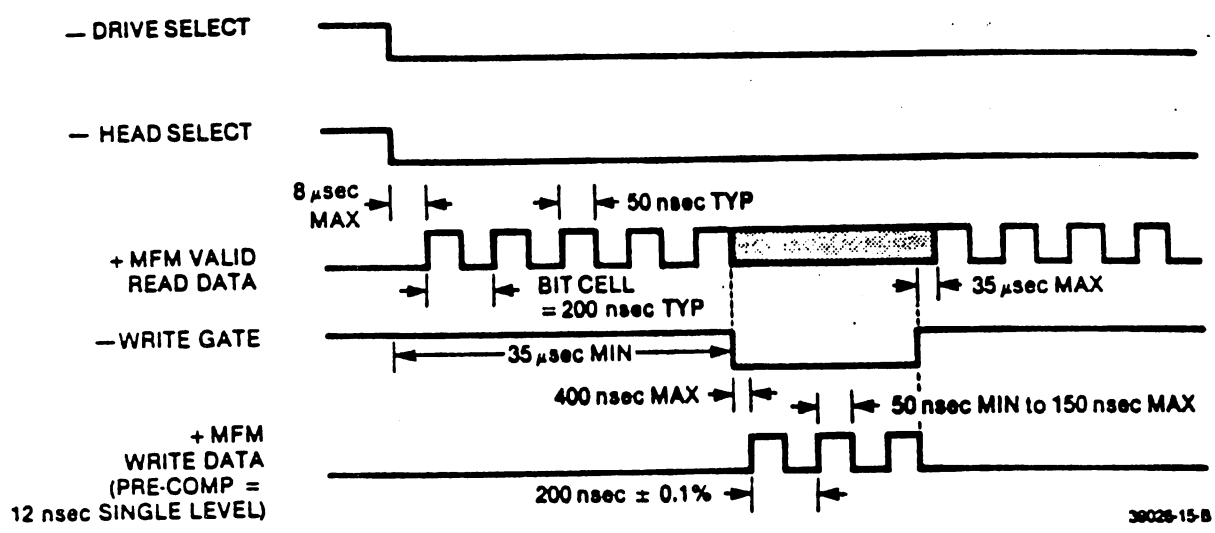


FIGURE 2-10. MFM READ/WRITE DATA TIMING

2.4.2 MFM Read Data

The data recovered by reading a pre-recorded track are transmitted to the host system via the differential pair of MFM READ DATA lines. This transition of the +MFM READ DATA line going more positive than -MFM READ DATA lines represents a flux reversal on the track of the selected head while WRITE GATE is inactive. See figure 2-10.

2.5 SELECT STATUS

A status line is provided at the J6/P6 connector to inform the host system of the selection status of the drive.

The DRIVE SELECT line is driven by a TTL open collector driver as shown in figure 2-8. This signal will go active only when the drive is programmed as drive X (X = 1, 2, 3, or 4) by proper placement of the shorting plug in the vicinity of J5, and DRIVE SELECT X line at J5/P5 is activated by the host system. See figure 2-4 for the jumper location.

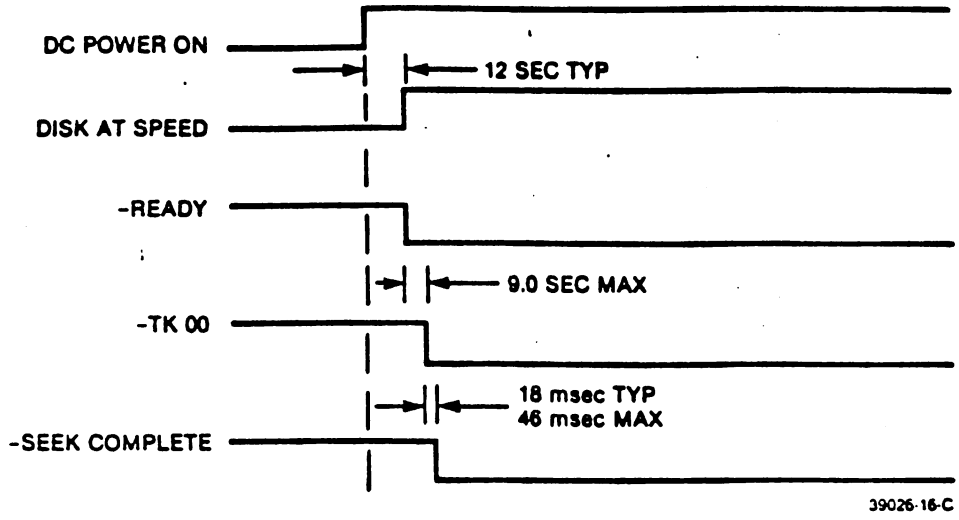
2.6 GENERAL TIMING REQUIREMENTS

The timing diagram shown in figure 2-11 illustrates the necessary sequence of events (with associated timing restrictions) for the proper operation of the drive.

Note that a recalibrate to track 00 sequence is initiated at every dc power-on. For this auto-recall sequence to function, the following conditions must be met:

a. The STEP input at J5/P5 is held active.

b. The spindle is spinning at its regular speed.



☆ FIGURE 2-11. GENERAL CONTROL TIMING REQUIREMENT

2.7 POWER INTERFACE

These drives require only dc power for operation.

The dc power to a 706/712 drive is via connector J1/P1 located on the solder side of the PCB. The two dc voltages and their specifications, along with the J1/P1 pin designations are shown in table 2-2.

Power from the +5 and +12V supplies may be applied in any order. However, the +5V power must be asserted within 20 seconds of the +12V power-on application.

☆ TABLE 2-2. DC REQUIREMENTS

P6 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (P TO P)
1	+12 V	±0.6 V DC ±1.2 V STARTING*	.75 A TYPICAL 3.9 A STARTING*	500 mV MAX ALLOWABLE
2	+12 V RETURN			
3	+5 V RETURN			
4	+5 V	±0.25 V DC	1.6 A TYPICAL 2.4 A MAX	50 mV MAX ALLOWABLE

*10 SEC MAX.

39252 10-A

2.8 FRAME GROUNDING

These drives require ac grounding of the baseplate. This grounding is accomplished in either of two ways:

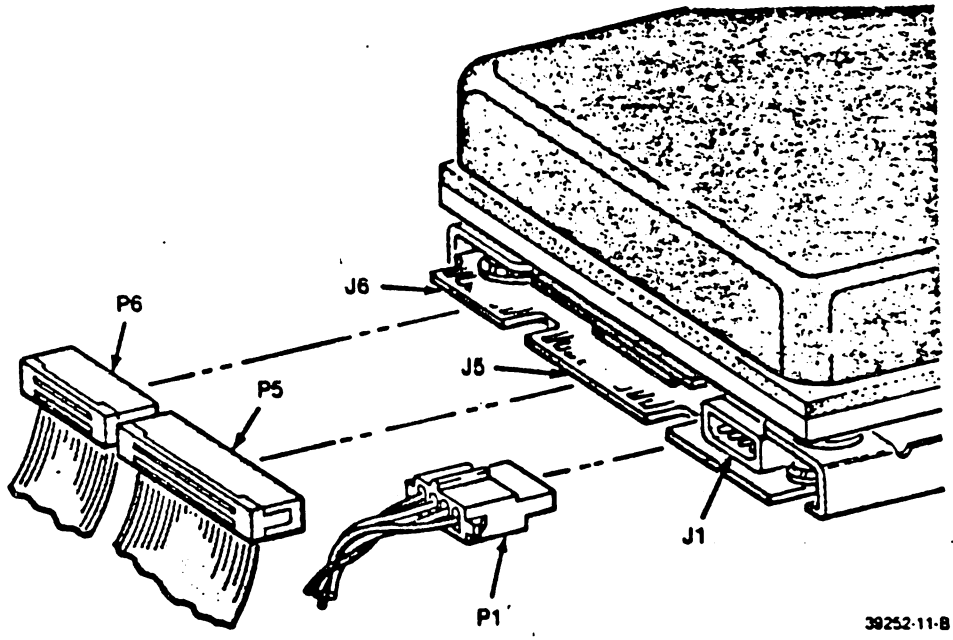
a. The dc voltage returns (+12 V and +5 V) are tied to the ac ground at the power supply.

b. A separate ground wire (#18 AWG or larger) is attached to a grounding lug on the baseplate in the vicinity of the interface connectors.

SECTION III
PHYSICAL INTERFACE

3.1 INTRODUCTION

The electrical interface between a 706/712 drive and the host system is via three connectors. The first connector, J1, provides the dc power; the second connector, J5, provides the control signals for the drive; and the third connector, J6, provides for the radial connection of the read/write signals.

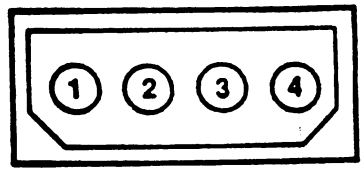


☆ FIGURE 3-1. INTERFACE CONNECTOR LOCATIONS

3.2 J1/P1 CONNECTION

The dc power connector, J1, is mounted on the component side of the PCB. J1 is a 4-pin AMP Mate-N-Lok connector, P/N 350211-1. The recommended mating connector is AMP P/N 1-480424-0 utilizing AMP pins P/N 61473-1. J1, pin 1, is labeled on the component side of the PCB. Wire used should be #18 AWG. Figure 3-2 illustrates the connector as seen on the component side of the drive PCB.

PIN #	DESIGNATION
1	+12 V
2	+12 V RETURN
3	+5 V RETURN
4	+5 V



☆ FIGURE 3-2. J1 CONNECTOR

3.3 J5/P5 CONNECTION

Connection to J5 is through a 34-pin PCB edge connector. The dimensions for this connector are shown in figure 3-3. The pins are numbered 1 through 34 with the odd numbered pins located on the component side of the PCB, and even pins located on the solder side of the PCB. Pin 2 is located at the end of the PCB connector closest to the J1 connector and is labeled. A key slot is provided between pins 3 and 5. The recommended mating connector for P5 is a Scotchflex ribbon connector, P/N 3463-0001.

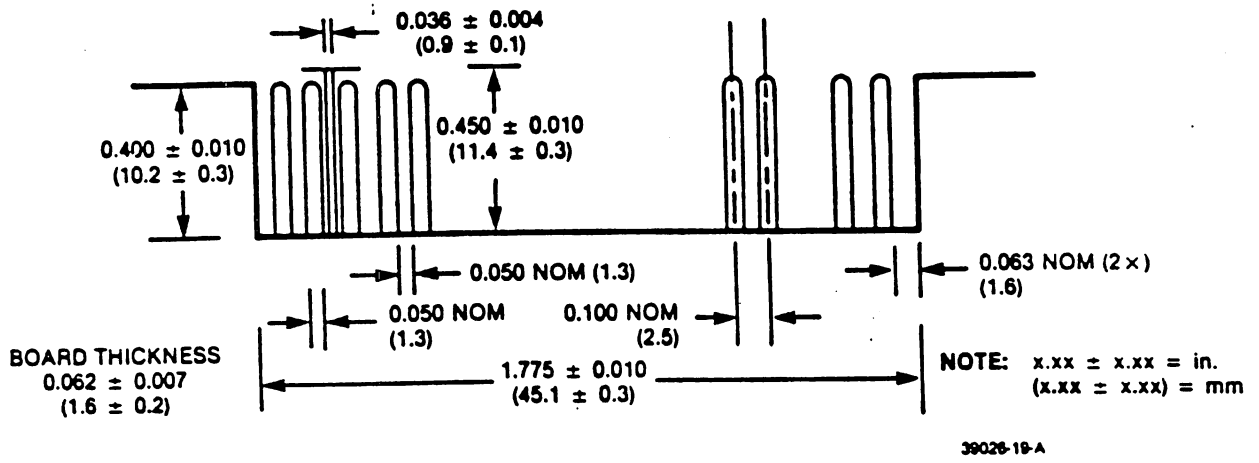


FIGURE 3-3. J5 CONNECTOR DIMENSIONS

3.4 J6/P6 CONNECTION

Connection to J6 is through a 20-pin PCB edge connector. The pins are numbered 1 through 20 with the odd numbered pins located on the component side of the PCB. The recommended mating connector for P6 is a Scotchflex ribbon connector, P/N 3461-0001. A key slot is provided between pins 3 and 5. Figure 3-4 shows the dimensions of the connector.

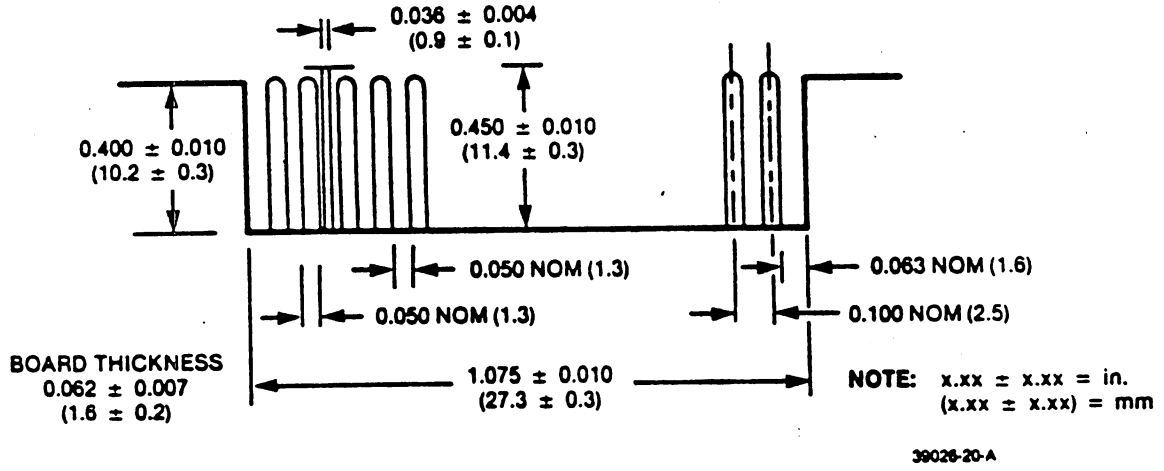
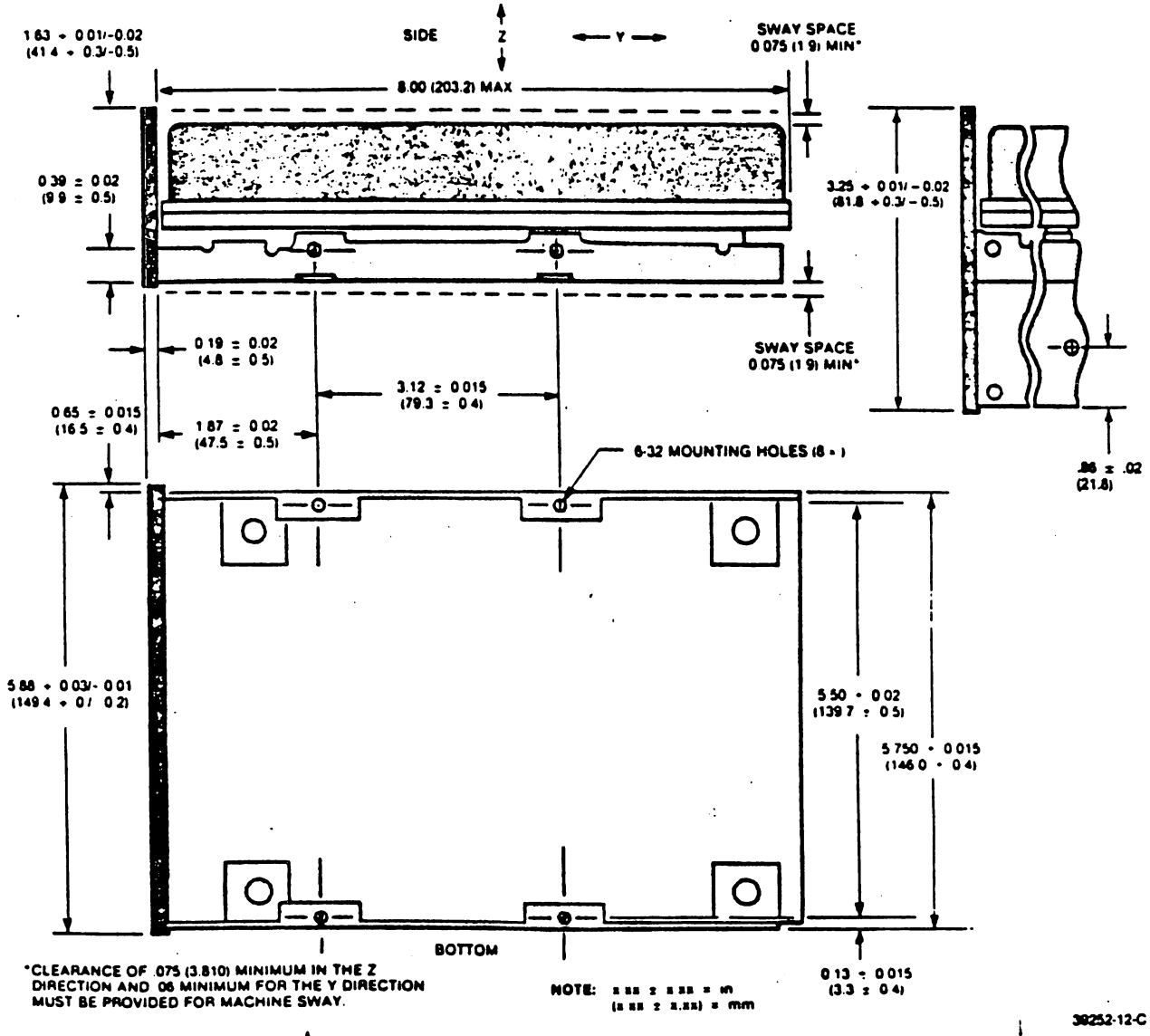


FIGURE 3-4. J6 CONNECTOR DIMENSIONS

SECTION IV
PHYSICAL SPECIFICATIONS

4.1 MECHANICAL DIMENSIONS

See figure 4-1 for the dimensions of the Shugart 700 series drives.



☆ **FIGURE 4-1.** MOUNTING DIMENSIONS

4.2 MOUNTING

The 706/712 drives are capable of being mounted in any position.

CAUTION

These drives must be mounted with four machine screws. The screws may be installed in either the vertical or horizontal plains into the side rails. The screws must be torqued to ten inch/pounds. The required sway space is 0.075 inch.

SECTION V
MEDIA DEFECTS AND ERRORS

5.1 ERROR MAPPING AND QUALIFICATION

In high density digital recording storage systems, it is necessary to increase reliability and improve operational performance. This is done by providing an error detection and correction scheme. For disk storage systems, the predominant error pattern is a burst of errors occuring in one or more tracks. These errors are drop-outs (absent bits), drop-ins (bits added), or bits shifted from their nominal position beyond the tolerance of the data separator.

5.1.1 Causes of Errors

The following conditions may result in errors:

a. Marginal signal to noise ratio of the read/write circuits.

b. Marginal characteristics of the media and the read/write heads.

c. Mispositioning of the read/write heads on the disk.

d. Defects or imperfections in the disk media.

5.1.2 Error Definition

An error is a discrepancy between recorded data and original data. There can be an extra or missing bit, i.e., a "0" can be transformed into a "1" or vice versa.

Errors fall into two categories: "hard" or "soft." Hard errors are usually the result of media defects and will be repeatable. Soft errors are often caused by items "a" through "c" of paragraph 5.1.1, and will normally not be repeatable.

5.1.3 Media Defect Definition

Most errors resulting from media defects are classified as hard errors. They are attributable to small imperfections in the oxide coating of the disk, such as an impurity within the oxide itself, or a scratch on the surface of the oxide coating.

As the storage size and density of information increases, these defects become more apparent to the system. Winchester technology utilizes a higher bit packing ratio than older types of drives and is therefore more susceptible to this type of error.

5.1.4 Error Map

All drives are scanned for hard errors during the manufacturing process. All hard errors (media defects) are logged and an error map is attached to each drive. Each defect listed contains the following information

a. Track number

b. Head number

c. Byte count accurate to ± 4-bytes (indicates the defective bytes as a location from physical index)

d. Length of defect in bits

The error map accompanying each drive will typically provide the locations of more hard errors than will be detected by the user system. There are situations, however, where a magnetic anomaly or extra defects caused by improper handling may cause an error that is unique to a particular format or bit pattern. Such a flaw may present itself as a hard error, in addition to those reported on the error map. In the event this situation occurs, it is recommended that the defect be added to the error map and mapped out.

5.1.5 User Error Mapping

Occasionally, errors shown on the error maps supplied with the drive will not show up as errors in the user's system. Similarly, the user may find hard errors in addition to those on the error map during the user's functional tests

The recommended method of mapping is to create a defect directory at cylinder 00. This directory should include the locations of all defective areas, as well as alternate track assignments for those areas.

5.2 ERROR ACCEPTANCE CRITERIA

The drive, as received from the factory, will meet the following error criteria:

a. No disk will have more than ten defective tracks. Of these ten tracks, no more than three will contain multiple defects. Additionally, track 00 of all heads is guaranteed to be error free.

b. Errors separated by less than 20 bytes from beginning to end, or less, 20 bytes long, are considered one error.

5.3 SYSTEM GENERATED ERRORS

It should be noted that errors may also be present as a result of system electrical noise, marginal timing conditions, ground loops in the dc power distribution cable, electro-magnetic interference, radio frequency interference, etc.

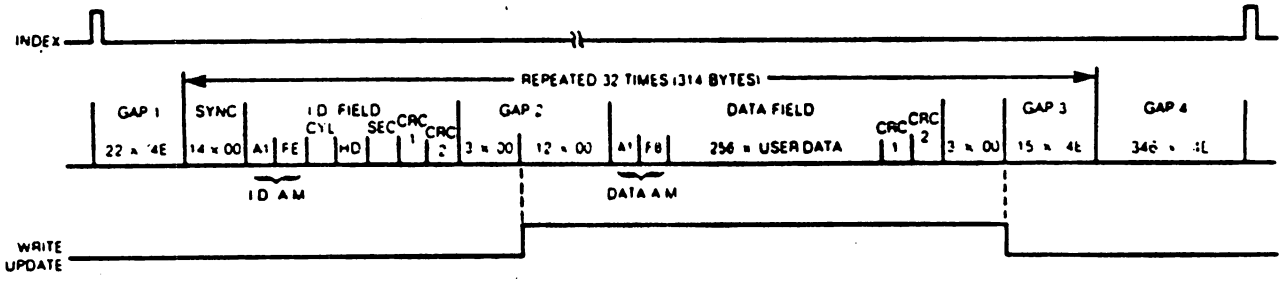
SECTION VI
RECORDING FORMAT

6.1 TRACK FORMAT

The pupose of a format is to organize a data track into smaller, sequentially numbered blocks of data called sectors. The 706/712's format is a soft sectored type, which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address, plus cylinder and head information. The ID field is then followed by a user data field.

The soft sectored format is a slightly modified version of the IBM system 34 double density format commonly used on 8-inch floppy disk drives. The encoding method used here is modified frequency modulation (MFM).

Figure 6-1 shows each track divided into 32 sectors. Each sector has a data field 256 bytes in length. However, if sector interleaving is used, Gap 4 can be reduced to 32 bytes minimum to accommodate 33 sectors per track. If sector interleaving is not used, and 33 sectors are desired, Gap 3 is 25 bytes and Gap 4 becomes 26 bytes minimum.



NOTES:
1. MINIMUM TRACK CAPACITY — 10416 BYTES.
2. WRITE TO READ RECOVERY TIME = 8 MICROSECONDS.
3. HEAD SWITCHING TIME = 8 MICROSECONDS.

39026-23

FIGURE 6-1. TRACK FORMAT

The beginnings of both the ID field and the data field are flagged by unique characters called address marks.

An address mark is two bytes in length. The first byte is always an "A1" data pattern. This is followed by either an "FE" pattern which is the pattern used to define an ID address mark, or an "F8" which is a data address pattern.

The "A1" pattern violates the encode rules for MFM by omitting on clock transition between bits 4 and 5. This makes the address mark patten unique to any other serial bit combination.

All ID and data field are followed by a 16-bit cyclic redundancy check (CRC) character used for data verification. Each CRC polynomial is unique for a particular data pattern.

Surrounding the ID and data fields are gaps called Interrecord gaps.

6.2 GAP LENGTH CALCULATIONS

6.2.1 Gap 1

The purpose of Gap 1 is to provide a head switching recovery period so that, when switching from one track to another, sequential sectors may be read without waiting the rotational latency time. In addition, Gap 1 allows

physical position "drift" of the index pulse as a function of drive temperature. Gap 1 should be at least 22 bytes (30 bytes recommended) long to correspond with the head switching time and index drift. Gap 1 is immediately followed by a sync field for the ID field of the first sector.

6.2.2 Gap 2

Following the ID field, and separating it from the data field, is Gap 2. Gap 2 provides a known area for the data field write update to occur. The remainder of this gap also serves as the sync-up area for the data field address mark. The length of Gap 2 is determined by the data separator lock-up performance.

6.2.3 Gap 3

Gap 3, following the data field, is a speed variation tolerance area. This allows for a situation where a track has been formatted while the disk is running two percent slower (3531 rpm), then write updated with the disk running at highest speed (3603 rpm).

Gap 3 should be at least 15 bytes in length (this includes two bytes for write turn off).

6.2.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track. This allows the disk to rotate at the highest rated speed without overflowing the track during a format operation. The format operation which writes the ID fields, begins with the first encountered index and continues to the next index.

6.3 WRITE PRECOMPENSATION

Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This is a large factor contributing to bit shift. Other phenomena such as random noise, speed variation, etc., will also cause bit shift, but to a lesser degree.

The effect of bit shift can be reduced by a technique call precompensation, which, by detecting which bits will occur early and which bits will occur late, can effectively minimize the shift by writing these bits in the opposite direction of the expected shift. Bit shift is more apparent on the innermost dat tracks due to pulse crowding. Therefore, precompensation should only be at track numbers greater than or equal to 128. The optimum amount of precompensation for a 706/712 drive is 12 nsec for both early and late written bits. Table 6-1 shows various bit patterns for precompensation. Precompensation pattern detection bits are shifted through a 4-bit shift register. The bit is written out of the third position.

☆ **TABLE 6-1.** WRITE PRECOMPENSATION

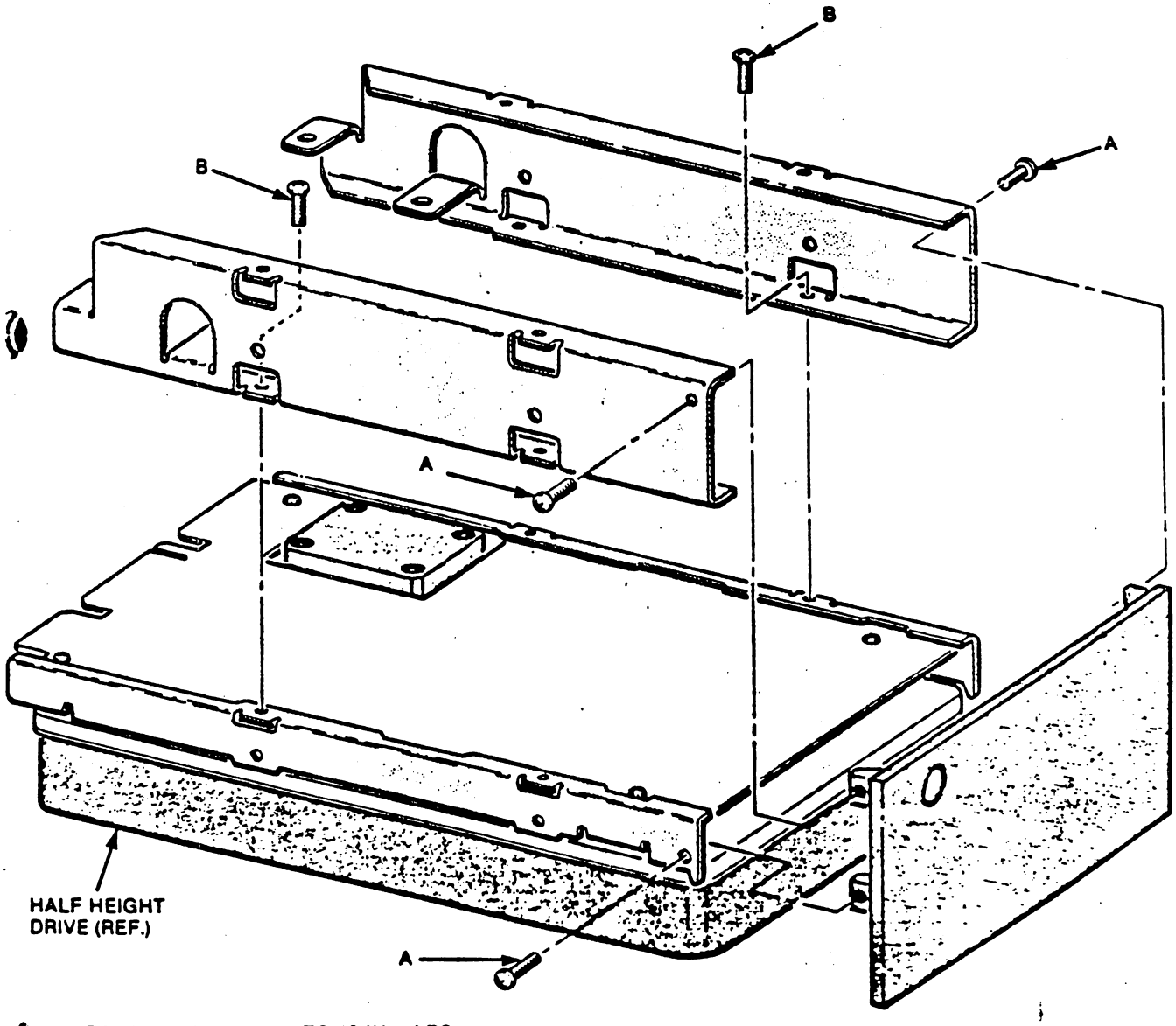
WRITE POSITION	DIRECTION OF SHIFT
0 0 0 0	= ON TIME CLOCK
0 0 0 1	= LATE CLOCK
0 0 1 0	= ON TIME DATA
0 0 1 1	= EARLY DATA
0 1 0 0	= ———
0 1 0 1	= ———
0 1 1 0	= LATE DATA
0 1 1 1	= ON TIME DATA
1 0 0 0	= EARLY CLOCK
1 0 0 1	= ON TIME CLOCK
1 0 1 0	= ON TIME DATA
1 0 1 1	= ———
1 1 0 0	= ———
1 1 0 1	= ———
1 1 1 0	= LATE DATA
1 1 1 1	= ON TIME DATA

BIT IS WRITTEN OUT OF THIRD POSITION 39026-24

SECTION VII
CUSTOMER INSTALLABLE OPTIONS

7.1 FULL-HEIGHT FACEPLATE KIT

One of the customer installable options currently available for the Shugart 706/712 disk drives is the Full-height Faceplate Kit, P/N 061597-0. See figure 7-1.



TORQUE SCREWS, B, TO 10 IN.—LBS.

TORQUE FRONT PANEL MOUNTING SCREWS A TO 2.5 IN.-LBS.

39402-01

FIGURE 7-1. FULL HEIGHT FACEPLATE KIT

7.2 LOW-POWER SLOW START JUMPER

In certain system configurations it may be desireable to use a Low-Power Slow Start mode of initialization of the drive. In cases when this is necessary, the mode can be selected by grounding pin 13 of the microprocessor.

On early versions (i.e., MLC 4 only) of the 706/712 PCB (P/N 26141 and 26159) this is accomplished by shorting between pins 12 and 13. See figure 7-2.

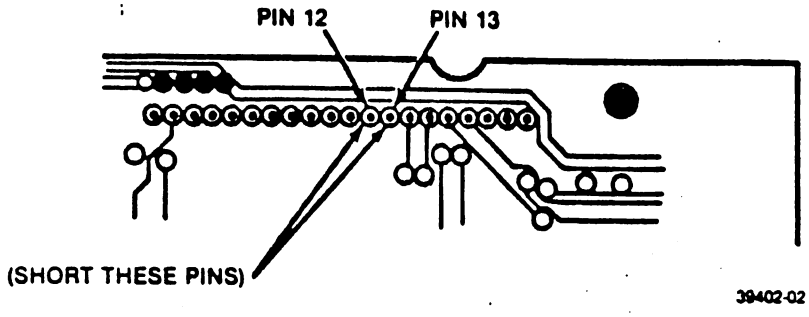


FIGURE 7-2. LOW POWER OPTION (EARLY MODELS)

On later versions (MLC 5 and above) it is necessary to fabricate a small jumper and install it in location E3 of the PCB. See figure 7-3.

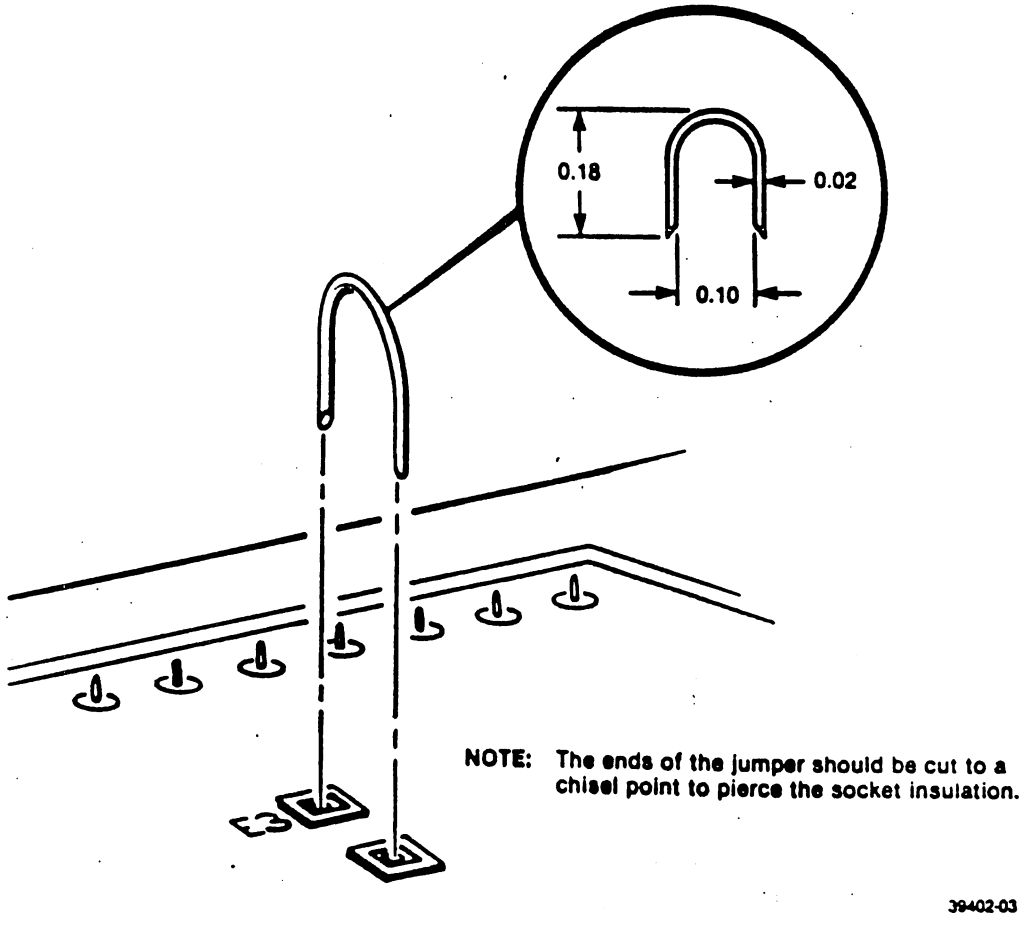


FIGURE 7-3. JUMPER INSTALLATION AND FABRICATION

In each of the above applications, grounding is to be applied to the solder side of the PCB, and removal of the board is not necessary.

SECTION VIII
THEORY OF OPERATIONS

8.1 INTRODUCTION

All of the tasks of the PCB microprocessor are separated into the following groups:

a. High priority time critical tasks

b. Lesser priority time critical tasks.

c. System initialization tasks

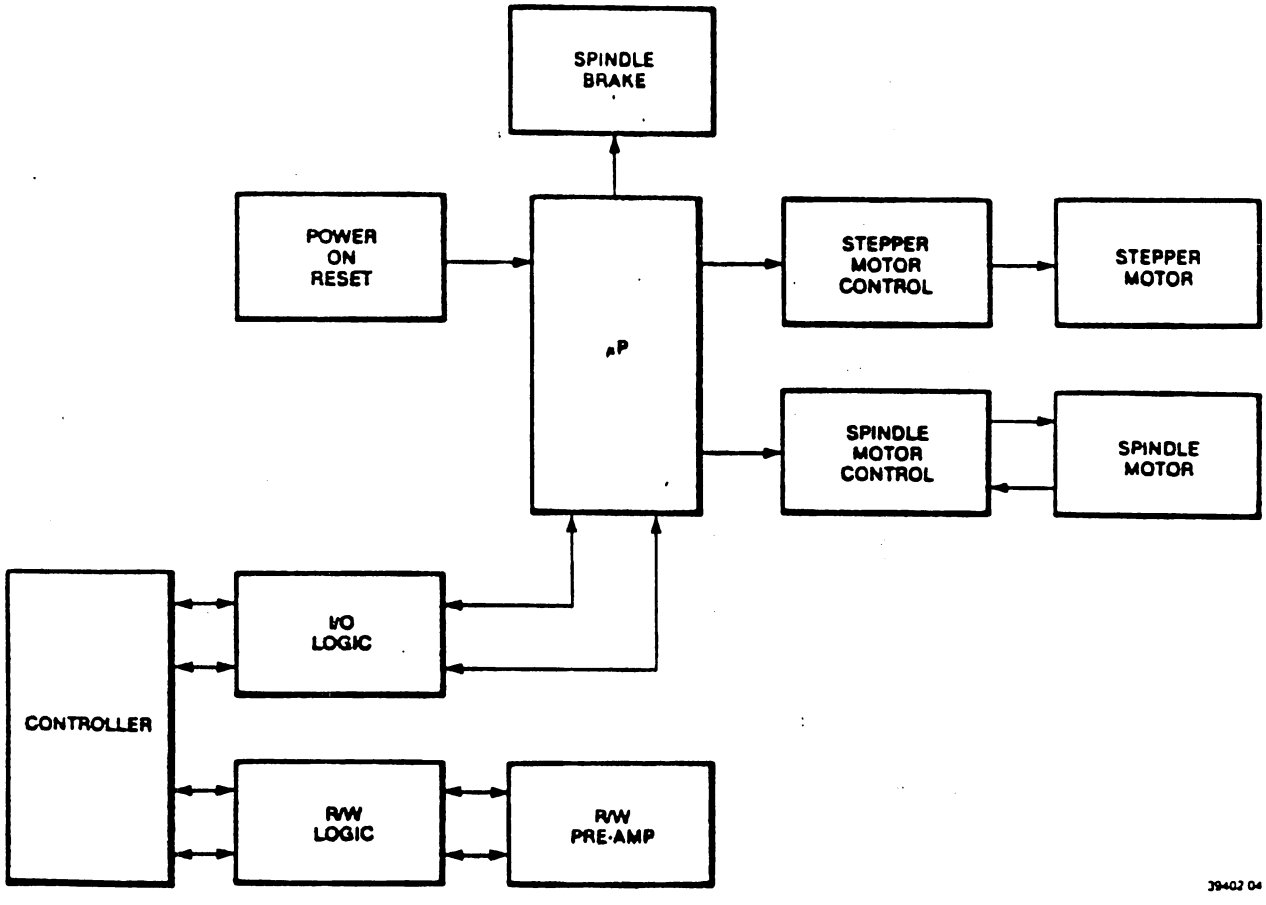


FIGURE 8-1. LOGIC DIAGRAM

8.2 HIGH PRIORITY CRITICAL TASKS (FOREGROUND)

The high priority time critical tasks consist of the following:

a. Generate the spindle motor waveform and measure the revolution time.

b. Detect and accumulate the step pulses from the interface.

c. Generate the stepping waveforms applied to the stepper motor, and perform the actuator velocity ramping (up and down) including pulse width modulation.

d. Time out the actuator damping interval.

These tasks are updated once each 90 μsec by using the microprocessor's internal timer to generate an interrupt for each update. These tasks cannot be interrupted by another task while they are being executed.

The set of program routines associated with these tasks is collectively called the "foreground."

Foreground routines are arranged so that they will sequentially execute one after the other, with each routine performing any necessary action, then handing control to the next routine. The last routine turns processing over to other tasks until the next timer interrupt arrives, at which the foreground process starts over. See figure 8-2.

The following subparagraphs detail the actual foreground routines.

8.2.1 Foreground Loop Control

This is the entry point for the 90 μsec interrupt request which is set up at the beginning of the "background" routines. Refer to paragraph 8.3.

This routine saves the accumulator, clears the timer interrupt flag, and updates the background gate counter. Control then passes to the Spindle Motor Foreground.

8.2.2 Spindle Motor Foreground

This measures the revolution period in increments of foreground time by being triggered by INDEX. It then generates a Pulse Width Modulated (PWM) waveform to control spindle motor power. Control now passes to Motor Fault Foreground.

8.2.3 Motor Fault Foreground

This routine determines if the spindle motor speed is correct. If it is not, control is passed to the Foreground End and Interrupt Return routine and all seek functions are skipped. If speed is correct, control passes to the Step Input Buffering Function.

8.2.4 Step Input Buffering Function

If Step Input is not enabled, this means that actuator seeks are still in process, in which case this routine exits immediately to the Stepper Damping Time Out routine. If Step Input is enabled, this routine adds any additional steps to the total step count; the direction is saved; the Step Input flag is disabled; and the Ramp Calculate flag is set true. Control will then pass to the Stepper Damping Time Out Routine.

8.2.5 Stepper Damping Time Out Routine

Damping can be enabled through the Seek Function Foreground or Actuator Lubricant Unstick Routine (Background). If it is not enabled, the routine exits to the Seek Function Foreground. If it is enabled, the actuator is decelerated somewhat with a track arrival delay. This is followed by an additional settling delay which also allows checking for any additional step pulses. If any more step pulses are received, the routine exits early without Setting Seek Complete true. Exit is made to Seek Function Foreground.

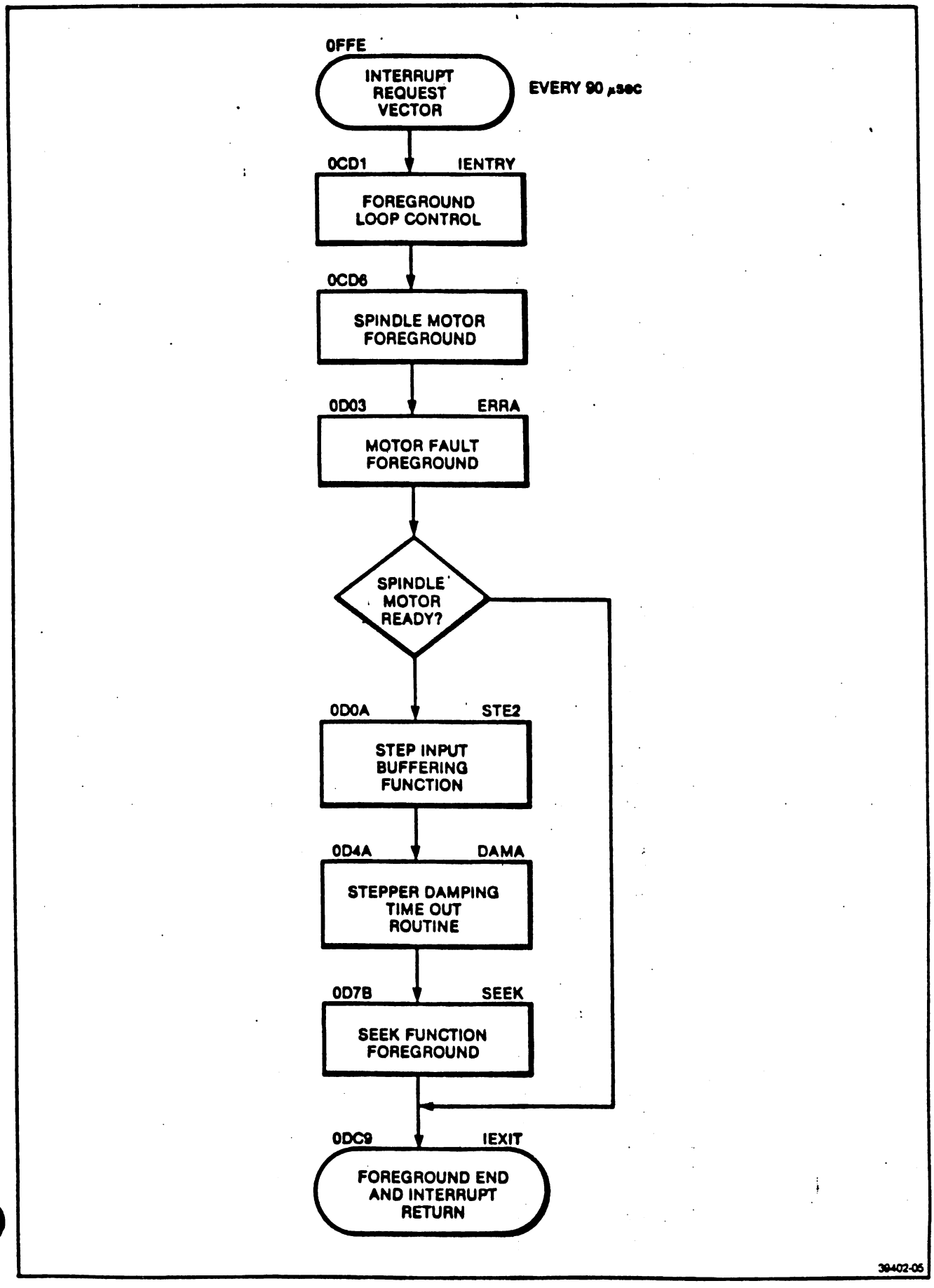


FIGURE 8-2. FOREGROUND ROUTINES SEQUENCING

8.2.6 Seek Function Foreground

The seek flag is set from the Seek Ramping Calculate Function (background). If the seek flag is set, then a step delay is provided to allow time for step settling. If the delay is not done, then the routine exits to Foreground End and Interrupt Return. Otherwise the routine gets a ramp table value and determines if ramping is up or down. If ramping is down and seek is complete, then the actuator slew voltage is tuned off; the seek fuction is disabled; and the damping fuction is enabled.

If seek is not complete, and ramping is up or down, then step timing is saved; direction is determined; the cylinder address is updated; the new stepper phase is output on port B (see table 8-1); and the routine exits to Foreground End and Interrupt Return.

TABLE 8-1. I/O PORT CONFIGURATION

	PIN NO.	ASSIGNMENT
PORT A	PA7	+ DIR
	PA6	+ TRK 000
	PA5	+ FAULT
	PA4	-FAULT CLEAR
	PA3	-READY
	PA2	+ SEEK COMPLETE
	PA1	UNUSED
	PA0	+ INDEX (+ EDGE)
PORT B	PB7	+ COIL A
	PB6	+ COIL B
	PB5	+ COIL C
	PB4	+ COIL D
	PB3	-STEPPER ENABLE
	PB2	UNUSED
	PB1	UNUSED
	PB0	UNUSED
PORT C	PC7	-SLOW SPIN-UP
	PC6	+ REDUCE IW
	PC5	-RUN SPINDLE
	PC4	+ BRAKE PICK
	PC3	+ LED
	PC2	UNUSED
	PC1	UNUSED
	PC0	UNUSED
PORT D	PD7	+ SEL
	PD6	-DELAY
	PD5	-EXERCISE
	PD4	+ ACTUATOR SLEW
	PD3	+ STEP INPUT COUNT D
	PD2	+ STEP INPUT COUNT C
	PD1	+ STEP INPUT COUNT B
	PD0	+ STEP INPUT COUNT A

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8.2.7 Foreground End and Interrupt Return

This routine simply restores the accumulator from the stack and returns to the background.

8.3 LESSER PRIORITY CRITICAL TASKS (BACKGROUND)

The less time critical tasks are referred to as the "background" and are performed in between foreground interrupts, after the last foreground routine has ended, but before the foreground restarts. Average foreground execution time is approximately 55 μsec; therefore, out of every 90 μsec time period, the background has about 40 μsec to perform its tasks.

The background tasks are arranged sequentially like the foreground, however the last background routine hands control back to the first, thereby establishing a continuous loop. For convenience in timing certain non-critical events, the background loop rate in made self-synchronous with the foreground.

This is accomplished by allowing the beginning of background loop execution to proceed only on every fifth foreground interrupt. Therefore, background loop execution time is 450 μsec (5 × 90 μsec). The only exception to this is that the spindle motor background control routines are exempted from this "gating" process in order to minimize control system phase error.

The less time critical tasks consist of the following:

a. Calculating the duty cycle of the spindle motor power waveform, based upon the measured revolution time.

b. Monitoring the disk revolution time to generate the Drive Ready signal to the interface, and to determine if spindle motor faults have occurred.

c. Determining the necessary ramp-up and ramp-down parameters to perform a seek, given the step pulse count as received from the interface.

d. Performing the automatic actuator reset to cylinder 0 during the drive power-up.

e. Moving the actuator a full stroke in and out twice in order to distribute the actuator bearing lubricant during drive power-up.

f. Self-exercising the actuator with continuous random seeks and checking for seek errors when the drive exercise jumper has been installed.

The following subparagraphs detail the actual background routines. See figure 8-3.

8.3.1 System Startup Code

This code initializes the stack pointer and binary arithmetic mode with the following results (see table 8-1):

a. On Port A the READY and FAULT flags are set to false, and the FAULT CLEAR line is momentarily pulsed true.

b. On Port B the stepper coil bits are put into Phase A and the Stepper Enable is made false.

c. On Port C, Reduce Write Current and Brake Pick are true; Run Spindle and LED are false.

d. On Port D the Actuator Slew is false.

On all four ports, all bits not assigned as outputs are configured as inputs.

The routine then jumps to Spindle Motor Initialization.

8.3.2 Spindle Motor Initialization

This routine initializes the spindle motor control constants and variables. The spindle brake is held at high current for about one second. Brake power is then reduced and the spindle motor is ramped up to 100 percent for about 8 seconds, using pulse width modulation.

Full spindle power is held for an additional X seconds while the spindle index is counted. If X or more index pulses have occurred, then control goes to Seek Function Initialization, otherwise there is a spindle failure and control goes to the Microprocessor Control Fault Indicator function.

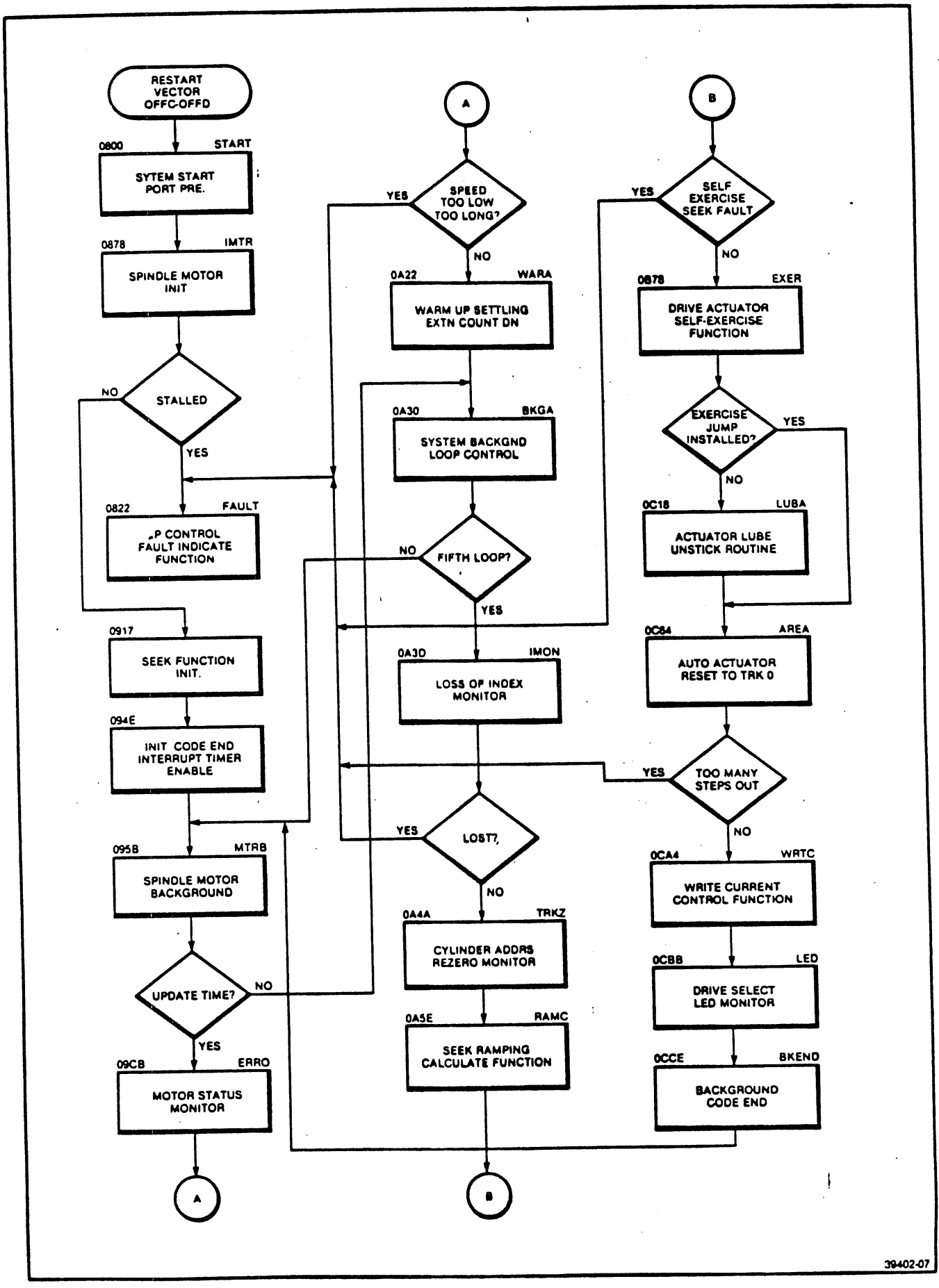

FIGURE 8-3. BACKGROUND ROUTINES SEQUENCING

8.3.3 Microprocessor Control Fault Indicator Function

This routine removes power to the spindle motor and stepper motor; the foreground interrupts are halted, and the READY line is set false. The FAULT latch is pulsed and:

a. If no jumpers are installed, or if the delay jumper (E1) is installed, then all motor power is removed and the LED is flashed as shown in table 8-2.

b. If only the exercise jumper (E2) is installed, then the microprocessor returns to System Startup and restarts.

TABLE 8-2. LED FAULT CODES

NUMBER OF FLASHES	SOURCE OF FAULT
1	RESERVED.
2	RESERVED.
3	SPINDLE FAILED TO START.
4	SPINDLE FAILED AFTER ACHIEVING FULL SPEED SUCCESSFULLY.
5	ACTUATOR FAILED TO RESTORE TO CYLINDER ZERO.
6	ACTUATOR SEEK ERROR DETECTED DURING DRIVE SELF-EXERCISE.
7	LOSS OF SPINDLE INDEX SIGNAL.

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8.3.4 Seek Function Initialization

This initializes the actuator seek function control constants and variables. The routine then goes directly to Initialize Code End.

8.3.5 Initialize Code End

This starts the 90 μsec foreground interrupts, and the system enters the continuous background loop by going directly to Spindle Motor Background.

8.3.6 Spindle Motor Background

This takes the index time flag, passed from the foreground, and determines if the speed is correct. If it is, no changes are made and the routine goes to the Motor Status Monitor.

If the speed is not correct, the index time error is integrated and added to the current index time error to determine and set the motor power factor. The routine then goes to the Motor Status Monitor.

8.3.7 Motor Status Monitor

This monitors the index time to determine if the motor speed is out of tolerance. It sets the FAULT line to true if the speed varies more the ± 1.61 percent for six revolutions. If the speed drops below 92 percent for more than ten revolutions, the routine jumps to Control Fault Indicate Function (paragraph 8.3.3), otherwise it goes to the Warm-up Settling Extension Countdown.

8.3.8 Warm-up Settling Extension Countdown

A countdown of two minutes allows drive warm-up time and provides longer seek settling time during warm-up. The routine then goes to System Background Loop Control.

8.3.9 System Background Loop Control

If five 90 μsec foreground loops have occurred since the last time this function was entered, then control proceeds to Loss of Index Monitor; otherwise control goes back to Spindle Motor Background (paragraph 8.3.6).

8.3.10 Loss of Index Monitor

If INDEX has not occurred during the last 115 msec, then control goes to the Control Fault Indicate Function (paragraph 8.3.3); otherwise control proceeds to Cylinder Address Rezero Monitor.

8.3.11 Cylinder Address Rezero Monitor

If the actuator is on cylinder 0 and the exercise jumper (E2) is not installed, then the cylinder address variables are set to zero; otherwise control proceeds to the next step.

8.3.12 Seek Ramping Calculate Function

If Ramp Calculate is not enabled by either the Step Input Buffering Function (paragraph 8.2.4) or the Drive Actuator Self-exercise Function (paragraph 8.3.13), the control proceeds to the Drive Actuator Self-exercise Function.

If Ramp Calculate is enabled, it accepts the step sum and direction of inputs and produces the necessary seek control values to effect a buffered seek. The actuator track zero flag is monitored and outward seeks from cylinder 0 are inhibited, unless the delay jumper (E1) is installed in which case such seeks are allowed (this facilitates the adjustment of the crash stop and track zero flag).

If the exercise jumper (E2) is installed, the actuator cylinder address variable will be compared with the track zero flag to detect possible seek errors during self-exercise.

If seek errors are detected, control goes to the Control Fault Indicate Function (paragraph 8.3.3), otherwise control passes to Drive Actuator Self-exercise Function.

8.3.13 Drive Actuator Self-exercise Function

If the exercise jumper (E2) is installed then this routine uses its internal random number generator to create a continuing series of pseudo-random seek values which insure full disk coverage during exercise.

If the delay jumper (E1) is not installed, this function will delay itself for 10 msec; if it is installed, the delay will be 500 msec. If the exercise jumper (E2) is not installed the control proceeds to Actuator Lube Unstick Routine.

8.3.14 Actuator Lube Unstick Routine

This routine is enabled by a flag passed from the Automatic Actuator Reset to Track Zero function, otherwise known as Recal (recalibrate). It seeks from cylinder 0 to the end cylinder and back twice. It enables the damping function when done, and control passes to the next step.

8.3.15 Automatic Actuator Reset to Track Zero (Recal Function)

Upon system start, the Seek Function Initialization (paragraph 8.3.4) sets the Recal Flag (RCFLG) to indicate that the actuator arm has not been calibrated to track zero and to provide for a ten revolution delay before Recal. The Motor Status Monitor (paragraph 8.3.7) checks to see of the unit has been recalibrated. If not, it checks the disk revolution period to see if the disk is running fast enough.

If it is, RCFLG is incremented once each time the Motor Status Monitor is entered. After ten entries, i.e., ten disk revolutions, RCFLG is incremented to zero. If it is not, the routine is exited. If it is, the actuator is stepped outward 512 steps or until track zero is found.

The Actuator Lube Unstick Routine is enabled by setting the LUBE flag (paragraph 8.3.14) and control passes to the Write Current Control Function.

8.3.16 Write Current Control Function

This routine sets +REDUCE IW signal on port C, bit 6 high, when the cylinder address (TRKL and TRKH) is greater than the write current switchover point (WRITSW). See table 8-1.

The routine then passes control to Drive Select LED Monitor.

8.3.17 Drive Select LED Monitor

This function checks port D, bit 7 (+SEL), to see if it is high; indicating that the drive is selected. If it is, bit 3 in BKPC (port C Backgroung Bit Control) is set high. If +SEL is low, then bit 3 in BKPC is set low. See table 8-1.

Control now proceeds to the next routine.

8.3.18 Background Code End

This routine merely jumps to the beginning of Spindle Motor Background, continuing the background loop.

8.4 SYSTEM INITIALIZATION TASKS

System initialization tasks are performed only once for each microprocessor restart. Once most initialization tasks are completed, the foreground interrupts are started and control is given to the continuous background loop. Remaining initialization tasks are completed in the background loop and make use of its time (as gated in the foreground) to time necessary events.

These initialization tasks consist of:

a. Setting up the microprocessor internal registers and placing the various input and output pins of such into the proper initial state.

b. Clearing the drive fault latch.

c. Applying power to the spindle motor and verifying that it begins to rotate properly.

SECTION IX
PACKAGING INSTRUCTIONS

9.1 UNCRATING

Due to the integral spindle actuator lock, no special instructions for uncrating or packaging are required.

The Shugart 706/712 drives are shipped in two manners as follows:

a. A single unit in a single carton (figure 9-1).

b. Ten units in a single carton (figure 9-2).

It is suggested that packing materials be kept in case the unit must be returned to Shugart for repair. Regardless, the unit must be individually packaged in comparable packing as shipped to preclude damage in shipping and handling. Damage to the unit as a result of inadequate packaging will void the warranty on the unit.

Inspection of the unit(s) should be made in accordance with the specifications of paragraph 9.2.

9.2 RECOMMENDED RECEIVING INSPECTION

9.2.1 Packaging and Identification

The individual and palleted containers should be inspected for exterior damage.

Each shipment contains a packing slip, listing as a minimum the Customer Purchase Order Number, quantity, stock number, dash level, and MLC level.

Each unit is individually protected as shown in figures 9-1 and 9-2.

The container should be free of foreign matter and clean.

9.2.2 Mechanical Inspection

The following visual checks should be made for each unit:

a. Verify the model number, serial number, and MLC level.

b. Check for loose screws and sub-assemblies.

c. Inspect for loose connectors or missing jumpers.

d. Check for exposed wires on cables and connectors.

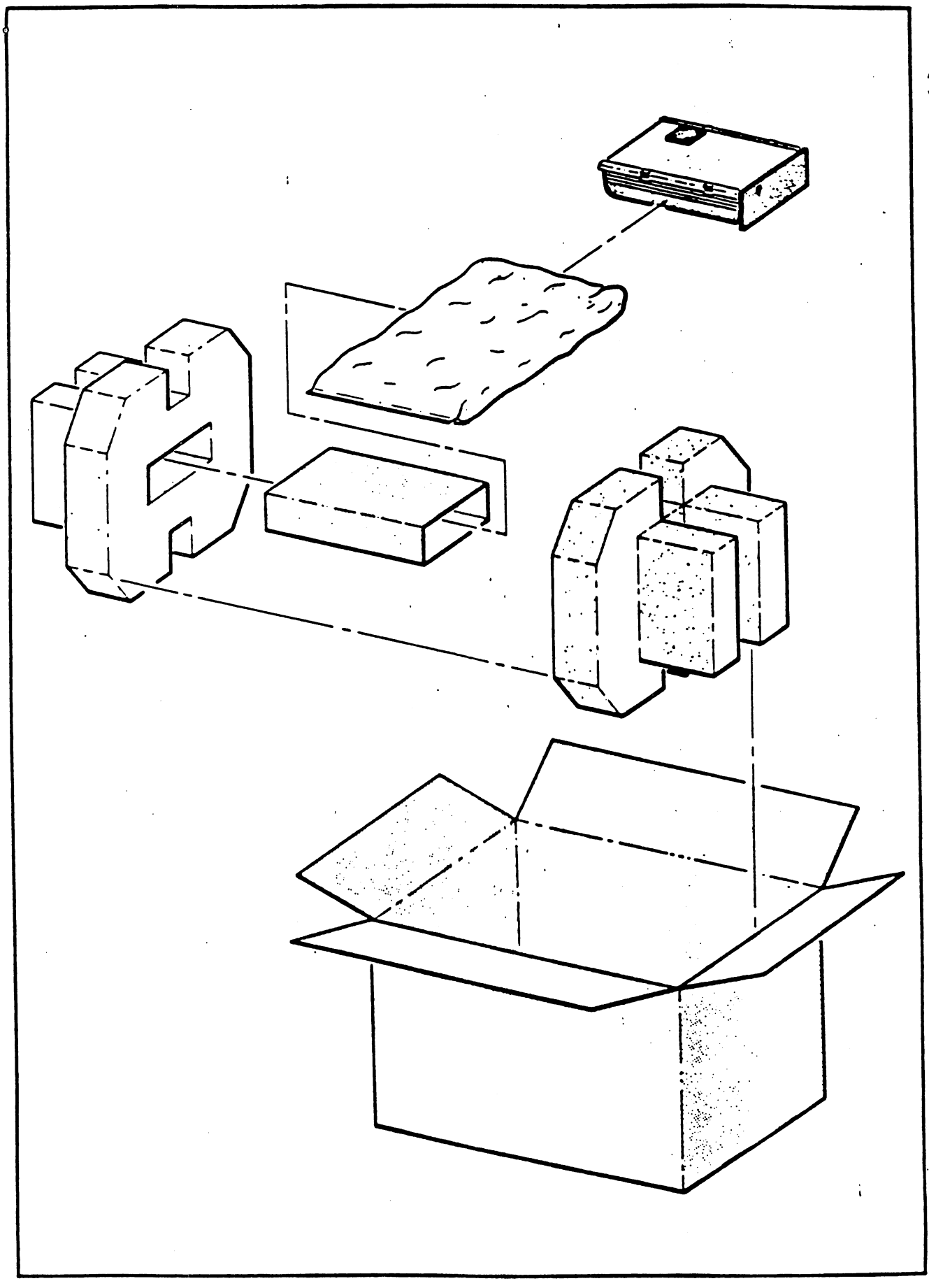

FIGURE 9-1. SINGLE UNIT PACKAGING CONFIGURATION

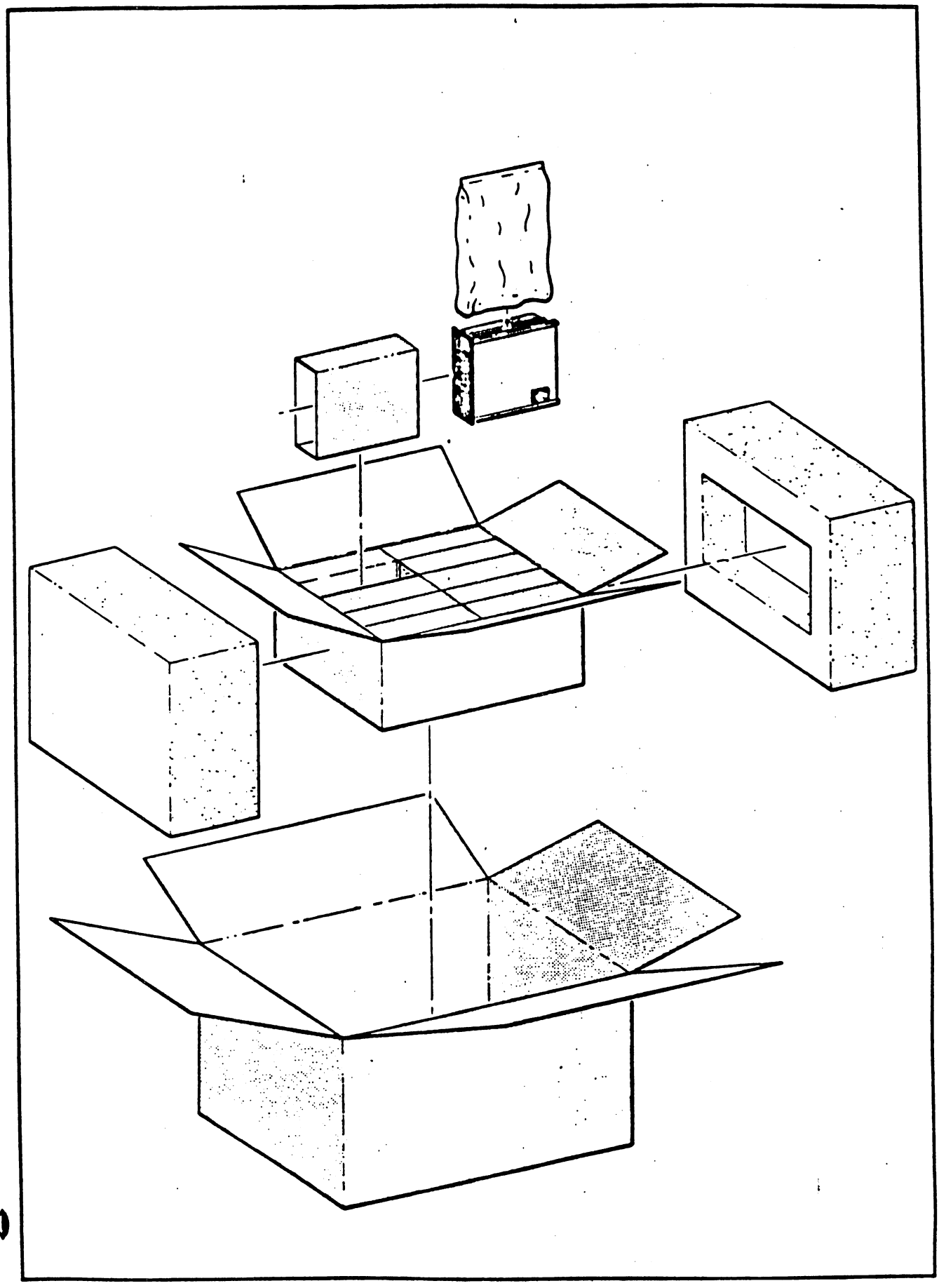

FIGURE 9-2 TEN UNITS PACKAGING CONFIGURATION

°9.2.3 Functional Testing

Shugart recommends using the ADC T-650 Tester with Level E-6 Software. This tester is specially programmed for all 5.25 and 8-inch fixed disk products.

The functional tests performed by the ADC Tester are as follows:

D = Prompt character and indicates the program is ready to accept commands from the user.

IP = Inspect Phase command code is available for displaying the contents of a phase.

PP = Print Parameters. See table 9-1

TABLE 9-1. PRINT PARAMETERS

STEP RATE (×0.1 MS)	= 30
MARGIN CODE	= 3
MAX. HEAD	= 3
STEP MODE	= 0
MAX. CYLINDER	= 319
MAX. ERROR CNT	= 0
BUFFER ERROR RETRY LIMIT	= 5
PRECOMP START CYLINDER	= 128
LOW WRITE I START CYLINDER	= 200
DENSITY MODE	= 1 MKM 32 + 256

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The following example (table 9-2) is a print out of the test program with the Printer Option for the ADC.

TABLE 9-2. TEST PROGRAM

WHICH PHASE? 0		
MS/	4	SET MARGIN CODE = 3
TM/	1	TEST MARGINS
P2/	1	SET WORST CASE PATTERN
F1/	1	FORMAT DISK DENSITY 1
WT/	1	WRITE DATA INTEGRITY TEST
RT/	1	READ DATA INTEGRITY TEST
RR/	500	RANDOM READ DATA TEST
RV/	1	READ REVERSE TEST
WA/	1	OVERWRITE TEST
RA/	1	OVERREAD TEST
WC/	1	WORST CASE SEEK TEST
TM/	1	TEST MARGINS
HO/	1	HOME THE DRIVE
PK/	353	MAX CYLINDER

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9.3 PACKING FOR RESHIPPING

To prepare a drive for shipment:

a. Locate the heads to the Shipping Zone (refer to para. 1.4.8).

b. Place the drive in the protective plastic sleeve.

c. Place this configuration into the inner container.

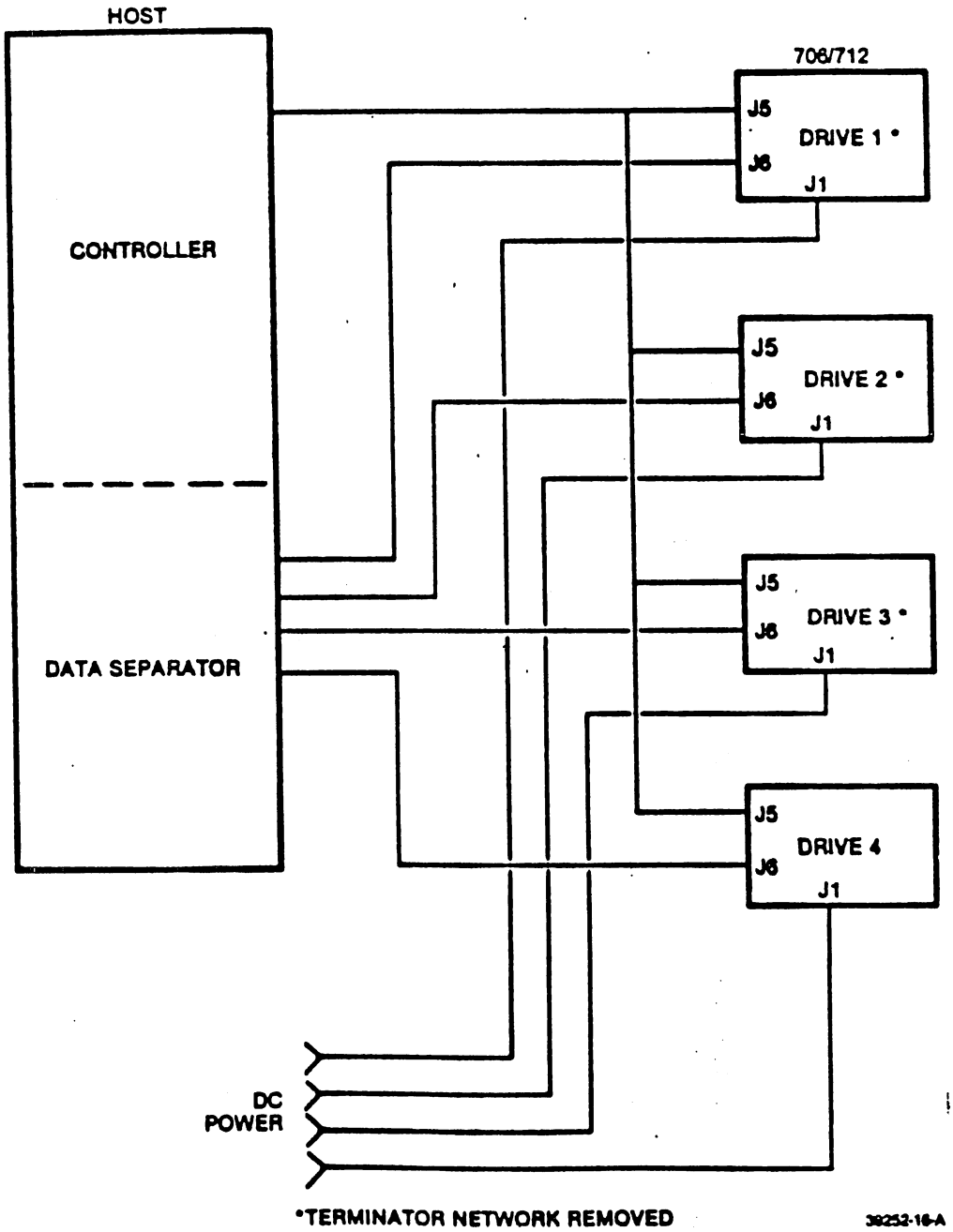
d. The inner container is to be sandwiched between the foam inserts.

e. The entire array is then placed into the outer container and sealed.

Failure to follow these procedures may result in damage to the drive(s).

SECTION X
DRIVE INTERCONNECT

The electrical connection between the Shugart 706/712 and the control system is shown in figure 10-1. For daisy-chain configurations, the terminating networks must be removed from all but the last drive in the chain. Refer to paragraph 2.3.



☆ FIGURE 10-1. MULTIPLE DRIVE CONFIGURATION

SECTION XI
SPARE PARTS

Shugart Corporation, in its commitment to provide service to its customers, has available a dedicated and professional Spare Part/Logistic support group to support the OEM customer base as well as the end user.

11.1 ROUTINE ORDER ENTRY

Routine orders (domestic open accounts) in the U.S. may be placed with Shugart Corporation by phone, facsimile, TWX, or by mail. All verbal orders will be booked as received but will require confirming purchase documents before the order is processed for confirmation or shipment.

PHONE:	(408) 737-7900 (Ask operator for Spares)
TWX:	(910) 339-9355
FACSIMILE:	(408) 735-7486
MAIL:	Shugart Corporation 475 Oakmead Parkway Sunnyvale, CA 94086 ATTN: Spare Parts Dept.

11.2 EMERGENCY ORDER ENTRY

Requests for parts required on an emergency basis should be communicated to Shugart Corporation by either TWX or phone. Be particularly careful to ensure that all applicable information is communicated.

SECTION XII
MAINTENANCE

12.1 INTRODUCTION

The Shugart 706/712 has been designed to require no maintenance under normal operating conditions. This section will discuss those steps to be taken in the event of a drive malfunction.

12.2 MAINTENANCE EQUIPMENT

The only equipment required is an ADC T-650 Tester and an oscilloscope. Refer to paragraph 9.2.3. for ADC test procedure.

12.3 DIAGNOSTIC TECHNIQUES

The 706/712's are equipped with a self-exerciser that supplements any diagnostic requirements.

12.4 TEST POINT LOCATIONS

Although test points are evident on the PCB, these are used for testing during the manufacturing operations. No testing is required of the end user.

12.5 TROUBLESHOOTING

Tables 12.1 through 12.3 show the procedures for determining possible problems.

TABLE 12-1. PCB VERSUS DRIVE FAILURES

DESCRIPTION	PROBLEM IS IN		
	THE DRIVE	THE PCB'S	EXTERNAL
MOST ERRORS OCCUR ON TRK 00	X		
ERROR OCCURS ON TRK 317	X		
WRITE FAULT IN WRITE MODE		X	
ONLY SELECT HEAD 0 AND HEAD 1 NOT HEAD 2 AND 3		X	
SYSTEM TIME OUT ERROR*	X	X	
DRIVE UNABLE TO COME UP TO SPEED*	X	X	
DRIVE NOT RUNNING TESTS WITH OTHER FIXED DRIVES**			X
BRAKE NOT FUNCTIONING RIGHT***		X	
GND BUTTON NOISY		X	

*TRY WITH KNOWN GOOD PCB'S. IT COULD BE THE DRIVE OR PCB'S.
**MAKE SURE TO CHECK THAT THE PCB'S HAVE DRIVE SELECT JUMPER AND TERMINATING JUMPERS.
***ADJUSTMENT OF BRAKE IS VERY IMPORTANT. USE 20 MIL SHIM FOR PROPER ADJUSTMENT BETWEEN BRAKE AND SPINDLE.

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TABLE 12-2. INSPECTION OF THE DRIVE

DESCRIPTION	PROBLEM IS IN		
	THE DRIVE	THE PCB'S	EXTERNAL
COVER DAMAGE/BEND IN COVER ETC.	X		
LEAK IN THE COVER GASKET	X		
CUT IN THE FLEX CABLE OR TRACES BROKEN IN FLEX CABLE	X		
PCB'S SMOKED/BURN OUT		X	
MISCELLANEOUS BROKEN PARTS	X		
NOISE FROM HDA MAY BE DUE TO: HEAD DAMAGE	X		
BAND BROKEN	X		
DISC NOT CLAMPED	X		
DAMPER LOOSE	X		
NOISY SPINDLE MOTOR	X		
DRIVE NOT COMING UP TO SPEED, COUNT THE NUMBER OF FLASHES ON LED			
1 TIME			X**
2 TIME (NOT ASSIGNED)			
3 TIME	X		
4 TIME	X		
5 TIME*	X	X	
6 TIME	X		
7 TIME	X		

*TRY WITH KNOWN GOOD PCB'S.
**MOST LIKELY THE POWER SUPPLY.

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TABLE 12-3. SIGNALS INSPECTION

CHECK THE DIFFERENTIAL SIGNAL ON TP11 AND TP12 IN BOTH WRITE AND READ MODE ON ALL THE HEADS AND RECORD AMPLITUDE AND RESOLUTION.

DESCRIPTION	PROBLEM IS IN		
	THE DRIVE	THE PCB'S	EXTERNAL
SIGNAL LOOKS OK ON SOME HEADS AND NOT ON OTHERS	X		
SIGNAL LOOKS GOOD ON TP11 AND TP12 AND NOT ON TP14 AND TP16		X	
DRIVE NOT HANDLING DATA		X	
WRITE FAULT WHEN TRYING TO WRITE		X	
DRIVE NOT SEEKING		X	
SIGNAL LOOKS GOOD ON TP11 AND TP12 DURING WRITE MODE BUT NO SIGNAL DURING READ MODE	X	X	

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12.6 CHECKS AND ADJUSTMENTS

The only adjustment necessary to the 706/712 is brake adjustment after installing a new PCB, or when necessary. The following steps define the procedures to be followed (see figure 12-1):

a. With the control PCB is its normal position, note that the brake pad and spindle motor can be seen through the slot opening.

b. Loosen the five screws securing the PCB to the drive; do not remove.

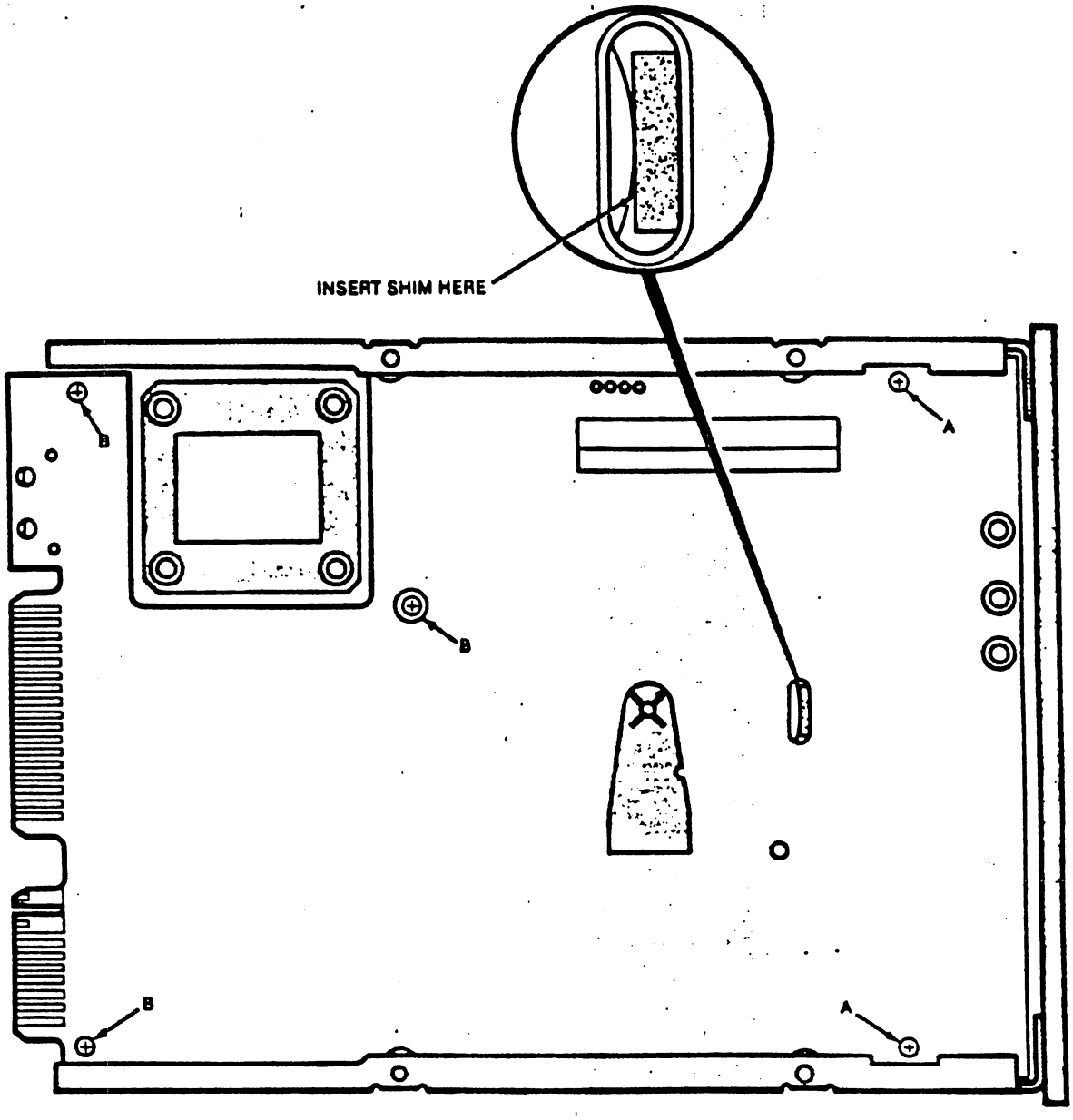

FIGURE 12-1. LOCATIONS DIAGRAM

c. Insert a flexible 0.020 inch (0.5 mm) shim between the brake pad and the spindle motor. Pull the PCB, from the connector end, allowing the brake pad to press firmly against the shim and spindle rotor.

d. Tighten the two screws labeled "A" to 5 in/lb (0.56 J) without releasing the PCB. Be sure that the brake pad is pressed firmly against the rotor.

e Insert another 0.020 inch (0.5 mm) shim under the screws labeled "B" and tighten them individually. Remove that shim and check for a 0.01-0.02 inch (0.3-0.5 mm) gap between the screw head and the board when light pressure is applied against the PCB. When properly fastened, the board should be allowed to "float" at the connector edge.

f. Remove all shims.

g. Push the brake pad away from the spindle rotor to see that the brake has sufficient stroke to clear the spindle. The stroke should be about 0.020 inch (0.5 mm).

h. After the five mounting screws have been properly tightened, fill the screw heads with glyptol.

12.7 REMOVAL AND REPLACEMENT PROCEDURES

12.7.1 Removal of Control PCB

The following steps define the process to be followed for the removal of the Control PCB (see figure 12-2):

a. Remove and retain the five mounting screws.

b. Lift the Control PCB and Front Panel Rail Assembly about 2 inches (51 mm) and unplug the spindle, stepper, and flex circuits.

c. Remove the PCB.

d. Replace the Front Panel Rail Assembly and mounting screws.

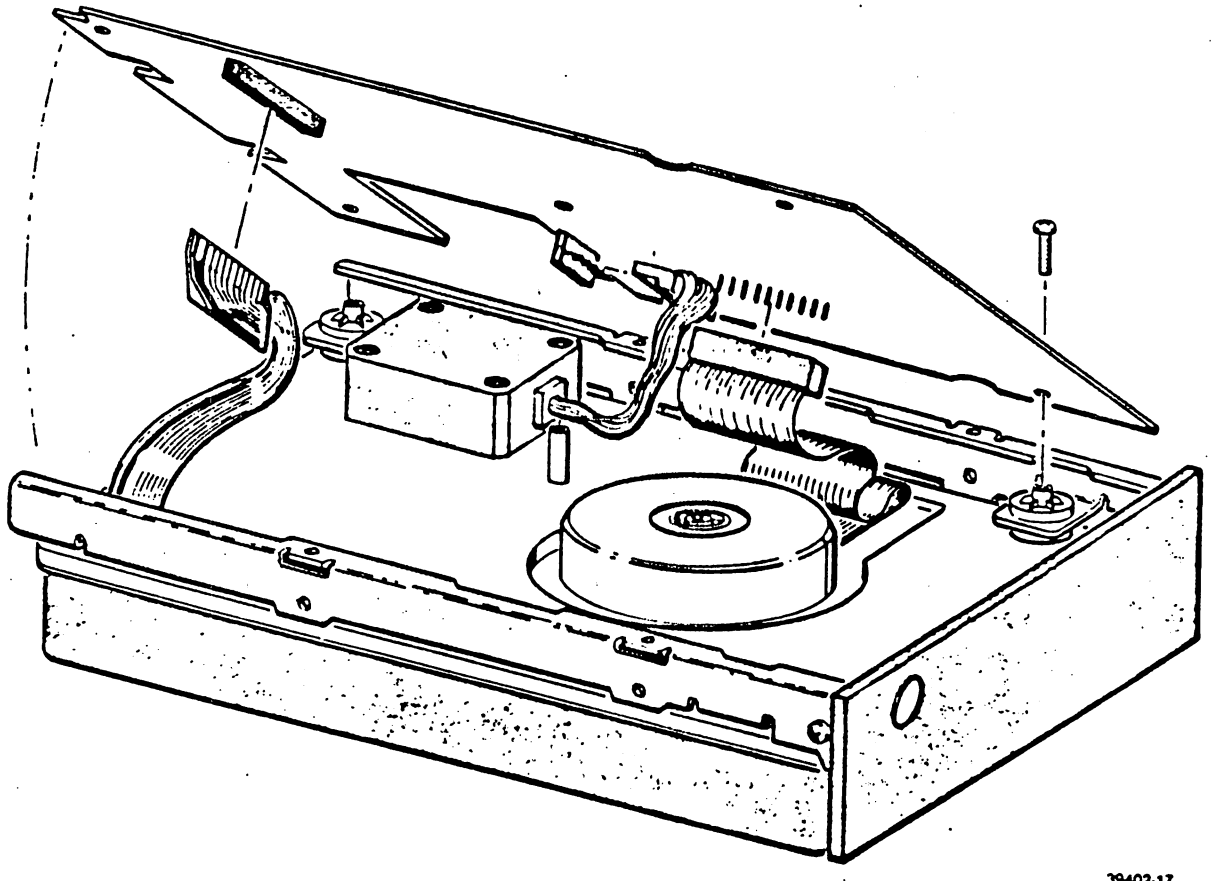

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FIGURE 12-2. REMOVAL/REPLACEMENT OF CONTROL PCB

12.7.2 Replacement of Control PCB

The following steps give the sequence with which to install a control PCB (see figure 12-2):

a. Remove and retain the five mounting screws.

b. Place the Control PCB on the drive at an angle, as shown, to allow the cables to be plugged in. Place the edge with the cut-out under the lip of the side rail, but over the stand-offs.

c. Plug in the three circuit cables. Be sure the cables are fully inserted into position.

d. Lower the Control PCB carefully on to the stand-offs with the cables not interferring with the spindle motor. Be sure the spindle motor cable is not sandwiched between the microprocessor and the baseplate.

e. Insert the five mounting screws through the board and into the stand-offs but DO NOT TIGHTEN UNTIL BRAKE ADJUSTMENT IS MADE (refer to paragraph 12.6).

12.8 ALIGNMENT PROCEDURES

The 706/712 drives require no special alignment.

12.9 PREVENTIVE MAINTENANCE

The 706/712 drives require no preventive maintenance.

SECTION XIII
ILLUSTRATED PARTS CATALOG

13.1 DESCRIPTION

The Illustrated Parts Catalog (IPC)is arranged so that the figure will always precede the parts listing and, when possible, will appear directly above the parts list or on the left hand page immediately preceding it.

The first number in the list will always refer to the reference number of the part within the figure.

Part numbers enclosed in parenthesis refer to parts belonging to a Next Higher Assembly (NHA) and are of importance only to those customers with alternate assemblies. Following the description of these parts, the designation NHA P/N _____ gives the part number of the assembly to which they pertain. When applicable to the customer's assembly, these alternate parts will be used in lieu of the part listed directly above them. Assume that the quantity per assembly for these alternate parts is the same unless otherwise directed.

When an assembly is referred to within a figure and a further breakdown is shown on another figure, then the referenced number will be called out.

13.2 INDENTED LEVEL

The parts list is indented to show the levels of assembly within a figure. The major assembly will always be unindented. All parts or assemblies that attach to the assembly will be indented one space. Parts within these assemblies will be indented two spaces and so on.

13.3 QUANTITY PER ASSEMBLY

The quantity listed is the quantity used on the major assembly. Major assemblies themselves will never have a quantity listed.

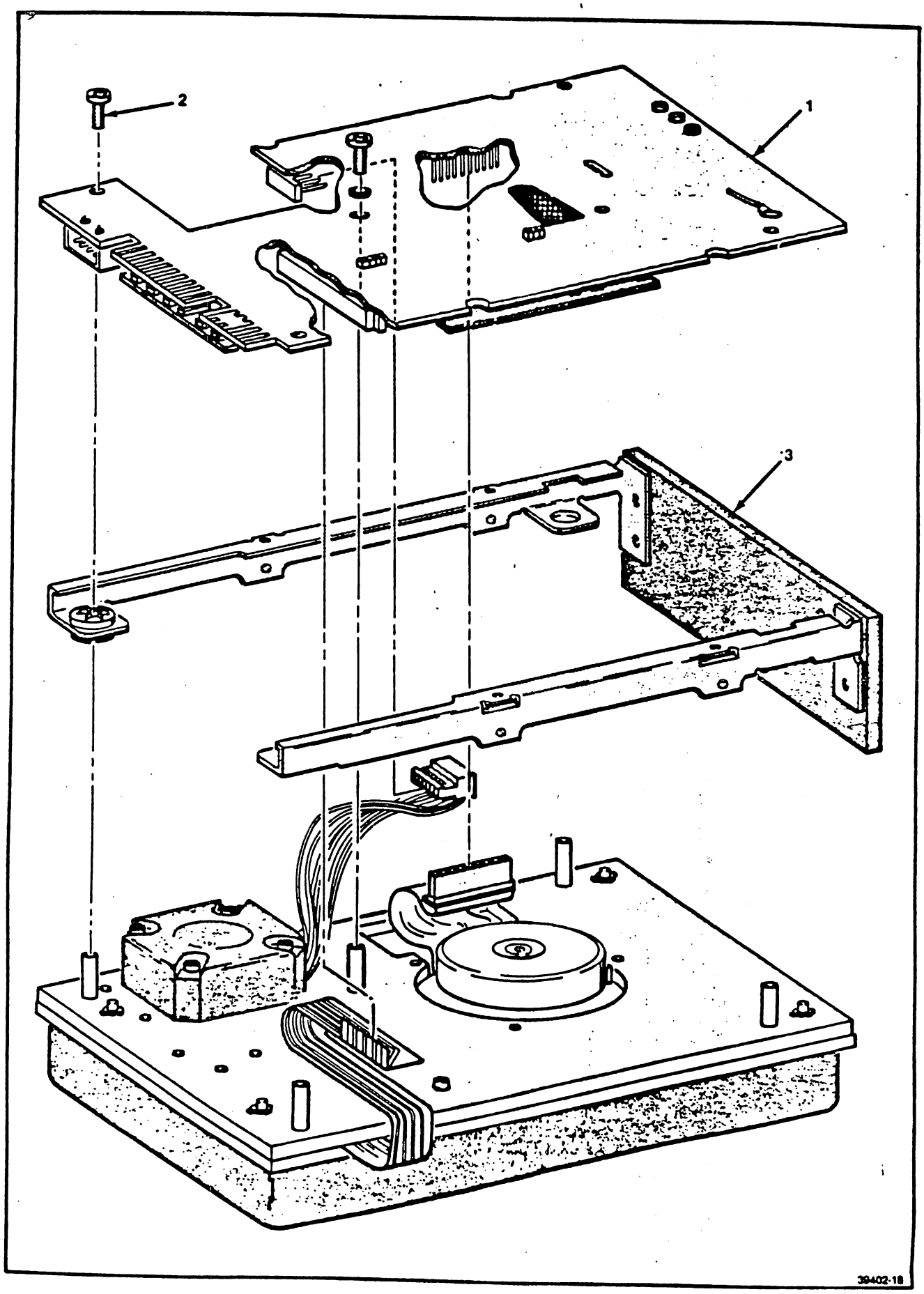

FIGURE 13-1. SHUGART 706/712 ASSEMBLY

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QUANTITY
1-1	26173-0 26177-0	CONTROL PCB (706) CONTROL PCB (712)	1
2	12233-0	SCREW, PHILLIPS, PAN HEAD (#4-40 x 5/16) WITH NYLON PAD	5
3	61213-2	FRONT PANEL AND RAIL ASSEMBLY	1

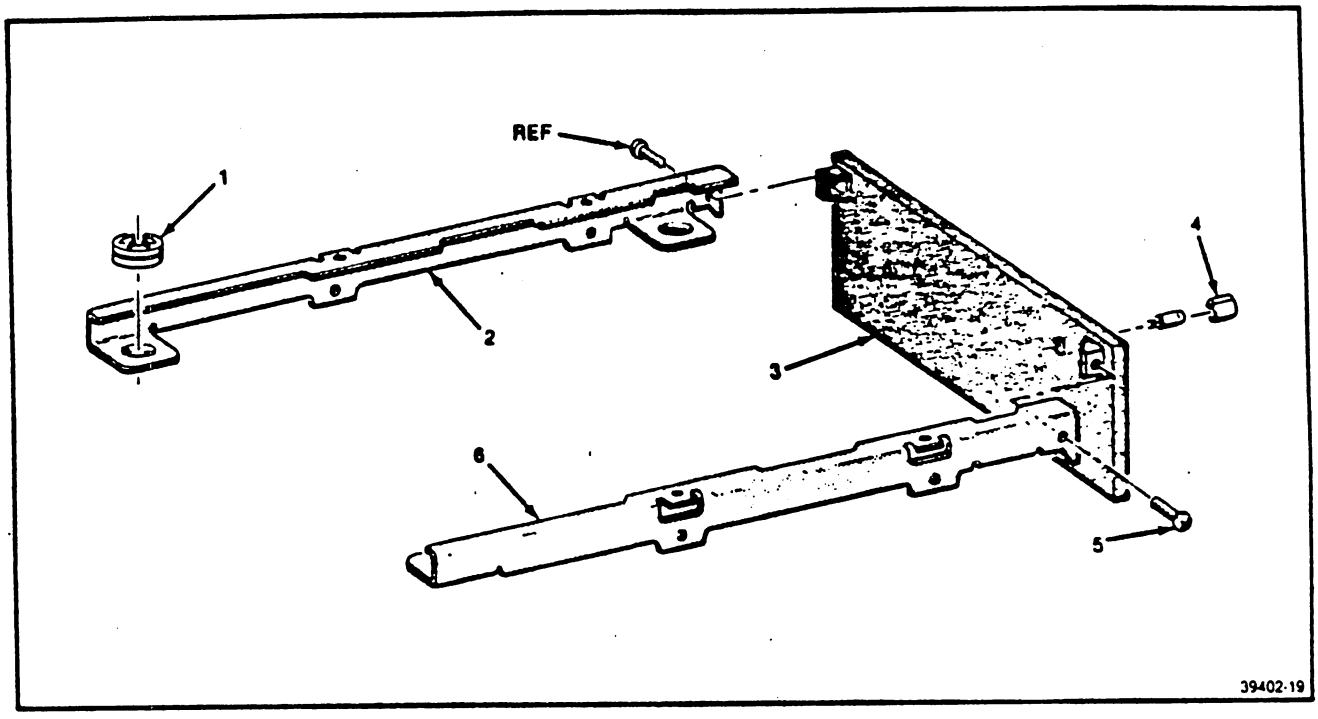

FIGURE 13-2. FRONT PANEL AND RAIL ASSEMBLY

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QUANTITY
2-1	61306-0	SHOCK MOUNT	4
2	61292-1	RAIL, RIGHT SIDE	1
3	61288-0	FRONT PANEL	1
4	11338-0	LENS	1
5	12207-0	SCREW, THREAD FORMING (#4-20 x 1/4)	2
6	61291-1	RAIL, LEFT SIDE	1

13.4 RECOMMENDED SPARE PARTS STOCKING GUIDE

The spare parts stocking guide is broken down into three levels. These levels are: Site or Field Support Engineer (level 1), Branch Office (level 2), and Depot or Headquarters (level 3). The quantities listed assume that the Site is replenished by the Branch immediately and the Branch replenished by the Depot within 30 Days.

The inventories that the levels can maintain are:

Site	1 to 20 machines
Branch	1 to 100 machines
Depot	
Depot only parts	Unlimited
Branch replenishment	Same as Branch ratio

Table 13-1 shows the spare parts required to support the 706/712 in the field.

TABLE 13-1. SHUGART 706/712 SPARE PARTS STOCKING GUIDE

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT
11338-0	LENS		4	8
26173-0	CONTROL PCB (706)	2	4	8
26177-0	CONTROL PCB (712)	2	4	8
61218-2	FRONT PANEL AND RAIL ASSEMBLY	1	4	8
61288-0	FRONT PANEL		2	4
61291-1	RAIL, LEFT SIDE		2	4
61292-1	RAIL, RIGHT SIDE		2	4
61306-0	SHOCK MOUNT		16	100

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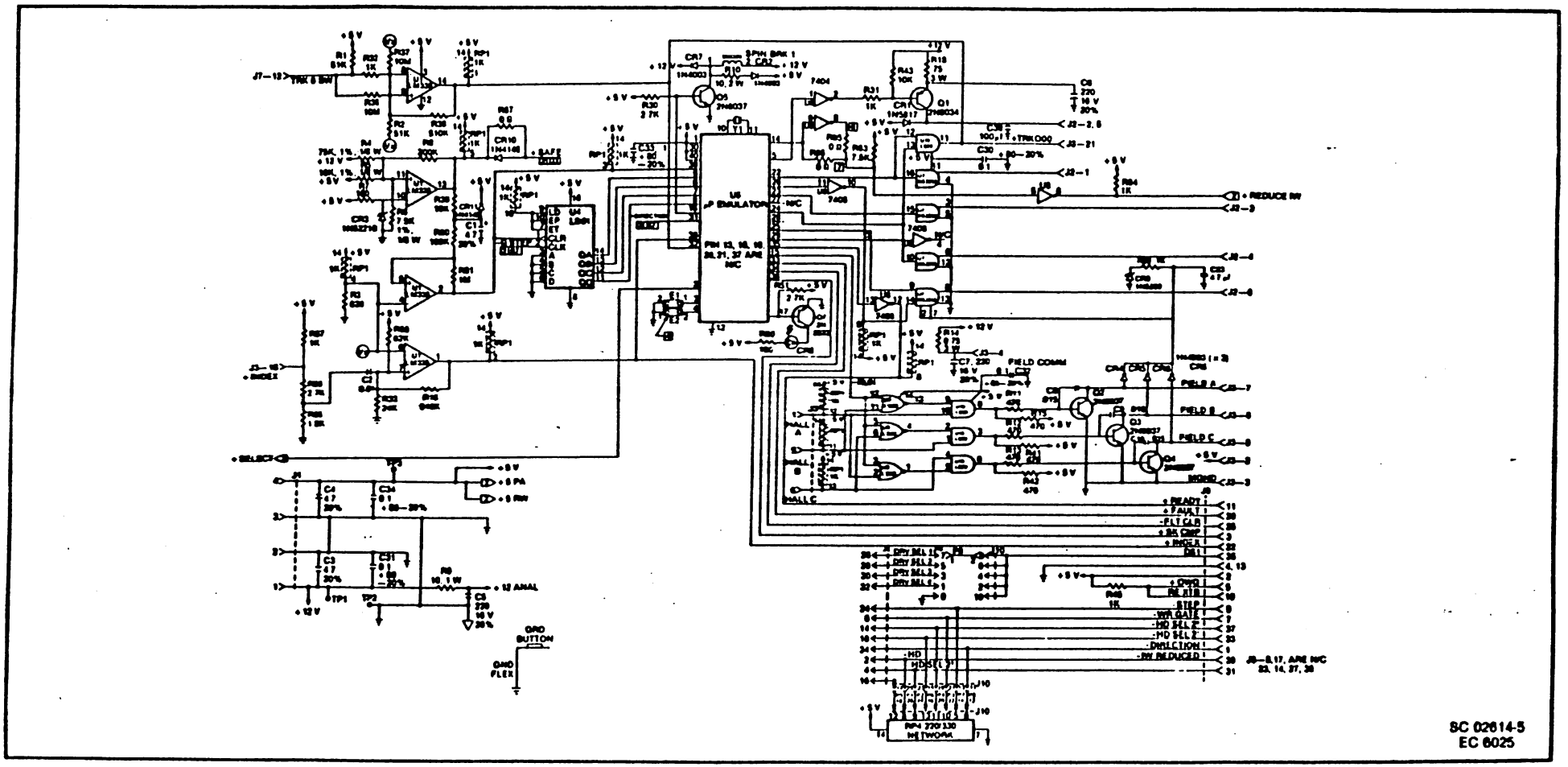
SECTION XIV
SCHEMATIC DIAGRAMS

The following schematic diagrams are furnished to aid in malfunction analysis.



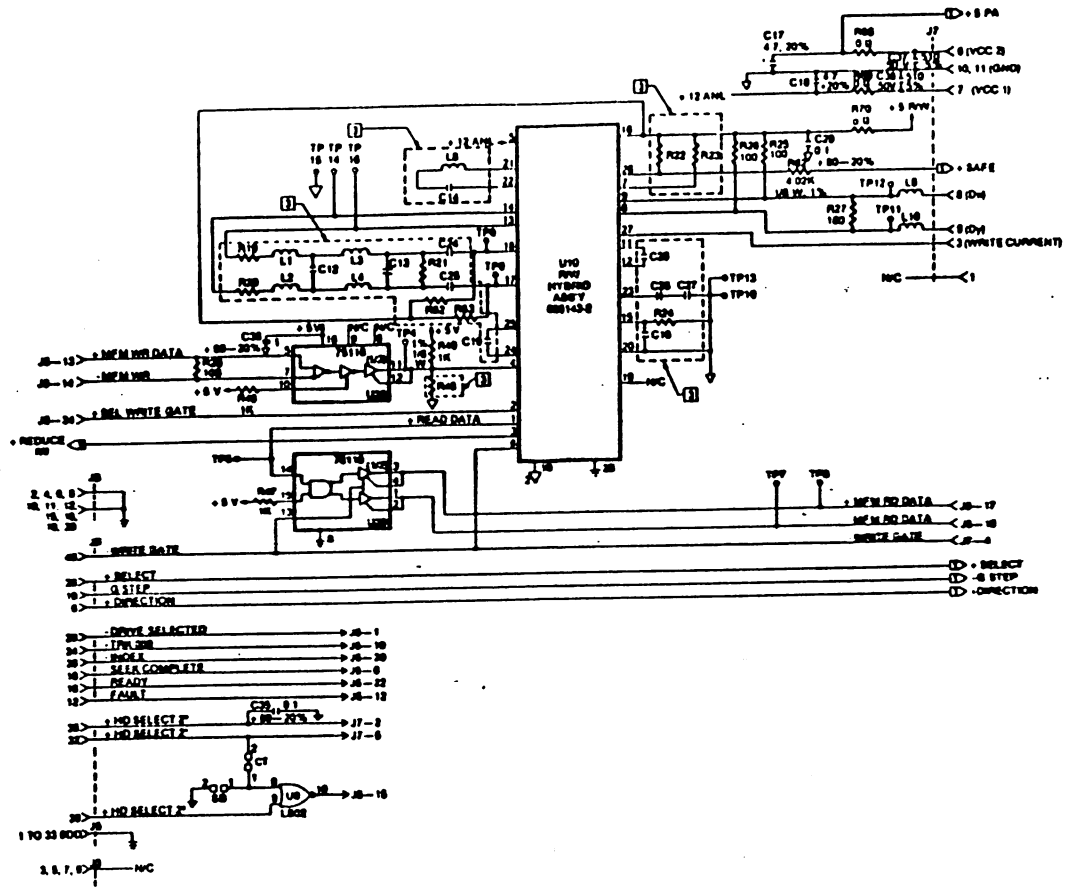
SC 02614-5
EC 6025

NOTES: (UNLESS OTHERWISE NOTED)

1. ALL CAPACITORS ARE IN MICROFARADS, 50 V, 10%
2. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
3. COMPONENTS NOT USED WHEN R/W ASM 62B143-2 INSTALLED
4. ⊠ INDICATES SHORTING PLUG INSTALLED. SHORTING PLUGS, AT E1 AND E2 ARE FOR TEST USE ONLY
5. ▷ DENOTES OFF SHEET CONNECTION
6. R66 USED WHEN U18 IS PIGGYBACK ASM
7. R66 USED WHEN U18 IS LSI DEVICE

LAST USED				NOT USED
CAP	C39	INDUCTOR	L10	CONN J8
IC	U39	XSTR	Q7	IC U2,3,8,11,12,13,14, 15,16,17,18
RES	R78	TEST POINTS	TP10	
CONN	J10	RES PACK	RP4	RES PACK RP2 RP3
DIODE	CR11	CONN (PLUG)	P8	LS L6,L7

FIGURE 14-1. CONTROL PCB SCHEMATIC (1 of 2)



SC 02614-5
EC 6025

FIGURE 14-1. CONTROL PCB SCHEMATIC (2 of 2)

NOTES: (UNLESS OTHERWISE NOTED)

1. ALL CAPACITORS ARE IN MICROFARADS, 50 V, 10%.
2. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
3. COMPONENTS NOT USED WHEN R/W ASM 888143-8 INSTALLED.
4. ⋘⋙ INDICATES SHORTING PLUG INSTALLED. SHORTING PLUGS, AT E1 AND E2, ARE FOR TEST USE ONLY.
5. ▷ DENOTES OFF SHEET CONNECTION.
6. R66 USED WHEN U10 IS PIGGYBACK ASM.
7. R66 USED WHEN U10 IS LSI DEVICE.

LAST USED				NOT USED
CAP	C39	INDUCTOR	L10	CONN J9
IC	U20	XSTR	Q7	IC U2,3,8,11,12,13,14, 15,16,17,18
RES	R78	TEST POINTS	TP16	
CONN	J10	RES PACK	RP4	RES PACK RP2,RP3
DIODE	CR11	CONN (PLUG)	P9	L8,L9,L7