READ/WRITE LSI 51250

1.0 DESCRIPTION

The Shugart 51250 is a 28 pin monolithic integrated circuit intended for use as a general purpose read/write function in high density Shugart disk drives. This I.C., when combined with a suitable PreAmplifier, incorporates all the control and circuit functions necessary to write data on a disk and read it back. The IC's data output is a standard TTL signal.

1.1 FEATURES

- o Operation with single 5 V supply.
- o Read/Write control switch.
- o Write current source whose output current is externally selectable.
- o Delta Write current control for increasing write current on ~~inside~~ OUTSIDE tracks.
- o High Speed Write Data divide-by-two circuit.
- o Differential Dx, Dy write current switch whose output current is externally set.
- o Two stage AGC'd Read Amplifier whose maximum gain is 47 db with 20 db of AGC range.
- o Active differentiator.
- o Threshold and zero-crossing detectors.
- o Delayed data sample one-shot.
- o High speed data sample "D" flip-flop.
- o Dual edge triggered data detection one-shot.
- o T^2L output stage that can be enabled or disabled by a separate data enable input signal. The output stage is automatically disabled when the circuit is in write mode.

2.0 DEVICE APPLICATION AND USAGE

All disk drive systems require some sort of read-write circuitry. In the past, this function was accomplished by a relatively large number of discrete and integrated components that use a lot of space and dissipate a lot of power. With the Shugart 51250 Integrated circuit, this function can now be accomplished with one I.C. and less than .5 watts dissipation, plus added features that are not usually seen in read/write circuitry, such as AGC.

2.1 The external components required for this circuit are as follows:

1. Compensation capacitor
2. Resistor for Dx, Dy current set
3. Resistor for Write Current set
4. Delayed data sample one-shot timing capacitor
5. Dual edge triggered one-shot timing capacitor
6. AGC time constant capacitor
7. AGC time constant resistor
8. Suitable Pre-Amplifier
9. Differentiator capacitor
10. Low-pass filter

3.0 FUNCTIONAL DESCRIPTION

3.1 Read Mode Operation (Figure 1)

Differential read data enters the circuit as a voltage across the resistor network connected to pins 8, 9. These resistors serve four functions. In Read mode, they act as part of the gain determining element for the Pre-Amp. For the Read Write I.C., they serve as pull-up biasing resistors for the first gain stage. The other two functions will be covered in Section 3.2. In Read mode, pin 6 is high and all the circuitry concerned with writing data is powered down with the exception of the write data flip-flops. These flip-flops are left on and cleared during read in preparation for the next write cycle. This is done so that Write Current, through the head, starts in the same phase each time a write sequence begins. The first stage amplifier provides an AGC'd gain of between 5 and 25 db. The signal exits the circuit as a constant amplitude differential signal on pins 13, 14. The signal is then sent on to a differential low-pass filter.

3.0 FUNCTIONAL DESCRIPTION

3.1 Read Mode Operation (cont)

External Low-Pass Filter Requirements

The Differential Low Pass filter bandwidth needs to include the 3/2 harmonic of the highest flux reversal pattern recorded. Spectrum analysis reveals the presence of this harmonic in any pattern where the read signal returns to the baseline. This bandwidth will permit minimum amplitude distortion as the 3/2 harmonic is essential to accurate peak timing. Also, the filter needs to have constant time delay characteristics within the passband for the same reason. A Bessel filter could be successfully used in this position.

After the Low Pass filter, the signal is then sent back into the I.C. via pins 17, 18 to a constant gain 22 db amplifier. After the signal gets amplified, it goes to a peak detector and the differentiator input. The components connected to pin 15 are used for filtering and to establish the AGC attack and decay time constants. The AGC signal reference level is established inside the die. This level is a fractional portion of the power supply voltage. The output of the AGC amplifier is connected back to the gain control circuitry of the 1st stage where the loop is closed. The differential signal out of the 2nd. stage of gain is sent on to the next stage where it gets differentiated. The components connected to pins 21, 22 make up the differentiation network.

Differentiator Network Requirements

This external network can be a single capacitor or a network combination of resistance, capacitance and inductance depending on the application requirements. Experience has shown that a noise advantage can be gained by using a series combination of R, C and L where the upper resonance slope is used to roll-off out of band, high end noise. The Q can be best determined experimentally.

After the differentiator, the signal passes on to threshold detectors and a zero crossing detector (see Figure 3 for details). The outputs of these circuits are digital signals and go to the "D" input of a flip-flop and an exclusive-or gate.

The exclusive-or gate is used to produce a pulse whose width is proportional to the difference between the zero crossings and thresholds of the differentiated data signal. (Data thresholds can be determined from Fig. 4.) The leading edge of the pulse is delayed by the "Data Sample one-shot". The combination of the delayed leading edge zero crossing, threshold detectors and "D" flip-flop make up a sampling circuit that samples the threshold detected differentiated data at an interval determined by the value of the timing capacitor connected to pin 23.

Differentiator Network Requirements (cont)

The outputs of the "D" flip-flop go to a one-shot that responds to the positive edges of either the Q or $\overline{Q}$ outputs. External capacitance connected to pins 24, 25 set the pulse width of this one-shot. (See Figure 5). The output of the one-shot drives the T^2L output circuit. Pin 3 is a TTL compatible input used to disable pin one, TTL read data out.

3.2 Write Mode Operation

Write mode operation is defined as a TTL low on pin 6. This condition causes the following changes inside the read write circuit to take place:

A. All amplifier stages are powered down.

B. Read data output is disabled.

C. Write current source is turned on.

D. Dx, Dy current source is turned on.

E. Write data latch reset is released.

The resistor or current source connected to pin 26 sets the write current out of pin 27. Pin 27 current will be approximately ten times the program current at pin 26. This current goes to the Pre-Amp wherein it gets steered to which-ever head is being used for writing data to the disk. Pin 4 is a TTL input and is used to modulate write current by $\pm$ 5% for different write current requirements, depending on whether the head is on an inside or outside track.

The differential Dx, Dy write current out pins 8, 9 are set by the resistor or current source on pin 7. This current should also be set to 1/10 of the intended Dx, Dy output current. In write mode, the resistor network connected to Dx, Dy, serve as load resistors for the current into pins 8, 9 and also act as biasing resistors for the Pre-Amp input stage.

Write data enters the I.C. as a TTL signal into pin 5. This signal is then divided by two corresponding to the positive edges of the incoming data stream. The divided data signal is then used to control the Dx, Dy current switch that sends the data to the head as a differential signal. This signal is then steered inside the Pre-Amp to the appropriate write head.

4.0 51250 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings:

Supply Voltage pins 1, 16	7 V
Power Dissipation	640 mW
Operating Temperature Range	0° to $70^\circ C$
Storage Temperature Range	-50° to $150^\circ C$
Pin Temperature (soldering for 10 sec)	$300^\circ C$

$T_A = 25^\circ C$, $V_{CC} = 5.0$ V (unless otherwise specified)

Note: All currents are given in absolute values unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage Range (Pins 1, 16)	Note 1	5.75 (4.75 ?)	5.0	5.25	V
V_{CC} Supply Current (Pins 1, 16)	Read Mode	24.3	27	29.7	mA
	Write Mode	58.5	65	71.5	mA
Write Current Source Output (Pin 27)	V_6 Low Note 3	0	30	100	mA
Allowable Operating Voltage Range (Pin 27)	Note 1, V_6 Low	0.75		V_{CC}	V

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Write Current Set Input (Pin 26)	Note 3 Sink		3.75	15.00	mA
V_{26}			.644$\pm$1% of V_{CC}		V
I_{27} out / I_{26} in	V_4 High	7.50	7.65	7.80	
	V_4 Low	6.50	6.65	6.80	
Write Control (Pin 4)					
Input High Voltage		.360$\times V_{CC}$		V_{CC}	V
Input Low Voltage		0		.340$\times V_{CC}$	V
Input High Current				50	uA
Input Low Current			-160	-500	uA
Input Clamp Diode	@ 10 uA			-1.5	V
-Write Gate (Pin 6)					
Input High Voltage		.360 V_{CC}		V_{CC}	V
Input Low Voltage		0		.340 V_{CC}	V
Input High Current				50	uA
Input Low Current			-160	-500	uA
Input Clamp Diode				-1.5	V
High	Read mode				
Low	Write mode, Output disabled				
Write to Read Recovery Time	Note 3		30	-	us

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Write Date Input (Pin 5)					
Input High Voltage		.360 V_{CC}		V_{CC}	V
Input Low Voltage		0		.34 V_{CC}	V
Input High Current				50	uA
Input Low Current			-160	-500	uA
Input Clamp Diode	@ 10 uA			-1.5	V
Input freq.	V_6 Low, Symmetrical signal		5.0	50.0	MHz
Dx-Dy Current Set Input (Pin 7)	Note 3, V_6 Low		.350	1.5	mA
V_7	V_6 Low		.8$\pm$1% of V_{CC}		V
$I_{8,9} \div I_7$	V_6 Low	9.6	9.8	10.0	
Dx-Dy Current Source Outputs (Pins 8,9)	Note 3, V_6 Low		3.5	15	mA
Allowable Operating Voltage Range (Pins 8 or 9)	Note 1, V_6 Low	.6 V_{CC}		V_{CC}	V
I_8 or I_9 Off	V_6 Low	0.0		2.0	uA

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Frequency Differential (Pins 8 & 9)	V_6 Low		.5 of Pin 5		MHz
Dx, Dy Asymmetry	V_6 Low, Note 2		1.0	2.0	ns
Read Mode Input Capacitance (Pins 8,9)	V_6 High Between pins		1.5		pf
(Pin 8 or 9) to gnd.	V_6 High		2.0		pf
Input Resistance	V_6 High	20K	40K		ohms
Input Offset Current			.4		uA
Input Bias Current			5	10	uA
Compensation Capacitance (Pins 11, 12)			18		pf
Output Resistance (Pins 13, 14)			20		Ω
Band width (1st stage)	-3 db point		45		MHz
Gain (1st stage)		5		25	db
AGC Range (1st stage)	V_6 High		20		db
Input Level	V_6 High	10	35	100	MVPP Diff.
Output Voltage Swing (Pins 13, 14)	RL = 600		175		MVPP Diff.

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
AGC (Pin 15)	V_6 High				
V_{15} Operating Range	Note 1	1.4		3.0	V
External components (Pin 15)	See fig. 1.				
AGC Attack Time	V_6 High, Note 3		1		us
AGC Decay Time	V_6 High, Note 3		250		us
2nd. Stage Input Capacitance (Pins 17,18)	V_6 High Between Pins		1.5		pf
(Pin 17 or 18) to gnd.	V_6 High		2.0		pf
Input Resistance	V_6 High	20K	40K		ohms
Input Offset Current			.4		uA
Input Bias Current			5	10	uA
Band Width (2nd. stage)	-3 db point		45		MHz
Gain (2nd. stage)		23	24	25	db
Input Level (Pins 17,18)			75		MVPP Diff.

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differentiator	V_6 High				
Capacitance Value (Pin 21,22)	Note 4		(See Fig. 4)		pf
One-Shot (Pin 23)	See Fig. 6				
High level Voltage	V_6 High, Note 1	.55 V_{CC}	.56 V_{CC}	.57 V_{CC}	V
"D" flip-flop clock level	Note 1	.402 V_{CC}	.412 V_{CC}	.422 V_{CC}	V
End of ramp Voltage level	Note 1	.280 V_{CC}	.290 V_{CC}	.300 V_{CC}	V
I Discharge		340	350	360	uA
I Charge		3.5	4	4.5	mA
Output Pulse Width (Pins 24, 25)	See fig. 5				
Peak-Peak Swing (Pin 24 or 25)		.195 V_{CC}	.196 V_{CC}	.197 V_{CC}	V
Peak to Threshold (ΔV) (Pin 24 or 25)		.159 V_{CC}	.160 V_{CC}	.161 V_{CC}	V

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Discharge Current (Pins 24 or 25)		290	300	310	uA
-Data Enable Input (Pin 3)					
Input High Voltage		2.0			V
Input Low Voltage				.8	V
Input High Current				50	uA
Input Low Current			-160	-500	uA
Input Clamp Diode	@ 10 uA			-1.5	V
High	Output disabled				
Low	Output Inabled				
Read Data Output (Pin 3)	V_6 High				
Output High Voltage	Standard TTL	2.4	3.2		V
Output Low Voltage	Output load		.25	0.4	V
Output High Current			0.80	5.0	mA
Output Low Current			1.6	16.0	mA

NOTES:

1. These voltage values are with respect to the network ground terminal.

2. This measurement is made by triggering the scope from pin 5 signal, then observing pins 8 and 9 differentially. The output should look like a "double triggered" signal of half frequency of pin 5, pins 8, 9 traces should cross in the center of the swing of < 4.0 ns.

3. This value is affected by the size of the external components used.

4. The value of capacitance is dependent on the frequency of the data being used and the percent of peak threshold desired. (See Fig. 4)

51250 BLOCK DIAGRAM

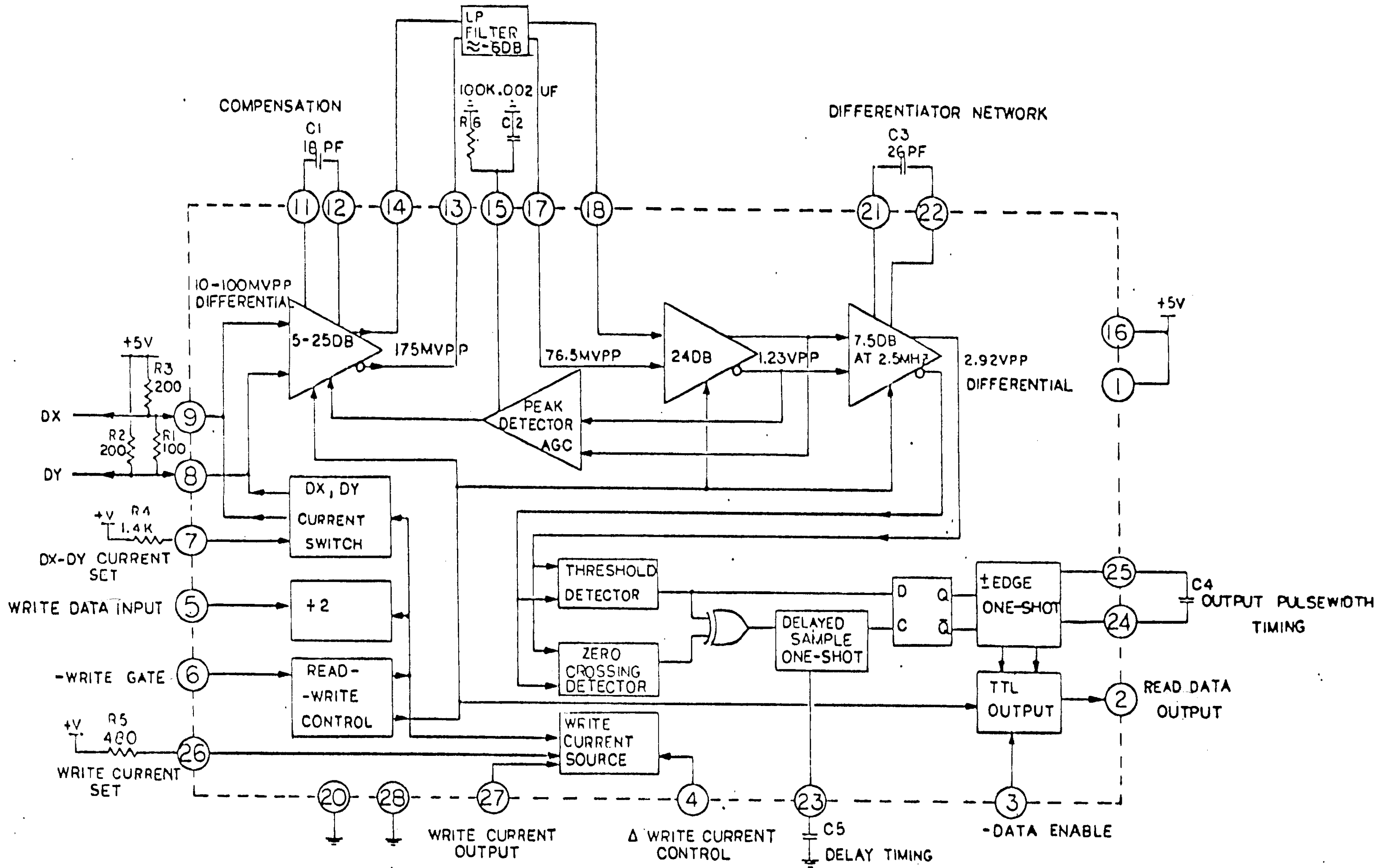


FIGURE 1

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE 51250 BLOCK DIAGRAM
CASE DEPTH	LINEAR ±.XX ±.XXX			DWG J. Regnier 6/29/77 RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR ±			CHK
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			APR SHEET OF
				C SCALE DOC CODE PART NO

PART NO.

TYPICAL PARTIAL SYSTEM

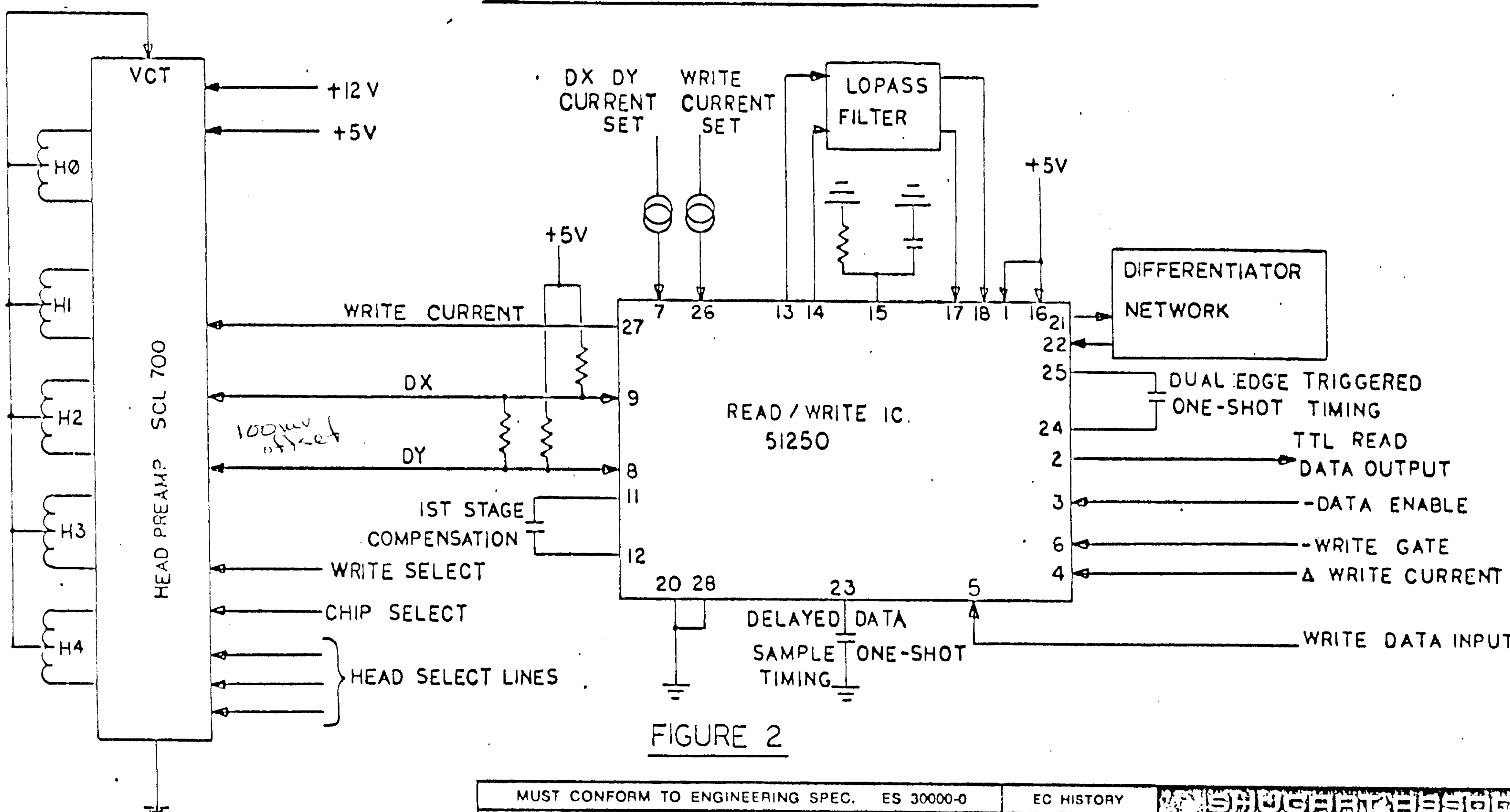


FIGURE 2

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0				EC HISTORY	
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED		DATE	NO.
		LINEAR	±.XX		
CASE DEPTH			±.XXX		
HARDNESS		ANGULAR±			
SURFACE TREATMENT	ES	CORNERS EDGES BROKEN	OUTSIDE MAX		
			INSIDE MAX		

SHUGART ASSOCIATES

TITLE PARTIAL SYSTEM BLOCK DIAGRAM			
DWG	G. Regnier	6/28/83	RELEASED FOR ASSEMBLY
CHK			
APR			SHEET OF
B	SCALE	DOC CODE	PART NO REV

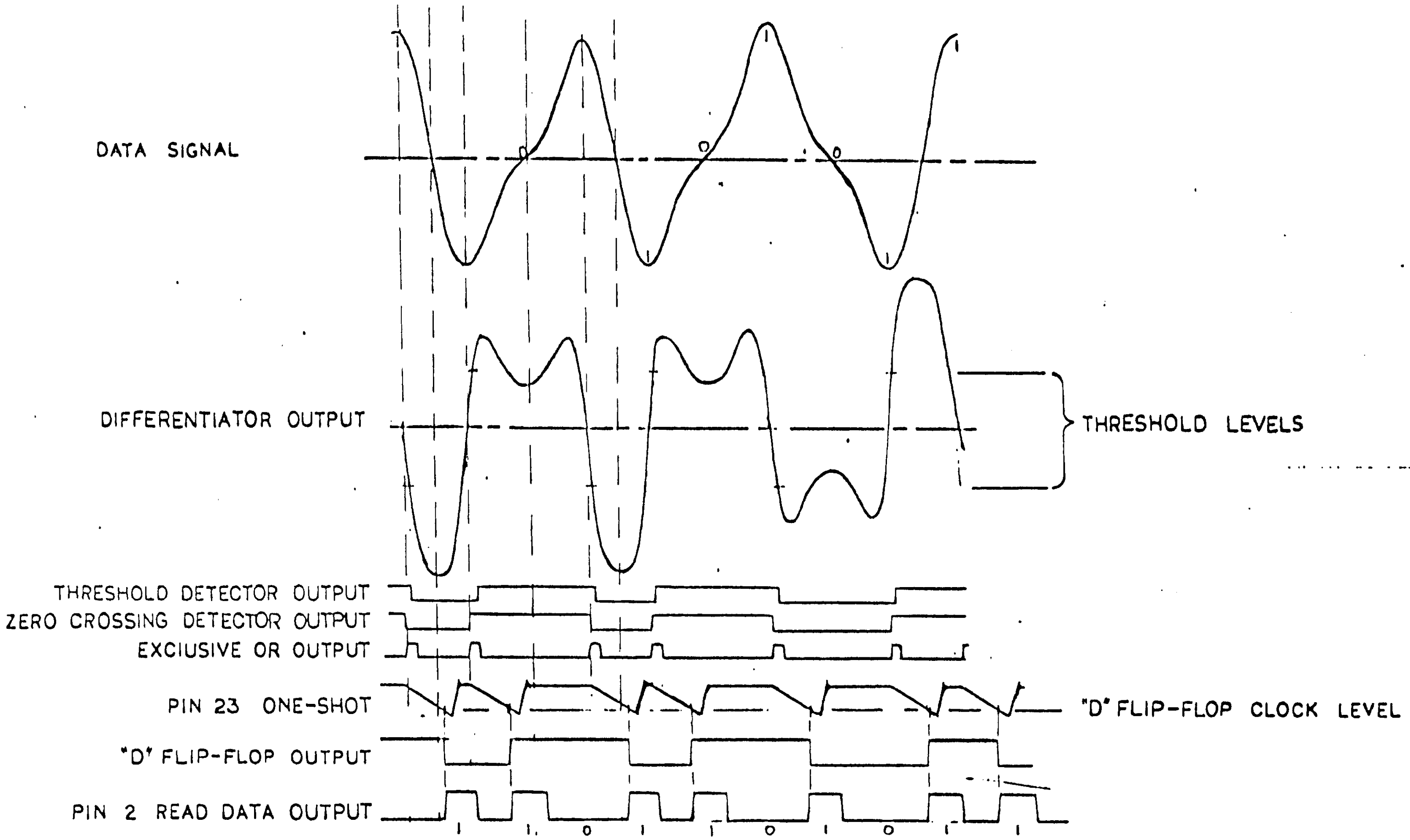


FIGURE 3

PART NO.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE DATA DETECTION WAVEFORMS
	LINEAR ±.XX			DWG J. Regnier 6/29/73 RELEASED FOR ASSEMBLY
CASE DEPTH	±.XXX			CHK
HARDNESS	ANGULAR ±			APR SHEET OF
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			B SCALE DOC CODE PART NO REV

51250

TITLE DIFFERENTIATOR/COMPARATOR THRESHOLD

SHEET OF

THRESHOLD VS FC

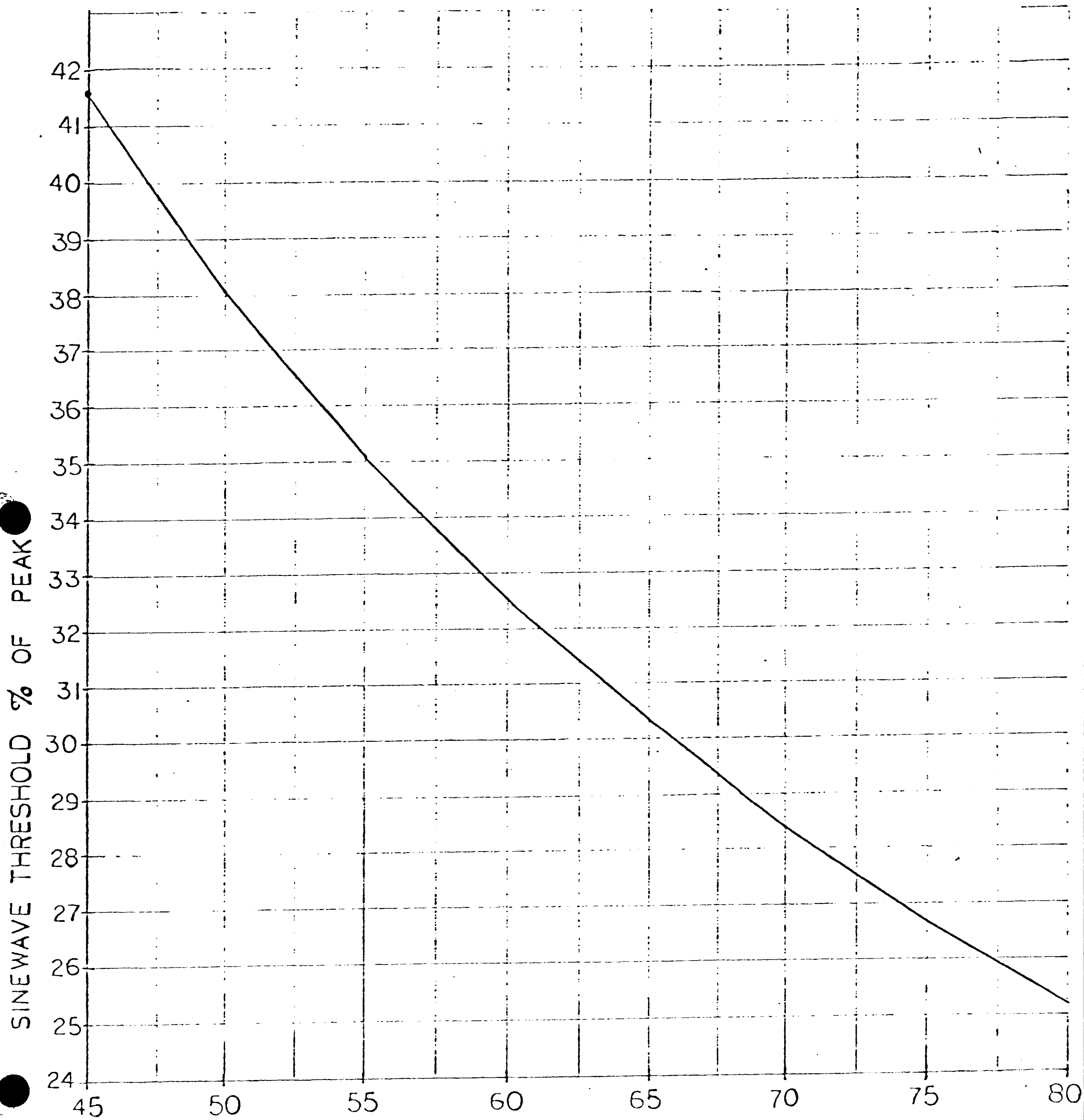
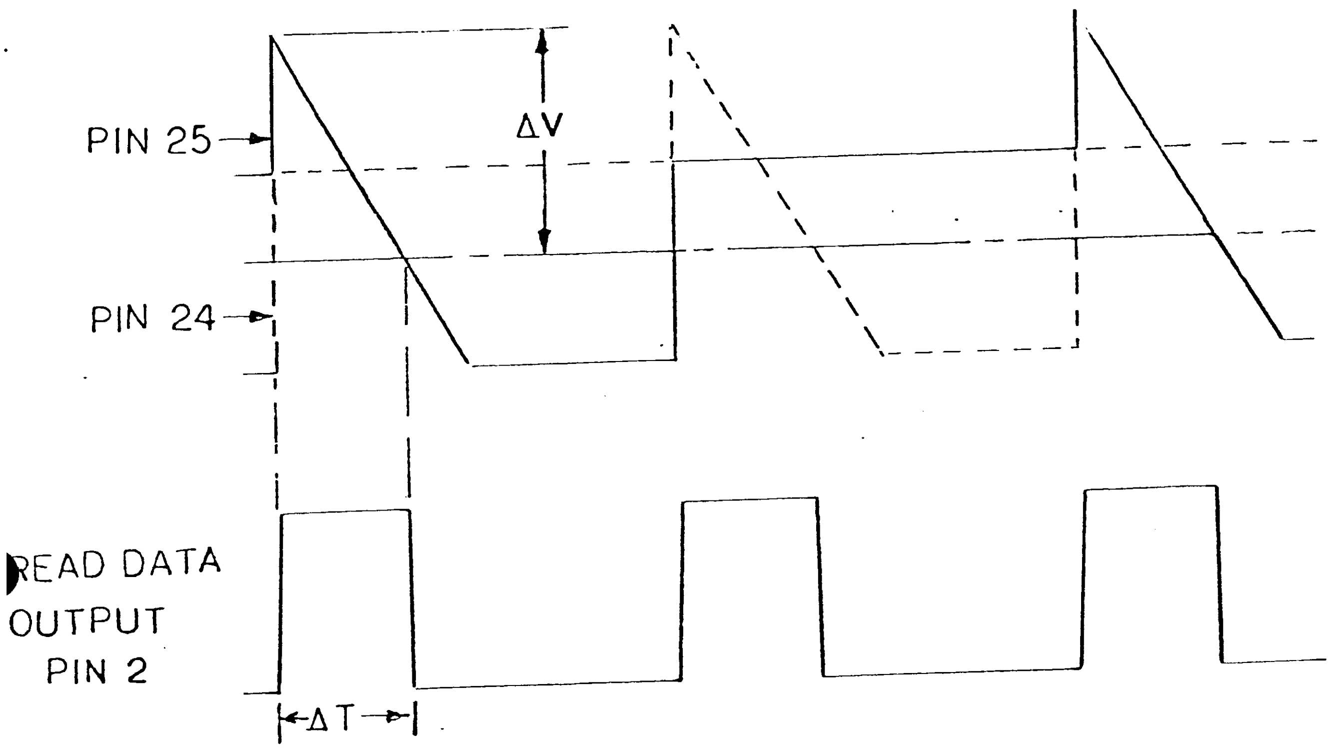


FIGURE 4

TITLE READ DATA PULSEWIDITH



$$\Delta T = C4 \frac{\Delta V}{I}$$

WHERE:

$\Delta V = 800MV$

$I = 300UA$

FIGURE 5

51250

SHEET OF

TITLE ONE-SHOT TIMING

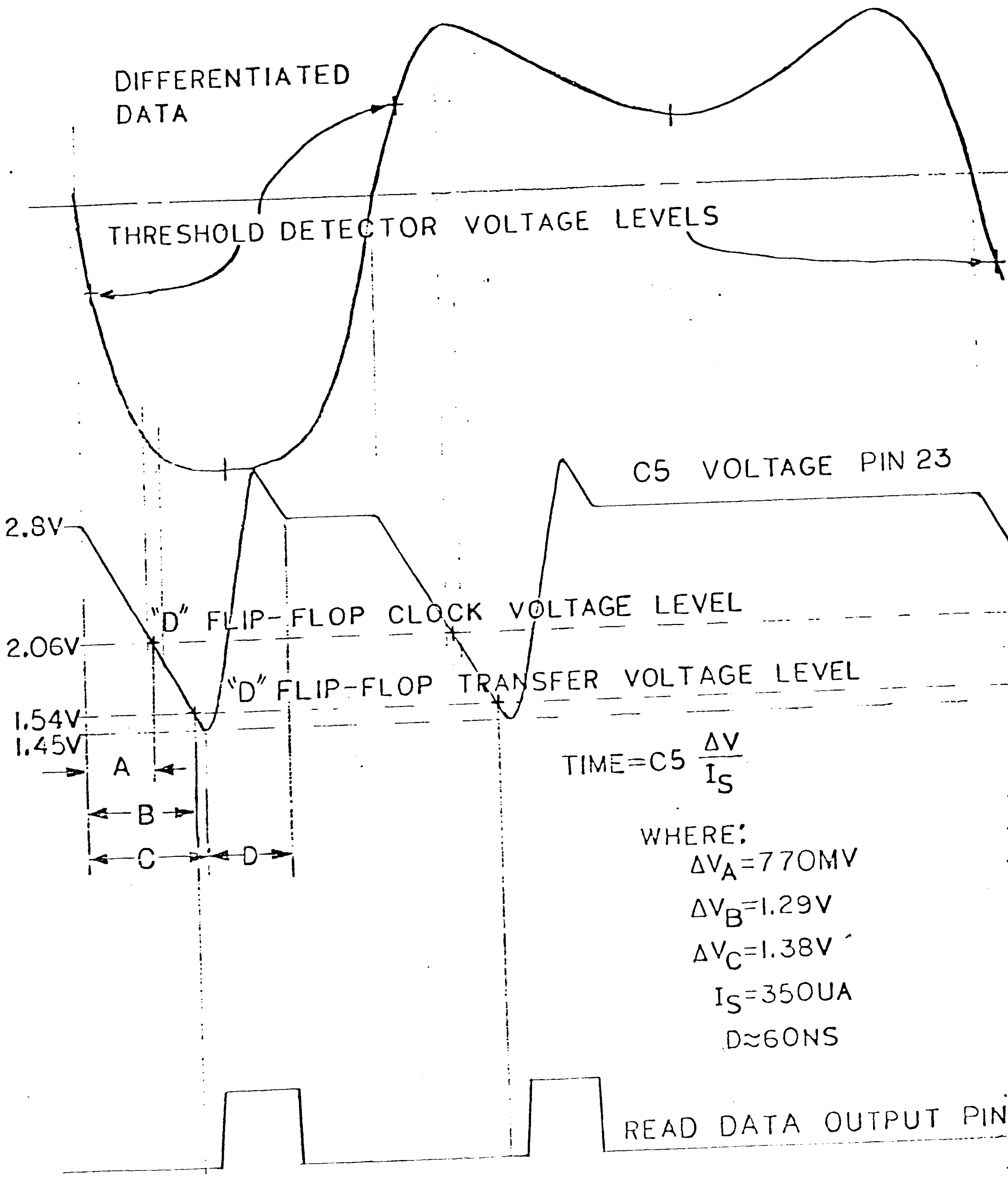
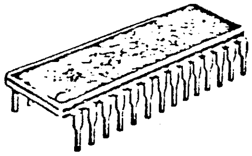


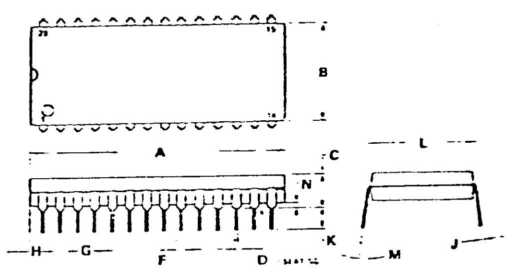
FIGURE 6

PACKAGE OUTLINE

PLASTIC

Case 710-02
28-Pin Plastic





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	35.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 710-02

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D) SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.