

- [54] **REAL-TIME SIMULATION OF POINT SYSTEM HAVING MULTIDIRECTIONAL POINTS AS VIEWED BY A MOVING OBSERVER**
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- [51] Int. Cl.² **G09B 9/08; B64G 7/00; H04N 7/18**
- [58] Field of Search **35/10.2, 12 K, 12 N, 35/12 P; 46/1 B; 178/DIG. 22, DIG. 35**

[56] **References Cited**

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Primary Examiner—R. Stephen Dildine, Jr.
 Attorney, Agent, or Firm—Paul Hentzel; James C. Kesterson

[57] **ABSTRACT**
 A night visual aircraft system receives flight data from

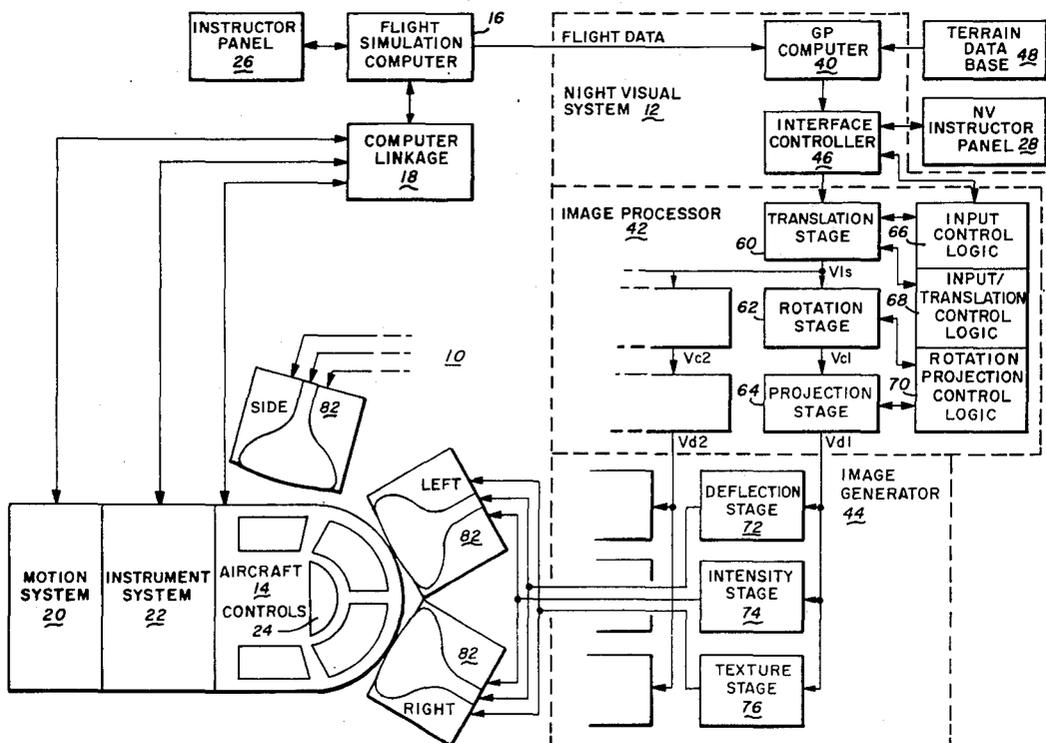
an aircraft simulator, and ground light data from the gaming area data base. A computer within the night visual system organizes this image data by frame in a buffer memory according to a particular format of addresses, sequences, and bit places. The following types of image data are uniquely positioned in the format:

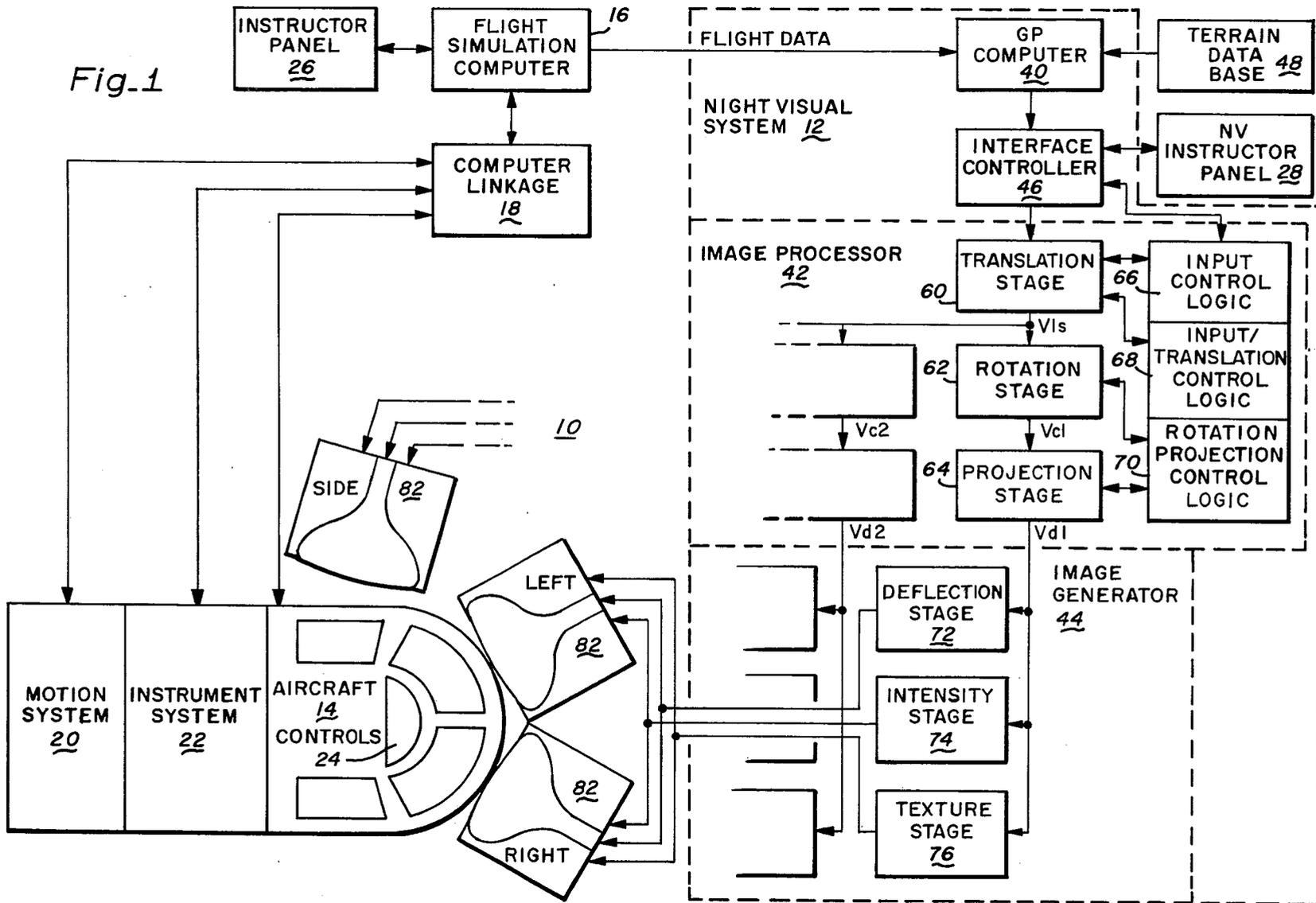
- A position vector (V_p), defining the changing position of the aircraft with respect to the terrain data origin.
- Rotational matrix data defining the changing attitude of the aircraft with respect to the axes of the terrain coordinate system.
- Light source position data defining the position of terrain lights with respect to the origin of the terrain data.
- CIF data, defining the direction, color, intensity, option code, and defocus (size) of individual lights.

An image processor receives the formatted image data and translates and rotates to correspond to the perspective of the simulated pilot view, maintaining the directional aspect of the lights. The data is then projected into two-dimension display vectors.

An image generator receives the display vectors and other image data to provide analog inputs to a CRT device mounted as a window display in the simulated aircraft.

21 Claims, 8 Drawing Figures





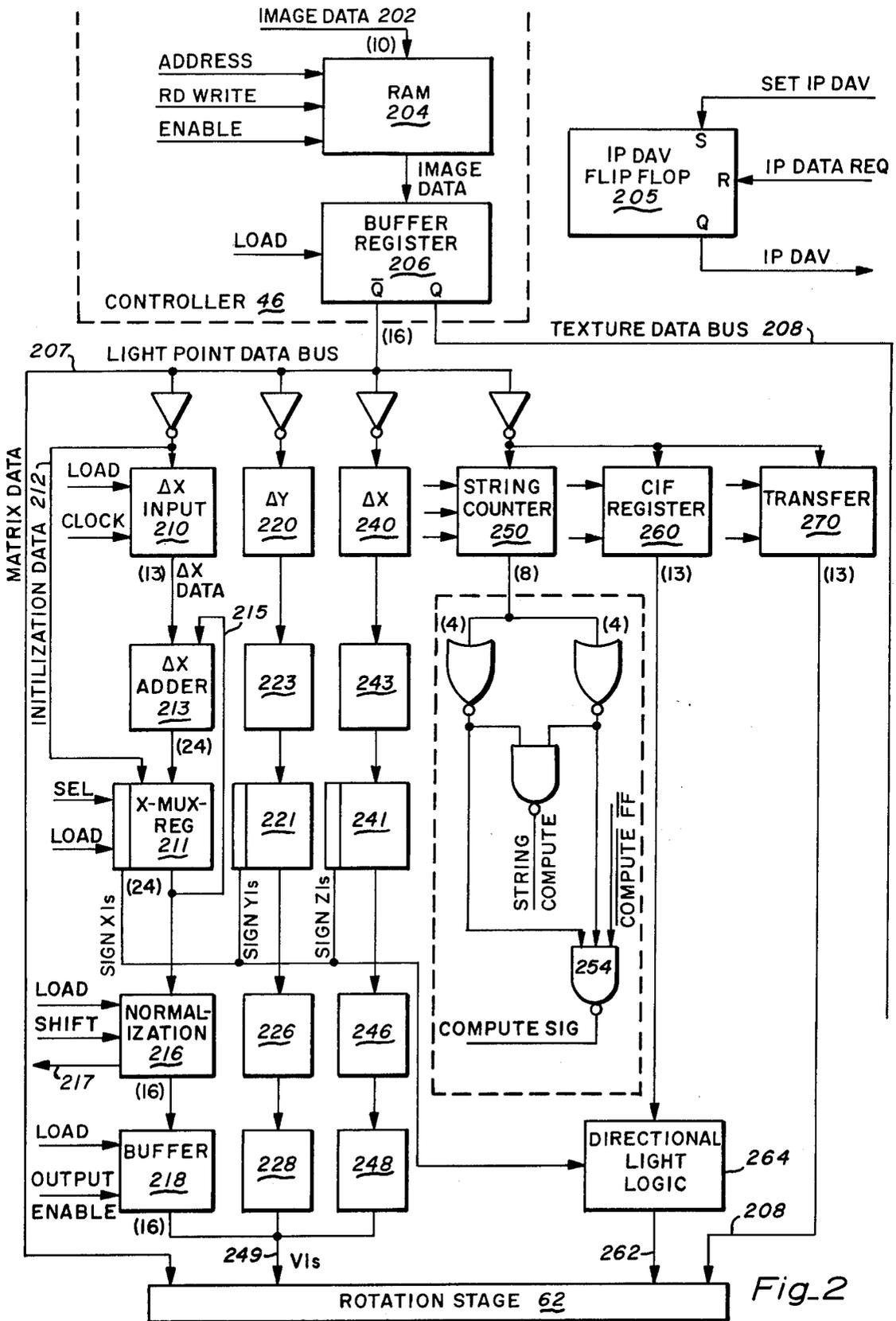


Fig-2

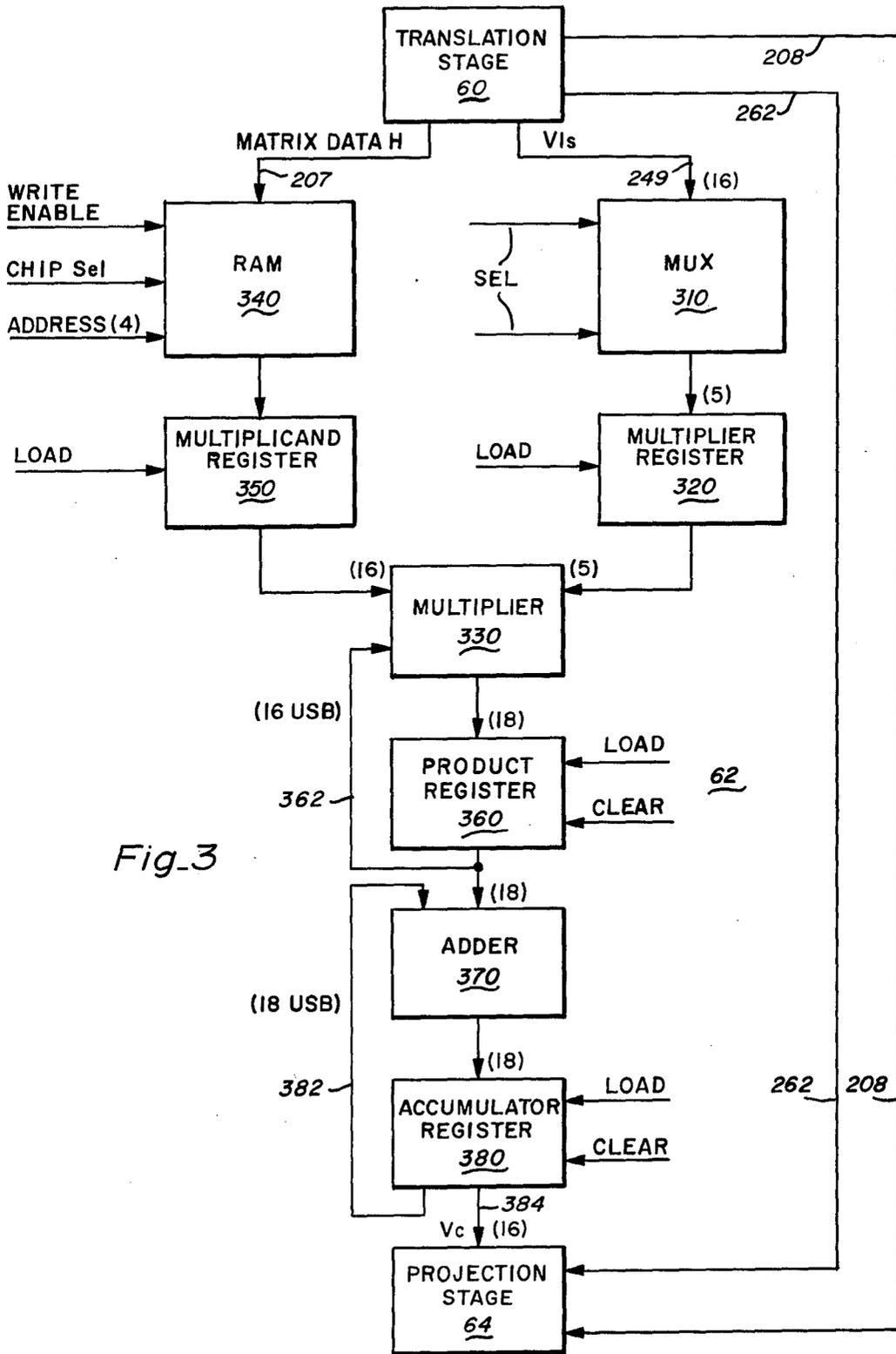


Fig. 3

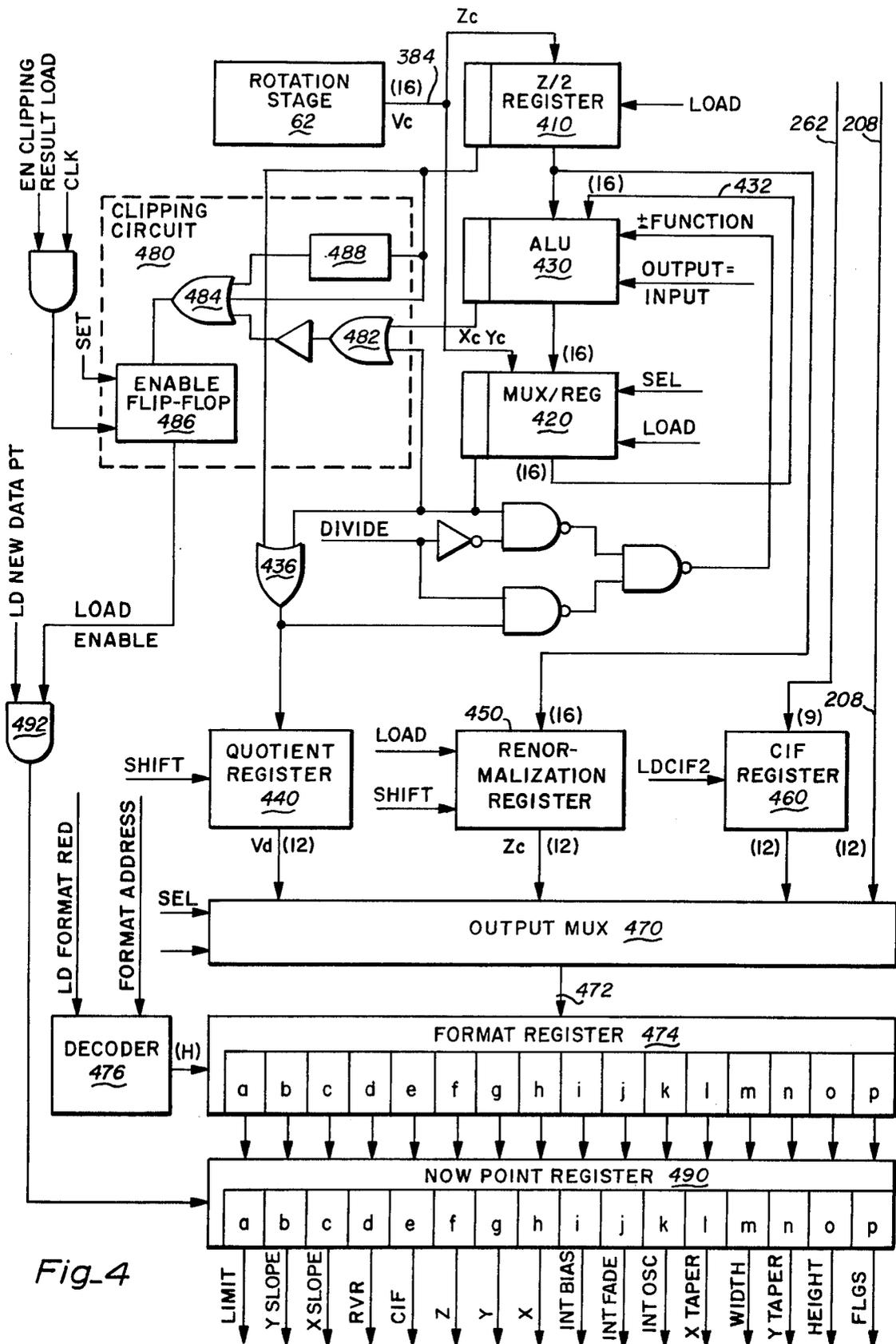


Fig-4

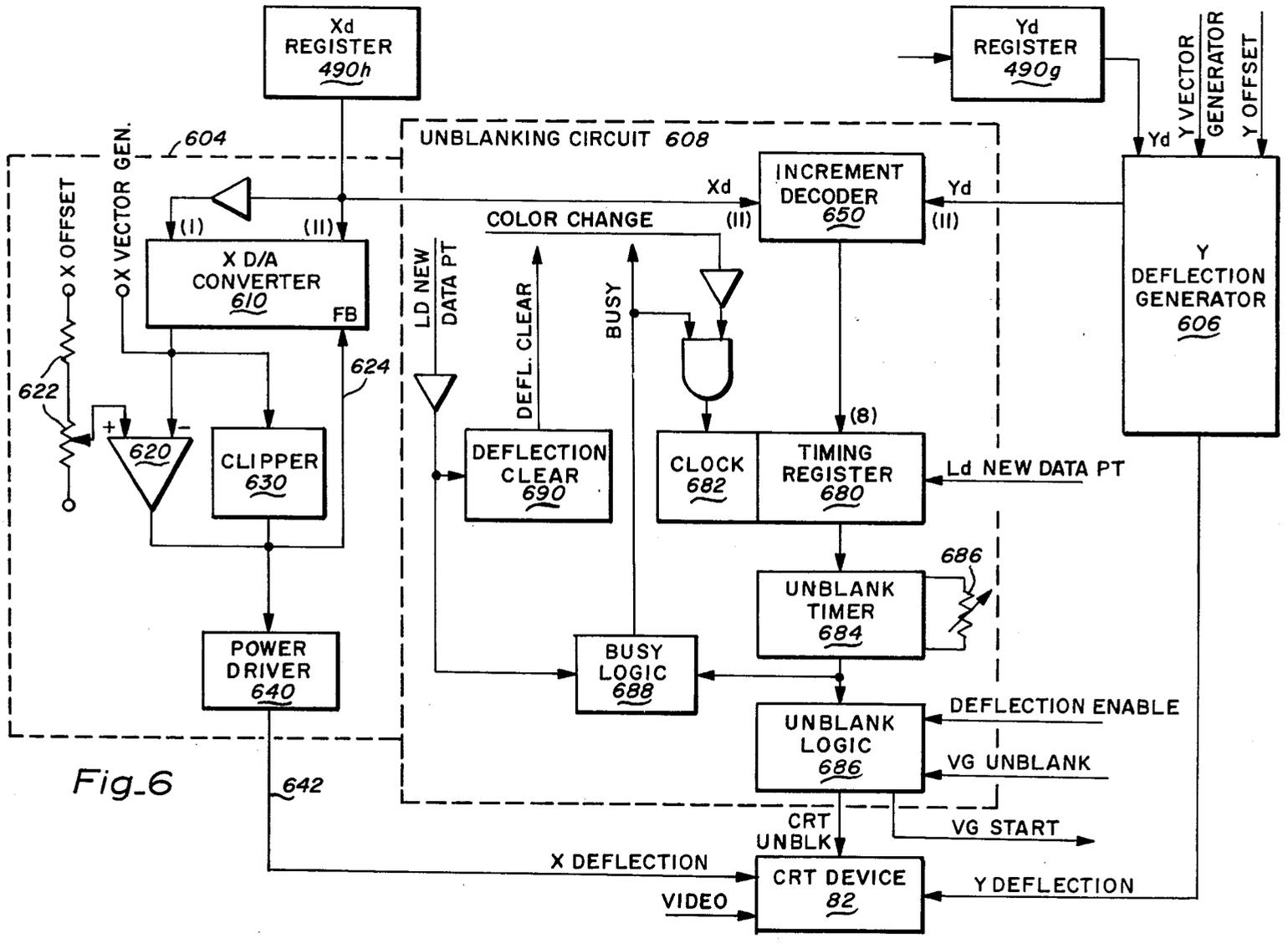


Fig. 6

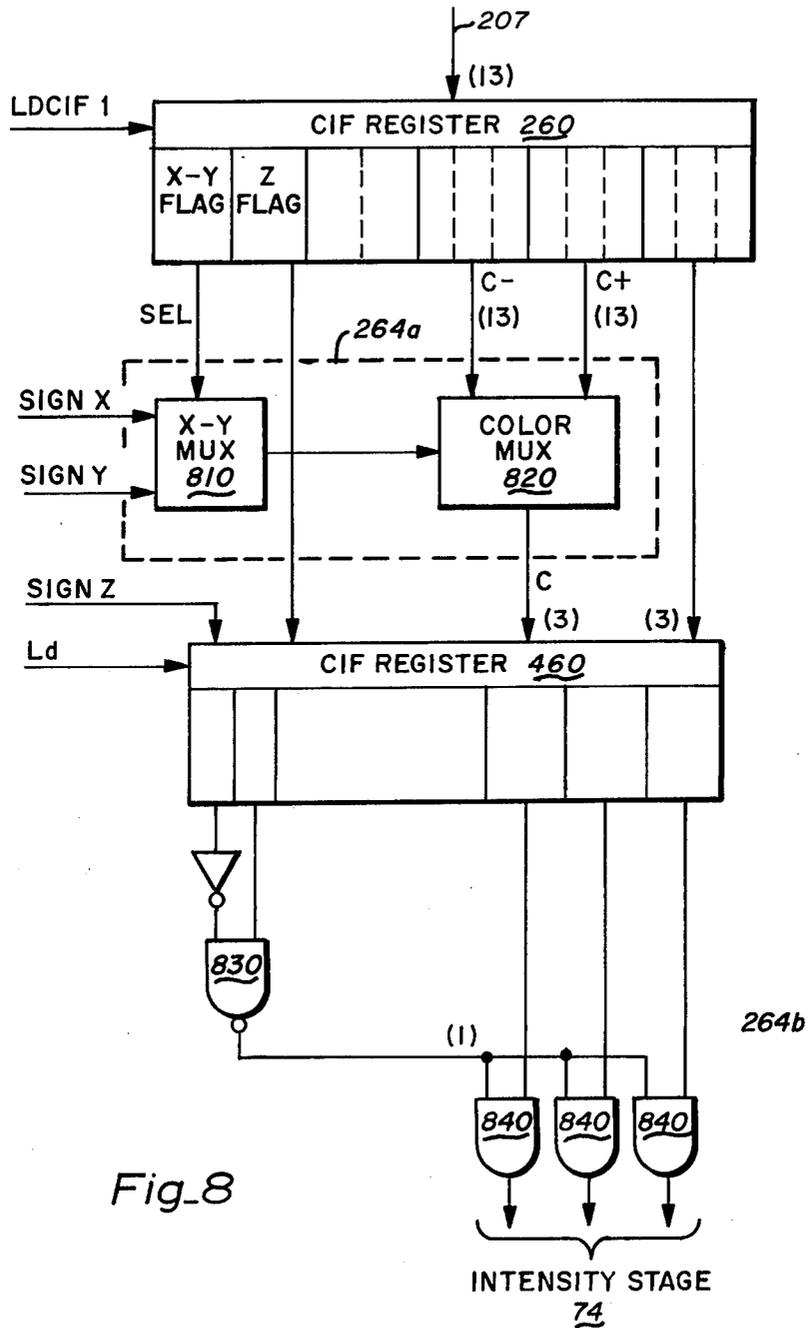


Fig. 8

REAL-TIME SIMULATION OF POINT SYSTEM HAVING MULTIDIRECTIONAL POINTS AS VIEWED BY A MOVING OBSERVER

BACKGROUND OF THE INVENTION

This invention relates to real-time digital image generation of a gaming area as viewed from a maneuverable viewpoint, and more particularly to such image generation of directional point structures displayed as points of light.

Heretofore, digital image generation (DIG) has been used in architecture and mathematics to display three-dimensional objects. The viewer could maneuver the display to obtain different perspective views, helpful in building the objects or understanding the relationship between parts thereof. However, these systems were basically nondynamic and lacked the realism of real-time maneuvering.

Directional points in these systems have been processed by software. They were treated as separate light for each distinguishable orientation and color. Airport centerline lights are visible in red or green depending on the direction of the approaching aircraft. These lights were software processed as two lights occupying the same position: one red and black light, and one black and green light. For a string of similarly colored lights, the software would compute the relative position of the pilot to the light string and from this divide the light string into two separate strings, of different color, if the relative position required that two colors be presented.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to:

provide a real-time, realistic DIG display system which processes directional point data rapidly and efficiently;

provide DIG display system with directional point capability which is simpler, less expensive, more compact and more reliable;

provide a DIG display system employing a data base including directional points and hardware for determining the visible aspects of the directional points in the perspective of the viewer;

provide a DIG display system which may be expanded to provide a plurality of window displays having related fields of vision;

provide a DIG display system in which the image data is formatted to colors (including black) for each distinguishable direction;

provide a highly realistic night visual aircraft simulation system which simulates directional lights prominent during night flying conditions;

provide a DIG system in which all of the object data are processed each frame without preselection as a function of the orientation of the observer.

DESCRIPTION OF THE FIGURES

Further objects and advantages of the present invention, and the operation of the night visual system, will become apparent from the following detailed description taken in conjunction with the drawings, in which:

FIG. 1 is a block diagram of the night visual system and peripheral equipment showing data flow relationships;

FIG. 2 is a logic circuit of the translation stage wherein delta data (ΔX , ΔY , ΔZ) is translated into light source vectors (Vls);

FIG. 3 is a logic circuit of the rotation stage wherein the Vls is multiplied by a rotation matrix in response to the aircraft attitude to provide channel vectors (Vc);

FIG. 4 is a logic circuit of the projection stage wherein Xc and Yc are divided by Zc to project Vc into the X-Y plane to form deflection vector (Vd);

FIG. 5 is a logic circuit of the input logic control which activates the translation stage;

FIG. 6 is a logic circuit of the deflection stage which generates X and Y deflection voltages in response to Vd (Xd , Yd);

FIG. 7 is a pictorial view of a landing field showing the directional lights responsive to each axis; and

FIG. 8 is a detailed logic circuit for directional light logic shown in FIG. 2.

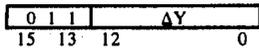
GENERAL DESCRIPTION OF NIGHT VISUAL FLIGHT SIMULATION SYSTEM 10

FIG. 1 shows a flight simulation system 10 with night visual capabilities provided by a night visual (NV) system 12. A simulated aircraft 14 is linked to flight simulation computer 16 and NV system 12 through computer linkage 18. Flight simulation computer 16 controls motion system 20 and instrument system 22 of aircraft 14 in response to the pilot's maneuvering action at aircraft controls 24. Additionally, instructors at instructor panel 26 and NV panel 28 may create useful training situations such as engine failure, disabled landing gear, etc. which affect the handling of aircraft 14. NV system 12 is formed by general purpose computer 40 such as Digital Equipment Corporation PDP 11/35, image processor 42, image generator 44, and interface controller 46. Interface controller 46 is provided to control image data flow from GP computer 40 to image processor 42 via a data buffer, to process instructor data from panel 28 to GP computer 40, and to process flight data from aircraft 14 to image processor 42.

GP computer 40 receives flight data, such as aircraft position, aircraft attitude (roll, pitch and yaw), etc. from computer 16. GP computer 40 additionally receives night-time earth data from data base 48 such as landing lights, light strings, environmental lights, beacons, etc., preferably including the intensity, color and size of each light source. Preferably, the aircraft position data is an aircraft position vector Vp extending from the simulated position of aircraft 14 to the origin of the earth coordinate system. In order to simplify conception and data organization, the origin is preferably located proximate the touchdown area of the runway and X axis of data base 48 is coincident to the runway centerline. An updated Vp is supplied each display frame by flight simulation computer 16 as the flight parameters of aircraft 14 change. GP computer 40 combines Vp and the position of certain key light sources (i.e. the first light in each string) from data base 48 for providing a series of initialization vectors Vi to image processor 42. The earth data also includes the relative position of other light sources (delta data) including the rest of the light string (string data). Translator stage 60 in image processor 42 combines the delta data with the appropriate Vi to provide a light source vector Vls for each remaining light source. Rotation stages 62 rotate each Vls by combining it with aircraft attitude data (a 3×3 rotation matrix). A different rotation is required for each channel or viewing axis

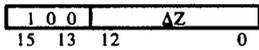
-continued
Similar to INX.

IYC (Increment Y and Compute)



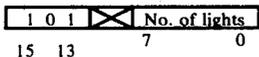
Similar to IXC.

INZ (Increment Z)



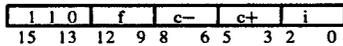
Similar to INX. An IZC can be provided with a larger code base. However, in a night visual airport application, vertically stacked lights (delta X = delta Y = 0) are unusual.

STG (String)



Defines the number of lights in a string of uniformly spaced lights of the same color and intrinsic intensity. The spacing between lights in a string is defined by the delta X, delta Y, and delta Z codes immediately following the STG code.

CIF (Color, Intensity Code, Flags)



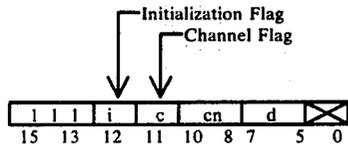
Defines the color (c) and intrinsic intensity (i) of the light source.

c = color codes, positive and negative relative position for bidirectional light sources which are disclosed in more detail in the Section titled "Preferred Embodiment of Directional Light".

i = intensity code

f = options control code

XFR (Transfer)



Code (111) transfers the next data word to the window or channel specified by cn (three bits) and the data register specified by the data address field, d (three bits). The word following a transfer code is an initialization data without any code bits.

cn = The window channel to which the data is being directed.

d = Destination of data transfer. The source is the data word immediately following the XFR.

i = Initialization Flag. A 1-bit in this bit position indicates a data transfer for initialization, as shown in the following table.

c = Channel flag. A 1-bit in this bit position indicates that the data transfer is channel-dependent, thus requiring channel select specification in cn.

TABLE OF XFR CODES*

XFR	i	c	cn	d		
15	13	12	11	10	8 7 5 4 0	
5	Initial Value					
	1	0	000			
X, 8 LSB						
	1	0	001			
X, 15 MSB + sign						
10	1	0	010			
Y, 8 LSB						
	1	0	011			
Y, 15 MSB + sign						
	1	0	100			
Z, 8 LSB						
	1	0	101			
Z, 15 MSB + sign						
15	Rotation matrix to designated channel, in order of: h(21), h(22), h(23) h(11), h(12), h(13) h(31), h(32), h(33)					
	1	1	cn			
20	Data to designated channel and register					
	0	1	cn			

*Blank fields are not decoded; 111 in bit positions 13 to 15 are common to all XFR
DATA REGISTER FORMAT: 1 Limit applies to DX
0 Limit applies to DY

Register Address (Xfer Sequence)	MSB											LSB
0	11	10	LIMIT								0	
30	11	DY								0		
2	11	DX								0		
3	11	10	9	RVR						0		
35	TYPE		COLOR			INTRINSIC INTENSITY						
4	11	9	8	6	5	0						
5	11	Z								0		
6	11	Y								0		
7	11	X								0		
45	S	8	7	6	5	4	3	2	1	0	T	
9	S	8	7	6	5	4	3	2	1	0	F ₁ F ₂	
10	9	8	7	6	5	4	3	2	1	0	S	
11	9	8	7	6	5	4	3	2	1	0	G	
12	S	8	7	6	5	4	3	2	1	0		
13	S	8	7	6	5	4	3	2	1	0		
50	7	X		1	X							
EOM	15	13	12	5	4	3	0					

End of Mode:
Used to empty the image processor pipeline. The EOM code must follow immediately an IXC or IY code is used to terminate the light point mode and to start the vector write mode.

DETAILED DESCRIPTION OF NV COMPUTER 12

Each stage of NV computer 12 is shown in detail in FIGS. 2 through 6. Preferred embodiments are disclosed at the detailed logic level. Each component is described by function, input-output characters, or conventional nomenclature to enable one skilled in the arts of simulation, digital design, and computer programming to practice the invention. The components are additionally designated by the manufacturer's IC type number from the following integrated circuits data books:

Texas Instruments Incorporated, "The TTL Data Book for Design Engineers," First Edition, Copyright 1973.

National Semiconductor Corporation, "Digital Integrated Circuits," January 1974.

Advanced Micro Devices Inc., "Advanced Micro Devices Data Book," Copyright 1974.

unless otherwise specified. Further, many inverters are employed throughout NV system 10 for buffering signals with multiple loads. These buffer inverters are type 74S04 unless otherwise stated.

TRANSLATION STAGE 60

FIG. 2 shows translation stage 60 of image processor 42 and a portion of controller 46. Controller 46 receives image data in sequential order from computer 40 at an input 202 of a random access memory 204. The image data is arranged by frame in data blocks M bits wide and N words long. In this embodiment the frame block is 16 bits X, a multiple of 1024 words, and generates about 2000 light points making up the scene content of a single 1/30 second frame of CRT device 82. RAM 204 handshakes with a core memory in GP computer 40 to reproduce each frame of data. Image data is sequentially transferred from RAM 204 through a buffer register 206 to a light point data bus 207 and a texture data bus 208 in response to load pulses from interface controller 46.

RAM 204 may be formed by 16 1024 bit RAMS (93415 Fairchild) connected in parallel for holding the frame data. Register 206 may be formed by four 4 bit registers (74S175).

Frame data is coded as described in section II to enable one of six input registers 210, 220, 240, 250, 260 or 270 connected to light source data bus 207. X coordinate data for light sources in data base 48 is coded either INX(000) or IXC(010) and is loaded into a delta X input register 210 in response to load pulses from input control logic 66, preferably in concert with clock signals from a sync clock gate. Initialization vector data (V_i) follows a code XFR (111) and loads into X-Mux/Reg 211 on select from translation control logic 68. Initialization vectors load through bypass lead 212 to avoid delta X adder 213.

Initialization vectors position landmark points in data base 48 such as the beginning of light strings. After X-Mux 211 has been initialized, the delta X data of subsequent points in the string is loaded into input register 210 and passes through X adder 213 where each delta X is added to the X coordinate of the previous light point in the string generating the X_i s portion of the vector V_i s (X_i s, Y_i s, Z_i s) for each light source. Mux register 211 holds these previous coordinates and cycles them back to adder 213 on lead 215 for updating.

A normalization register 216 loads the updated X coordinate data, and left shifts leading zeros or ones for negative numbers in response to translation control logic 68. The first difference between most- and second-most-significant bit in normalization register 216 generates a normalization complete signal back to translation control logic 68 on lead 217. Normalization complete in any of the X, Y or Z normalization registers 216, 226 or 246 stops the normalization process of all the registers insuring that the normalized points maintain consistent dimension units and remain on the same line of vision as viewed on display 82. Normalization has the advantage of reducing the 24 bit initializa-

tion data into 16 bits of normalized data by eliminating either leading zeros or ones for negative numbers. The data load is reduced to 66% with negligible loss in position resolution. Logic control 68 then loads the normalized data into an output buffer register 218 which temporarily holds the data while X data for the next light point is accumulated.

Input register 210 may be formed by two 6 bit buffer registers (74S174) and one 4 bit buffer register (74S175) for accommodating the 13 remaining data bits. The three MSB of the 16 bit input on bus 207 was consumed by input code. These three bit places are now used in register 210 to propagate the sign bit to fill the 24 bit places of adder 213 input. Delta X data is a short distance for which 13 bits have been allotted, while initialization data is generally a greater distance and has been allotted 24 bits. Adder 213 may be formed by six 4 bit binary full adder (74283). X-Mux 211 may be formed by six quadruple 2 input multiplexer with storage (74298). Normalization register 216 may be formed by three 8 bit shift registers (74199). Buffer 218 may be formed by four TRI STATE quad D flip-flops (DM 8551 National).

Y coordinate data is coded INY(010) or IYC(011) for loading into delta Y input register 220. Y data is processed through delta Y adder 223 and Y-Mux 221 as described above with respect to X. Y data is left shifted in normalizer 226 and loaded into Y buffer 228. Z coordinate data is coded INZ(100) and is processed through the corresponding components 240, 243, 241, 246 and loads into Z output buffer 248. Preferably, both Y and Z components are constructed and operate identically to the X components to provide the Y_i s and Z_i s components of V_i s.

Output buffers 218, 228 and 248 operate in a TRI STATE configuration to output light source vectors (V_i s) on lead 249 to rotation stage 62 in response to an output enable signal from translation logic control 68. Only one output buffer may be enabled at one time which prevents mixing of X, Y and Z data.

Data on bus 207 concerning the number of light points in a string is coded STG(101) and through input logic control 66 enables a string counter 250 to load. The string data is held in counter 250 until a count pulse is received from logic control 68. Counter 250 then counts down through a zero detect circuit 252 providing a string complete signal back to translation logic control 68. Counter 250 may be formed by two down counters (74193). Zero detect 252 may be formed by two NOR gates (7425) and one NAND gate (74S00) as shown.

Data on bus 207 concerning color, intensity and flags is coded CIF(110) and through logic control 66 enables a CIF register 260 to load the CIF data. Register 260 holds the CIF data while coordinate data is processed on line 262 through translation stage 60 and rotation stage 62. Register 260 then loads into another CIF register (460 in FIG. 4) which holds the CIF data while coordinate data is processed through projection stage 64. The CIF data is then forwarded to image generator 44. CIF register 260 may be formed by two 6 bit registers (74S174) and one 1 bit flip-flop (74S74).

The 13 bits following code XFR(111) are additional code bits for identifying initialization vectors, rotation data, and texture data which are contained in the subsequent words. The XFR additional code is loaded into a transfer register 270 and processed into input control logic 66 to control the flow of light point data on subse-

quent word. Register 270 may be formed by two 6-bit registers (74S174) and one 1-bit flip-flop (74S74).

Texture data on bus 208 specifies painted (or greater-than-light-source-size) areas which are colored by electron beam scanning in the CRT displays.

The channel flat bit (XFR code 111, bit 11) indicates the window or viewing axis of the data. Each view axis or perspective requires a separate rotation stage 62, projection stage 64, image generator 44. However, the two front windows of aircraft 14 have very similar perspectives and may share a common channel which inputs to both devices 82 left and 82 right. Device 82, if implemented, requires a separate channel which is identified by the flag bits.

ROTATION STAGE 62

FIG. 3 shows rotation stage 62 of image processor 42 which multiplies the V 's at input 249 by a rotation matrix H provided on data bus 207 to produce the rotated vector or channel vector $V_c(X_c Y_c Z_c)$:

$$\begin{array}{r} X_c \\ Y_c \\ Z_c \end{array} = [H] \begin{array}{r} X_l \\ Y_l \\ Z_l \end{array}$$

The rotation matrix H is developed from yaw (ψ , left), pitch (θ , down) and roll (ϕ , right) motions. Assuming that the order of rotation is ψ followed by θ followed by ϕ , the matrices for the separate rotations from translated to rotated pilot eye or channel coordinates are as follows:

$$H\psi = \begin{bmatrix} \cos\psi & \sin\psi & 0 \\ -\sin\psi & \cos\psi & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$H\theta = \begin{bmatrix} \cos\theta & 0 & -\sin\theta \\ 0 & 1 & 0 \\ \sin\theta & 0 & \cos\theta \end{bmatrix}$$

$$H\phi = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi & \sin\phi \\ 0 & -\sin\phi & \cos\phi \end{bmatrix}$$

The composite matrix H describing this rotation is given by the matrix product

$$[H] = [H\phi] [H\theta] [H\psi]$$

The aircraft attitude matrix H is constant for each frame and is therefore computed only once per frame for each channel.

A multiplier multiplexer 310 receives 16 bit X_l , Y_l or Z_l data on lead 249 and sequentially outputs the data in four 4 bit parts (plus one carry place) to a multiplier register 320 in response to select signals from control logic 70. Register 320 receives the multiplexed 5 bit data in response to load signals from control logic 70, and simultaneously outputs to a flow-through multiplier array 330. The nine elements of rotation matrix data (H) from bus 207 load into a 16 word X 16 bit/word RAM 340 in response to control logic 68. As required during the rotation calculation, control logic 70 addresses RAM 340 and loads particular elements into a multiplicand register 350 which simultaneously outputs to array 330. Array 330 is a 16 bit by 4 bit multiplier and outputs to a product register 360 the product of a given matrix element times one of the 5 bit parts from register 320. Feedback line 362

causes the 16 MSB of these partial products to be combined to form the product of one element-coordinate product to product register 360. Four multiplication cycles are required for each position input data from 249. Accumulator register 380 holds the first element-coordinate product (18 bits) and adds the remaining two through adder 370 on feedback line 382 (18 MSB) as the remaining products become available from product register 360. Three cycles of accumulator 380 are required to form a single rotated coordinate coefficient (16 bits) at rotation stage output 384.

Multiplier MUX 310 may be three dual 4-1 MUX (75S153) connection parallel with one 4 bit input surplus. Multiplier register 320 may be one 6 bit register (74S174). Multiplier array 330 is eight flow-through multipliers (Am25505 Advanced Micro Devices) in 16 bit \times 4 bit configuration. RAM 340 may be four 16 word memories (74S189) with 5 words surplus. Multiplicand register 350 may be two 6-bit registers (74S174) and one 4-bit register (74S175) connected in parallel. Product register 360 may be three 6-bit registers (74S174) connected in parallel. Adder 370 may be four 4-bit binary full adders (74283). Accumulation register 380 may be three 6-bit registers (74S174).

PROJECTION STAGE 64

FIG. 4 shows projection and clipping stage 64 of image processor 42 which projects three-dimensional vectors $V_c(X_c Y_c Z_c)$ from stage 62 into a two-dimensional deflection vector V_d containing deflection data X_d and Y_d used by image generator 44 for positioning the electron beam in CRT displays. This projection is accomplished by dividing X_c and Y_c by Z_c through the binary division nonrestoring technique (described in "Digital Arithmetic — I" by Y. Chu, pages 39-43). $Z/2$ register 410 loads the divisor $Z_c/2$ and Mux/Register 420 selects and loads the dividend $X_c/2$ or $Y_c/2$ in response to control logic 70. The inputs to registers 410 and 420 are right-shifted by one digit to divide the V_c data on line 394 by two. Arithmetic logic unit ALU 430 then receives the dividend through a shift return loop 432 and adds or subtracts $Z_c/2$ thereto in response to a \pm function from logic 70. The dividend $\pm Z_c/2$ term is loaded into Mux 420, returned to ALU 430, and then combined with another $\pm Z/2$. The 16 bit output of ALU 430 is slew wired with respect to the 17 bit input to Mux 420 causing a division by two right shift. The binary division by Z_c requires 12 cycles for each X projection and each Y projection. The X_c/Z_c and Y_c/Z_c quotients are generated one bit at a time, MSB first, by comparing the sign bit (MSB) of Z_c with the sign bit of the partial remainder with Mux 420 through sign gate 436. The quotient bits individually enter quotient register 440 and are left-shifted by control logic 70. Z_c is loaded into renormalization register 450 and is right-shifted by control logic 68 the same number of places as were left-shifted in normalization 246 in translation stage 60. Color, intensity, and flag data on line 262 is loaded into CIF register 460 in response to control logic 68.

The contents of registers 440, 450 and 460 plus texture data on line 208 pass through multiplexer 470 and appear on output 472 in response to select signals from control logic 70. Data on line 472 is serially loaded into format registers 474a-p by decoder 476 in response to LOAD FORMAT REGISTER and FORMAT ADDRESS from control logic 68. Output 472 may inter-

face with a remotely positioned image generator 44, preferably through suitable line driver devices such as DM8830s. Clipping circuit 480 compares the sign bits of $Z_c/2$, $(X_c \text{ or } Y_c)/2$, and the contents of ALU 430 to determine if the light point being processed is within the field of view of the associated window or channel. The field of view may be logic clipped to any desired size; however, a square field of vision (53.14° by 53.14°) along the X and Y dimension is preferred because the arc cotangent of 26.57° is two. Thus, if $(X_c \text{ or } Y_c)/Z_c$ is less than two as determined by gate 482 and 484, the light point is within the logic field of view and enable flip-flop 486 provides a Load Enable signal to new point register 490 through new point gate 492 which, in junction with LOAD NEW DATA POINT from control 70, forwards the content of register 490 to image generator 44.

Gate 482 compares the sign bit of $(X_c \text{ or } Y_c)/2$ initially in register 420 to the sign bit of $(/X_c/ \text{ or } /Y_c/) + Z_c/2$ initially in register 420 to the sign bit of $(/X_c/ \text{ or } /Y_c/) + Z_c/2$ initially in register 430 to determine if $(X_c \text{ or } Y_c)$ is greater or less than $-Z_c/2$. All points having X_c or Y_c data greater than $-Z_c/2$ are outside the field of view and are not forwarded to image generator 44. The output of gate 482 is inverted and compared with the sign of $Z_c/2$ by gate 484 to inhibit all $-Z_c$ data. Gate 484 also inhibits all data within a given distance from aircraft 14 through one detector 488 which monitors the 10 MSBs of Z_c to inhibit all data with a Z_c value of five places or less.

Z register 410 may be three 6-bit registers (74S174). Mux/Register 420 may be five quadruple, 2-input multiplexers (74298) with storage. ALU 430 may be four 4-bit flowthrough arithmetic logic units (74S181). Sign gate 436 may be an exclusive OR gate (74S86). Gate 484 may be a three-input NOR gate (7427) with output inverted by a three-input NOR gate (7427) having two unused inputs grounded. Enable flip-flop 486 may be a JK flip-flop (74S112) with presetting and resetting gating circuitry responsive to control logic 70. One detector 488 may be two 5-input NOR gates (74S260) and one 2-input AND gate (74S08) having a high level output in the absence of ones. Register 474 and 490 may each be 28 6-bit registers (74174) operated in 12 pairs. Decoder 476 may be a 4-to-16 decoder (74154) with two surplus outputs. Gate 492 may be an AND gate (74S08).

The field of view cross-section is determined by the shape of each simulated window and may be controlled in many ways, i.e. software clipping by GP computer 40, logic clipping by image processor 42, electronic clipping by analog circuits in image generator 44, or optically clipped in CRT device 82. Alternatively, the dimensions of the effective display may depend on more than one form of clipping. In the present case a square pyramid of vision is established clipping circuit 480; however, a cone of vision may be established by providing a round CRT.

INPUT CONTROL LOGIC 66

FIG. 5 shows the detailed logic circuitry for input control logic 66. Image data bus 207 supplies a three bit decoder 510 with the three MSB of codes 15, 14, and 13 which are decoded into the eight code outputs for loading the six input registers of translation stage 60. The codes are described in more detail in Section VI, Data Format. Output zero INX(000) and output one IXC(001) are ORed through NAND gate 520 for

loading X coordinate data into delta X input register 210. Output two INY(010) and output three IYC(011) are ORed through AND gate 522 for loading Y coordinate data into delta Y input register 220. Output one IXC and output three IYC are ORed through NAND gate 524 to set a compute flip flop 526 into the compute mode. Compute flip flop 526 outputs to translation control logic 68 to initiate a compute operation. Output four INZ(100) loads Z coordinate data into delta Z input register 240. Output five STG(101) loads string length data into string counter 250. Output six CIF(110) loads color-intensity-flag data into CIF input register 260. Output seven XFR(111) loads additional code data into transfer register 270 and sets XFR flip flop 528 into the XFR mode. Flip flop 528 outputs to translation control logic 68 to indicate additional decoding is required. Sync gates 530 are preferably provided for syncing the loading pulses to translation stage 60. A Set and Decode Enable signal from translation control logic 68 clocks flip flop 526 and 528 through a NAND gate 540 and strobes three bit decoder 510 to initiate operation of input control logic 66 after each operation of translation control logic 68. A Clear Enable signal from translation control logic 68 clears flip flops 528 and 528 through a NAND gate 542 at the end of each operation. Flip flops 527 and 528 are synced by clock pulses through gates 540 and 542.

Input control logic 66 additionally decodes bits 12-4 from transfer register 270. Initialization bit 12 and channel bit 11 output into a gate network to provide:

Matrix Data signal to translation control logic 68 through AND gate 550 when bit 12 and bit 11 are true.

Enable All (-) signal to channel gates 570 through AND gate 552 when channel bit 11 is false.

Format Data signal to translation control logic 68 through AND gate 554 when bit 12 is false and bit 11 is true.

Load Format Register signal to projection stage 64 through NAND gate 556 when bit 12 is false, bit 11 is true, and an Enable Format signal from translation control logic 68 is false.

Destination Enable signal to destination decoder 572 through AND gate 558 and NAND gate 560 when bit 12 is true, bit 11 is false, and the Enable Format signal is false.

Channel data bits 10, 9, and 8 from transfer register 270 are additionally decoded into one of eight window perspectives or channels by a channel decoder 574. Decoder 574 outputs into eight channel gate 570 which are ORed with Enable All from gate 552. When Enable All is true, a single gate 570 is enabled by channel data to process rotation matrix data unique to that channel. When Enable All is false all gates 570 are enabled to process image data required by all channels. Channel data bits 7, 6, and 5 from transfer register 270 are additionally decoded by destination decoder 572 to one of six destination gates 576 during initialization operation for providing load signals to the appropriate translation accumulator 214, 224, or 244. An Enable All signal from translation control logic 68 enables all translation accumulators to load simultaneously during delta data or light point operation.

Decoders 510, 572, and 574 may be three-dual, two-line to four-line decoder (74155) connected in a three-line to eight-line configuration. AND gates 520, 522, 550, 552, 558, and 576 may be two input AND gates (74S08). NAND gates 524, 530, 540, 542, and 570

may be two input NAND gates (74S00). NAND gates 556 and 560 may be three input NAND gates (74S10). AND gate 554 may be a three input AND gate (74S11). Flip flops 526 and 528 may be one-half of a 4 bit register (74S175).

INPUT/TRANSLATION CONTROL LOGIC 68

The following flow chart description discloses the operation of input/translation control logic 68. The

operation includes STEPS 0-34 which are clocked in the order listed, and DECISIONS A-O. Control logic has three internal phases of operation (I, II, III) which occur as indicated. Numerous hardware circuits could be designed to perform these sequences generating the desired control signals to translation stage 60 and control logic 70.

LOADING TRANSLATION STAGE 60 INPUT REGISTER

STEP 0	(a)	Initial state of input/translation control logic 68.		
	(b)	Begin Phase I (XYZ counter 00).		
STEP 1		SET AND DECODE ENABLE signal enables 3 bit decoder 510, flip flop 526, and flip flop 528 to be set by 3 bit data code, permitting light point data to load into one of registers 210, 220, 240, 250, 260 or 270 of translation stage 60 if IP DAV true from IP DAV flip flop 205.		
	DECISION A	Is IP DATA AVAILABLE true?	YES	STEP 2
			NO	STEP 1
STEP 2		IP DATA REQ signal from control logic 68 resets flip flop 205.		
	DECISION B	Is COMPUTE flip flop 526 set?	YES	DECISION M
			NO	DECISION C
	DECISION C	Is TRANSFER flip flop 523 set?	YES	DECISION D
			NO	STEP 1
	DECISION D	Is destination of data either RAM 340 (matrix data) or format register 474 (texture data)?	YES	STEP 9
			NO	DECISION E
	DECISION E	Is END OF MODE signal in transfer register 270 true?	YES	DECISION J
			NO	STEP 3

INITIALIZATION OF MUX/REG 211, 221, OR 241

STEP 3		No operation - waiting for DECISION F to be YES.		
	DECISION F	Is IP DATA AVAILABLE true?	YES	STEP 4
			NO	STEP 3
STEP 4		EN FORMAT signal (inputs to gates 556 and 560) causes initialization data to load into 211, 221 or 241.		
STEP 5	(a)	IP DATA REQ signal resets flip flop 205.		
	(b)	CLEAR ENABLE signal from control logic 68 clears flip flops 526 and 528 and transfer register 270.		
	(c)	Return to STEP 1.		

INITIALIZATION OF RAM 340 OR FORMAT REGISTER 474

STEP 9	(a)	Clear RAM/format address counter in control logic 70.		
	(b)	Set ENABLE flip flop 486.		
STEP 10		No operation - waiting for DECISION G to be YES.		
	DECISION G	Is IP DATA AVAILABLE true?	YES	STEP 11
			NO	STEP 10
STEP 11	(a)	Enable RAM 340 to write if MATRIX DATA signal from gate 550 true.		
	(b)	EN FORMAT signal enables gate 556 making load format register signal true for enabling decoder 476.		
STEP 35		No operation - provide settling period before STEP 12.		
STEP 12	(a)	IP DATA REQ signal clears flip flop 205.		
	(b)	Advance RAM/format address counter (of STEP 9a).		
	DECISION H	Is RAM/format address counter equal to 8 and MATRIX DATA signal from gate 550 true?	YES	STEP 1
			NO	DECISION I
	DECISION I	Is RAM/format address counter equal to 15?	YES	STEP 6
			NO	STEP 10
STEP 6		No operation - waiting for DECISION J to be YES.		
	DECISION J	Is DISPLAY BUSY signal from busy logic 688 true?	YES	STEP 6
			NO	STEP 7
STEP 7	(a)	Load new point register 490.		
	(b)	Same as STEP 5b.		
	(c)	Return to STEP 1.		

END OF MODE

STEP 13		No operation - waiting for DECISION J to be YES.		
	DECISION J	Is MULTIPLICATION/DIVISION DONE signal from control logic 70 true?	YES	STEP 14
			NO	STEP 13
STEP 14	(a)	Begin Phase II (XYZ counter 01).		
	(b)	Same as STEP 5b.		
	(c)	Provide MULTIPLICATION START signal to control logic 70.		
	(d)	Provide DIVISION START signal to control logic 70.		
STEP 15		No operation - waiting for DECISION K to be YES.		
	DECISION K	Same as DECISION J	YES	STEP 16
			NO	STEP 15
STEP 16		Begin Phase III (XYZ counter 10). Provide DIVISION START signal to control logic 70.		
STEP 17		No operation - waiting for DECISION L to be YES.		
	DECISION L	Same as DECISION J	YES	STEP 18
			NO	STEP 17
STEP 18	(a)	Set startup flip flop in control logic 68.		
	(b)	Return to Phase I.		
	(c)	Return to STEP 1.		

LIGHT DATA PROCESSING

-continued

STEP 19	Enable loading of buffer registers 218, 228 or 248 if STARTUP flip flop (STEP 18a) is set and if Phase II is true.		
DECISION M	Same as DECISION J	YES NO	STEP 20 STEP 19
STEP 20	(a) Provide MULTIPLICATION START signal except when STARTUP flip flop is set and Phase I is true. (b) Provide DIVISION START signal except when STARTUP flip flop is set and Phase I true or Phase II true. (c) Begin next phase. (d) Clear RAM/format address counter (STEP 9a). (e) Clear STARTUP flip flop (STEP 18a) if Phase III true (prior to STEP 20c). (f) Load CIF register 460 if Phase III true (prior to STEP 20c).		
DECISION N	Is Phase I true (prior to STEP 20c)?	YES NO	STEP 21 DECISION Q
DECISION O	Are COMPUTE signal from gate 254 not true and Phase III true (prior to STEP 20c)?	YES NO	STEP 21 STEP 19
STEP 21	(a) ENABLE ALL signal from control logic 68 enables gates 576 to enable loads to MUX/registers 211, 221 and 241 from adders 213, 223 and 243. (b) Same as STEP 5b. (c) Enable string counter 250 to count down one light.		
STEP 22	Enable normalize registers 216, 226 and 246 to load data from MUX/registers 211, 221 and 241.		
STEPS 23-33	Allow normalize registers 216, 226 and 246 to left shift until NORMALIZATION COMPLETE signal.		
STEP 34	(a) Same as STEP 23. (b) Return to STEP 19.		

ROTATION AND PROJECTION CONTROL LOGIC

70

30 The following flow chart description discloses the operation of rotation-projection control logic 70 similar in approach to Section XII.

ROTATION CONTROL SEQUENCE

STEP 0	(a) Clear product register 360. (b) Clear accumulation register 380.		
DECISION A	Is MULTIPLICATION START from control logic 68 true?	YES NO	STEP 2 STEP 1
STEP 1	Provide MULTIPLICATION DONE signal to control logic 68.		
DECISION B	Same as DECISION A	YES NO	STEP 2 STEP 1
STEP 2	(a) Same as STEP 0a. (b) Select BYTE 0 from MUX 310. (c) Load multiplier register 320. (d) Load multiplicand register 350. (e) Provide OUTPUT ENABLE to X buffer register 218.		
STEP 3	(a) Load product register 360. (b) Select BYTE 1 from MUX 310. (c) STEP 2c. (d) STEP 2e.		
STEP 4	(a) STEP 3a. (b) STEP 0b. (c) Select BYTE 2 from MUX 310. (d) STEP 2c. (e) STEP 2e.		
STEP 5	(a) STEP 3a. (b) Select BYTE 3 from MUX 310. (c) STEP 2c. (d) Advance RAM/format counter of STEP 9a (Section XII). (e) STEP 2e.		
STEP 6	STEP 3a.		
STEP 7	Load accumulator register 380.		
STEP 8	(a) STEPS 2a-d. (b) Provide OUTPUT ENABLE signal to Y buffer register 228.		
STEP 9	(a) STEPS 3a-c. (b) STEP 8b.		
STEP 10	(a) STEP 3a. (b) STEP 4c. (c) STEP 2c. (d) STEP 8b.		
STEP 11	(a) STEP 3a. (b) STEP 5b. (c) STEP 2c. (d) STEP 5d. (e) STEP 8b.		
STEP 12	STEP 3a.		
STEP 13	STEP 7.		
STEP 14	(a) STEPS 2a-d. (b) Provide OUTPUT ENABLE signal to Z buffer register		

-continued

		248.		
STEP 15	(a)	STEPS 3a-c.		
	(b)	STEP 14b.		
STEP 16	(a)	STEP 3a.		
	(b)	STEP 4c.		
	(c)	STEP 2c.		
	(d)	STEP 14b.		
STEP 17	(a)	STEPS 5a-d.		
	(b)	STEP 14b.		
STEP 18	(a)	STEP 3a.		
	(b)	STEP 1.		
STEP 19	(a)	STEP 7.		
	(b)	STEP 1.		
	(c)	Load buffer registers 218, 228 and 248 if Phase II true.		
	(d)	Return to DECISION A.		
PROJECTION CONTROL SEQUENCE				
STEP 0		No operation - waiting for DECISION A to be YES.		
DECISION A		Is DIVISION START signal from control logic 68 true?	YES	STEP 2
			NO	STEP 1
STEP 1	(a)	Provide DIVISION DONE signal to control logic 68.		
	(b)	Select texture data bus 208 through output MUX 470.		
DECISION B		Same as DECISION A	YES	STEP 2
			NO	STEP 1
STEP 2	(a)	Select Xc,Yc into MUX register 420.		
	(b)	Load MUX register 420.		
	(c)	Select CIF register 460 through output MUX 470.		
	(d)	Provide CIF format address to decoder 476.		
	(e)	Load Z/2 register 410 if Phase I true.		
	(f)	Provide load format register signal to decoder 476 if Phase I true.		
	(g)	Load clipping result into ENABLE flip flop 486 if Phase I true.		
STEP 3	(a)	Provide DIVIDE signal NOT TRUE to projection stage 64.		
	(b)	Load clipping result into ENABLE flip flop 486 if Phase I not true.		
	(c)	STEP 2c.		
	(d)	STEP 2d.		
	(e)	Enable register 450 to load from register 410 if Phase I true.		
STEP 19	(a)	Provide output = input function to ALU 430.		
	(b)	STEP 2b.		
	(c)	Select ALU 430 into MUX/register 420.		
	(d)	Allow renormalization register 450 to right shift until renormalization complete if Phase I true.		
STEP 4-14	(a)	Provide DIVIDE signal TRUE to projection stage 64.		
	(b)	Enable quotient register 440 to shift one quotient bit.		
	(c)	STEP 19c.		
	(d)	STEP 2b.		
	(e)	STEP 19d.		
STEP 15	(a)	STEP 4a.		
	(b)	STEP 4b.		
	(c)	STEP 4c.		
	(d)	STEP 4d.		
	(e)	Select register 440 through output MUX 470 if Phase I false.		
	(f)	Provide Yd format register address to decoder 476 if Phase III true.		
	(g)	Provide Xd format register address to decoder 476 if Phase II true.		
	(h)	Provide LOAD FORMAT REGISTER signal to decoder 476.		
	(i)	Select register 450 through output MUX 470 if Phase I true.		
	(j)	Provide Zc format register address to decoder 476 if Phase I true.		
STEP 16	(a)	STEP 15e.		
	(b)	STEP 15f.		
	(c)	STEP 15g.		
	(d)	STEP 15i.		
	(e)	STEP 15j.		
DECISION C		Is Phase III true?	YES	DECISION D
			NO	DECISION A
DECISION D		Is DISPLAY BUSY true?	YES	STEP 17
			NO	STEP 18
STEP 17		No operation - waiting for DECISIONS C and D. to be YES and NO, respectively.		
STEP 18	(a)	Load new point register 490.		
	(b)	STEP 1b.		
	(c)	Return to DECISION A.		

DEFLECTION STAGE 72

FIG. 6 shows X deflection generator 604, Y deflection generator 606 and CRT unblanking circuit 608 which receive digital deflection data Xd and Yd from projection stage 64 and generate analog X and Y de-

flexion voltages and unblank periods for CRT display devices 82. In deflection generator 604, Xd data from new point register 490h enters X A/D converter 610. The MSB of Xd is inverted from the 2's complement format of register 474h into the binary format. Opera-

tional amplifier 620 receives the analog output of A/D 610 which is summed with X VECTOR GENERATOR signal. Amplifier 620 also receives X OFFSET signal through scaling resistors 622 for positioning the CRT display within the rotated data window of state 72. The analog output of amplifier 620 is preferably limited to ± 5 volts by clipping network 630 which defines the X dimension of the CRT display. The ± 5 ma output of amplifier 620 is preferably increased to ± 100 ma by power driver 640. X deflection voltage at output 642 drives the deflection circuits of display device 82. Y deflection generator 606 is identical in structure and operation to X generator 604.

A/D converter 610 may be a 12 bit binary unipolar device (AD562 KD-BIN) from Analog Devices which provides a feedback resistor in feedback line 624. Amplifier 620 may be a feedback operational amplifier (NE531) from Signetics in summing configuration. Resistors 622 are preferably 10,000 ohms each. Clipping network 630 may be two 5.1 volt zenor diodes (1N751A) connected in reverse polarity and in back-to-back configuration with two switching diodes (1N914). Power driver 640 may be a suitable output amplifier capable of driving ± 5 volts at a load current of ± 200 ma at a maximum full output frequency of 3 MHz, such as power driver (model 9824) by Optical Electronics Incorporated.

Unblanking circuit 608 generates CRT UNBLANK to CRT devices 82 causing the electron beam to strike the CRT phosphor simulating a light point in data base 48. A CRT blank period or beam stabilization increment between each point activation is determined for each new light point and is sufficient to permit acceleration, movement and deceleration of the electron beam. First, X_d and Y_d load into increment decoder 650. Decoder 650 retains the previous data point X_d and Y_d , and by systematic comparison to the new light point X_d and Y_d , identifies which is greater, delta X_d or delta Y_d . Then decoder 650 enters a 1 into timing register 680 along one of eight outputs in accordance with the magnitude of the identified delta. Clock 682 then progressively left shifts the 1 to the MSB activating unblank timer 684. The number of clock pulses required is greater for larger deltas allowing time for the electron beam to move to the new light source position. Unblank timer 684 determines the exposure time during which the electron beam activates the CRT phosphor. Potentiometer 686 is provided for adjusting the unblank period to accommodate the video gain of CRT device 82 and for particular CRT phosphors. A 5 microsecond unblank period is preferred for the Kratos 25 inches beam penetration display CM 325S1. Unblank logic 686 combines the output of unblank timer 684 with DEFLECTION ENABLE from control logic 70 to provide CRT UNBLANK to CRT device 82.

Busy logic 688 inhibit data processing through new point register 490 by a BUSY signal to control logic 70 between the loading of each new point into image generator 44 and the termination of the CRT UNBLANK period for that new point. BUSY also inhibits clock 682 during the same period.

Deflection clear circuit 690 limits the time period during which the deflection coils in CRT device 82 will be required to maintain any electron beam position. After expiration of the maximum deflection period, which in the present case is about eight milliseconds, clear circuit 690 provides DEFLECTION CLEAR to control logic 70. Clear circuit 690 prevents damage to

the deflection coils during startup, shutdown, or system malfunction which might otherwise cause maximum deflection current to needlessly flow through the coils beyond the ratings of the coils.

Increment decoder 650 and the operation of BUSY is shown in more detail in patent application Ser. No. 642,645 entitled "Real-Time Simulation of a Point System Having Coordinated Data Flow as Viewed by a Moving Observer" and filed on Dec. 19, 1975 by R. G. Nielsen and assigned to the present assignee.

Timing register 680 may be an 8-bit register (74199) with J and K inputs at + 5 volts and clock-inhibit grounded.

Clock 682 may be any oscillator having a three-dimensional period.

Unblank timer 684 may be a oneshot (74121) using the A1 and A2 inputs and an external 20K ohm timing resistor.

Unblank logic 686 may be an AND gate (7410) and a 50 ohm driver (7440) connected in series therewith.

Busy logic 688 may be a flip-flop (7474) set by LD NEW DATA PT and clocked by the inverted output of timer 684, with D input grounded.

PREFERRED EMBODIMENT OF DIRECTIONAL LIGHT

FIG. 7 shows an airport runway 710 positioned within a stationary XYZ coordinate system 730 with a string of centerline lights 720M marking the midportion of runway 710, bidirectional lights 720TD marking the touchdown portion of runway 710, and bidirectional lights 720E marking the end of runway 710. Centerline light string 720 is coincident with axis 730X of coordinant system 730; and each bidirectional light is orientated transversely of axis 730X establishing a color threshold plane $X=C$ perpendicular to axis 730X. C is the X coordinate of the bidirectional light. Lights 720TD and 720E and X axis responsive. Simulated aircraft 740 is shown approaching runway 710 with the cockpit at the origin of moving XYZ coordinate system 742. During a normal approach axis 742X, 742Y and 742Z of moving coordinate system 742 are generally parallel to axis 730X, 730Y and 730Z respectively of stationary coordinate system 730. During the approach of aircraft 740 directional centerline lights 720TD are visible as green lights in the front display 82 of craft 740, lights 720M are visible as white lights, and lights 720E are visible as red. Lights 720TD and 720E are bidirectional and are visible in the reverse color pattern to accommodate aircraft landing in the opposite direction on runway 710. As lights 720TD pass directly under aircraft 740 their visible color changes to red; lights 720M do not change color, and lights 720E change from red to green. That is, when X_l s coordinate of each bidirectional light (in aircraft coordinate system 742) is positive that light is green and when X_l s is negative, that light is red. In the case of aircraft 740 lights 720TD and 720E are clipped from the field of view by projection stage 64 just prior to changing color. However, lights 720 may be visible from the side display of aircraft 740, especially if aircraft 740 lands to one side of the centerline axis 730X.

A second aircraft 750 is shown taxiing along adjacent runway 752 which is at an angle with respect to center axis 730X of runway 710. The coordinate system 754 for aircraft 750 is translated from ground coordinate system 730 by position vector V_p of aircraft 750 without rotation. The axes of moving system 754 are gener-

ally parallel to the corresponding axes of ground system 730. The color of each directional light is a function of the sign of the X coordinate X_l s. When X_l s is positive that light is green; when X_l s is negative that light is red. Centerline lights 720 are visible in the front display of aircraft 750, and lights 720TD and 720E still appear as green or red, and will change color as the origin of translated moving coordinate system 754 passes through the color threshold plane for each light. By orientating the X axis of stationary coordinate system 730 to be coincident to, or merely parallel with, centerline lights 720, the color of each light 720TD and 720E is determined by the sign of the X coordinate of that light as translated into the moving coordinate system by translation stage 60 prior to rotation by rotation stage 62.

Y responsive bidirectional light strings 760 are shown on runway 762 parallel to axis 730Y. Lights 760 establish a $Y=C$ color threshold plane, and their color is dependent on the sign of Y_l s in translated unrotated coordinate system 750. Light 780 on top of building 782 is one color responsive, and establishes a color threshold plane $Z = \text{height of building 782}$ (assuming light 770 to be mounted at roof level). Light 780 changes from on (any color) to off (black) as viewed from descending aircraft passing through the height Z plane.

FIG. 8 shows XY directional logic 264a for converting the sign bit of X_l s of lights 720TD and 720E and Y_l s of lights 760 into one of two colors C- or C+. XY Mux 810 receives both SIGNX and SIGNY from the MSB of X Mux 211 and Y Mux 221, respectively, and selects either X or Y as the color sensitive axis in response to XY Flag bit, a 0 or 1 in the MSB of CIF register 260. CIF register 260 contains 3 bits of C- and three bits of color C+ provide a selection of eight colors (or shades of colors) including black for each side of the color threshold plane. The proper color C is selected by color Mux 820 in response to a select signal from XY Mux 810. The selected color C is loaded into CIF register 460 in response to a load signal from control logic 68.

Z directional logic 264b is responsive to SIGNZ of light 780 from Mux 241 (which is loaded into the MSB of CIF register 460) and Z Flag from the second MSB of registers 260 and 460. Z code indicates whether or not the light being processed is Z axis responsive. Z gate 830 combines SIGNZ with Flag Z and outputs to three intensity gates 840. Three bits intensity data input to intensity gate 840 to provide eight intensity levels out to intensity stage 74. Zero intensity (black) may be introduced by the 000 code of the intensity code bits. Black may also be introduced by a 0 from SIGNZ and Z code for a light which is black in one direction.

XY Mux 810 may be three NAND gates (74S00) connected in multiplexer configuration using the Q and Q bar outputs of the flip-flop forming the MSB of CIF register 260. Color Mux 820 may be three sections of one Quad two input Mux (74S157). Gate 830 may be a NAND gate (7400) and gates 840 may be AND gates (7408).

Multiaxis directional lights responsive to XZ or YZ such as bidirectional landing lights on the deck of an aircraft carrier may be processed by logic 264. An XYZ responsive light requires a Flag bit for each axis and, if desired, a color data for Z. An XYZ light has a selection of colors separately activated for each quarter hemisphere by XYZ sign data.

Runway 790 which is not parallel to either axis 730X or 730Y may incorporate bidirectional effects by a data rotation operation performed by software in GP computer 40 or additional hardware in image processor 42.

CONCLUSION

It will be apparent to one skilled in the art that the objects of this invention have been accomplished by processing image data, including directional point data, through the system to a display device. Directional flag bits are provided to define the character (color, intensity, etc.) and orientation (X, Y or Z responsive) of each directional point.

The foregoing specification is for illustrative purposes only and modifications may be made in the disclosed embodiment without departing from the scope of the invention. For example, an entire face of an object may have directional characteristics which are defined by the directional data and painted into the CRT display. The reflective properties of a surface or the nature of the illumination may create directionally dependent shading. Further, the directional characteristic may relate to color, intensity, on-off, occulting or other considerations.

We claim as our invention:

1. A data processor responsive to observer position and orientation data and to object point data to simulate an image display of the visual relationship between an observer in a moving coordinate system and the object points in at least one object coordinate system; at least one object data source for providing object point digital position data, and directional data for object points having characteristics which vary as a function of the direction in which the object is viewed; computer means for receiving object point data and adapted to receive observer position and orientation data, responsive to the received data for providing a predetermined image digital data format having dedicated code bits for identifying classes of data; a hard-wired image circuit which receives the image data format and is responsive to the code bits for processing the data, and responsive to the observer position data for translating the object point data into the observer coordinate system, and responsive to the orientation data for rotating the object point data to accommodate the observer's axis of viewing, and which is adapted to forward the object point data to the image display device for providing a scene of the object point data in the observer perspective; and a hard-wired direction circuit which compares the observer position data with the object point data of each object point for determining the specific direction of the observer position relative to each object point, and which selects specific directional data for each object point based on the determined direction.
2. The data processor of claim 1, wherein the directional data defines the orientation and visual characteristics of at least a portion of the object points.
3. The data processor of claim 2, wherein at least some of the object points are light points having directional aspects.
4. The data processor of claim 3, wherein the light points have directional intensity.

5. The data processor of claim 4, wherein the light points have directional color.

6. The data processor of claim 3, wherein each the directional light point is responsive to the observer position along one axis of the object coordinate system axis, and establishes a threshold plane perpendicular to the axis of response defined by the relationship:

$$X = A$$

where X is any axis of the object coordinate system and A is a different constant for each light point.

7. The data processor of claim 6, wherein each directional light point is position responsive to two axes and establish threshold planes defined by the relationship:

$$\begin{matrix} X = A \\ Y = B \end{matrix}$$

where X and Y are any two axes of the object coordinate system and A and B are different constants for each light point.

8. The data processor of claim 7, wherein each directional light point is position responsive to all three axes and establishes threshold planes defined by:

$$\begin{matrix} X = A \\ Y = B \\ Z = C \end{matrix}$$

where X, Y and Z are the axes of the object coordinate system and A, B and C are different constants for each light point.

9. The data processor of claim 3, wherein the directional lights form at least one set of lights responsive to the observer position along at least one axis of the object coordinate system.

10. The data processor of claim 9, wherein at least one set of lights form a string parallel to one axis.

11. The data processor of claim 10, wherein at least one string of lights is position responsive to the parallel axis.

12. The data processor claim 11, wherein the string of lights is color responsive.

13. The data processor of claim 3, wherein the directional lights form at least two sets of lights, one set responsive to at least one axis and the other set responsive to at least one other axis.

14. The system of claim 3, wherein some of the object light points have directional aspects responsive to observer position along at least one axis of the object coordinate system, and the data format includes directional data indicating the particular axis of the object

coordinate system to which each directional light is responsive.

15. The system of claim 14 wherein the origin of the observer coordinate system is coincident with the observer, and the hard-wired direction circuit is responsive to the signs of the directional light point coordinates in the observer coordinate system to select the proper characteristics of the directional aspects responsive to each axis of the object coordinate system.

16. A real-time digital system for simulating the image of a point structure as viewed by a movable observer within a gaming area, comprising:

object digital data source for providing object point data including a plurality of directional points having at least one directionally dependent characteristic;

observer digital data source for providing real-time observer orientation data and real-time position vectors extending from a first reference point in the observer coordinate system to a second reference point in the object coordinate system;

computer means responsive to the position vectors for translating object coordinates into observer coordinates, and for entering the orientation data and the object data and the directional data into storage according to a predetermined format;

image processor responsive to the formatted data for adjusting the perspective of the object data to conform to the orientation of the observer;

direction circuit responsive to the observer position relative to each object point for providing the corresponding directionally dependent characteristic; image generator responsive to perspective adjusted data for providing deflection voltages; and

display means responsive to the deflection voltages for providing a scene of the object data source in the perspective of the observer.

17. The system of claim 16, wherein the first reference point in the observer coordinate system is the origin of the observer system and is proximate the apex of the simulated field of vision.

18. The system of claim 17, wherein the second reference point in the object coordinate system is the origin of the object coordinate system.

19. The system of claim 16, wherein the display means is a CRT device with X and Y deflection circuits responsive to the deflection voltages for generating points of excitation on the CRT phosphor screen.

20. The system of claim 19, wherein the directional points are intensity responsive to direction and the image generator provides an intensity voltage to the control input of the CRT device.

21. The system of claim 19, wherein the CRT device is a random deflection type.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 4,027,403
DATED : June 7, 1977
INVENTOR(S) : David R. Marsh and Raymond C. Osofsky

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 6, line 22, insert "codes" after "XFR".

Col. 6, line 54, change "IY" to --IYC. The EOM--.

Col. 19, line 5, change "state 72" to --stage .--

Col. 19, line 39, change "1" to --"1"--.

Col. 19, line 42, change "1" to --"1"--.

Col. 21, line 34, change "0 or 1" to -- "0" or "1"--.

Col. 24, line 8, change "characteristics" to --characteristic--.

Signed and Sealed this

Twenty-second Day of November 1977

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

LUTRELLE F. PARKER
Acting Commissioner of Patents and Trademarks