

BFD-68 SYSTEM HARDWARE

PREFACE

THIS MANUAL DESCRIBES THE CHARACTERISTICS OF THE SSB MINIFLOPPY INTERFACE. THIS INTERFACE ALLOWS USERS OF THE SWTPC 6800 MICRO-COMPUTER SYSTEM TO EASILY INTERFACE UP TO THREE S.A. 400 MINIFLOPPY DISKETTE STORAGE DRIVES.

BOOT AND I/O ROUTINES

TO FACILITATE DISC I/O A ROM HAS BEEN PROVIDED ON THE DISC INTERFACE BOARD. THE ROM CONTAINS ALL NECESSARY I/O ROUTINES TO READ, WRITE, SEEK, STEP AND RESTORE THE DISC DRIVES. IN ADDITION, A DISC BOOT ROUTINE HAS BEEN INCLUDED IN THE ROM TO ALLOW EASY ACCESS TO ANY SYSTEM STORED ON A DISC.

DISC CONTROL

DISC CONTROL IS ACHIEVED BY THE USE OF THE WESTERN DIGITAL FD1771B-01 FLOPPY DISC CONTROLLER IC. THIS IC CONTROLS READ/WRITE FORMAT, HEAD STEP, SEEKING, AND CHECKS THE WRITE PROTECT STATUS OF THE DISC. THE READ/WRITE FORMAT CAN BE PROGRAMMED TO MANY FORMATS INCLUDING IBM 3740 FORMAT. CRC GENERATION AND CHECKING ARE ALSO PERFORMED WITHIN THE FD1771B-01 IC. ADDITIONAL INFORMATION ON PROGRAMMING THE FLOPPY DISC CONTROLLER CHIP MAY BE FOUND IN THE WESTERN DIGITAL FD1771B-01 PRODUCT GUIDE.

FD1771B-01 CONTROL

ALL COMMUNICATIONS BETWEEN THE HOST SYSTEM AND THE FD1771B-01 IC ARE THROUGH A 6820 PIA. CONTROL LINE FUNCTIONS OF THE FD1771B-01 ARE HANDLED BY THE A-PORT AND OTHER PROGRAMMABLE CONTROL INPUT/OUTPUT PINS OF THE PIA. DATA TO AND FROM THE FLOPPY DISC CHIP IS TRANSMITTED THROUGH THE B-PORT OF THE PIA.

ROM

THE ROM LOCATED AT U17 PROVIDES 512X8 BITS OF INFORMATION FOR THE USER. THE ROM ADDRESSING IS DECODED TO USE ALL UNUSED ADDRESSES IN THE I/O PAGE BETWEEN '8020'H AND '83FF'H. THE 9328 DECODER U23 PROVIDES HIGH ORDER ADDRESS DECODING. USE OF UNUSED AREAS OF THE I/O PAGE IS ACHIEVED BY REQUIRING ADDRESS BIT 5 TO BE TRUE TO ENABLE THE ROM. ADDRESS BITS 0-4 OF THE ROM ARE DRIVEN BY ADDRESS LINES 0-4. ADDRESS BITS 5-8 ARE DRIVEN BY ADDRESS LINES 6-9. THE FIGURE BELOW ILLUSTRATES THE INTERLEAVING OF I/O AND ROM ADDRESSES.

ROM MEMORY MAP

	'8000'H	USED BY I/O
	'801F'H	
	'8020'H	USED BY ROM
	'803F'H	
	'8040'H	USED BY I/O
	'805F'H	
	'83A0'H	USED BY ROM
	'83BF'H	
	'83C0'H	USED BY I/O
	'83DF'H	
	'83E0'H	USED BY ROM
	'83FF'H	

THE ABOVE FIGURE SHOWS I/O MEMORY ILLUSTRATED PAGES OF 32 WORDS. WHEN BIT 5 IS A 0 THAT 32 WORD PAGE IS USED AS I/O LOCATIONS. WHEN BIT 5 IS A 1 THAT PAGE IS DECODED BY THE ROM AS ONE OF ITS ADDRESSES AND THE PARTICULAR BYTE OF INFORMATION REQUIRED IS PLACED ON THE SYSTEM DATA BUSS.

DISC INTERFACE

ADDRESS DECODING FOR THE 6820 PIA IS PROVIDED FOR BY NAND GATE U22 AND THE 9328 DECODER, U16. THE 74LS30 8-INPUT NAND GATE U22 GENERATES THE NON-PROGRAMMABLE ADDRESS DECODING OF THE ADDRESS BITS A5-A12 AT U22-8 TO THE CS2- INPUT AT U4 PIN 23. REGISTER SELECTION WITHIN THE PIA IS CONTROLLED BY ADDRESS LINES A0 AND A1 AT U4 PINS 36 AND 35.

THE PIA DATA INPUTS (U4, 26-33) ARE TIED DIRECTLY TO THE THE NEGATIVE TRUE SYSTEM DATA BUSS. CARE MUST BE EXERCISED IN PROGRAMMING THE PIA AS THE PIA EXPECTS TO SEE POSITIVE TRUE DATA AT THE SYSTEM PORT. ALL CONTROL FUNCTIONS SENT TO THE PIA SHOULD FIRST BE COMPLEMENTED BY THE CONTROLLING PROGRAM. ALL CONTROL INFORMATION RECEIVED FROM THE PIA SHOULD BE INTERPRETED AS NEGATIVE TRUE DATA BY THE RECEIVING PROGRAM. THE DAL- LINES OF THE FD1771B-01 IC ARE TIED TO THE B-PORT OF THE PIA AT U11(10-17). DATA TO AND FROM THE FD1771B-01 ON THE DAL LINES IS DEFINED AS NEGATIVE TRUE DATA. AS DATA IS NOT INVERTED THROUGH THE PIA, IT IS NOT NECESSARY TO INVERT DATA FROM OR TO THE FD1771B-01 AS IS REQUIRED WITH THE CONTROL REGISTERS OF THE PIA. DATA EXCHANGE BETWEEN THE PIA AND FD1771B-01 ARE CONTROLLED BY THE FOLLOWING CONTROL LINES:

WRITE ENABLE

CB2 OF THE PIA IS USED TO STROBE INFORMATION FROM THE 6820 INTO THE FD1771B-01. CRB BITS 3-5 SHOULD BE PROGRAMMED TO '101'. IN THIS MODE CB2 IS CLEARED ON THE POSITIVE TRANSITION OF THE FIRST 'E' PULSE FOLLOWING A WRITE 'B' DATA REGISTER OPERATION AND SET HIGH ON THE POSITIVE TRANSITION OF THE NEXT 'E' PULSE. DURING WRITE OPERATIONS THE READ FLIP-FLOP, U15, MUST BE DISABLED BY PROGRAMMING A-PORT BITS 6 AND 7 TO 1 AND 0 RESPECTIVELY.

REGISTER SELECT

A-PORT BITS 0 AND 1 DRIVE THE REGISTER SELECT LINES OF THE FLOPPY DISC CONTROLLER CHIP. PA0 DRIVES ADDRESS LINE A0 AND PA1 DRIVES ADDRESS LINE A1.

CHIP SELECT

A-PORT BIT 2 (U4-4) DRIVES THE CHIP SELECT INPUT OF THE FD1771B-01. WHEN PA2 IS 0 THE FLOPPY DISC CHIP WILL BE ENABLED.

READ ENABLE

READING INFORMATION FROM THE FDC IS CONTROLLED BY ITS READ ENABLE INPUT AT U11-4. THIS INPUT IS DRIVEN BY THE READ ENABLE FLIP-FLOP U15-6. FLIP-FLOP U15 IS USED IN TWO MODES. MODE ONE IS USED WHEN READING CONTROL REGISTERS IN THE FD1771B-01. MODE TWO IS USED WHEN READING DATA FROM THE DISC. IN MODE ONE PA6 (U4-8) IS PROGRAMMED TO '0'. PA6 LOW FORCES U15-6 TO THE LOW STATE THEREBY ENABLING INFORMATION FROM SELECTED REGISTER ONTO THE DAL LINES (U11,7-14). THIS INFORMATION CAN THEN BE READ IN ON THE B-PORT OF THE PIA. IN MODE TWO PA6 AND PA7 (U4-8,9) ARE PROGRAMMED TO '1'S. WHEN DRQ (U11-38) COMES TRUE AND PA7 IS TRUE FLIP-FLOP U15 WILL BE SET ON THE POSITIVE TRANSITION ON THE 1 MHZ CLOCK (U15-12). DRQ IS ALSO TIED TO THE CA2 INPUT OF THE PIA (U4-39). THIS PROGRAMMABLE PIN IS PROGRAMMED AS AN INPUT TRIGGERED BY A POSITIVE TRANSITION (CRA BITS 3-5 =110). ON THE POSITIVE TRANSITION OF DRQ, IRQA AT U4-38 WILL BE SET LOW (IRQA REFLECTS THE STATUS OF THE BIT SET BY THE POSITIVE TRANSITION AT INPUT CA2(U4-39)). THE IRQA OUTPUT IS USED TO DRIVE THE K INPUT FOR READ ENABLE FLIP-FLOP U15. AS LONG AS IRQA REMAINS ACTIVE LOW U15 WILL NOT BE ALLOWED TO RESET. U15 SETTING CAUSES A BYTE OF DATA FROM THE FLOPPY DISC TO BE PLACED ON THE DAL LINES (U11-7,14). WHEN THE PROCESSOR DETECTS CRA BIT 6 SET IT CAN THEN READ THE BYTE OF DATA ON THE DAL LINES THROUGH THE B-PORT DATA REGISTER. AFTER THE PROCESSOR HAS READ THE DATA FROM THE B-PORT THE FLAG IN THE A-PORT CONTROL REGISTER IS CLEARED BY READING THE A-PORT DATA REGISTER. READING THE A-PORT DATA REGISTER ALSO DEACTIVATES IRQA. THIS ALLOWS U15 TO RESET THEREBY PREPARING THE FLOPPY DISC CHIP FOR THE NEXT BYTE OF DATA FROM THE DISC.

HEAD LOAD TIMING

HEAD LOAD TIME OF THE S.A. 400 MINIFLOPPY IS APPROXIMATELY 75 MILLISECONDS. THE 9602 ONESHOT (U14) PROVIDES THE DELAY SIGNAL REQUIRED FOR PROPER OPERATION OF THE FD1771B-01. THE TIME DELAY GENERATED PREVENTS THE FLOPPY DISC CONTROLLER FROM READING OR WRITING BEFORE THE HEAD HAS HAD TIME TO SETTLE.

DISC INTERFACE SIGNALS

DISC SELECT

DURING OPERATION ONE OF THREE DISCS MAY BE SELECTED AT ANY ONE TIME. DISC SELECT IS CONTROLLED BY PIA A-PORT BITS 3, 4 AND 5. PA6 PROGRAMMED TO A '1' SELECTS DISC 0. PA4 PROGRAMMED TO A '1' SELECTS DISC 1 AND PA5 PROGRAMMED TO A '1' SELECTS DISC 2. THE PIA DISC SELECT LINES ARE BUFFERED BY THE 7438 NAND BUFFER LOCATED AT U3. U3 PROVIDES THE REQUIRED DRIVE CAPABILITY NEEDED TO DRIVE THE DISC INTERFACE BUSS. IN ORDER FOR A DISC TO BE SELECTED BOTH HEAD LOAD FROM THE FDC AND ONE OF THE DISC SELECT BITS FROM THE PIA MUST BE ACTIVE. HEAD LOAD FROM THE FD1771B-01 IS BUFFERED BY BUFFER-INVERTER U9(1,2) AS THE FDC OUTPUTS WILL DRIVE ONLY ONE NORMAL TTL LOAD.

MOTOR ON

THE MOTOR ON FUNCTION HAS BEEN MODIFIED FROM THE ORIGINAL CONTROLLER. THE MOTOR IS NOW TURNED ON AS SOON AS THE DISC IS SELECTED AND WILL STAY ON AS LONG AS THE DISC SYSTEM IS ACCESSED. U10 IS WIRED AS A RETRIGGERABLE ONE-SHOT AND HAS A PERIOD OF APPROXIMATELY 30 SECONDS. AFTER THE LAST HEAD LOAD, U9-2 GOES HIGH WHICH REVERSE BIASES D1 ALLOWING THE 555 TIMER TO TIME OUT. U3-3 IS A BUFFERED OUTPUT USED TO DRIVE THE MON- LINE OF THE SA400 DRIVE.

ONE-SHOT U14 IS USED TO PROVIDE A MOTOR START DELAY AND A HEAD LOAD DELAY. THE MOTOR START DELAY IS DISABLED BY U10-3 AFTER THE MOTOR IS STARTED. THIS ALLOWS FASTER ACCESS TO THE DISC.

WRITE DATA

THE WRITE DATA SIGNAL AT U11-31 IS BUFFERED BY U2-1. WRITE DATA ON THE DISC INTERFACE BUSS IS NEGATIVE TRUE DATA.

WRITE GATE

THE WRITE GATE SIGNAL AT U11-30 IS BUFFERED BY U2-4. WRITE GATE ALONG WITH WRITE DATA CONTROLS WRITING OF DATA TO THE SELECTED DISC.

STEP

THE STEP PULSE AT U11-15 IS BUFFERED TO THE DISC INTERFACE BUSS BY U2-9. THE STEP OUTPUT PROVIDES THE STEP INSTRUCTION TO THE DISC AT A CONTROLLED RATE. THE STEP RATE IS PROGRAMMED BY THE USER. FOR THE S.A. 400 THE STEP RATE SHOULD BE PROGRAMMED TO 40 MSEC PER STEP. FOR ADDITIONAL INFORMATION ON STEP RATES SEE THE WESTERN DIGITAL FD1771B-01 PRODUCT GUIDE.

DIRECTION

THE DIRECTION OUTPUT OF THE FD1771B-01 (U11-16) IS BUFFERED BY U2-12. FOR STEP-IN (TOWARDS THE DISC HUB) THE DIRECTION LINE WILL BE HIGH. FOR STEP-OUT THE DIRECTION LINE WILL BE LOW (THIS LEVEL WILL BE REVERSED ON THE BUSS).

TRACK 00

THE TRACK 00 STATUS OF THE SELECTED DISC IS BUFFERED BY U1-2 AND IS ANDDED TO FKTR00-. THIS SIGNAL IS GENERATED BY A ONE-SHOT WHICH IS TRIGGERED BY THE POWER-ON/RESET PULSE GENERATED BY U21-7. THIS SIGNAL "FAKES" THE WD1771-1 INTO THINKING IT IS ON TRACK 00. THIS ALLOWS THE SYSTEM TO RESPOND FASTER AFTER A RESET.

WRITE PROTECT

WRITE PROTECT IS BUFFERED BY U1-5. RESISTOR R5 PROVIDES THE REQUIRED PULLUP. THE WRITE PROTECT LINE REFLECTS THE STATUS OF THE CURRENTLY ACTIVE DISC. IF THE WRITE PROTECT HOLE IN THE DISC IS COVERED THE WRITE PROTECT LINE WILL BE LOW. THE BUFFERED WRITE PROTECT LINE U1-6 DRIVES U11-36. BEFORE DOING ANY WRITE OPERATIONS THE WRITE PROTECT LINE IS SAMPLED. IF THE LINE IS LOW THE WRITE OPERATIONS WILL BE ABORTED BY THE CONTROLLER CHIP.

READ DATA

READ DATA- IS BUFFERED BY NAND GATE U19-(4,5). IT IS THEN SENT THROUGH A ONE-SHOT TO SHAPE THE SIGNAL. FROM HERE THERE ARE TWO OPTIONS: OPTION 1) IS TO USE THE EXTERNAL DATA SEPARATOR, AND OPTION 2) IS TO USE THE DATA SEPARATOR INTERNAL TO THE FD1771-1. THE FDC BOARD IS CONFIGURED TO OPERATE WITH THE EXTERNAL DATA SEPARATOR. THE INTERNAL SEPARATOR MAY BE SELECTED BY CUTTING THE TRACES BETWEEN PADS B,C, AND D AND INSERTING JUMPERS TO THE ALTERNATE PADS. THE DIFFERENCE BETWEEN THE TWO SEPARATORS IS ONE OF RESOLUTION; THE EXTERNAL SEPARATOR IS BETTER AT REJECTING JITTER FROM AN SA400, AND THUS IT IS RECOMMENDED THAT THE EXTERNAL DATA SEPARATOR BE USED.

THE EXTERNAL DATA SEPARATOR CONSISTS OF IC'S U8, U9, U12, U18, U19, AND U20. THE SEPARATOR WORKS BY GENERATING "WINDOWS" THROUGH WHICH DATA AND CLOCK PULSES ARE GATED FROM READ DATA- TO THE FD1771-1. THE SYNCHRONIZATION OF THE SEPARATOR TO THE INCOMING DATA IS DONE BY RETRIGGERABLE ONE-SHOTS U8, U18, ASSOCIATED GATES, AND FLIPFLOPS.

INDEX PULSE

THE INDEX PULSE IS BUFFERED BY AND GATE U1-13. PULLUP IS PROVIDED BY RESISTOR R6. THE BUFFERED INDEX PULSE SIGNAL AT U11-11 DRIVES U11-35. THIS SIGNAL PROVIDES SYCHRONIZATION INFORMATION FOR THE FLOPPY DISC CHIP.

PREVENTATIVE MAINTENANCE

ACCORDING TO SHUGART ASSOCIATES THERE IS NO PREVENTATIVE MAINTENACE REQUIRED FOR THE S.A. 400 MINIFLOPPY. IF ADDITIONAL INFORMATION IS DESIRED A COPY OF THE SHUGART SERVICE MANUAL MAY BE PURCHASED FROM SMOKE SIGNAL BROADCASTING.

THERE ARE NO ADJUSTMENTS REQUIRED ON THE SSB MINIFLOPPY INTERFACE.

COOLING REQUIREMENTS

THE BFD-68 DISC INTERFACE HAS NO SPECIAL COOLING REQUIREMENTS, OTHER THAN PROVIDING AIR SPACE ON ALL FOUR SIDES OF THE CABINET. SHOULD THE USER DECIDE TO ADD A FAN, ONE MAY BE ORDERED FROM SMOKE SIGNAL BROADCASTING OR THE UNIT MAY BE SENT IN FOR MODIFICATION. CAUTION: 120 VOLTS IS PRESENT INSIDE THE CABINET. REMOVE ALL POWER TO THE UNIT BEFORE OPENING THE CABINET AND INSTALLING A FAN.

INSTALLING ADDITIONAL DRIVES

ADDITIONAL SHUGART SA400 DRIVES MAY BE INSTALLED IN THE FIELD. TO INSTALL A SECOND OR THIRD DRIVE, PROCEED AS FOLLOWS:

- 1) LOCATE THE DRIVE SELECT JUMPERS LOCATED IN A DIP SOCKET ON THE TOP CORNER OF THE BOARD ON THE SA400 DRIVE.
- 2) THE JUMPERS ARE CUT AS SHOWN IN THE TABLE BELOW:

DRIVE	CUT	REMOVE
0	MX, DS2, DS3	
1	MX, DS1, DS3	RESISTOR PACK 760-3-R150 OHM
2	MX, DS1, DS2	RESISTOR PACK 760-3-R150 OHM

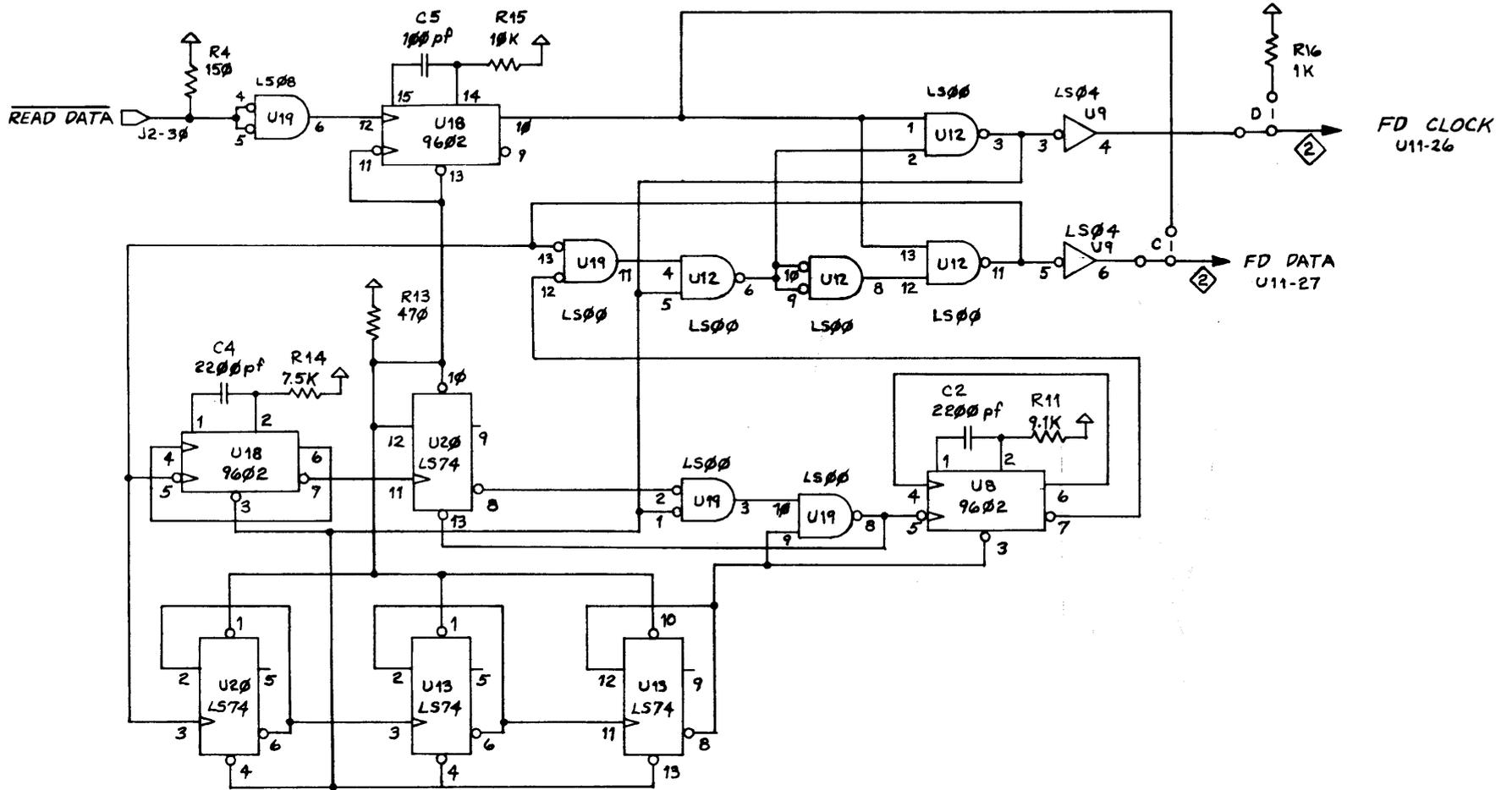
NOTE: THE RESISTOR PACK IS REMOVED FROM ALL DRIVES EXCEPT THE DRIVE WHICH IS ON THE END OF THE RIBBON CABLE CONNECTING TO THE CONTROLLER (NORMALLY THIS IS DRIVE ZERO).

DISKETTE REQUIREMENTS

THE SMOKE SIGNAL BROADCASTING BFD-68 USES THE STANDARD SIZE MINIFLOPPY MEDIA WITH ONE INDEX HOLE. FOR MAXIMUM FLEXIBILITY IN ADAPTING OUR SYSTEM TO SPECIAL USER REQUIREMENTS, WE USE A SOFT-SECTORED DISC FORMAT. THUS, DISKETTES DESIGNED FOR THE SPECIALIZED REQUIREMENTS OF HARD-SECTORED SYSTEMS SUCH AS THE NORTHSTAR WHICH USE MULTIPLE INDEX HOLES WILL NOT WORK WITH THE BFD-68. IF YOU INADVERTENTLY TRY TO FORMAT A MULTIPLE INDEX HOLE DISKETTE, THE FORMATTING PROGRAM WILL REPORT A VERY LARGE NUMBER OF "BAD SECTORS".

DELAY ON POWER ON

THERE IS A DELAY OF SEVERAL SECONDS WHEN FIRST BOOTING THE SYSTEM AFTER APPLYING POWER TO THE HOST COMPUTER ON A TWO OR THREE DRIVE SYSTEM. THIS IS A FUNCTION OF THE LOGIC INTERFACE TO THE CONTROLLER CHIP AND OCCURS ONLY ON TWO OR THREE DRIVE SYSTEMS.



CLOCK SEPARATOR LOGIC

SCALE: NONE

APPROVED BY:

DRAWN BY T. KIRVEN

DATE: 13 SEPT. 77

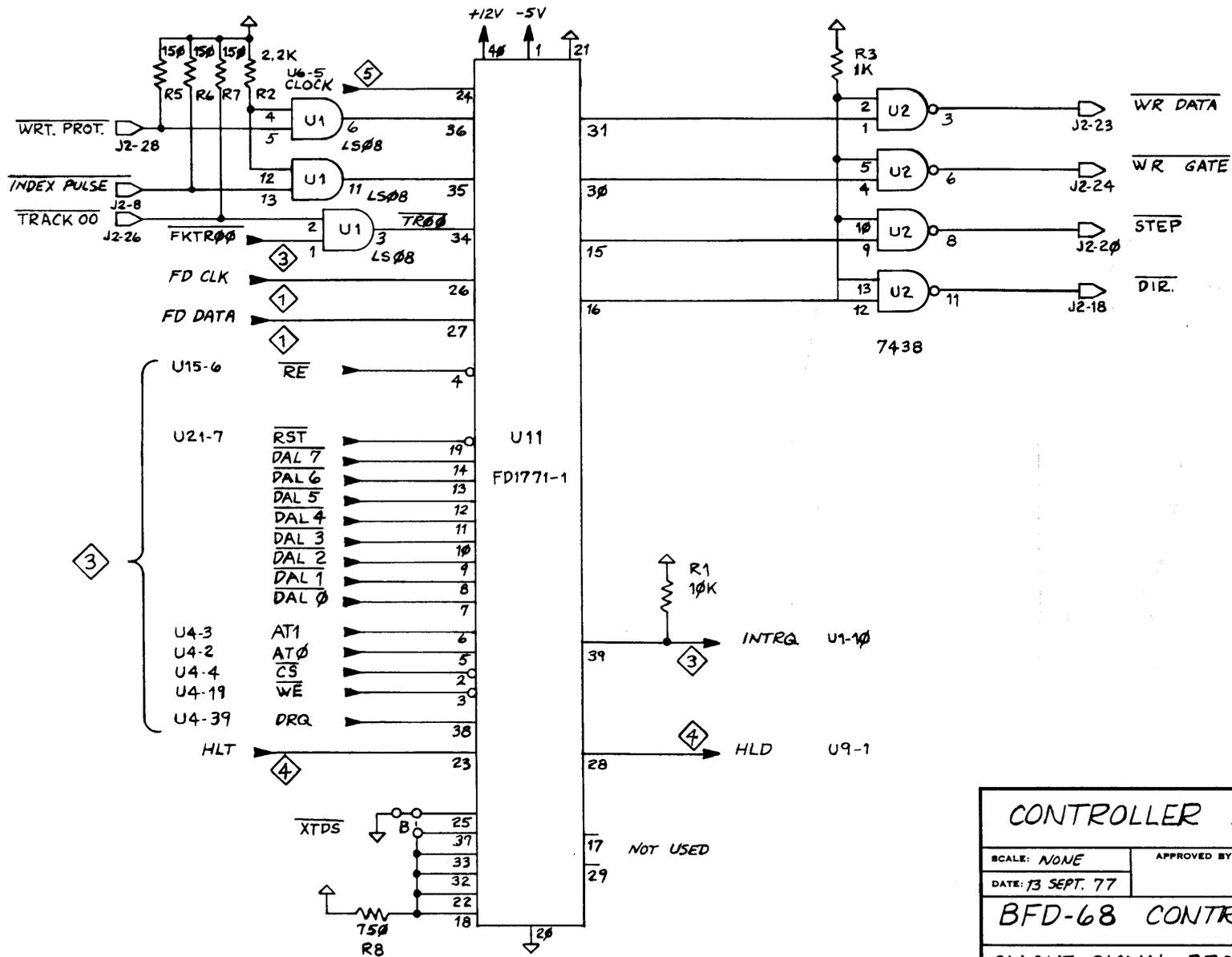
REVISED

BFD-68 CONTROLLER CARD

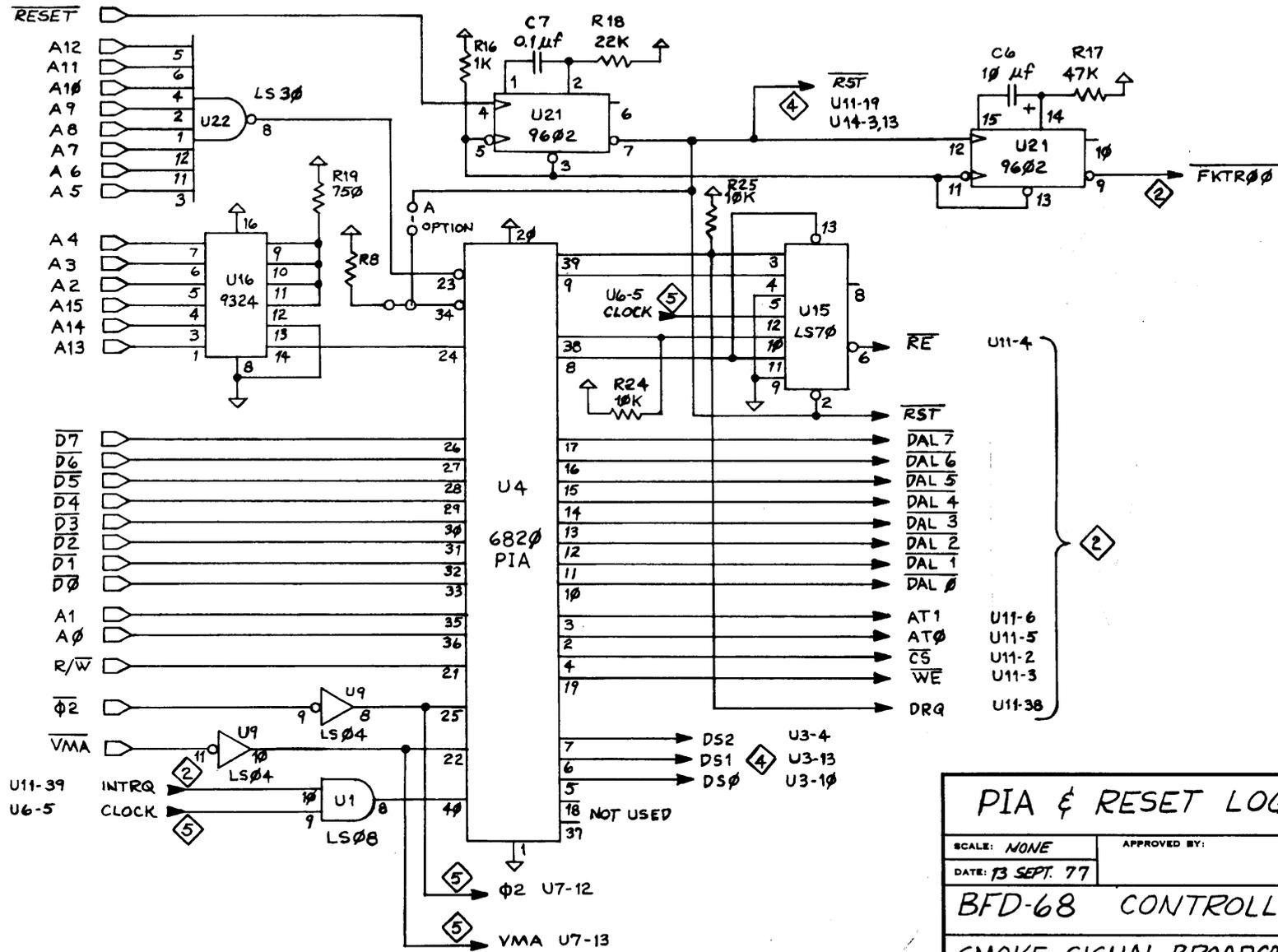
SMOKE SIGNAL BROADCASTING

DRAWING NUMBER

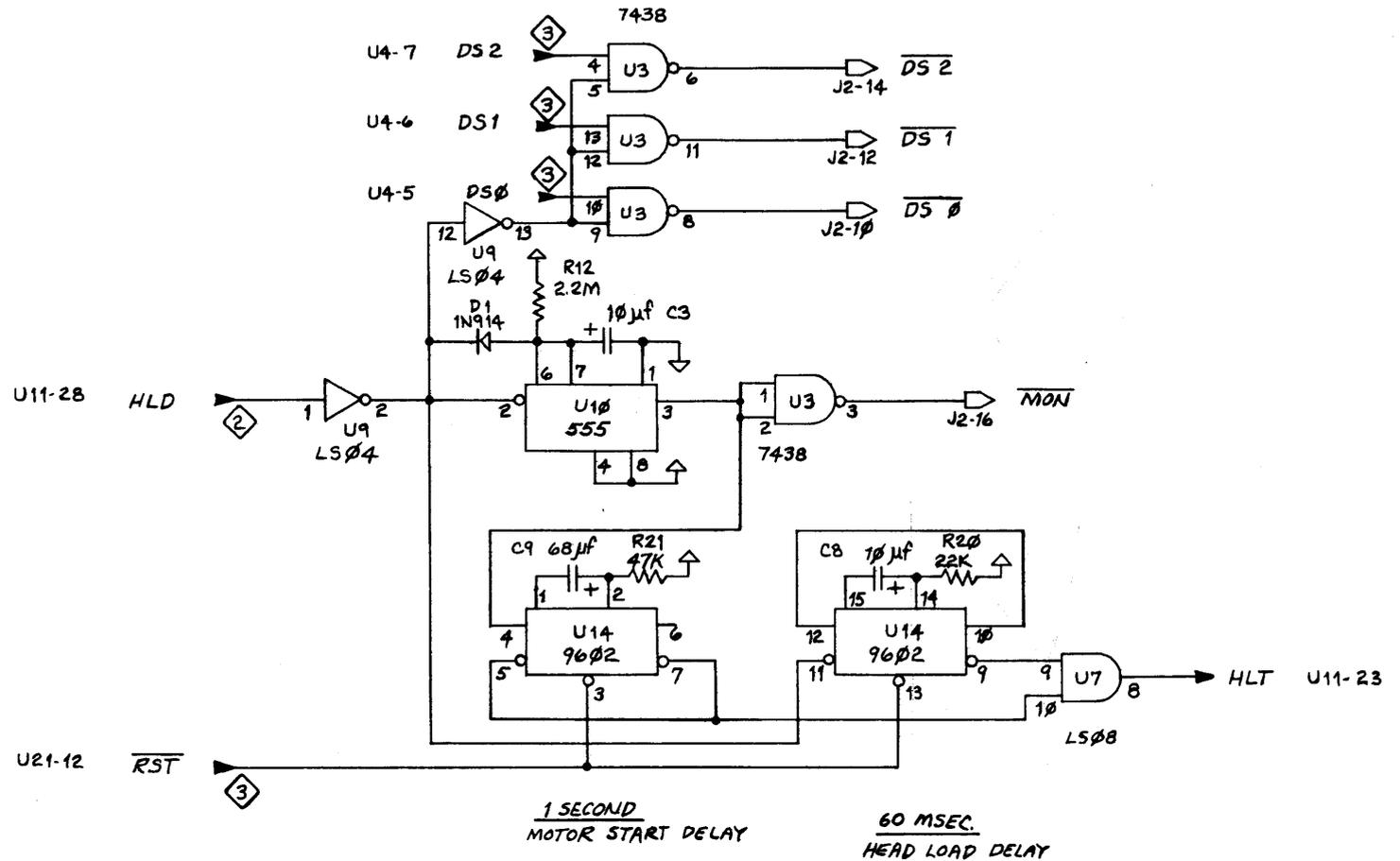
B7738-1



CONTROLLER LOGIC		
SCALE: NONE	APPROVED BY:	DRAWN BY: T. KIRVEN
DATE: 13 SEPT. 77		REVISED
BFD-68 CONTROLLER CARD		
SMOKE SIGNAL BROADCASTING		DRAWING NUMBER: B7738-2



PIA & RESET LOGIC		
SCALE: NONE	APPROVED BY:	DRAWN BY: T. KIRVEN
DATE: 13 SEPT. 77		REVISED
BFD-68 CONTROLLER CARD		
SMOKE SIGNAL BROADCASTING	DRAWING NUMBER	B7738-3



DELAY LOGIC

SCALE: NONE

APPROVED BY:

DRAWN BY T. KIRVEN

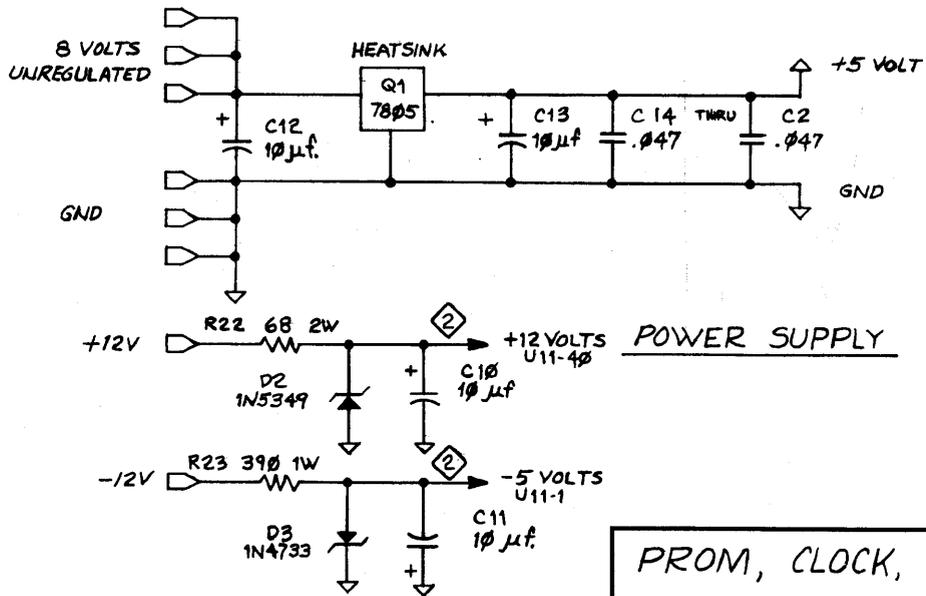
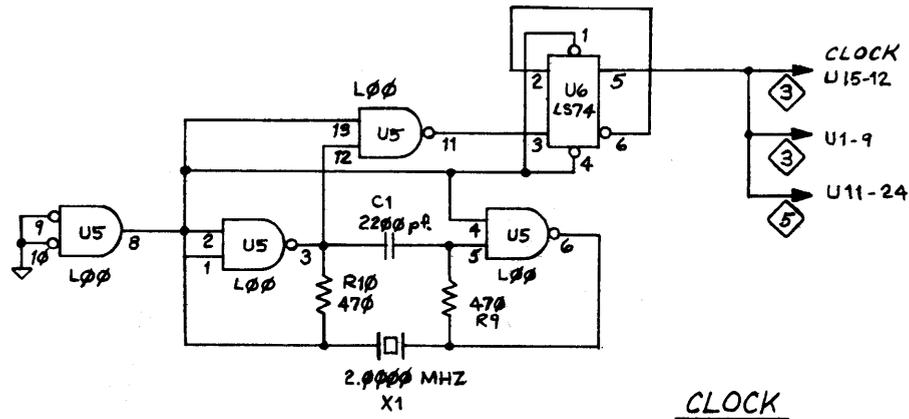
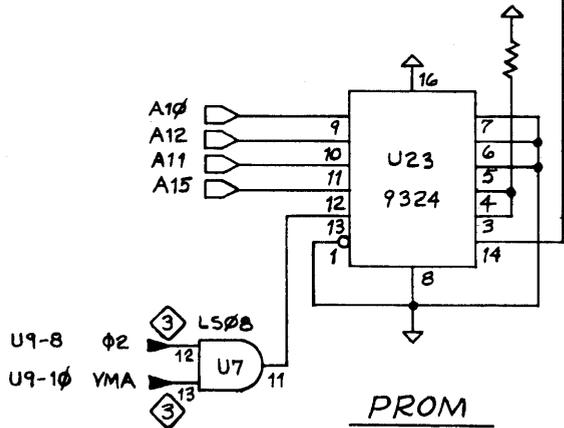
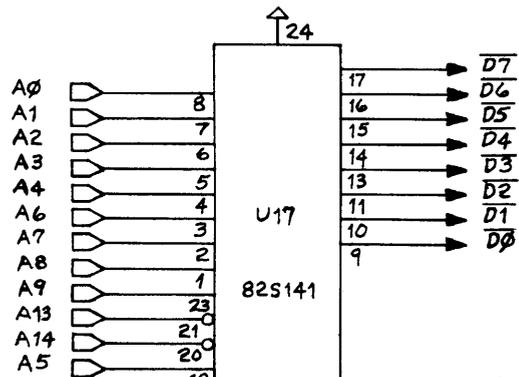
DATE: 13 SEPT. 77

REVISED

BFD-68 CONTROLLER CARD

SMOKE SIGNAL BROADCASTING

DRAWING NUMBER
B7738-4



PROM, CLOCK, POWER SUPPLY

SCALE: NONE	APPROVED BY:	DRAWN BY T. KIRVEN
DATE: 13 SEPT. 77		REVISED
BFD-68 CONTROLLER CARD		
SMOKE SIGNAL BROADCASTING		DRAWING NUMBER B-7738-5