OMTI 5055
MEMORY CONTROLLER
PROGRAMMABLE
DATA SEQUENCER
REFERENCE MANUAL
OCTOBER 4th, 1986

Scientific Micro Systems, Inc.

PRELIMINARY

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CMOS VLSI DEVICE

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SECTION 1

INTRODUCTION

1.1 DESCRIPTION

The OMTI 5055 Memory Controller / Programmable Data Sequencer is a CMOS application specific integrated circuit (ASIC) mounted in an 84-pin plastic leaded chip carrier (PLCC).
The OMTI 5055 manages the flow of data between a serial peripheral interface and a byte-oriented host interface, while also controlling access to an external RAM buffer memory. It is designed to be used with a microprocessor having either a Z8 or 8051 type bus structure for advanced peripheral or controller design.
A typical system configuration showing the use of the chip is illustrated in Figure 1.

The OMTI 5055 is composed of two functional sections :
1) a dual port channel Memory Controller section,
2) a Programmable Data Sequencer Section.

The function of the Memory Controller section is to control the transfer of blocks of data between the Data Sequencer section and an external RAM buffer memory, and between the buffer memory and the host interface.
The Memory Controller has two independently controlled channels to accomplish this:
- channel 0 for the Data Sequencer,
- channel 1 for the host interface.

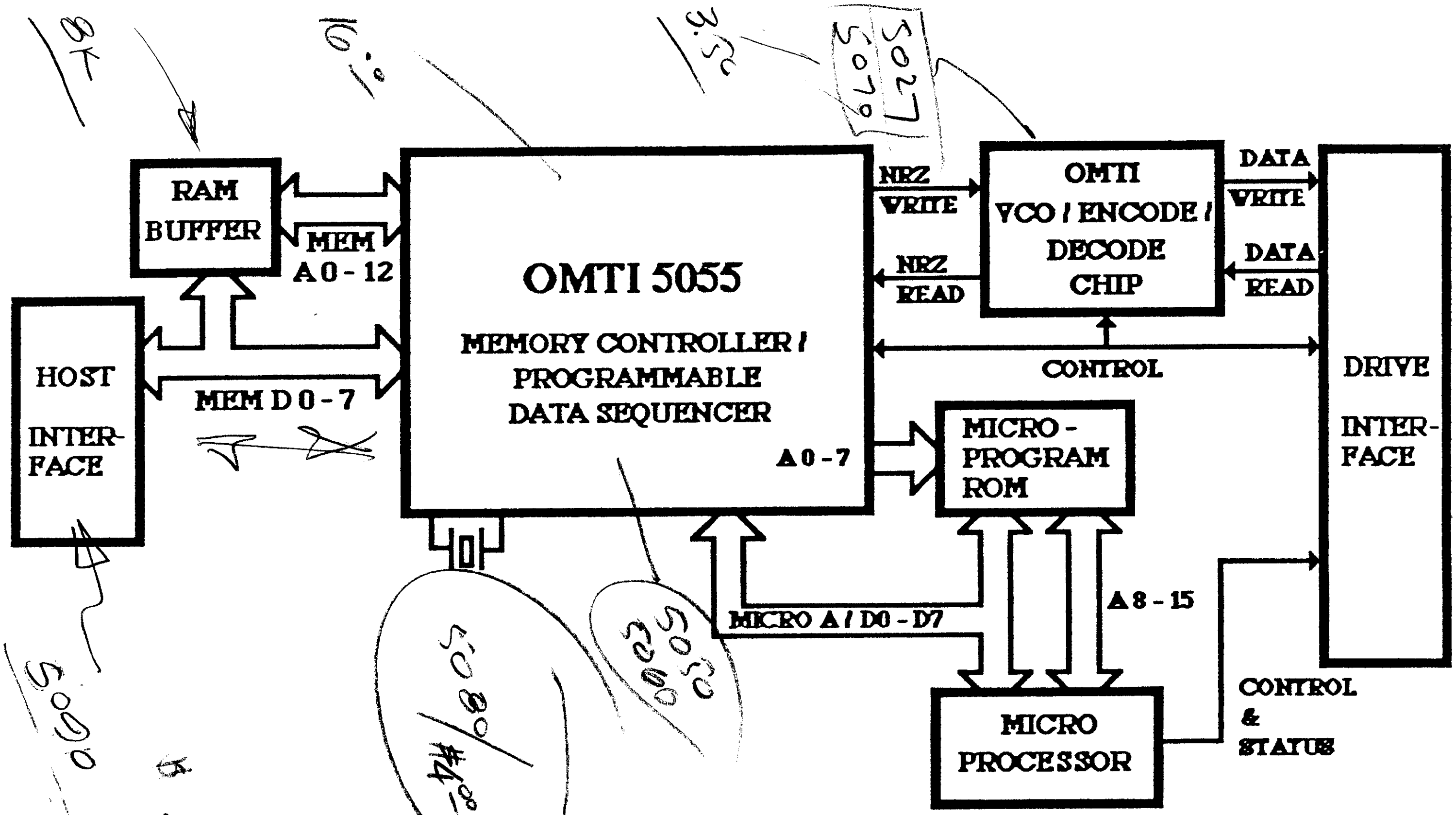
When the Data Sequencer is not using channel 0, this channel may also be used to allow the microprocessor to access the RAM buffer.

A dual-bus structure is used so the disk data transfers and the micro-processor can be operating at the same time without impacting the disk transfer rate or the performance of the micro-processor.

The OMTI 5055 is designed to be used with a RAM buffer, a byte oriented micro-processor, and appropriate drivers and receivers and may be used with :
- either the OMTI SDM-M050 or the OMTI 5070 Encode/Decode/VCO device for MFM data
- or the OMTI SDM-R075 or the OMTI 5027 Encode/Decode/VCO device for 2,7 RLL code

to provide all the functions needed to interface to disk drives using MFM or 2-7 encoded data such as ST-506 or ST-412 and ST-238 compatible drives.

The Programmable Data Sequencer provides the bit-serial data management, format control, error detection, and serialization/de-serialization functions normally associated with data controllers. The chip is designed to be used directly with NRZ (Non-return to Zero) interfaces such as ESDI (Enhanced Standard Drive Interface).
Complete variability and flexibility of disk format is made available by means of an on-chip 64 x 8 RAM.



TYPICAL SYSTEM CONFIGURATION

1.2 FEATURES

ARCHITECTURAL OVERVIEW

Figure 2 illustrates a conceptual block diagram of the Memory Controller / Programmable Data Sequencer. It includes the main internal logic blocks and the interface blocks. Each of these is described below.

The Registers/Control block contains 2 groups of 8-bit internal control registers and associated control logic.
One group of registers is used for the Memory Controller section of the chip, the other group is used for the Programmable Data Sequencer section. Some of these registers may be individually written to by the microprocessor to initialize the parameters that control data transfer, and to initiate the data transfer command. The other registers may be individually read by the microprocessor to obtain status information about command execution.

The Address Generator block outputs addresses to the RAM buffer memory during the transfer of data between buffer & host, and between buffer and disk. The Address Generator automatically increments the address value to point to the next location in the buffer after each byte of data has been transferred.

The Serial/Parallel Data Converter block translates between the serial NRZ form of data used to and from the disk drive, and the byte-parallel form used on the host memory bus. High speed shift registers are used to perform the conversion.

The ECC/CRC block generates and checks the ECC or CRC bytes that are appended to the disk-sector ID and data fields. Bit 6 of WR28 controls whether the CRC polynomial x16+x12+x5+1 or an ECC polynomial is appended to the ID field.

When the floppy format is selected, both ID and Data fields will use the serial implemented polynomial, regardless of WR28.

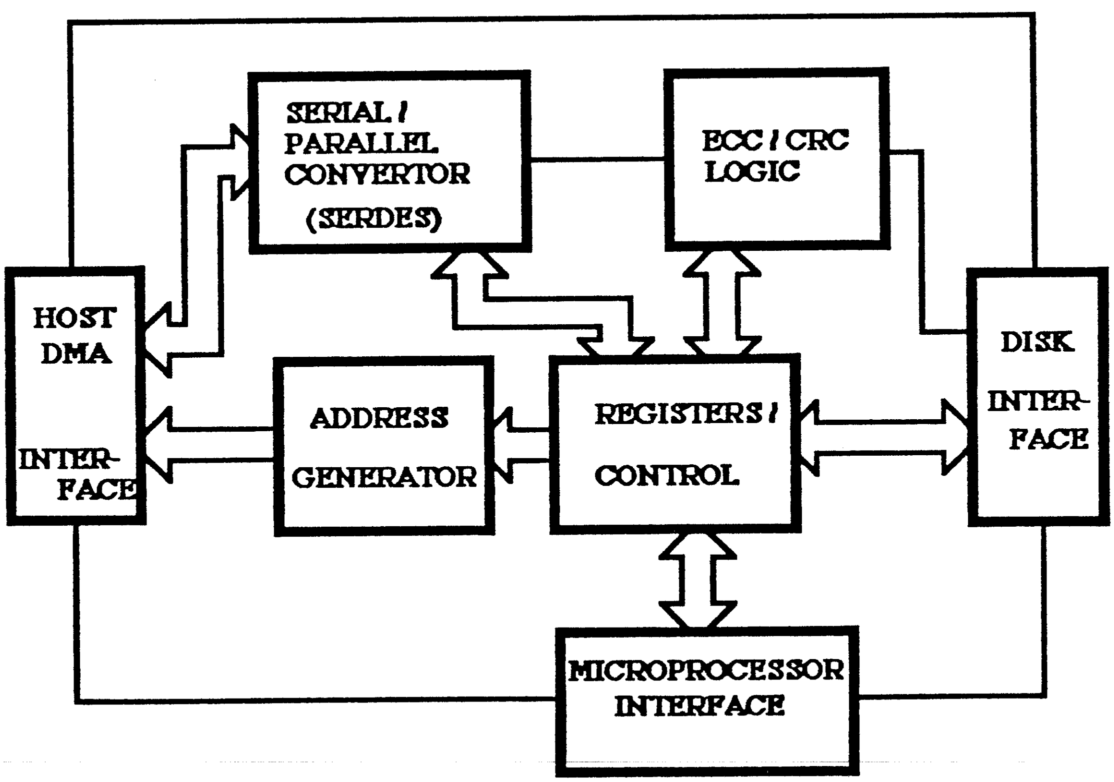
Four CRC and ECC polynomials are available depending on the setting of WR15. The polynomials are as follows:

16-bit: x16+x12+x5+1. (Floppy compatible serial implementation).
32-bit: x32+x24+x18+x15+x14+x11+x8+x7+1.
48-bit: (Proprietary).
56-bit: (Proprietary).

The Host/Buffer Interface consists of an 8-bit data bus, a 13-bit address bus addressing up to 8K bytes external RAM and various control signals.

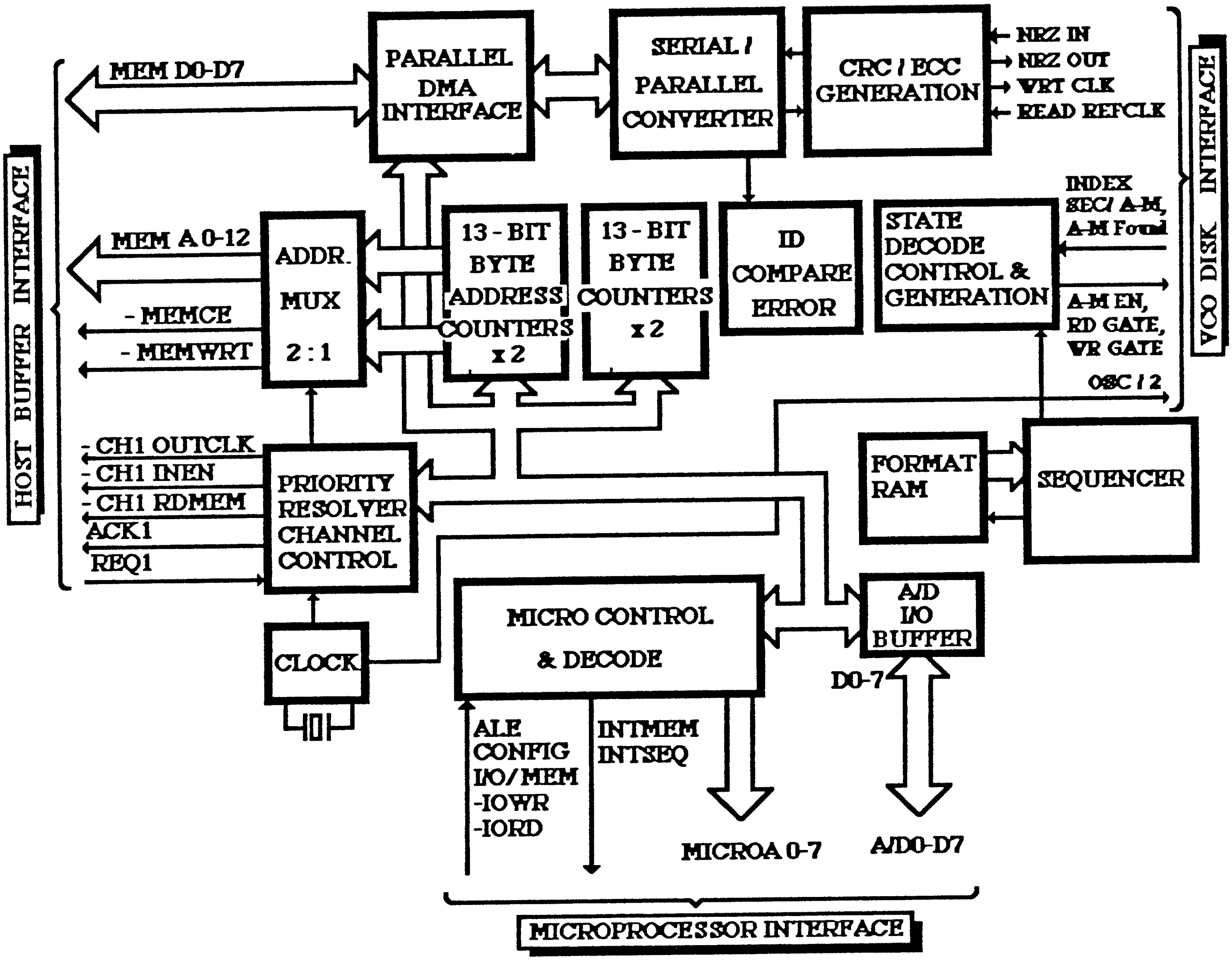
The Microprocessor Interface consists of an 8-bit multiplexed address/data bus, an 8-bit demultiplexed address bus and various microprocessor bus control signals.

The Drive Interface contains the serial data lines to and from the disk (or encode/decode circuitry) and various control signals needed during reading and writing.



CONCEPTUAL BLOCK DIAGRAM

Figure 3 below shows the detailed block diagram of the chip.



FUNCTIONAL BLOCK DIAGRAM

MEMORY CONTROLLER FEATURES

* High Performance Dual-Bus Architecture.

* Two independent DMA channels.

* 5 megabyte device bandwidth.

* 13-bit Addresses and Count registers for each channel.

* Independent mask for channel-end interrupt.

* Configurable SCSI Request / Acknowledge handshake protocol.

* Bus access resolved on channel priority basis.

* Logic to latch and output the low order microprocessor address.

* Programmable Request / Acknowledge and interrupt polarity.

* Programmable auto-count re-initialization.

* Programmable memory access cycle timing (2 to 5 clock cycles).

PROGRAMMABLE DATA SEQUENCER FEATURES

* High-level Instruction Set including :

  - Individual Sector Formatting.

  - Track Formatting.

  - Read ID.

  - Read/Write Long.

  - Read Syndrome.

  - Verify (with data in buffer).

  - Check Data ECC.

  - Check Track Format

* 10 MHz bit rate--up to 10 Mbit/sec Drive Data Transfer Rate.

* Programmable Disk Format.
  - Programmable Sector Size up to 65,536 bytes/sector (by increments of 1 byte).
  - Programmable ID Data and Size.
  - Programmable Gap Sizes and Fill Characters.
  - User-definable Header Flag Byte or Nibble.
  - Selectable 32, 48 or 56 bit ECC Polynomial and ID CRC or ECC or Flexible disk compatible ID and Data Field CRC.
* Hard or Soft Sector Modes.
* NRZ Serial Disk Interface.
* Direct Interface to ESDI Type Drives.
* Multi-sector Transfer capability with Automatic Sector Increment.
* Programmable Automatic ID Retries.
* Surface-mount Plastic 84-pin Leaded Chip Carrier Package.
* Low Power Consumption.
* Strobe Logic to access External Registers on the Micro Bus.
* Logic to Transfer Data between the Micro Bus and Buffer Memory.

1.3 D. C. INFORMATION

1.3.1 Absolute Maximum Ratings:

Parameter	Min	Max	Unit
Supply voltage (Vcc) with respect to GND -	-0.3	+7.0	Volts.
DC Input Voltage (Vin)	-0.3	(Vcc + 0.3)	Volts
DC Output Voltage (Vout)	-0.3	(Vcc + 0.3)	Volts
Input Rise/Fall Times		100	nSec
Clamp Diode Current (Iik, Iok)		+ 5.0	mA
DC Output per pin		4.0	mA
Power Dissipation @70 C, Vcc max.		320	mW.
Storage temperature	-40	+125	Degrees C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

1.3.2 Standard Test Conditions:

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows.

Parameter	Min	Max	Unit
Supply Voltage (Vcc)	+4.75	+5.25	Volts
DC Input / Output Voltage (Vin, Vout)	0.0	Vcc	Volts
Ambient operating temperature	0	+70	Degrees C.
Input Rise/Fall Times (Tr, Tf)		25	nSec
Power Dissipation (Read cycle 2 Mhz, 20 Mhz clock)		125	mW.

1.3.3 D. C. Characteristics :

Parameter	Conditions	Min	Max	Unit
Voh - Output High Voltage	Vdd = min Ioh = Iohmax *	2.4		Volt
Vol - Output Low Voltage	Vdd = min Iol = Iolmax *		0.4	Volt
Vih - Input High Voltage		2.2		Volt
Vil - Input Low Voltage			0.8	Volt
Iih - Output High Current	Vdd = max Vin = Vdd		10.0	uA
Iil - Output Low Current	Vdd = max Vin = Vss		10.0	uA
Iozh - Input Leakage	Vdd = max Vout = Vdd		10.0	uA
Iozl - Output Leakage	Vdd = max Vout = Vdd		10.0	uA
Icc - Quiescent supply current	Vdd = max Ta = 70 C		5.0	mA

1.4 A.C. CHARACTERISTICS

Parameter	Conditions	Min	Max	Unit
Crystal Frequency	Vdd = Min Ta = 70 C		20	Mhz
RD/REF/CLK Frequency			10	Mhz

1.5 OUTPUT DRIVER CHARACTERISTICS

* Output signals have one of three types of drive strengths:

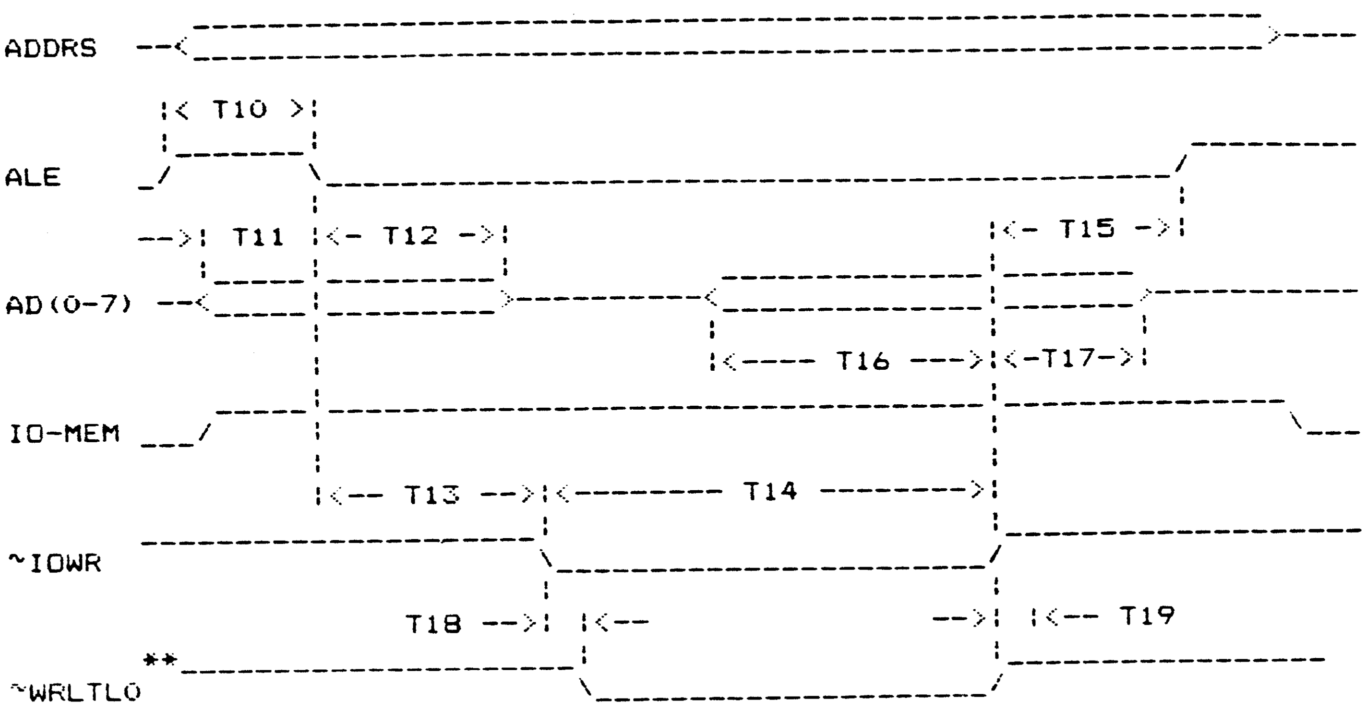
Type 2 : Iolmax = 2.0 mA, Iohmax = -2.0 mA
Type 4 : Iolmax = 4.0 mA, Iohmax = -4.0 mA
Type 8 : Iolmax = 8.0 mA, Iohmax = -8.0 mA

The following Table indicates the Drive Strength for each output driver signal:

Signal	Driver Type	Signal	Driver Type
ACK 1	2	-MEMWRT	2
A/D 0-7	4	MICRO A 0-7	2
AM ENABLE	2	NRZ OUT	2
-CH1NEN	2	OSC	2
-CH1OUTCLK	2	OSC/2	8
-CHQRDMEM	2	OSC/4	2
-GRPRD	2	RDGATE	2
-GRPWT	2	RD/REFCLK	2
INTMEM	2	-ROMCE	2
INTSEQ	2	SEQA 0-4	2
MEMA 0-12	2	WRT CLK	2
-MEMCE	2	WRT GATE	2
-MEMD0-7	4		

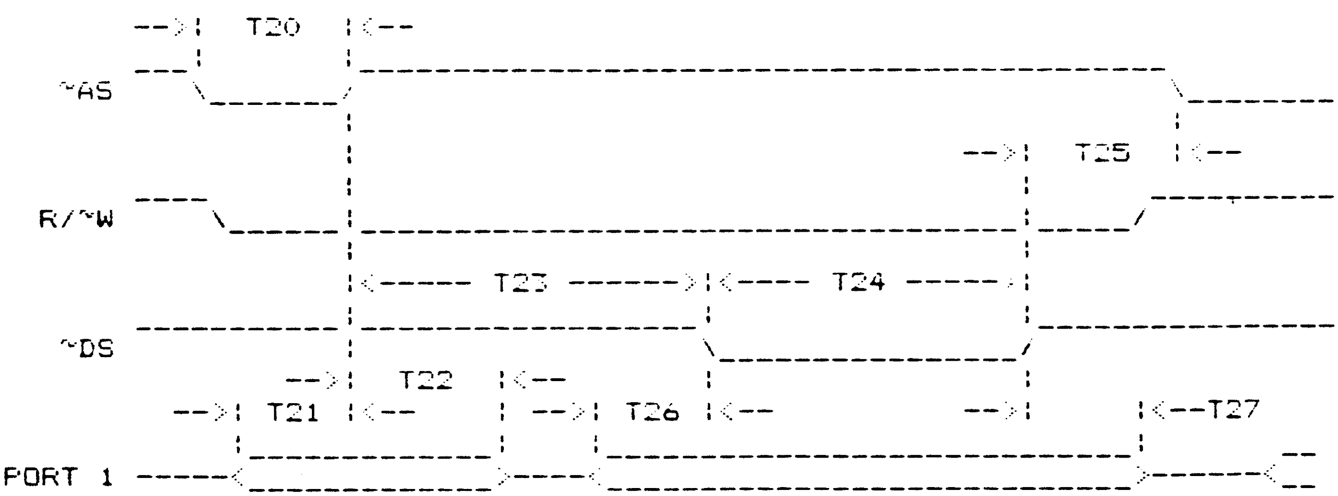
1.6 TIMINGS

1.6.1 Microprocessor WRITE Internal Register Operation, (Configuration = 1, 8051 mode)

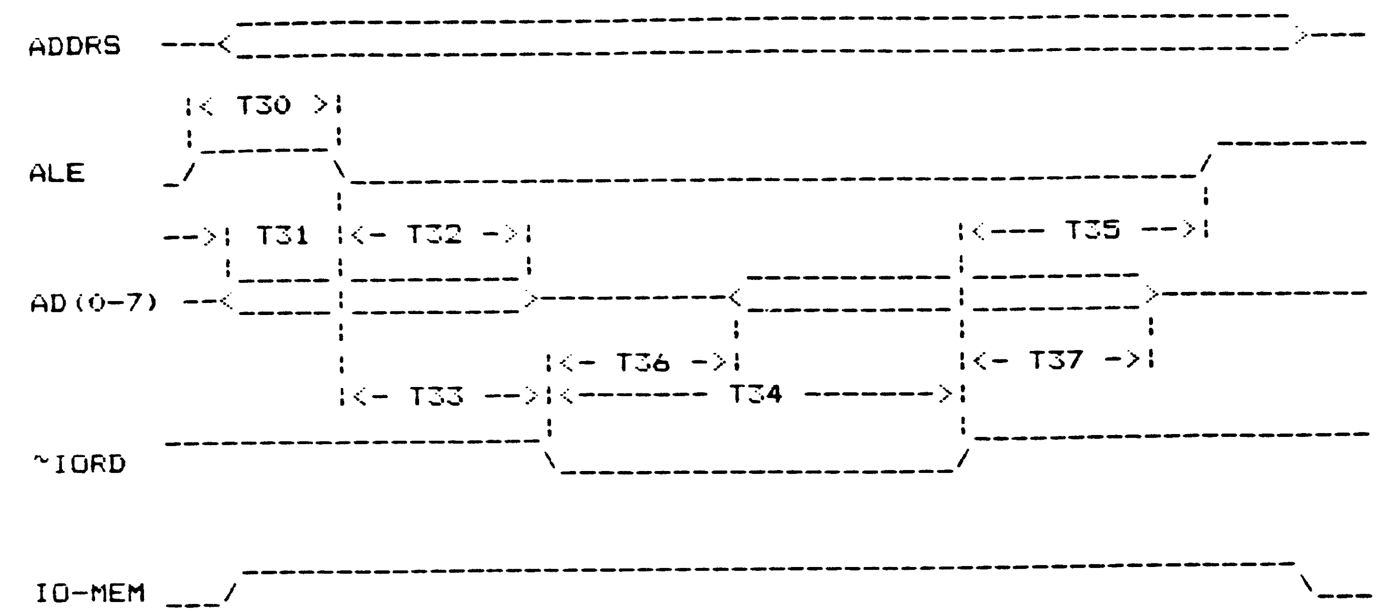


** Used for an external register write operation.

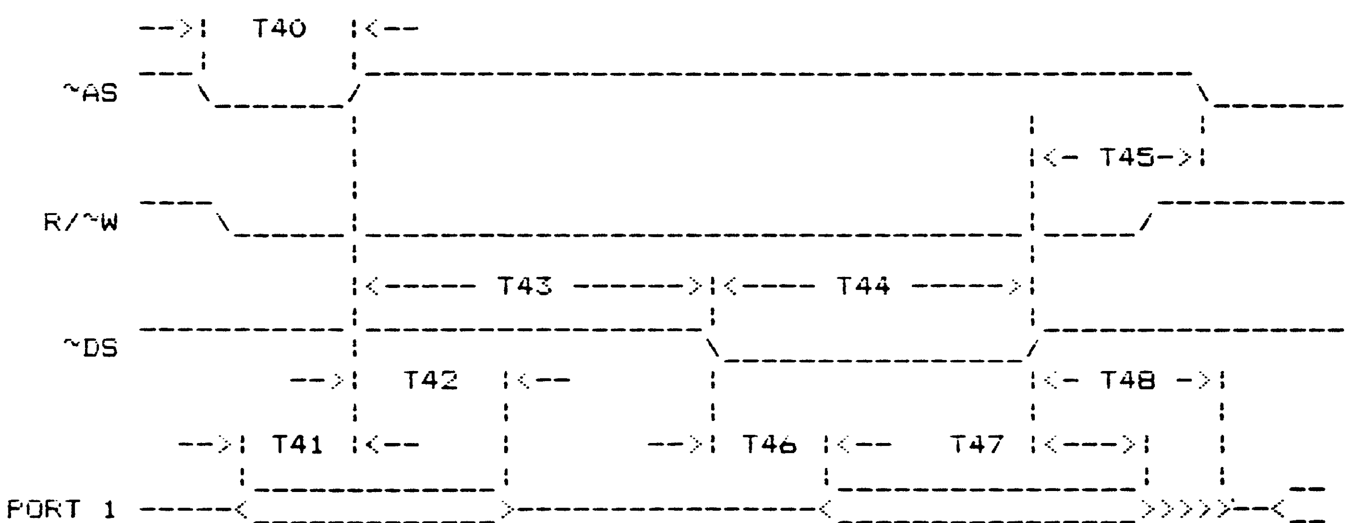
1.6.2 Microprocessor WRITE Internal Register Operation, (Configuration = 0, Z8 mode)



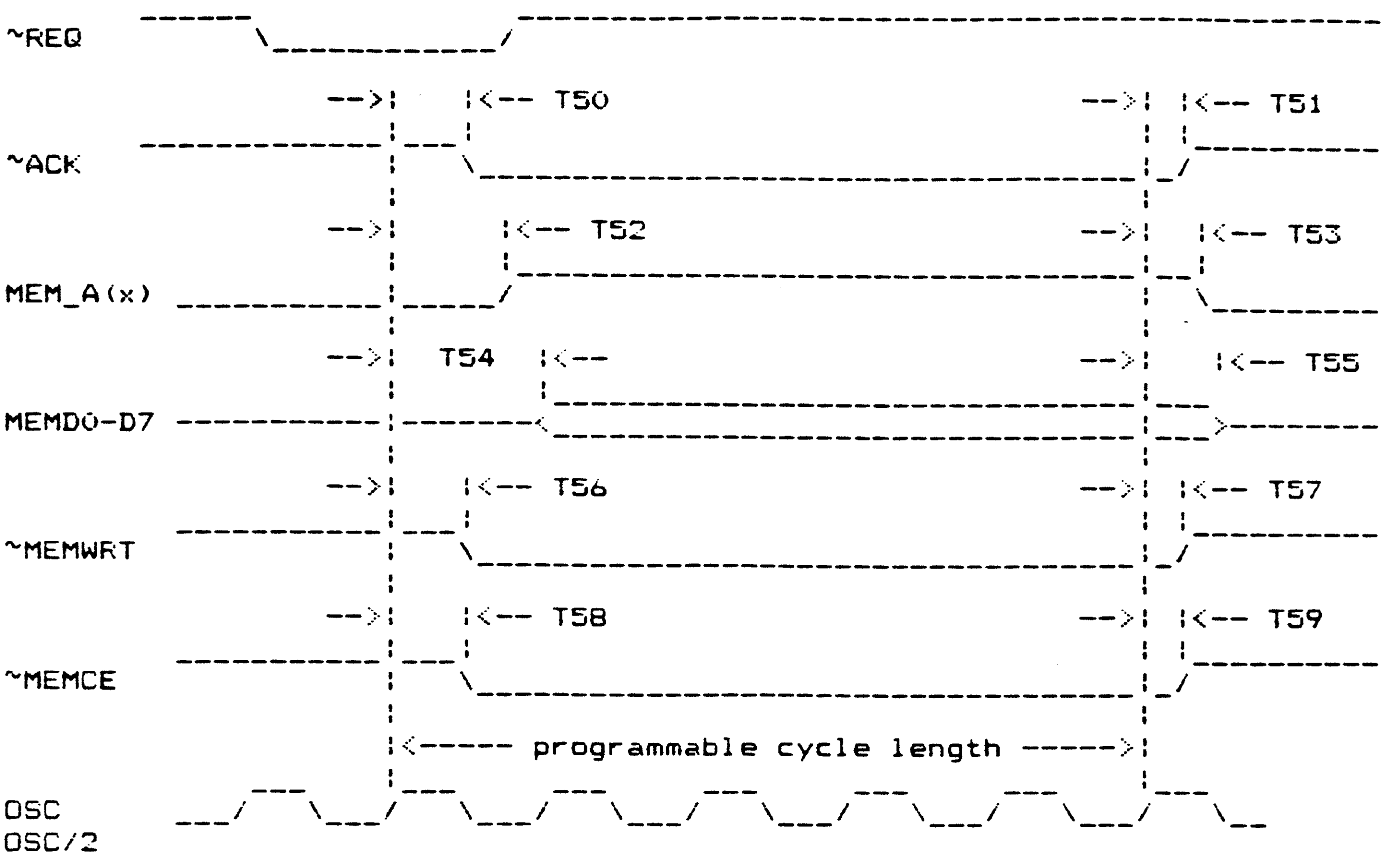
1.6.3 Microprocessor READ Internal Register Operation, (Configuration = 1, 8051 mode)



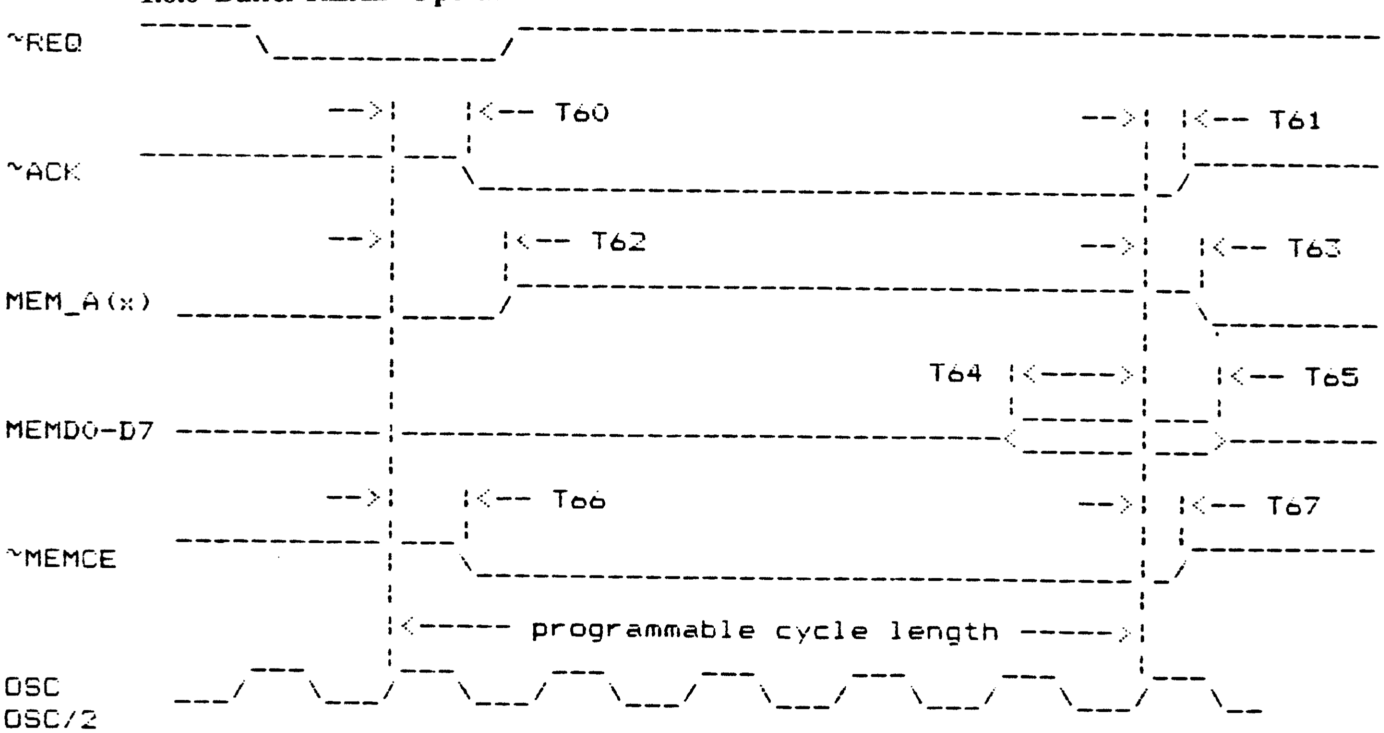
1.6.4 Microprocessor READ Internal Register Operation, (Configuration = 0, Z8 mode)



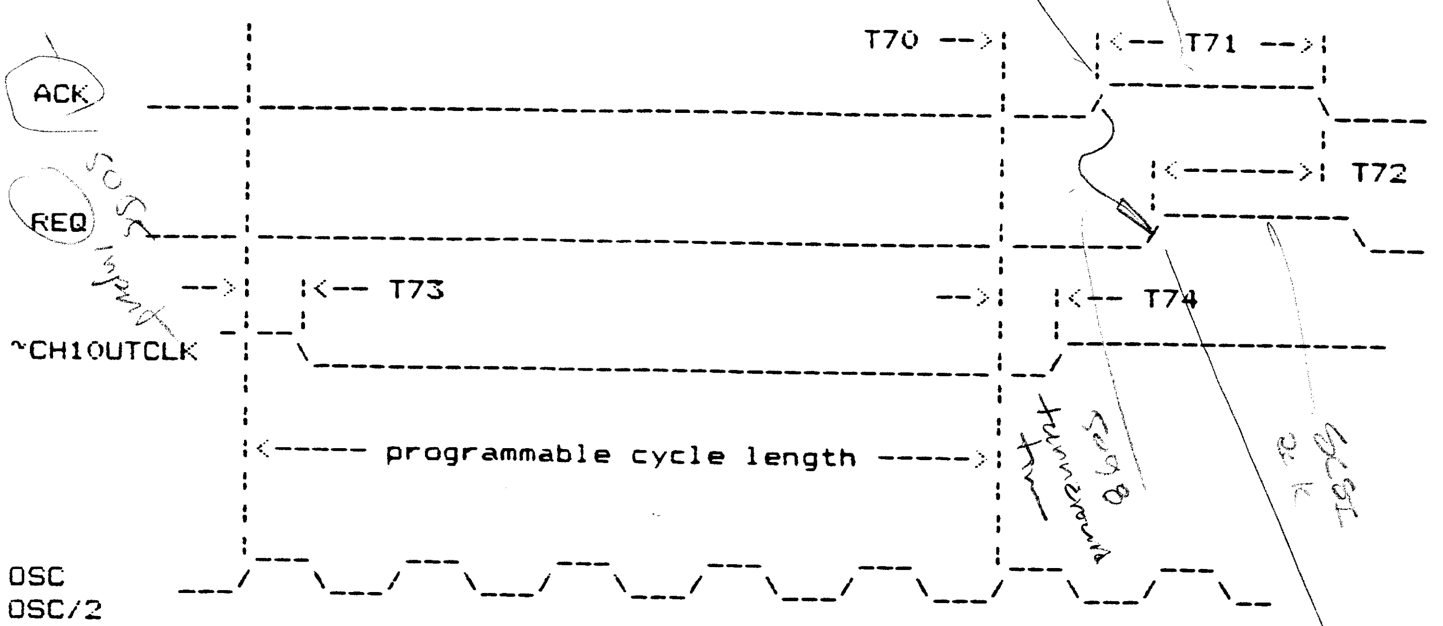
1.6.5 Buffer WRITE Operation



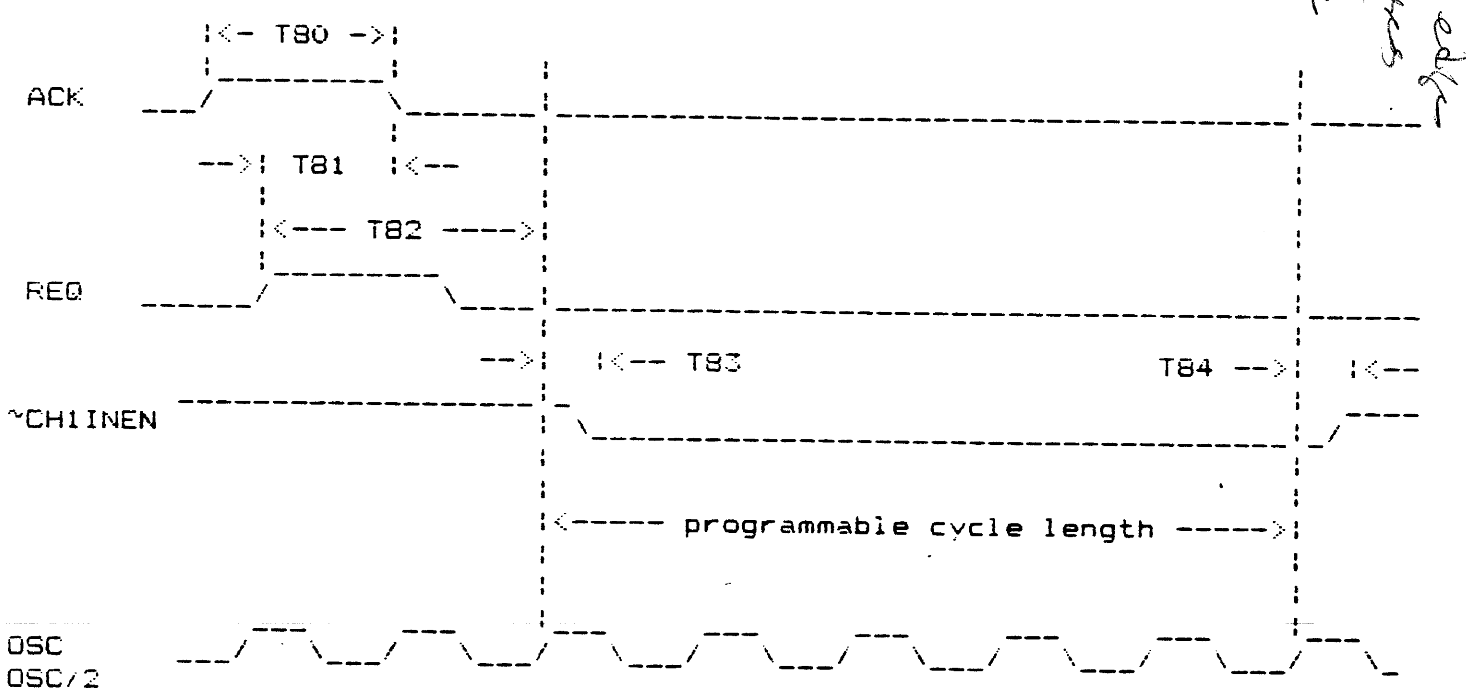
1.6.6 Buffer READ Operation



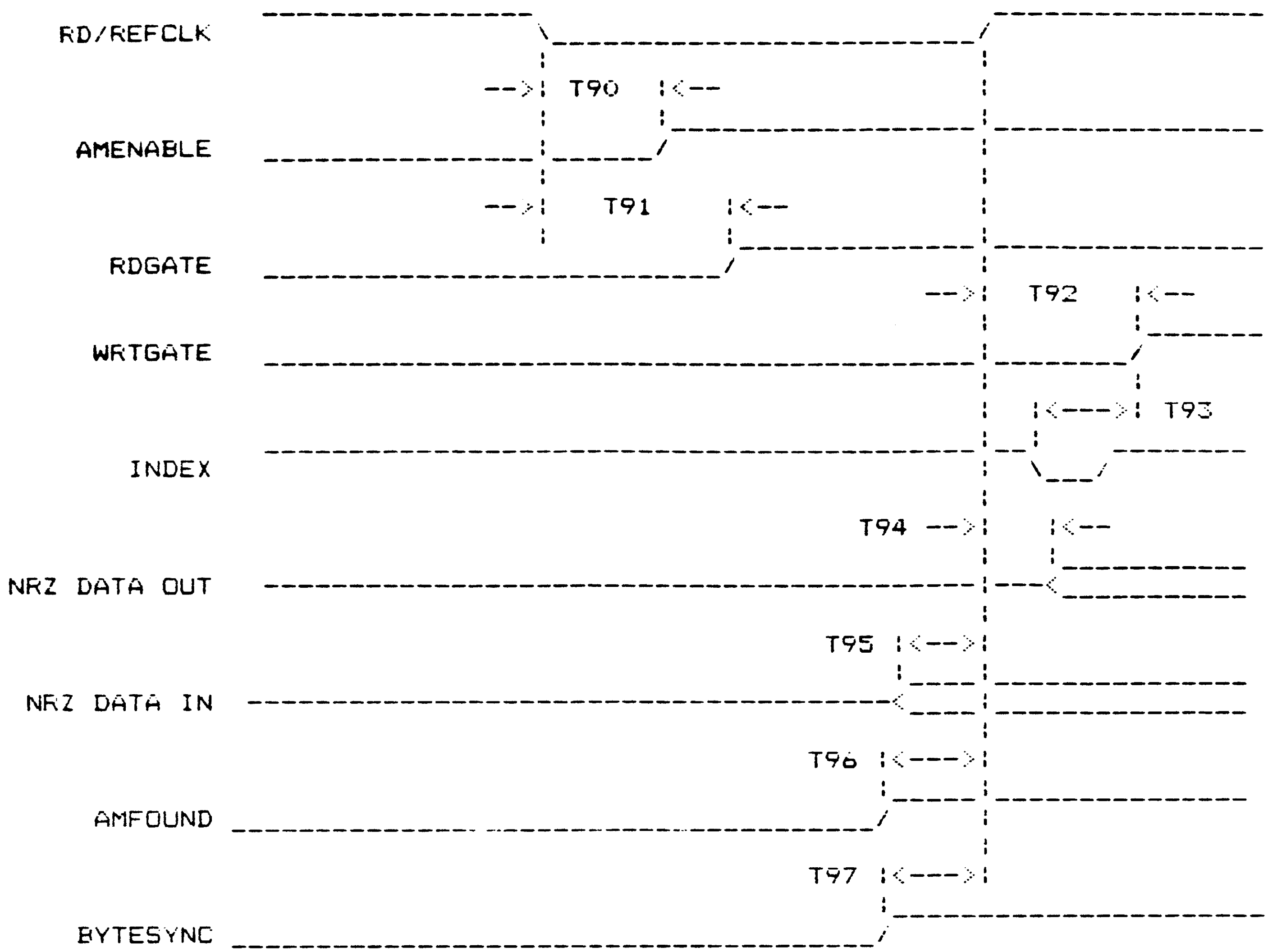
1.6.7 Buffer READ Operation (SCSI Configuration)



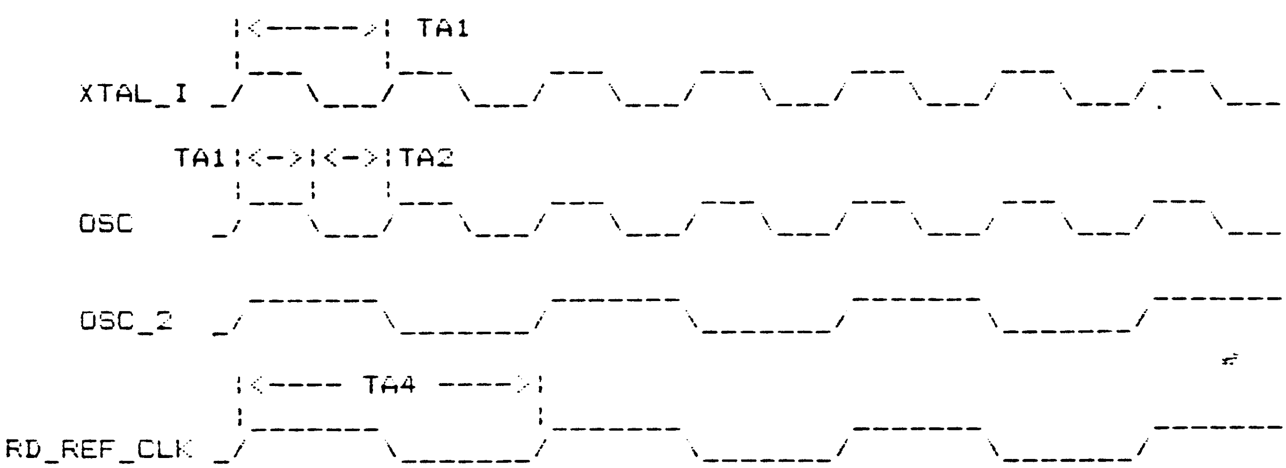
1.6.8 Buffer WRITE Operation (SCSI Configuration)



1.6.9 Control / Data Signal Timing



1.6.10 CLOCK / DATA Limits



TIMING REQUIREMENTS

Symbol	Paragraph	Parameter	Min.	Max.
T10	1.6.1	ALE pulse width.	50	
T11	1.6.1	Address low byte setup time	25	
T12	1.6.1	Address low byte hold time.	25	
T13	1.6.1	ALE low to ~ IOWR.	50	
T14	1.6.1	~ IOWR pulse width.	100	
T15	1.6.1	~ IOWR high to ALE high	40	
T16	1.6.1	Data setup time.	25	
T17	1.6.1	Data hold time.		50
T18	1.6.1	~ IOWR low to ~ WRTL0 low.		20
T19	1.6.1	~ IOWR high to ~ WRTL0 high.		20
T20	1.6.2	~ AS pulse width.	50	
T21	1.6.2	Address low byte setup time	25	
T22	1.6.2	Address low byte hold time.	25	
T23	1.6.2	~ AS high to ~ DS low	50	
T24	1.6.2	~ DS low pulse width	100	
T25	1.6.2	~ DS high to ~ AS low	40	
T26	1.6.2	Data setup to ~ DS (write)	25	
T27	1.6.2	Data hold after ~ DS (write)		50
T30	1.6.3	ALE pulse width	50	
T31	1.6.3	Address low byte setup time	25	
T32	1.6.3	Address low byte hold time.	25	
T33	1.6.3	ALE low to ~ IORD low	50	
T34	1.6.3	~ IORD pulse width	100	
T35	1.6.3	~ IORD low to ALE high	40	
T36	1.6.3	~ IORD low to data valid		50
T37	1.6.3	~ IORD high to data invalid	0	
T38	1.6.3	~ IORD high to data hi-z		35
T40	1.6.4	~ AS pulse width	50	
T41	1.6.4	Address low byte setup time	25	
T42	1.6.4	Address low byte hold time	25	
T43	1.6.4	~ AS high to ~ DS low	50	
T44	1.6.4	~ DS low pulse width	100	
T45	1.6.4	~ DS high to ~ AS low	40	
T46	1.6.4	~ DS low to data valid (read)		50
T47	1.6.4	~ DS high to data invalid (read)	0	
T48	1.6.4	~ DS high to data hi-z (read)		35
T50	1.6.5	~ ACK delay from start of cycle		20
T51	1.6.5	~ ACK delay from end of cycle		25
T52	1.6.5	Valid address from start of cycle		20
T53	1.6.5	Address hold time from end cycle		45
T54	1.6.5	Valid data from start of cycle		40
T55	1.6.5	Data hold time from end of cycle	30	40
T56	1.6.5	~ MEMWRT delay from start of cycle		30
T57	1.6.5	~ MEMWRT delay from end of cycle		20
T58	1.6.5	~ MEMCE delay from start of cycle	30	40
T59	1.6.5	~ MEMCE delay from end of cycle		20

TIMINGS(continued)

Symbol	Paragraph	Parameter	Min.	Max.
T60	1.6.6	~ ACK delay from start of cycle		20
T61	1.6.6	~ ACK delay from end of cycle		25
T62	1.6.6	Valid address from start of cycle		20
T63	1.6.6	Address hold time from end cycle		45
T64	1.6.6	Data setup time from end of cycle	25	
T65	1.6.6	Data hold time from end of cycle	5	
T66	1.6.6	~ MEMCE delay from start of cycle		40
T67	1.6.6	~ MEMCE delay from end of cycle		20
		*Start of a RAM Buffer read/write cycle is defined as the first rising edge of RD/REF CLK (with valid latch setup time) after REQ is valid.		
T70	1.6.7	End of cycle to ACK high		125
T71	1.6.7	ACK pulse width	150	
T72	1.7.7	REQ high to ACK low	100	150
T73	1.6.7	Start of cycle to ~ CH1OUTCLK low		25
T74	1.6.7	End of cycle to ~ CH1OUTCLK high		25
T80	1.6.8	ACK pulse width	150	
T81	1.6.8	REQ high to ACK low	100	150
T82	1.6.8	REQ high to start of cycle	225	
T83	1.6.8	Start of cycle to ~ CH1INEN low		25
T84	1.6.8	End of cycle to ~ CH1INEN high		25
T90	1.6.9	AMENABLE delay from RD/REFCLK		30
T91	1.6.9	RDGATE delay from RD/REFCLK		40
T92	1.6.9	WRTGATE delay from RD/REFCLK		30
T93	1.6.9	WRTGATE delay from INDEX		30
T94	1.6.9	NRZ DATA OUT valid from RD/REFCLK		25
T95	1.6.9	NRZ DATA IN Setup time	20	
T96	1.6.9	AMFOUND setup time	25	
T97	1.6.9	BYTESYNC setup time	20	
TA1	1.6.10	Pulse width from crystal	33	
TA2	1.6.10	OSC output high		55%
TA3	1.6.10	OSC output low	45%	
TA4	1.6.10	RD/REFCLK pulse width	100	

SECTION 2

REGISTERS

There are two groups of registers in the OMTI 5055 :
- one for the Memory Controller section
- and another for the Programmable Data sequencer section.

Each group contains two types of registers :
- writeable control registers (WRxx)
- and readable status registers (RRxx).

The tables below summarize the registers per group, and a description of the bits in each register follows the tables.

2. 1 MEMORY CONTROLLER REGISTERS

CONTROL (WRITE) REGISTERS		*STATUS (READ) REGISTERS*	
Write	**Functions**	**Read**	**Functions**
WR0	**Channel 0 Address 0-7**	**RR0**	**Channel Status**
WR1	**Channel 0 Address 8-12**	**RR1**	Not used
WR2	**Channel 0 Byte Count 0-7**	**RR2**	**Channel 0 Byte Count 0-7**
WR3	**Channel 0 Byte Count 8-12**	**RR3**	**Channel 0 Byte Count 8-12**
WR4	**Channel 1 Address 0-7**	**RR4**	Not used
WR5	**Channel 1 Address 8-12**	**RR5**	Not used
WR6	**Channel 1 Byte Count 0-7**	**RR6**	**Channel 1 Byte Count 0-7**
WR7	**Channel 1 Byte Count 8-12**	**RR7**	**Channel 1 Byte Count 8-12**
WR8	**Channel 0 Control**	**RR8**	Not used
WR9	**Channel 1 Control**	**RR9**	Not used
WR10	**Memory Cycle Timing**	**RR10**	Not used
WR11	**ECC Select**	**RR11**	**Micro-DMA Memory to Group**
WR12	**Group Write Strobe**	**RR12**	**Group Read Strobe**
WR13	**Group Write Strobe**	**RR13**	**Group Read Strobe**
WR14	**Group Write Strobe**	**RR14**	**Group Read Strobe**
WR15	**Group Write Strobe**	**RR15**	**Group Read Strobe**

2.2 PROGRAMMABLE DATA SEQUENCER REGISTERS

CONTROL (WRITE) REGISTERS		*STATUS (READ) REGISTERS*	
Write	**Functions**	**Read**	**Functions**
WR16	Sequencer Command	RR16	Sequencer Status
WR17	Sequencer Loop Count	RR17	Extended Sequencer Status
WR18	Index Time-Out	RR18	Retry Count/State Address
WR19	Sub-Block Count	RR19	Flag Byte
WR20	Cylinder (High Byte)	RR20	Cylinder (High Byte)
WR21	Cylinder (Low Byte)	RR21	Cylinder (Low Byte)
WR22	Head	RR22	Head/Flag
WR23	Sector Number	RR23	Sector Number
WR24	Micro to Memory	RR24	Memory to Micro
WR25	Sequencer Start/Re-Start	RR25	Sequencer Loop Count
WR26	Sequencer Loop State	RR26	Test Register
WR27	Bit Ring Start Count	RR27	Force Index Register
WR28	ECC Control	RR28	Not Used
WR29	Configuration Control	RR29	Not Used
WR30	Seq Value Register & Seq Start	RR30	Seq Value Register & Seq Start
WR31	Seq Count Register & Seq Start	RR31	Seq Count Register & Seq Start

2.3 REGISTER ADDRESS MAP

A/D4	A/D3	A/D2	A/D1	A/D0	WRITE	READ
0	0	0	0	0	WR0	RR0
0	0	0	0	1	WR1	Not Used
0	0	0	1	0	WR2	RR2
0	0	0	1	1	WR3	RR3
0	0	1	0	0	WR4	Not Used
0	0	1	0	1	WR5	Not Used
0	0	1	1	0	WR6	RR6
0	0	1	1	1	WR7	RR7
0	1	0	0	0	WR8	Not Used
0	1	0	0	1	WR9	Not Used
0	1	0	1	0	WR10	Not Used
0	1	0	1	1	WR11	Not Used
0	1	1	0	0	WR12	RR12
0	1	1	0	1	WR13	RR13
0	1	1	1	0	WR14	RR14
0	1	1	1	1	WR15	RR15
1	0	0	0	0	WR16	RR16
1	0	0	0	1	WR17	RR17
1	0	0	1	0	WR18	RR18
1	0	0	1	1	WR19	RR19
1	0	1	0	0	WR20	RR20
1	0	1	0	1	WR21	RR21
1	0	1	1	0	WR22	RR22
1	0	1	1	1	WR23	RR23
1	1	0	0	0	WR24	RR24
1	1	0	0	1	WR25	RR25
1	1	0	1	0	WR26	RR26
1	1	0	1	1	WR27	RR27
1	1	1	0	0	WR28	Not Used
1	1	1	0	1	WR29	Not Used
1	1	1	1	0	WR30	RR30
1	1	1	1	1	WR31	RR31

WR = Write Register. RR = Read Register.

A/D7 through A/D0 are the micro-processor address/data lines. A/D 5 through 7 must be set to zero.

2.4 MEMORY CONTROLLER WRITE REGISTERS

2.4.1 WRITE REGISTER 00, 04: MEMORY ADDRESS 0 through 7

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

The Memory Address 0-7 register specifies the least significant byte of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). This address is automatically incremented after each byte of data is transferred.

2.4.2 WRITE REGISTER 01, 05: MEMORY ADDRESS 8 through 12

Bit	7	6	5	4	3	2	1	0
Byte	00 - 1Fh							

The Memory Address 8-12 register specifies the most significant five bits of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). This address is automatically incremented by overflow of the Memory Address 0-7 register.

2.4.3 WRITE REGISTER 02, 06: BYTE COUNT 0 through 7

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

The Byte Count 0-7 register specifies the least significant byte of the number of transfers to be performed. The byte count is automatically decremented after each transfer.

2.4.4 WRITE REGISTER 03, 07: BYTE COUNT 8 through 12

Bit	7	6	5	4	3	2	1	0
Byte	00 - 1Fh							

The Byte Count 8-12 register specifies the most significant five bits of the number of transfers to be performed. The byte count is automatically decremented by underflow of the Byte Count 0-7 register.

2.4.5 WRITE REGISTER 08 : CHANNEL 0 CONTROL

```
==========================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
==========================================
       |     |     |     |     |     |     |     |
       |     |     |     |     |     |     |     0= Channel Disable
       |     |     |     |     |     |     |     1 = Channel Enable
       |     |     |     |     |     |     |
       |     |     |     |     |     |     0 = Read RAM
       |     |     |     |     |     |     1 = Write RAM
       |     |     |     |     |     |
       |     |     |     |     |     0 = Auto Byte Count Re-Load Disabled
       |     |     |     |     |     1 = Auto Byte Count Re-Load Enabled
       |     |     |     |     |
       |     |     |     |     0 = Interrupt Disable
       |     |     |     |     1 = Interrupt Enable
       |     |     |     |
       |     |     |     0 = Byte Count = 0 Disables Channel
       |     |     |     1 = Channel Always Enabled
       |     |     |
       |------- |------- |---0 = Reserved
```

BIT 0
Bit 0 enables or disables the channel.

BIT 1
Bit 1 specifies the direction of data transfer.
When set, data is transferred from the RAM buffer memory to the Data Sequencer (or to RR24 in a Memory-to-Micro transfer);
When cleared, data is transferred from the Data Sequencer (or from WR24 in a Micro-to-Memory transfer) to the RAM buffer memory.

BIT 2
When bit 2 is set, completion of a block transfer (byte count = 0) is followed by the automatic reloading of the channel's Byte Count register with its value prior to the transfer. This option allows a sequence of records to be transferred, without requiring re-initialization of the channel's Address and Byte Count registers prior to each record's transfer. (For continuous operation, bits 0 and 4 in this register must also be set).

BIT 3
When bit 3 is set, completion of a block transfer (byte count = 0) is followed by an interrupt request being sent to the microprocessor (the INT MEM signal becomes asserted). The microprocessor responds to the interrupt by reading the Channel Status register RR0 or, if bit 4 is set, by issuing another command.

When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the necessity of polling when only a single channel is being used.

BIT 4
When bit 4 is cleared, the channel will automatically be disabled when the byte count becomes equal to zero. To begin another operation on the channel, the enable bit (bit 0) must be reprogrammed by reading the status register.

When bit 4 is set, the channel remains enabled after the byte count equals zero. In this case, interrupts are re-enabled (bit 3 is set) by the microprocessor.

BITS 5, 6 and 7 are reserved.
They must be set to zero.

2.4.6 WRITE REGISTER 09 : CHANNEL 1 CONTROL

```
=============================================
 Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
=============================================
        |     |     |     |     |     |     |     |
        |     |     |     |     |     |     |     0 = Channel Disable
        |     |     |     |     |     |     |     1 = Channel Enable
        |     |     |     |     |     |     |
        |     |     |     |     |     |     0 = Read RAM
        |     |     |     |     |     |     1 = Write RAM
        |     |     |     |     |     |
        |     |     |     |     |     0 = Auto Byte Count Re-Load Disabled
        |     |     |     |     |     1 = Auto Byte Count Re-Load Enabled
        |     |     |     |     |
        |     |     |     |     0 = Interrupt Disable
        |     |     |     |     1 = Interrupt Enable
        |     |     |     |
        |     |     |     0 = Byte Count = 0 Disables Channel
        |     |     |     1 = Channel Always Enabled
        |     |     |
        |     |     0 = Request Low to High Edge
        |     |     1 = Request High to Low Edge
        |     |
        |     0 = Acknowledge Low Strobe
        |     1 = Acknowledge High Strobe
        |
        0 = Channel Req / Ack Protocol
        1 = SCSI Req / Ack Protocol
```

BIT 0
Bit 0 enables or disables the channel.

BIT 1
Bit 1 specifies the direction of data transfer.
When set, data is transferred from the RAM buffer memory to the Host Interface.
When cleared, data is transferred from the Host Interface to the RAM buffer memory.

BIT 2
When bit 2 is set, completion of a block transfer (byte count =- 0) is followed by the automatic reloading of the channel's Byte Count register with its value prior to the transfer. This option allows a sequence of records to be transferred, without requiring re-initialization of the channel's Address and Byte Count registers prior to each record's transfer. (For continuous operation, bits 0 and 4 in this register must also be set.)

BIT 3
When bit 3 is set, completion of a block transfer (byte count = 0) is followed by an interrupt request being sent to the microprocessor (the INT MEM signal becomes asserted). The microprocessor responds to the interrupt by reading the Channel Status register RR0 or, if bit 4 is set, by issuing another command.

When bit 3 is cleared, interrupts from the channel are disabled. This option avoids the necessity of polling when only a single channel is being used.

BIT 4
When bit 4 is cleared, the channel will automatically be disabled when the byte count becomes equal to zero. To begin another operation on the channel, the enable bit (bit 0) must be reprogrammed by reading the status register.

When bit 4 is set, the channel remains enabled after the byte count equals zero. In this case, interrupts are re-enabled (bit 3 is set) by the microprocessor.

BITS 5 and 6
Bits 5 and 6 control the polarity of the request (REQ1) and acknowledge (ACK1) signals, respectively.

BIT 7
When bit 7 is set, the channel will use the SCSI request/acknowledge data transfer handshake protocol.
When bit 7 is cleared, the channel will use the standard request/acknowledge protocol.

2.4.7 WRITE REGISTER 10 : MEMORY CYCLE TIMING

```
============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
============================================
       |     |     |     |     |     |     |     |
       |     |     |     |     |     |     0     0 = 2 Clock Cycles
       |     |     |     |     |     |     0     1 = 3 Clock Cycles
       |     |     |     |     |     |     1     0 = 4 Clock Cycles
       |     |     |     |     |     |     1     1 = 5 Clock Cycles
       |     |     |     |     |     |
       |     |     |     |     |     0 = Interrupt  Active Low
       |     |     |     |     |     1 = Interrupt  Active High
       |     |     |     |     |
       |     |     |     |     0 = OSC/2 to Memory Control Section
       |     |     |     |     1 = OSC to Memory Control Section
       |     |     |     |
       |     |     |     0 = Index : Active High
       |     |     |     1 = Index : Active Low
       |     |     |
       |     |     0 = Sector / AM Found : Active High
       |     |     1 = Sector / AM Found : Active low
       |     |
       |     0 = Data Field Sync TimeOut : 512 bits
       |     1 = Data Field Sync TimeOut : 32 bits
       |
       0 = Reserved
```

BITS 0 and 1
Bits 0 and 1 specify the number of clock cycles used in the memory cycle for each word transferred. This option is provided to allow a range of RAM memory speeds to be used.

BIT 2
Bit 2 specifies the polarity of the Memory Controllers's Interrupt line (INT MEM).

BIT 3
Bit 3 specifies the clock signal frequency that is used within the memory control section of the chip. When bit 3 is set, this clock signal will be at the same frequency as the crystal.
When cleared, the clock frequency will be one half the crystal frequency.

BIT 4
Bit 4 is specifies the polarity of the INDEX input signal.

BIT 5
Bit 5 is specifies the polarity of the SECTOR / AM-FOUND input signal.

BIT 6
Bit 6 is specifies the value of the Data Field Sync TimeOut (when enabled by WR28 bit 7).

BIT 7 is reserved.
This must be set to zero.

2.4.8 WRITE REGISTER 11 : ECC POLYNOMIAL SELECTION

```
==============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
==============================================
        |      |      |      |      |      |      |      |
        |      |      |      |      |      |      0      0 = #1  16 bit CRC
        |      |      |      |      |      |      0      1 = #2  32 bit ECC
        |      |      |      |      |      |      1      0 = #3  48 bit ECC
        |      |      |      |      |      |      1      1 = # 4  56 bit ECC
        |      |      |      |      |      |
        |------- |------- |------- |------- |------- |--- 0 = Reserved
```

BITS 0 and 1
Bits 0 and 1 select one of four ECC polynomials. They are:

#1 = x16+x12+x5+1 (Floppy compatible CRC)
#2 = x32+x24+x18+x15+x14+x11+x8+x7+1
#3 = (Proprietary).
#4 = (Proprietary).

Bits 2 through 7 must be set to zero.

2.4.9 WRITE REGISTER 12 through 15 : EXTERNAL GROUP STROBE

```
==================================================================
Bit |   7   |   6   |   5   |   4   |   3   |   2   |   1   |   0   |
==================================================================
Byte |                          00 - FFh                              |
==================================================================
```

When these registers are written, -GRPWRT is asserted and can be used to strobe information from the microprocessor's data bus into a peripheral chip. The information in these may be used as additional device control lines.

2.5 PROGRAMMABLE DATA SEQUENCER WRITE REGISTERS

2.5.1 WRITE REGISTER 16 : SEQUENCER COMMAND

```
=============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
=============================================
       |     |     |     |     |     |     |     |
       |     |     |     |     |     |     |     1 = Read Enable
       |     |     |     |     |     |     |
       |     |     |     |     |     |     1 = Write Enable
       |     |     |     |     |     |
       |     |     |     |     |     0 = Normal
       |     |     |     |     |     1 = Format or Read ID
       |     |     |     |     |
       |     |     |     |     0 = Normal
       |     |     |     |     1 = Long (ECC to/from Buffer)
       |     |     |     |
       |     |     |     0 = Normal
       |     |     |     1 = Syndrome to Buffer
       |     |     |
       |     |     0 = Abort on ID Flag Non zero
       |     |     1 = Ignore ID Flag
       |     |
       |     0 = Normal
       |     1 = Verify (Buffer to Disk Data)
       |
       0 = Normal
       1 = No data transfer
```

A write to the Command register initiates a command. The command is defined by the bit combination in this register and the other Data Transfer registers.

BIT 0:
When bit 0 is set (1), the operation is a READ command. Data is transferred from the disk to the buffer memory.

BIT 1
When bit 1 is set (1), the operation is a WRITE command. Data is transferred from the buffer memory to the disk.

Bits 0 and 1 should not be set (1) at the same time.

The remaining bits 2-7 are Command type modifiers, and depending on a READ or WRITE command have different meanings.

BIT 2
When bit 2 is set (1) and the operation is a READ, only ID fields will be read to the buffer.

If the operation is a write and bit 2 is set (1), the command is a FORMAT function.

BIT 3
When bit 3 is set (1), both the data and ECC check bits will be written or read to/from the buffer.

BIT 4
When bit 4 is set (1) and the operation is a READ LONG, both the data and the syndrome (the result of the ECC check) are written to the buffer.

BIT 5
When bit 5 is cleared (0), this allows processor intervention on all flag conditions. Reads or writes to a sector with a nonzero flag byte or nibble will cause the command to abort and the FLAG BYTE/NIBBLE NONZERO bit of the Extended Status register to be set. After having determined the cause of the error, the micro-processor may choose to read or write the sector anyway, in which case it sets the IGNORE FLAG/FORMAT SECTOR bit and re-issues the command.

When set (1) on READ and WRITE commands, the flag byte/nibble will be ignored.

When set (1) on FORMAT commands, the command is a Format Sector command and keys on the SECTOR line instead of the INDEX line. For this function the sequencer must be in HARD SECTORED MODE.

BIT 6
When bit 6 is set (1) on a READ command, a byte by byte compare is accomplished by reading data from the buffer and comparing it with data from the disk.

BIT 7
When bit 7 is set (1) on a READ command, it permits data fields to be read and checked for ECC errors without transferring the data to the buffer.

2.5.2 WRITE REGISTER 17 SEQUENCER LOOP COUNT

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sectors							

This register specifies the number of sectors to be read or written, or in the case of a FORMAT command, the number of sectors on the disk. (Actually, the value in this register specifies the number of times the loop in the predefined state sequence for the particular command is executed). This value is decremented for each sector handled by the command. An internal register contains the initial value of this register, so that for repeated commands involving the same number of sectors, the register will be automatically reloaded with the proper value.

Once a command has been issued the real time contents of this register can be read by reading the Sequencer Loop Count register (RR25).

2.5.3 WRITE REGISTER 18 : INDEX TIME-OUT

Bit	7	6	5	4	3	2	1	0
Byte					Number of Revolutions before time-out			

This register specifies the number of disk revolutions (as measured by the number of Index pulses) before a command is aborted. Valid values are 2 through 15. This feature allows the sequencer to do automatic retries when it cannot find the ID. This register gets re-initialized after every successful transfer for multi-block commands. When a command is aborted because of Index Tim-out, the Extended Status INDEX TIME-OUT status bit will be set. A holding register holds the value so this register only has to be loaded when a change is required.

2.5.4 WRITE REGISTER 19: SUB-BLOCK COUNT

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sub-blocks per Sector							

The Sub-Block Count is used to determine the number of data bytes per sector.
The sector size = (Sub-Block Count + 1)*Data Field Count.
The Data Field Count is from the State Controller registers.

EXAMPLES

Sector Size (Bytes)	Sub Block Count	Data Count
128	7h	10h.
256	Fh	10h.
512	1Fh	10h.
1,024	3Fh	10h.
2,048	7Fh	10h.
65,536	FFh	00h. (00=256)

This register should be loaded at initialization and any time a different sector size is being used.

2.5.5 WRITE REGISTER 20 through 23: ID REGISTERS

These four registers are compared to the first four bytes of the ID field read from the disk to determine if the desired sector has been found. Before any command, except FORMAT and CHECK TRACK FORMAT, these registers should be loaded with the first four bytes of the desired ID.

WRITE REGISTER 20 (High Byte) & 21: (Low Byte): CYLINDER (ID BYTES 0&1)

HIGH BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

LOW BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

These above two registers specify the first two bytes of the ID field. The allowed values are 0000 through FFFFh.

WRITE REGISTER 22: HEAD ADDRESS (ID Byte 2)

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh or X0 - XFh							

This byte specifies the third byte of the ID field. If the HEAD/FLAG Byte is selcted (bit 2, WR29) only the low nibble of this byte is compared. Valid values are 00 through 0Fh. When the FLAG BYTE is selected, the valid values are 00 through FFh.

WRITE REGISTER 23: SECTOR NUMBER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFH							

This register specifies the fourth byte of the ID, normally used as the sector number to be read or written. It is a counter register that is auto-incremented at the end of a valid data field operation. This feature allows sequential operations on one track without having to reload the ID write registers.

2.5.6 WRITE REGISTER 24 : MICRO TO MEMORY

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFH							

This register is used to transfer data from the micro-processor bus to the buffer memory.

The micro-processor can write to the buffer memory through this register, and data is latched in this register during transfers from a peripheral on the micro-processor bus to the buffer memory. (Refer to RR15 for details of the peripheral to buffer transfer.

When the micro-processor writes to WR24, the data is latched into WR24. The Data Sequencer then generates a request to DMA channel 0 to transfer the data from WR24 to the buffer memory location addressed by the DMA at ACK0 time.

The micro-processor should set up channel 0 of the DMA before initially writing to WR24. Subsequent writes to a contiguous block of data do not require re-initialization.

If the DMA does not respond to the channel 0 request, the Micro- Memory Over/Under Run and the Extended Status Nonzero bits in the Status and Extended Status registers will be set.

2.5.7 WRITE REGISTER 25: SEQUENCER START/RE-START

Bit	7	6	5	4	3	2	1	0
Byte	Re-Start State 0X - FXh				Start State X0 - XFh			

During the execution of a command;
-bits 0-3 specify the state number at which the sequencer will begin execution;
-bits 4-7 specify the state number from which the sequence will be re-started after the state number specified in WR26 has been reached.

This value depends on the command and the particular disk configuration. The normal values are 33h for all commands except Format, which is 21h.

This register is also used to address the internal State Control registers. Valid address values are 00 through 0Fh.

2.5.8 WRITE REGISTER 26: SEQUENCER LOOP STATE

Bit	7	6	5	4	3	2	1	0
Byte				RFBS	Loop State X0 - XFh			

Register File Bank Select

This register determines the state number when the State Controller is looping, at which point a jump to the RE-START state is performed. This value depends on the command and the particular disk configuration.

2.5.9 WRITE REGISTER 27 : BIT RING START COUNT

Bit	7	6	5	4	3	2	1	0
Byte					Start Bit X0-XFh			

This register allows the user to specify the bit-level timing relationship between sync detect and byte clock. This register should be initialized with a 03h.

2.5.10 WRITE REGISTER 28 : ECC / CRC CONTROL

```
==============================================
 Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
==============================================
        |     |     |     |     |     |     |     0 = ECC Clear on Init
        |     |     |     |     |     |     |     1 = ECC Preset on Init
        |     |     |     |     |     |     |
        |     |     |     |     |     |     0 = DATA to ECC
        |     |     |     |     |     |     1 = -DATA to ECC
        |     |     |     |     |     |
        |     |     |     |     |     0 = ECC Feedback
        |     |     |     |     |     1 = -ECC Feedback
        |     |     |     |     |
        |     |     |     |     0 = ECC Data Out
        |     |     |     |     1 = -ECC Data out
        |     |     |     |
        |     |     |     0 = ECC Check Data
        |     |     |     1 = -ECC Check Data
        |     |     |
        |     |     0 = Xfer Disabled
        |     |     1 = Xfer Enabled
        |     |
        |     0 = ID Check - ECC
        |     1 = ID Check = CRC
        |
        0 = Disable DATA Sync Timeout
        1 = Enable DATA sync Timeout
```

The ECC CONTROL register allows format and media compatibility with a variety of peripheral chips and various error correction formats.

BIT 0
BIT 0 determines whether or not initialization of the ECC shift register string is cleared (to all zeros) or preset (to all ones).

BIT 1
Bit 1 determines the polarity of NRZ input data to the ECC circuitry.

BIT 2
Bit 2 determines the polarity of the ECC feedback signal.

BIT 3
Bit 3 determines the polarity of the ECC write data output.

BIT 4
Bit 4 determines the polarity of the ECC check signal.

BIT 5
Bit 5 enables the auto-read DMA write function. In this mode data is transferred from an external peripheral chip to the data buffer via RR11.

BIT 6

BIT 6 is used to choose which type of error detection code is used for the ID field.

When bit 6 is set (1), the ID check characters are generated by the CCITT CRC-16 bit polynomial $x^{16} + x^{12} + x^5 + 1$.

When bit 6 is cleared (0), the ID check characters are generated by the ECC polynomial selected by WR11. This feature is not available if the floppy compatible polynomial is selected. Note that the setting of this bit and WR11 must match the length of the ID ECC/CRC field in the format RAM.

BIT 7

When bit 7 is set and an ID field has been properly read, failure to find the data field sync after 512 bit times will result in a Data Field Sync Time-out Error. Setting WR10 bit 6 will change this Time-Out value to 32 bits for test purposes.

2.5.11 WRITE REGISTER 29 : CONFIGURATION CONTROL

```
============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
============================================
       |     |     |     |     |     |     |     0 = Soft Sectored Mode
       |     |     |     |     |     |     |     1 = Hard Sectored Mode
       |     |     |     |     |     |     |
       |     |     |     |     |     |     0 = 1 Field Sync
       |     |     |     |     |     |     1 = 2 Field Sync
       |     |     |     |     |     |
       |     |     |     |     |     0 = Head/Flag Mode
       |     |     |     |     |     1 = Flag Byte Mode
       |     |     |     |     |
       |     |     |     |     0 = Not ESDI Mode
       |     |     |     |     1 = ESDI Mode
       |     |     |     |
       |     |     |     0 = Internal Sync Detect
       |     |     |     1 = External Sync Detect
       |     |     |
       |     |     0 = Disable Write Gate Edge
       |     |     1 = Enable Write Gate Edge
       |     |
       |     0 = Interrupt High True
       |     1 = Interrupt Low True
       |
       0 = Interrupt Disabled
       1 = Interrupt Enabled
```

BIT 0
BIT 0 selects between the Hard Sectored and Soft sectored drives. In the Hard sectored mode the SECTOR line is used to re-synchronize the sequencer at State 15 and thereby determine the sector boundaries.

BIT 1
BIT 1 selects between the 1 field sync (hard sector) and 2 field sync (soft sector) formats. The 1 byte sync is normally used by ESDI drive interfaces and the 2 byte sync (SYNC BYTE, MARKER BYTE) is used by the ST506/412 type drives.

BIT 2
Bit 2 selects between HEAD/FLAG byte (RR22) or FLAG byte Modes (RR19). The Data Sequencer allows the ID field to contain a flag nibble or a byte of information that can be used to alert the firmware that a flag condition with that sector exists, thereby stopping a command if the Ignore Flag Condition bit is not set.

If bit 2 is cleared (0), the flag information is contained in bits 4-7 of byte 2 (Flag/Head) of the ID field.

If bit 2 is set (1), the flag information is the 5th byte of the ID field. This bit also determines which read register contains the flag bits that are read from the disk. If the flag nibble is selected, the Head/Flag byte (RR22) contains the flag information; and if the flag byte is chosen, the Flag Byte register (RR19) will contain the flag information.

BIT 3
Bit 3 selects between an ESDI and a non-ESDI interface.

If the EDSI mode is cleared (0), the Sequencer is in ST-412 mode, and asserts READ GATE as soon as any Non-Format command is issued. This mode must be used to interface to the OMTI 5070 MFM and 5027 2,7 RLL ENcode/Decode chips (or OMTI SDMs devices).

If bit 3 is set (1), ESDI mode is configured, and the sequencer assumes the ESDI Search Address/Address Mark Found mode of handshake.

BIT 4
Bit 4 selects between internal sync detect (used for ESDI type interfaces) and external sync detect (used when the sequencer is configured with the OMTI 5070 and OMTI 5027 Encode/Decode/VCO chip or OMTI SDms devices)..

If bit 4 is cleared (0), the sequencer performs the BIT to BYTE synchronization by performing a bit to bit compare with the serial data in shift register and the sync field state value.

If bit 4 is set (1), the sequencer keys off of the AM-FOUND line to perform BIT to BYTE synchronization.

BIT 5
BIT 5, when set, disables the write gate for two bit times after the ID postamble field only on a Format Track command, thereby providing an edge of write gate for every PLO sync field as required by some ESDI-type drives.

Bit 6 selects between interrupt active low or high.

If bit 6 is cleared (0), and the interrupt is enabled (bit 7), an interrupt will be active HIGH.

If bit 6 is set (1), and the interrupt is enabled (bit 7), an interrupt will be active LOW.

BIT 7
Bit 7 enables or disables interrupts. If enabled, an interrupt is generated by any conditon that caused the sequencer to change from a BUSY or NOT BUSY status. The interrupt is cleared by reading the Status Register (RR16).

2.5.12 WRITE REGISTER 30: SEQUENCER VALUE REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register is used to select a VALUE in the internal RAM Register File indexed by WR25.

2.5.13 WRITE REGISTER 31 : SEQUENCER COUNT REGISTER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register is used to select a COUNT in the internal RAM Register File indexed by WR25.

2.6 MEMORY CONTROLLER READ REGISTERS

2.6.1 READ REGISTER 00 : CHANNEL STATUS

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	1 = Channel 1 Word Count > 129	1 = Channel 0 Word Count > 129	1 = Channel 1 Interrupt	1 = Channel 0 Interrupt	1 = Channel 1 Enabled	1 = Channel 0 Enabled

BIT 0 and 1
Bits 0 and 1 show the status of the Memory Controller channels 0 and 1 respectively.

BITS 2 and 3
Bits 2 and 3 show interrupt status for channel 0 and 1 respectively.

BITS 4 and 5
Bits 4 and 5 are cleared for each channel when the last 128 bytes of data are being transferred.

2.6.2 READ REGISTER 02, 06 : BYTE COUNT VALUE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register contains the least significant byte of the current count contained in the byte count register. See Write Register 2,6.

2.6.3 READ REGISTER 03, 07 : BYTE COUNT VALUE

Bit	7	6	5	4	3	2	1	0
Byte	00 - 1Fh							

This register contains the most significant byte of the current count contained in the byte count register. See Write Register 3,7.

2.6.4 READ REGISTER 12 through 15 : EXTERNAL GROUP STROBE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

When these registers are read, -GRPRD is asserted and may be used to strobe information from a peripheral chip onto the microprocessor's data bus. When the Transfer Enable bit in the ECC Control Register (WR24) is set, a read of register RR15 will enable data to be latched into the MICRO TO MEMORY register (WR24). The rising edge of this strobe will cause a DMA request and transfer the data to the buffer.

2.7 PROGRAMMABLE DATA SEQUENCER READ REGISTERS

2.7.1 READ REGISTER 16: SEQUENCER STATUS

```
==========================================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
==========================================================
       |     |     |     |     |     |     |     1 = Busy
       |     |     |     |     |     |     |
       |     |     |     |     |     |     1 = Data Field ECC Error
       |     |     |     |     |     |
       |     |     |     |     |     1 = Data Sync or Marker not found
       |     |     |     |     |
       |     |     |     |     1 = Data Verify Error
       |     |     |     |
       |     |     |     1 = ID ECC/CRC Error
       |     |     |
       |     |     1 = ID Sync or Marker not found
       |     |
       |     1 = ID Data Compare Error
       |
       1 = Extended Status Non-zero
```

The status register holds sequencer status information and is read at the completion of every command to determine whether execution was successful. During command execution, this register may be polled by the micro-processor in order to determine the bit-significant status on a sector-by-sector real time basis. For example, when a time-out has occurred, the micro-processor can determine whether or not an ID was read successfully (though the ID did not compare), or whether no ID's were successfully read, in which case the disk is improperly formatted or incompatible with the controller.

BIT 0
Bit 0 is set (1), when a command is in progress.

Bit 0 is cleared (0), when the sequencer is in a quiescent state.

BIT 1
Bit 1 is set during read operations when the sequencer detects an ECC error in the data field.

BIT 2
Bit 2 is set when, in external sync mode, the Address Mark is detected (A-M FOUND is true) but the byte value does not compare with the sync or marker byte.

BIT 3
Bit 3 is set when an error is detected during the READ VERIFY (byte by byte compare) command.

BIT 4
Bit 4 is set if an ECC or CRC error is detected in the ID field.

BIT 5
Bit 5 is set during execution of read/write operations if the sector/s ID sync and ID address mark cannot be found. The number of disk revolutions which may occur before this bit is set is determined by the value in WR18.

BIT 6
Bit 6 is set when the sequencer detects that the four-byte ID data field does not correspond to the contents of WR20-23.

BIT 7
Bit 7 is set when any bit in the Extended Status register RR17 is set.

2.7.2 READ REGISTER 17 EXTENDED SEQUENCER STATUS

```
=============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
=============================================
       |     |     |     |     |     |     |    1 = Drive Data Over/Under Run
       |     |     |     |     |     |     |
       |     |     |     |     |     |    1 = Micro Mem Over/Under Run
       |     |     |     |     |     |
       |     |     |     |     |    1 = Index Time-out
       |     |     |     |     |
       |     |     |     |    1 = Flag Byte/Bit Non-Zero
       |     |     |     |
       |     |     |    1 = Data Field Sync Time-out
       |     |     |
       |     |    1 = Registers 19 through 23 are invalid
       |     |
       |    1 = Sector (Latched)
       |
      1 = Index (latched)
```

The Extended Status register contains additional sequencer status information about command execution.

BIT 0
Bit 0 is set when the DMA Channel 0 does not respond within one byte time with acknowledge (ACK0) to the Data Sequencer's request (REQ0) for a DMA data transfer.

BIT 1
Bit 1 is set when the DMA channel 0 does not respond after the micro-processor reads or writes RR24 or WR24.

BIT 2
Bit 2 is set after the sequencer has tried to search for an ID in which ID Sync, ID Compare and ID ECC/CRC have not all been true a sector for the programmed number of retries loaded into WR18.

BIT 3
Bit 3 is set on a READ or WRITE command after the sequencer has found the proper ID but there is a FLAG Non-zero condition.

BIT 4
Bit 4 is set on a READ or WRITE command if the sequencer finds the proper ID but the data field sync has not been detected after 512 or 32 bit times (enabled by WR28 bit 7, and Time-out value selected by WR10 bit 6).

BIT 5
Bit 5 is initially set by any command to the sequencer but is cleared after the sequencer has processed any valid ID and RR19-RR23 have a valid ID stored. If after an index time-out this bit is set, RR19-RR23 have the last valid ID processed available.

BIT 6
Bit 6 is a means for the micro-processor to poll for a SECTOR / AM FOUND from the disk. This bit is latched so a very narrow pulse can still be captured.

BIT 7
Bit 7 is a means for the micro-processor to poll for an INDEX pulse from the disk. This bit is latched so a very narrow pulse can still be captured.

List of Status bits initialized by issuing a non abort command:

STATUS REGISTER

BIT	NAME	BIT VALUE
0	Busy	1
1	Data ECC Error	0
2	Data Sync + Marker Not Found	0
3	Data Verify Error	0
4	ID ECC/CRC Error	1
5	ID Sync + Marker Not Found	1
6	ID Compare Error	1
7	Extended Status Non-Zero	X

EXTENDED STATUS REGISTER BIT

0	Disk Data Over/Under-run	X
1	Micro Memory Over/Under-run	X
2	Index time-out	0
3	Flag Bit / Byte Non-Zero	X
4	Data Field Sync Time-out	0
5	Invalid ID	1
6	Sector	X
7	Index	X

2.7.3 READ REGISTER 18 RETRY COUNT /STATE ADDRESS

Bit	7	6	5	4	3	2	1	0
Byte	0X-FX = Sequencer State				X0-XF = Retry Count			

Bits 0-3 of this status register contain the actual number of disk revolutions counted on a sector by sector basis to find a valid desired sector on a READ or WRITE command.

Bits 4-7 represent the real-time value for the internal state machine of the sequencer. This information is useful for synchronizing the program to the sequencer. It is necessary to debounce this information since the state of the sequencer is changing asynchronously to the micro-processor.

2.7.4 READ REGISTER 19: FLAG BYTE (Header Byte 5)

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh = Flag Byte							

This register contains the fifth byte of header information read from the disk in a real time mode. If the format of the disk does not have five bytes of ID data, this register will not contain any valid information. If the sequencer is configured in the Flag Byte Mode and the Flag Byte Non-Zero Extended Status Bit is set, this register will contain the flag information.

2.7.5 READ REGISTER 20 (High Byte) & 21 (Low Byte): CYLINDER (ID BYTES 0 & 1)

HIGH BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

LOW BYTE

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

2.7.6 READ REGISTER 22 HEAD ADDRESS / FLAG (ID Byte 2)

Bit	7	6	5	4	3	2	1	0
Byte	FLag				Head Address			

2.7.7 READ REGISTER 23 SECTOR NUMBER

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

These four registers are the real time updated value of the current ID information from the disk. They are updated on every ID that have valid ID Sync but are not required to have valid ID CRC/ECC. Of the four registers, RR24 represents the first byte of ID information while the RR27 register contains the fourth byte of ID information. If the sequencer is configured in Flag Bit Mode, the high nibble of RR26 contains the flag information.

2.7.8 READ REGISTER 24 MEMORY TO MICRO

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register is used to transfer data from the buffer memory to the micro-processor bus.

The micro-processor can read the buffer memory through this register and data is latched in RR24 during transfers from the buffer memory to a peripheral on the memory data bus. (Refer to RR15 for details of the buffer to peripheral transfer).

When the micro-processor reads RR24, the data in the register is transferred to the micro-processor. The Data Sequencer then does a channel 0 DMA request to get ready for the next micro-processor read.

Channel 0 of the DMA should be initialized before starting a buffer read sequence. It is required to configure the DMA channel 0 control register to be in a read memory /write peripheral mode.

NOTE: It is necessary for the micro-processor to do a read of this register and discard the information the first time after initializing the DMA controller when reading data from the buffer memory. This function is required to set the first channel 0 DMA request and is considered a PRE-FETCH.

If the DMA does not respond to the channel 0 request, the Micro-Memory Over/Under Run and the Extended Status Nonzero bits in the Extended Status and Status registers will be set.

TRANSFERS BETWEEN A PERIPHERAL ON THE MICRO-PROCESSOR BUS AND MEMORY.

The Data Sequencer has the capability to transfer data from a peripheral chip that is on the micro-processor A/D bus to or from buffer memory. To transfer data from the peripheral chip to buffer memory , the micro-processor reads address RR15. To transfer data from buffer memory to the peripheral chip, the micro-processor read address RR11. This operation is enabled by setting the XFER ENABLE bit (bit 5) in the ECC Control register (WR28). Channel 0 of the DMA is used and should be initialized before starting the transfer.

When the micro-processor does a read from address RR11, the Data Sequencer generates a read strobe on pin 67 (-GRPRD), enabling the data to be latched into the Micro to Memory register (WR24). The rising edge of the strobe causes a DMA cycle, using REQ0 and ACK0 to write the contents of WR24 into the buffer memory.

When the micro-processor reads address RR11, the Data Sequencer generates a write strobe on pin 66 (-GRPWRT), enabling data to be written to the peripheral from the Memory to Micro register (RR24). On the trailing edge of the strobe, a DMA cycle is initiated, using REQ0 and ACK0, to read the next buffer memory location into RR24, in order to prepare for the next transfer.

It is necessary to pre-fetch the first byte from the buffer memory before doing the transfer to the peripheral. The micro-processor does this by setting up the DMA channel 0 control register then reading the Memory to Micro register (RR24). The Data Sequencer does a DMA cycle, using REQ0 and ACK0, to transfer the data from the buffer memory to the Memory to Micro register (RR24). This pre-fetches the data that will be written to the peripheral on the next transfer.

2.7.9 READ REGISTER 25 SEQUENCER LOOP COUNT

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Byte	**00 - FFh**							

This register contains the real time value of the sequencer loop counter. This value is decremented every time the sequencer is incremented from the Loop End State to the Restart State. This information is valuable in a multi-sector command for the micro-processor to synchronize to the sequencer. It is necessary to debounce this information since the state of the sequencer is changing asynchronously to the micro-processor.

2.7.10 READ REGISTER 26 : TEST REGISTER

```
=============================================
Bit |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
=============================================
       |     |     |     |     |     |     |     1 = Header Check Compare
       |     |     |     |     |     |     |
       |     |     |     |     |     |     1 = ECC Gate
       |     |     |     |     |     |
       |     |     |     |     |     1 = ECC Initialize
       |     |     |     |     |
       |     |     |     |     1 = Ring Counter Enable
       |     |     |     |
       |     |     |     1 = Loop Counter = 0
       |     |     |
       |     |     1 = Skip State
       |     |
       |     1 = Disk Cycle
       |
       1 = Memory cycle
```

This register allows read access to various internal signals for test purposes.

2.7.11 READ REGISTER 27 : FORCE INDEX

If this register is read, an internal INDEX signal is generated with the same timing as the -IORD input signal.

2.7.12 READ REGISTER 30 : SEQUENCER VALUE REGISTER & SEQ START

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register returns the VALUE in the internal RAM (Register File) indexed by WR25.

2.7.13 READ REGISTER 31 : SEQUENCER COUNT REGISTER & SEQ START

Bit	7	6	5	4	3	2	1	0
Byte	00 - FFh							

This register returns the COUNT in the internal RAM (Register File) indexed by WR25.

2.8 LIST OF OMTI 5055 COMMANDS

Commands are issued to the Programmable Data Sequencer by initializing all necessary parameters, then writing the command to the SEQUENCER COMMAND register (WR16).

HEX	BITs 7654 3210	COMMANDs
00	0000 0000	ABORT
01	0000 0001	NORMAL READ
02	0000 0010	NORMAL WRITE
05	0000 0101	READ ID
06	0000 0110	FORMAT TRACK
09	0000 1001	READ LONG
0A	0000 1010	WRITE LONG
0E	0000 1110	FORMAT TRACK LONG
19	0001 1001	READ SYNDROME LONG
1D	0001 1101	READ ID SYNDROME LONG
21	0010 0001	READ-IGNORE FLAG
22	0010 0010	WRITE-IGNORE FLAG
26	0010 0110	FORMAT SECTOR
29	0010 1001	READ LONG-IGNORE FLAG
2A	0010 1010	WRITE LONG-IGNORE FLAG
39	0011 1001	READ SYNDROME-IGNORE FLAG
41	0100 0001	VERIFY
49	0100 1001	VERIFY LONG
59	0101 1001	VERIFY SYNDROME LONG
61	0110 0001	VERIFY-IGNORE FLAG
69	0110 1001	VERIFY LONG-IGNORE FLAG
79	0111 1001	VERIFY SYNDROME LONG-IGNORE FLAG

81	**1000 0001**	**CHECK DATA ECC**
85	**1000 0101**	**CHECK TRACK FORMAT**
A1	**1010 0001**	**CHECK DATA ECC-IGNORE FLAG**

==

There are other combinations of bits that can be written to the SEQUENCER COMMAND register, but the results may not defined.

2.8.1 COMMAND DESCRIPTION

ABORT 00h

Issuing an ABORT to the Command register when the Data Sequencer is busy will abort the executing command. The status goes from Busy to Not-Busy. If enabled, the INTERRUPT will be set.

NORMAL READ 01h

The READ command is used to transfer a block(s) of data from the disk to the buffer.

NORMAL WRITE 02h

The WRITE command is used to transfer block(s) of data from the buffer memory to the disk.

READ ID 05h

The READ ID command is used for transferring ID sequencially from the disk to the buffer memory.

FORMAT TRACK 06h

The FORMAT command is used to format one track on the disk. After the command is issued, the Data Sequencer waits for the next INDEX pulse. On the rising edge of INDEX, the Data Sequencer turns on WRT GATE; and it stays on until the loop counter has counted through zero. If (as in a normal FORMAT TRACK command) the LOOPEND State equals an 0Fh, WRT GATE is turned off on the next rising edge of INDEX, and an INTERRUPT is set (if enabled). If the Enable Write Gate Edge bit is set (Bit 5, WR29), WRT GATE is disabled for 2 bit times preceding each data field preamble. This feature is an option for some ESDI type formats.

The size of each field of each sector on the track is determined by the counts in the State Controller Register. Except for the ID Data field, the ID ECC/CRC field and the Data ECC field, the values for all other fields are determined by the values in the State Controller Registers. The ID data field bytes are read by the Data Sequencer from the buffer memory using DMA channel zero. It is the firmware responsibility to configure DMA channel 0 to the correct mode and point to a location in buffer memory where a contiguous table of physically sequential ID data field is located.

The ID ECC/CRC and the data ECC fields values are generated by the Data Sequencer based on the contents of the ECC control and polynomial registers. The sequence loop count (WR17) defines the number of sectors on a track (the number of State Controller loops.)

INITIALIZATION

Before issuing the FORMAT command, the micro-processor should write the number of sectors on the track to the Sequencer Loop Count Register. The Index Timeout register should be loaded with a number greater than 1.

The Sub-Block Count is used to define the number of data bytes per sector.

The sector size = (Sub-Block Count +1)*Data Field Count.

The Sub Block Count is from (WR19) and the Data Field Count is from the State Controller memory.

The Sequencer Start/Re-Start register should be loaded with 21h and the Sequence Loop State register should be loaded with 0Fh.

The ID Data field bytes are read by the Data Sequencer from the buffer memory using DMA channel zero. It is the firmwares responsibility to configure DMA channel 0 to the correct mode and point to a location in buffer memory where a contiguous table of physically sequential ID data field is located.

FORMAT SECTOR 26h

The FORMAT SECTOR command can be used on Hard Sectored disks to format one or more sectors. After the command is issued, the Data Sequencer will start the format on the next SECTOR or INDEX pulse and format for the number of sectors specified in the Sequencer Loop Count register.

It is the responsibility of the micro-processor to issue the command during the sector just before the sector to be formatted. The micro-processor can count the sectors since Index by polling the Extended Status register Index and Sector bits. This command allows the controller to easily map out bad sectors even after the disk has been formatted and used.

2.8.2 PARAMETER INITIALIZATION BEFORE ISSUING COMMANDS

The ID Write Registers should be set to the desired disk location if this has not already been done. Note: The sector register gets incremented after each error free block is transferred so it is not necessary to re-initialize it for sequential block transfers.

The Sub-Block Count only needs to be re-initialized if the block size changes.

The Sequencer Start/Re-Start and Sequencer Loop State registers should be initialized to 33h and 0Eh respectively, and do not need to be changed except when doing FORMAT. Do not forget to change back after configuring for these commands.

Status after READ LONG commands -- ECC invalid bit = 1.

Initialization

After a RESET, the chip goes not-busy, the read gate (RD GATE) and write gate (WRT GATE) signals are reset and the Disk Data Over/Under Run and Micro-memory Over/Under Run bits (Bits 0 and 1, RR17) in the Extended Status are cleared.

It is the responsibility of the micro-processor firmware to initialize all other parameters after a power-up. This includes all of the Transfer Control registers and the internal State Control RAM.

ID Search

In Non-ESDI mode, after a Read/Write type command is issued to the Sequencer, RD GATE is asserted. Three bit times after A-M FOUND signal goes active, the Data Sequencer then compares the Sync byte followed by the Marker byte. Then the Sequencer reads the ID Data which is latched into the ID read registers (RR19 thru RR23), and compared with the contents of the ID write registers (WR20 thru WR23).

If they compare, the ID DATA NO COMPARE bit in the Status register is cleared. If the ID compared, the flag byte/nibble is checked. If the flag byte/nibble is nonzero, the command is aborted with the FLAG BYTE/NIBBLE NONZERO bit in the Extended Status register set (1).

The ID ECC/CRC is read and checked. If good, the ID ECC Error bit in the Status register is cleared.

If there were any ID type Errors (ID Sync, ID Compare or ID ECC/CRC), the Data Sequencer will automatically de-assert RD Gate and loop back to the Start State to retry the desired sector ID. The Sequencer searches until it finds the valid ID or for the number of revolutions specified in the Index Time-Out register.

Data Transfer

If the ID Sync, ID compared, the flag byte/nibble was zero and the ID ECC/CRC was good, RD Gate is de-asserted and re-asserted to read the data field.

When in the External Sync Detect mode (Bit 4, WR29), after the Address Mark is detected (A-M FOUND activated) the value of the Data Sync byte then the Data Marker byte is compared to the value in the State Control memory. If they do not compare, the command is aborted with the Data Sync + Marker Not Found bit in the Status register set.

If A-M Found is not detected within 512 or 32 bit times after RD GATE is activated, the command is aborted with the Data Field Sync Time-Out bit in the Extended Status register set.

After the A-M Found is detected and the Data Sync and Data Marker Bytes are valid, the Sequencer then uses REQ0 and ACK0 to request the DMA to transfer the data to the buffer memory.

If, during the data transfer, the DMA does not respond within one byte time to the Data Sequencer request (REQ0); the Disk Data Over/Under run bit set in the Extended Status register.

When the command is complete or aborted, the status will go Not Busy; and if enabled, the interrupt will be set.

SECTION 3

PIN DESCRIPTIONS

Symbol	Type	Pin #	Name and Function
ACK1	O	23	**Memory Acknowledge (Programmable).** This signal notifies the host interface that its request to Channel 1 has been granted; it is issued in response to the REQ signal. When Channel 1 is configured for the SCSI protocol, the ACK 1 output drives the SCSI REQ (Request) signal.
A/D0- ,A/D7	I/O	4 to 11	**Multiplexed Address/Data Bus. (Active High,3-state.)** These multiplexed lines interface with the low-order eight bits of the micro-processor's Address/Data bus. Addresses are latched into the address (register) on the falling edge of ALE. If the address is within the range of the internal chip select, data is either written into or read from the Memory Controller/ Data Sequencer registers, depending on whether -IOWR or -IORD is active.
ALE (8051 Mode) - AS (Z8 Mode)	I	2	**Address Latch Enable. (Active High.)** When in the 8051 mode, the falling edge of the signal is used to latch the address on the micro-processor bus (A/D-0-A/D7) into the internal address buffer. The falling edge of ALE is used to latch A/D 0-7 into the address register. When in the Z8 mode, the rising edge is used to latch the address.
A-M ENABLE	O	62	**Address Mark Enable. (Active High.)** If ESDI mode is selected, this output is active at state 1 strobe time. This function is used for writing an Address Mark to the disk. If ESDI mode is not selected, A-M ENABLE is active for state strobe 3 and 9, and may be used to enable external encoding of a "missing-clock" sync byte.
A-M FOUND	I	65	**Address Mark Found. (Active High.)** This signal is used by the Data Dequencer during a read operation for byte synchronization. This is an output from the VCO/Encode/Decode chip, and is used for MFM or 2,7 byte synchronization. If internal synchronization is configured, this input should be grounded.
-CH1INEN	O	26	**Channel 1 Input Enable (Active Low)** This output is used to enable data from the host interface buffer during a memory write cycle.
-CH1OUTCLK	O	25	**Channel 1 Out Clock (Active Low)** This output is used to clock data from a memory read cycle into an external register in the host interface.

Symbol	Type	Pin #	Name and Function
CH1RDMEM	O	27	**Channel 1 Read Memory (Active Low)** This signal is an inverted output of bit 1 in the Channel 1 control register. It is used to drive the host interface signal I/O.
CONFIG	I	75	**Configuration. (Active High.)** This input signal is internally pulled-up and is used to select which micro-processor bus type the chip is configured for, and the polarity of the WRT GATE signal. When this line is grounded, the chip is configured for an 8051 type processor; and the WRT GATE signal is active low. When it is left open, the chip is configured for a Z8-type processor, and the WRT GATE signal is active high.
-GRPRD	O	67	**Group Read Strobe. (Active Low.)** This output is strobed whenever the microprocessor reads addresses RR12 through RR15. It can be used to enable status onto the microprocessor bus (A/D 0-7) . This output can be used as an external peripheral chip select like an Intel 8255 PIO or 8273 FDC.
-GRPWRT	O	66	**Group Write Strobe. (Active Low.)** This output is strobed whenever the microprocessor does a write to addresses WR12 through WR15.It can be used to latch data from the microprocessor's data bus (A/D 0-7) into an external register. This output can be used as an external peripheral chip select like an Intel 8255 PIO or 8273 FDC.
INDEX	I	3	**Index. (Active High.)** This signal from the disk is pulsed each revolution. The Data Sequencer uses the rising edge of this signal during formatting for synchronizing and for timing out commands.
INT MEM	O	79	**Interrupt, Memory Controller (Programmable)** This output is asserted whenever the Channel Interrupt Enable bit, in that channel's Control register, is set and Channel Enable goes to a zero. This output is de-asserted whenever the microprocessor does a write to the Channel Control register of the interrupting channel. The polarity of the interrupt line is specified by bit 2 in the Memory Cycle Timing register (WR10).
INT SEQ	O	80	**Interrupt, Data Sequencer (Programmable)** If enabled, this output is asserted when the Data Sequencer has completed executing a command. This output is deasserted when the micro-processor reads the Status register.

Symbol	Type	Pin #	Name and Function
- IO/-MEM (8051 mode) -DM (Z8 mode)	I	82	**I/O/-Memory (I/O Active High.)** **-Data Memory (Active Low.)** This signal is used for active high chip enable. - When in /8051 mode, this line is connected to the 8051's IO/MEM line; - in Z8 mode, this line is an active low chip enable.
-IORD (8051 mode)	I	81	**I/O Read (Active Low.)** This input, when low, enables the information from the register selected by the previously latched address onto the micro-processor bus (A/D0-7).
-DS (Z8 Mode)			**Data Strobe. (Active Low)** This input, when low, provides the timing for data movement to or from selected registers and the micro-processor bus (A/D0-7).
-IOWR (8051 mode)	I	83	**I/O Write. (Active Low.)** When this input is low, it gates information from the microprocessor bus (A/D0-7) into the register selected by the previously latched address.
R/-W (Z8 mode)			**Read/Write. (Active High.)** This signal determines the direction of the data transfer. When low with -DS low, data is written from the micro-processor bus (A/D0-7) to the Data Sequencer. When high with -DS low, it enables the info from the selected register to the microprocessor.
MEMA 0-12	O	39 and 41 and 45 to 48 and 50 to 56	**Memory Address (Active High)** The Memory Address bus is used to output the contents of the memory address register of the chip's currently selected channel to the external buffer memory.
-MEMCE	O	44	**Memory Chip Enable (Active Low)** This output is an active low chip enable for the external buffer memory addressed by MEMA 0-12. - When both this output and -MEMWRT are asserted, data is written to the selected address in the buffer memory. - When this output is asserted and -MEMWRT is deasserted, data is read from the buffer memory.
MEM D0 - 7	I/O	32 to 38 and 40	**Memory Data. (Active High.)** This 8-bit bidirectional bus is used to transfer data to and from the external DMA buffer memory. the MEM D (0-7) lines are driven when -ACK0 or -CH1OUTCLK are low.

Symbol	Type	Pin #	Name and Function
- MEMWRT	O	49	**Memory Write (Active High.)** This output is an active low write enable for the external buffer memory.
MICROA 0-7	O	12 to 19	**Micro Address (Active High)** This 8-bit address bus is the address demultiplexed from the microprocessor's address/data bus (A/D 0-7) which is latched on the falling edge of ALE. This bus may be used to access the microprocessor's external memory and peripheral chips.
NRZ IN	I	58	**NRZ Data In. (Active High.)** This serial data input line is the NRZ read data from the drive or data separator.: - OMTI SDM-M050 or OMTI 5070 MFM Encode/Decode/VCO chip - or either OMTI SDM-R075 or OMTI 5027, 2-7 Encode/Decode/VCO chip. - or ESDI-type disk drive.
NRZ OUT	O	57	**NRZ Data Out. (Active High.)** When WRT GATE is true active, this line outputs serial NRZ write data from the Data Sequencer. All formatted fields (gaps, header, data, ECC etc.) are output to : - OMTI SDM-M050 or OMTI 5070 MFM Encode / Decode / VCO chip - or either OMTI SDM-R075 or OMTI 5027, 2-7 Encode / Decode / VCO chip. - or ESDI-type disk drive.
OSC	O	31	**Oscillator. (Active High.)** This is a (free running) TTL (level clock) output and is at the XTAL (crystal) frequency.
OSC/2	O	30	**Oscillator 2. (Active High.)** This signal is a free running (TTL level) clock (output) at one-half the oscillator input frequency XTAL frequency.
OSC/4	O	76	**Oscillator 4. (Active High.)** This signal is a free running (TTL level) clock (output) at one-fourth of the oscillator input frequency XTAL frequency.
RD GATE	O	60	**Read Gate. (Active High.)** This signal is asserted during a Data Sequencer read operation, and indicates that the drive or data separator should present read data on the NRZ IN line. The OMTI SDM-M or SDM-R (5070 or 5027) VCO/Encode/Decode chip must provide AM FOUND when the sequencer is in external sync mode.

Symbol	Type	Pin #	Name and Function
RD / REFCLK	I	59	**Read/Reference Clock. (Active High.)** This input signal has two alternative functions. When WRT GATE is true, this signal is used as a write clock to generate the write data at the NRZ-OUT pin. When RD GATE is true, a read clock locked to the read data on NRZ-IN must be supplied.
REQ1	I	20	**Memory Request (Programmable)** This is an asynchronous channel request input for Channel 1, used by the host interface to obtain access to the buffer memory. When Channel 1 is configured for the SCSI protocol, the REQ1 input is driven by the SCSI ACKnowledge signal.
-RESET	I	24	**Reset. (Active Low.)** When asserted, this input signal resets RD GATE or WRT GATE and puts the Data Sequencer in a not-Busy mode.
-ROMCE	O	78	**ROM Chip Enable (Active Low)** This output is asserted when -IORD is true and both -IOWR and IO/-MEM are false. It may be used as a chip enable signal for the microprocessor's external (P)ROM.
SECTOR/ A-M FOUND	I	68	**Sector /Address Mark Found/Sync. (Active High.)** This input can be configured as either : - the Sector line from a hard-sectored drive, - or as the Address-Mark-Found (soft sector) input from an ESDI-type drive.
SEQ A0 to SEQ A4	O	70 to 74	**Sequencer State Address Lines. (Active High.)** The address lines SEQ A0-A3 select the sequencer's state (0 - 15); SEQ A4 selects the state's Count or Value field (Count = 1, Value = 0). These lines show the current location being addressed in the internal ram buffer.
WRT CLK	O	69	**Write Clock. (Active High.)** This output is a clock at the RD/REFCLK frequency. The high to low edge of this clock is used by the Data Sequencer to clock the NRZ OUT write data signal.
WRT GATE	O	61	**Write Gate. (Configurable.)** This signal is asserted during a Data Sequencer write operation and indicates that the data on the NRZ OUT line should be written on the disk. The polarity of WRT GATE is selected by the CONFIG signal : - when CONFIG is grounded, WRT GATE is active low. - when CONFIG is left open, WRT GATE is active high.

Symbol	Type	Pin #	Name and Function
XTAL 0 - 1	I	28 29	**Crystal 0-1. (Active High.)** The XTAL lines may be connected to an external crystal oscillator to provide the oscillator signal for deriving the OSC OSC/2 and OSC/4 function outputs. If an external clock source is available, a clock input may be connected to XTAL 0 input, with XTAL 1 line left open. If a crystal is used, it must be a fundamental parallel resonant type, between the range of one to 20 Mhz. An external register must be connected accross the Xtal with a capacitor to ground from both sides of the crystal.
VDD 1 - 4	I	21 42 63 84	**Vdd. +5.0 Volts.**
VSS 1 - 4	I	1 22 43 64	**Ground.**
Spare		77	

SECTION 4

PACKAGING

84-Pin Plastic Leaded Chip Carrier

UNIT(mm)