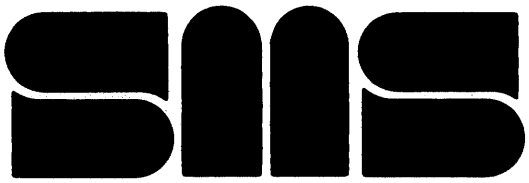

OMTI 5080 SCSI
MULTIFUNCTIONAL DEVICE
REFERENCE MANUAL
September 1985

Scientific Micro Systems, Inc.

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MULTIFUNCTIONAL DEVICE

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

The OMTI 5080 is designed to be used for three separate interface support functions. Used as an SCSI Controller, the 5080 provides interfacing in both Initiator and Target roles with arbitration and disconnect/reconnect support. As a disk I/O interface, the 5080 will support up to four drives. Additionally, the 5080 can be configured to support a QIC 02 interface.

The 5080 is optimized for use with the OMTI disk controller chip family, which includes the 5050 Data Sequencer and the 5060 DMA Controller, to provide a minimum hardware design with no sacrifice in performance or features.

APPLICATIONS

* SCSI or SASI Host Adapters
* Computers with SCSI or SASI ports
* SCSI Controllers
* SCSI Drives
* DISK Interface Control
* QIC 02 Interface Control

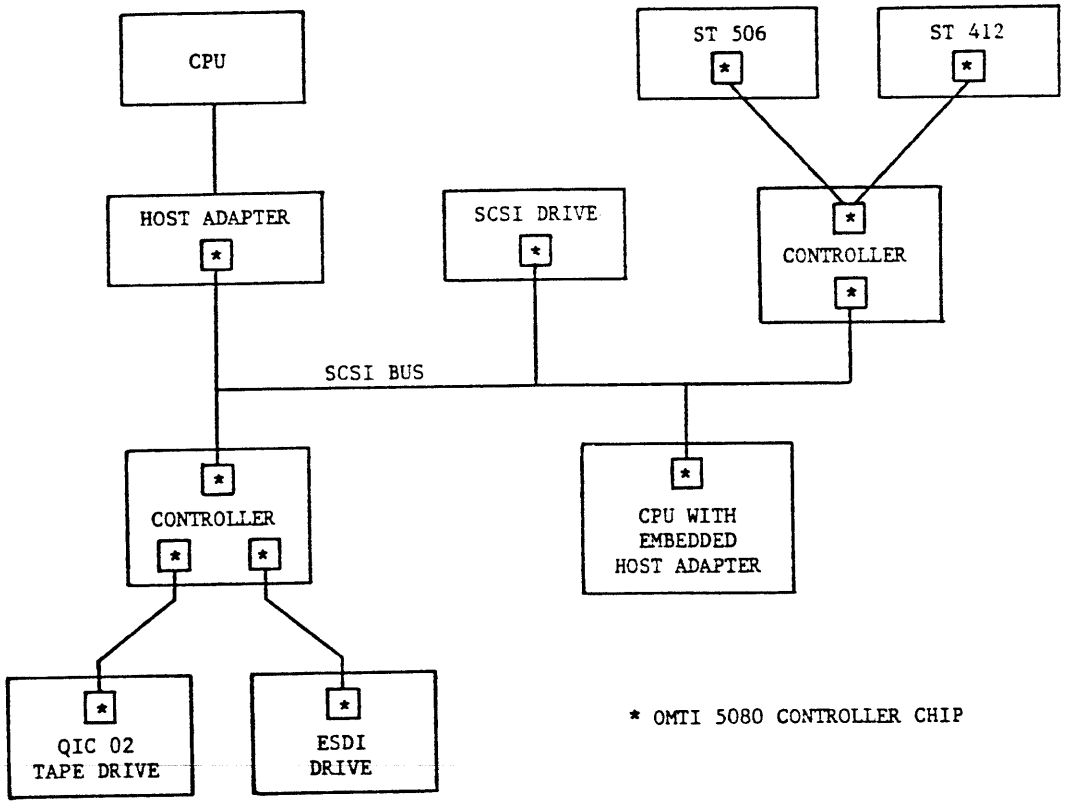


Figure 1. Application Examples Diagram

FEATURES

* Various interface support capability. Programmable to be used for one of the following three types of interface:

    1) SCSI (Small Computer System Interface) or SASI.
    2) QIC 02 Tape Interface (or ANSC X3T9.6 device level interface for Streaming Tape drives).
    3) Winchester disk drive interface (ST506/412, EDSI, 412HP, etc.)

* Includes single-ended drivers and receivers

* Microprocessor direct control of bus signals

* Programmable I/O or DMA transfer modes

* Programmable microprocessor interrupt mode

* Programmable SCSI Initiator and Target roles

* Supports SCSI disconnect/reconnect functions

* Programmable SCSI arbitration delay from clock input

* Programmable SCSI Initiator and Target ID

* Programmable parity check

* High Performance dual-bus architecture

* Includes six bus driver ground pins

* 68-pin plastic leaded chip carrier

* Low power consumption (CMOS technology)

ARCHITECTURAL OVERVIEW

The following drawings are the Conceptual and Functional Block Diagrams of the 5080 SCSI Multifunctional Device.

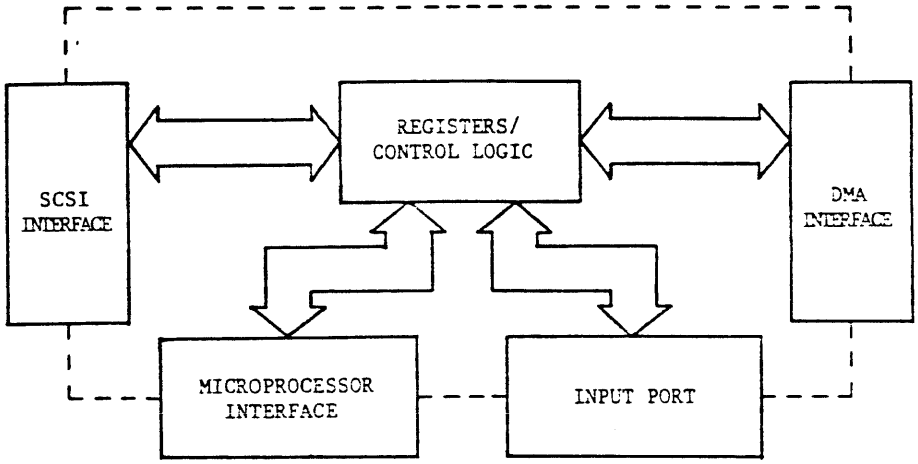


Figure 2. Conceptual Block Diagram

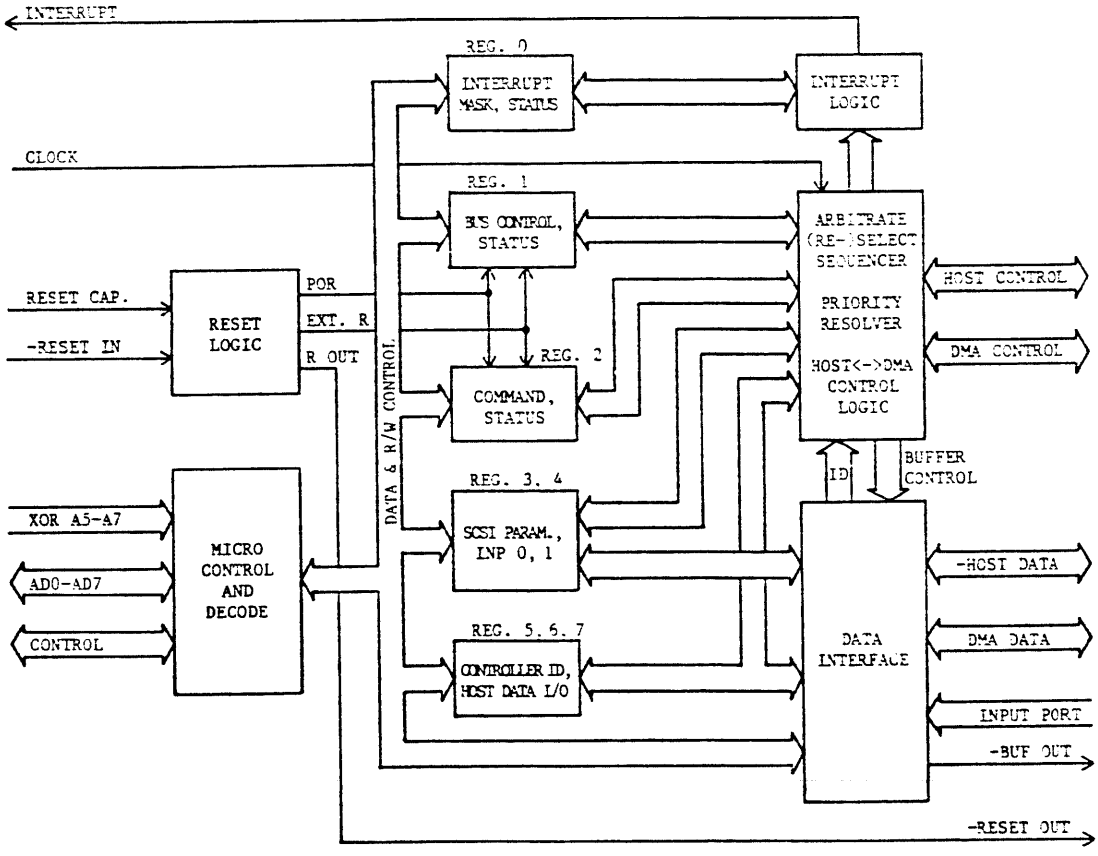


Figure 3. Functional Block Diagram

Registers/Control Logic

The Registers/Control block contains eight 8-bit internal registers and associated control logic. The write registers may be individually written to initialize the parameters that control data transfer, and for data transfer to the host bus. The read registers may be individually read to obtain status information about command execution, and for data transfer from the host bus.

Host Interface

Communication with the host is via an 8-bit bidirectional port. The host interface circuit contains the logic to transfer data between the host I/O port and either the DMA interface or the microprocessor interface.

DMA Interface

The DMA interface circuit contains the logic to transfer data to and from the 5060 DMA Memory Controller or equivelent logic. The 5060 DMA Memory Controller provides the addresses in the buffer to which this data is to be transfered. Communication with the DMA controller is over an 8-bit bidirectional bus, with request/ acknowledge handshake signals for control.

Local Microprocessor Interface

This block contains the logic which allows the local microprocessor to read and write the internal registers, and communicate with the host and DMA interfaces. Address decoding for all interfaces and internal registers is contained within this block.

Input Port

This block provides a path for the microprocessor to read jumper-selectable options, or any other data input.

The following diagram illustrates the main data paths within the 5080, and the type of I/O driver/receiver on each interface. Multiple source data outputs are individually selected with a multiplexer, with select lines generated by logic input from registers and control interface signals.

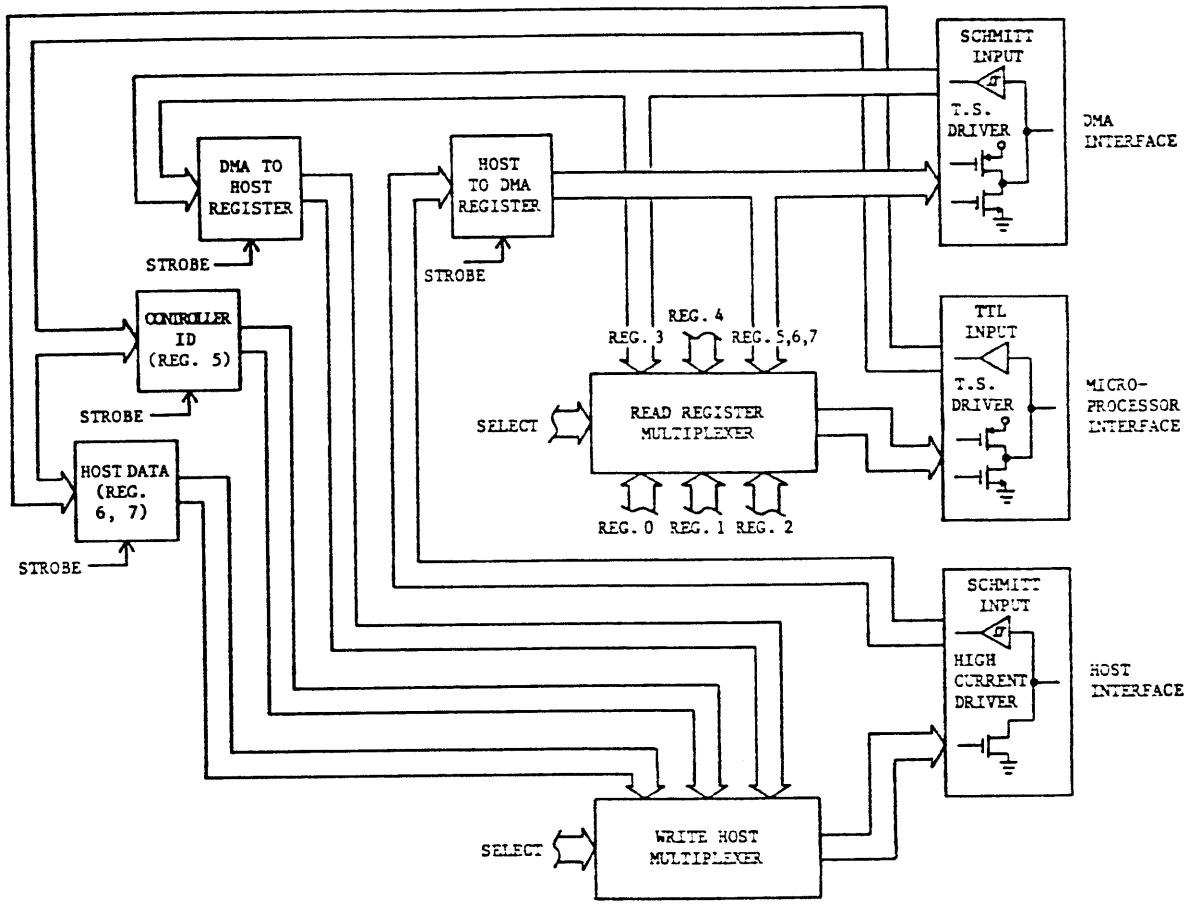


Figure 4. Internal Data Path and Interface Diagram

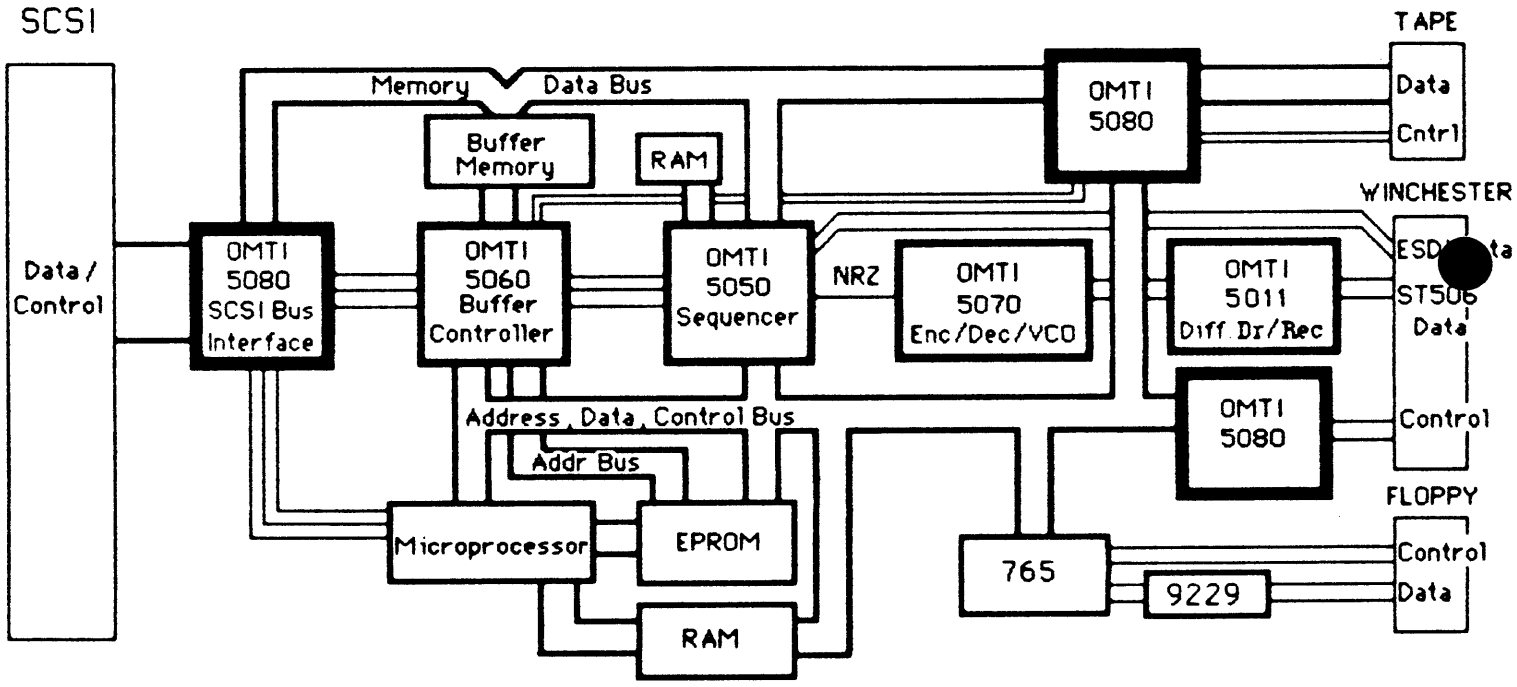


Figure 5. Typical System Configuration

Illustrated above is a typical system configuration, incorporating three 5080's in three modes of operation. Also included in the diagram is the 5050 Data Sequencer, the 5060 Four Channel DMA Controller, the 5070 VCO/Encode/Decode, and the 5011 Driver/ Receiver chip.

CHAPTER 2

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 5080's basic function is to provide a versatile interface to the SCSI bus. The 5080 device can serve in either target or initiator role, depending on it's initialization. Selection/ reselection and arbitration are handled by the 5080 device after the associated parameters have been entered into it's internal registers. The 5080 device provides the logic to interface the SCSI bus to a DMA data transfer device such as the OMTI 5060 DMA Controller. Microprocessor data transfers can also be performed through the 5080 device, either with automatic control of SCSI handshake or by direct microprocessor control via the 5080's Bus Control Register.

Additional functions provided in the 5080 device are support for QIC 02 and disk I/O interfaces. The QIC 02 support functions are similar to the SCSI support functions, with the exception of the selection/reselection and arbitration. Disk I/O interface can be accomplished by microprocessor access to the 5080's Bus Control Register.

The 5080 is designed to be used with a microprocessor having the proper control signals, such as the Z8 or 8051. Refer to the timing diagrams and pin descriptions for specific details.

REGISTERS

Registers in the 5080 provide a wide range of control over the device. They allow for selection of interrupting conditions, control of the SCSI bus and initiation/termination of commands. They provide programmable timing for the SCSI Selection/Reselection and Arbitration phases, as well as logic for arbitration. Various status bytes can be read for proper device control. Data transfer is initiated by reading and writing certain 5080 device registers. Refer to Table 1 for a list of the registers, and Tables 2 through 10 for the bit conditions associated with these registers.

5080 Register Organization

Table 1. Register Assignments and Addressing

ADDRESS 4 3 2 1 0	REGISTER NUMBER	REGISTER FUNCTION WRITE	READ
0 0 0 0 0	0	Interrupt mask	Interrupt Status
0 0 0 0 1	1	Bus Control	Bus Status
0 0 0 1 0	2	Command	Status
0 0 0 1 1	3	SCSI Arbitration Timing	Input Port 0
0 0 1 0 0	4	SCSI Arbitration Timing	Input Port 1
0 0 1 0 1	5	Controller ID	Host data (direct)
0 0 1 1 0	6	Host Data out (no handshake)	Host data (latch - no handshake)
0 0 1 1 1	7	Host data out (with handshake)	Host data (latch - with handshake)

Address bits 5-7 = Chip Select

Table 2. Register 0 - Interrupt Mask/Status

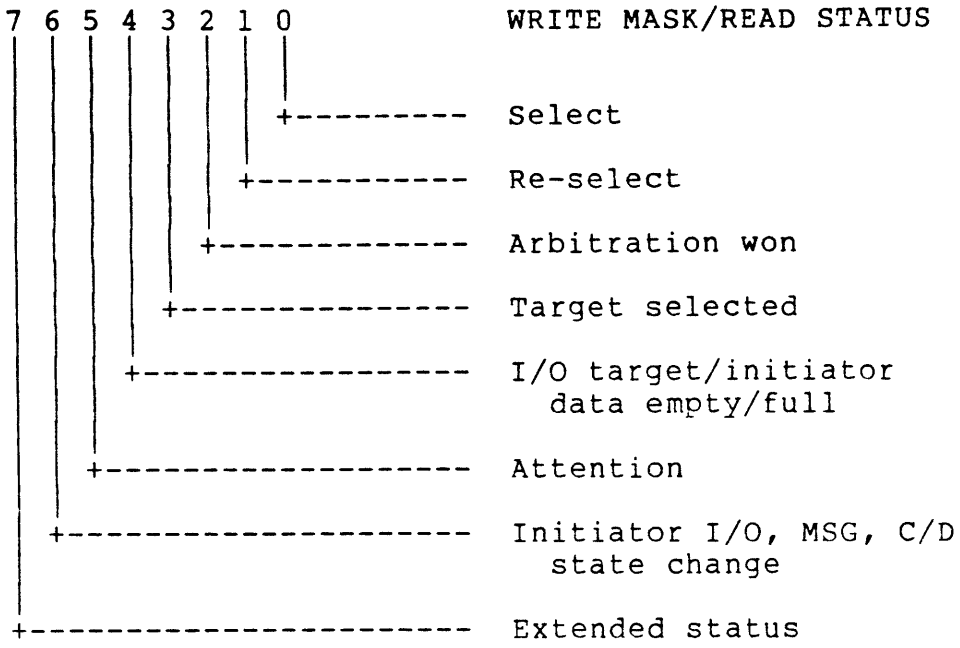


Table 3. Register 1 - Bus Control/Status, SCSI Mode

WRITE

DATA BUS 7	6	5	4	3	2	1	0	SCSI FUNCTION
0	0	0	0	0	0	0	0	Clear REQ
0	0	0	0	0	0	0	1	Clear ACK
0	0	0	0	0	0	1	0	Clear SEL
0	0	0	0	0	0	1	1	Clear BSY
0	0	0	0	0	1	0	0	Clear I/O
0	0	0	0	0	1	0	1	Clear C/D
0	0	0	0	0	1	1	0	Clear MSG
0	0	0	0	0	1	1	1	Clear ATN
1	0	0	0	0	0	0	0	* Set REQ
1	0	0	0	0	0	0	1	** Set ACK
1	0	0	0	0	0	1	0	Set SEL
1	0	0	0	0	0	1	1	Set BSY
1	0	0	0	0	1	0	0	* Set I/O
1	0	0	0	0	1	0	1	Set C/D
1	0	0	0	0	1	0	0	Set MSG
1	0	0	0	0	1	1	1	Set ATN

* Can only be set in I/O and Target mode.
** Can only be set in I/O and Initiator mode.

READ

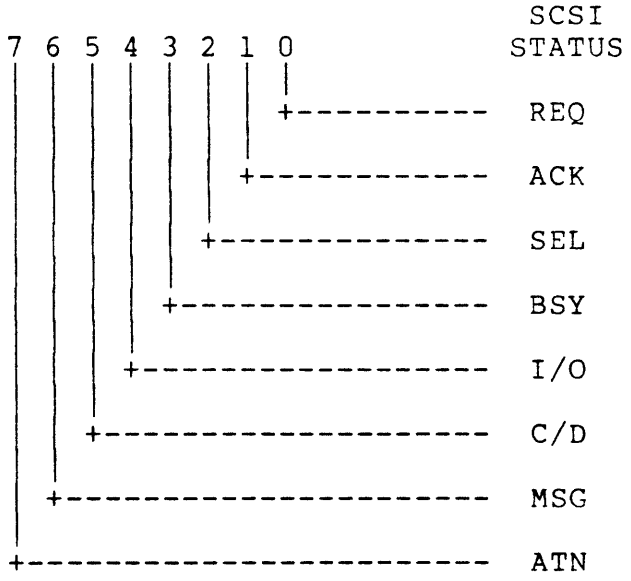


Table 4. Register 1 - Bus Control/Status, QIC 02 Mode

WRITE

DATA BUS 7 6 5 4 3 2 1 0	QIC 02 FUNCTION
0 0 0 0 0 0 0 0	Clear XFER
0 0 0 0 0 0 0 1	Clear ACK
0 0 0 0 0 0 1 0	Clear REQ
0 0 0 0 0 0 1 1	Clear ONLINE
0 0 0 0 0 1 0 0	Clear DIR
0 0 0 0 0 1 0 1	Clear EXCPT
0 0 0 0 0 1 1 0	Clear READY
0 0 0 0 0 1 1 1	Clear RESET
1 0 0 0 0 0 0 0	* Set XFER
1 0 0 0 0 0 0 1	** Set ACK
1 0 0 0 0 0 1 0	Set REQ
1 0 0 0 0 0 1 1	Set ONLINE
1 0 0 0 0 1 0 0	* Set DIR
1 0 0 0 0 1 0 1	Set EXCPT
1 0 0 0 0 1 1 0	Set READY
1 0 0 0 0 1 1 1	Set RESET

* Can only be set in I/O and Target mode.
** Can only be set in I/O and Initiator mode.

READ

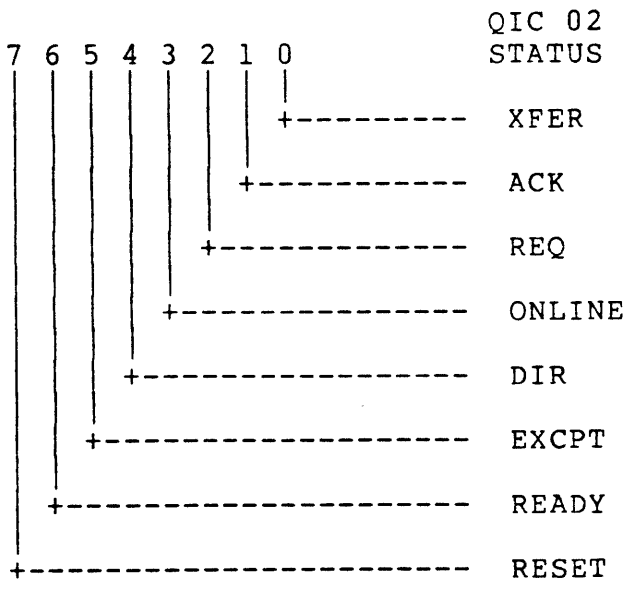


Table 5. Register 1 - Bus Control/Status, Disk I/O Mode (ST412/ESDI)

WRITE

DATA BUS 7 6 5 4 3 2 1 0	DISK I/O FUNCTION
0 0 0 0 0 0 0 0	Clear INDEX
0 0 0 0 0 0 0 1	Clear SECTOR
0 0 0 0 0 0 1 0	Clear TRK 0
0 0 0 0 0 0 1 1	Clear DIR
0 0 0 0 0 1 0 0	Clear SEEK CMP
0 0 0 0 0 1 0 1	Clear READY
0 0 0 0 0 1 1 0	Clear WRT FLT
0 0 0 0 0 1 1 1	Clear STEP
1 0 0 0 0 0 0 0	* Set INDEX
1 0 0 0 0 0 0 1	* Set SECTOR
1 0 0 0 0 0 1 0	* Set TRK 0
1 0 0 0 0 0 1 1	Set DIR/CMD DATA
1 0 0 0 0 1 0 0	* Set SEEK CMP
1 0 0 0 0 1 0 1	* Set READY
1 0 0 0 0 1 1 0	* Set WRT FLT
1 0 0 0 0 1 1 1	Set STEP/XFER REQ

* These functions SHOULD NOT be SET while in DISK I/O mode.

READ

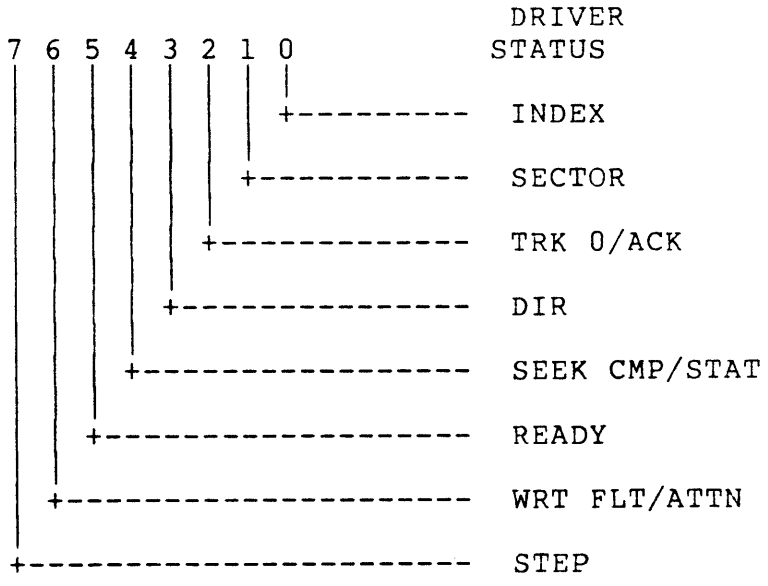


Table 6. Register 2 - Command/Status

WRITE

DATA BUS 7	6	5	4	3	2	1	0	FUNCTION
0	0	0	0	0	0	0	0	Set Arbitration Complete
0	0	0	0	0	0	0	1	Set Target Mode
0	0	0	0	0	0	1	0	Set I/O Mode
0	0	0	0	0	0	1	1	Set Select Arbitration
0	0	0	0	0	1	0	0	Set Driver I/O Disable
0	0	0	0	0	1	0	1	Set SCSI Mode
0	0	0	0	0	1	1	0	Set Interrupt High
0	0	0	0	0	1	1	1	Set Parity No-Check
1	0	0	0	0	0	0	0	Set Arbitration Sart
1	0	0	0	0	0	0	1	Set Initiator Mode
1	0	0	0	0	0	1	0	Set DMA Mode
1	0	0	0	0	0	1	1	* Set Re-Select Arbitration
1	0	0	0	0	1	0	0	Set Driver I/O Enable
1	0	0	0	0	1	0	1	* Set QIC 02 Mode
1	0	0	0	0	1	1	0	Set Interrupt Low
1	0	0	0	0	1	1	1	Set Parity Check

* QIC 02 and RE-SELECT both set=DISK I/O mode.

READ

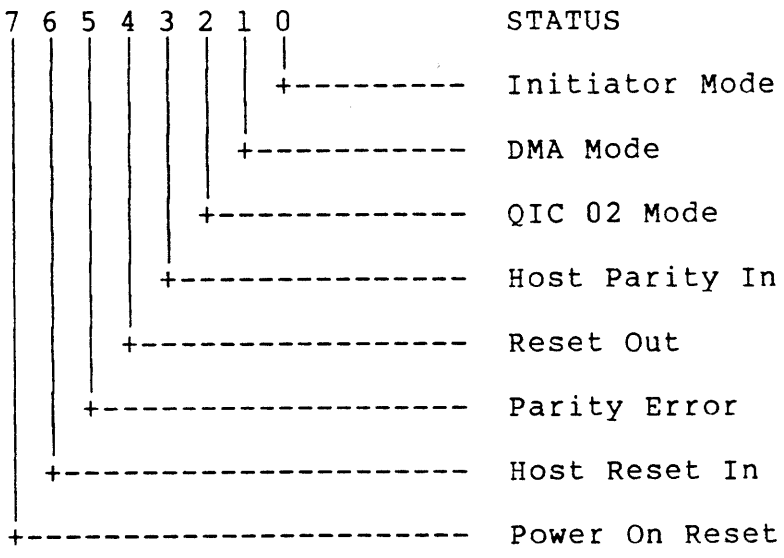


Table 7. Register 3 - SCSI Arbitration Timing 0/Input Port 0

WRITE (10 MHZ Clock)

```
+----  7 6 5 4   3 2 1 0  ----+
|                             |
```

DELAY ENABLE BUSY		BUS FREE PHASE	
0 0 0 0	not valid	0 0 0 0	not valid
0 0 0 1	200 ns	0 0 0 1	200 ns
0 0 1 0	300	0 0 1 0	300
0 0 1 1	400	0 0 1 1	* 400
0 1 0 0	500	0 1 0 0	500
0 1 0 1	600	0 1 0 1	600
0 1 1 0	700	0 1 1 0	700
0 1 1 1	* 800	0 1 1 1	800
1 0 0 0	900	1 0 0 0	900
1 0 0 1	1000	1 0 0 1	1000
1 0 1 0	1100	1 0 1 0	1100
1 0 1 1	1200	1 0 1 1	1200
1 1 0 0	1300	1 1 0 0	1300
1 1 0 1	1400	1 1 0 1	1400
1 1 1 0	1500	1 1 1 0	1500
1 1 1 1	1600	1 1 1 1	1600

* Values defined by SCSI specification.

READ

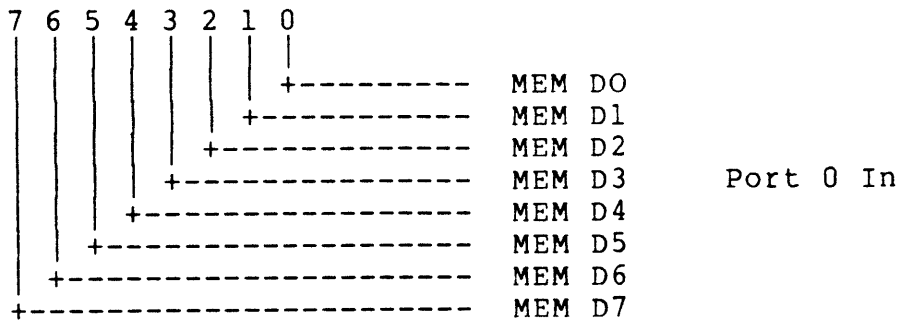


Table 8. Register 4 - SCSI Arbitration Timing 1/Input Port 1

WRITE (10 MHZ Clock)

```
          +----  7 6 5 4   3 2 1 0  ----+
          |                             |
```

DELAY ENABLE SELECT		ARBITRATION DELAY	
0 0 0 0	not valid	0 0 0 0	not valid
0 0 0 1	400 ns	0 0 0 1	400 ns
0 0 1 0	600	0 0 1 0	600
0 0 1 1	800	0 0 1 1	800
0 1 0 0	1000	0 1 0 0	1000
0 1 0 1	* 1200	0 1 0 1	1200
0 1 1 0	1400	0 1 1 0	1400
0 1 1 1	1600	0 1 1 1	1600
1 0 0 0	1800	1 0 0 0	1800
1 0 0 1	2000	1 0 0 1	2000
1 0 1 0	2200	1 0 1 0	* 2200
1 0 1 1	2400	1 0 1 1	2400
1 1 0 0	2600	1 1 0 0	2600
1 1 0 1	2800	1 1 0 1	2800
1 1 1 0	3000	1 1 1 0	3000
1 1 1 1	3200	1 1 1 1	3200

* Values defined by SCSI specification.

READ

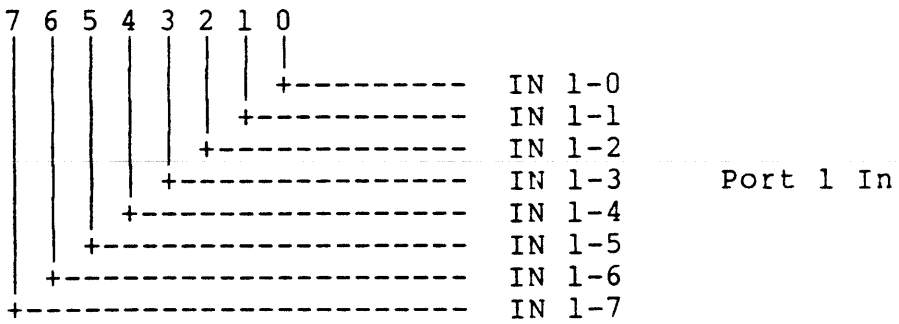


Table 9. Register 5 - Controller ID/Host Data

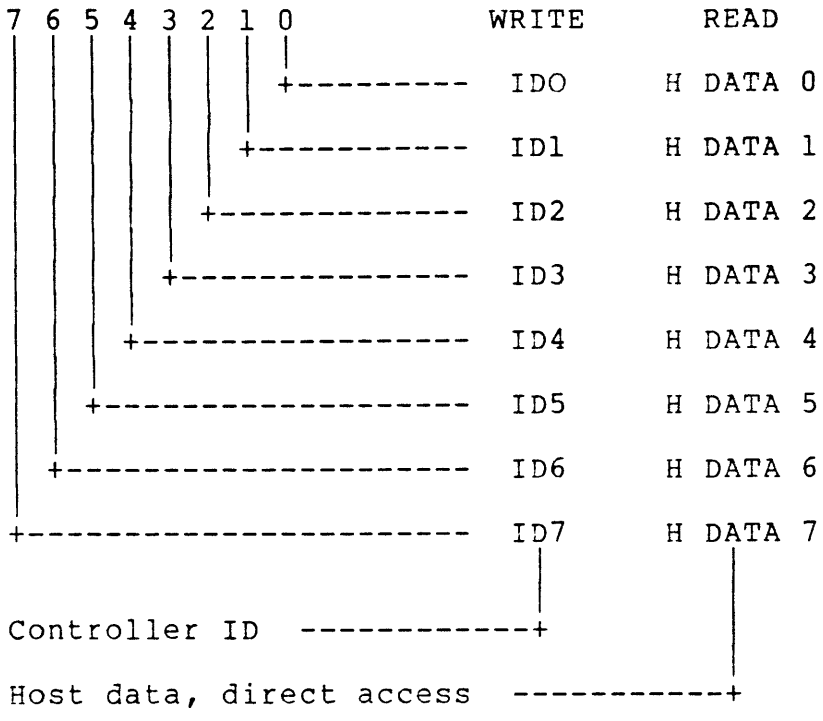
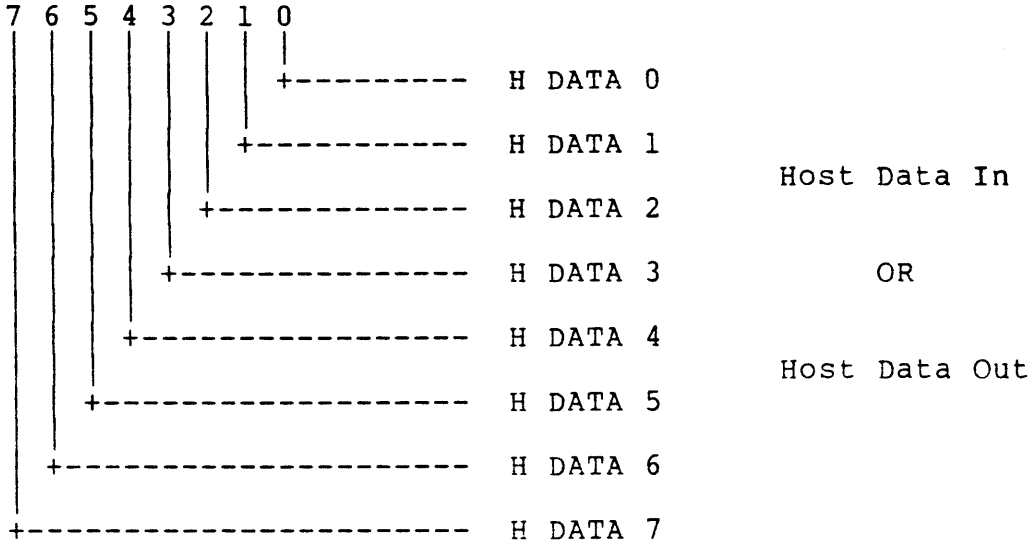


Table 10. Register 6 - Host Data I/O (no handshake)
Register 7 - Host Data I/O (with handshake)



I/O Port Signals -vs- Command Register Mode Settings

Table 11. SCSI Mode

	PIN NO.	DRIVER DIS.	SCSI DRIVER EN. TARGET I/O	SCSI DRIVER EN. TARGET DMA	SCSI DRIVER EN. INIT. I/O	SCSI DRIVER EN. INIT. DMA
-REQ	54		X			
-ACK	47				X	
-BSY	45	X	X	X	X	X
-SEL	51	X	X	X	X	X
-I/O	55		X			
-C/D	53		X	X	X	X
-MSG	50		X	X	X	X
-ATN	44	X	X	X	X	X

Note: "X" indicates I/O Port Signal -vs- Modes that can be asserted by a microprocessor write to the Bus Control Register (Reg. 1). In certain cases it may not be applicable to assert these signals.

Table 12. QIC 02 Mode

	PIN NO.	DRIVER DIS.	QIC 02 DRIVER EN. TARGET(2) I/O	QIC 02 DRIVER EN. TARGET(2) DMA	QIC 02 DRIVER EN. INIT.(2) I/O	QIC 02 DRIVER EN. INIT.(2) DMA
-XFER	54		X			
-ACK	47				X	
-TONLINE	45	X	X	X	X	X
-TREQUEST	51	X	X	X	X	X
-DIRECT	55		X	X		
-TEXCPT	53		X	X	X	X
-RDY	50		X	X	X	X
-TRESET	44	X	X	X	X	X

Notes:
1. "X" indicates I/O Port Signal -vs- Modes that can be asserted by a microprocessor write to the Bus Control Register (Reg. 1). In certain cases it may not be applicable to assert these signals.
2. In QIC 02 terminology, TARGET = DEVICE and INIT. = HOST.

Table 13. Disk I/O Mode

	PIN NO.	DRIVER DIS.	DISK I/O DRIVER EN. TARGET I/O	DISK I/O DRIVER EN. TARGET DMA	DISK I/O DRIVER EN. INIT. I/O	DISK I/O DRIVER EN. INIT. DMA
-INDEX	54		X			
-SECTOR	47				X	
-DIR	45	X	X	X	X	X
-TRK 0	51	X	X	X	X	X
-SEEK CMP	55		X	X		
-READY	53		X	X	X	X
-WRT FLT	50		X	X	X	X
-STEP	44	X	X	X	X	X

Note: "X" indicates I/O Port Signal -vs- Modes that can be asserted by a microprocessor write to the Bus Control Register (Reg. 1). In certain cases it may not be applicable to assert these signals.

Register Descriptions

REGISTER 0 INTERRUPT MASK/INTERRUPT STATUS

This register gives the user control over the condition(s) causing an interrupt, and access to a byte indicating status of all interrupt conditions.

WRITE Operation (INTERRUPT MASK)

This register allows the user to select the condition(s) by which INTERRUPT (pin 60) will become asserted. The bit condition for the mask to disable an interrupt is cleared (0). A set (1) bit will enable that condition to activate the interrupt pin. Interrupting conditions are described in the next section.

Power-on or external resets have no effect on this register.

READ Operation (INTERRUPT STATUS)

A read of this register allows the user to determine what condition caused INTERRUPT (pin 60) signal to become asserted. A description of the conditions for each bit of this register is as follows:

Bit 0 - Select
Indicates that the SCSI bus is in the Selection Phase. The following conditions exist:

-SEL is asserted
-BSY is deasserted
-I/O is deasserted
Target ID is on the SCSI bus and at least one bit completes a logical "AND" with Controller ID (Reg. 5, write).
No parity error if parity is enabled.

This bit is cleared when any of these conditions are no longer met.

Bit 1 - Reselect
Indicates that the SCSI bus is in the Reselection Phase. The following conditions exist:

-SEL is asserted
-BSY is deasserted
-I/O is asserted
Target ID is on the SCSI bus and at least one bit completes a logical "AND" with Controller ID (Reg. 5, write).
No parity error if parity is enabled.

This bit is cleared when any of these conditions are no longer met.

Bit 2 - Arbitration won
Indicates that this bus device has completed the Arbitration Phase and has won arbitration. The following conditions exist:

-SEL is asserted
-BSY is deasserted (by this device)
-I/O is asserted (if Reselect)
-I/O is deasserted (if not Reselect)
The logical "OR" of the Target & Initiator ID is on the SCSI bus (Reg. 5 & 6, write).

This bit is cleared when a Set Arbitration Complete command is issued.

Bit 3 - Target selected
Indicates that the Selection Phase is complete and the Target has control of the SCSI bus. The following conditions exist:

-SEL is asserted
-BSY is asserted (Asserted by Target)
-I/O is asserted (If Reselect)
-I/O is deasserted (if not Reselect)
The logical "OR" of the Target & Initiator ID is on the SCSI bus (Reg. 5 & 6, write).

This bit is cleared when a Set Arbitration Complete command is issued or -BSY is not asserted.

Bit 4 - I/O Target/Initiator data empty/full
This bit indicates the status of the I/O data transfer during the -REQ/-ACK handshake cycle. The 5080 device Command/Status Register (Reg. 2) must be set up in the following way:

Driver I/O Enable
SCSI Mode
I/O Mode

If the 5080 device is in Target Mode, this bit will be set when -ACK becomes deasserted. In the Initiator Mode, this bit will be set when -REQ becomes asserted. It will be reset by any of the following conditions:

A microprocessor read of the Host Data Registers 6 or 7.
A microprocessor write to the Host Data Register 7.
If any of the following command register modes are changed:

Driver I/O Enable
SCSI Mode
I/O Mode

This bit is cleared when any of these conditions are no longer met.

Bit 5 - Attention
This bit being set is an indication that the -ATN signal is in the asserted state.

Bit 6 - Initiator I/O, MSG, C/D state change.
If the Command Register (Reg. 2) is set up in Initiator or Disk I/O Mode, then a state change on the -I/O, -MSG, or -C/D (or their QIC 02/Disk I/O counterpart) signals will cause this bit to be set. This bit will be reset on the trailing edge of a microprocessor read of the Interrupt Status Register (Reg. 0), or any type of 5080 device reset.

Bit 7 - Extended Status

The Extended Status bit is an indication of a reset or parity error condition. It will be set if any of the following conditions occur:

-RST (pin 48) asserted
Power On Reset
Parity Error on the Host Bus (if parity is enabled)

This bit will be cleared on the trailing edge of a microprocessor read of the Status Register (Reg. 2).

REGISTER 1 BUS CONTROL/BUS STATUS

There are three main modes that the 5080 device can be used in. These are SCSI Mode, QIC 02 Mode, and Disk I/O Mode. All of these modes have access to one 8 bit I/O port, which will be used for the signals specific to the mode selected. The I/O port, with certain exceptions, can be accessed by a microprocessor write/read operation on the Bus Control/Bus Status Register.

WRITE Operation (BUS CONTROL)

Most individual bits on this port can be set or cleared by writing a specific byte to the Bus Control Register (Reg. 1). Refer to Tables 11, 12, and 13, and the Register 1 table (Tables 3, 4, and 5) specific to the mode you will be using for a list of these bytes, and mode-specific exceptions.

This register is cleared by a power-on or external reset.

READ Operation (BUS STATUS)

A status of the port signals specific to the 5080 device mode selected can be obtained by a microprocessor read of the Bus Status Register (Reg. 1). Each "1" bit in the Bus Status byte indicates an asserted state of that signal. Refer to the Register 1 table specific to the mode you will be using for a list of the Bus Status bits.

REGISTER 2 COMMAND/STATUS

Register 2 is the main command/status register for the 5080 device. As a command register, it is used to set modes, sub-modes, and conditions by which the 5080 device operates. As a status register, it is used to verify mode settings, host parity, parity errors, and reset status.

WRITE Operation (COMMAND)

A microprocessor write to Register 2 allows the user to select the modes and conditions for the application desired. There are sixteen options to be selected, the first eight being the complement of the second eight. Therefore, the user may select one option from each complement pair (bit 0 through 2 selects the option pair, bit 7 selects the option). Refer to Tables 11, 12, and 13, and the Register 2 - Command/ Status table (Table 6) for additional information.

This register is cleared by a power-on or external reset.

A description of each complement pair of commands and its hexadecimal byte is as follows:

00 H - Set Arbitration Complete
80 H - Set Arbitration Start

Set Arbitration Start is the command to start the SCSI Arbitration Phase. When a SCSI Bus Free Phase is detected by -SEL and -BSY being deasserted, the 5080 device initiates a SCSI Arbitration Phase. The arbitration phase continues until one of the following conditions occur:

Arbitration has been won by this bus device. A Set Arbitration Complete command is issued.

The 5080 device continues arbitration attempts after -SEL is found to be asserted (another device has captured the bus) or another device with a higher priority ID is found to be on the bus. The Set Arbitration Complete command must be used to disable any further arbitration attempts by the 5080 device.

01 H - Set Target Mode
81 H - Set Initiator Mode

Set Target Mode configures the 5080 device to react as a SCSI Target when in SCSI Mode, and as a QIC-02 Device when in QIC-02 Mode.

Set Initiator Mode configures the 5080 device to react as a SCSI Initiator when in SCSI Mode, and as a QIC-02 Host when in QIC-02 Mode.

02 H - Set I/O Mode
82 H - Set DMA Mode

I/O Mode is used to allow the microprocessor to transfer data directly to and from the -Host Data Bus (0 - 7) without using DMA channels. More information on access to the -Host Data Bus can be obtained in the description of Registers 5, 6, and 7.

DMA Mode allows for a DMA controller to have access to the -Host Data Bus and control of the SCSI/QIC 02 handshake signals. Data is transfered to and from the -Host Data Bus by way of the Memory Data Bus.

Note: If the 5080 device is set up in SCSI and Initiator Mode, a state change on the -I/O, -C/D, or -MSG signals will put the device in I/O Mode. To resume in DMA Mode, a Set DMA Mode command must be reissued.

03 H - Set Select Arbitration
83 H - Set Reselect Arbitration

The Select or Reselect Arbitration command is set in SCSI Mode to provide the correct -I/O condition on the SCSI bus during the Arbitration phase. For Select Arbitration, -I/O will be deasserted, and for Reselect Arbitration, -I/O will be asserted. To select Disk I/O Mode, QIC 02 Mode and Reselect Arbitration must be set. See the description of "Set SCSI Mode/Set QIC 02 Mode" for additional information on Disk I/O Mode.

04 H - Set Driver I/O Disable
84 H - Set Driver I/O Enable

Driver I/O Disable/Enable gives the user the capability of disabling certain pins as output drivers. Refer to Tables 11, 12, and 13 for additional information.

05 H - Set SCSI Mode
85 H - Set QIC 02 Mode

SCSI Mode and QIC 02 Mode are two of the main operating modes of the 5080 device. However, a third mode, Disk I/O Mode, can be entered by selecting QIC 02 Mode and Re-Select Arbitration. This mode is also described in this section.

SCSI Mode configures the 5080 device to mantain control of the SCSI bus as either a Target or Initiator bus device.

QIC 02 Mode configures the 5080 device to handle the QIC 02 handshake signals, control signals, and data transfers.

Disk I/O Mode configures the 5080 device as an I/O interface to an ST 506/412, or ESDI type drive. Control/status signal communication is carried out by microprocessor write/read operations on the Bus Control/Status Register (Reg. 1).

06 H - Set Interrupt High
86 H - Set Interrupt Low

Interrupt High/Low allows the user to select the polarity of the interrupting signal on the Interrupt pin (pin 60).

07 H - Set Parity No-check
87 H - Set Parity Check

Parity No-check/Check allows the user to disable/enable the parity checking logic for the -Host Data Bus. If parity checking is disabled, no interrupts are created by parity errors and no parity error is indicated in a microprocessor Read of the Command/Status Register (Reg. 2).

READ Operation (STATUS)

A read of this register provides the user with an 8-bit status of various mode settings and signal conditions. A description of these status bits is as follows:

Bit 0 - Initiator Mode

High - Initiatior Mode set
Low - Target Mode set

Bit 1 - DMA Mode

High - DMA Mode set
Low - I/O Mode set

Bit 2 - QIC 02 Mode

High - QIC 02 Mode set
Low - SCSI Mode set

Bit 3 - Host Parity In

High - Host Parity asserted
Low - Host Parity deasserted

Bit 4 - Reset Out

High - Reset in progress
Low - No reset in progress

Bit 5 - Parity Error

High - Host Data Parity error has occured
Low - No Host Data Parity error latched

Bit 6 - Host Reset In

High - Host Reset signal has occured
Low - No Host Reset signal latched

Bit 7 - Power On Reset

High - Power On Reset internal to the 5080 has occured
Low - No Power On Reset status latched

Bits 0 - 3, and 5 are cleared by a power-on or external reset. Bits 5 - 7 are cleared after a read of this register takes place. Bit 4 is a direct reflection (inverted) of the condition of the -RESET OUT signal.

REGISTER 3 SCSI ARBITRATION TIMING 0 / INPUT PORT 0

WRITE Operation (SCSI ARBITRATION TIMING 0)

Register 3, in a microprocessor write operation, consists of two 4-bit timing value registers used by the 5080's arbitration/selection logic for SCSI delay timing. A list of the delay options can be found in the Register 3 - SCSI Arbitration Timing 0/Input Port 0 table (Table 7).

Bits 0 - 3 are for the Bus Settle Delay after -SEL and -BSY are deasserted. The delay range for Bus Settle Delay is from 200 ns to 1600 ns, in increments of 100 ns.

Bits 4 - 7 are for the Bus Clear Delay before this bus device asserts -BSY. The delay range for Bus Clear Delay is from 200 ns to 1600 ns, in increments of 100 ns.

Power-on or external resets have no effect on this register.

READ Operation (INPUT PORT 0)

A microprocessor read of Register 3 will provide the user with direct access to the MEM D(0-7) bus (inverted), with input buffered through Schmitt Triggers. This register can be accessed independant of any Command Register settings or other conditions. No other registers or signals are affected.

REGISTER 4 SCSI ARBITRATION TIMING 1 / -INPUT PORT 1

WRITE Operation (SCSI ARBITRATION TIMING 1)

Register 4, in a microprocessor write operation, consists of two 4-bit timing value registers used by the 5080's arbitration/selection logic for SCSI delay timing. A list of the delay options can be found in the Register 4 - SCSI Arbitration Timing 1/Input Port 1 table (Table 8).

Bits 0 - 3 are for the Arbitration Delay after -BSY is asserted. During this time, the -Host Data Bus is monitored for a higher priority ID, and -SEL is monitored for assertion by another bus device. If the delay times out prior to these conditions, -SEL will be asserted. The delay range for Arbitration Delay is from 400 ns to 3200 ns, in increments of 200 ns.

Bits 4 - 7 provide the Bus Settle delay value after -SEL is asserted by this bus device. The -BSY signal is deasserted upon completion of this delay. The delay range for the Bus Settle Delay is from 400 ns to 3200 ns, in increments of 200 ns.

Power-on or external resets have no effect on this register.

READ Operation (-INPUT PORT 1)

Register 4 provides the user with access to an 8-bit input port. Data is recieved through Schmitt Triggers, with input pull-ups. A microprocessor read operation on this register will put bits 0 - 7 on the data bus in an inverted state. Bits 0 - 4 are from Input Port 1 (pins 24 - 28). Bits 5, 6, and 7 are from -BUF IN (pin 29), -IN ENABLE (pin 30), and -OUT CLK (pin 31), respectively. This register can be accessed independant of any Command Register settings or other conditions. Bit 5 will appear as -BUF OUT (non-inverted) on pin 22 of the 5080 device. No other registers or signals are affected.

This port can be used to provide a SCSI bus device ID or other options from a set of jumpers.

REGISTER 5 CONTROLLER ID/HOST DATA

WRITE Operation (CONTROLLER ID)

A microprocessor write to this register provides the 5080 device with this Initiator/Target bus device's ID, for use during the SCSI Arbitration Phase and Selection/Reselection Phase. For the Arbitration Phase, it will be placed on the -Host Data Bus after the Bus Free Phase along with -BSY being asserted. For the Selection/Reselection Phase, the contents of this register and the -Host Data Bus are logically "ANDed". If the result of the "AND" is true, the Select or Reselect Interrupt Status bit will be set.

Power-on or external resets have no effect on this register.

READ Operation (HOST DATA)

A microprocessor read operation to this register provides direct access to the contents of the -Host Data Bus (inverted). Data can be transfered from the -Host Data Bus without the 5080 device directly controlling the SCSI signals.

REGISTER 6 HOST DATA I/O (no handshake)

A microprocessor write to this register serves two purposes, depending on the mode and phase of operation. In SCSI Mode, during arbitration, this register holds the target's ID to be logically "OR"ed with the initiator's ID in Register 5. It is then placed on the -Host Data Bus after -SEL is asserted and at least two Bus Settle Delays have occured. The other purpose, involving both Write and Read operations, is to transfer data to and from the -Host Data Bus without the 5080 device directly controlling the SCSI handshake signals. Handshake can be provided by the microprocessor through a write to the Bus Control Register (Reg. 1). In Disk I/O Mode, this register can be used as an output port for head and drive select signals.

Power-on or external resets have no effect on this register.

REGISTER 7 HOST DATA I/O (with handshake)

Register 7 also transfers data to and from the -Host Data Bus, except that the 5080 device handles the -REQ/-ACK handshake when a microprocessor write or read to this register occurs. The device must be set in SCSI Mode, Driver I/O Enable, and I/O Mode. When Target Mode is set, the 5080 device will control the -REQ signal. When Initiator Mode is set, it will control the -ACK signal. No other signals are directly controlled by the 5080 device when accessing this register.

Power-on or external resets have no effect on this register.

CHAPTER 3

INTERFACING

SIGNAL DESCRIPTIONS

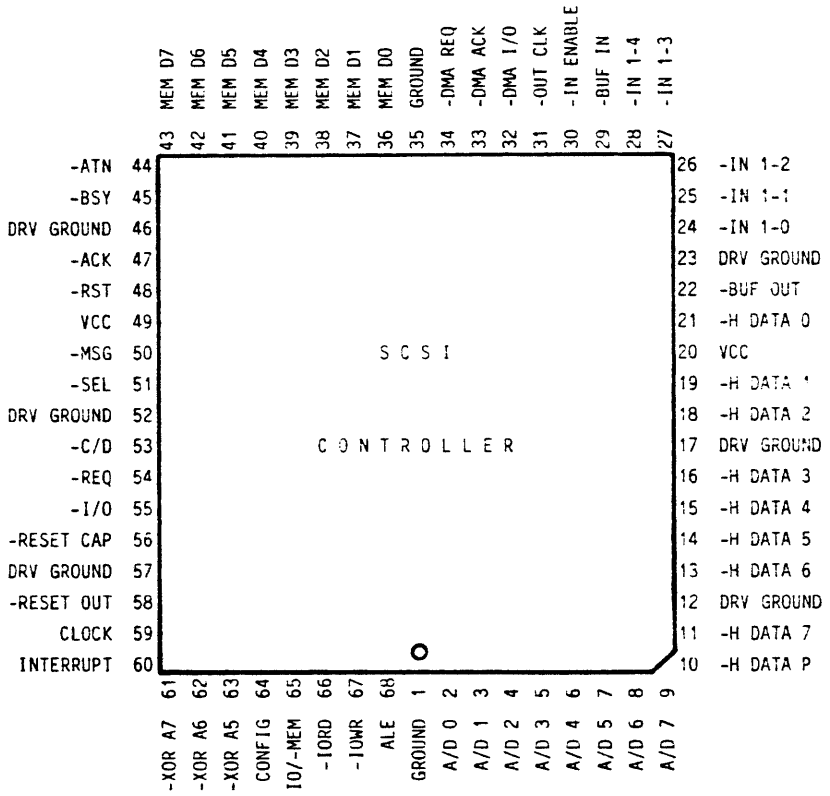


Figure 6. Pin Configuration, SCSI Controller Application

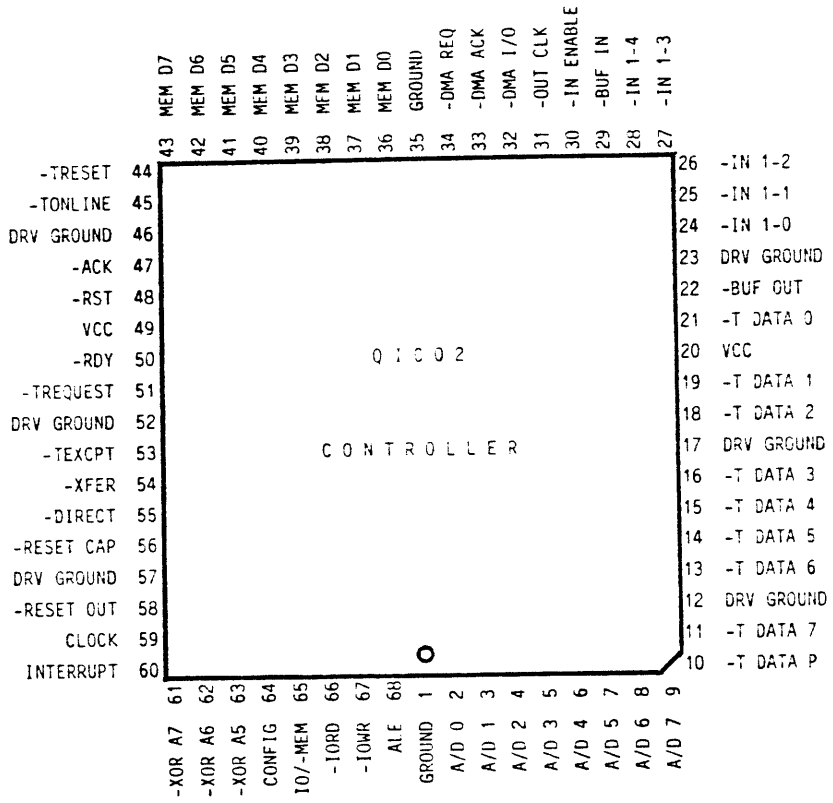


Figure 7. Pin Configuration, QIC 02 Controller Application

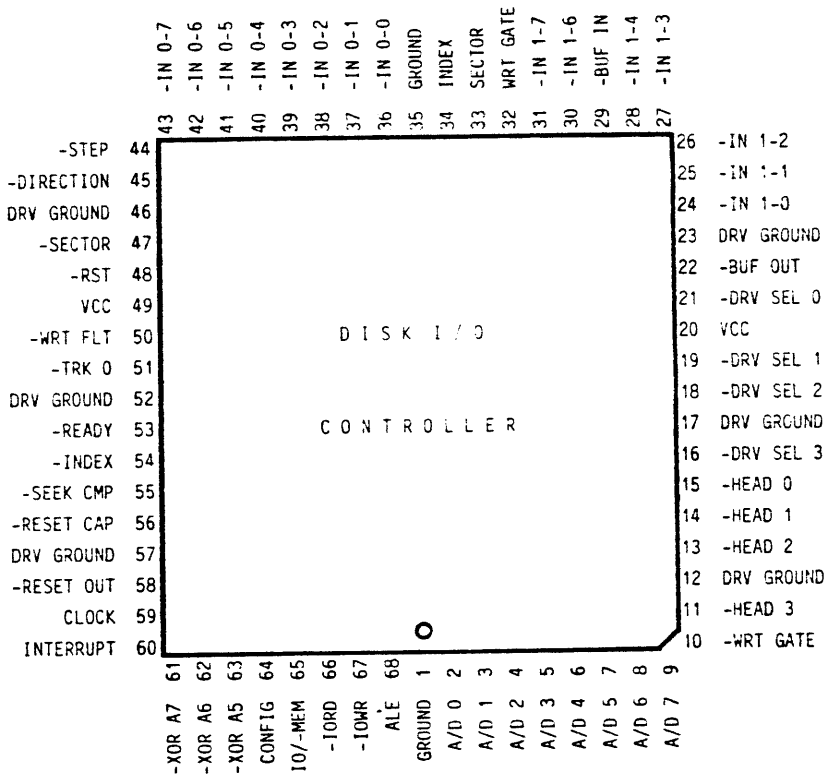


Figure 8. Pin Configuration, Disk I/O Controller Application

Table 14. Pin Descriptions, Signals Common to All Modes

Symbol	Type	Pin #	Name and Function
A/D 0-A/D 7	I/O	2-9	Address/Data Bus. (Active High, 3-state.) These Three-state address/data lines interface with the microprocessor lower 8-bit address/data bus. The addresses are latched into the address latch on the falling edge of ALE. The 8-bit data is either written into or read from the SCSI controller register, depending on -IOWR or -IORD input control lines, if the address is within the range of the internal chip select.
-BUF OUT	O	22	Buffer Out. (Active Low.) This open drain output driver may be used to provide a reset to the SCSI bus under external microprocessor control.
-IN 1 0-4	I	24-28	Input Port 1. (Active Low.) These internally pulled-up inputs may be used for default setup information. For example, the SCSI default controller ID may be set with the bits of this port. These bits are accessible to the microprocessor in an Input Port 1 read operation (Register 4, read).
-BUF IN	I	29	Buffer In. (Active Low.) This input provides direct control of the -BUF OUT signal on pin 22. It may be read as bit 5 of Input Port 1 (Register 4, read).
-RST	I	48	Reset. (Active Low.) This input is asserted by the host to abort any operation in progress and return the bus to the idle state. It provides Interrupt Status (Register 0, read) with an asserted bit 7, and Status Register (Register 2, read) with an asserted bit 6.

Symbol	Type	Pin #	Name and Function
-RESET CAP	I/O	56	Reset Capacitor. (Active Low.) The -RESET CAP pin is to be connected to an external capacitor to provide a power-on reset signal of externally controllable pulse width. The capacitor is discharged by either a power-on condition to the 5080 or a -RST signal. (pin 48). The -RESET OUT time is determined by the RC time constant of an internal ≅100K resistor and the external capacitor. When the capacitor charges to a 3.0v threshold, the -RESET OUT signal is deasserted. If an external open collector reset signal is applied to pin 56, the 5080 will react as it would to a -RST signal or power-on reset, except no reset status bits or reset interrupt will be set.
-RESET OUT	O	58	Reset Out. (Active Low.) This output is asserted on power up or when the SCSI reset input is asserted. It remains asserted until the RC time constant of pin 56 reaches the 3.0v threshold, as stated by the -RESET CAP description.
CLOCK	I	59	Clock. (Active High.) This input is for a free running clock used for the internal arbitration logic. All timing is calculated with a 10 MHz clock frequency. In order to meet SCSI specifications, any change in this frequency should be kept within a range of 2.5 MHZ - 13.75 MHZ.
INTERRUPT	O	60	Interrupt. (Active High on Reset, Programmable.) This output, if enabled, is asserted when any enabled interrupting sequence is detected, and is cleared when the microprocessor reads status or the interrupting event is disabled or deasserted. Refer to the Register Descriptions section under Register 0, READ Operation for specific information on clearing an interrupting condition.

Symbol	Type	Pin #	Name and Function
-XOR A5-A7	I	61-63	Exclusive-OR Address 5-7. (Active Low.) These internally pulled-up inputs are used for the internal chip select. Grounding one or more of these inputs will enable the corresponding A/D 5 - A/D 7 address high signal(s) to select the 5080 device. Therefore, if another group chip select is required, ground the appropriate line(s).
CONFIG	I	64	Configuration. (Active High.) This internally pulled-up line is used to select the microprocessor strobe inputs. When this input is grounded, the chip is configured for an 8051 type microprocessor using individual read and write strobes. When left open, the chip is configured for a Z8 type microprocessor with separate strobe and read/write signals.
VCC	I	20, 49	VCC. +5 Vdc
GND	I	1, 35	Ground.
DRV GND	I	12, 17, 23, 46, 52, 57	Drive Ground (isolated from circuit ground plane).

Table 15. Pin Descriptions, Signals Specific to SCSI Mode

Symbol	Type	Pin #	Name and Function
-H DATA P	I/O	10	Host Data Parity. (Active Low.) This driver/receiver I/O line in output mode is odd parity of the host data bus. In input mode the host must generate odd parity of the bus and the SCSI controller will check for valid parity if internally enabled.
-H DATA 0-7	I/O	21, 19,18, 16-13, 11	Host Data 0-7. (Active Low.) These driver/ receiver input/output signals are the 8-bit data bus from/to the SCSI data bus. As inputs, they provide data to the internal Host-to-DMA Register. As outputs, they transfer data from the internal Write Host Multiplexer to this bus. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-IN ENABLE	I	30	Input Enable. (Active Low.) This input enables data from the -H DATA 0-7 bus (latched) to the MEM D0-D7 bus for DMA write.
-OUT CLK	I	31	Output Clock. (Active Low.) This input strobes data from the MEM D0-D7 bus to the internal DMA-to-Host Register. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-DMA I/O	I	32	DMA I/O (Active Low.) This input, in DMA and Target Mode, provides direct control of the -I/O signal (pin 55) by the DMA controller.
-DMA ACK	I	33	DMA Acknowledge. (Active Low.) This input, in DMA and Initiator Mode, clocks the -ACK (pin 47) asserted on its trailing edge. In DMA and Target Mode, it provides direct control of the -REQ signal (pin 54).
-DMA REQ	O	34	DMA Request. (Active Low.) This output, in DMA and Target Mode, is directly controlled by the -ACK input (pin 47). In DMA and Initiator Mode, it is directly controlled by the -REQ input (pin 54).

Symbol	Type	Pin #	Name and Function
MEM DO-D7	I/O	36-43	Memory Data Bus. (Active High.) These input/output signals are the 8-bit data bus from/to the DMA buffer memory. As inputs, they provide data to the internal DMA-to-Host Register, and to a Register 3, read operation. As outputs, they transfer data from the internal Host-to-DMA Register to this bus. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-ATN	I/O	44	Attention. (Active Low.) This driver/receiver I/O line allows direct microprocessor control of/access to the -ATN signal through a write/read of Register 1, Bus Control/Status.
-BSY	I/O	45	Busy. (Active Low.) This driver/receiver I/O signal indicates that the bus is in use. In Initiator Mode, (for selection) it is received, asserted, then deasserted by the 5080 device under control of the internal state generator. In Initiator Mode, (for reselection) it is received, asserted/deasserted (depending on the SCSI phase required) through a write/read of Register 1, Bus Control/Status. In Target Mode, (for selection) it is received, asserted/deasserted (depending on the SCSI phase required) through a write/read of Register 1, Bus Control/Status. In Target Mode, (for reselection) it is received, asserted, then deasserted by the 5080 device under control of the internal state generator.
-ACK	I/O	47	Acknowledge. (Active Low.) This driver/receiver I/O signal is an indication that data is available from, or has been received by, the initiator. In Target Mode, this signal is received by the 5080 device. If DMA Mode is set, -ACK has direct control of the -DMA REQ signal (pin 34).

Symbol	Type	Pin #	Name and Function
			In Initiator Mode, this signal is asserted by the 5080 device. If DMA Mode is set, then -DMA ACK (pin 33) clocks this signal to asserted, and -REQ (pin 54) clears it to deasserted. If I/O Mode is set, then -ACK is either under the control of the Bus Control Register (Register 1, write) or the Host Data I/O Port (Register 7, automatic control of -ACK upon data write/read).
-MSG	I/O	50	Message. (Active Low.) This driver/receiver I/O signal indicates that a SCSI Message Phase is in progress. The microprocessor has direct control of, or access to, the -MSG signal through the Bus Control/Status Register (Register 1, write/read).
-SEL	I/O	51	Select. (Active Low.) This driver/receiver I/O signal is an indication that the SCSI Bus is in the Selection or Reselection Phase. In Target Mode and Selection Phase, this signal is received by the 5080 device through the Bus Status Register (Register 1, read). In Target Mode and Reselection Phase, this signal is asserted by this 5080 device, under control of it's internal state generator. In Initiator Mode and Selection Phase, this signal is asserted by this 5080 device, under control of it's internal state generator. In Initiator Mode and Reselection Phase, this signal is received by this 5080 device to control it's internal state generator.
-C/D	I/O	53	Control/Data. (Active Low.) This driver/receiver I/O signal indicates whether Control or Data information is on the data bus. In Target Mode, it is asserted by the 5080 device for all command data transfers. In Initiator Mode, this line is received to indicate that the target has command/data to transfer.

Symbol	Type	Pin #	Name and Function
-REQ	I/O	54	Request. (Active Low.) This driver/ receiver I/O signal is an indication that data is to be transfered to, or received from, the initiator. In Target Mode, this signal is asserted by the 5080 device. If DMA Mode is set, then -DMA ACK has direct control of this signal. If I/O Mode is set, then -REQ is either controlled by the Bus Control Register (Register 1, write), or the Host Data I/O Port (Register 7, automatic control of -REQ upon data write/read). In Initiator and DMA Mode, this signal is received by the 5080 device and has direct control of the -DMA REQ signal (pin 34).
-I/O	I/O	55	Input/Output. (Active Low.) This driver/ receiver I/O signal controls data transfer direction with respect to the initiator. During the Reselection Phase, this signal asserted indicates that the winning bus device is a target. In Target and DMA Mode, this signal is asserted by the 5080 device under direct control of the -DMA I/O signal (pin 32). In Target and I/O Mode, this signal is under the control of the Bus Control Register (Register 1, write). In Initiator Mode, this signal is available to the Bus Status Register (Register 1, read).

Table 16. Pin Descriptions, Signals Specific to QIC 02 Mode

Symbol	Type	Pin #	Name and Function
-T DATA P	I/O	10	Tape Data Parity. (Active Low.) Generates odd-parity of the tape data bus on output, expects odd-parity on bus on input. Controller checks for valid parity if internally enabled.
-T DATA 0-7	I/O	21, 19,18, 16-13, 11	Tape Data 0-7. (Active Low.) These driver/ receiver input/output signals are the 8-bit data bus from/to the QIC-02 data bus. As inputs, they provide data to the internal Host-to-DMA Register. As outputs, they transfer data from the internal Write Host Multiplexer to this bus. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-IN ENABLE	I	30	Input Enable. (Active Low.) This input enables data from the -T DATA 0-7 bus (latched) to the MEM D0-D7 bus for DMA write.
-OUT CLK	I	31	Output Clock. (Active Low.) This input strobes data from the MEM D0-D7 bus to the internal DMA-to-Host Register. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-DMA I/O	I	32	DMA I/O (Active Low.) This input, in QIC-02 Mode, serves no purpose and would normally be grounded.
-DMA ACK	I	33	DMA Acknowledge. (Active Low.) This input, in DMA and Device (Target) Mode, provides direct control of the -ACK signal (pin 54).
-DMA REQ	O	34	DMA Request. (Active Low.) This output, in DMA Mode, is directly controlled by the -ACK/-XFER input (pin 47).

Symbol	Type	Pin #	Name and Function
MEM DO-D7	I/O	36-43	Memory Data Bus. (Active High.) These input/output signals are the 8-bit data bus from/to the DMA buffer memory. As inputs, they provide data to the internal DMA-to-Host Register, and to Input Port 0 (Register 3, read). As outputs, they transfer data from the internal Host-to-DMA Register to this bus. Refer to Figure 5, Internal Data Path and Interface Diagram for additional information.
-TRESET	O	44	Reset. (Active Low.) This driver/receiver I/O signal, in Host (Initiator) Mode, is asserted by the Bus Control Register (Register 1, write) to initiate a device initialization. In Device (Target) mode, the Bus Status Register (Register 1, read) receives the reset signal.
-TONLINE	I/O	45	Online. (Active Low.) This driver/receiver I/O line, in Host (Initiator) Mode, is asserted by the Bus Control Register (Register 1, write) prior to transferring a read or write command. It is deasserted to terminate that read or write command. In Device (Target) mode, the Bus Status Register (Register 1, read) receives the online signal.
-ACK -XFER	I I	47 47	(Host Application.) (Device Application.) Acknowledge/Transfer. (Active Low.) This driver/receiver I/O line, in QIC 02 Mode, operates as a receiver only. In DMA mode, it is in direct control of -DMA REQ (pin 34) whether in Host (Initiator) or Device (Target) mode. In I/O mode, the Bus Status Register (Register 1, read) receives this signal. In Host (Initiator) Mode, this pin receives the -ACK bus signal to indicate that data has been taken in a write operation, or that data is available in a read operation. In Device (Target) Mode, this pin receives the -XFER bus signal to indicate that data is available in a write operation, or that data has been taken in a read operation.

Symbol	Type	Pin #	Name and Function
-RDY	I/O	50	Ready. (Active Low.) This driver/receiver I/O line, in Device (Target) Mode, is asserted by the Bus Control Register (Register 1, write) when a command is completed or when the device is ready to receive/transmit the next block or receive the next command. In Host (Initiator) Mode, the Bus Status Register (Register 1, read) receives the ready signal.
-TREQ	I/O	51	Tape Request. (Active Low.) This driver/ receiver I/O line in Host (Initiator) Mode is asserted by the Bus Control Register (Register 1, write) to indicate that command data has been placed on the data bus for a Command operation, or that status has been taken from the bus in a Status Input operation. This line is asserted only when -RDY or -EXC is asserted by the tape device. In Device (Target) mode, the Bus Status Register (Register 1, read) receives this signal.
-TEXCPT	I/O	53	Tape Exception. (Active Low.) This driver/ receiver I/O line in Device (Target) Mode is asserted by the Bus Control Register (Register 1, write) to indicate that an exception condition exists. The device expects status command and status input following -TEXCPT. In Host (Initiator) Mode the Bus Status Register (Register 1, read) receives the -TEXCPT signal.
-XFER	O	54	(Host Application.)
-ACK	O	54	(Device Application.) Transfer/Acknowledge. (Active Low.) This driver/receiver I/O line, in QIC 02 Mode, operates as a driver only. In DMA mode, it is under the direct control of -DMA ACK (pin 33), whether in Host (Initiator) or Device (Target) mode. In I/O mode, the Bus Control Register (Register 1, write) asserts this signal.

Symbol	Type	Pin #	Name and Function
			In Host (Initiator) Mode, this pin generates the -XFER bus signal to indicate that data is available in a write operation, or that data has been taken in a read operation. In Device (Target) Mode, this pin generates the -ACK bus signal to indicate that data has been taken in a write operation, or that data is available in a read operation.
-DIRECT	I/O	55	Direction. (Active Low.) This driver/receiver I/O line in Device (Target) Mode is asserted by the Bus Control Register (Register 1, write) to indicate the direction of data transfer: From the device when -DIR is asserted. To the device when -DIR is deasserted. In Host (Initiator) Mode, the Bus Status Register (Register 1, read) receives the -DIRECT signal.

Table 17. Pin Descriptions, Signals Specific to Disk I/O Mode

Symbol	Type	Pin #	Name and Function
-HEAD 0-3	O	15-13,11	Head Select 0-3. (Active Low.) These active low outputs are used to enable the desired drive read/write head. These lines are controlled directly by bits 4-7 of the Host Data Port (Register 6, write).
-DRV SEL 0-3	O	21,19, 18,16	Drive Select 0-3. (Active Low.) These active low outputs select one of up to four disk drives. The outputs are controlled directly by bits 0-3 of the Host Data Port (Register 6, write).
-IN 1 6,7	I	30-31	Input Port Bits 6,7. (Active Low.) These internally pulled-up inputs, along with -IN 1 0-5, are accessed through Input Port 1 (Register 4, read), and may be used for any desired setup or sensing function.
WRT GATE	I	32	Write Gate. (Active High.) This is an input signal from the data sequencer which indicates that data is being output to the drive. This signal passes through the Disk I/O controller to pin 10, -WRT GATE.
SECTOR	O	33	Sector. (Active High.) This is an output to the data sequencer and indicates a sector mark or address found condition has been detected. This signal originates on pin 47, and is gated to this output.
INDEX	O	34	Index. (Active High.) This is an output to the data sequencer and indicates that an index pulse has been detected. This signal originates on pin 54, and is gated to this output.
-IN 0 0-7	I	36-43	Input Port 0-7. (Active Low.) These Schmitt Trigger inputs are accessed through Input Port 0 (Register 3, read), and can be used for any desired setup, sensing, or data acquisition function.

Symbol	Type	Pin #	Name and Function
-STEP	O	44	Step. (Active Low.) This output produces a negative pulse for positioning the drive read/write heads. It is controlled by writing the appropriate byte to the Bus Control Register (Register 1).
-DIR	O	45	Direction. (Active Low.) This output controls the direction the read/write heads move when stepped. A low signal results in the heads stepping in toward the disk hub while a high signal results in the heads stepping out towards the disk rim. It is controlled by writing the appropriate byte to the Bus Control Register (Register 1).
-SECTOR	I	47	Sector. (Active Low.) Input from the drive indicating a sector pulse has been detected. This signal is gated through to pin 33.
-WRT FLT	I	50	Write Fault. (Active Low.) An input from the drive indicating a write fault condition exists. It is accessed by reading the appropriate bit in the Bus Status Register (Register 1).
-TRK 0	I	51	Track 0. (Active Low.) An input from the drive indicating the heads are positioned over track 0, the outermost track. It is accessed by reading the appropriate bit in the Bus Status Register (Register 1).
-READY	I	53	Ready. (Active Low.) An input from the drive indicating that the spindle is up to speed and that the drive is ready for seeks and data transfers. It is accessed by reading the appropriate bit in the Bus Status Register (Register 1).
-INDEX	I	54	Index. (Active Low.) This input from the drive indicates that the drive has detected an index pulse. This signal is gated through to pin 34.

Symbol	Type	Pin #	Name and Function
-SEEK CMP	I	55	Seek Complete. (Active Low.) This signal from the drive indicates that the read/write heads have settled on the final track at the end of a seek and that a data transfer may begin. It is accessed by reading the appropriate bit in the Bus Status Register (Register 1).

Table 18. Pin Descriptions, Signals Specific to 8051 Mode

(CONFIG = LOW)

Symbol	Type	Pin #	Name and Function
I/O-MEM	I	65	I/O/-Memory. (Active High.) This input enables -IORD and -IOWR strobes if asserted, and disables those strobes if deasserted.
-IORD	I	66	I/O Read. (Active Low.) This input strobe is used by the microprocessor to read status information from the SCSI controller with the proper address for chip and register selection.
-IOWR	I	67	I/O Write. (Active Low.) This active low input strobe is used by the microprocessor to load information into the SCSI controller with the proper address for chip and register selection.
ALE	I	68	Address Latch Enable. (Active High.) This input strobe is for storing address 0-7 into the address register on the falling edge of ALE for internal chip and register select.

Table 19. Pin Descriptions, Signals Specific to Z8 Mode

(CONFIG = HIGH)

Symbol	Type	Pin #	Name and Function
-DM	I	65	Data Memory. (Active Low.) This input enables the data strobe, -DS, if asserted, and disables -DS if deasserted.
-DS	I	66	Data Strobe. (Active Low.) This active low input is used by the microprocessor to read status information from the SCSI controller, if R/-W is asserted, or to load information into the SCSI controller if R/-W is deasserted.
R/-W	I	67	Read/Write. (Active High.) This input determines whether a read operation (R/-W high) or a write operation (R/-W low) is desired by the microprocessor.
-AS	I	68	Address Strobe. (Active Low.) This input strobe is for storing addresses 0-7 into the address register on the rising edge of -AS for internal chip and register select.

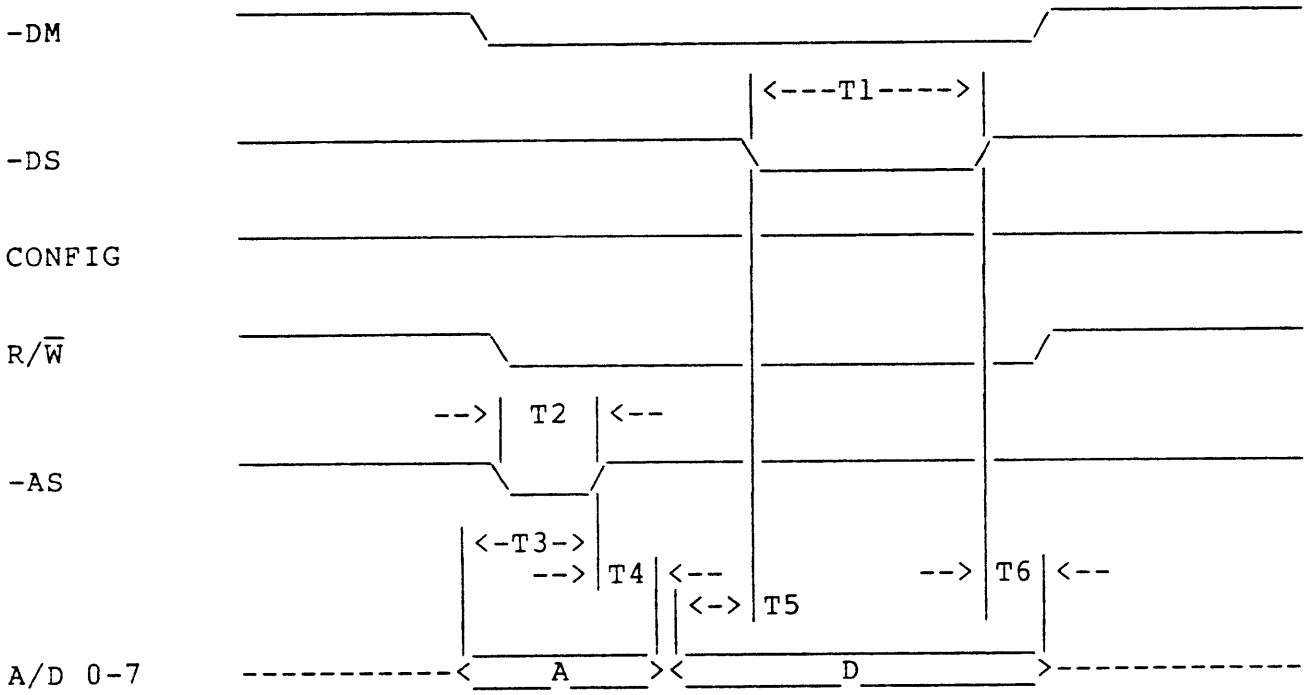
A.C. CHARACTERISTICS

The relevant timing diagrams and A.C. characteristics for interfacing the 5080 Controller chip are given below. For more information about the microprocessors, refer to Zilog's Z8681/82 ROMless Z8 Microcomputer Product Specification or to Intel's 8051 Single Chip 8-Bit N-Channel Microprocessor Data Sheet.

Z8 Mode Timing Characteristics (CONFIG = HIGH)

Write Operation, Z8 Configuration

Signal

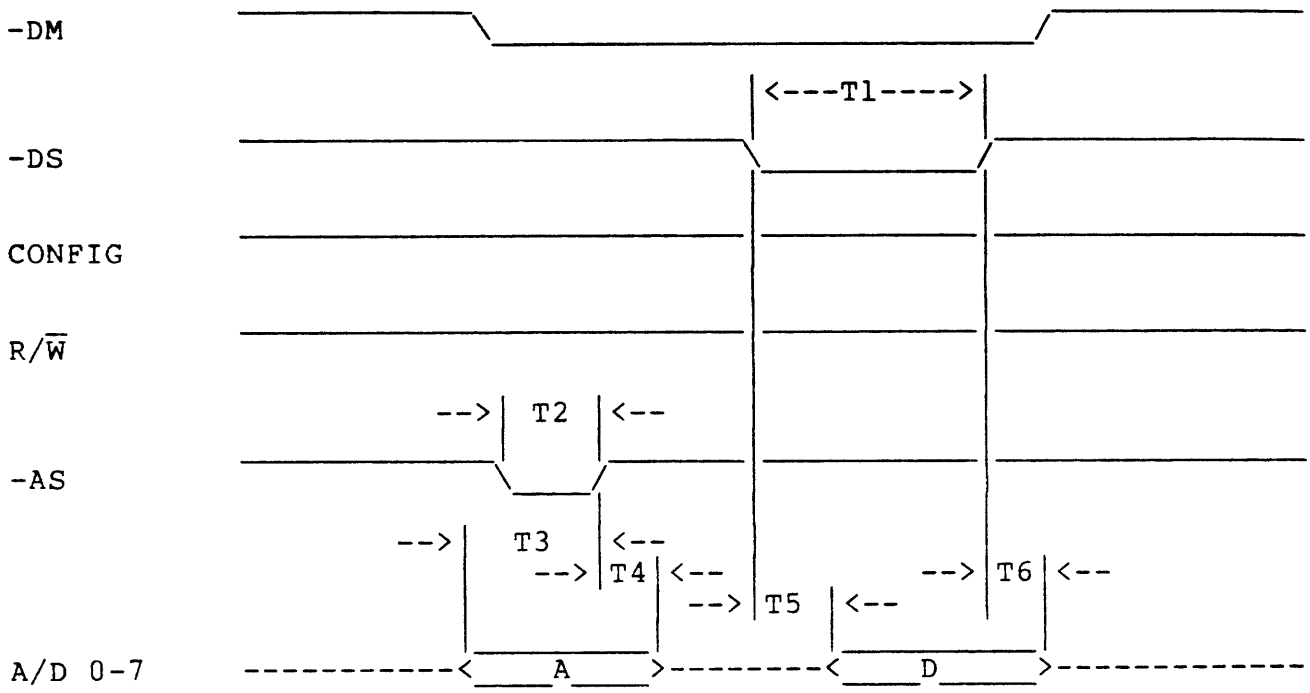


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS High	25			ns
T4	Address Hold after -AS High	25			ns
T5	Data Setup to -DS Low	25			ns
T6	Data Hold after -DS High	25			ns

Read Operation, Z8 Configuration

Signal



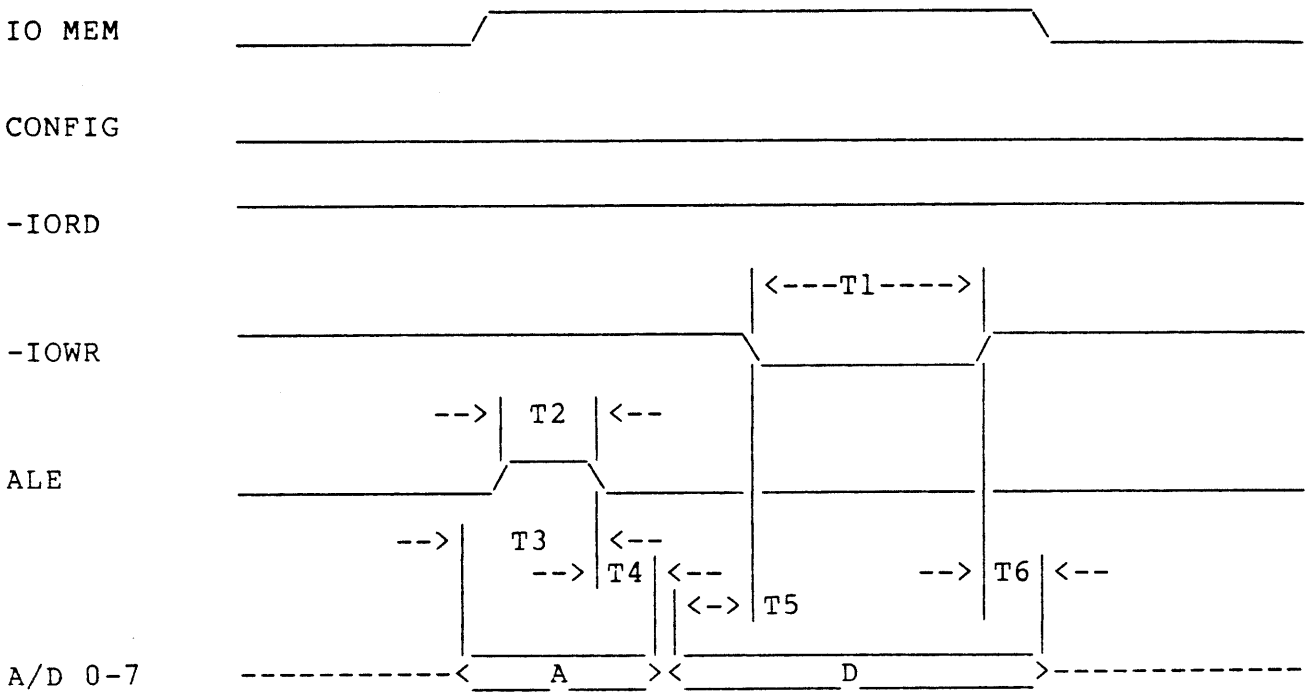
VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-DS Low Pulse Width	100			ns
T2	-AS Low Pulse Width	50			ns
T3	Address Setup to -AS High	25			ns
T4	Address Hold after -AS High	25			ns
T5	Data Valid from -DS Low			50	ns
T6	Data Float after -DS High		35		ns

8051 Mode Timing Characteristics (CONFIG = LOW)

Write Operation, 8051 Configuration

Signal

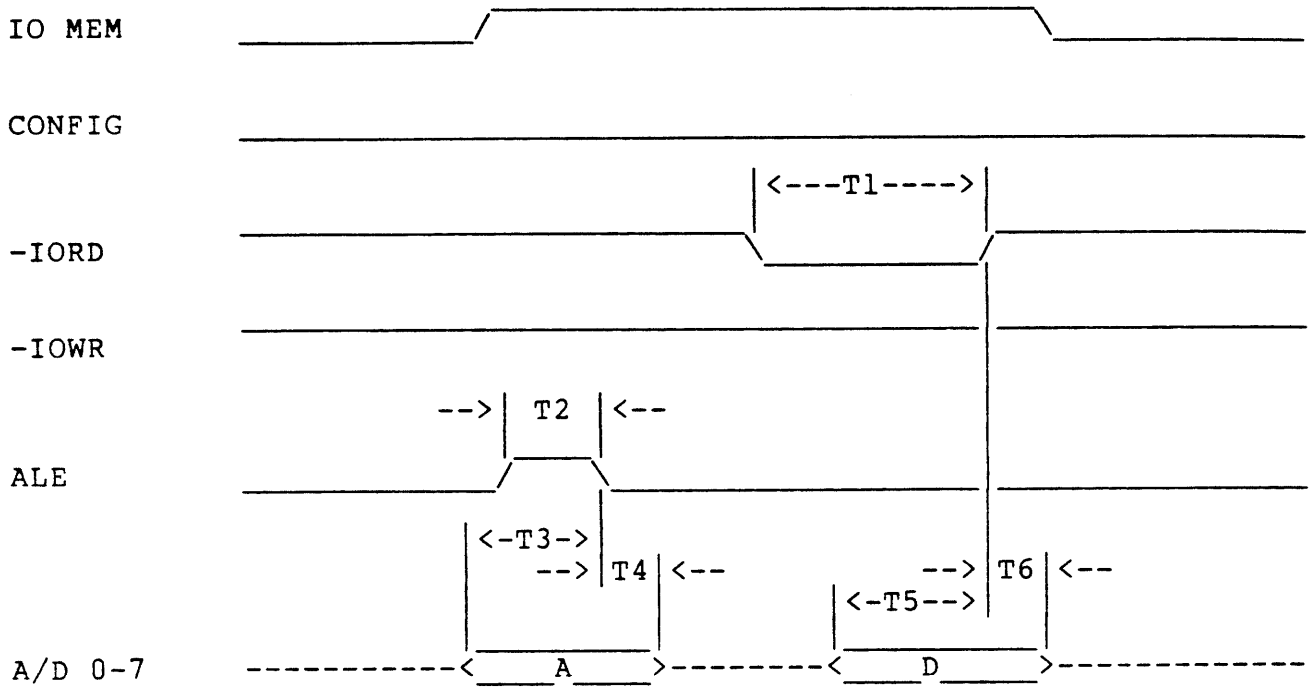


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-IOWR Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE Low	25			ns
T4	Address Hold after ALE Low	25			ns
T5	Data Setup to -IOWR Low	25			ns
T6	Data Hold after -IOWR High	25			ns

Read Operation, 8051 Configuration

Signal

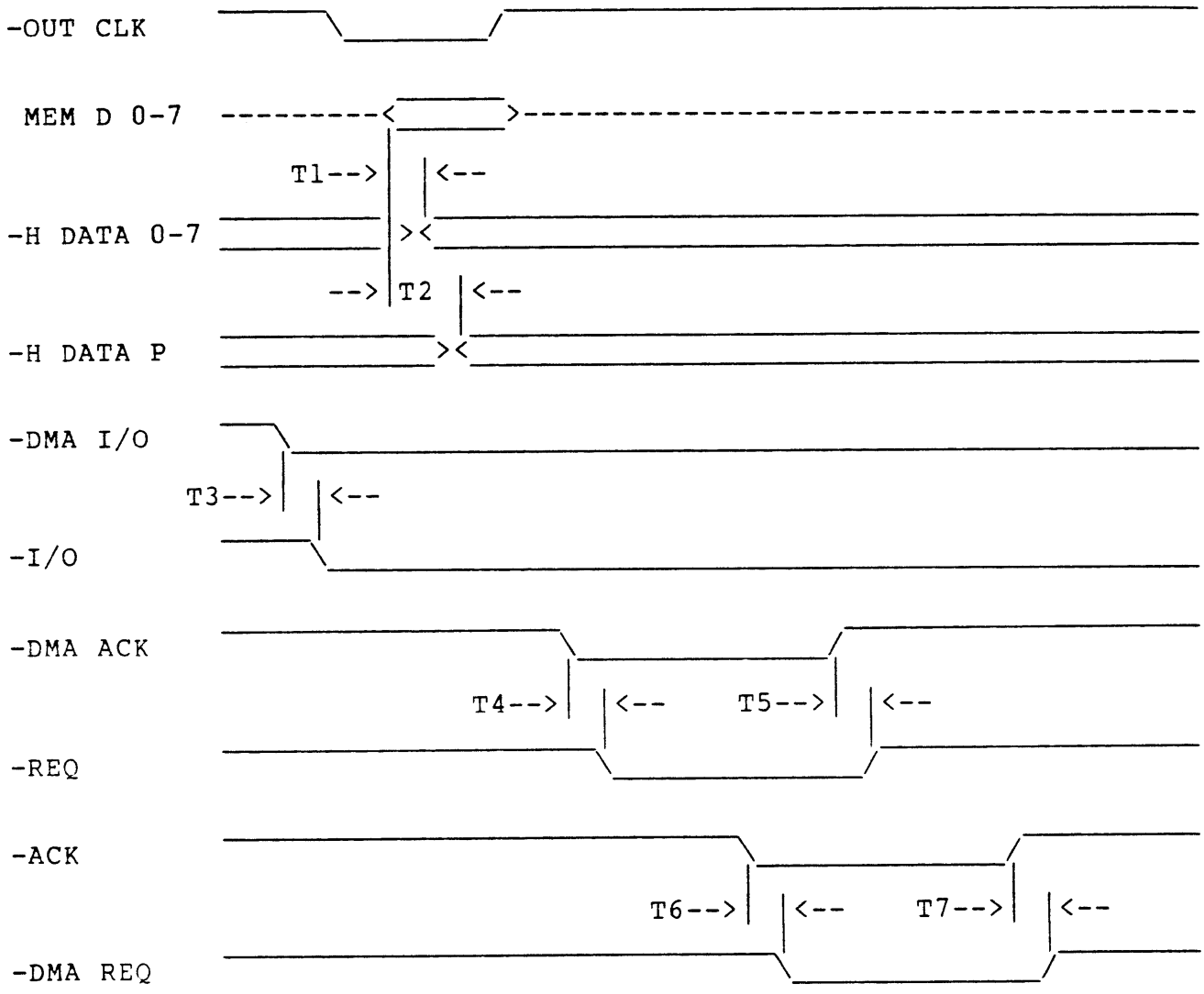


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-IORD Low Pulse Width	100			ns
T2	ALE High Pulse Width	50			ns
T3	Address Setup to ALE Low	25			ns
T4	Address Hold after ALE Low	25			ns
T5	Data Valid from -IORD Low			50	ns
T6	Data Float after -IORD High		35		ns

SCSI TARGET DMA OUT

Signal

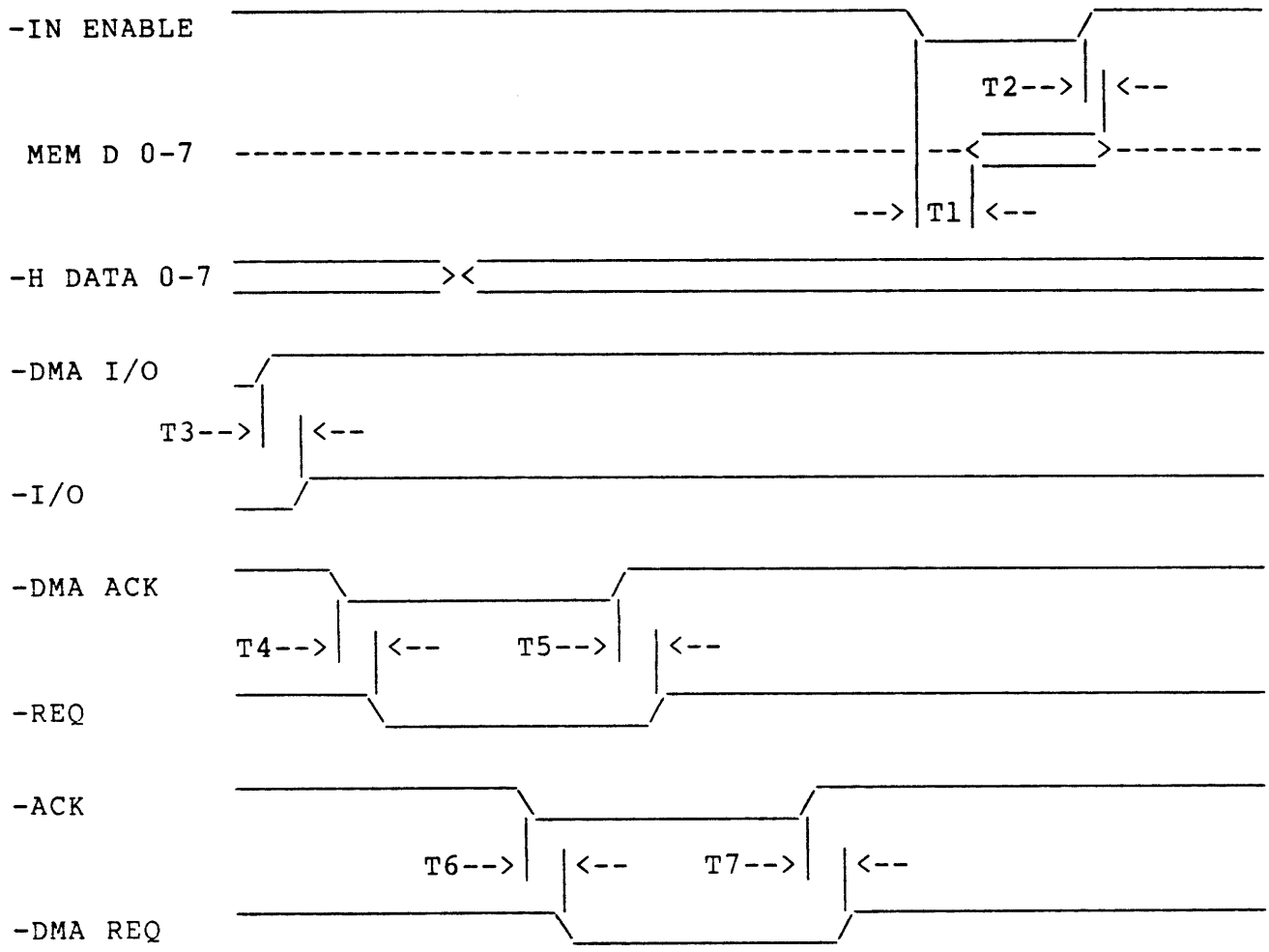


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	MEM D 0-7 valid to -H DATA 0-7 valid		40		ns
T2	MEM D 0-7 valid to -H DATA P valid		46		ns
T3	-DMA I/O to -I/O delay		30		ns
T4	-DMA ACK to -REQ delay		21		ns
T5	-DMA ACK false to -REQ false delay		22		ns
T6	-ACK to -DMA REQ delay		37		ns
T7	-ACK false to -DMA REQ false delay		33		ns

SCSI TARGET DMA IN

Signal

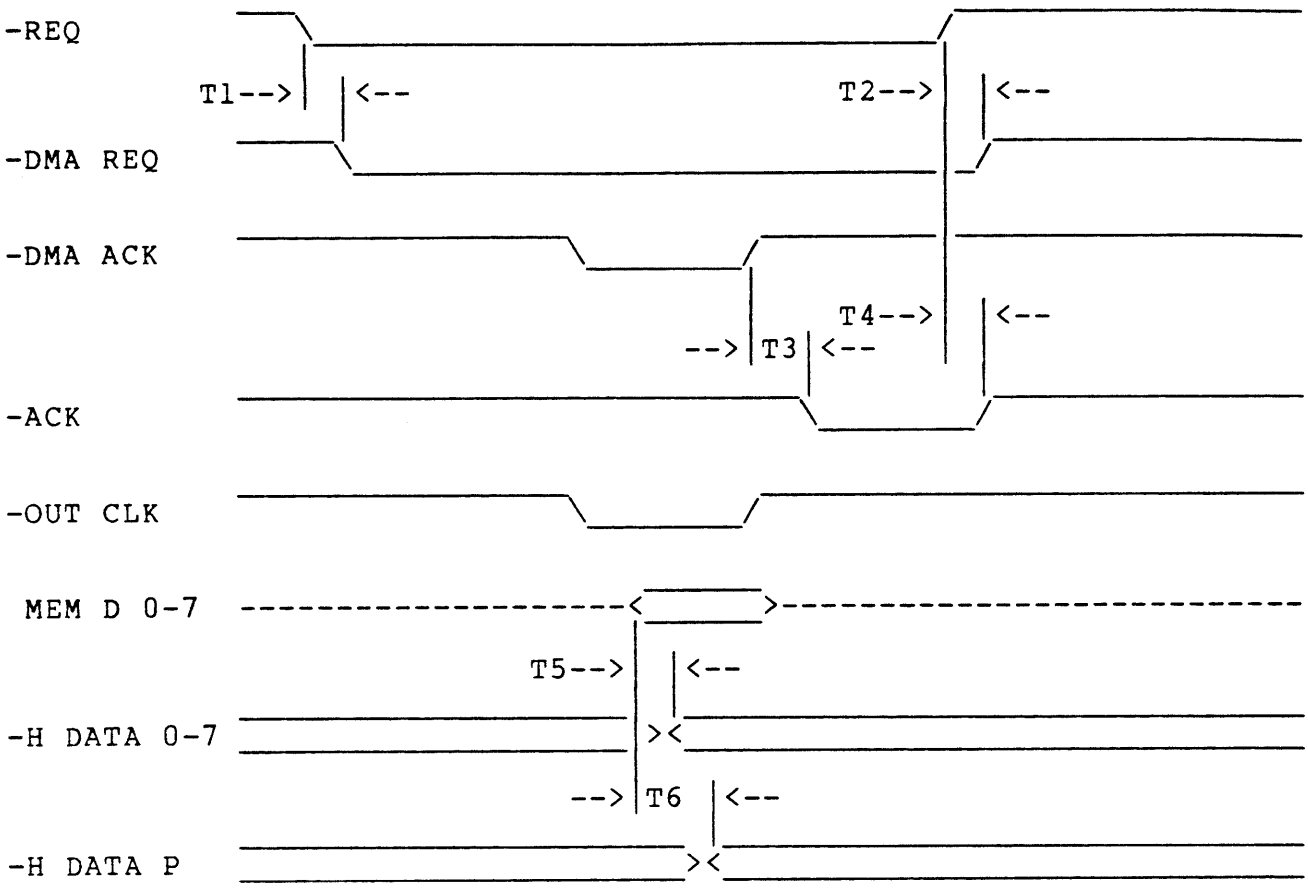


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-IN ENABLE to MEM D 0-7 valid		25		ns
T2	MEM D 0-7 data hold time		20		ns
T3	-DMA I/O to -I/O delay		30		ns
T4	-DMA ACK to -REQ delay		21		ns
T5	-DMA ACK false to -REQ false delay		22		ns
T6	-ACK to -DMA REQ delay		37		ns
T7	-ACK false to -DMA REQ false delay		33		ns

SCSI INITATOR DMA OUT

Signal

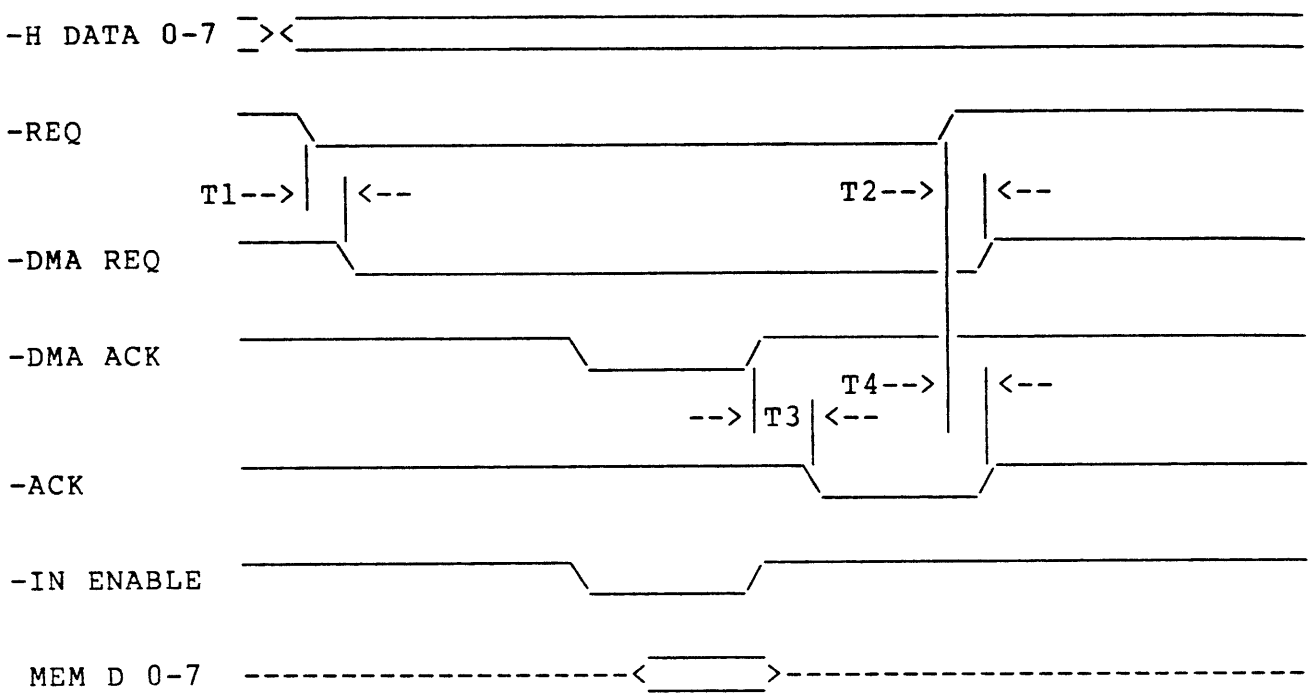


VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-REQ to -DMA REQ delay		31		ns
T2	-REQ false to -DMA REQ false delay		36		ns
T3	-DMA ACK false to -ACK delay		20		ns
T4	-REQ false to -ACK false delay		35		ns
T5	MEM D 0-7 valid to -H DATA 0-7 valid		29		ns
T6	MEM D 0-7 valid to -H DATA P valid		46		ns

SCSI INITATOR DMA IN

Signal



VCC = 5.0V, TA = 25°C

Symbol	Item	Min.	Typ.	Max.	Unit
T1	-REQ to -DMA REQ delay		30		ns
T2	-REQ false to -DMA REQ false delay		36		ns
T3	-DMA ACK false to -ACK delay		19		ns
T4	-REQ false to -ACK false delay		33		ns

Multiplication factors to convert from nominal environment:

Process	+1 std. deviation	1.35
	-1 std. deviation	0.65
Voltage	4.75V	1.06
	5.25V	0.95
Temperature	0°C	0.93
	70°C	1.15

PACKAGE DIMENSIONS

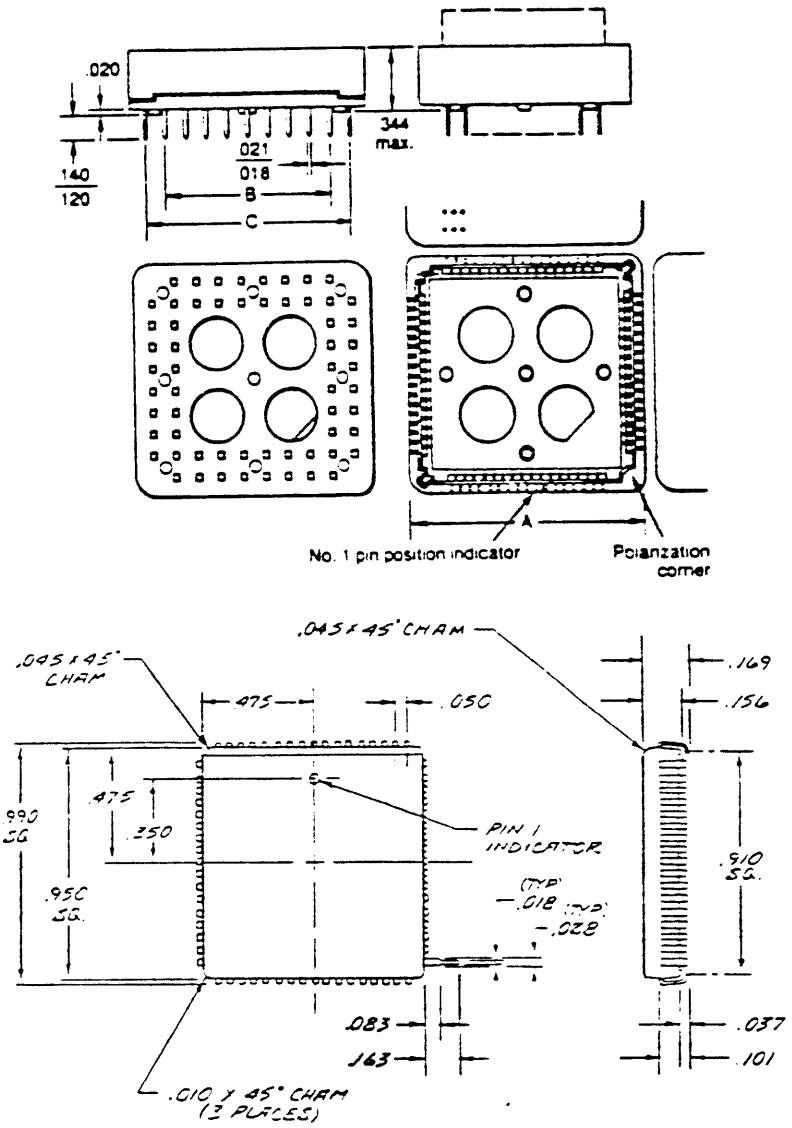


Figure 9. Socket and Package Dimensions

D.C. CHARACTERISTICS

Absolute Maximum Ratings

- Voltage on all pins with respect to GND range from -0.3 to 7.0 Vdc.
- Ambient operating temperature is 0°C to +70°C.
- Storage temperature is from -65°C to +150°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

Standard Test Conditions

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current is into the reference pin. Standard conditions are as follows:

- VCC = 5.0 Vdc +/- 0.25 Vdc.
- GND = 0 Vdc
- 0°C < TA < 70°C

D.C. Characteristics

Parameter	Min	Max	Unit
Input High Voltage	2	VCC	V
Input Low Voltage	-0.3	0.8	V
Output High Voltage	2.4	VCC	V
Output Low Voltage		0.4	V
High-level Output Current		-4	mA
Low-level Output Current		4	mA
Input Leakage	-30	10	uA
Output Leakage		10	uA
VCC Supply Current		50	mA

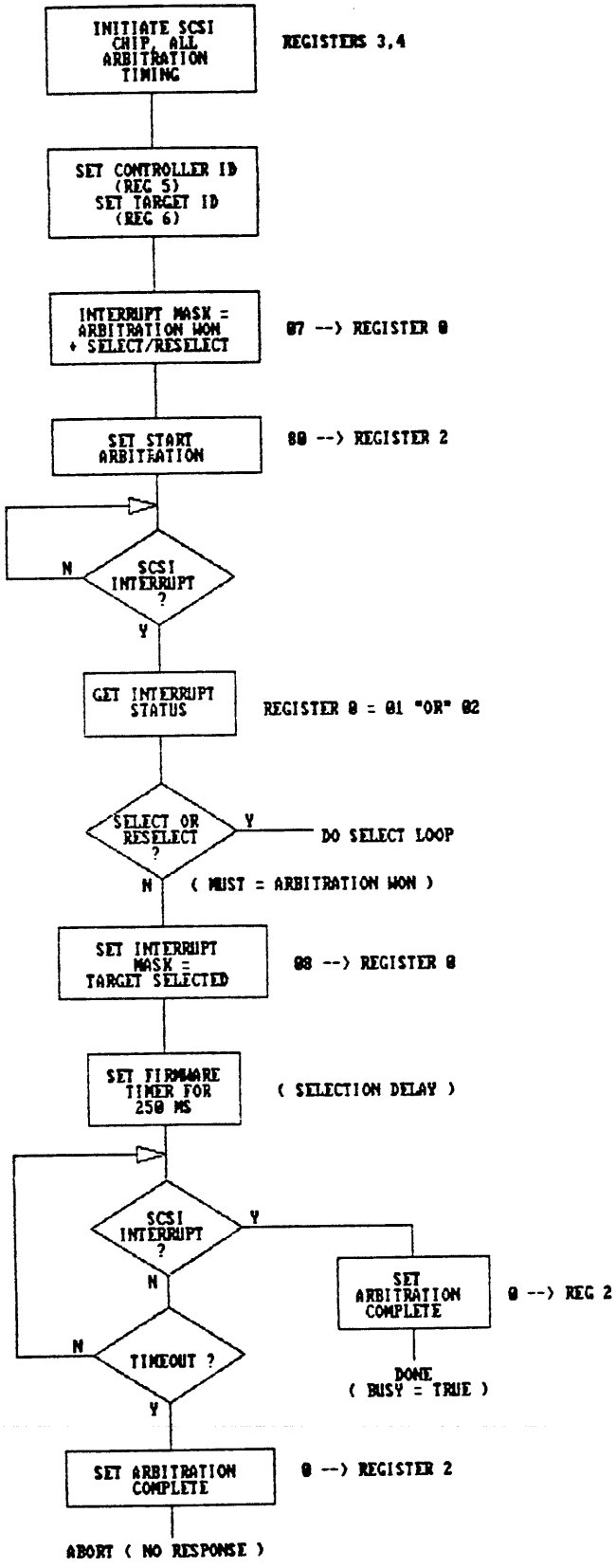
Drivers/Receivers

- Drivers — Sink 48 mA @ 0.5 Vdc asserted
- Receivers — Asserted at input = 0 to 0.8 Vdc
  Nonasserted at input = 2.0 to 5.25 Vdc
  Minimum hysteresis = 0.2 Vdc

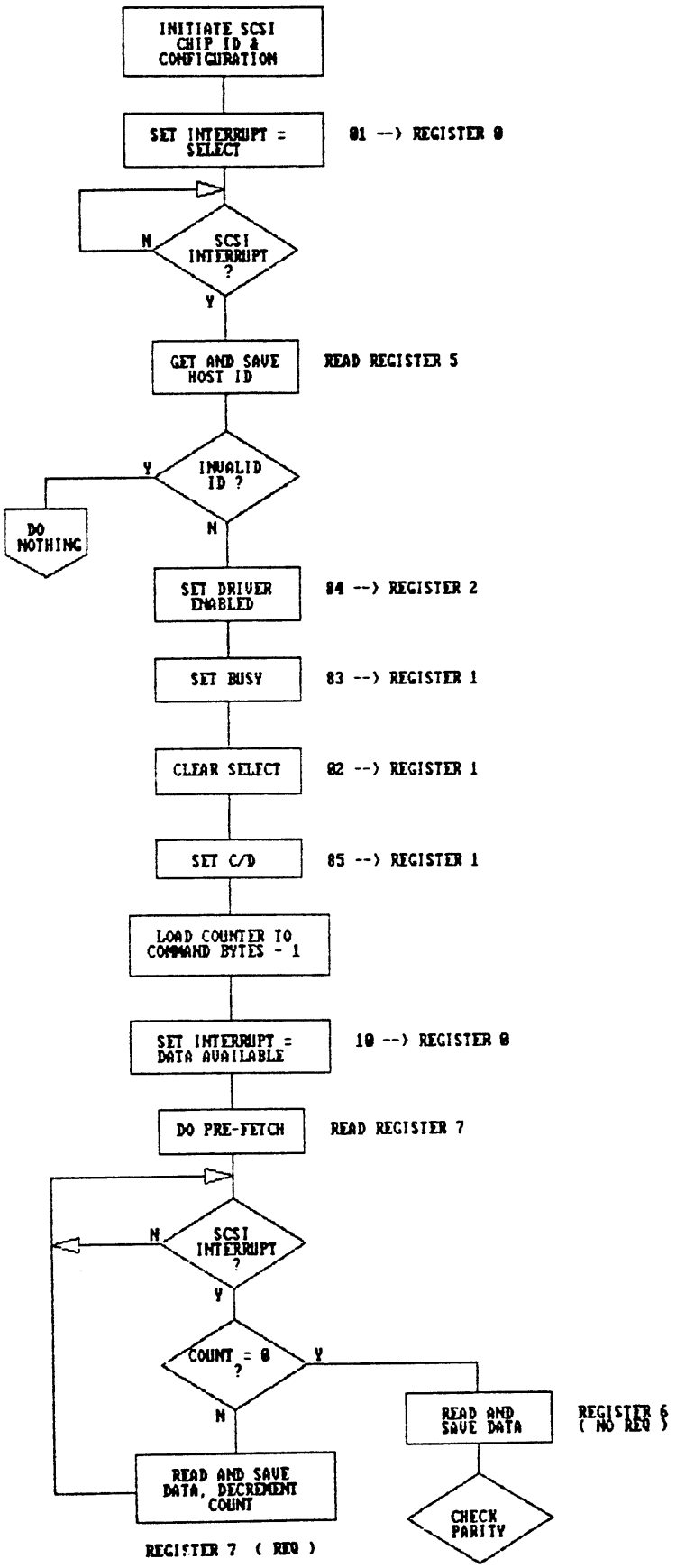
APPENDIX A

SCSI IMPLEMENTATION FLOW CHARTS

ARBITRATE MODE



SELECTION MODE



SEND COMMAND