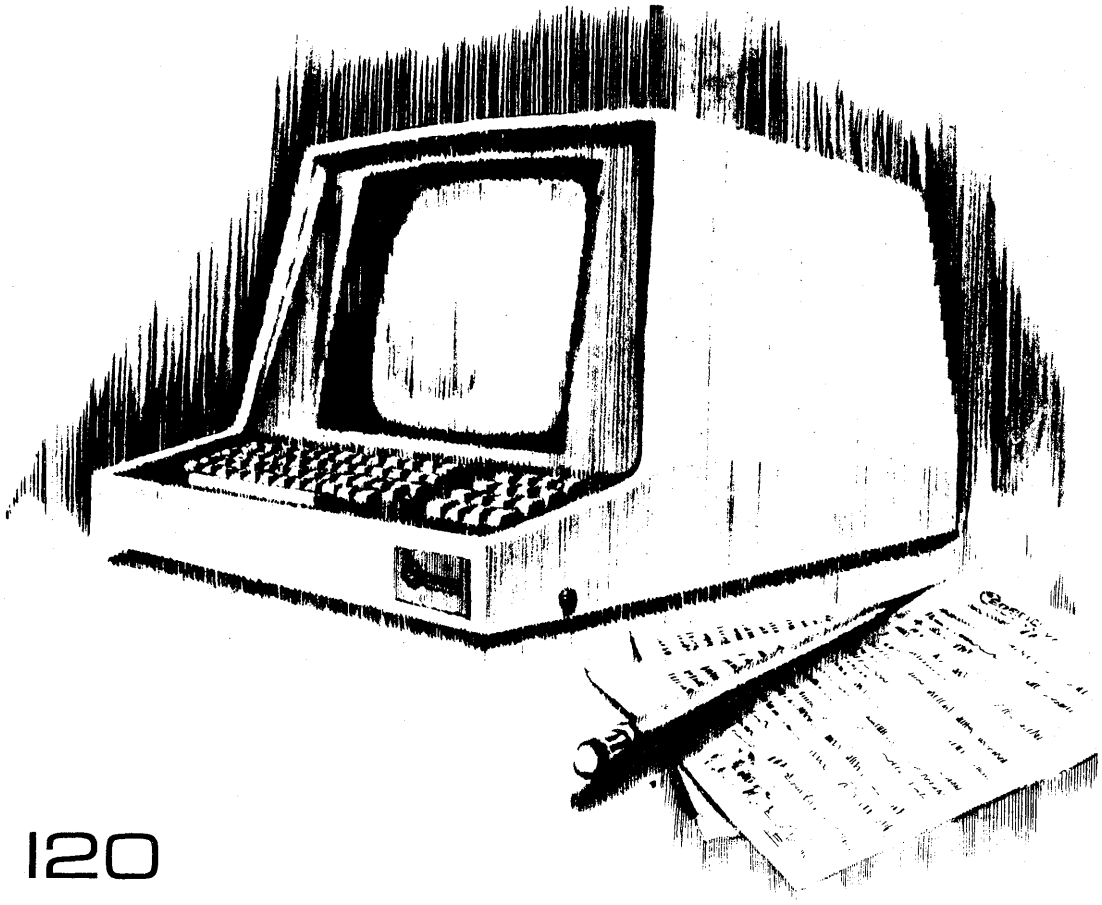
SOROC for '80



IQ 120
DISPLAY TERMINAL
THEORY OF OPERATION
MANUAL

SOROC TECHNOLOGY, INC.

165 FREEDOM AVE., ANAHEIM, CALIF. 92801

WARRANTY

Soroc Technology Incorporated warrants each IQ 120 Video Display Terminal to be free of defects in material and workmanship for a period of 90 days from the date of shipment to the original customer.

Soroc Technology Incorporated will correct any defect in material or workmanship which, in the opinion of Soroc Technology Incorporated, was not caused by improper use or abuse of the terminal for the period of the warranty, when the terminal is returned freight prepaid to the factory in Anaheim, California.

Authorization to return equipment for warranty repair must be obtained from:

Soroc Technology Incorporated
Customer Service
1560 Orangethorpe Way
Anaheim, California 92801
(714) 992-2860

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ANAHIME CA, 92801

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IQ 120 SPECIFICATIONS

1.0. INTRODUCTION

This section describes the specifications for the IQ 120 including operational, physical, and environmental operating characteristics.

I

1.1. DISPLAY FORMAT

1920 characters arranged in 24 horizontal lines of 80 characters per line.

1.2. SCREEN

Rectangular, 12 inches diagonal, P4 phosphor.

1.3. DISPLAY MEMORY

1920 character (8-bit) MOS RAM memory.

1.4. CHARACTER SET

96 characters (includes lower case alphabetic characters.)

1.5. DISPLAY REFRESH RATE

60 hertz, 50 Hz Optional

1.6. CURSOR CONTROL

Forespace, backspace, upline, downline, new line, return, home, tab, and absolute cursor addressing.

1.7. FIELD PROTECTION

Any part or parts of the display can be designated as protected to prevent inadvertent overtyping. Protected fields are displayed as reduced intensity video.

1.8. TRANSMISSION MODES

Standard - Conversation mode (full or half-duplex). Characters are transmitted as they are typed.

Optional - Block mode. Transmit unprotected line or page when commanded.

1.9 KEYBOARD

73 keys including numeric pad and cursor positioning keys.

1.10. EDITING FEATURES

Clear screen, type-over, absolute cursor addressing, erase to end of page, and erase to end of line or field.

1.11 REPEAT

Automatic 15 character per second repeat actuated by pressing any key for one half second or longer.

1.12. PARITY GENERATION

Switch selectable odd, even or none.

1.13. WORD FORMAT

Switch selectable seven or eight data bits with either one or two sop bits.

1.14. INTERFACE

EIA RS-232-C and/or current loop optional.

1.15. DATA RATES

Switch selectable: 75, 110, 150, 300, 600, 1000, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 and 19200.

1.16. DIMENSIONS

12.5" high, 18" wide, 21" deep.

1.17. WEIGHT

45 pounds.

1.18 POWER REQUIREMENTS

115 Vac, 60 Hz, 130 watts. 230 Vac, 50 Hz optional.

1.19. OPERATING ENVIRONMENT

5 to 40^{o} C, 5 to 90% relative humidity (without condensation).

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I.Q. 120 FEATURES

2.1. SELECTABLE TRANSMISSION RATES

To meet the transmission rate requirements of a variety of computer interfaces, telephone data lines and modems, the IQ 120 can operate at data rates of 75, 110, 150, 300, 600, 1000, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, or 19200 baud. The operator can select any speed by means of a switch on the rear of the IQ 120.

2.2. MODES OF OPERATION

2.2.1. CONVERSATION MODE, HALF-DUPLEX. In the half-duplex mode, the IQ 120 can send and receive information to and from the remote computer, in only one direction at a time. Characters are displayed and simultaneously transmitted one character at a time as they are typed at the keyboard. Received characters are displayed as they are received.

2.2.2. CONVERSATION MODE, FULL-DUPLEX. In the full-duplex mode, characters are transmitted as they are typed but are displayed only on reception. Display of characters typed in the full-duplex mode is usually accomplished by the computer or modem echoing the characters back to the IQ 120. Characters may be received and transmitted simultaneously.

2.2.3. ROLL MODE. The IQ 120 is in the roll mode while in full- or half-duplex operation with the display unprotected. Executing a line advance function from the bottom line of the screen causes the entire display to move up one line, leaving a new blank line at the bottom. The top line is lost.

2.2.4. BLOCK MODE. (Optional) In the block mode, information is transmitted and received as complete messages or blocks of data (as opposed to the character-by-character operation in the conversation modes). The operator enters the complete message, up to a full screen in length, and the characters are stored and displayed but are not automatically transmitted. After entering the message, the operator can edit the displayed information and then type a special two code escape sequence which causes all or part of the message to be transmitted. In addition to the edit capability, the block mode provides faster transmission for large blocks of data than the conversation mode. Block mode also permits more efficient utilization of the computer and data transmission lines for many applications.

2.3. MODE SELECTION

A switch on the rear of the IQ 120 allows the operator to select between full-duplex, half-duplex, or block mode.

2.4. THE CURSOR

The cursor is a bright rectangular marker on the IQ 120 screen which indicates the entry point for the next character to be typed. As characters are entered, the cursor automatically moves from left to right across the display. When the cursor is positioned over a character already displayed on the screen, the character appears as a reverse image in the cursor. The cursor can be repositioned from the keyboard of the computer to any unprotected position on the display.

2.4.1. INCREMENTAL CURSOR CONTROL. The cursor can be moved up, down, left or right incrementally from the keyboard or the computer.

2.4.2. ABSOLUTE CURSOR ADDRESSING. The cursor can be positioned using an absolute address which contains the X- and Y-coordinate cursor location from either the keyboard or the computer.

2.5. EDIT CAPABILITIES

The standard IQ 120 allows the following capabilities for information editing:

1. Character type-over
2. Clear unprotected positions to nulls
3. Clear entire screen to nulls
4. Erase from cursor position to end of line/field
5. Erase from cursor position to end of page

2.6. FIELD PROTECTION

Areas on the IQ 120 display can be designated by the

operator or the computer as protected fields. These fields appear at a lower brightness level than the rest of the display and have the following characteristics:

1. Protected areas cannot be typed over unless the terminal is first removed from the protected mode. This prevents inadvertent over-typing.

2. Protected areas cannot be typed over by the computer unless the IQ 120 is first removed from the protected mode.

3. Protected areas are not transmitted by IQ 120.

2.7. IQ 120 KEYBOARD FEATURES

The IQ 120 features a 73 key keyboard (figure 1-1). In addition to the upper and lower case alphanumeric keys, a numeric pad is provided for ease of entering numeric data. Also included on the IQ 120 keyboard are 4 cursor control keys which are provided to take full advantage of the extensive capability of the IQ 120.

An auto repeat feature is provided on the IQ 120 keyboard which provides the capability to automatically repeat any key function other than the escape key at the rate of 15 characters per second without having to depress a separate repeat key. The auto repeat feature becomes effective anytime a key is pressed for longer than one half a second.

3

IQ 120 OPERATION

3.0 INTRODUCTION

This section describes the use of the various keys on the IQ 120 keyboard. The keyboard is shown in Figure 1-1. All key functions except ESCAPE will automatically repeat. All functions may be performed from the keyboard by using the indicated key (or keys) or by the computer by using the indicated ASCII function code.

3.1. HOME KEY

This key causes the cursor to return immediately to the first character position of the first line (called home position). If the IQ 120 is in the protected mode and the home position is a protected character, the cursor will be positioned to the first unprotected position on the screen. This operation may be accomplished with CTRL (36 Octal).

3.2. RETURN KEY

This key causes the cursor to move to the first character position of the present line, or to the first unprotected position of the present line if the IQ 120 is in the protected mode. This operation may be accomplished with CTRL M (15 Octal).

3.3. ← → KEYS

These keys move the cursor in the direction of the arrow. If the IQ 120 is in the protected mode and the adjacent

position in the direction of the arrow is protected, the cursor will skip the entire protected field and stop at the first unprotected position. The forespace (→) and backspace (←) operations may also be accomplished with the CTRL L (014 Octal) and CTRL H (010 Octal) function codes respectively.

3.4. ↑ KEY

This key moves the cursor straight up. If the IQ 120 is in the protected mode and the position directly above the cursor is protected, the cursor will move up and then to the left from that position to the first unprotected position. This operation may also be accomplished with the CTRL K (013 Octal) function code.

3.5. ↓ KEY

This key moves the cursor straight down. If the IQ 120 is in the protected mode and the position directly below the cursor is protected, the cursor will move down and to the right from that position to the first unprotected position. If the cursor is on the bottom line and the display is in unprotected mode, a ROLL operation is accomplished (see section 2.2.3.). If the display is protected, the cursor recycles to the top line. This operation may also be accomplished using the CTRL J (012 Octal) function code.

3.6. TAB KEY

In the protected mode, this key causes the cursor to move to the first unprotected character position following the next protected field. If there are no protected fields

between the cursor and the end of the screen, the cursor goes to home or to the first unprotected position. This operation may also be accomplished using the CTRL I (011 Octal) function code.

3.7. SPACE BAR

Pressing the space bar causes an ASCII space code to be stored in the display memory and a blank space to appear on the screen.

3.8. SHIFT KEY

This key is pressed to type the character marked in the upper portion of the typing key or to select upper case characters if the IQ 120 has the lower case option installed.

3.9. CLR KEY

This key clears the display and stores null codes in the display memory and homes the cursor.

3.10. CTRL KEY

This key, when held down while simultaneously typing another key which generates a transmittable code, causes the bit pattern of the character code to be modified. The control character is transmitted to the computer only in conversation mode and is never stored by the IQ 120. The control function can also be performed by the computer transmitting the indicated ASCII function code.

3.10.1 NEW LINE (CTRL underline) Positions the cursor to the first character position of the next line or the first unprotected position on the line if the IQ 120 is in protected mode. ASCII US code (037 Octal).

3.10.2 BEEP. (CTRL G) Sounds the audible beep in the IQ 120. ASCII BELL code (007 Octal).

3.11. ALPHA KEY

The Alpha key is an alternate action key. When the alpha key is pressed, the keyboard will be locked in the alpha mode until the alpha key is pressed a second time. In the alpha mode, all alphabetical keys on the keyboard are shifted to upper case but all other keys are unaffected. This is a hardwired function and cannot be set by the computer.

3.12. ESC KEY

When the escape key is pressed in full duplex mode, an ASCII escape code (033 Octal) is transmitted to the computer. When the escape key is pressed in half duplex, an ASCII escape code is sent to the computer and causes the next character pressed to be interpreted by the IQ 120 as the second code in one of the escape sequences described below. When the escape key is pressed in block mode, no character is sent to the computer but the next character key pressed is interpreted by the IQ 120 as the second code in an escape sequence. All codes generated by the IQ 120

keyboard and transmitted from the computer are recognized by the terminal as seven-bit USASII codes as shown in table 7-7.

3.13. STANDARD ESCAPE SEQUENCES FEATURES

3.13.1 SET PROTECT MODE (ESC &). This sequence sets the IQ 120 into the protected mode, preventing the cursor from entering any position containing a character previously designated as protected. When an ESC & is issued to the IQ 120, the cursor is moved to the home position. If the home position is protected, the cursor is moved to the first unprotected position after the home position.

3.13.2 RESET PROTECT MODE (ESC '). This sequence sets the IQ 120 into the unprotected mode allowing the cursor to enter and overtype protected areas. The protectable status of previously protected characters is maintained such characters will again become protected when the display is returned to the protected mode.

3.13.3 START WRITE PROTECT (ESC)). This sequence sets the IQ 120 into the write protect mode and designates all characters typed until the end write protect sequence as protectable characters; however these characters are protected only if protect mode (ESC &) is set.

3.13.4 END WRITE PROTECT (ESC (). Removes the IQ 120 from the write protect mode so all characters typed thereafter are unprotected.

3.13.5 LOAD CURSOR (ESC =). The next two characters following the ESC = sequence represent the absolute cursor row and column coordinates respectively. The cursor coordinate ASCII codes are listed in table 7-7.

3.13.6 KEYBOARD ESCAPE CONTROLS

3.13.6.1 DISABLE KEYBOARD (ESC #). Disables the IQ 120 keyboard.

3.13.6.2 ENABLE KEYBOARD (ESC "). Enables the IQ 120 keyboard. (Cannot be entered from keyboard once the keyboard is disabled.) Keyboard can be enabled by pressing the CLR key.

3.13.7 CLEAR OPERATIONS

3.13.7.1 CLEAR DISPLAY TO NULLS (ESC*). Clears entire display to unprotected null codes, and sets unprotected mode.

3.13.7.2 CLEAR UNPROTECTED DISPLAY TO NULLS (ESC +). Stores unprotected nulls in all unprotected locations on the screen. Does not change protect mode. If unprotected mode was set, clears the entire display to nulls.

3.13.7.3 ERASE LINE (ESC T). Clears the unprotected positions from the cursor to the end of the line to nulls. If protected data is on the same line as the cursor, the data from the cursor to the first protected character will be cleared to nulls, and all data beyond the first protected character will remain unchanged.

3.13.7.4 ERASE PAGE (ESC Y). Clears the unprotected positions of the display, storing unprotected nulls in memory

from the cursor to the end of the page.

3.14 STET BLOCK SEND ESCAPE SEQUENCE

3.14.1 SEND LINE (ESC 4). This sequence moves the cursor to the first character position on the line after storing the current cursor position. All unprotected characters from the start of the line except NULLS are transmitted sequentially as the cursor moves forward to its original position. As protected fields are encountered, an ASCII CR (015 Octal) is transmitted to signal the end of the sequence.

3.14.2 SEND PAGE (ESC 5). This sequence moves the cursor to the HOME position after storing the current cursor position. All unprotected characters from the HOME position, except NULLS, are transmitted sequentially as the cursor moves forward to its original position. As protected fields are encountered, as ASCII FS code (034 Octal) is transmitted. An ASCII US code (037 Octal) is transmitted at the end of each line. When the cursor returns to its original position, an ASCII CR code (015 Octal) is transmitted and transmission is terminated.

3.15. AUXILIARY PORT ESCAPE SEQUENCE

3.15.1 AUXILIARY PORT ON (ESC @). Enables data received on the communications interface to be transmitted through the auxiliary port.

3.15.2 AUXILIARY PORT OFF (ESC A). Disables transmission through the auxiliary port.

3.16 OPTIONAL PRINTER PORT ESCAPE SEQUENCE

3.16.1 PRINTER SEND (ESC P). This sequence moves the cursor to the HOME position after storing the current cursor position. All characters, including those that are protected and excepting NULLS, from the HOME position are transmitted sequentially as the cursor moves forward to its original position. The transmission sequence starts by transmitting ASCII CR (015 Octal) and LF (012 Octal) codes, with the CR and LF codes also being transmitted at the end of each line and at the end of transmission.

4

IQ 120 SYSTEM ORGANIZATION

4.1. INTRODUCTION

The IQ 120 is organiz ed into the following major electrical assemblies:

1. Keyborad
2. Logic board
3. Display monitor
4. Transformer, fan, and upper chassis wiring assembly.

The power supply, keyboard, and transformer and fan are shown in figure 4-1 while the logic board is shown in figure 4-2.

4.2 KEYBOARD

The keyboard assembly, key switches, and keyboard encoding logic are mounted on a single printed circuit board as shown in figure 4-1. The keyboard provides the interface between the IQ 120 operator and the other electronic assemblies. When a key is pressed, the keyboard electronics provide the appropriate key code and control signals to the logic board. The keyboard is attached to the main logic board via a sixteen conductor ribbon cable.

4.3. LOGIC BOARD

The logic board contains the control electronics,

memory, character generation circuity, plus the interface electronics to the communications line, the keyborad, and the display monitor.

4.4. POWER REGULATORS

The power supply regulators provide the basic regulated supply voltages used by the keyboard, display monitor, and logic board. It resides on the display monitor PCB.

4.5. DISPLAY MONITOR

The display monitor receives video data and drive signals from the logic board and coverts these signals to dot patterns on the screen.

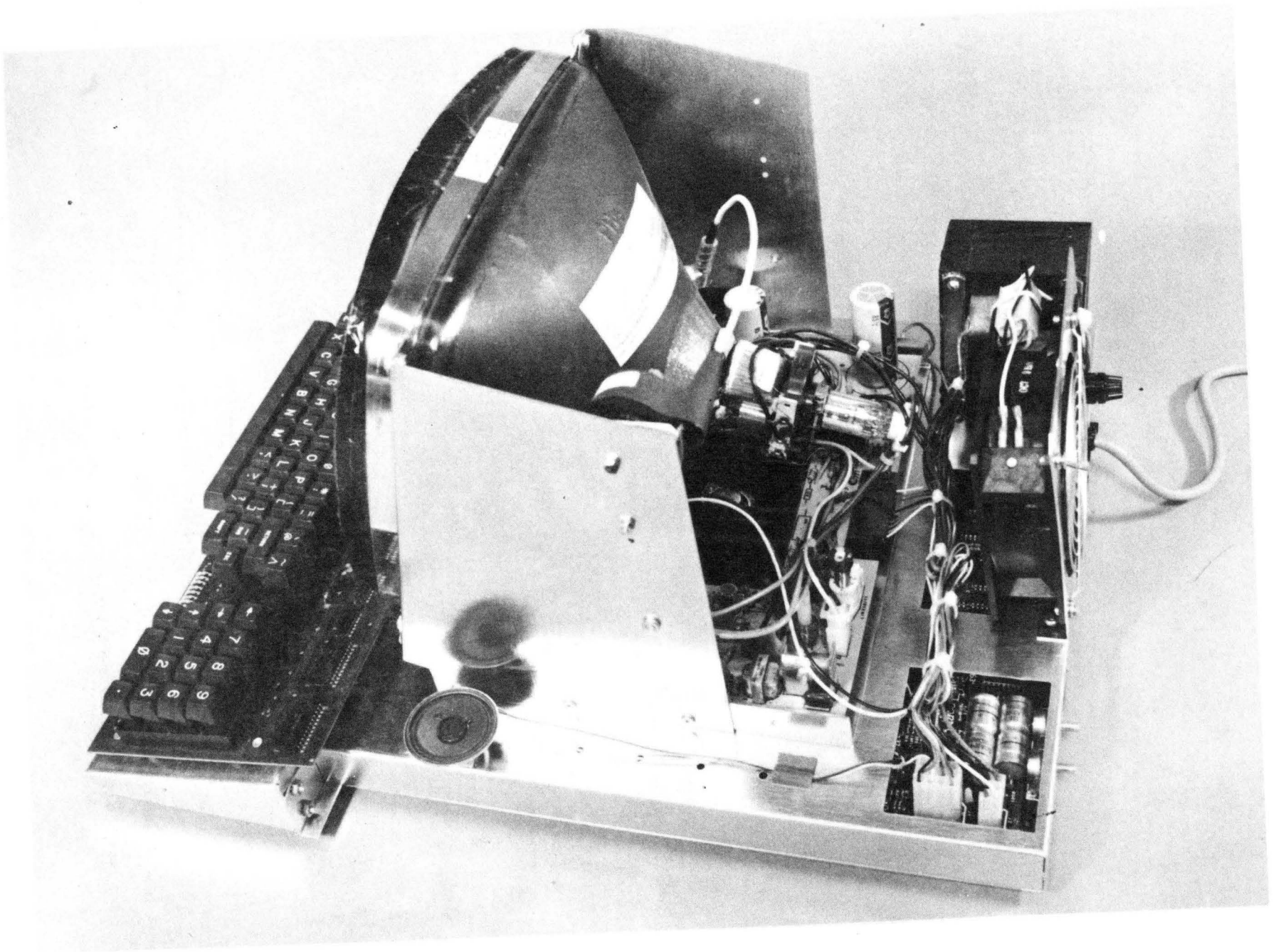
4.6. UPPER CHASSIS

The upper chassis wiring consists of the input voltage wiring, A.C. power distribution, the power supply transformer, the fan, and the interconnecting cabling between subassemblies.

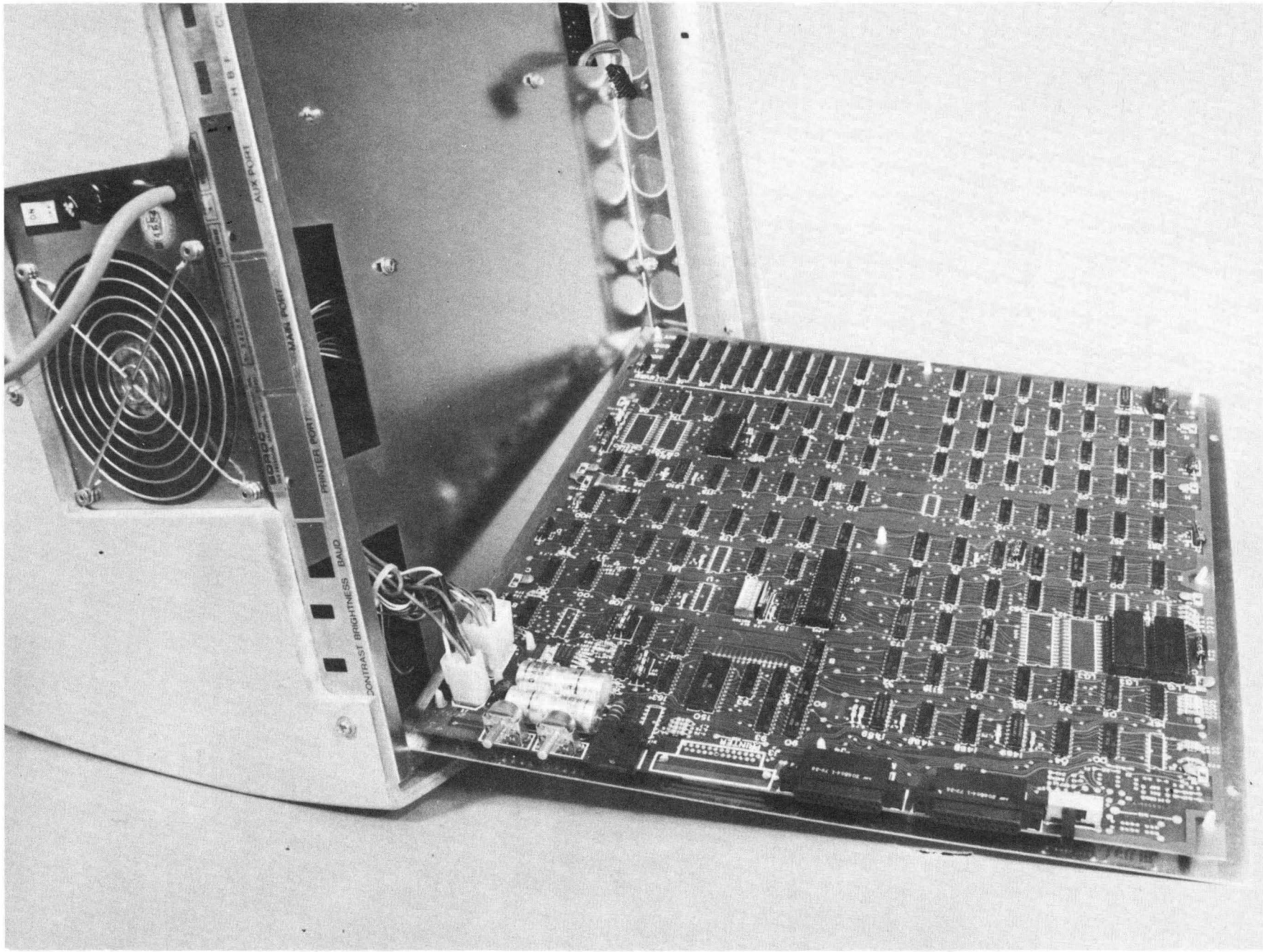
4.7. MECHANICAL CONSTRUCTION

The mechanical assembly of the IQ 120 is shown in exploded view in drawing 100054. The main chassis supports the display monitor assembly, as well as the transformer, fan and the power supply module. The keyboard support chassis is bolted to the front of the main chassis, and supports the keyboard assembly. The logic board is mounted to the basepan by eight snap on plastic hold downs and the basepan is attached to the bottom of the main chassis by four screws.

The fan bracket at the center of the top rear of the main chassis is op riveted to the main chassis and holds the power ON-OFF switch, as well as the fuse holder. The A.C. line cord also enters the unit through a grommet strain relief busing in the fan bracket.



I.Q. 120 TOP CHASSIS



I.Q. 120 DISPLAY LOGIC CIRCUIT BOARD

V

IQ 120 THEORY OF OPERATION

5.1. INTRODUCTION

The following paragraphs describe the electronic operation of the IQ 120 terminal. In reading the Theory of Operation reference should be made to the logic drawings (Dwg. No. 100052) in SECTION 6 of the manual.

Drawing 100049 provides a function block diagram of the IQ 120, showing the various functional circuits, principle inputs and outputs, and the sheet number of drawing 100052 which shows the detailed logic for each block. Each of the blocks shown on drawing 100049 is described in the following paragraphs in sheet order sequence.

5.2. KEYBOARD INTERFACE

The keyboard interface is shown on logic sheet #1. The purpose of the keyboard interface is to accomplish the operations indicated by the signal lines from the keyboard. The interface also synchronizes the keyboard strobe to prevent interaction with the internal operation of the IQ 120. The keyboard connector is a 16 pin IC socket located in the lower left hand corner of the main logic board (location L1).

5.2.1. DATA INPUTS. The data inputs from the keyboard consist of seven lines, labeled KB IN 1 through KB IN 7 (zone 1B4), located on pins L1-9 through 15, respectively. These lines carry "true" data (logic 1 = +5 vdc) and reflect the ASCII code associated

with any key pressed on the keyboard. The input code is presented statically, that is, the ASCII code appears on these lines as long as the key is pressed. These seven keyboard data lines enter the display logic through two 3-state, 2 to 1 multiplexers (74LS257, locations F1 and F2, zone 1B3). The other set of inputs to these multiplexers are the refresh memory outputs. The selected set of data lines are enabled on the system bus for further distribution.

5.2.2. DATA PATH SELECTION. Keyboard data is gated onto the system bus only when the display is refreshing the CRT and the processor is halted. This is done to give the processor the maxium operating time. The keyboard is therefore enabled onto the system bus during the first 64 character times of the lowest visible raster scan of every character line. This is accomplished with two gates. Three input NAND gate H10 (7410, zone 1A2) is labeled KB OUT EN-, has two inputs to control the data line enable. The first SCREEN REFRESH, places the signal in the bisible portion of every raster line. The second, CHC CARRY, selects the lowest visible raster scan of every character line. Therefore, the data is gated to the system bus for the full 80 character times of the selected character scan. However, EN KB IN (NAND gate H3 zone 1C3) only allows the keyboard strobe (KEYSTROBE) to be detected during the first 64 character times of the selected raster line. NO ESC (NAND F5 zone 1A2) is used to control the operation of the ESC (escape) key on the keyboard. If the ESC caode is received at the keyboard interface without the SHIFT control line being active (SHIFT, L2-2, 3 low), the strobe generation is inhibited and no operation is performed. The decoding of the ESC code is done by AND gates F3 and F4 (zone 1A3). The standard IQ 120 keyboard has jumper options

with which the keyboard can be made to operate in either mode. That is, the automatic activation of the SHIFT line when the ESC key is pressed or separate and simultaneous pressing of the ESC and SHIFT keys. (SEE KEYBOARD OPTIONS)

5.2.3. KEYBOARD STROBE CIRCUIT. The purpose of the keyboard strobe circuit is to take the keystrobe from the keyboard, which is asynchronous with respect to the system operations, and generate a synchronized load pulse for the UART transmitter circuit. KEY-STROBE from the IQ 120 keyboard is a level input in that it remains active (hgih) for as long as any key is held depressed by the operator. This signal enters the keyboard interface circuit on pin 6 of the keyboard connector (location L1, zone 1C4). 3 input NAND gate K3 (zone 1C3) is the main controlling gate for keyboard strobe generation. The KEYSTROBE from the keyboard is sensed on pin 1. Gate F4 will inhibit generation of KBUDART- if KD DISABLE is high. This is from a processor-controlled flip-flop that inhibits keyboard operation when high. If all of the previously described conditions are met, output F4-8 will go low. Once all conditions are met, flip flops K1-5 and K1-9 are ready to be activated. When output K1-6 goes low, keyboard load UART (KD LD UART_) from NAND gate K2 (zone 1C1) goes low. This is the load pulse for the UART transmitter. One CPC1 clock time later, output K1-9 goes low setting KB LD UART- high.

These two flip-flops are then locked in this state until the key is released and KEYSTROBE from the keyboard goes low. At this time flip-flops clock back to their set state awaiting the next rise of

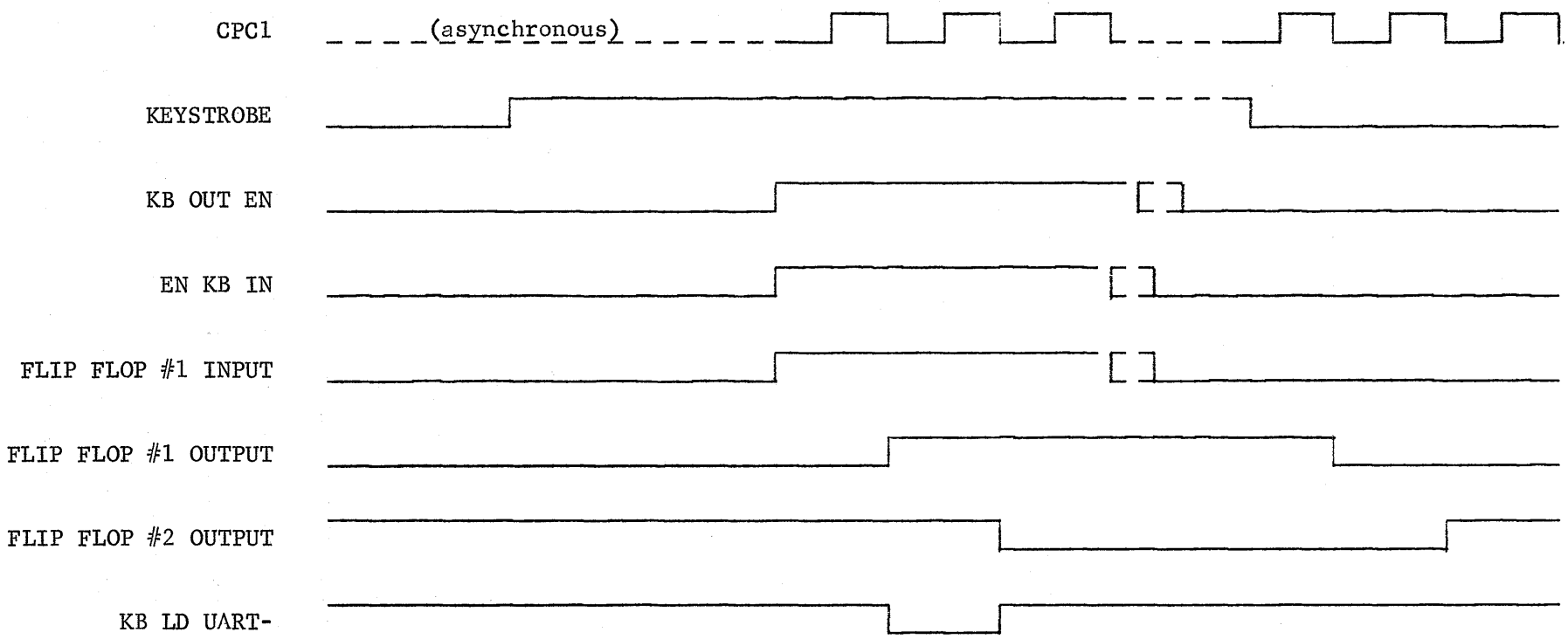


Fig.5-1 KEYBOARD LOADING UART

KEYSTROBE. Repeating is accomplished by the signal line labeled REPT (zone 164) from the keyboard on L1-7. If this signal is high, a 15 Hz repeat clock (REPT CLK, zone 1C4) is enabled into the keystrobe circuit and generates REPEAT STROBE from NAND gate K2-6 (zone 1C3). REPEAT STROBE clears the latched flip-flops each time it goes low and allows CPC1 to generate a transmitter loading pulse (KB LD UART) when it goes high. This will repeat until the key on the keyboard is released.

5.2.4. KEYBOARD CONTROL SIGNALS. The first control line is called BREAK and enters the keyboard interface on pin 4 (zone 1D4) of the keyboard connector (L1). This signal is the output of the BREAK key and is used primarily to drive the RS-232-C TRANSMITTED DATA line to a "spacing" state which the computer can interpret in various ways. A BREAK is also generated during a KBCLEAR at K2-3 (zone1D2). The last two control signals from the keyboard are CTRL and SHIFT. These have no other purpose in this interface than to generate a hardware clear of the IQ 120. All encoding functions of these lines are accomplished on the keyboard and are part of the data on the KB in lines. If the clear key, or optional, the CLEAR and SHIFT, go high sinultaneously, keyboard clear (KB CLEAR-) from RELIEVER (L2-11 zone 1D3) goes low. This signal asynchronously clears the repeat clock B1 (zone 1D3) and the clear flip-flop B6 (zone 1D2). This initiates a CLEAR operation. The operation will start when the KB CLEAR- signal goes high (CLR key released). The flip-flop is already indicating a CLEAR to the display hardwar- by the preset (B6-10) input being low. The counter B1 now starts counting CLC16 pulses which have a duration of 16.667 milliseconds.

Therefore, CLEAR will be active (CLEAR high, CLEAR- and CLR-low) to the display until the "QB" output of counter B1 goes high. At this time, the CLEAR flip-flop will be clocked by DPC8 and the system is ready to run. When this counter is not being used for the CLEAR timimg, it runs continuously and generates the clock for the keyboard repeat operation (REPT CLK). When power is first applied to the system, capacitor C22 (zone 1D3) will be discharged making KB CLEAR-low. This sets flip-flop B6, initiating a clear operation. When C22 is charged through R12, DB CLEAR- goes high, allowing flip-flop B6 to be reset by REPT CLK and DPC8, and normal IQ 120 operation can commence.

5.3 PROGRAMMABLE LOGIC ARRAYS

The PROGRAMMABLE LOGIC ARRAYS provide the IQ 120 with the ability to make decisions which effect the sequencing of the program. The PLA listing is shown in the back of this manual.

5.3.1. PROGRAMMABLE LOGIC ARRAY INPUTS. The programmable logic array (PLA) (Dwg. No. 100052 sheet 2) used in the IQ 120 has 14 inputs from which it can make decisions. Six of these imputs have signals which are always present regardless of the mode in which IQ 120 is operating. The remaining eight inputs use two input multiplexers C5 and D5 (2A3 and 2B3) to switch input signals depending on the operating made. The IQ 120 has two operating modes (called Mode 0 and 'Mode 1). Mode 0 is the mode in which the display awaits for a command from the computer or keyboard and is also called the "idling" mode. During this time the source of the bus data is the receiver; therefore the unit waits until a byte of data is assembled in the receiver and presented to the bus on BUS 1 through BUS 7.

The presence of a non-zero word on the bus indicates to the PLA that it has to decode this non-zero word and determine if it is a byte to write into the refresh memory, a legal action control byte, or a non-decodable control code. The five inputs labeled DEQ1 through SEQ4 from counter D6 (2C3) are used by the PLA to properly sequence the program and provide a means by which the program can be looped. SEQUENCE COUNTER D6 (2C3) automatically increments on every system strobe (ST2-) unless it is told to load a constant from the PLA outputs or to clear unconditionally. The loading from the PLA outputs (PLA 01 thru PLA 04) is the means by which program jumps are accomplished. The clearing of counter D6 occurs on system clearing (CLEAR high) or when the program moves between modes when loading the operation counter (LD OPN). The movement from Mode 1 to Mode 0 is accomplished when the command GO TO M0 is issued. Therefore, the SEQUENCE COUNTER is synchronously cleared when the output D14-12 (7427, zone 2C3) is asserted. The final stage of the sequence counter is located in the first stage of a separate counter (74163, location B4, zone 2B2). Normally, this stage, DEQ5, is set by the carry from the SEQUENCE COUNTER (SEQ CARRY high) and is not preset by the PLA. This stage also clears on the movement from Mode 1 to Mode 0 (GO TO M0). The first four sequence counts, SEQ1 through SEQ4, are used in both operating modes to sequence the program; however, DEQ5 is presented as an input to the PLA only in the idling mode (Mode 0).

Another input that is always present at the PLA input is called ILLEGAL (PLA pin 2, zone 2C3). The purpose of this input is to indicate the status of the registers used to address the refresh memory. When the address registers are set to a location in

memory that is part of the displayable portion (character position less than 80, character line less than 24) this signal is low; however, if the position is addressing 80 or greater, or the line is addressing 24 or greater, this signal is high indicating to the PLA that the cursor is "illegal". In this manner, the PLA knows when a line or page operation is complete. Pin 27 of the PLA holds the signal that tells the PLA which mode is presently active. This is used for proper interpretation of the eight variable input pins: 3,4,5,6,7,8,9 and 26. Seven of these inputs (3,4,5,6,7,8 and 9) in Mode 0 are the seven BUS lines used for decoding input bytes. Therefore, actual data can only be decoded in Mode 0.

After the PLA receives a byte from the bus, the mode shifts from Mode 0 (the idling mode) to Mode 1 (the operational mode). This mode is the operational mode because it is entered when the PLA has determined which operation is to be performed. Some of the operations designated are major-type operations such as CLEAR TO END OF PAGE and SKIP. Other operations are designated for purely internal-type operations such as FORWARD PROTECT TEST, which tests to see if the memory location under the cursor is protected and moves the cursor forward out of the protected field. The desired operation is selected on the move from Mode 0 to Mode 1 by presetting a specific 4 bit constant into a register called the OPERATION REGISTER (74163, location C6, zone 2D2). Its four outputs, OPN1 through OPN4, are sent to PLA inputs 6.5.4.3 via the multiplexer (74157, zone 2B3, location C5) when Mode 1 is active. The only control the program has over the OPERATION REGISTER is the ability to preset it to a specific count by the application of

the PLA outputs PLA 01 through PLA 04 to the A,B,C, and D inputs of C6. The hardware CLEAR circuit clears this register to zero. The is done to accomplish the clearing of the refresh memory on power up since Mode=1, OPN=0 is designated as the CLEAR TO END OF PAGE operation.

The four remaining inputs to the PLA for Mode 1 give specific display-type information to the PLA. The first of these is PROT MODE (input D5-11, zone 2A4). This is the output of a program-controlled latch which indicates to the PLA to interpret those locations in memory containing bit 8 as being protected (ny means of PROT BIT). The next input is SYNC XMTR BUSY (input D5-5, zone 2A4). This input is used during block-type transmissions from the terminal to the computer or printer. It indicates to the program that a character is presently resident in the transmitter register and the program should wait until this signal goes low before loading another character for treansmission. PROT BIT is a PLA input (D5-14, zone 2A4) which indicates that the cursor is on a character that is protected and that it whould not be changed. The last Mode 1 input is COND (input D5-2, zone 2B4). This term is entirely program controlled and interpreted. That is, there are no hardware implications in setting or clearing this latch.

5.3.2. PROGRAMMABLE LOGIC ARRAY OUTPUTS. The outputs of the PLA's installed are all in parallel. The output word consists of 8 bits that are decoded to do two basic types of operations. First, if PLA 08 (PLA pin 10, zone 2C3) is low, the operation is to load a 4 bit constant into some register in the system. The selection of the destination register is accomplished by 1 of 8 decoder E3 (7442, location E3, zone 2C2). Note that if PLA 08 is low, then PLA

08 is low, then PLA 07, PLA 06, and PLA 05 are decoded by E3 to select the destination. The four bit constant to be loaded is then on the four remaining PLA output bits, PLA 01 through PLA 04. A register of this type is located in B4 (zone 2B2). The one output SEQ5, was described in the previous paragraph. The remaining three outputs are used when the print and block transmit PLA is intalled. PRINT and ENB BLK XMT outputs have hardware implications while COND is only sensed by the program. This register is cleared when the display is initialized (when the power first is turned on), the CLEAR key is pressed on the keyboard, or on the transition from Mode 1 to Mode 0.

Gate A2 provides a means of dissabling the PLA's for testing purposes.

5.4 PLA OPERATION DECODERS

Logic sheet 3 shows the manner in which the 8 bit output of the PLA is decoded to accomplish the many operations used to control the IQ 120. In the previous section, it was described how constants are entered into the processor system. The operation decoded on sheet 3 involve those elements that require just one pulse to accomplish a task, such as incrementing a counter, clearing a register, etc. These operations are identified in the output word by having the most significant bit, PLA 08 high. The remaining seven bits, PLA 01 through PLA 07, are then used to determine the specific operation. This type output word is further configured to allow the issuing of two commands sinultaneously. Notice that there are four, 1 of 8 decoders (7442's, location E4, E6, E7 and E8). Once enabled, each decoder requires only three bits to make the final identification. Therefore, PLA 07 is used to select

a pair of decoders (E4-E6 or E7-E8), PLA 06 throught PLA 04 select from eight different operations from 4 or E8, and PLA 03 through PLA 01 another eight operations from E6 or E7. The operations were placed on these decoders to make use of this ability to issue two commands simultaneously. If PLA 07 is low, then gates E1-6 (zone 3C3) and E1-12 (zone 3B2) are disabled and PLA 07- (zone 3B3) goes high. This signal then enables gates E1-8 (zone 3B3) and E2-6 (zone 3C2); therefore, in this situation, decoders E7 (zone 3B3) and E8 (zone 3C1) will provide the output pulses. At this time, note that a decode of 7 on each decoder is designated NOP (no operation). This is used in the event that only a single operation is desired. The unused decoder is then presented with a decode of 7. If PLA 07 is high, then decoders E4 (zone 3C3) and E6 (zone 3B1) are active. The paired decoders also put out different types of output. The presence of the system strove in the gates driving decoders E4 and E7 limits the output to the width of STI. Therefore, these two decoders have outputs that are only 91.8 nsec wide. The latter pulse is used in situations where an enabler type term is required.

Decoder E4 (zone 3C3) is used to control the cursor registers which address the memory and provide the cursor on the display. These registers can be incremented, (INCR), decremented (DECR), and loaded from the system bus (LOAD). CURL is the register that determines which character line contains the cursor and CURP which character position on that line. The only command from the decoder not associated with the cursor registers is LOAD BCUR-. This command is used to save the contents of the cursor register in

another register called the BUFFERED CURSOR REGISTER. This command simultaneously saves both CURP and CURL.

Decoder E7 (7442, zone 3B3) is used for an assortment of commands that require an output the width of the system strobe (91.8 nsec). DECR BCURL- and DECR BCURP- are used to individually decrement the count stored in the BUFFER CURSOR REGISTERS. That is, the stored line count can be decremented without affecting the stored position count. These commands are used primarily to return the cursor to its original cursor location after moving it for an editing operation and to terminate a block-type send operation at the original cursor location. SET BEEP- is issued when an ASCII BEL code is received from the line. This activates the beeper circuit. PRINT TIMER- is used when the printer attached to the printer port requires a set time delay following the issueing of a carriage return/line feed sequence. DECR CURP2 is a command that affects the CURSOR POSITION REGISTER. It is used when the cursor is being moved backward and is decremented from the first position of the line. DECR CURP2 allows a quick movement to a decode of 79 which is the last position of the line. INCR ROLL is used when the display has to roll the entire screen up one character line.

Decoder E8 (7442, zone 3C1) is used primarily to control the status latches. SET/CLR MODE- are commands issued when the appropriate ESC sequences are received by the IQ 120. The protect mode flip-flop, when set, tells the display to protect all data bytes in the refresh memory that have bit 8 high. If bit 8 is low, all data in the refresh memory is considered unprotected. SET/CLR KB DIS- are commands that are used to control imput from the keyboard. When the keyboard disable flip-flop is set, the keyboard interface

circuit is unable to see the keystrobe from the keyboard. This flip-flop is also controlled by ESC sequences from the computer by means of the bus and PLAs. SET/CKR WRITE PROT- are commands which determine whether incoming data will be tagged with bit 8 high when it is written into the refresh memory. If it is set, bit 8 will be written high until the write protect flip-flop is reset.

The last operation output out of this decoder is GO TO M0. This command is issued by the program when a Mode 1 operation is completed and the unit is ready to idle again in Mode 0. This command initializes the operational circuits. All outputs out of this decoder (7442, location E8, zone 3C1) are one instruction time wide (approx.640 nsec).

Decoder E6 (7442, zone 3B1) also provides 640 nsec output pulses. The first output from this decoder is CLR BCURL-. This is used to clear the stored line address in the VUFFERED CURSOR LINE register without affecting the BUFFERED CURSOR POSITION register. This command is used when the cursor has to be moved on a line oriented editing operation. LOAD UART EN- is a command that is issued when the bus holds a data byte to be transmitted to the computer or the printer. It is the load pulse to the UART transmitter. CLR BFR EN- is used when the buffer that accepts data from the UART receiver needs to be cleared. This command is issued primarily when a sequence operation is decoded. Once the lead-in code has been decoded, the input buffer is cleared and the unit waits for the next non-zero input. This prevents the sequence code from being written into the display memory. CLR CURL EN- and CLR CURP EN- are commands used to take the cursor to the first position of the line (CLR CURP EN-) or to the top line of the display (CLR CURL EN-).

When a data byte is resident on the system bus, issuing WRITE EN- will cause that information to be written into the refresh memory at a location determined by the contents of the cursor line and position registers.

5.4.1. BUS SOURCE SELECTION. This circuit determines which register will be the source of data onto the system bus. When selected, a source remains on the bus until another source is identified. This circuit consists of register (74163, location D4, zone 3B3) and decoder (7442, location D3, zone 3B2). The register (D4) is loaded with a constant which is then decoded to identify the bus source. The three least significant bits of the register are the source identification. The most significant bit (PLA 04) is actually a refresh control. If this bit is high, refreshing of information to the display is inhibited to allow more operating time to the program which speeds up the current operation. This signal is called CLR SCREEN (output D4-11, zone 3B3). The first decoder (D3) output enables the input buffer from the UART to the bus. This is called EN BFR OUT- and is a decode of 0. A decode of 2 places the output of the refresh memory onto the system bus. The information on the bus is that contained in the memory location determined by the contents of the cursor registers.

EN LIT OUT- is activated by a decode of 3. The literal circuit is actually a read-only memory that holds the delimiters used in block-type transmissions to the line or to the printer. The last used decode is 7 and is labeled BUS NULL-. This simply places a null (all 0's) code on the bus to be used in clearing operations.

A selected source is automatically removed from the bus when the keyboard is ready to output data to the line. This is accomplished by raising KB OUT EN (7442 input D3-12, zone 3B2). When the keyboard is

returned to the bus. Notice that the register is automatically cleared when the processor moves from Mode 1 to Mode 0. This puts the UART input buffer (EN BFR OUT- low) on the bus upon entry into the idling mode.

5.4.2. OPERTIONAL MODE SELECTION. The operational mode is determined by a single flip-flop (74LS113, location B6, zone 3A3). This flip-flop is automatically set upon initialization, placing the unit in Mode 1 which is the operational mode. This is done because the screen can only be cleared in Mode 1. When an operation is completed in Mode 1, the command GO TO M0 is issued. This clears all operational circuits and causes the Mode 0 output to go high (location B6-6, zone 3A3). The movement back to Mode 1 is caused when an input byte is decoded in Mode 0 and the OPERATION REGISTER is loaded with the appropriate code. This raises LD OPN (input B6-3, zone 3A3).

OPERATIONAL MODE LATCHES

The purpose of the PROT MODE latch is to indicate to the program that those bytes resident in the refresh memory with bit 8 high should be considered protected and cannot be overwritten. This condition occurs when this output PROT MODE (74175, location E11-2, zone 4D3) is high. This latch is initialized off and is subsequently set or cleared with two character ESC sequences (an escape code followed by another USASCII code).

The WRITE PROT latch is provided to allow writing potentially protected data into the refresh memory. If this latch is set, all data written into the memory will be tagged bit 8 true. Then if the PROT MODE is on (see above), these bytes will be protected. This latch is also controlled by ESC sequences from the receiver.

The hardware control of these latches is as follows. The 74157 (E11) attempts a load on every system strobe (ST2-, E11-9). If no change is desired, all of the set and clear lines from the PLA command decoders will be high and the current status of the latches are fed back to the latch inputs through the NAND gate (7400, location E9) and the AND gat- (7408, location E10).

If one of the stages is to be set by the program, the appropriate set signal is driven active (low) which unconditionally forces the latch input to a high state. On the next system strobe, this condition is saved and the "set" signal goes inactive. The normal feedback path maintains this new condition. If the program desires to clear this bit, the "clear" signal is issued which drives the 7408 input low. This, in turn, causes the latch input to go low which is saved on the next system strobe. In this manner, the computer can change the operational status of these latches until the next initialization process is activated.

LITERAL CIRCUIT

The purpose of this circuit is to provide, to the system bus, pre-programmed transmission constants. These constants are automatically inserted into a block-type transmission to indicate that the cursor has encountered a protected field, the end of a line, or the end of a message. This circuit operates in the following. A programmable read-only memory (82S123, location D1,, zone 4B3) holds the actual constants. The program selects the actual constant desired by loading a three bit address register (74173, location D2, zone 4B4) with the command LD LIT ADR- (D2-9, zone 4B4). This three bit address is sent to the PROM along with two additional bits that identify the type of transmission such as, block transmission to the line or a print message to the printer. The PROM accepts these address lines and outputs the constant to the line when the signal EN LIT OUT- is asserted. The output of the prom goes directly to the bus since the 82S123 is a three-state device.

SYSTEM STROBE GENERATION

The last circuit on logic sheet #4 is the system strobe generation and control. The system strobe (ST) is a pulse 91.8 nsec wide and normally occurs every 643 nsec. The generation of the strobe is inhibited when the signal NO STROBE- (7427, location D14-6, zone 4A4) is active (low). This condition occurs if the unit is refreshing the screen (SCREEN REFRESH, D14-3, zone 4A4), the keyboard is on the bus (KB OUT EN, D14-5, zone 4A4), or the unit is in the last instruction time before screen refresh (CPC CARRY, location D14-4, zone 4A4). NO STROB- inhibits the strobe generation at input H10-11 (zone 4A3). The strobe width is determined by the signal DPC8 which comes from the display counter chain and enters the strobe generation circuit at H10-10

(zone 4A3). Input H10-9 (zone 5A3), shown on the schematic with a pull-up resistor, is used by an external tester to stop the unit during trouble-shooting. Output H12-8 (STI-, zone 4A3) is then the inverted system strobe. Further buffering for additional drive capability is accomplished by the two buffers D13-2 and D13-4 located in zone 4A3.

DISPLAY TIMING COUNTERS

The display timing counters are located on logic sheet 5. The purpose of the display timing chain is to synchronize the presentation of addresses and video data with the CRT monitor. In the IQ 120 it further provides the signals by which the processing section of the display knows when it can operate. This counter chain consists of four separate counters and a master oscillator.

MASTER OSCILLATOR

The oscillator consists of two NAND gates (E15-8 and E15-11), two feedback resistors (1K ohm), a coupling capacitor (100 pf), and a 10.8864 MHZ crystal. This signal is shaped through two additional elements (E15-3 and E15-6) to generate the two phases CLK and CLK-. This entire circuit is located in zones D3 and D4. The signal labeled CLK- is sent to the first counter in line as its clock.

DOT POSITION COUNTER

This counter is a single 74163 located in zone C4. It has four outputs labeled DPC1, DPC2, DPC4 and DPC8-. The purpose of this counter is to keep track of the horizontal dot times in a character and is designed to provide a division of seven. This allows five dot times for video and two dot times for the space between characters. This counter is preset to a count of 10, counts through a maximum of 15, and automatically recycles to a count of zero. The zero count is used as the preset to the shift register that serializes the video data.

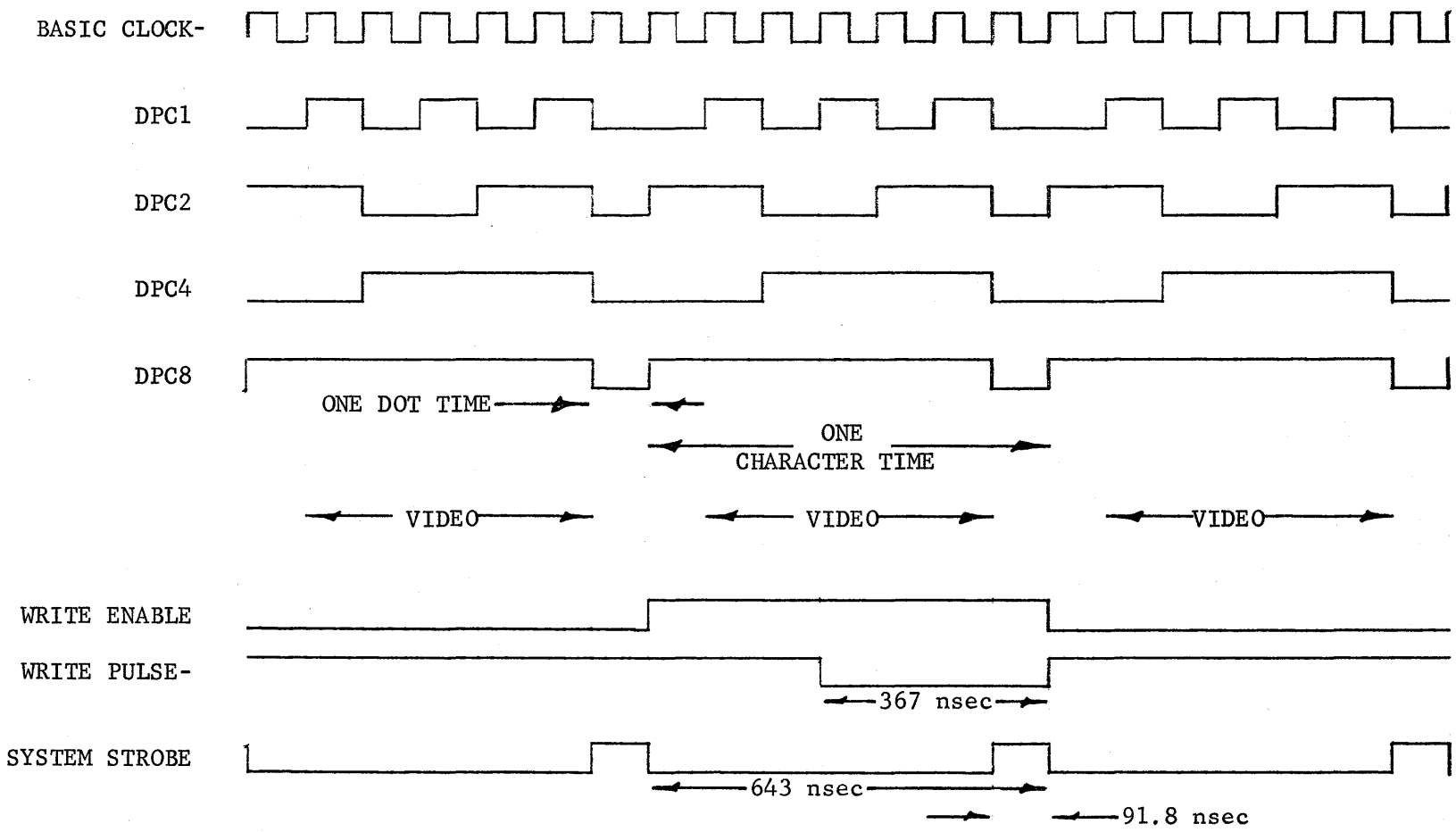


Fig.5-2 DOT POSITION COUNTER
and associated signals

Therefore, the video occurs during the decodes DPC=11 through DPC=15 and the blanking during decodes DPC=0 and DPC=10. The zero count is used as the DPC preset term (F15-9) and the clock to the next counter in line.

CHARACTER POSITION COUNTER

The next counter is a seven stage element called the CHARACTER POSITION COUNTER. It is located in zones B4 and C4 and is labeled in binary weighted fashion from CPC1 through CPC64. The purpose of this counter is to count the character times on one raster sweep of the CRT. The total division of the CPC counter is 96; 80 counts in the visible video time and 16 counts during horizontal retrace. This counter consists of two 74163's (K6 and L7). It starts a cycle at a count of zero and proceeds in a binary manner up to a count of 79, which is the last character time during video. At this time, the counter is preset to a count of 240 and increments to the maximum count of 255. This latter interval is the horizontal retrace time. The signal labeled CPC80 also designates the retrace time. CPC CARRY (K6-15, zone 5B4) is high during the last character time of horizontal retrace. The signal generated by the 7474 (F11-5, zone 5C3) and called HBLANK is used to shut off the serial video stream during retrace. It is delayed from CPC80 by two character times because of the register and character generator delays located in the address path. The signal generated by the 7410 (K3-8, zone 5B3) and called CPC=79-, is used as the preset to the CPC counter (K6-9 and L7-9) and indicates the last character time during the visible portion of the sweep.

CHARACTER HEIGHT COUNTER

The leading edge of HBLANK is used as the clock to the counter called the XHARACTER HEIGHT COUNTER (CHC). This counter consists of a

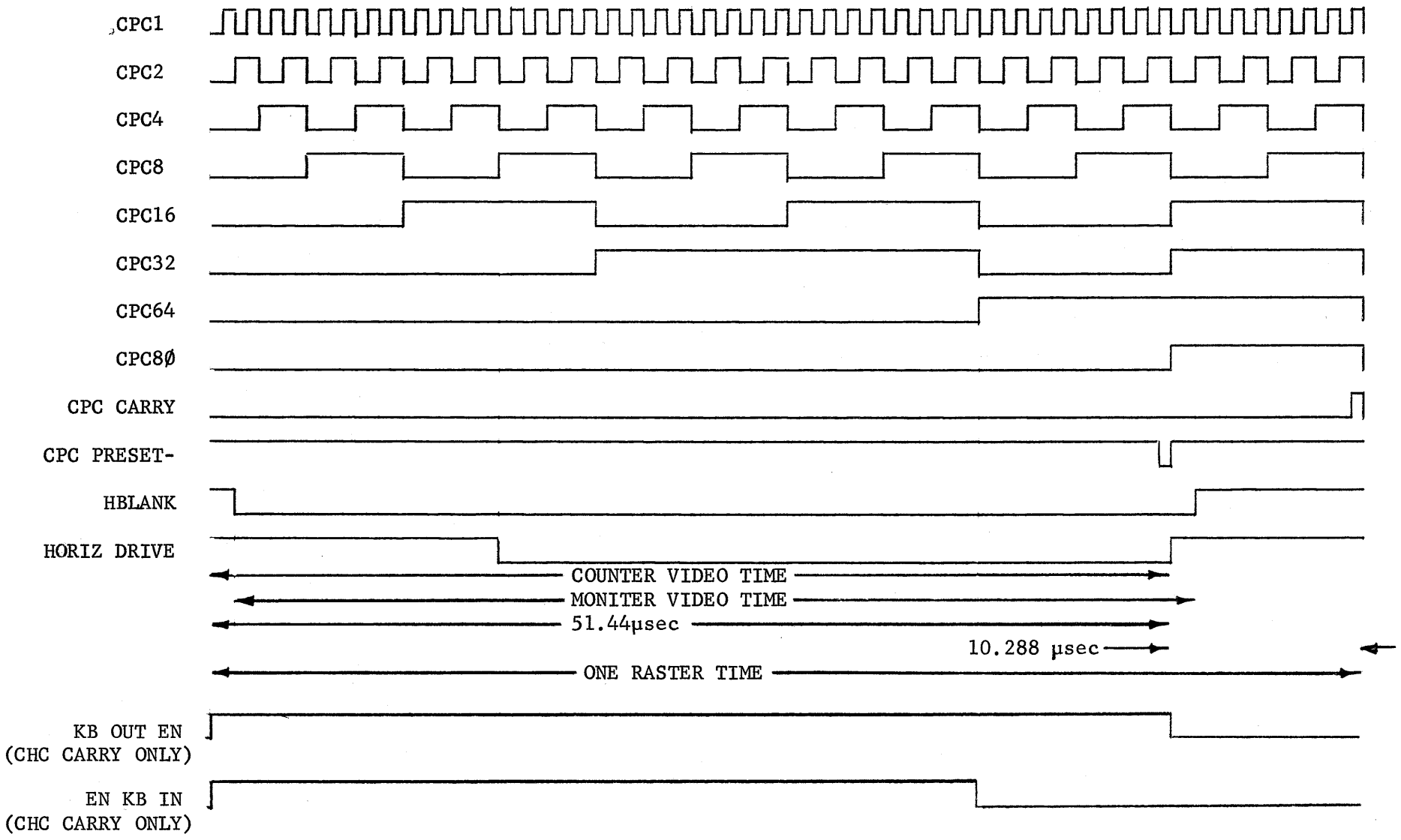


Fig. 5-3

CHARACTER POSITION COUNTER
and associated signals

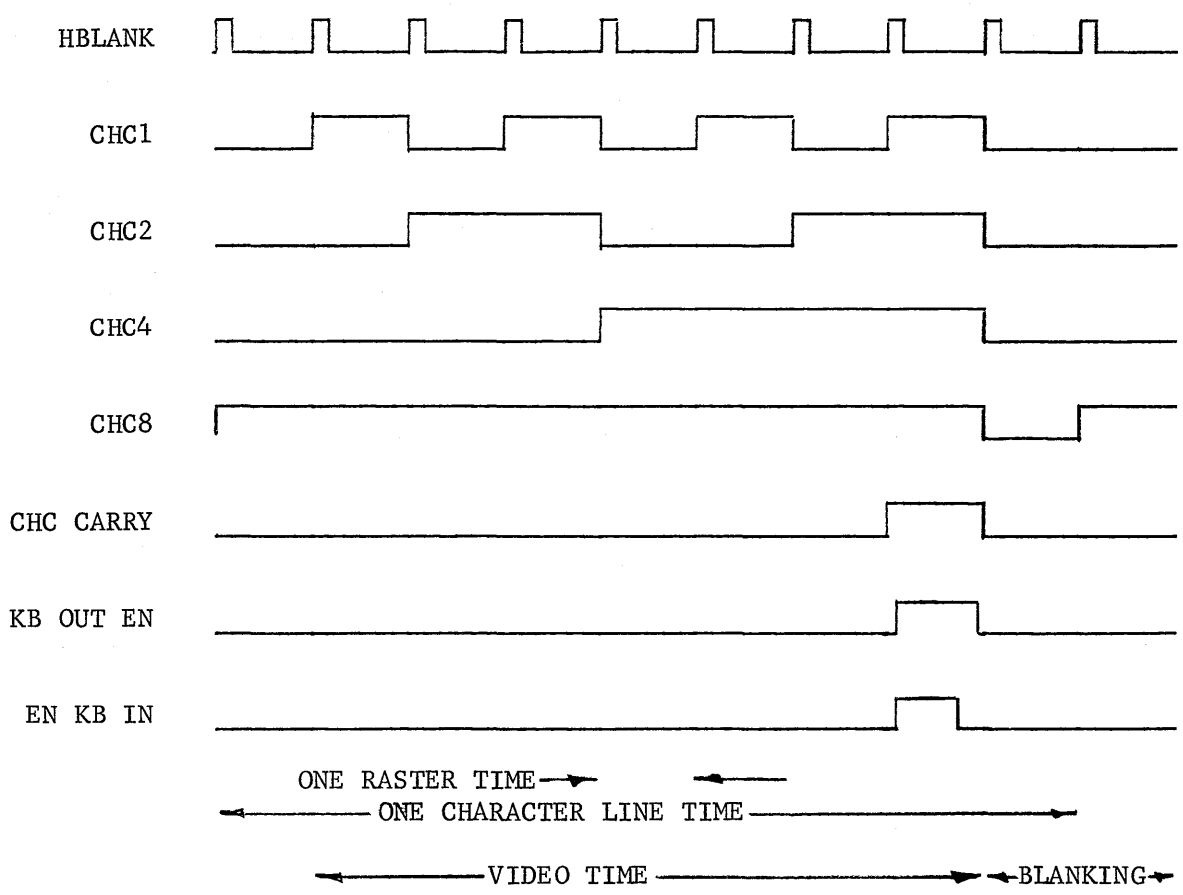


Fig. 5-4
CHARACTER HEIGHT COUNTER
and associated signals

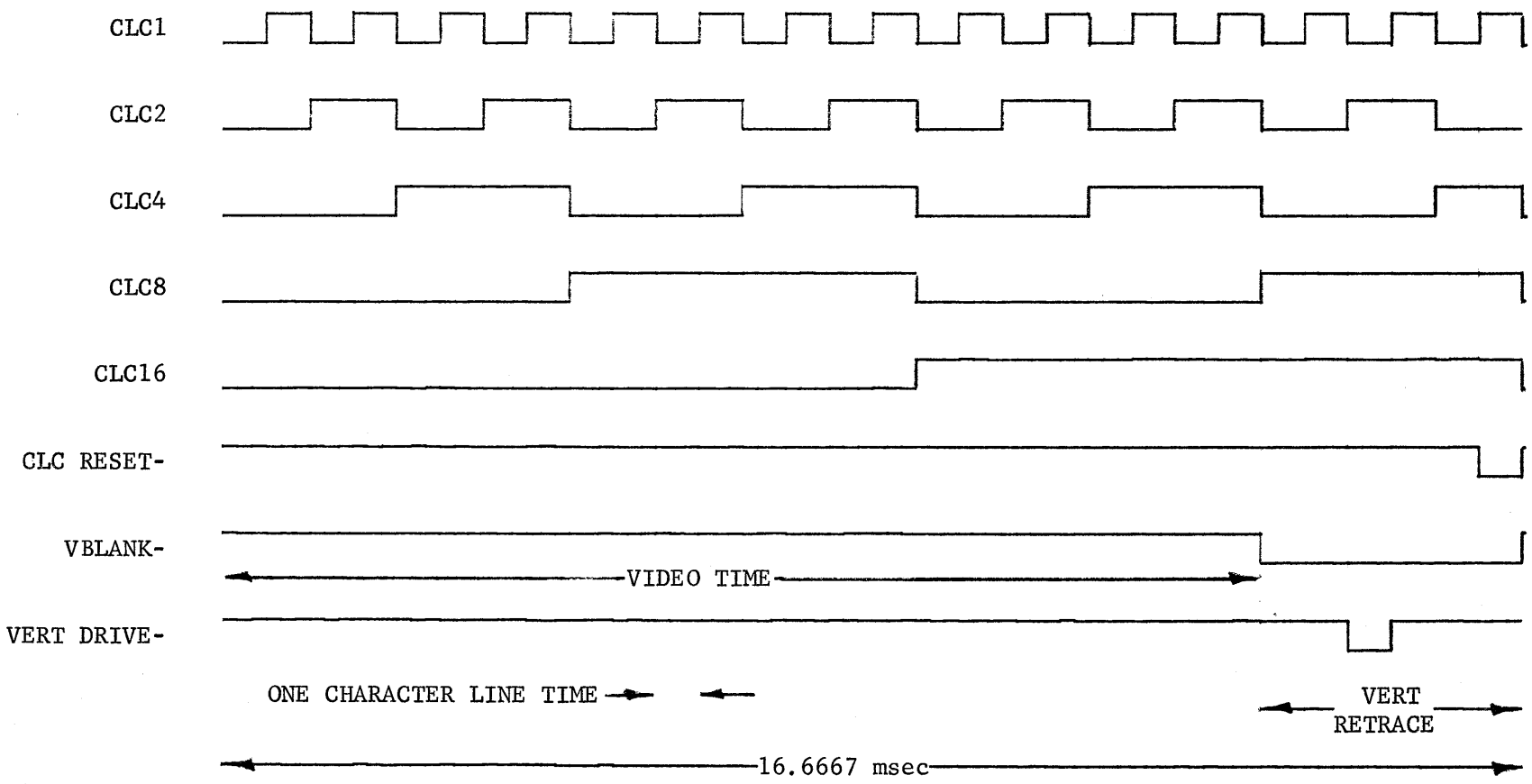


Fig. 5-5
CHARACTER LINE COUNTER
and associated signals

single 74163 (location H11, zone 5D2). This counter's purpose is to count the raster lines used to generate one character vertically. Its total division is 9 and it starts at a count of 8, increments up through the maximum count of 15 to zero, and presets back to 8. Video is generated during counts 9 through 15 and blanking occurs during counts 0 and8. The signal labeled CHC CARRY (H11-15, zone 5C2) indicates the last visible raster line during a character time. The outputs of this counter go to the character generator to time its outputs. The final stage, CHC8 (H11-11, zone 5C2), is used as the clock to the next counter.

CURSOR LINE REGISTER

This register consists mainly of a 7474 D-type flip-flop and a 74193 binary, up/down counter (H4 and J6 respectively, zones 6B3 and 6A3). The cursor line register is a five stage counter, CURL1 through CURL16, which places the display cursor on one of 24 character lines. Note that CURL decodes 0 through 23 are legal, displayable lines. Therefore, the signal labeled CURL ILLEGAL- (7400, location L5, zone 6A2) is provided to indicate to the program when the CURL register has been incremented from decode 23 to decode 24, decremented from 0 to 31, or preset to an illegal, non-displayable address. The controls available to the program concerning this register are: INCR CURL (unconditionally advances); DECR CURL (Unconditionally decrements); CLR CURL (sets all 0's); and LOAD CURL (loads the five least significant bits from the bus). CURL1, located in the 7474 flip-flop, is further controlled by the 12/24 line mode, CURL1 is permanently held in the high state. Therefore, the cursor can only reside on the odd lines. This control, 12 LINE EN enters the circuit at H3-6, z one 6B4; and H3-2, zone 6A4.

CURSOR POSITION REGISTER

The cursor position register consists of two binary up/down counters

(74193's, locations K7 and L8, zones 6C3 and 6D4) whose seven outputs are labeled in binary order, CURP1 through CURP64. This register places the cursor on one of 80 displayable addresses on a character line. However, since this counter has a maximum count of 127, a signal is generated to indicate to the program that the cursor position register holds a count greater than the maximum displayable position of 79. This signal, called CURP ILLEGAL-, is generated by L5-8 (7400, zone 6C3) and indicates that eigher CURP64 and CURP32 or CURP64 and CURP16 are high sinultaneously. In either case, the decode is higher than CURP=79. Like the CURSOR LINE REGISTER, the CURSOR POSITION REGISTER can be incremented (INCR CURP), decremented (DECR CURP), loaded (LOAD CURP), and cleared (CLEAR CURP). A code conversion occurs when the cursor position register is loaded from the bus. The IQ 120 takes an ASCII "SPACE" code and converts it to the zero, or home, position. All subsequent position are counted up from this base "SPACE" code (HEX 20). This conversion is accomplished by an inverter (7404, location F10-12, zone 6C4), an AND gate (7408, H2-8, zone 6C4), OR gate (7432, F9-6, zone 6C4) and an exclusive OR gate (7486, J11-11, zone 6C4).

BUFFERED CURSOR LINE

This register consists of two counters (74193's, location J2 and J3, zones 6A1 and 6B1). The purpose of this register is to remember the original location of the cursor when it has to be moved to accomplish any given operation. There are two commands from the processor to control this register. First is LOAD BCUR. This command simply transfers the contents of the CURSOR LINE REGISTER to the BUFFERED CURSOR LINE register and leaves the contents of CURL unchanged. The

execution of this instruction allows the processor to move the cursor and be able to return it to its original ine count. This signal comes directly from the PLA command decoders and is a pulsed signal since the 74193's have asynchronous preset inputs (a clock is not required to load). This LD BCUR- signal enters at J2-11 and J3-11 (zones 6A1 and 6B1 respectively). The second command from the processor is a DECR BCURL- which enters this circuit at F6-1 (7408, zone 6B2). Each time this signal is issued, the BCURL register is decremented. This operation is used by the program to count the number of lines to reach the original line that contained the cursor. For example, to transmit data from the home position to the cursor, the value of the cursor register would be loaded into BCURL and the cursor register would be cleared to zero. Each time the CURSOR register was incremented, BCURL would be decremented. When BCURL goes to zero, the cursor would contain the original value of the cursor line register. Input F6-2 (7408, zone 6B2) is only active if the IQ 120 is operating in 12 line mode. In this mode the BUFFERED CURSOR LINE register is only allowed to contain even counts. Therefore, after a DECR BCURL- command takes the register to an off count, the driving NAND gate (7410, location F5-12, zone 6B2) is enabled on the next system strobe and the register is clocked to an even count. The signal labeled BCURL ILLEGAL (74LS113, location H1-9, zone 6B1) is generated when enough DECUR BCURL- commands have been issued to decrement the counter to 0. On the next DECR BCURL- command, the BCURL ILLEGAL signal is raised through the direct set input of the flip-flop (location H1-10, zone 6B1). This signal, in turn, clears the BUFFERED CURSOR LINE register. BCURL ILLEGAL, being high, also is the indication that the original line has been reached. It also now enables the program

to clock the BUFFERED CURSOR POSITION register. This condition is only cleared when the program moves back to the idling mode (Mode0). The program also has the capability of setting the BCURL ILLEGAL flip-flop directly by issuing the CLR BCURL- command that enters the circuit at B5-1 (7404, zone 6B1).

BUFFERED CURSOR POSITION

This register, like the BUFFERED CURSOR LINE, consists of two 74193's (locations D4 and L4, zones 6C2 and 6D2). Its purpose is identical to the BUFFERED CURSOR LINE register described in the previous section except that it buffers the cursor position. This register loads from the CURP output on the same command that loads the BUFFERED CURSOR LINE, LD BCUR-. It also has a decrementing command, DECR BCURP-. However, this command cannot decrement the counter unless the signal BCURL ILLEGAL is active (high). Once the decrementing clock is enabled, this counter counts down until a clock is issued when the counter is sitting at zero. At this time, the flip-flop (74LS113, location H1-6, zone 6C2) labeled BCURP ILLEGAL- is directly dirven active. This signal is sent to gate input K3-3 (7410, zone 6C1) which in turn, drives the signal called ILLEGAL to its active state (high). This is sensed by the program and indicates that the cursor is back in its original loaction. The BCURP ILLEGAL flip-flop stays in its active state for only one cycle and clears itself automatically. The circuit located in zone 6D1 generates the actual clear signals used by CURP and CURL. The program issues the commands CLR CURP EN- and CLR CURL EN- which are clocked into the 74175 (location H6, zone 6D1). Therefore, the actual clearing of the registers occurs during the instruction time following the issuance of the clear enable signals.

MEMORY ADDRESS GENERATION

Schematic sheet #7 shows the manner in which the address to the refresh

memory is generated. There are two different sources of memory addresses in the IQ 120. First is the sequential addressing of the memory for refreshing the screen. This address is essentially stages of the system counters that keep track of the position of the CRT raster at any given moment. The two counters that provide the addressing for the memory are the CHARACTER POSITION COUNTER and the CHARACTER LINE COUNTER. The other source of memory address are the CURSOR POSITION and CURSOR LINE registers that the program uses to accomplish its operations.

ADDRESS SOURCE SELECTION

The primary selection between the two address sources (CURP/CURL and CPC/CLC) is accomplished through three 2:1 multiplexer IC's (74157; locations L9, K8, and J7; zones 7B2, 7A4 and 7D4 respectively). Their use is dictated by a signal called SCREEN REFRESH which controls the three IC's mentioned above through their select inputs (pin 1). When this signal is high, the screen is being refreshed and the CPC/CLC combination is being used through the "B" inputs of the multiplexers. When this signal is low, the program is operating and the CURP/CURL combination is being utilized. SCREEN REFRESH IS generated by D9-8 (7427, zone 7D3). This signal is generated by CHC VIDEO TIME- which restricts SCREEN REFRESH to those seven raster scans that display video information. This signal is on D9-10 (zone 7D3). The next signal enters on D9-9 (zone 7D3) and is labeled CPC80. This signal is low during the video portion of any raster scan. The last input to this gate (7427, input D9-11, zone 7D3) shuts off the screen refresh if the unit is in vertical retrace (VBLANK-) or if the program shuts off the refresh (BFR CLR SCRN-). These last two signals are OR'ed in gate C14-8 (7400, zone 7D3).

ROLL COUNTER

The ROLL COUNTER consists of a counter (74161, location H8, zone 7B4) and a flip-flop (7474, location H4, zone 7C4). The purpose of this circuit is to allow the processor to "roll" the data on the screen up one line without actually moving the data in the refresh memory. This counter is cleared on initializing and it counts the number of times that the program wants the screen rolled. This counter always remains legal, that is it always holds a number between 0 and 23. This recycling is accomplished by the NAND gate (7420, location P8-6, zone 7B3) that decodes the count 23 and clears the counter on the next clock. If the unit is operating in the 12 line mode, the first stage (ROLL1) is held in a high state which always keeps the count odd. This is accomplished by the jumper located in zone 7C4. This ROLL COUNTER output is added to the line portion of the multiplexed address input. This addition is done in the full adder (7483, location J8, zone 7D3). The output of this adder creates a "virtual" address for the line portion of the address. For example, if the ROLL COUNTER is sitting at zero and the actual line address is also at zero, the sum will also be zero which will be the first line displayed. However, if the roll counter is sitting at a count of 1 (one roll operation since initialization) and the system address desires the top line (CLC = 0) then the sum will be 1 and the first line displayed at the top of the screen will be the line that was originally the second line on the screen before the roll operation). The purpose of the second adder in line (7483, zone 7D2) is to watch the output of the first adder and keep it within legal limits (between 0 and 23). This is because the sum from the first adder can exceed 23. Therefore a line address of 24 out of the first adder is converted to 0, 25 to 1, etc.

REFRESH MEMORY CHIP SELECTION

The refresh memory in the IQ 120 is organized to place all of the odd lines in one group of memory and all of the even lines in another. This was done to facilitate the even lines in another. This was done to facilitate the 12/24 line option. The proper memory IC package is done by generation of the appropriate memory chip enable (EN 12- or EN 24-).

This is accomplished by the exclusive-or gate (7486, zone 7C2) located in IC location J11-6. Another 7486 is used as an inverter to generate the other chip enable. The unit is normally shipped in the 24 line mode.

ADDRESS FOLDING

The multiplexer located in zone 7A3 (74157, location K9) is used to change the address when the addressed position exceeds a count of 63. In that respect, this display operates with a format of 30 lines with 64 characters per line, although it visually looks like a 24 line display with 80 characters per line. This is to prevent holes in the memory of 48 characters, which is the difference between the 80 character line and the binary count of 128.

REFRESH MEMORY

The refresh memory in the IQ 120 consists of 2048 bytes with 8 bits per byte. The 8 bits consist of the 7 bit ASCII code in bits 1 through 7 with bit 8 being utilized as the protect indicator. Because of the 24 lines by 80 characters per line format, the unit actually uses only 1920 locations out of the available 2048. The address lines generated on schematic sheet 7 go directly to all 16 of the static, 1K, MOS memory devices. These address lines are labeled MEM ADR 1 through MEM ADR 512 (zones 8C4 and 8D4) and they select 1 of 1024 memory locations contained in a chip. The selection between odd/ even memory ICs is done utilizing the chip select lines. EN 12- is the chip select signal for the line of memory that is installed regardless of whether the unit is operating in the 12 or 24 line mode. This signal is found in zone 8A3. En 24- is the chip select that is used for the additional ine of memory that is normally installed as part of the 24 line option, and it enters this circuit in zone 8A2.

The data inputs of the last significant seven bits come directly from the system bus and are connected to pin 11 of their respective memory ICs. Bit 8, the protect bit, is essentially the WRITE PROT flip-flop. This line can go high only in Mode 0 since all new data entry is done in this mode. When in Mode 1 this input line is always low.

The last input to the memories is the R/W input. This input is held high when the current operation is a "read" command. When new data is to be written into the currently addressed location, this line is dropped to a low level. This writing operation is accomplished using a flip-flop (7474, location F11-8, zone 8A3) and a gate (7432,

location F9-8, zone 8A3). The flip-flop generates a write pulse of proper width on every cycle. The gate is utilized to enable this write pulse (input F9-10) to the R/W input of the memories (pin3) only when commanded by the processor (input F9-9, zone 8A3). The wirte pulse is sent to all memories because the chip has to be selected before the actual write operation can be accomplished.

MEMORY OUTPUTS

The memory outputs are first buffered before they are used because of the limited drive capability of the MOS memories. Therefore, the outputs of the refresh memory can be considered the outputs of the TTL output buffers. The buffers accomplish one other function. They are used to generate a NULL code that can be written into the memory via the system bus for editing operations. This is accomplished when the signal labeled BUSS NULL-, in zone 8A2 is activated (driven low). This signal is activated by a command from the processor which has the effect of placing a NULL (all 0's) code on the system bus.

The last function on this schematic sheet is the generation of the signal called PROT BIT. This gate (7427, location D15-12, zone 8C1) combines the fact that the protect bit in the memory (bit 8) is high and the PROT MODE is active. If both of these conditions are present, PROT BIT is asserted and is sensed by the IQ 120 program as a protected character. If either of these two conditions is missing, the character is considered unprotected and can be overwritten during any editing operation. Thus it can be seen that low intensity information can be resident on the CRT screen and not be protected until th- PROT MODE slip-flop is activated by an ESC sequence.

VIDEO GENERATION

The main purpose of schematic sheet #9 is to take the output of the memory at the proper time and convert it to a serial video data stream to send to the monitor.

ADDRESS PATHS

The memory outputs come to a buffer before being presented to the character generators. The purpose of this buffer (74173, locations J12 and J14, zones 9D4 and 9C4 respectively) called CGIN is to provide a full cycle time for the character generator to access. Without this buffer, the access time of the memory and the access time of the character generator (both MOS devices) would combine and exceed the character time allotted. The clock input to this register, CGIN, is DPC8- which designates the end of the character time. The presence of this register in the address path delays the video presentation one character time. The outputs of this register, CGIN1 through CGIN7, are then used by the character generator and its associated cirucitry. CGIN8 is used to generate the low intensity video field that is potentially protected.

CHARACTER GENERATORS

The upper case character generator (2513, location H15, zone 9C3) is a 64 character, 5x7 MOS device. It contains all of the Upper Case alpha characters, numerals, and punctuation used in the IQ 120. The lower case codes resident in the refresh memory are converted to display the euqivalent upper case characters. The lower case option requires the insertion of another character generator which generates the 32 characters in the lower case columns of the ASCII code chart. This character generator for lower case (2513, zone 9B3)is located at H14. Position H12 is occupied by character generator ROM that

stores both the upper and lower case character sets. It is normally the only character generator supplied.

Next is the circuit used to enable the proper character generator in the case where the lower case option is installed. The detection of an upper case code is accomplished utilizing an AND gate (7408, location H9-3, zone 9D3). Input H9-2 looks at bit 6 of the code and H9-1 looks at bit 7. Therefore, if bits 6 and 7 are both H16A, as they are in upper case ASCII codes, then output H9-3 will go high. This indicates that the upper case generator, if installed, should b-enabled. Gate E13-11 (7408, zone 9D3) is used to dissable the vidio signal if a NULL code is detected.

VIDEO SERIALIZER

The output of the character generator is presented in parallel form, 5 bits wide. This information is preset into the video serializer (74166, location F14, zone 9C2). This shift register uses the basic clock of the system as its shift clock, CLK-, which enters on pin7. The preset of this shift register is driven by DPC8-, which occurs every 643 nsec which is the character rate. The CLEAR input of the serializer is driven by a signal that is only active (low) when the unit is run as a 12 line display. This clears the shifter if 12 line is enabled (input F5-3 high) and the CHARACTER LINE COUNTER is on an even count (CLC1=0). The serial video data then appears on the serializer output (74166, location F14-13, zone 9B2).

VIDEO CURSOR CIRCUIT

The generation of the video cursor basically involves comparing the CURSOR POSITION COUNTER (CPC) against the CURSOR POSITION REGISTER (CURP), and the CURSOR LINE COUNTER (CLC) against the CURSOR LINE REGISTER (CURL). When both terms compare, it is time to generate the

cursor. The CURP/CPC comparison is accomplished in two comparators (7485's, locations K5 and L6, zones 9A3 and 9A2 respectively). The CURL/CLC is done with a single comparator (7485, location J4, zone 9A4). When the line portion compares, the equal indication is used to enable the position comparator (input K5-3, zone 9A3). When all 12 terms compare, a signal called CNTR CUR (output L6-6, zone 9A2) is generated indicating that it is time to display the cursor. However, a delay of two character times is required because of the delays in the address path. The CGIN register injects one character time of delay and the character generator introduces the other. Therefore, the video cursor is delayed through two 74175 stages (location F12-10 and F12-7, zone 9A2) whose clock goes at the character rate. The final output of this delay circuit, VIDEO CUR is used to invert the serical video path by using an exclusive-or gate (7486, location J11-3, zone 9C1). Thus, the output labeled VIDEO (7486, location J11-3, zone 9C1) is the signal that is sent to the video driver. Bit 8 of the CGIN register is delayed one character time to create the signal, VIDEO PROT-, that is used to generate the low intensity video that potentially designates a protected field.

MONITOR DRIVE SIGNALS

The drive pulses for the monitor are generated on schematic sheet #10. The signal, called VERT DRIVE- zone 10D3 is sent directly to the monitor through connector J1-11. The horizontal drive signal is created in flip-flop E12-6 (74109, zone 10D4) and is derived from the CHARACTER POSITION COUNTER. This signal, HOR DRIVE, is sent to the monitor through connector J1-10.

VIDEO DRIVER

The video driver consists of two invertsers (7404, locations B15-4 and B15-6, zone 10A2) and a resistor network to set the proper voltage levels. The bottom inverter (B15-6) is for the video data and is fed by the 7420, F8-8, whose inputs consist of the serial video stream and the horizontal and vertical blanking signals. Therefore, this signal will be active if the monitor's sweep is out of the horizontal or vertical retrace times. The other inverter (7404, location B15-4, zone 10B2) is used to create the low intensity video fields. If its input is high, the output will go low, thereby creating a lower "high" output at the contrast pot. This diminishes the intensity of the signal on the CRT face. This inverter is driven by the signal VIDEO PROT which is a signal delayed from bit 8 in the REFRESH MEMORY.

BAUD RATE GENERATION

The transmission baud rates in the IQ 120, shown on sheet 11, are generated without a separate oscillator. Selected outputs from the main counter chain are utilized as the inputs to divider networks to create the fifteen rates available in this unit.

The 19.2 KBaud clock is derived by using THE MAIN CLOCK, two 74161 counters CLK and dividing it thru D11 and C11 in zone D4. Subsequent binary divisions are done by two binary counters (7493, locations AB9 and AB9.5, zone 11C4). This chain provides all baud rates from 75 that are multiples of 2 up to 19.2 KBaud.

CHARACTER POSITION COUNTER output, CPC32, is used directly as the 16x clock for 2000 baud.

The DOT POSITION COUNTER also provides the clock from which the 7200, 3600, and 1800 baud rates are derived. DPC1 is first divided by 10 through a decade counter (7490, location AB8, zone 11B4). This output is then further divided by 4 by two stages of a binary counter (7493, locations A9-12 and A9-9, zone 11A4) to provide the 16X clock for 7200 baud. Two additional binary divisions then create the rates for 3600 and 1800 baud. The last clock is for 110 baud. The 1200 Baud output is counted down to 110 Baud by the 74163 (all zone 11A4) to produce this clock.

BAUD RATE SELECTION

The baud rate clock for the main I/O port of the IQ 120 is selected using a 16:1 data selector (74150, location A10, zone 11D2). The fifteen rates are placed in decending order on the inputs. The actual selection by the operator is accomplished by a rotary switch on the back panel which is labeled from 0 to 15. The lowest number

on the switch selects the lowest rate (position 0 = 75 baud).

The following table shows all of the rates and positions:

POSITION	BAUD RATE
0	75
1	110
2	150
3	300
4	600
5	1000
6	1200
7	1800
8	2000
9	2400
10	3600
11	4800
12	7200
13	9600
14	19200
15	19200

The printer port baud rate is internally selected with a jumper strap. This jumper pattern is schematically shown in zone 11D3. An important thing to remember is that only one jumper should be installed to avoid shorting two baud rates together.

The actual clock seen by the transmitter/receiver is then selected by a 2:1 data selector (74157, location B11-4, zone 11D2) depending on whether the IQ 120 is transmitting to the line or printing.

TRANSMITTER/RECEIVER

The transmitter/receiver used in the IQ 120 is an Universal Assynchronous Receiver Transmitter (UART) which is a combination receiver and transmitter. The transmitter and receiver in this device run essentially independently except for the word configuration controls.

RECEIVER

The receiver circuit consists of 8 outputs from the UART. Seven of these are the data lines which reflect the received character and are labeled UART DATA 1 through UART DATA 7 (TR1602, location C8, zone 12D3). These seven data lines go to the INPUT BUFFER. The last output utilized by the IQ 120 is the data ready signal (C8-19, zone 12B3). This signal goes high when the UART detects the middle of the STOP bit on a serial, incoming word. This indicates to the unit that it can unload the parallel information from the UART. Data ready is sent to the AND gate (7408 input E10-10, zone 12B2) where it is combined with the signal called NEXT CHARACTER. This signal is active (high) when the input buffer is not being used. If this condition exists, the LD BUFFER signal is generated (7474, location E14-5, zone 12B2) which takes the parallel 7 bits from the UART outputs and loads the input buffer. This code will remain in the input buffer until the IQ 120 processes it. This completion of the operation is indicated to the input buffer by the raising of the signal called CLEAR INPUT BFR which originates at latch H6-6. (74175, zone 12D3). This signal is initiated by one of two paths. The program can issue a command to clear the buffer which is called CLR BFR EN- (zone 12D4). This moves unconditionally through the OR function (7408, E5-11) located in zone 12C3. The input buffer can also be cleared automatically

when moving from Mode 0 to Mode 1. This operation is detected by gate B7-3 (7432, zone 12D4). This gate determines that the program is presently operating in Mode 0 and is attempting to issue a load OPERATION REGISTER command. This is required because the IQ 120 program also loads the OPERATION REGISTER when it id operating in Mode 1. This signal is OR'ed with the program initiated clearing and enables the input of the latch. The LD BFR flip-flop (E14, zone 12B2) is also used to clear the DATA READY signal from the UART since the leading edge of this signal indicates that the UART has been unloaded. This clearing is done into the DATA RECEIVED RESET input to the UART (C8-18, zone 12B3).

This null detection is accomplished by two 7427's (D9-6 and D9-12, zones 12B4 and 12C4 respectively) and one 7420 (D10-3, zone 12B3). When this signal, NULL ON BUS-, is active (low), no load pulse can be generated at UART pin 23. The two output signals from the UART used by the transmitter section are THRE and TRE (pins C8-22 and C8-24 respectively). TRE is the output that indicates whether or not there is a character in the serializer presently being transmitted. If this signal is high, the serializer is empty. If THRE is high, it indicates that the input holding register is empty. Both signal high simultaneously represents the condition that the transmitter is idling. If one of these two signals is low, the signal called XMTR BUSY (7404, location B5-8, zone 12B1) is asserted. The transmitter is also considered busy when the program is in the process of loading the UART. This is accomplished by PROG LD UART- at input E9-10 (7400, zone 12B2). The SMTR BUSY signal is then clocked through a latch (74175, location E11-10, zone 12B1) to synchronize this signal

with the system strobe. The resulting signal is called SYNC XMTR BUSY (zone 12B1) which is sensed by the PLA to control transmission.

UART CLOCKS

The CLEAR-TO-SEND signal from the line or the printer is used to signal the processor that it is OK to transmit. The selection of the proper CLEAR-TO-SEND signal, MAIN CTS- or PRINTERS CTS-, to use is done through a 2:1 data selector (74157, location B11-12, zone 12A4). When in conversation mode (HDX or FDX), this output is used to generate a SYNC XMTR BUSY signal so that the processor will not attempt to send data to THR UART.

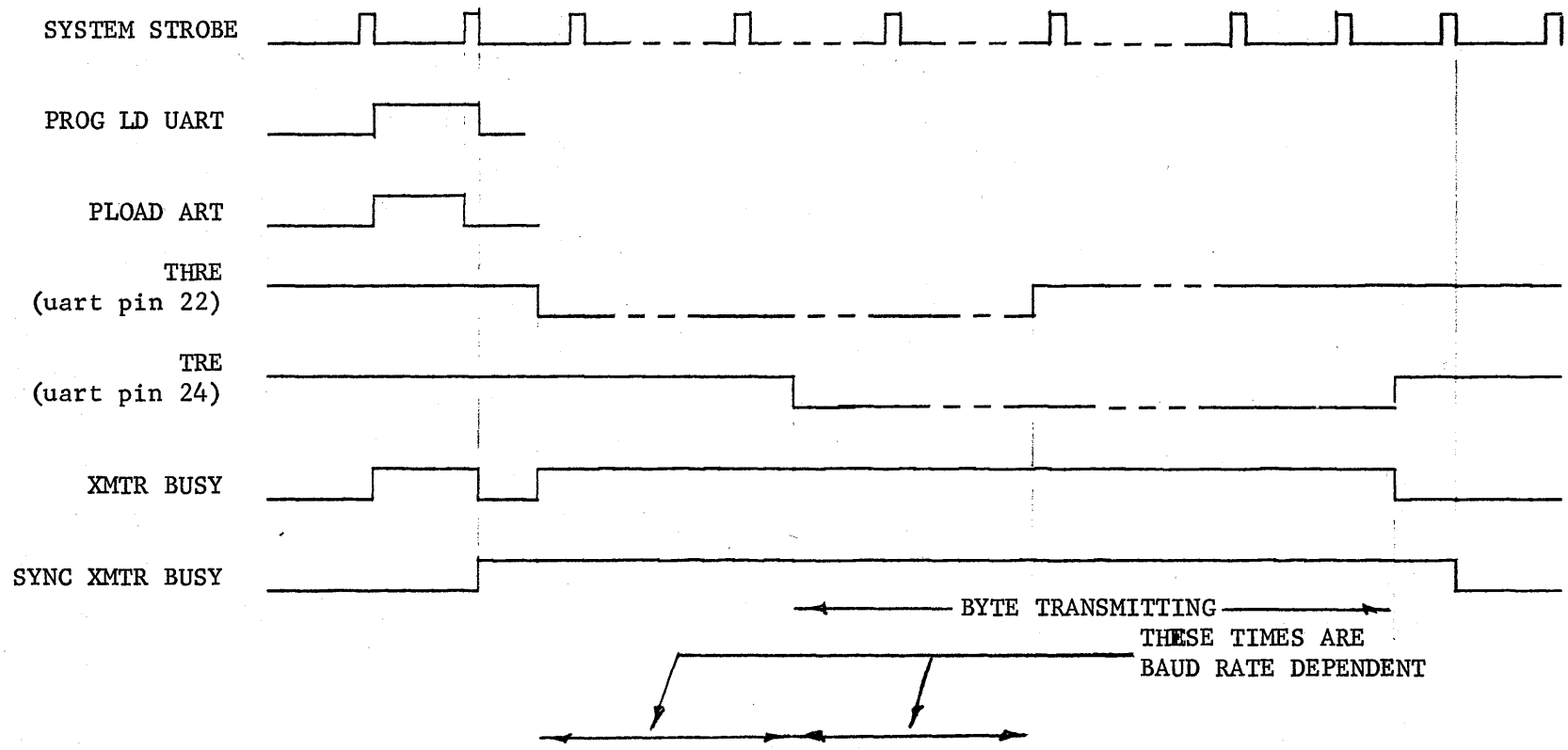
TRANSMITTER

The transmitter section loads data to be sent from the IQ 120 system bus. These inputs are located in zone 12C3 (UART, locations C8-26 through C8-32). The load pulse enters the UART ON pin 23 (zone 12B3) and is called LD UART-. There are two sources for this signal. First, the keyboard can recognize a keystrobe and generate a load pulse to the UART (see description for sheet #1).

Then, the program can generate a load pulse during block transmission to the line or the printer called PLOAD UART- which is OR'ed with the KB LOAD UART- signal in gate D10-11 (7400, zone 12B4). The program actually issues a command called LD UART EN- which enters the circuit at inverter H7-1 (7404, zone 12D4). This, in turn, generates a signal called PROG LD UART (74175, location H6-2, zone 12D3) which is active for one instruction cycle. The rising edge of this signal sets a flip-flop (7474, location E14, zone 12C3) which is actually the load pulse to the UART. The load pulse is actually shorter than a program cycle by the width of the system strobe which allows the output signals from the UART to respond in time for the next instruction. The actual loading of the UART is conditioned by the fact that the bus holds a NULL code. The IQ 120 never transmits this NULL code.

WORD CONFIGURATION

The outputs of the 2:1 multiplexer located in C8.5 (zone 12C2) are used to select the word configuration for the main port and the auxiliary port. The SELECT input to this 74157 is controlled by the signal PRINT. Therefore, this signal is high only when the unit is in the midst of a printing operation. When this signal is low, the implication is that the main port is selected and consequently the



PROGRAMMED UART LOADING

five switches that control the main port word configuration are selected. These switches are part of the DIP switch located in 10. Output C8.5-4 is used to select the number of stop bits. This output, connected to pin 36 of the UART (STOP BIT SELECT) chooses two stop bits when high and one stop bit when low. This is driven by switch #4 for the main port and switch #1 for the printer port. A low level for this control input is selected by turning the switch "on". Multiplexer output C8.5-12 (74157, zone 12C2), connected to UART pin 35, is used to enable or inhibit the generation of parity. When this input to the UART is high, no parity will be generated. Main port parity generation control is accomplished using switch #5 and the printer port by switch #2. Multiplexer output C8.5-7 is used to select the parity type once the parity generation is enabled on UART pin 35. Even parity is selected by driving UART pin 39 to a high level and odd parity is selected using a low level. The main port selection is accomplished using switch #7 in location C13. Printer parity selection is done with switch #3. Remeber that this selection is active only if parity generation has been enabled on the input PARITY INHIBIT. Multiplexer output C8.5-9 is connected to UART input pin 38 (WORD LENGTH SELECT 1). When this input is high, an eight bit word is selected. Seven bits of data is selected when this input is low. The main port selection uses switch #6. Printer port does not allow for eight bit transmission. The last switch (#8) is used by the main port to select an "always high" or "always low" parity bit. This is accomplished by first inhibiting the parity generation, selecting an eight bit data word, and using switch #8 to select the polarity.

RS232 Interface

Refer to Dwg. #100052, sheet 13.

The main purpose of the RS232 interface is to convert system logic levels to levels complying with the levels specified in EIA specification RS232C and to convert R232 levels to normal logic levels. The RS232 levels are marking or true level = -10 volts nominal; space, false level = +10 volts nominal.

The signals provided by the interface are SEND DATA (serial data transmitted by the terminal to the line), and REQUEST TO SEND (this signal indicated to the line that the terminal wishes to transmit data). Signals monitored by the terminal are RECEIVE DATA (serial data sent by the line to the terminal), and CLEAR TO SEND (this signal is used to inform the terminal that the computer is ready to send data to the terminal). Data to be transmitted is generated by the transmitter as UART OUT (13B4) and is buffered by the 7408, B8-11, zone 13B4. The buffered UART OUT signal is applied to the input of the multiplexor (74157) located in zone B3, position B11-6 and B11-11. The select input to the multiplexor is normally low unless a print operation is being performed (print operation will be discussed under print option). Under these conditions the data on B11-11 is multiplexed to B11-9 as MAIN SEND DATA. MAIN SEND DATA is applied to the input of 7432, B3-2, zone 13C4, and the inverter A3-10 (zone 13C4). The inverter output is sent to the 7400 gate which enables the data paths depending on the position of the HALF/BLOCK/FULL switch.

If the switch is in the full duplex position (FDX), data is applied to the 7408 located in position B2-1, zone C3.

The B2-2 input is controlled by the output of B3-3, zone 13C3 which in

turn is controlled by B3-1 (EN BLOCK MODE-). If block mode is not selected, this signal will be high causing the output B3-3 high and B2-2 to be high. Thus, MAIN SEND DATA is gated to B2-3, zone C3 and the output of this gate will follow its B2-1 inputs. The output of B2-3 is applied to B2-10, zone C2. The other input to this gate is normally high signal BREAK EN-. This signal goes low whenever the BREAK key on the keyboard is depressed and remains low as long as the key is held down. The purpose of this signal is to force the output B2-8 to a low state which will in turn force the Transmitted Data line A6-6, zone C1 to a high or spacing state. If break enable is not active, B2-8 transmits the data on B2-10 to B2-5 where it is ored with transmitted data and sent on, A6-4, zone C1 where it is inverted and converted to RS232 levels. The data is transmitted to the line via connector J4-2, zone C1. This connector is located in the center of the rear panel of the terminal.

HALF-DUPLEX MODE

If the unit is in half-duplex mode as selected by the mode selection switch, the MAIN SEND DATA is transmitted in the same manner as described above; however, MAIN SEND DATA is also applied to the input of the 7432, B3-10, zone C1. B3-9 is low as we are not in block mode so B3-8 will follow the level on B3-10.

Asseming the B2-13 is in its normally high state, the data at B2-12 will be transmitted to B2-11. This data is applied to the input to the receiver section of the UART where it is sensed by the program and, if it is a displacable character, is loaded into memory and displayed on the CRT.

BLOCK MODE

When the mode selection switch is set to the block mode position, the MAIN SEND DATA from the keyboard is applied to B2-12 zone C3 and is sent to UART receiver (signal UART IN) zone C1 in the same manner as described under half-duplex mode above so long as the EN BLK XMT signal applied to B3-9 (zone C1) is low, but data is not transmitted since the BLOCK position of the switch disables gate A2-6 which prevents the data from reaching B2-1 (zone C3). When a block transmission is initiated, EN BLK XMT- goes low, allowing MAIN SEND DATA at B3-2 zone C4 to be transferred to B3-3 and subsequently to B2-2 (zone C3). At this time the EN BLK XMT signal goes high at the input to the 7432, B3-9 (zone C1) causing UART IN to be held hgih regardless of the state of B3-10, thus preventing data from being sent to the UART receiver. Note that the transmission portion of the block mode operation is independent of the position of the mode selection switch sine if EN BLK XMT- (zone C4) goes false when the mode selection switch is in the FDX or HDX position MAIN SEND DATA will be applied to both B2-1 and B2-2 (zone C3) and subsequently to B2-3.

RECEIVED DATA

Received data is the serial RS232 level data signal from the line. This signal enters the unit via connector J4 pin 3 zone D4. At this point the signal has RS232 leveles. The 1489, A7-1,3 (zone D4 and D3) converts RS232 level to TTL compatible levels for use in the unit. Any signal on pin 1 exceeding +3 volts is converted to a logic low and any signal of less than -3 volts is converted to a logic "1" at pin 3. The output of A7-3 is applied to B2-13 zone C3 and assuming that no data is applied to B2-12, the signal will be transferred to B2-11 and subsequently becomes the UART IN signal B3-8 zone C1. The

data is fed to the UART receiver and interpreted by the program as discussed previously. The "Request to send," and "clear to send" signals are used to control the flow of data to and from the computer, and thus to insure that MAIN SEND DATA is not applied to B2-12 (zone C3) at the same time that RECEIVED DATA is applied to B2-13.

CLEAR TO SEND

The communication line clear to send enters the unit on connector J4 Pin 5 zone B4, and is applied to input A7-13 of the 1489 (zone B4). The signal is applied to an input to the multiplexor B11-14 (zone 12A4). The clear to send control was discussed previously.

REQUEST TO SEND

The request to send signal may be derived in one of two ways depending on the jumper configuration shown zone B2. One position of this jumper pin 9 of RS232 driver A6 (zone C1) to ground. In this configuration REQUEST TO SEND connector J4 pin 4 zone C1 is held in a spacing state unconditionally. With the jumper in the other position, A6-9 is connected to the output of the inverter B5-8 (zone B3). The XMTR BUSY signal is applied to the input to the inverter B5-9. In this configuration the REQUEST TO SEND signal is held in a spacing state any time that the UART transmit register contains a character.

CONTROLLABLE RS232 AUXILIARY PORT OPTION

This port has the ability to enroute data received from the line to a second device. This port is a buffer and any device attached to this port must be configured to operate at the same data rate as the line. Data transmitted from this port can be turned on and off by means of a two code escape sequence. Transmitted data may be received and transmitted via the main port unconditionally. That is, data received by the auxiliary port may not be turned on and off.

AUXILIARY RECEIVED DATA

The data received by the main port is converted to TTL levels by 1489, A7 (zone D3 and D4) and is applied to input B3-13 of 7432 zone D2. The other input to this gate B3-12 is supplied by the $\overline{Q}$ output of the 7474 flip-flop B12 located in zone C2. When the unit is powered up, this flip-flop is reset via the clear 2- signal applied to clear input B12-13. If the appropriate escape sequence is detected by the program, the PLA output PLA01 is driven true and the decoded output EXTENSION CTRL- goes low. When the clocking signal ST2- goes low, the output of 7427 (D14-8 zone D2) goes high, and the high on B12-12 is transferred to the flip-flop outputs causing B12-8 to go false. When ST2- goes high, this conditon is latched in B12 and at the end of the cycle EXTENSION CTRL- goes positive holding D14-8 in a low state. B12 is reset when the program detects the appropriate escape sequence by driving EXTENSION CTRL- low with PLA01 low. The setting of B12 causes B12-8 to go low and thus B3-12 (zone 2D) goes low. The main port received data is thus transferred to the extension port receive data driver input A5-2 (zone D1) and is converted to RS232 levels at the output A5-3 and sent to connector J5 pin 3. Connector J5 is located on the rear of the unit and is labeled "AUX PORT."

AUXILIARY SEND DATA

The Send Data signal is received by the auxiliary port on connector J5 pin 2 and is converted to TTL levels by 1489, A4-4,6 (zone C2). The output of this 1489 (A4-6) is applied to the input to A6-5 of 1488 (zone C1), thru or gate B2-6 and is converted to RS232 levels and sent out on the main port Transmitted Data line via connector J4 pin 2.

AUXILIARY REQUEST TO SEND

This signal is received on connector J5 pin 4 converted from RS232 levels to TTL levels by 1489, A4-13, 11 (zone C4), and is reconverted to RS232 levels by 1488, A6-10, 8 and is applied to the main port request to send line via connector J4 pin 4.

AUXILIARY CLEAR TO SEND

The MAIN CTS- signal is applied to the inputs of the 1488 A5-12 and 13 (zone B1) and converted to RS232 levels at A5-11. This signal is transmitted out of the auxiliary port via connector J5 pin 5.

PRINTER OPTION

If the print option is installed and the appropriate escape sequence is received, the PRINT signal (zone B4) goes high and buffered UART OUT data is transferred via multiplexor B11 zone B3 to 1488, A5-6 (zone B1) via B11-7. This data is converted to RS232 levels at A5-6 and applied to the printer connector J3 at pin 3.

Several methods are provided to allow for printer delays (such as line feed and/or carriage return delays). The first method is to use a fixed delay of two seconds each time a line of data is sent to the printer from the IQ120. This is achieved by means of one shot (74123) A12 located in zone 13A2.

When the program senses the end of a display line, PRINT TIMER- A12-1 goes low triggering the one shot. At this time, A12-13 goes high for two seconds causing the signal printer CTS- to go high which causes the UART to stop sending data. The jumper must be installed in position 1 zone A3 to select this to happen.

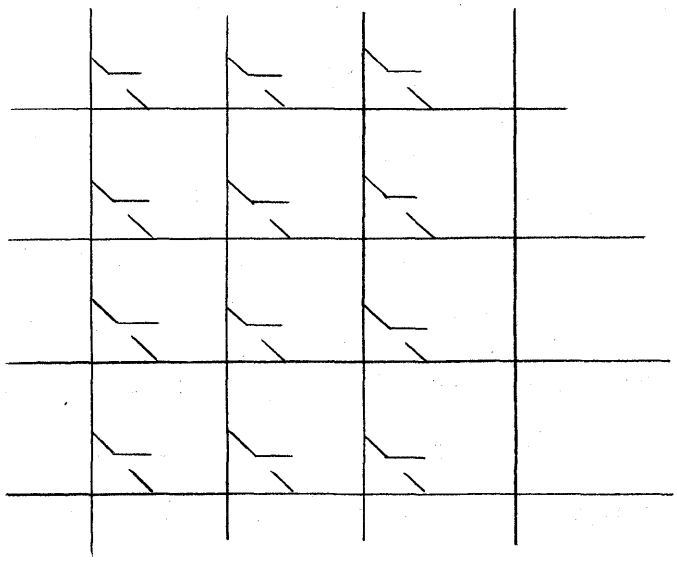
The printer itself may also control the printer time delay by means of the input on connector J3 pin 20 (zone A4). In this case either

a mark or space level may be used to inhibit data transmission, depending on whether the "2" or "3" jumper is installed (zone A3). Note that if the "2" jumper is used, the sense of the PRINTER CTS will be logically the same as the signal on J3-20. If the "3" is installed, the sense of PRINTER CTS will be the logical inversion of the signal on J3-20.

KEYBOARD THEORY OF OPERATION

Please refer to Drawing # 100037.

Each key of the keyboard occupies a position in a 16 x 16 matrix. Any switch closure will cause conducting path from one of the columns of the matrix to one of the rows of the matrix. A simplified diagram of this arrangement is shown below.



The full matrix is shown in the lower left hand corner of drawing 100037. The input to this matrix is a 74154 one of 16 decoder, and the output of the matrix is a 74150, 16 to 1 multiplexor. The select inputs to the 74150 pins 11, 13, 14, 15 are generated by a four stage binary counter (74LS298) in position A2.

The data inputs to the multiplexor are the 16 rows of the matrix. As A2 counts from 0 to 15, each of the 16 rows are sequentially gated to the output of the multiplexor (pin 10). When A2 resets to zero, it increments the counter (74LS298) in location A1. This counter supplies the inputs to the 74154 decoder in A12 which drives the 16 columns of the matrix.

Assume that the "P" key in position 32 of the matrix is depressed. If initially the counter in position A1 is at zero, column zero will be driven low. Since there are no switch closures in this column, the output of the 74150 (pin 10) will remain low since there is no conduction path from pin 1 on the 74154 (position 12) to any of the rows of the matrix. The rows are normally held high, unless driven low by a key closure, by the 4.7K pull up resistors to the left of the matrix. When A2 cycles from a count of fifteen to a count of zero, it will increment A1 and the decoded output of the 74154 (pin2) will drive column "1" low. The operation will continue until A2 has cycled from 0 to 15 a total of fifteen times since there are no switch closures in columns 0 through 14, and therefore the decoded outputs of A12 cannot be transferred to the row outputs. When the counter A2 makes its fifteenth transition from a count of fifteen to zero, A1 will be incremented to a count of 15. This count will be decoded and will drive pin 17 of A12 low. The signal is transferred via the contact closure of the "P" key to pin 8 of the 74150. ince this is the zeroth input of the multiplexor and since A2

and thus the selection lines of the 74150 is at zero, the low at pin 8 will be transferred to the inverted output of the 74150 (pin 10) as a high signal. This will cause pin 3 of the 74LS04 in location A5-4 to go high and the STOP- signal on its output pin 4 to go low. This signal forces the output of A8 pin 6 to go high unconditionally and inhibits the scan clock to A2, halting the counting of A2 and A1. Note that the code in A2 and A1 starting with SCAN 1 as the least significant bit and proceeding to SCAN 7, is 0001111 which is the USACII code for a "p". Thus by locating the key in the appropriate positions of the matrix, any of the USACII codes may be generated. Scan 1 through 4 are applied directly to the keyboard connector J1 on pins 9, 10, 11, and 12 respectively. The logic in the upper right hand corner of the drawing is to provide for generation of shift and control codes. Note that to shift the lower case alpha character residing in columns 4 and 5, bit six must be complimented. If the shift key is open, the input to the 74LS32 (A4-4) is high and A4-6 will be unconditionally high. If the alpha key is also open, both inputs to the 74LS00, A3-6 will be high causing pin 1 of the 74 LS86, A6-3 to be low. Under these conditions SCAN 6 at A6-2 will be passed to input pin of the 74LS08 (A7-13). If the control key is open, A7-12 will be high and SCAN 6 at A6-2 becomes KB06 at A7-11. If, however, the shift key is depressed, A4-4 will be low and A4-6 will be controlled by SCAN 7- on A4-5. If SCAN 7- is high, the A3-5 will be high and SCAN 6 will pass to KB06 as above. If, however, SCAN 7- is low, A4-6 will be low and A3-6 will be forced high. This will cause A6-1 to be high and will cause SCAN 6 on A6-2 to be inverted at A6-3 and subsequently KB06 will be the inversion of SCAN 6. This has the effect of moving the lower case character in columns 6 and 7 of the USACII code chart to columns 4 and 5 of the code

chart. The alpha key is an alternate action key. If this key is depressed, A3-4 will be low any time that SCAN 8 and SCAN 7 are high. Note that only the alpha characters occupy matrix columns having values greater than 12. When the alpha key is depressed by itself, A3-6 will be high and thus KB06 will be the inversion of SCAN 6 only when an alphabetical key is depressed. Thus the alpha key will be shifted but all others will not.

Now consider the logic generating KB05. If the input on pin 10 of the 74LS86 in position A6 is low, SCAN5 will pass to KB05 (A6-8) non-inverted. If, however, A6-10 is high, KB05 will be the inversion of SCAN5. If the shift key is open, the input on pin 9 of the 74LS32 in position A4 will be high and A4-8 will be unconditionally high. Thus the input to inverter (74LS04) A5-9 will be high and the output A5-8 will be low and subsequently A6-10 will be low. Under these conditions SCAN5 will have the same logical sense as A6-8.

Now assume that the shift key is depressed. This will cause pin 9 of the 74LS32 in position A4 to be low. Under these conditions, the output A4-8 will follow the A4-10 input. A4-10 is connected to the output of the two input NAND gate (74LS00) located in position A3-8. This output will be high unless SCAN8 on A3-10 and SCAN7- on A3-9 are both high. If A3-8 is high, A4-8 will be high and A5-8 and A6-10 will be low, again causing SCAN5 to have the same sense as KB05. Now note that if SCAN8 is true and SCAN7 false, the matrix columns greater than or equal to eight but less than twelve are specified. The only characters that meet these requirements are those in columns ten and eleven of the matrix. When SCAN8 is high and SCAN7- is high, A3-8 will be low, and since the shift key is depressed, A4-8 will follow A4-10 and be low causing A5-8 and A6-10 to be high. Under these conditions KB05 (A6-8)

will be the inversion of SCAN5 (A6-9). This results in the numeric and punctuation codes in matrix column 11 to be shifted from column three in the USACII code chart to column 2. Also the punctuations in matrix column 10 are shifted from column 2 of the USACII code chart to column 3. Now consider the control key. If this key is closed then the output of the inverter (74LS04) in position A5 will control the inputs A7-10 and A7-12 of the 74LS08 in A7. If SCAN7 is true at A5-1, A5-2 and subsequently A7-10 and A7-12 will be low forcing DB07 and KB08 low unconditionally. This will cause the codes in columns 4 or 6 to be moved to the zeroth control column and the code in columns 5 and 7 to be moved to the "1" control code column.

KEYBOARD STROBE CIRCUIT

The keyboard strobe is generated by a 74123 located in position A9-4. The time delay of this one shot is set at 30 milliseconds. Each time a scan clock is generated, the oneshot is retriggered via input A9-2. When the scan clock is stopped, the one shot time out and A9-4 rises until the key is released and the scan clock starts again.

SCAN CLOCK GENERATION

The scan clock is generated by a NE555. The NE555 in combination with the 510 Ω resistor network and the .001 µf capacitor form a 1 megahertz oscillator. The oscillator output on pin 3 is fed to one input of the dual NAND (74LS00) A8-5. The other input STOP- on A8-4 is used to stop the scan clock as previously discussed.

SHIFT LINE

The shift line to the unit is generated by A8-11. If this goes high, it indicates to the unit that the shift key has been depressed. If the shift key is depressed, SHIFT- goes from high to low at the input to th- dual and gate A7-1. This forces A7-3 and A8-13 to go low, forcing A8-11 high. If jumper "A" is installed, the shift line may also be forced

high, provided both inputs to the 74LS32, A4-1 and 2 are low. This occurs if the scanner detects a contact closure of the ESCAPE key since the ISCAPE key resides in column 2 and row 11 of the scan matrix. A4-1 and A4-2 going low causes A4-3 to go low. This in turn causes A7-2, A7-3, and A8-13 to go low, forcing the shift line A8-11 high. Jumper "A" is installed if it is desired to generate escape codes without using the shift key since the terminal will not recognize or process an escape cade unless the shift line is high.

REPEAT FUNCTION

When the repeat line is high (A8-3 and J1-7), the unit repeats the operation specified by the key which is depressed at the rate of 15 times per second. The repeat line is driven high if either input to the 74LS00 (A8-3) is low. One way in which this may occur is for pin 5 on the 74123 one shot in A9 to be low. This is the state of the oneshot which exists when the oneshot is not triggered. When the scanner is scanning and no coincidence is found, pin 10 (STOP) of the 74150 and pin 5 of the dual and gate (74LS08) A7-5, will be low. Therefore, A7-6 and pin 9 of the oneshot A9 will be low. Under this condition, the oneshot will remain high. When a key depression is detected by the scanner, pin 10 of the 74150 goes high, causing A7-5 to go high. Assuming that A7-4 is high, A7-6 and A9-9 will go high. The oneshot will then stop retriggering and A9-5 will go low when the oneshot times out after 500 milliseconds. The low on A9-5 causes A8-1 to go low and A8-3 is forced high, generating a repeat signal to the terminal control logic via connector J1 pin 7. Pin A7-4 of the 74LS08 A7 is used to prevent repeating an escape code. If the dual OR gate (74LS32) in A4-3 detects an escape code, A4-3 will go low, foring A7-4 low. This will in turn force A7-6 and A9-9 low insuring that the oneshot continues to retrigger and A9-5 and A8-1 stay high.

CLEAR KEY

There are two jumper options to the clear key. If jumper "B" is installed, the clear key is placed in series with the shift key, and a clear operation may be performed only if the shift key is depressed along with the clear key. If jumper "C" is installed, the common of the clear key is grounded, and a clear operation is performed any time the clear key is depressed. Closing the clear key causes the shift, control, and repeat lines to go high simultaneously. This is detected as a hardware clear to the unit.

VIDIO MONITOR

Please refer to Dwg. # 100090 Sheet 1.

The purpose of the regulator subassembly is to supply a regulated +5 volts to the logic and to supply +15 volts for use in the monitor. The maximum current capacity of the 5 volt regulator is 5 ams., and the capacity of the fifteen volt regulator is 1.5 amps.

The monitor consists of a vidio monitor unit and the power supply regulators for the entire terminal.

FIVE VOLT REGULATOR

The five volt regulator takes an input of 9.4 VAC on connector J1 pins 1 and 4. The AC is rectified by a bridge rectifier circuit made up of CR1-CR4. The output of the bridge is filtered by an 15,000 uf capacitor. The positive leg of the bridge is connected to pin 1 of the 78105 regulator. The reference pin (pin 3 of the 78105) is connected to the wiper and one side of a 100 ohm potentiometer. This side of the potentiometer is connected in series with a 3.3n resistor to the output pin 2 of the regulator. The other side of the potentiometer is connected to the negative leg of the bridge. The purpose of the 100 ohm pot is to provide an approximately $\pm$ 10 percent adjustment to the nominal 5 volt

output. The regulated output is filtered by a 47 mf capacitor, and the positive output is fed to pin 1 of connector J2. J2-2 is the return output.

15 VOLT REGULATOR

Refer to Dwg. # 100054. The AC input is connected to connector J1 pins 5 and 6, and the output is connected to J3, with J3-3 being the positive output and J3-2 being the return. This circuit is identical to the five volt regulator circuit with the exception that the bridge output is filtered by a 3300 f capacitor. The regulators are two 7815KC (15 volt regulators), and the output filter is a .1 f capacitor. The vertical and horizontal circuits have separate regulators which are supplied from the same bridge. The input to this circuit is 20.6 vac.

THEORY OF OPERATION

VIDEO AMPLIFIER

The video amplifier consists of Q5, R24, R21, R22, R23 and C19.

The incoming video signal is applied to the monitor through the contrast control and R24 to the base of Q5. Transistor Q5 and its components comprise a video amplifier with a gain of around 18. Q5 operates as a class-B amplifier and reamins cutoff until a DC-coupled, positive going signal arrives at its base. R23 provides series feedback which makes the voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variation. C19 bypasses the AC signal around the biasing network. The negative going signal at the collector of Q5 is DC-coupled to the cathode of the CRT. The class "B" biasing of the video driver allows a large video output signal to modulate the CRT'S cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

VERTICAL DEFECTION

Transistor Q6 is a programmable unijuntion transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R33, variable resistor PR4 and capacitors C3 and C4 form an RC network providing proper timing for the vertical section.

As power is applied, C3 and C4 change exponentially through R33 and PR4 until the voltage at the junction of PR4 and C3 equals the anode "A" firing voltage. At this time, one of the unijunction's internal diode that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R29.

R27 and R28 control the voltage at which the unijunction anode-to-anode gate becomes forwards biased. This feature "programs" the firing of Q6 and prevents the unijunction from controlling this parameter. The logic board supplies a negative going pulse to the vertical section through R26, C20, CR12, which lowers the gate of Q6 momenterally, causing it to fire, thus keeping it locked to the vertical frequence. The sawtooth voltage at the anode of Q6 is directly coupled to the base of Q7. Q7 is a driver amplifier consisting of two transistors in a darlington configuration. They are packaged together as a 3 terminal device. The output waveform from the unijunction transistor is not yet suitable to produce a satisfactory vertical sweep at this point, the waveform would produce severe striching at the top of screen and comprission on the bottom. A portion of the signal from Q7 is feed back through R32 and PR6 to the junction of C3 and C4 introducing a correction signal. The amount of this signal is determined by PR6. Q7 supplies base current through R31 and PR5 to the vertical output transistor Q8. Height control PR5 varies the amplitude of the sawthooth voltage present at the base of Q8 and varies the size of the vertical raster on the CRT.

The vertical output stage, Q8 uses a power transistor which operates as a class "A" amplifier. The output impedance of this device permits it to be directly coupled to the yoke from the collector. C21 is a DC blocking capacitor which allow only the AC voltages to produce yoke current. L4 is a relatively high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L4 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. R35 prevents oscillations by providing damping across the vertical deflection coil.

HORIZONTAL DEFLECTION

A positive going pulse is coupled through R5 to the base of Q3. The driver stage is either cut off or driven into saturation by the base signal. The output is a retangular waveform, and is transformer coupled to the base of the horizontal output stage. The buffer transformer's polarities are such that when Q3 is on Q4 is off and vise versa. During conduction of Q3, energy is stored in the buffer transformer. The voltage at the secondary is then positive and keeps Q4 cut off. As soon as the primary current of the buffer transformer is interrupted due to base signal driving Q3 into cut off, the secondary voltage changes polarity. Q4 startes conducting and its base current starts to flow. This gradually decreases at a rate determined by the transformer induction and circuit resistance.

The horizontal output stage has five main functions:

1. supply the yoke with horizontal sweep current.
2. supply +35V for vidio amplifier section.
3. supply -125V for CRT Baising.
4. supply +440V for CRT Drive.
5. supply 12KV for CRT.

Q6 acts as a switch which is turned on or off by the rectangular waveform on the base. This action supplies a square-wave pulse to power the flyback and horizontal sweep circuit. CR9 Damper diode, keeps the flyback from over oscillating.

L-2 adjust the amount of current in the horizontal sweep which adjusts the width. L-3, C-16, R3 adjust the horizontal sweep current waveform for horizontal linearity, C24 provides DC vlcoking and also provides "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube as the curvature of

the CRT face and deflection beam do not describe the same arc. The flyback retrace pulse is transformed through the secondary winding of the flyback, which is a multi voltage secondary, where it is rectified by CR6, CR7, CR8 and the high voltage rectifier in the anode lead of the flyback to provide the CRT with high voltage, the focuse and video amplifier operating voltage.

5 VOLTS

The A.C. winding for the 5 volt supply comes in on the sweep board through PSJ1, Pins 1 and 4. The AC voltage is rectified by diodes CR1, CR2, CR3, CR4 and filtered by C23. The unregulated DC from the filter is regulated through Q9 down to 5.1VDC. PR3 is an adjustment for the 5V regulator. 15 Volts for sweep comes in as PSJ1, Pins 5 and 6. CR5 and C22 rectify and filter the AC voltage. Q2 and Q1 regulate the vertical and horizontal 15V supply for the sweep electronics. PR7 adjust the horizontal 15V this should be set to obtain a reading of 15.75V $\pm$ 10%.

TOP CHASSIS WIRING

Please refer to Dwg. # 100031.

Primary AC Circuit

The primary AC circuit consists of the circuit breaker, the power ON-OFF switch, the fan, and the primary of the transformer. The black lead of the power cord is wired to pin 2 of the circuit breaker. The circuit breaker is wired in series with the transformer primary winding red lead) is connected to this position of the fan. The other side of the transformer primary winding is connected to the other fan terminal. This in turn is connected to the white lead of the AC power cord. The green lead of the AC power cord is connected to the chassis of the terminal.

TRANSFORMER SECONDARY

The transformer secondary consists of three windings:

1. 16.5 VAC volts used for the generation of the regulated $\pm$12 volts on the logic board.
2. 9.4 VAC used for generation of the regulated 5V on the power supply.
3. 20.6 VAC used for generation of the regulated +15 volts on the power supply.

See the exploded drawing number 100031. The violet leads (16.5 VAC) from the transformer are connected to connector Logic P2 at pins 1 and 4. The center tap of this winding (violet/white wire) is connected to pin 3 of Logic P2.

Pins 1 and 2 of power supply P2 carry the regulated +5 volts DC to the logic board. Connector Logic P2 as shown below:

2----------+5 volts P.C. (black)----------2

1----------+5 volt return (white)----------6

Logic P2 0,S, 02

FIGURE 5-1 +5 VOLT LOGIC CONNECTOR

Logic P2 is plugged into the logic board as shown in figure 100031. The 9.4 VAC (green wires) from the transformer are connected to pins 1 and 3 of connector power supply P1, and the 20.6 VAC (blue wires) from the transformer are connected to pins 4 and 6 of power supply P1. This connector is plugged into the power supply as shown in Dwg. #100031. Logic connector P1 carries the drive signals for the speaker used to generate a "beep" when CTRL G is issued to the terminal, and the video and drive signal for the video monitor.

The monitor connector is designated MONP1 on drawing 100031. Connector power supply P3 is used to carry the regulated +15 volts DC to the monitor via MONP1. The pin assignments for these connectors are shown in Fig. 5-2.

Connector Logic P1	Function	Color	Connector MON P1	Function	Color	Connector P.S. P2
6	Speaker	Yellow				
9	Speaker	Brown				
7	GND	White	1			
1	Brightness Pot	Orange	2			
3	Brightness Pot	Blue	3			
2	Brightness wiper	Red	4			
10	Horizontal Drive	Black	6			
5	Video	Violet	8			
11	Vertical Drive	Gray	9			
8	Video GND	White	10			
			7	+15 VDC	Black	3
			5	+15 VDC Return	White	2

FIGURE 5-2 LOGIC CONNECTOR P1, MONITOR CONNECTOR P1 AND POWER SUPPLY CONNECTOR P2

VI

SCHEMATIC DRAWINGS AND DIAGRAMS

All assy, logic and schematics

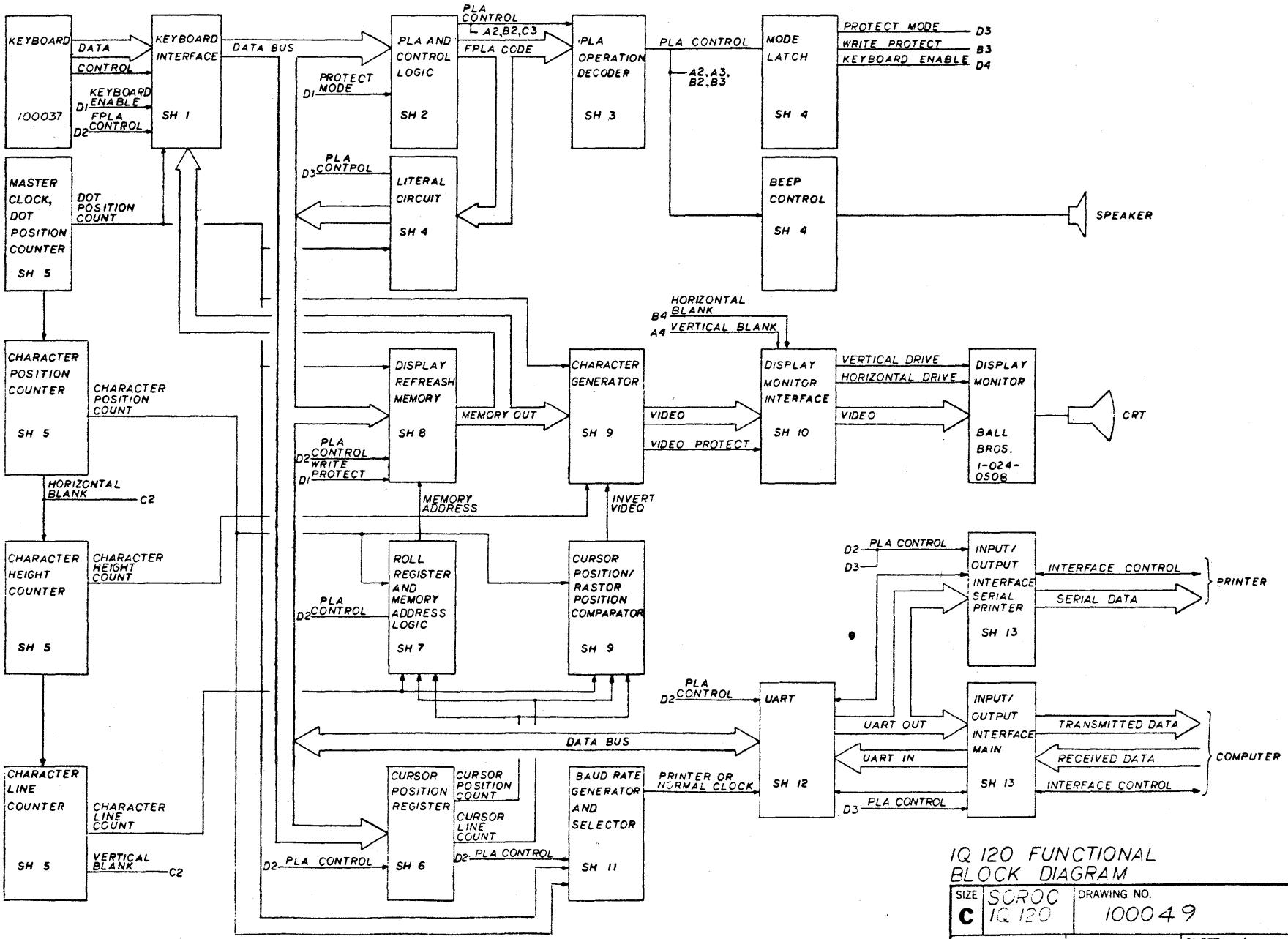
All drawings

-------assembly drawing

-------logic drawings

------- all schematics

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



IQ 120 FUNCTIONAL BLOCK DIAGRAM

SIZE	SCROC IQ 120	DRAWING NO. 100049
C		
SCALE		SHEET – 1 OF 1

DWG NO.

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
490001	490001				

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES	SOROC TECHNOLOGY, INC. 165 FREEDOM AVE. ANAHEIM CALIFORNIA
APPROVALS / DATE	
DRAWN	LOGIC BOARD ASSY IQ120
J Hartley 9/27/79	SCALE 1-1 / SIZE A / DRAWING NO. ML200003-9
CHECKED	
	DO NOT SCALE DRAWING / SHEET 1 OF 5

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: LOGIC BOARD ASSY. IO120

ML 200003-9

SHT 2 OF

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
1	100066-9	120 LOGIC PCB		1							
2											
3	600000	7400		8							
4	600002	7402		1							
5	600004	7404		7							
6	600008	7408		10							
7	600010	7410		4							
8	600011	7411		1							
9	600020	7420		1							
10	600027	7427		4							
11	600032	7432		5							
12	600037	7437		1							
13	600042	7442		6							
14	600074	7474		4							
15	600083	7483		2							
16	600085	7485		3							
17	600086	7486		1							
18	600090	7490		2							
19	600093	7493		3							
20											
21											
22	600109	74109		3							
23	600123	74123		1							
24	600150	74150		1							
25	600157	74157		8							
26	600161	74161		4							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: LOGIC BOARD ASSY. IQ120

ML 200003-9

SHT 3 OF

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
27	600163	74163		10							
28	600166	74166		1							
29	600173	74173		2							
30	600174	74174		2							
31	600175	74175		3							
32	600193	74193		7							
33	601010	74LS10		1							
34	602113	74S113		3							
35	602257	74S257		2							
36	603000	74H00		1							
37	604000	1488		2							
38	604001	1489		3							
39	604002	1602 OR UART AY5-1013		1							
40	604003	2120/21L02B		16							
41	604006	LG1A (82S101)		1							
42	604007	LG2B (82S101)		1							
43	604012	MCM65700P CHARACTER		1							
44											
45											
46	705102	5% ¼W 1K		2							
47	705151	5% ¼W 150 OHM		1							
48	705202	" " 2K		1							
49	705203	" " 20K		2							
50	705271	" " 270 OHM		1							
51	705472	" " 4.7 K		33							
52	705681	" " 680 OHM		1							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE:

DRAWN:

CHK:

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO:

QUANTITY

REV

TITLE: LOGIC BOARD ASSY. IQ 120

ML 200003-9

SHT 4 OF

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
53											
54											
55	715151	5% ½W 150 OHM		1							
56	725241	5% 1W 240 OHM		1							
57	784473	4.7K RESISTOR PACK -8PIN		1							
58											
59											
60	800001	100 PF 50V DISC		1							
61	800006	0.01 UF 100V DISC		11							
62	800203	15UF 20V AXIAL		9							
63	800204	100UF 20V AXIAL		3							
64	800207	900MFD 35V AXIAL		2							
65											
66											
67											
68	900000	KSP-16-6 KONEX POLAR LOCK,SOCKET		1							
69	900002	SOCKET 24 PIN SOLDER		1							
70	900003	SOCKET 28 PIN SOLDER		2							
71	900004	SOCKET 40 PIN SOLDER		1							
72	900200	25 PIN CONNECTOR 206584-1 AMP		2							
73	900201	6 PIN WAFER CONN. 09-18-5061		1							
74	900202	12 PIN WAFER CONN. 09-18-5121		1							
75	905000	IN914		4							
76	905001	IN4733 5V		1							
77	905002	IN4742 12V		1							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

TITLE: _____

REV

ML

SHT 5 OF

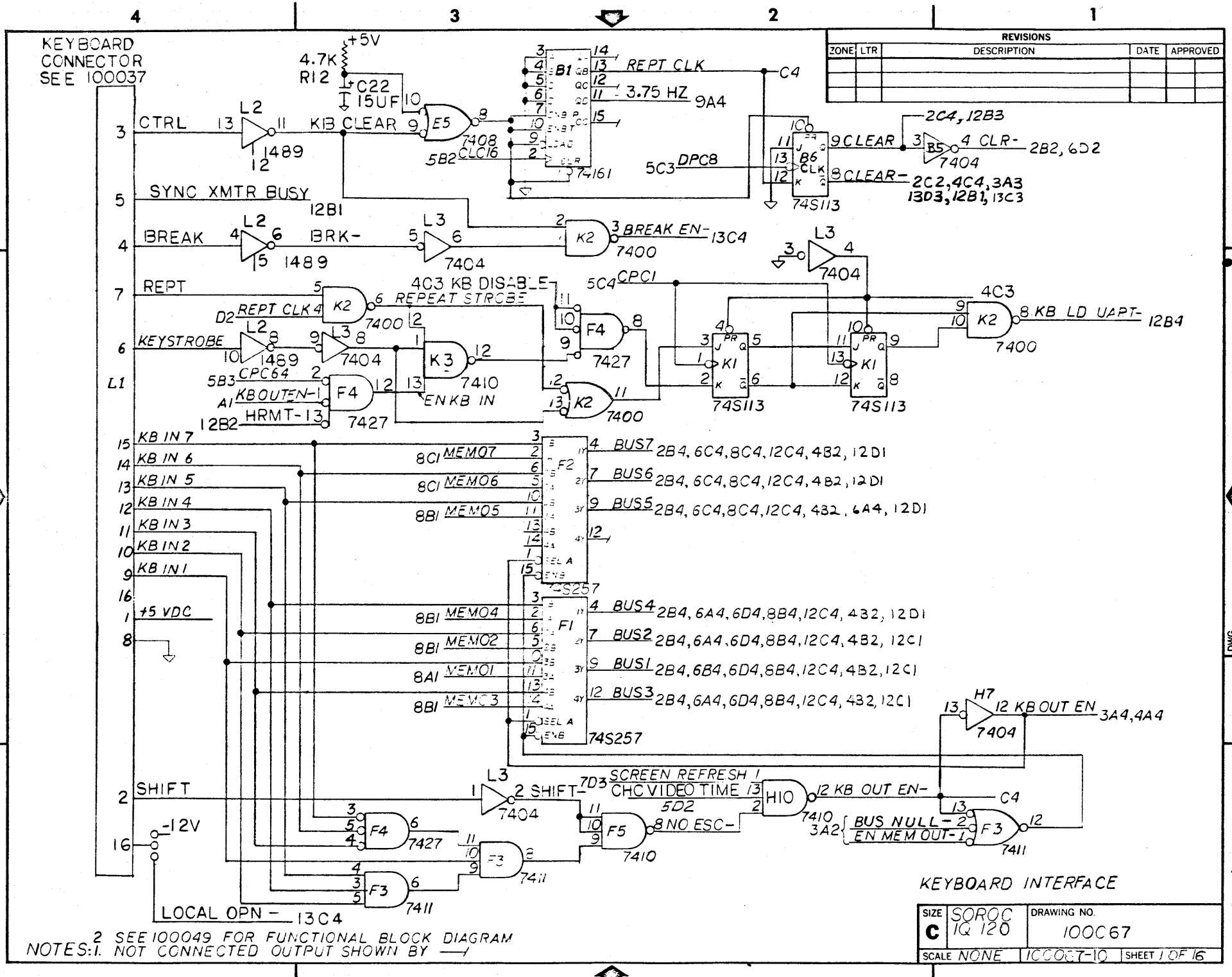
ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
79											
80											
81	905300	500 OHM BM6011 CTS		1							
82	905301	100 K BM6010 CTS		1							
83	905401	WO 2 G1 BRIDGE		1							
84	905402	CRYSTAL 10.9200 MH2		1							
85	905600	1X2323-3000 SAE LA2150315		1							
86	905602	MSS4350R		1							
87	905700	8 POS. DIP SWITCH 1008692 SAE		1							
88	905800	MC7912-CD VOLT. REG.		1							

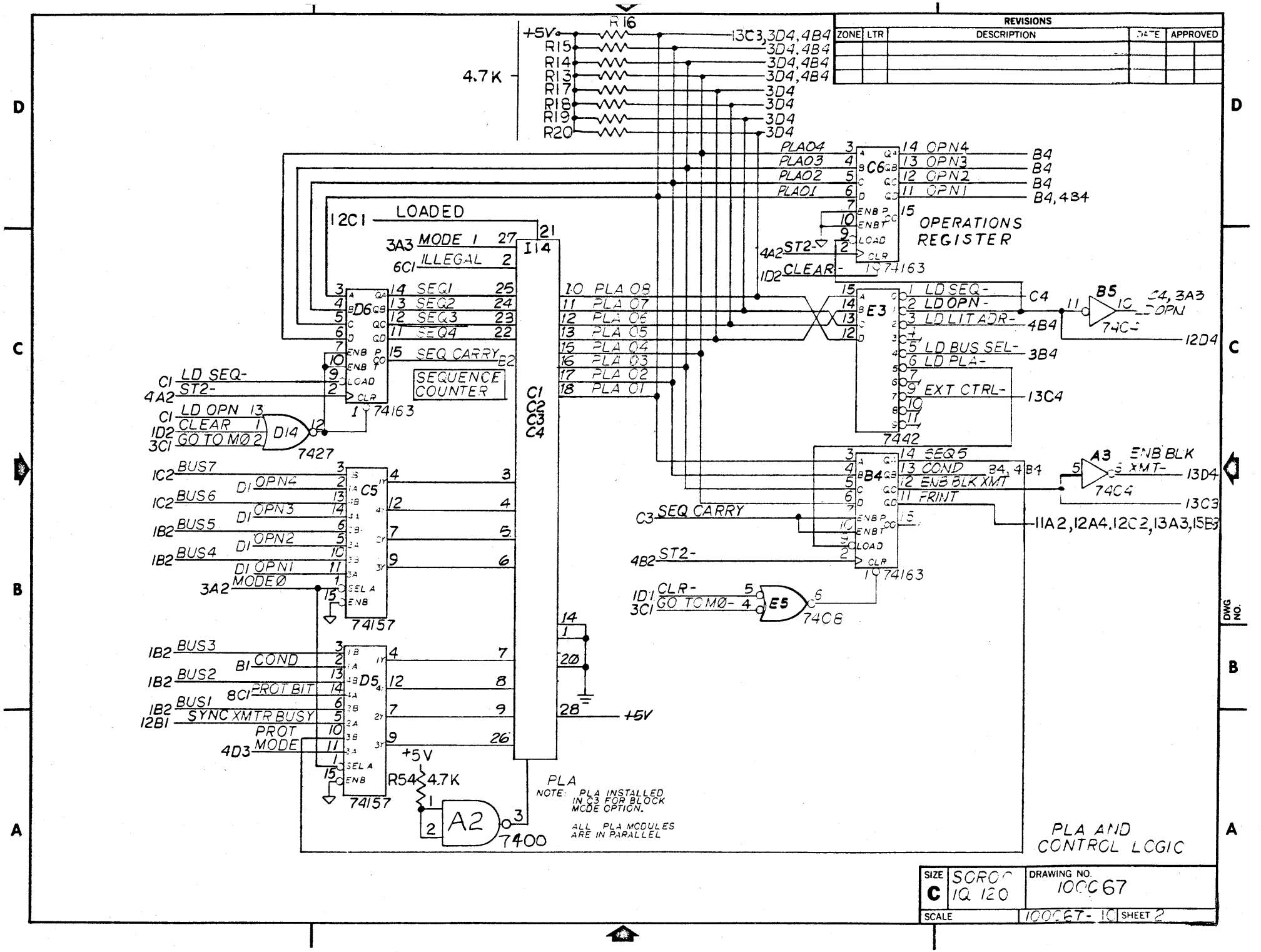
NOTES:

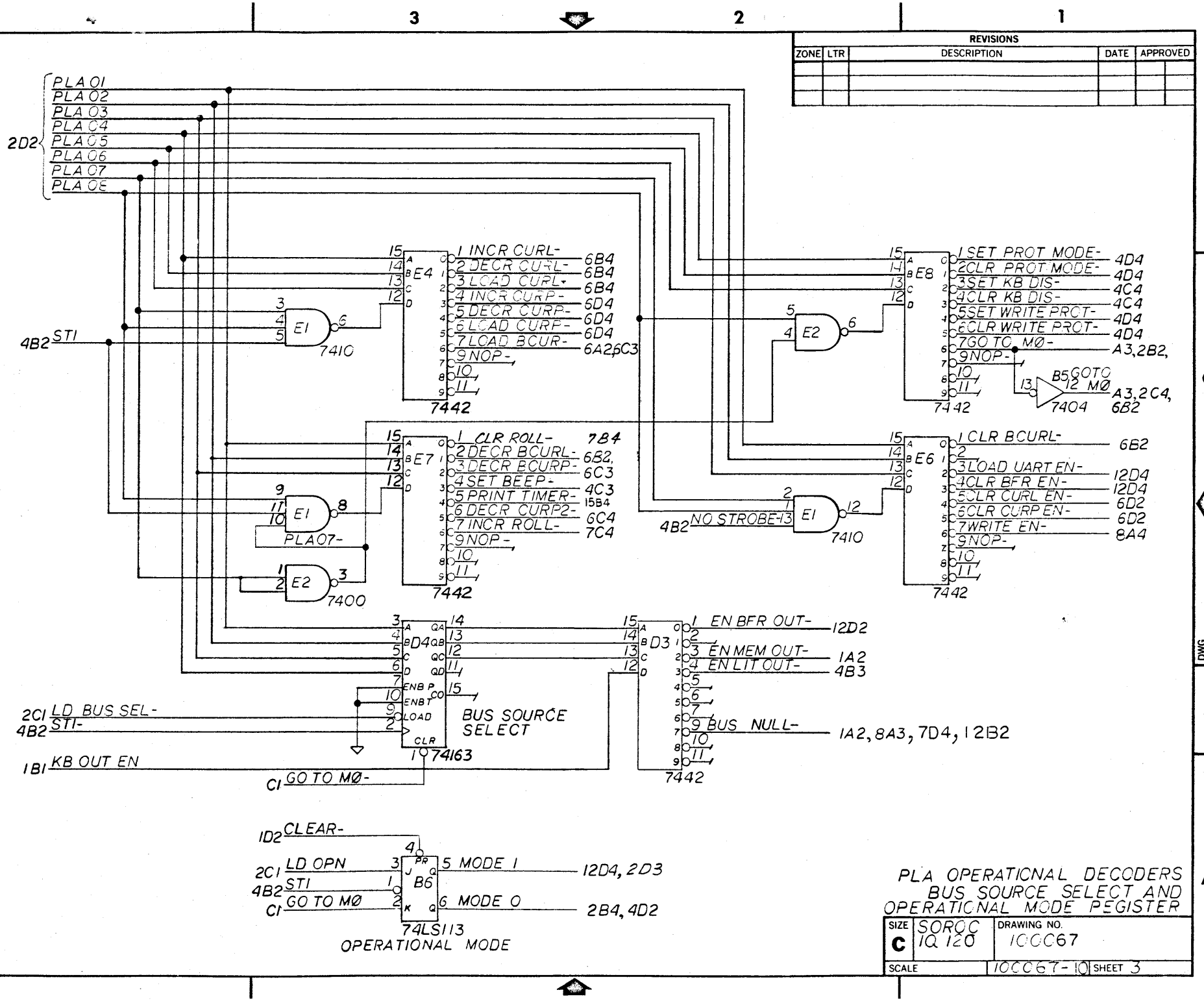
DATE KIT STAGED

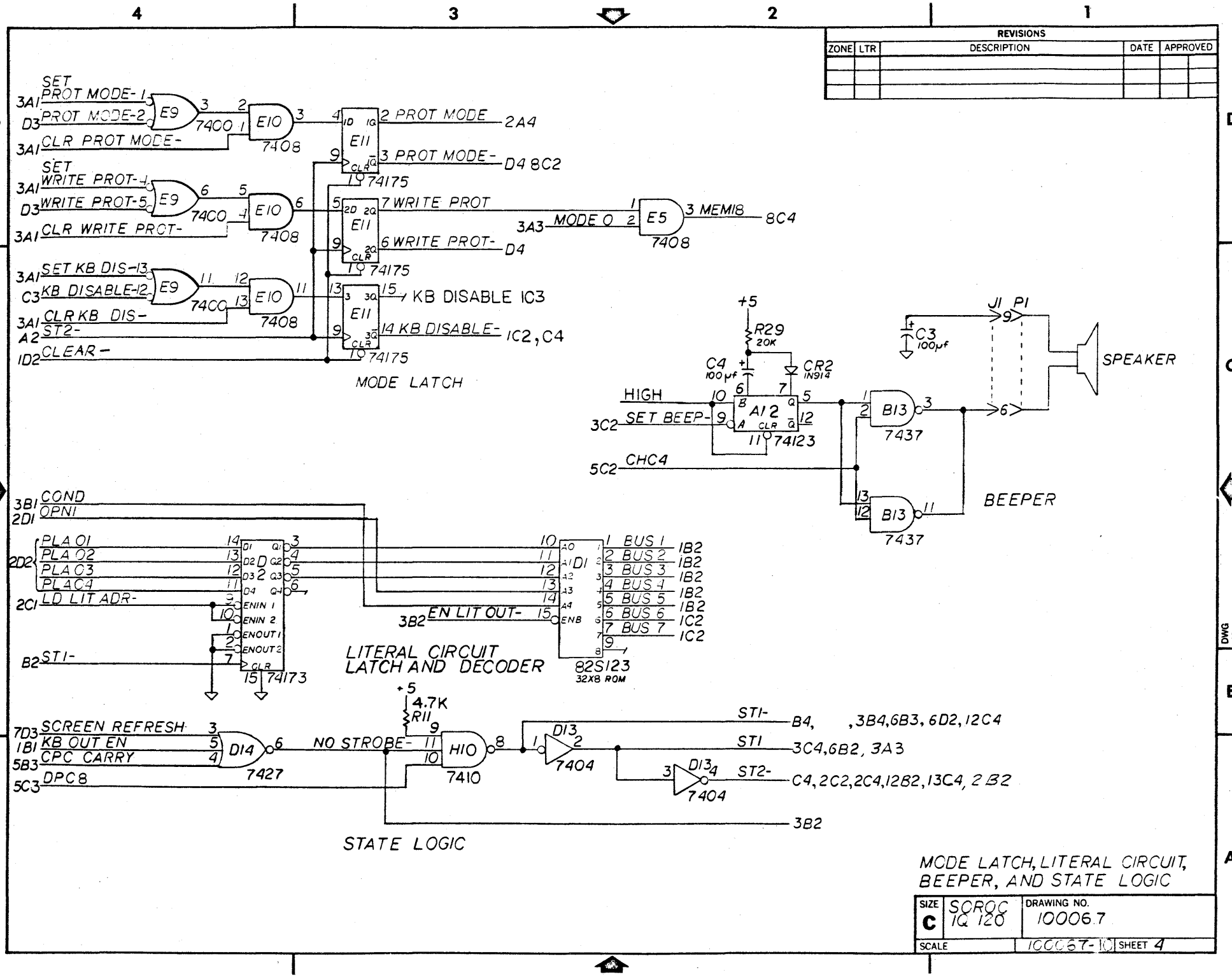
DATE KIT RELEASED

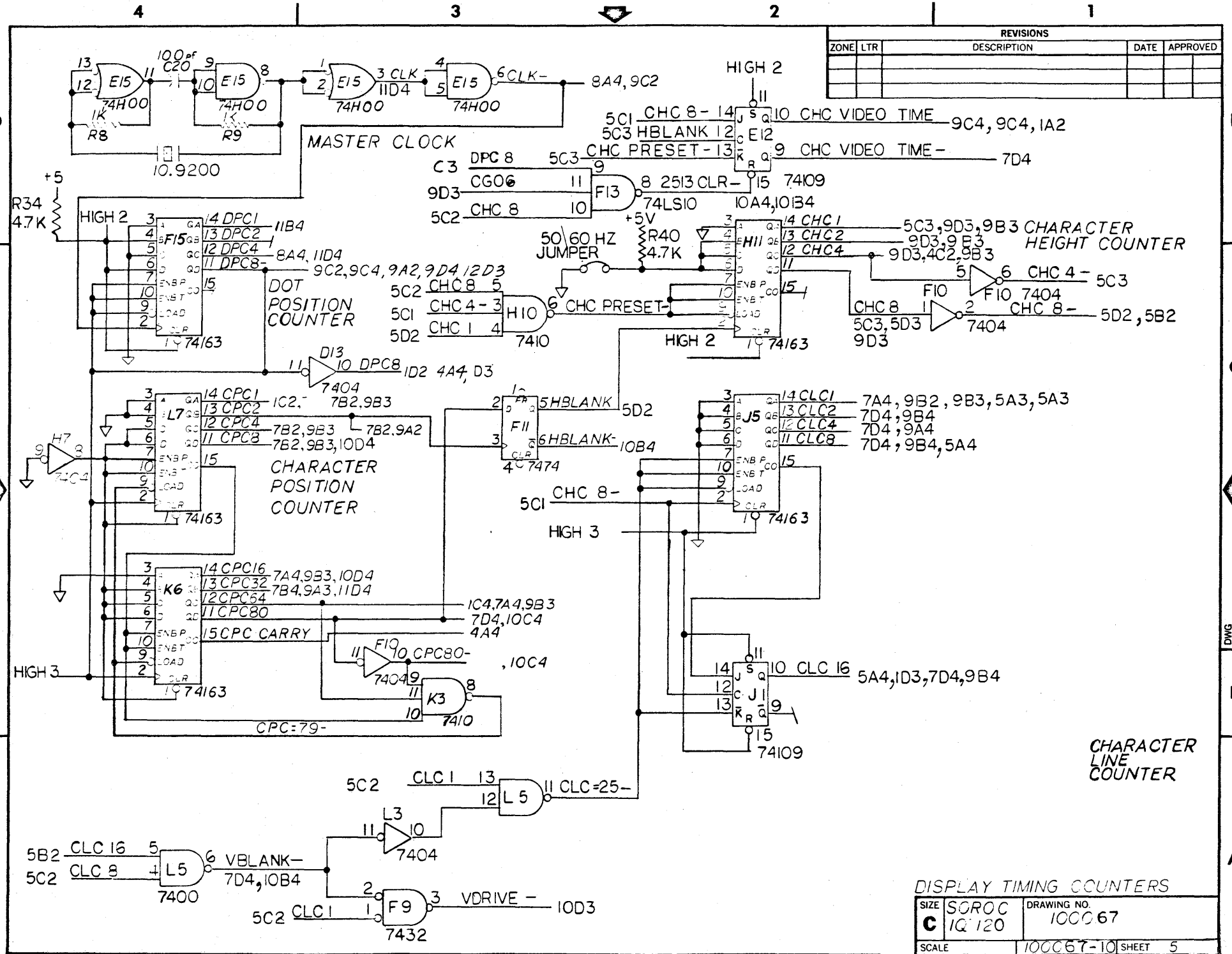
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		SOROC TECHNOLOGY, INC.		
APPROVALS	DATE	165 FREEDOM AVE. ANAHEIM CALIFORNIA		
D Sutton DRAWN	11/6/79	LOGIC BOARD ASSY.		
D Headley CHECKED	11/6/79	SCALE 1-1	SIZE D	DRAWING NO. 200003-10
D Mello	11-6-79	DO NOT SCALE DRAWING	SHEET 1 OF	

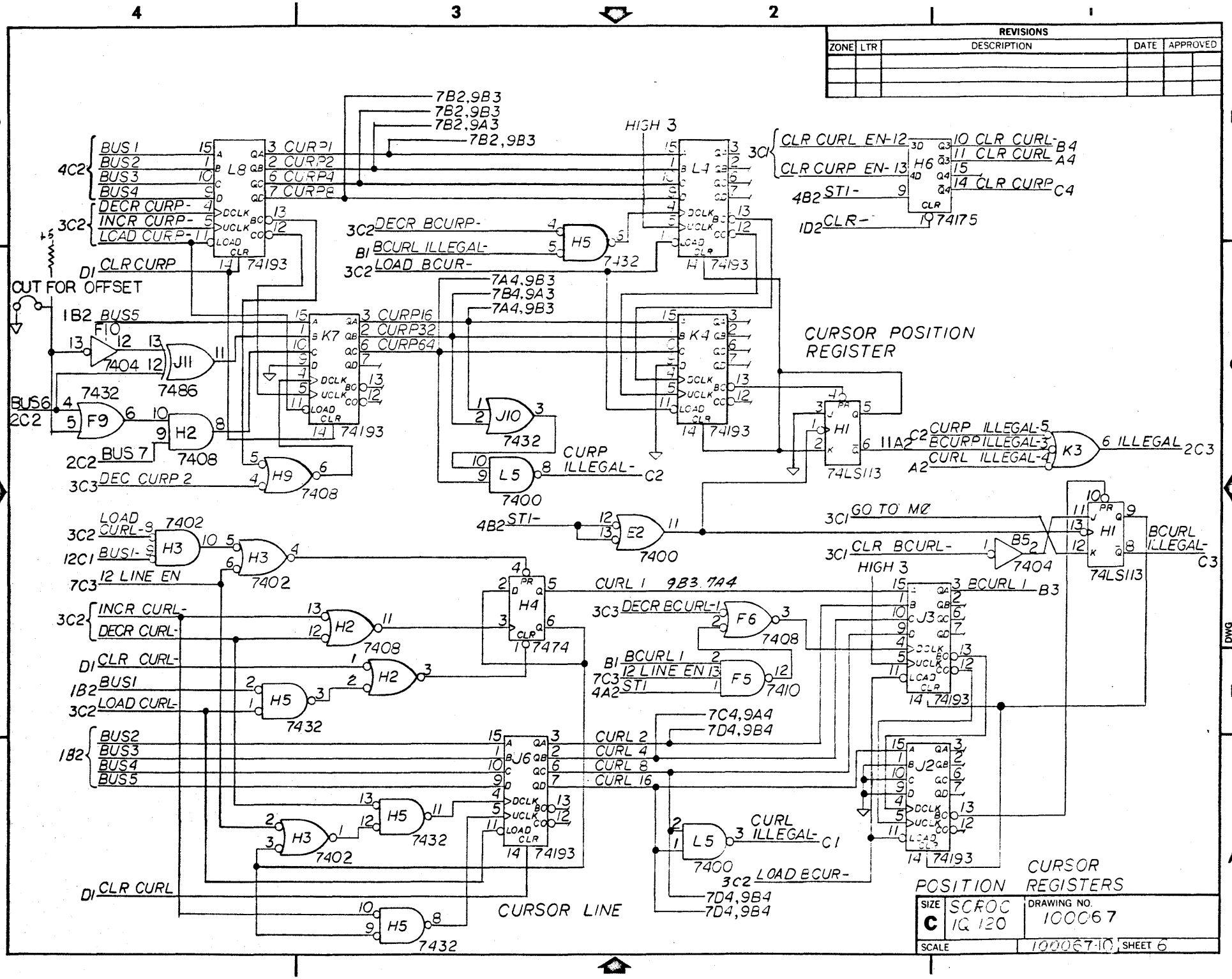

KEYBOARD CONNECTOR SEE 100037
+5V
4.7K R12
C22 15UF
CTRL
KB CLEAR
1489
7408
5B2 CLC16
B1
REPT CLK
3.75 HZ
9A4
C4
74161
5C3 DPC8
74S113
2C4, 12B3
9 CLEAR
4 CLR-
2B2, 6D2
7404
8 CLEAR-
2C2, 4C4, 3A3
13D3, 12B1, 13C3
SYNC XMTR BUSY
12B1
BREAK
IBRK-
BREAK EN-
13C4
7400
7404
REPT
REPT CLK 4
REPEAT STROBE
4C3 KB DISABLE
5C4 CPC1
KEYSTROBE
CPC64
5B3
KBOUTEN-1
A1
HRMT-13
12B2
ENKB IN
7410
7427
8 KB LD UAPT-
12B4
KB IN 7
KB IN 6
KB IN 5
KB IN 4
KB IN 3
KB IN 2
KB IN 1
+5 VDC
8C1 MEMO7
8C1 MEMO6
8B1 MEMO5
8B1 MEMO4
8B1 MEMO2
8A1 MEMO1
8B1 MEMO3
BUS7 2B4, 6C4, 8C4, 12C4, 4B2, 12D1
BUS6 2B4, 6C4, 8C4, 12C4, 4B2, 12D1
BUS5 2B4, 6C4, 8C4, 12C4, 4B2, 6A4, 12D1
BUS4 2B4, 6A4, 6D4, 8B4, 12C4, 4B2, 12D1
BUS2 2B4, 6A4, 6D4, 8B4, 12C4, 4B2, 12C1
BUS1 2B4, 6B4, 6D4, 8B4, 12C4, 4B2, 12C1
BUS3 2B4, 6A4, 6D4, 8B4, 12C4, 4B2, 12C1
74S257
H7
12 KB OUT EN
3A4, 4A4
SHIFT
2 SHIFT-
7D3
SCREEN REFRESH 1
CHC VIDEO TIME
5D2
H10
12 KB OUT EN-
C4
8 NO ESC-
BUS NULL-2
EN MEM OUT-1
3A2
-12V
LOCAL OPN -
13C4
SEE 100049 FOR FUNCTIONAL BLOCK DIAGRAM
NOTES: 1. NOT CONNECTED OUTPUT SHOWN BY —/
KEYBOARD INTERFACE
SIZE C
SOROC IQ 120
DRAWING NO. 100067
SCALE NONE
ICCOCT-10
SHEET 1 OF 16
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED

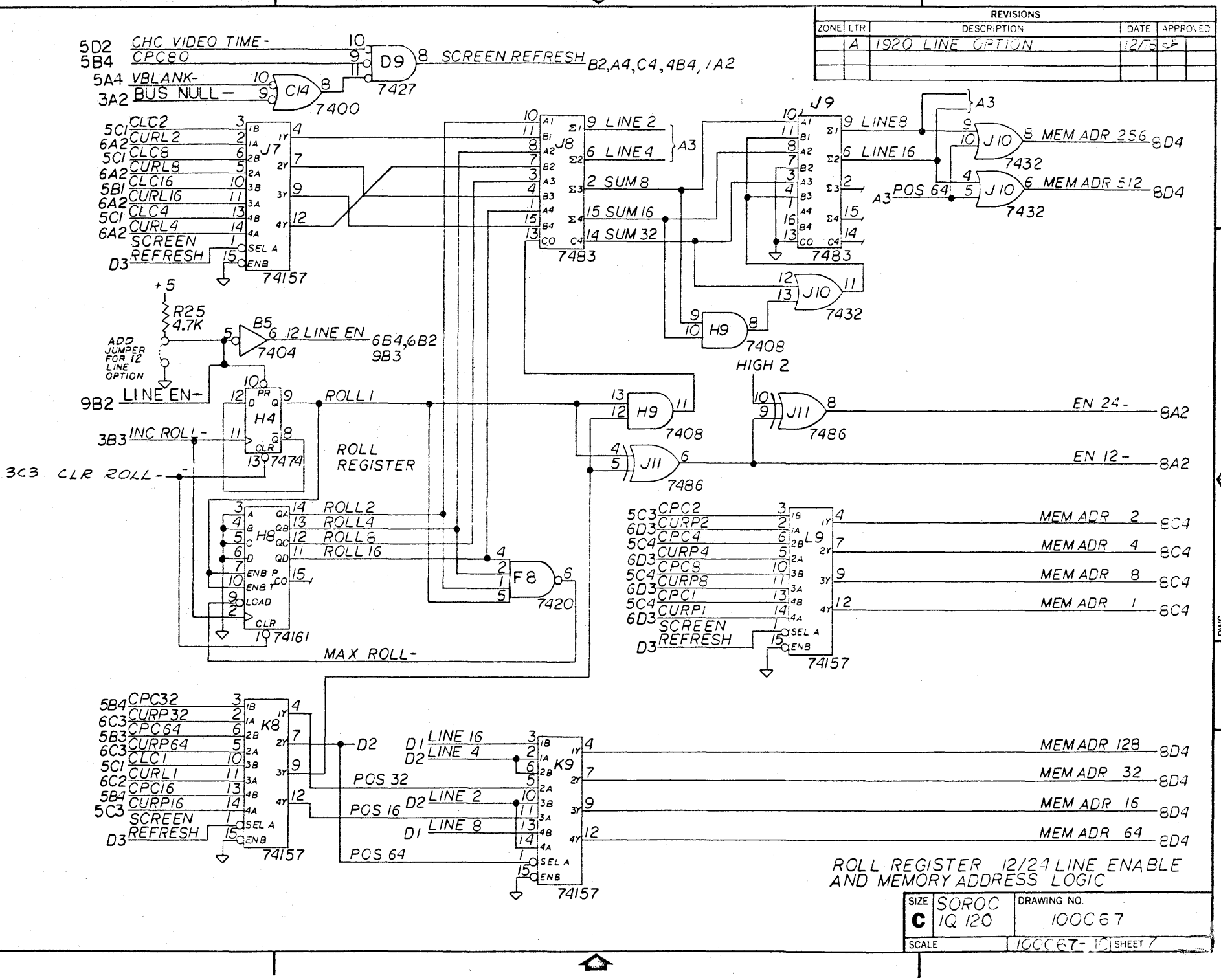

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
+5V
R16
R15
R14
R13
R17
R18
R19
R20
4.7K
13C3,3D4,4B4
3D4,4B4
3D4,4B4
3D4,4B4
3D4
3D4
3D4
3D4
PLA04
PLA03
PLA02
PLA01
C6
14 OPN4
13 OPN3
12 OPN2
11 OPN1
B4
B4
B4
B4,4B4
OPERATIONS REGISTER
74163
4A2 ST2-
1D2 CLEAR-
12C1 LOADED
3A3 MODE 1
6C1 ILLEGAL
D6
14 SEQ1
13 SEQ2
12 SEQ3
11 SEQ4
15 SEQ CARRY
E2
SEQUENCE COUNTER
74163
C1 LD SEQ-
4A2 ST2-
C1 LD OPN
CLEAR
3C1 GO TO MØ 2
D14
7427
I14
10 PLA 09
11 PLA 07
12 PLA 06
13 PLA 05
15 PLA 04
16 PLA 03
17 PLA 02
18 PLA 01
C1
C2
C3
C4
E3
1 LD SEQ-
2 LD OPN-
3 LD LIT ADR-
5 LD BUS SEL-
6 LD PLA-
9 EXT CTRL-
7442
C4
4B4
3B4
13C4
B5
74C4
C4, 3A3 LD OPN
12D4
B4
14 SEQ5
13 COND
12 ENB BLK XMT
11 FRINT
B4, 4
A3
74C4
ENB BLK XMT-
13D4
13C3
11A2,12A4,12C2,13A3,15B3
C3 SEQ CARRY
4B2 ST2-
74163
1D1 CLR-
3C1 GO TO MØ-
E5
74C8
IC2 BUS7
IC2 BUS6
IB2 BUS5
IB2 BUS4
3A2 MODEØ
C5
DI OPN4
DI OPN3
DI OPN2
DI OPN1
74157
IB2 BUS3
IB2 BUS2
IB2 BUS1
12B1 SYNC XMTR BUSY
4D3 PROT MODE
8C1 PROT BIT
BI COND
D5
74157
+5V
R54 4.7K
A2
7400
14
1
20
28
+5V
PLA
NOTE: PLA INSTALLED IN C3 FOR BLOCK MODE OPTION.
ALL PLA MODULES ARE IN PARALLEL
PLA AND CONTROL LOGIC
SIZE C
SCALE
SOROC IQ 120
DRAWING NO. 100067
100067-10 SHEET 2
DWG NO.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
PLA 01
PLA 02
PLA 03
PLA 04
PLA 05
PLA 06
PLA 07
PLA 0E
2D2
4B2 STI
E1
7410
E4
1 INCR CURL-
2 DECR CURL-
3 LOAD CURL-
4 INCR CURP-
5 DECR CURP-
6 LOAD CURP-
7 LOAD BCUR-
9 NOP-
10
11
7442
6B4
6B4
6B4
6D4
6D4
6A2,6C3
E2
7400
E7
1 CLR ROLL-
2 DECR BCURL-
3 DECR BCURP-
4 SET BEEP-
5 PRINT TIMER-
6 DECR CURP2-
7 INCR ROLL-
9 NOP-
7B4
6B2,
6C3
4C3
15B4
6C4
7C4
PLA07-
4B2 NO STROBE-13
E8
1 SET PROT MODE-
2 CLR PROT MODE-
3 SET KB DIS-
4 CLR KB DIS-
5 SET WRITE PROT-
6 CLR WRITE PROT-
7 GO TO MØ-
9 NOP-
4D4
4D4
4C4
4C4
4D4
4D4
A3,2B2,
B5 GOTO 12 MØ
A3,2C4,
6B2
7404
E6
1 CLR BCURL-
3 LOAD UART EN-
4 CLR BFR EN-
5 CLR CURL EN-
6 CLR CURP EN-
7 WRITE EN-
9 NOP-
6B2
12D4
12D4
6D2
6D2
8A4
D4
D3
1 EN BFR OUT-
3 EN MEM OUT-
4 EN LIT OUT-
9 BUS NULL-
12D2
1A2
4B3
1A2, 8A3, 7D4, 12B2
2C1 LD BUS SEL-
4B2 STI-
BUS SOURCE SELECT
74163
1B1 KB OUT EN
C1 GO TO MØ-
1D2 CLEAR-
2C1 LD OPN
4B2 STI
C1 GO TO MØ
B6
5 MODE 1
6 MODE 0
12D4, 2D3
2B4, 4D2
74LS113
OPERATIONAL MODE
PLA OPERATIONAL DECODERS
BUS SOURCE SELECT AND
OPERATIONAL MODE REGISTER
SIZE C
SOROC IQ 120
DRAWING NO. 10CC67
SCALE
10CC67-10 SHEET 3
DWG NO.

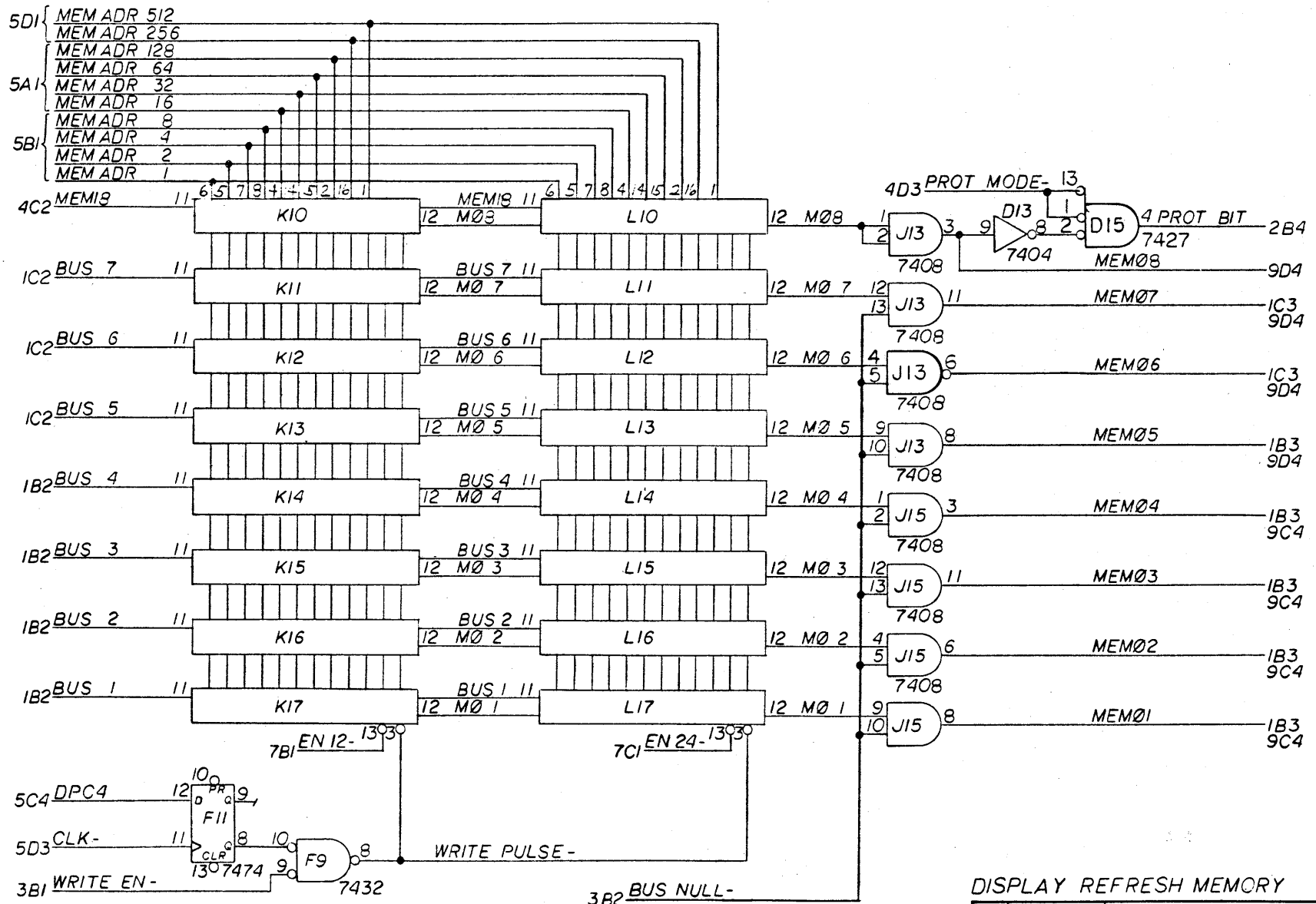

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
SET PROT MODE-1
3A1 PROT MODE-2
D3 CLR PROT MODE-
3A1 E9 E10 E11 7400 7408 74175
2 PROT MODE 2A4
3 PROT MODE- D4 8C2
SET WRITE PROT-4
3A1 WRITE PROT-5
D3 CLR WRITE PROT-
3A1 E9 E10 E11 7400 7408 74175
7 WRITE PROT
6 WRITE PROT- D4
3A3 MODE 0 E5 7408
3 MEMI8 8C4
3A1 SET KB DIS-13
C3 KB DISABLE-12
3A1 CLR KB DIS-
A2 ST2-
ID2 CLEAR-
E9 E10 E11 7400 7408 74175
KB DISABLE IC3
14 KB DISABLE- IC2, C4
MODE LATCH
+5
R29 20K
C4 100µf
CR2 IN914
HIGH
3C2 SET BEEP-
A12 74123
CHC4
5C2
B13 7437
C3 100µf
J1 P1
SPEAKER
BEEPER
3B1 COND
2D1 OPNI
2D2 PLA 01
PLA 02
PLA 03
PLA 04
2C1 LD LIT ADR-
B2 ST1-
ENIN 1
ENIN 2
ENOUT1
ENOUT2
CLR
74173
3B2 EN LIT OUT-
82S123 32X8 ROM
BUS 1 IB2
BUS 2 IB2
BUS 3 IB2
BUS 4 IB2
BUS 5 IB2
BUS 6 IC2
BUS 7 IC2
LITERAL CIRCUIT LATCH AND DECODER
+5
4.7K R11
7D3 SCREEN REFRESH
1B1 KB OUT EN
5B3 CPC CARRY
5C3 DPC8
D14 7427
NO STROBE-
H10 7410
D13 7404
STI- B4, ,3B4,6B3, 6D2, 12C4
STI 3C4,6B2, 3A3
ST2- C4, 2C2, 2C4, 12B2, 13C4, 2B2
3B2
STATE LOGIC
MODE LATCH, LITERAL CIRCUIT, BEEPER, AND STATE LOGIC
SIZE C
SCROC IQ 120
DRAWING NO. 10006.7
SCALE
100067-10
SHEET 4
DWG NO.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
MASTER CLOCK
10.9200
R8 1K
R9 1K
100pf C20
E15 74H00
8A4, 9C2
HIGH 2
5C1 CHC 8 - 14
5C3 HBLANK 12
CHC PRESET - 13
E12
10 CHC VIDEO TIME
9C4, 9C4, 1A2
9 CHC VIDEO TIME -
7D4
C3 DPC 8
9D3 CG06 11
5C2 CHC 8 10
F13 74LS10
8 2513 CLR -
15 74109
10A4, 10B4
+5
R34 4.7K
+5V
R40 4.7K
50\60 HZ JUMPER
F15 74163
14 DPC1
13 DPC2
12 DPC4
11 DPC8 -
11B4
8A4, 11D4
9C2, 9C4, 9A2, 9D4 12D3
DOT POSITION COUNTER
5C2 CHC 8 5
5C1 CHC 4 - 3
5D2 CHC 1 4
H10 7410
6 CHC PRESET -
H11 74163
14 CHC1
13 CHC2
12 CHC4
5C3, 9D3, 9B3 CHARACTER HEIGHT COUNTER
9D3, 9B3
9D3, 4C2, 9B3
F10 7404
6 CHC 4 -
5C3
CHC 8
5C3, 5D3
9D3
2 CHC 8 -
5D2, 5B2
D13 7404
10 DPC8
1D2 4A4, D3
L7 74163
14 CPC1
13 CPC2
12 CPC4
11 CPC8
1C2, 7B2, 9B3
7B2, 9A2
7B2, 9B3
7B2, 9B3, 10D4
CHARACTER POSITION COUNTER
H7 7404
F11 7474
5 HBLANK
6 HBLANK -
5D2
10B4
J5 74163
14 CLC1
13 CLC2
12 CLC4
11 CLC8
7A4, 9B2, 9B3, 5A3, 5A3
7D4, 9B4
7D4, 9A4
7D4, 9B4, 5A4
5C1 CHC 8 -
HIGH 3
K6 74163
14 CPC16
13 CPC32
12 CPC64
11 CPC80
15 CPC CARRY
7A4, 9B3, 10D4
7B4, 9A3, 11D4
1C4, 7A4, 9B3
7D4, 10C4
4A4
F10 7404
10 CPC80 -
, 10C4
K3 7410
CPC=79 -
J1 74109
10 CLC 16
5A4, 1D3, 7D4, 9B4
CHARACTER LINE COUNTER
5C2 CLC 1 13
12 L5
11 CLC=25 -
L3 7404
5B2 CLC 16 5
5C2 CLC 8 4
L5 7400
6 VBLANK -
7D4, 10B4
5C2 CLC 1
F9 7432
3 VDRIVE -
10D3
DISPLAY TIMING COUNTERS
SIZE C
SOROC IQ 120
DRAWING NO. 100067
SCALE
100067-10
SHEET 5
DWG NO.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
CURSOR POSITION REGISTER
CURSOR POSITION REGISTERS
CURSOR LINE
CUT FOR OFFSET
BUS1
BUS2
BUS3
BUS4
DECR CURP-
INCR CURP-
LOAD CURP-
CLR CURP
CURP1
CURP2
CURP4
CURP8
7B2,9B3
7B2,9B3
7B2,9A3
7B2,9B3
HIGH 3
CLR CURL EN-12
CLR CURP EN-13
STI-
CLR-
CLR CURL-
CLR CURL
CLR CURP
74175
DECR BCURP-
BCURL ILLEGAL-
LOAD BCUR-
7A4,9B3
7B4,9A3
7A4,9B3
BUS5
BUS6
BUS7
DEC CURP 2
CURP16
CURP32
CURP64
CURP ILLEGAL-
CURP ILLEGAL-5
BCURP ILLEGAL-3
CURL ILLEGAL-4
6 ILLEGAL
GO TO MC
CLR BCURL-
BCURL ILLEGAL-
LOAD CURL-
BUS1-
12 LINE EN
INCR CURL-
DECR CURL-
CLR CURL-
BUS1
LOAD CURL-
CURL 1 9B3,7A4
DECR BCURL-1
BCURL 1
12 LINE EN
STI
BCURL 1
CURL 2
CURL 4
CURL 8
CURL 16
7C4,9A4
7D4,9B4
CURL 3 ILLEGAL-
LOAD BCUR-
7D4,9B4
7D4,9B4
7400
7402
7404
7408
7410
7432
7474
7486
74193
74LS113
74193
SIZE C
SCROC IQ 120
DRAWING NO. 100067
SCALE
100067-10
SHEET 6


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | 1920 LINE OPTION | 12/5
5D2 CHC VIDEO TIME-
5B4 CPC80
D9
SCREEN REFRESH
B2,A4,C4,4B4,1A2
5A4 VBLANK-
3A2 BUS NULL-
C14
7400
7427
5C1 CLC2
6A2 CURL2
5C1 CLC8
6A2 CURL8
5B1 CLC16
6A2 CURL16
6A2 CLC4
5C1 CURL4
SCREEN REFRESH
D3
J7
74157
J8
7483
LINE 2
LINE 4
SUM 8
SUM 16
SUM 32
A3
J9
LINE 8
LINE 16
POS 64
J10
7432
MEM ADR 256
MEM ADR 512
8D4
+5
R25
4.7K
ADD JUMPER FOR 12 LINE OPTION
B5
7404
12 LINE EN
6B4,6B2
9B3
H9
7408
HIGH 2
9B2 LINE EN-
H4
7474
ROLL 1
3B3 INC ROLL-
3C3 CLR ROLL-
ROLL REGISTER
J11
7486
EN 24-
EN 12-
8A2
H8
74161
ROLL 2
ROLL 4
ROLL 8
ROLL 16
F8
7420
MAX ROLL-
5C3 CPC2
6D3 CURP2
5C4 CPC4
6D3 CURP4
5C4 CPC8
6D3 CURP8
5C4 CPC1
6D3 CURP1
L9
MEM ADR 2
MEM ADR 4
MEM ADR 8
MEM ADR 1
8C4
5B4 CPC32
6C3 CURP32
5B3 CPC64
6C3 CURP64
5C1 CLC1
5C1 CURL1
6C2 CPC16
5B4 CURP16
K8
D2
POS 32
POS 16
POS 64
D1 LINE 16
D2 LINE 4
D2 LINE 2
D1 LINE 8
K9
MEM ADR 128
MEM ADR 32
MEM ADR 16
MEM ADR 64
8D4
ROLL REGISTER 12/24 LINE ENABLE AND MEMORY ADDRESS LOGIC
SIZE C
SOROC IQ 120
DRAWING NO. 100C67
SCALE
100C67-1C SHEET 1
DWG NO.

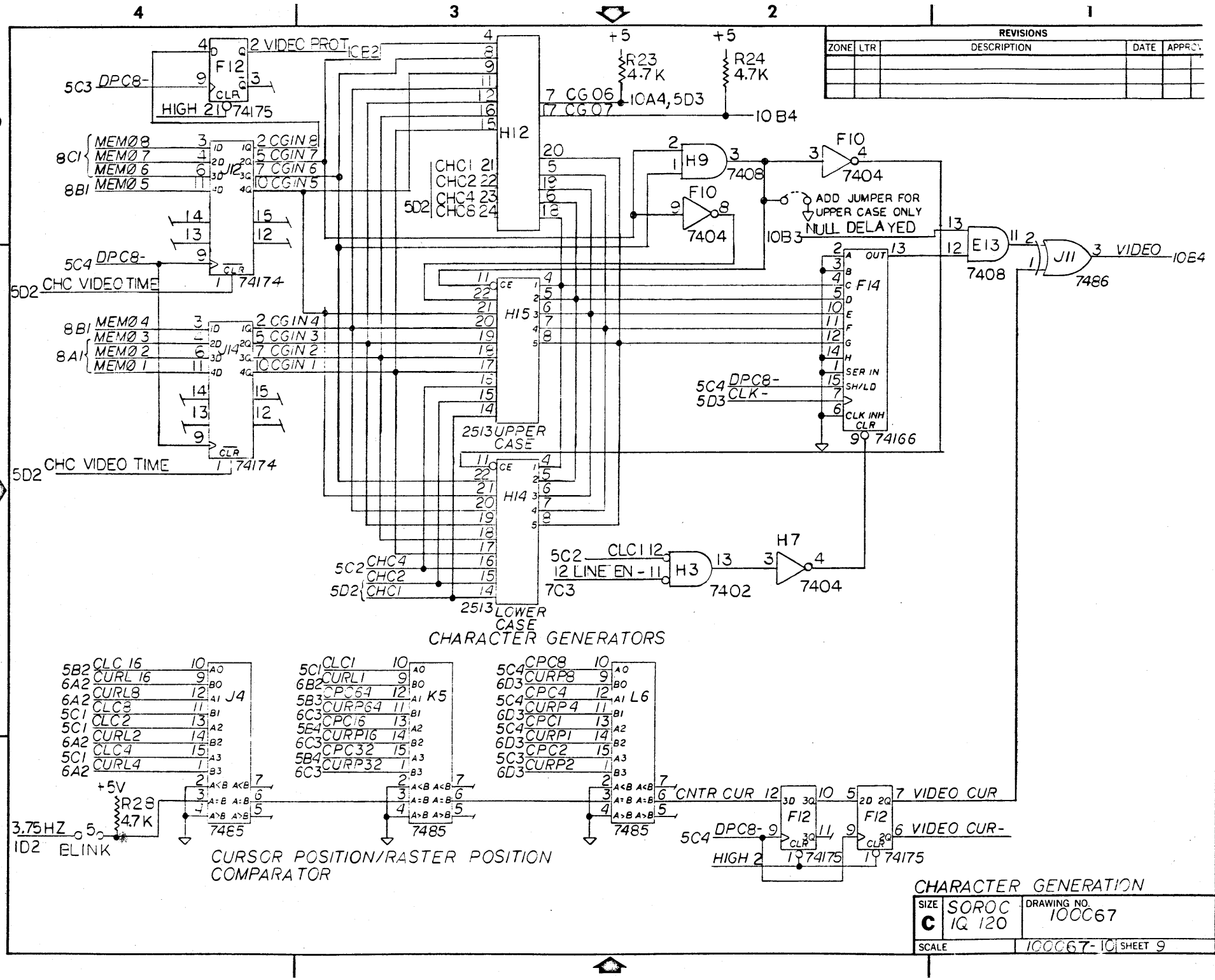
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



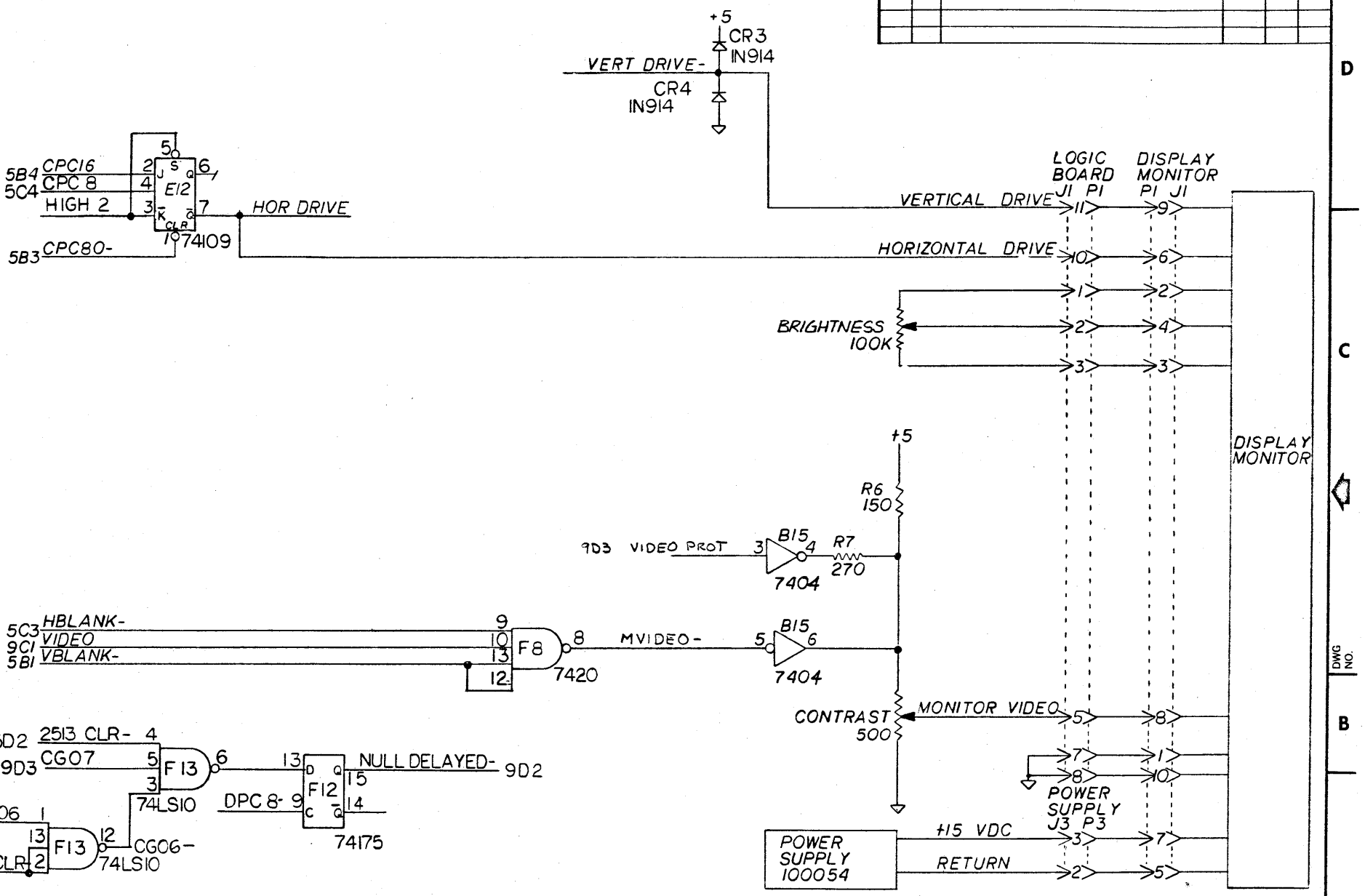
NOTE: RAMS ARE INSTALLED IN LIO THROUGH LI7 FOR 24 LINE OPTION
ALL ADDRESS LINES ARE COMMON
BUS LINES ARE COMMON BETWEEN ROWS

DISPLAY REFRESH MEMORY

SIZE		DRAWING NO.
C	SOROC IQ 120	100C57
SCALE		100C57-10 SHEET 8


REVISIONS
ZONE LTR DESCRIPTION DATE APPRO
2 VIDEO PROT
5C3 DPC8-
F12
HIGH 21 74175
ICE2
H12
+5
R23 4.7K
R24 4.7K
7 CG 06
17 CG 07
10A4, 5D3
10 B4
8CI MEM08 MEM07 MEM06
8BI MEM05
J12
CGIN 8 CGIN 7 CGIN 6 CGIN 5
CHC1 21
CHC2 22
CHC4 23
CHC8 24
5D2
H9
7408
F10
7404
ADD JUMPER FOR UPPER CASE ONLY
NULL DELAYED
10B3
E13
7408
J11
7486
3 VIDEO
10E4
5C4 DPC8-
5D2 CHC VIDEO TIME
74174
8BI MEM04 MEM03
8AI MEM02 MEM01
J14
CGIN 4 CGIN 3 CGIN 2 CGIN 1
H15
2513 UPPER CASE
H14
2513 LOWER CASE
F14
SER IN
SH/LD
CLK INH
CLR
5C4 DPC8-
5D3 CLK-
74166
5C2 CHC4
CHC2
5D2 CHC1
CLC1 12
12 LINE EN - 11
7C3
H3
7402
H7
7404
CHARACTER GENERATORS
5B2 CLC 16
CURL 16
6A2 CURL8
CLC8
5C1 CLC2
CURL2
CLC4
CURL4
J4
5C1 CLC1
6B2 CPC64
5B3 CURP64
6C3 CPC16
5B4 CURP16
CPC32
CURP32
K5
5C4 CPC8
6D3 CURP8
CPC4
5C4 CURP4
6D3 CPC1
5C4 CURP1
CPC2
5C3 CURP2
L6
7485
+5V
R28 4.7K
3.75HZ BLINK
1D2
CURSOR POSITION/RASTER POSITION COMPARATOR
CNTR CUR 12
F12
7 VIDEO CUR
6 VIDEO CUR-
5C4 DPC8-
HIGH 2
74175
CHARACTER GENERATION
SIZE C
SOROC IQ 120
DRAWING NO. 10CC67
SCALE
10CC67-10 SHEET 9

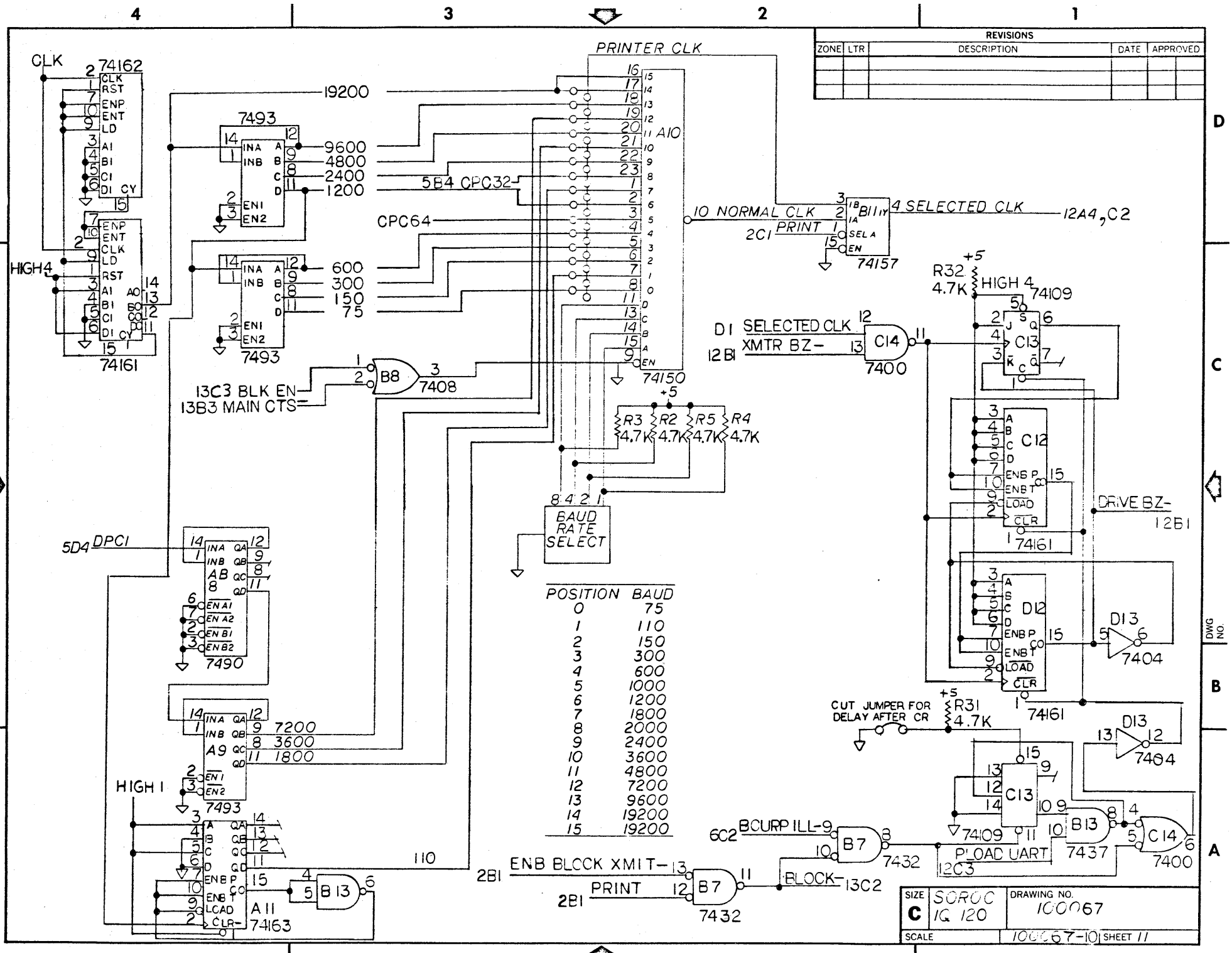
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

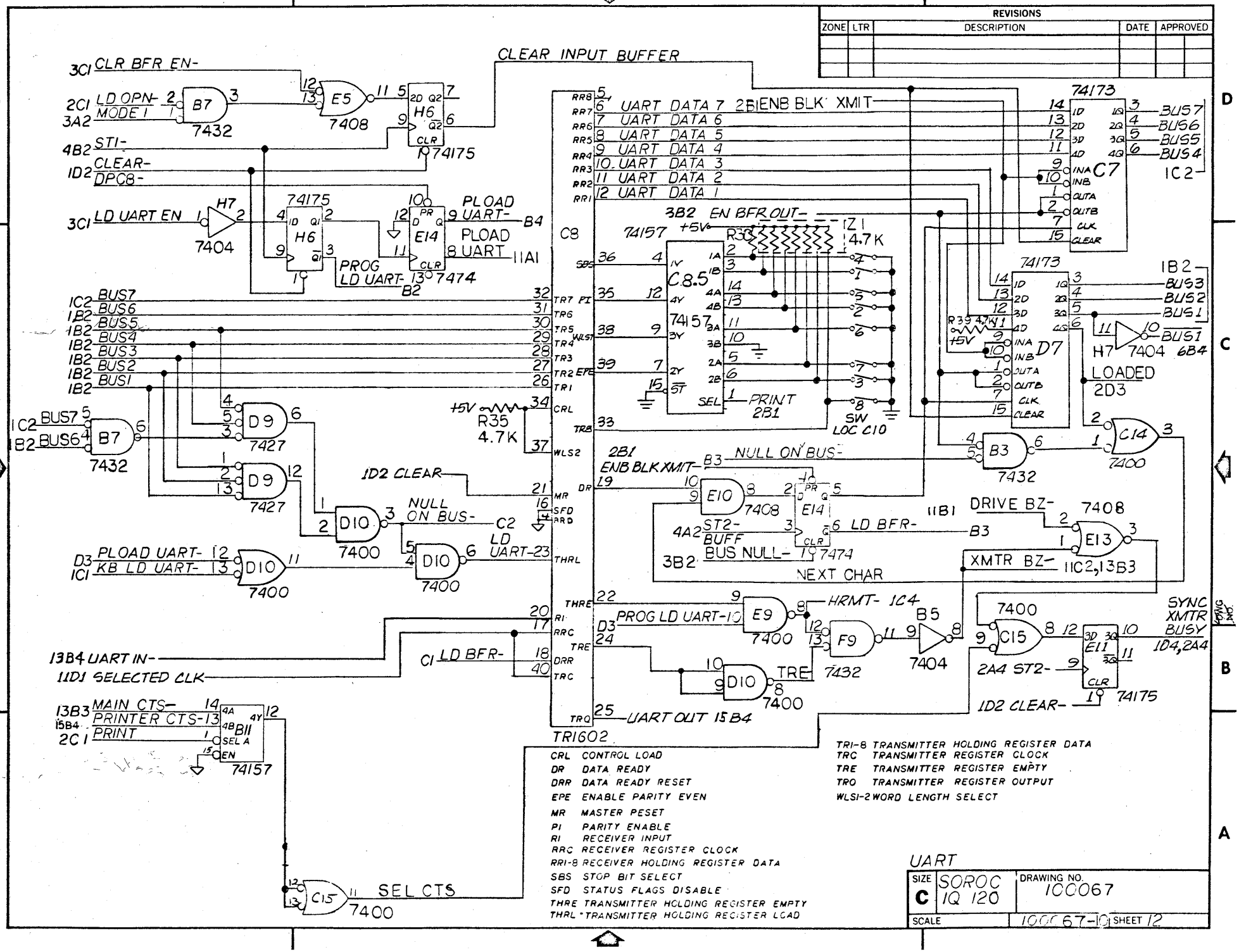


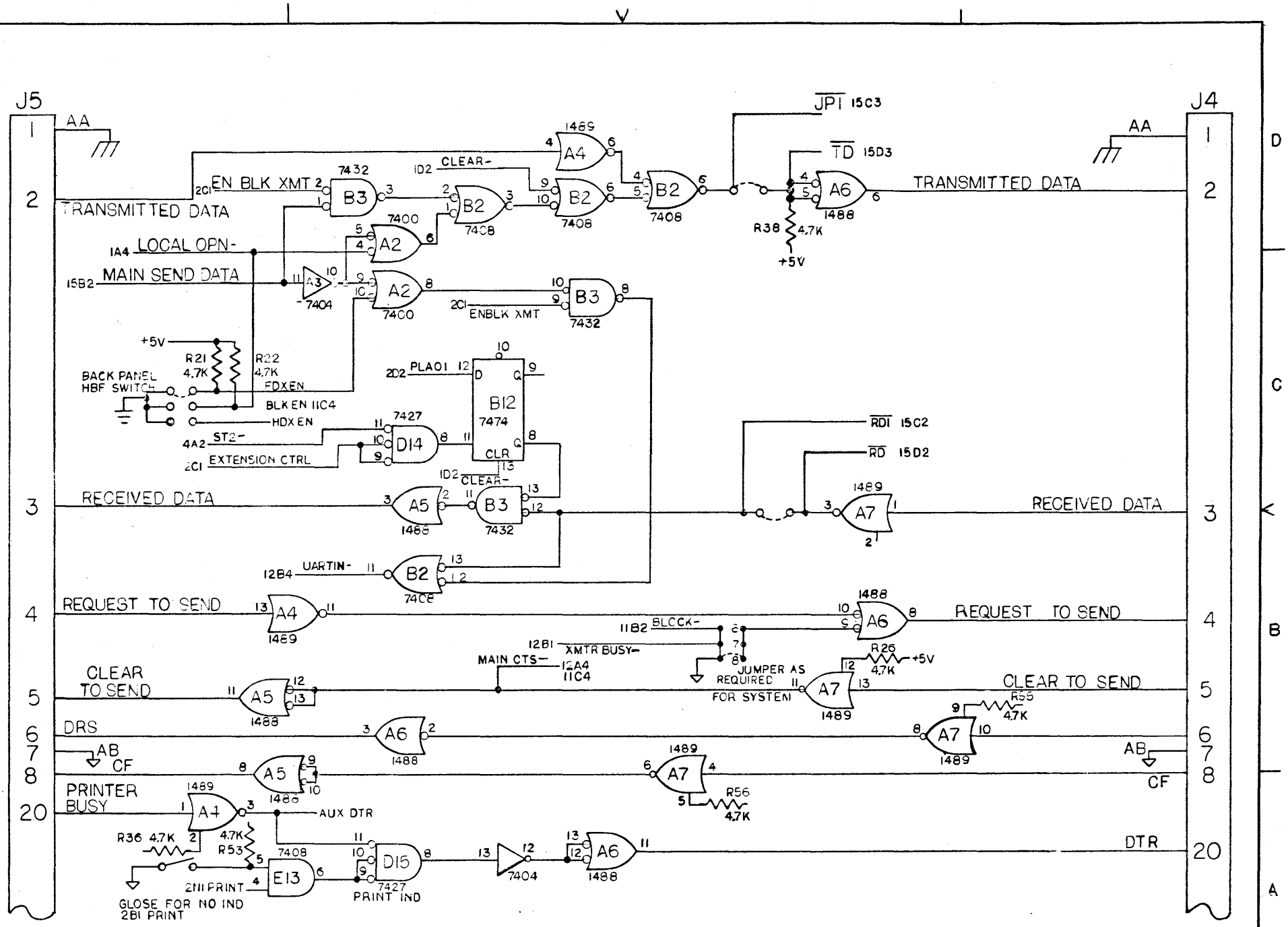
DISPLAY MONITOR INTERFACE

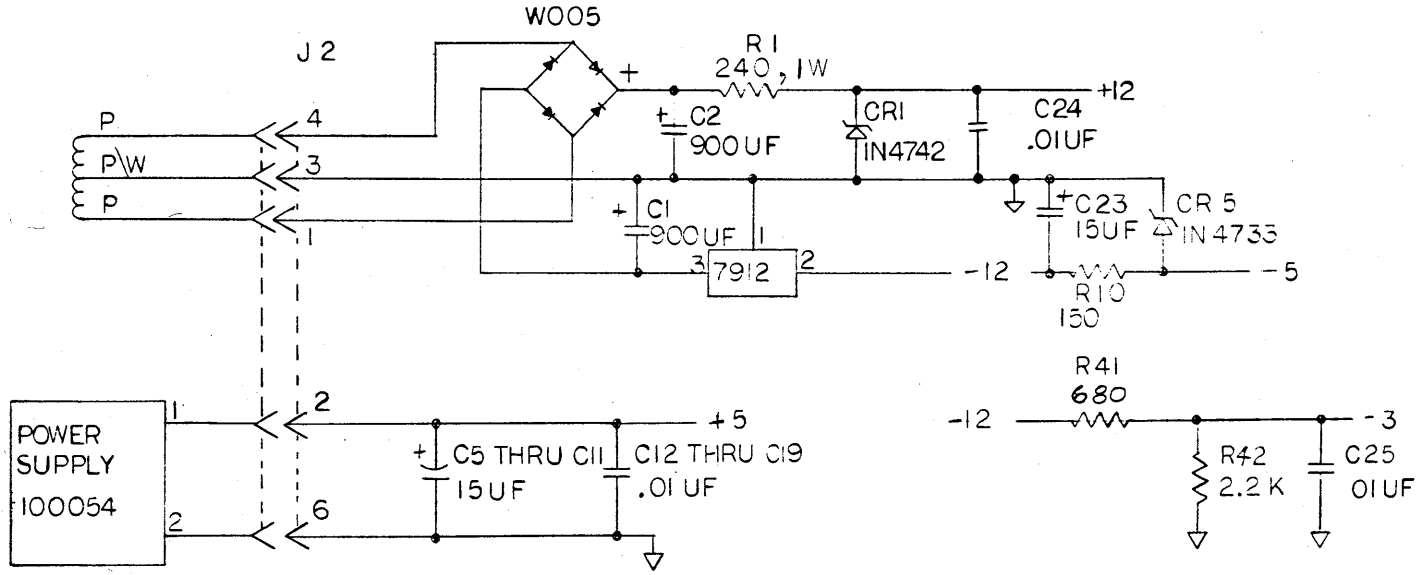
SIZE		DRAWING NO.
C	SCROC IQ 120	100067
SCALE	100067-10	SHEET 10

DWG NO.

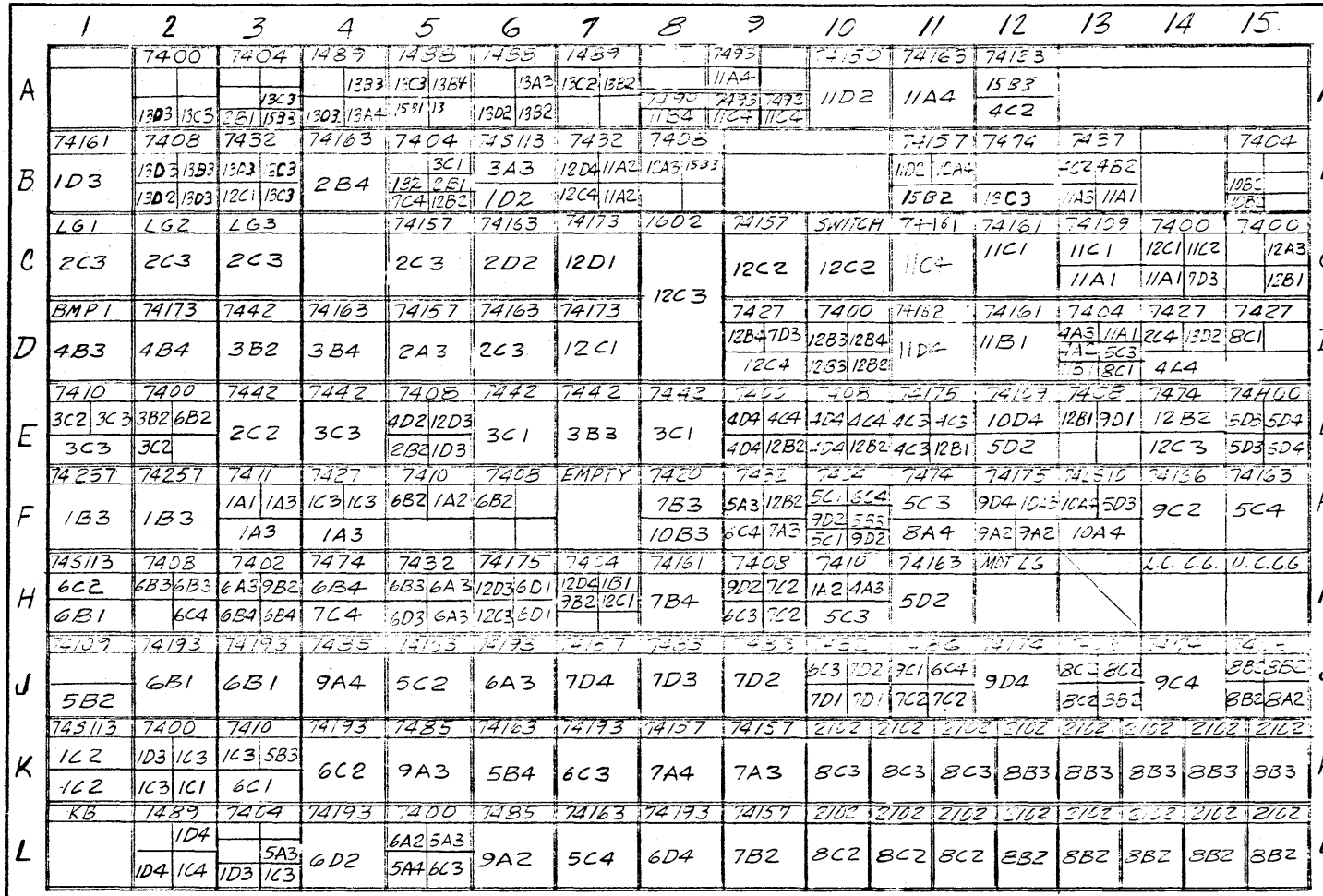

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
PRINTER CLK
CLK
74162
19200
7493
9600
4800
2400
1200
5B4 CPC32
CPC64
600
300
150
75
74161
HIGH 4
13C3 BLK EN
13B3 MAIN CTS
B8
7408
74150
A10
10 NORMAL CLK
2C1 PRINT 1
B11
4 SELECTED CLK
12A4, C2
74157
+5
R32
4.7K
HIGH 4
74109
D1 SELECTED CLK
12B1 XMTR BZ-
C14
7400
C13
C12
DRIVE BZ-
12B1
D12
D13
7404
74161
CUT JUMPER FOR DELAY AFTER CR
R31
4.7K
R3 R2 R5 R4
4.7K 4.7K 4.7K 4.7K
8 4 2 1
BAUD RATE SELECT
POSITION BAUD
0 75
1 110
2 150
3 300
4 600
5 1000
6 1200
7 1800
8 2000
9 2400
10 3600
11 4800
12 7200
13 9600
14 19200
15 19200
5D4 DPC1
7490
7200
3600
1800
A9
7493
HIGH 1
A11
74163
110
2B1 ENB BLOCK XMIT-
2B1 PRINT
B7
7432
6C2 BCURR ILL-9
BLOCK-
13C2
P LOAD UART
12C3
B13
7437
C14
7400
SIZE C
SOROC IQ 120
DRAWING NO. 100067
SCALE
100067-10
SHEET 11


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
CLEAR INPUT BUFFER
TRI602
UART
SOROC IQ 120
DRAWING NO. 100067
SIZE C
SCALE
100067-10 SHEET 12
CRL CONTROL LOAD
DR DATA READY
DRR DATA READY RESET
EPE ENABLE PARITY EVEN
MR MASTER PESET
PI PARITY ENABLE
RI RECEIVER INPUT
RRC RECEIVER REGISTER CLOCK
RRI-8 RECEIVER HOLDING REGISTER DATA
SBS STOP BIT SELECT
SFD STATUS FLAGS DISABLE
THRE TRANSMITTER HOLDING REGISTER EMPTY
THRL TRANSMITTER HOLDING REGISTER LOAD
TRI-8 TRANSMITTER HOLDING REGISTER DATA
TRC TRANSMITTER REGISTER CLOCK
TRE TRANSMITTER REGISTER EMPTY
TRO TRANSMITTER REGISTER OUTPUT
WLSI-2 WORD LENGTH SELECT


J5
J4
AA
TRANSMITTED DATA
EN BLK XMT
LOCAL OPN-
MAIN SEND DATA
ENBLK XMT
JPT 15C3
TD 15D3
TRANSMITTED DATA
R38 4.7K
+5V
RDI 15C2
RD 15D2
RECEIVED DATA
BACK PANEL HBF SWITCH
R21 4.7K
R22 4.7K
FDXEN
BLK EN 11C4
HDX EN
ST2-
EXTENSION CTRL
PLA01
CLEAR-
UARTIN-
REQUEST TO SEND
BLOCK-
XMTR BUSY-
MAIN CTS-
JUMPER AS REQUIRED FOR SYSTEM
R26 4.7K
CLEAR TO SEND
R55 4.7K
DRS
AB CF
R56 4.7K
PRINTER BUSY
AUX DTR
R36 4.7K
R53 4.7K
CLOSE FOR NO IND 2BI PRINT
2NI PRINT
PRINT IND
DTR
INPUT OUTPUT INTERFACE
SCALE
SIZE C
DRAWING NO. 100067-10
DO NOT SCALE DRAWING
SHEET 13



SCALE	SIZE	DRAWING NO
	C	100067-10
DO NOT SCALE DRAWING		SHEET 1

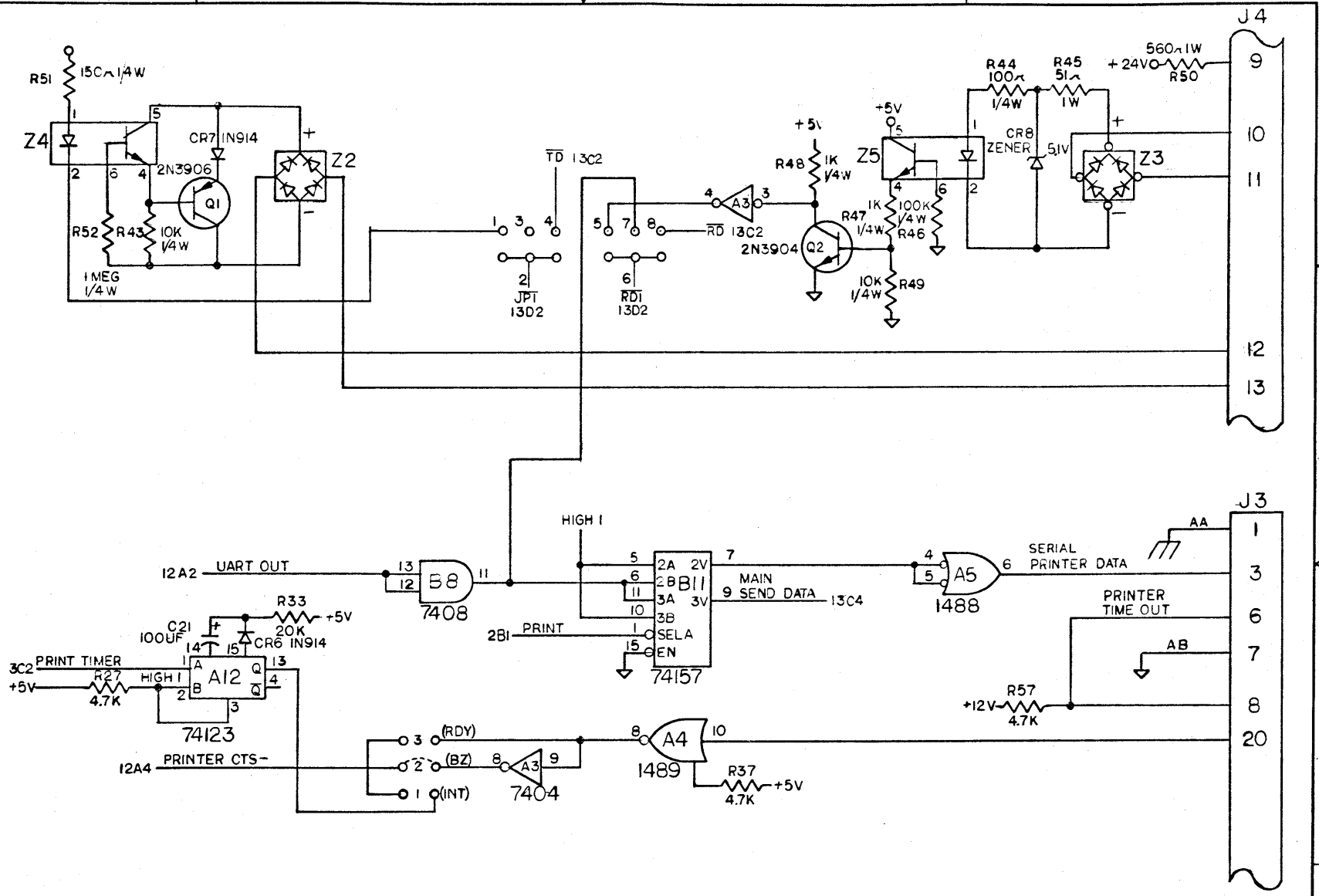


DES	VALUE	LOC
R1	240Ω 1W	4C2
R2	4.7K	11C2
R3	4.7K	11C2
R4	4.7K	11C2
R5	4.7K	4C2
R6	150Ω	10C2
R7	270Ω	10B2
R8	1K	5D2
R9	1K	5D4
R10	150Ω VSW	14C2
R11	4.7K	4A3
R12	4.7K	1D3
R13	4.7K	2D3
R14	4.7K	2D3
R15	4.7K	2D3
R16	4.7K	2D3
R17	4.7K	2D3
R18	4.7K	2D3
R19	4.7K	2D3
R20	4.7K	2D3
R21	4.7K	3C4
R22	4.7K	13C4
R23	4.7K	9C2
R24	4.7K	9C2
R25	4.7K	7C4
R26	4.7K	13E2
R27	4.7K	15B4
R28	4.7K	9A4
R29	20K	4C2
R30	4.7K	2C2
R31	4.7K	11B1
R32	4.7K	11C1
R33	20K	16B3
R34	4.7K	5D4
R35	4.7K	12C3
R36	4.7K	3A4
R37	4.7K	16B2
R38	4.7K	12D2
R39	4.7K	12C1
R40	4.7K	5C2
R41	680	14B1
R42	2.2K	14B1
R43	10.K	15D4
R44	100Ω	15D1
R45	51Ω	15D1
R46	100K	15D2
R47	1K	15D2
R48	1K	15D2
R49	10K	15C2
R50	560Ω	15D1
R51	150Ω	15D4
R52	1 MEG	15D4
R53	4.7K	13A4
R54	4.7K	2A3
R55	4.7K	13B1
R56	4.7K	13A2
R57	4.7K	5B1

DES	VALUE	LOC
C1	900 UF	4C2
C2	900 UF	14C2
C3	100 UF	4C2
C4	100 UF	4C2
C5	15 UF	14B3
C6	15 UF	14B3
C7	15 UF	14B3
C8	15 UF	14B3
C9	15 UF	14B3
C10	15 UF	14B3
C11	15 UF	14B3
C12	.01 UF	14B2
C13	.01 UF	14B2
C14	.01 UF	14B2
C15	.01 UF	14B2
C16	.01 UF	14B2
C17	.01 UF	14B2
C18	.01 UF	14B2
C19	.01 UF	14B2
C20	100 PF	5C4
C21	100 UF	16B4
C22	15 UF	1D3
C23	15 UF	14C2
C24	.01	14C2
C25	.01	14B2

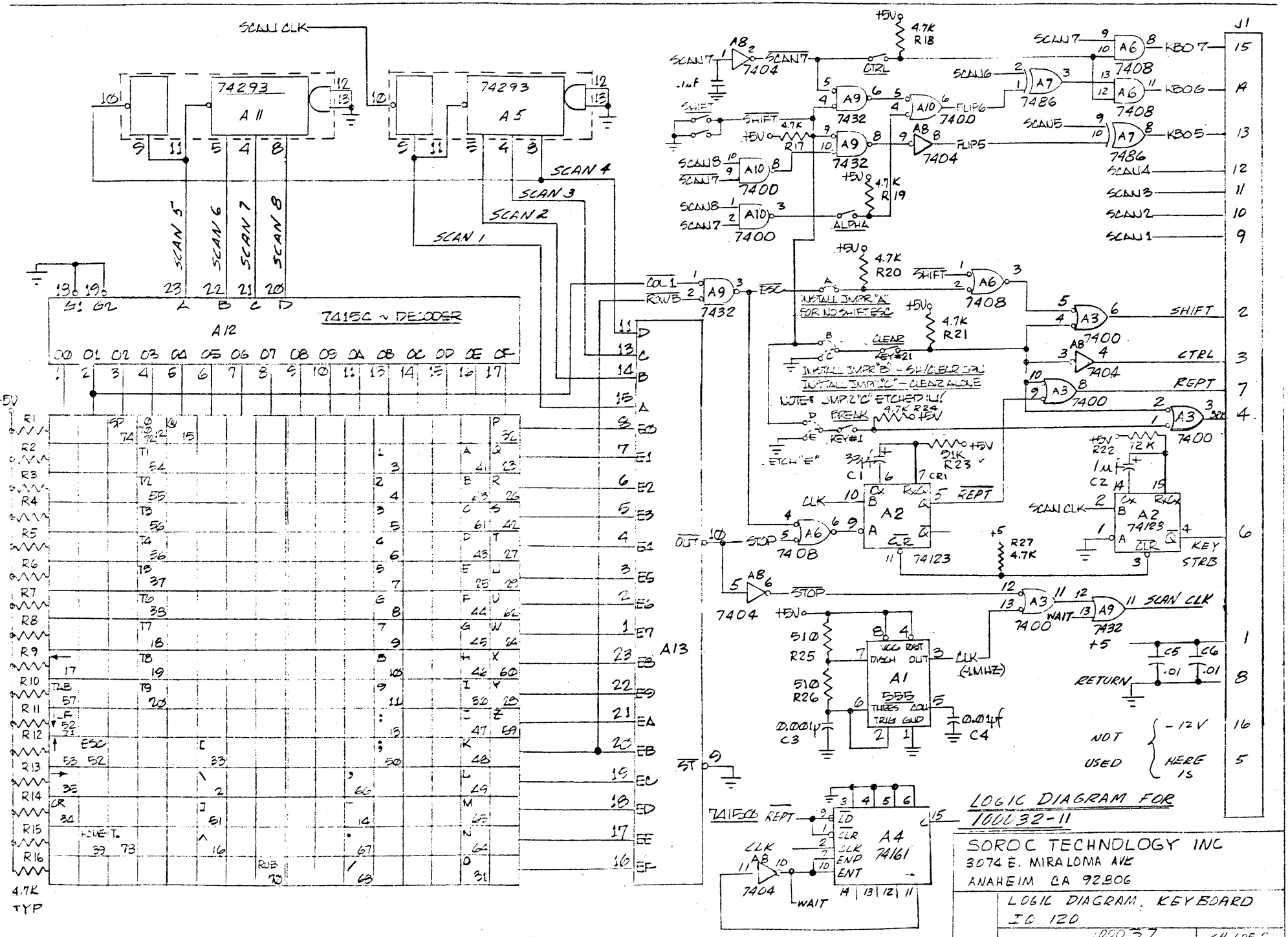
DES	VALUE	LOC
CR1	IN4733	14C2
CR2	IN914	4C2
CR3	IN914	10D2
CR4	IN914	12D2
CR5	IN4733	14C2
CR6	IN914	15B3
CR7	IN914	15D3
CR8	5.1V	15D1

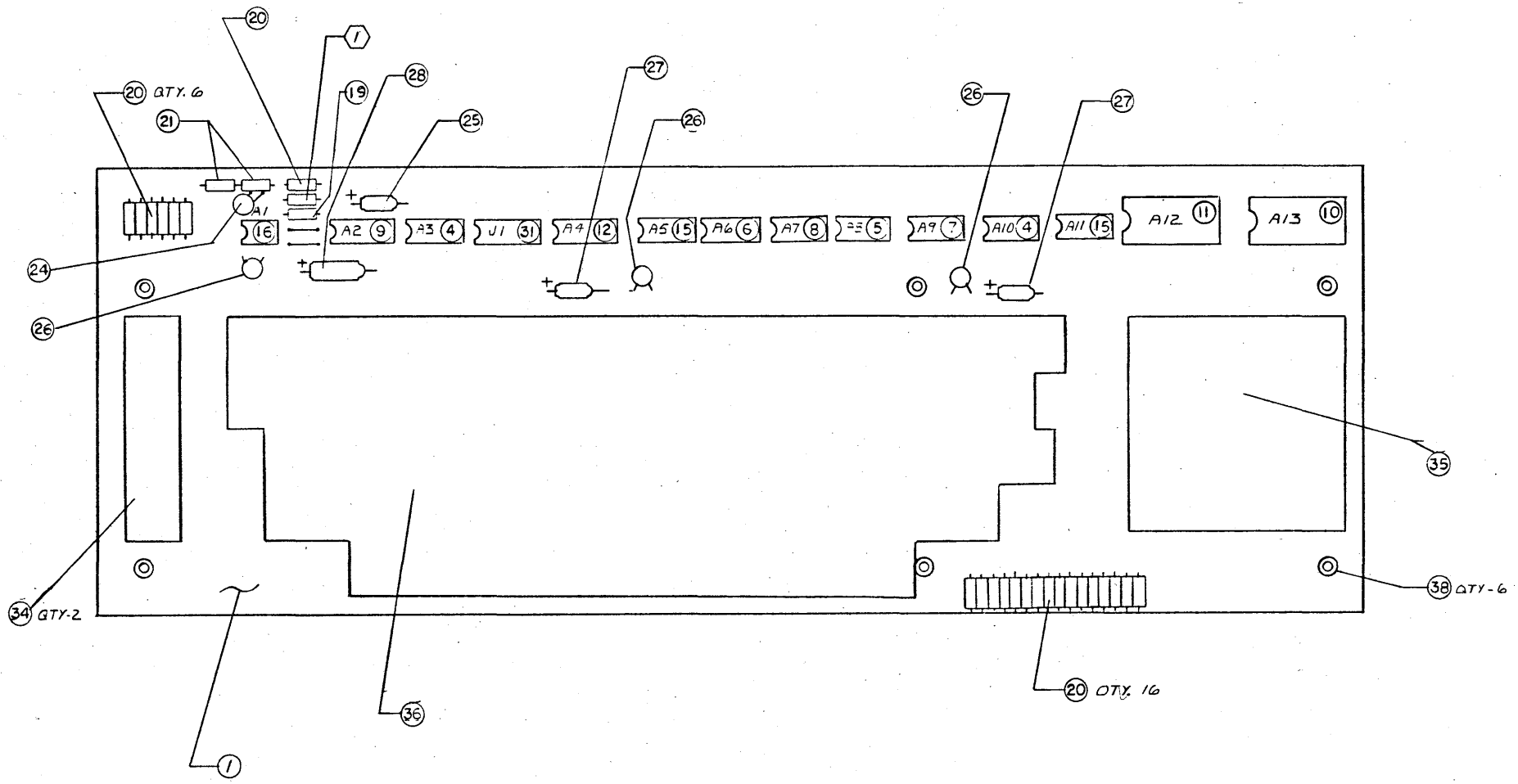
SCALE	SIZE	DRAWING NO.
	C	100067-10
DO NOT SCALE DRAWING		SHEET 16

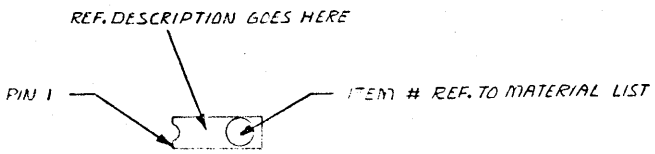


CURRENT LOOP
BLOCK MODE OPTIONS

SCALE	SIZE	DRAWING NO.
	C	100067-10
DO NOT SCALE DRAWING		SHEET 15


SCAN CLK
74293
A 11
74293
A 5
SCAN 4
SCAN 3
SCAN 2
SCAN 1
SCAN 5
SCAN 6
SCAN 7
SCAN 8
74154 ~ DECODER
A12
A13
4.7K TYP
+5V
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
ESC
RUB
HOME
CR
LF
TAB
J1
KBD 7
KBD 6
KBD 5
SCAN 7
SCAN 6
SCAN 5
SCAN 4
SCAN 3
SCAN 2
SCAN 1
SHIFT
CTRL
RPT
KEY STRB
SCAN CLK
WAIT
FLIP 6
FLIP 5
ALPHA
CLEAR
BREAK
ETCH "E"
INSTALL JMPR "A" FOR NO SHIFT ESC
INSTALL JMPR "B" - SH/CLR/BRK
INSTALL JMPR "C" - CLEAR ALONE
NOTE: JMPR "C" ETCHED IN
STOP
REPT
CLK (1MHZ)
RETURN
NOT USED
- 12 V
HERE IS
LOGIC DIAGRAM FOR
1000232-11
SOROC TECHNOLOGY INC
3074 E. MIRALOMA AVE
ANAHEIM CA 92806
LOGIC DIAGRAM, KEYBOARD
IO 120
1000357
SH 1 OF 2





HOW TO READ I.C.'S

NOTES: (1) SEE ECO A0019 AND A0021.

2. REFER TO MATERIAL LIST (ML) FOR PART DESCRIPTION.

IQ 120 STANDARD KEYBOARD ASSY DRWG.

SCALE	SIZE	DRAWING NO.
1 TO 1	C	200002-11
DO NOT SCALE DRAWING		SHEET 1 OF 1

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	490001				

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES

APPROVALS	DATE
P. Stetson DRAWN	10/1/79
J Headley CHECKED	9/10/79
D. Mecka	10-1-79

SOROC TECHNOLOGY, INC.

165 FREEDOM AVE. ANAHEIM CALIFORNIA

IQ120 STANDARD KEY BOARD ASSY

SCALE	SIZE	DRAWING NO.
	A	ML200002-11

DO NOT SCALE DRAWING | SHEET 1 OF 3

DATE: _____
DRAWN: _____
CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____
QUANTITY _____

REV

TITLE: IO120 STANDARD KEYBOARD

ML 200002-11

SHT 2 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
1	100032-11	P.C. BOARD 100032-11		1							
2											
3											
4	600000	I.C. 7400		2				A3,A10			
5	600004	7404		1				A8			
6	600008	7408		1				A6			
7	600032	7432		1				A9			
8	600086	7486		1				A7			
9	600123	74123		1				A2			
10	600150	74150		1				A13			
11	600154	74154		1				A12			
12	600161	74161		1				A4			
13											
14											
15	601293	I.C. 74LS293		2				A5,A11			
16	604004	I.C. 555		1				A1			
17											
18											
19	705123	RESISTOR 12k ¼W. 5%		1							
20	705472	" 4.7k " "		23							
21	705511	" 510Ω " "		2							
22											
23											
24	800002	CAPACITOR .001uF		1							
25	800004	" .1uF		1							
26	800006	" .01uF		3							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: IQ 120STANDARD KEYBOARD

ML 200002-11

SHT3 OF3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
27	800203	CAPACITOR 15uF		1							
28	800205	" 33uF		12							
29	800210	" 1MFD		1							
30											
31	900000	I.C. SOCKET 16 PIN		1				J1			
32											
33											
34	907700	1X4 MODULE		1							
35	907701	4 X 4 MODULE		1							
36	907702	55 KEY ARRAY		1							
37	909100	HEXHEAD 4-40 X ¼"		8							
38	909420	STAND-OFFS 9533-BB0632-3A		6							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
490001	490001				

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES	SOROC TECHNOLOGY, INC. 165 FREEDOM AVE. ANAHEIM CALIFORNIA
APPROVALS / DATE	
DRAWN: J. Stetson 10/1/79	FAB Assy - IQ 120
CHECKED: J. Headen 10/1/79	SCALE 1/1 · SIZE A · DRAWING NO. ML 200015
D. Mabe 10-1-79	DO NOT SCALE DRAWING · SHEET 1 of 5

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: FAB Assy- IQ120

ML 200015

SHT 2 OF 5

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
1	100034	Logo, Soroc		1							
2	100036	ID Strip/Pwr. Snp.		1							
3											
4	100113	Dual Transformer		1							
5											
6											
7											
8											
9	300051-1	IQ120 Chassis		1							
10	300051-2	IQ120 PCB Mount. Plate		1							
11	300051-3	IQ120 Keybd. Mount. Plate		1							
12	300051-4	IQ120 Fan Bracket		1							
13											
14											
15											
16	900103	Contacts 583259-2 AMP		10							
17	900104	Pin Crimp 350417-1 AMP		13							
18	900105	Male Terminal 350418-1 AMP		2							
19	900107	Contact 35037-3 AMP		8							
20	900206	10 Pin Edge Conn.583229-1		1							
21	900208	Cable Mtg. Conn. Blk360025-1		2							
22	900209	187 Faston 42799-2 AMP		10							
23	900212	250 faston 2-350803-2 AMP		4							
24	900213	110 FASTON 2-520080-2 AMP		2							
25	900400	6 PIN Housing 1-480704-0		1							
26	900401	3 PIN HOUSING 1-480700-0		1							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: FAB ASSY IO120

ML 200015

SHT 3 OF 5

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
27	900500	6PIN PLUG 03-09-1063 MOLEX		1							
28	900501	12PIN PLUG 03-09-1122 MOLEX		1							
29	900502	CONTACT KEY PLUG 583462-1		1							
30											
31											
32											
33	905603	ON/OFF TA201-TWB CARLING		1							
34											
35											
36											
37	907000	133LY2182 FAN, ETRI		1							
38	907001	760-960-43 FAN GUARD ETRI		1							
39	907100	SPEAKER 50K02 - BEC		1							
40	907310	PANEL MOUNT FUSE HOLDER		1							
41	907326	1AMP SLOW BLOW FUSE		1							
42	907600	C2103-076-6YPOWER CORD ELECTRIC		1							
43	907601	KC-D16AP-TT-12A KEBD. CABLE/KONEX		1							
44											
45											
46	909101	6-32 X 3/8" HEX HEAD		28							
47	909112	6-32 X 3/4 P.H.		5							
48	909113	10-32 X 1/4" P.H.		1							
49											
50	909202	#6FLAT WASHER		10							
51	909301	AD56ABS POP RIVET		4							
52	909303	POP RIVET - ASPE52		2							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: FAB Assy - IQ120

ML 200015

SHT 4 OF 5

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
53	909400	42037-2 #10 RING LUG		1							
54											
55	909600	18 AWG Black 6"		2							
56	909601	18 AWG Black 5"		1							
57	909603	18 AWG White 6"		1							
58	909604	18 AWG Black 15"		1							
59	909605	22 AWG Black 18"		1							
60	909606	22 AWG Brown 18"		1							
61	909607	22 AWG Red 18"		1							
62	909608	22 AWG Orange 18"		1							
63	909609	22 AWG Yellow 18"		1							
64	909610	22 AWG Blue 18"		1							
65	909611	22 AWG Violet 18"		1							
66	909612	22 AWG Grey 18"		1							
67	909613	22 AWG White 18"		2							
68	909614	18 AWG WHITE 15"		1							
72	909700	939 STRAIN RELIEF		1							
73	909750	LCBS-4N STANDOFF		10							
74	909775	SJ5009 BUMPER - WHITE		4							
78	909800	TIE-WRAP - RT-408 6"		8							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

DATE: _____

DRAWN: _____

CHK: _____

MATERIAL LIST

SOROC TECHNOLOGY, INC.

JOB NO: _____

QUANTITY _____

REV

TITLE: FAB ASSY IQ 120

ML 200015

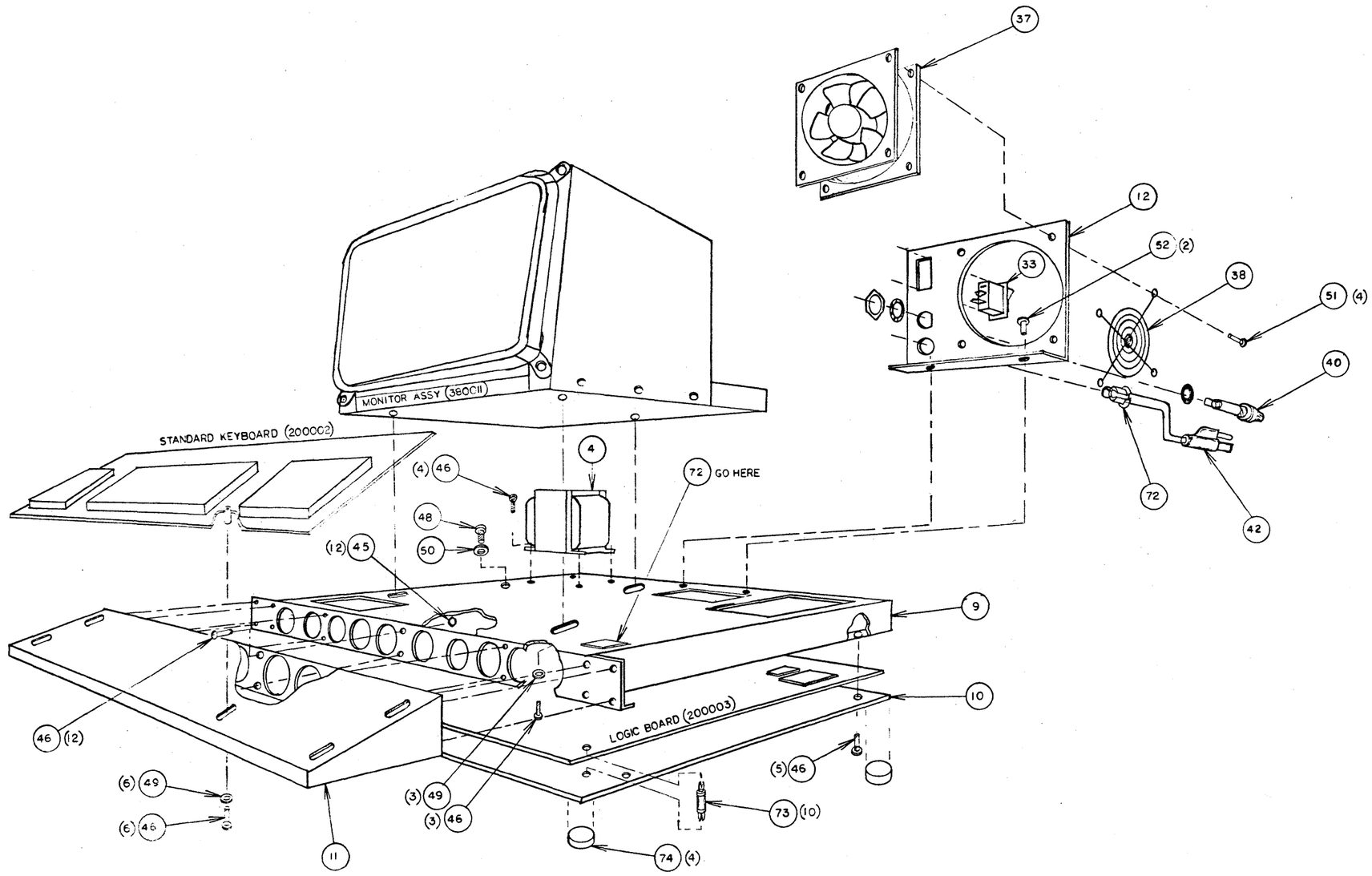
SHT 5 OF 5

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	EXT	ISS	SHT	REF. DES.	UNIT COST	LOT TOTAL	
79											
80	919004	INSUALTION .25 X 1.00 FIT-211		2							

NOTES:

DATE KIT STAGED

DATE KIT RELEASED

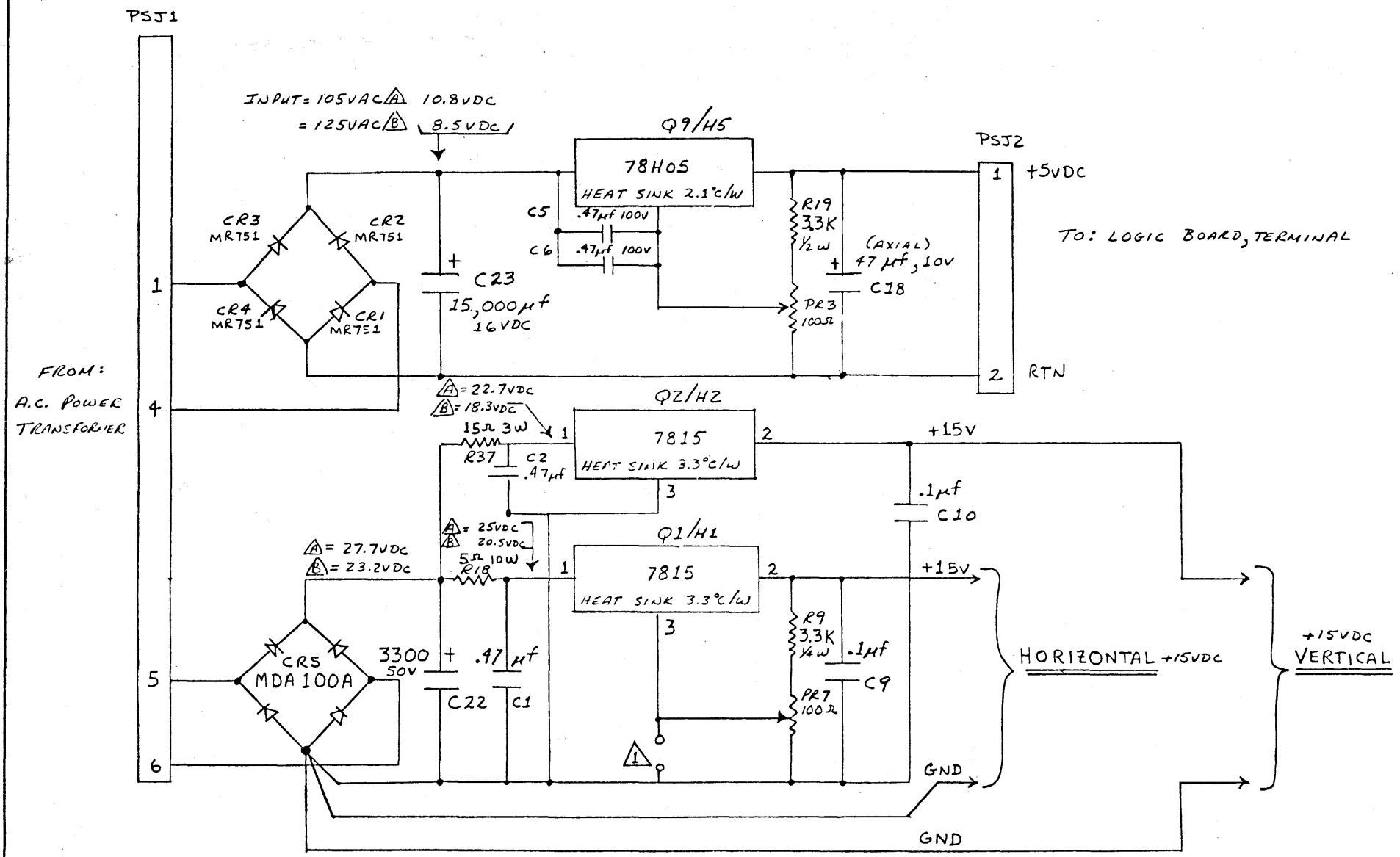


NOTES

1 ASSEMBLE COVER ASSEMBLING ITEMS 47 QTY 5 AND 50 QTY 5.

SOROC TECHNOLOGY, INC.	
SCALE:	APPROVED BY:
DATE: 12/5/79	DRAWN BY:
1Q120 FAB ASSY.	REVISED
	DRAWING NUMBER 220015

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



(1) 3.3K, 50Ω MAY BE REPLACED BY JUMPER

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS ±	DEC ±	ANGLES ±

APPROVALS	DATE
DRAWN	
CHECKED	

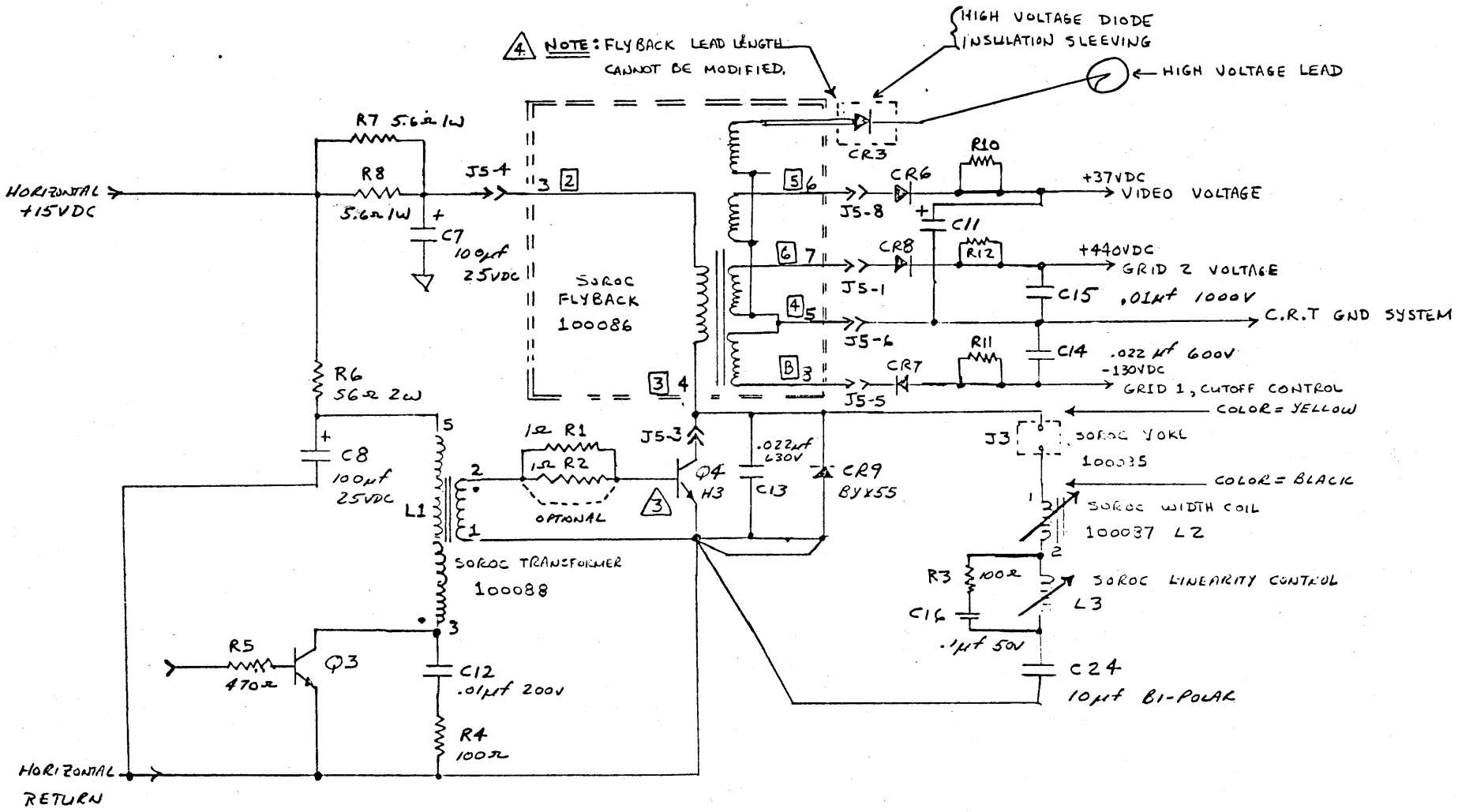
SOROC

SOROC C.R.T. POWER SUPPLY

SCALE	SIZE	DRAWING NO
	C	100090

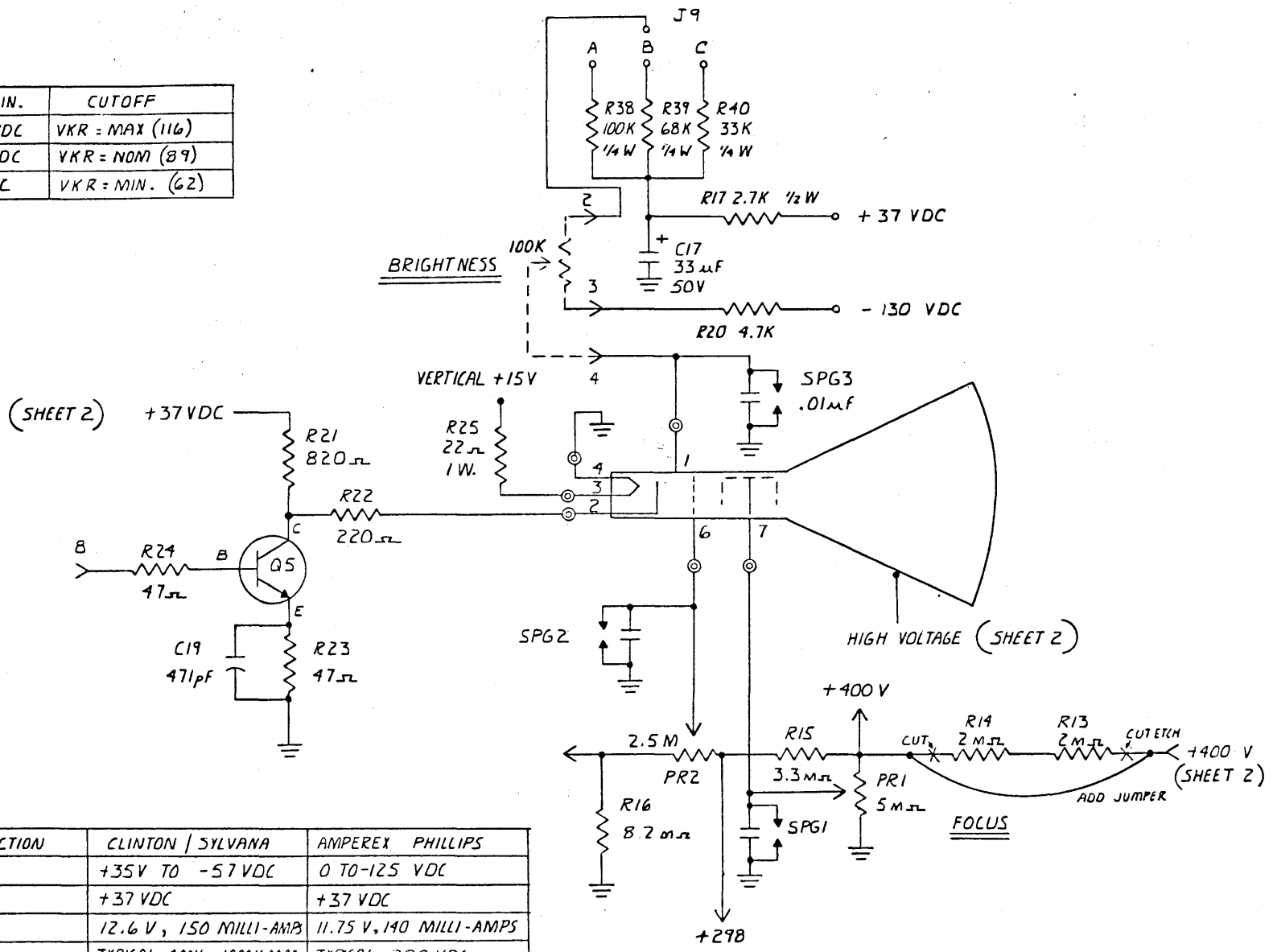
DO NOT SCALE DRAWING SHEET 1 OF 4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		SOROC
APPROVALS	DATE	SOROC C.R.T. HORIZONTAL SWEEP
DRAWN		
CHECKED		SCALE / SIZE C / DRAWING NO 100079
		DO NOT SCALE DRAWING / SHEET 2 OF 4

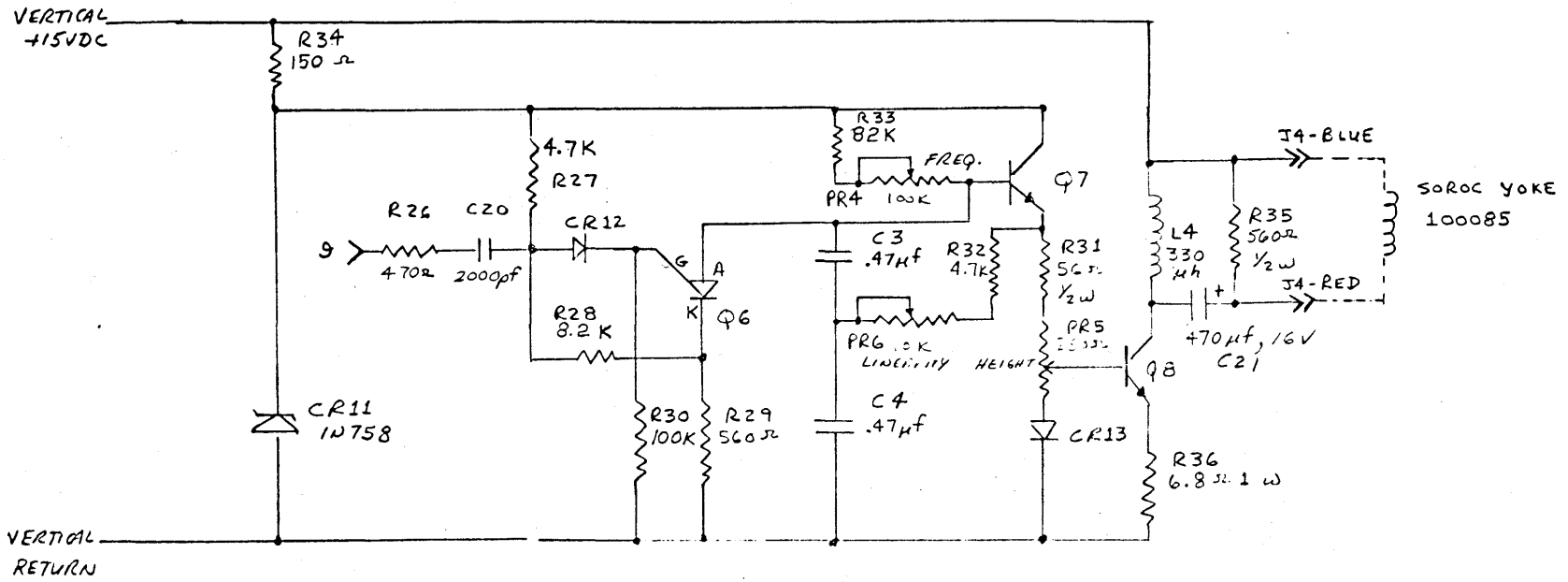
JMPR	PIN 2 MIN.	CUTOFF
A	- 45 VDC	VKR = MAX (116)
B	- 30 VDC	VKR = NOM (89)
C	0 VDC	VKR = MIN. (62)



PIN #	NAME / FUNCTION	CLINTON / SYLVANA	AMPEREX PHILLIPS
1	GRID 1	+35V TO -57 VDC	0 TO-125 VDC
2	CATHODE	+37 VDC	+37 VDC
3,4	HEATER	12.6 V, 150 MILLI-AMP	11.75 V, 140 MILLI-AMPS
6	GRID 2	TYPICAL 400V, +1000 V MAX.	TYPICAL, 280 VDC
7	GRID 4 (FOCUS)	TYPICAL 0-400 V, -500-+1100 MAX.	,-400 TO +1000 V
ANODE		TYPICAL 12KV, 16KV MAX.	TYPICAL 12KV, 11KV TO 18 KV

TITLE: SOROC C.R.T. C.R.T. CONTROL			
SCALE	SIZE C	DRAWING NO 100090	
DO NOT SCALE DRAWING		SHEET 3 OF 4	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

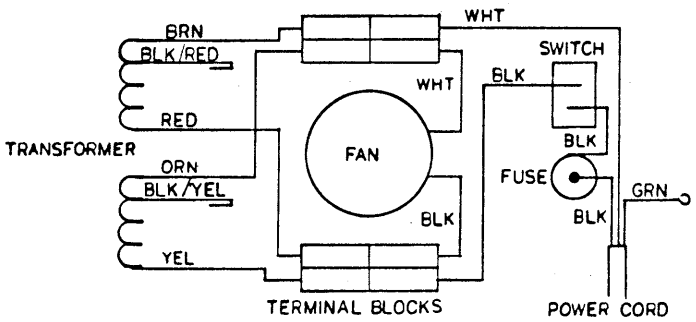
APPROVALS	DATE
DRAWN	
CHECKED	

SOROC

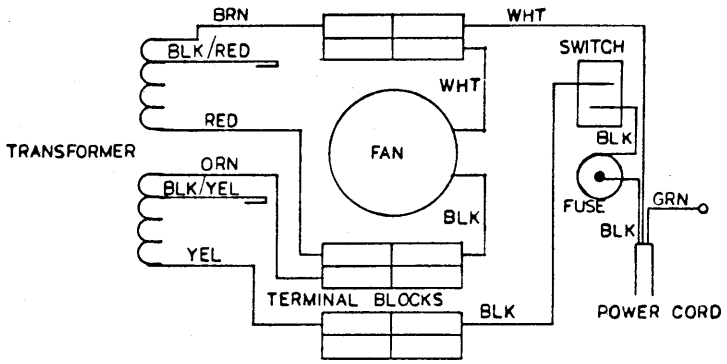
SOROC C.R.T.
VERTICAL SWEEP

SCALE	SIZE	DRAWING NO
	C	100090

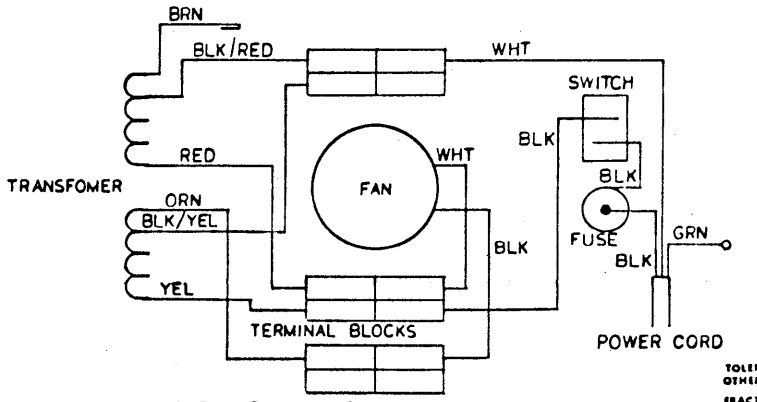
DO NOT SCALE DRAWING — SHEET 1 OF 1



115 VOLT AC WIRING



230VOLT AC WIRING



100 VOLT AC WIRING

NOTE:
FOR 100113 TRANSFOMER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		SOROC TECHNOLOGY, INC.	
APPROVALS	DATE	165 FREEDOM AVE. ANAHEIM CALIFORNIA	
DRAWN	10/8/74	100V - 115V - 230V WIRING DIAGRAM	
CHECKED	10/9/74	SCALE	SIZE C — DRAWING NO. 100096
		DO NOT SCALE DRAWING	SHEET 1 OF 2

VII

IQ 120 INSTALLATION

The following paragraphs describe the method of configurating the IQ 120 for a given installation.

Word Configuration

The communications word configuration refers to the number of bits in the word and the parity structure of the serial word transmitted and received by the main I/O port. The IQ 120 is normally shipped with the word configured for eight data bits, no parity, bit 8 always high and two stop bits: however, many other options are available to the user. Selections for both the mail port and the optional printer port are made by an eight position switch located in position C13 on the main logic board.

C13 SWITCH CONTROL

ON = Ø (Low)

OFF = 1 (high)

SWITCH POSITION	
1	PRINTER USE ONLY This switch selects the number of STOP bits in the printer word structure. ON = 1 STOP bit OFF = 2 STOP bits
2	PRINTER USE ONLY This selects PARITY ENABLED or NO PARITY ON = Parity enabled OFF = No parity
3	PRINTER USE ONLY This switch selects EVEN or ODD parity ON = Odd parity OFF = Even parity
4	MAIN PORT USE ONLY This switch selects the number of STOP bits. ON = 1 STOP bit OFF = 2 STOP bits
5	MAIN PORT USE ONLY This selects PARITY ENABLED or NO PARITY ON = Parity enabled OFF = No parity
6	MAIN PORT USE ONLY This switch selects main port word length ON = 7 bit word OFF = 8 bit word
7	MAIN PORT USE ONLY This switch selects EVEN or ODD parity ON = Odd parity OFF = Even parity
8	MAIN PORT USE UNLY This switch is for Bit Eight (8) control ON = Bit 8 always "Ø" (low) OFF = Bit 8 always "1" (high)

TABLE 7-2

BAUD RATE SELECTION

The main port must be set to the same baud rate as the computer in order to achieve error free transmission. The baud rates are selected by a rotary "thumb wheel" labeled "Baud" and located on the rear of the unit. See Rear Panel Photo. A number is displayed in the center of this switch. As the switch is rotated the number may be changed to any number from zero to fifteen. Each of the sixteen positions is associated with a given baud rate. These switch positions and their associated baud rates are listed in Table 7-5.

BAUD RATE TABLE

SWITCH POSITION	BAUD RATE
0	75
1	110
2	150
3	300
4	600
5	1000
6	1200
7	1800
8	2000
9	2400
10	3600
11	4800
12	7200
13	9600
14	19200
15	19200

TABLE 7-5

When interfacing the terminal to a computer directly rather than to a modem, the various signals (except for the two ground connections) are interchanged so that, for example, the transmitted data from the terminal (cir-uit BA) is connected to the computer received data (circuit BB) input connector. Figure 7-4 shows a typical interconnection between the terminal and a computer.

INTERFACING THE IQ 120 TERMINAL. The IQ 120 terminal uses the Electronic Industries Association (EIA) standard RS-232-C for the interconnection of the terminal to a computer. This specification defines the voltage, levels, logic states, and general signal requirements for the transmission of serial data between digital devices. The following paragraphs describe how the terminal is interfaced to another device using the RS-232-C interface.

The RS-232-C Interface. The data input/output (I/O) connector provides the following device interconnection lines:

Circuit	J4/P4 Pin	FUNCTION
AA	1	Protective ground. This ling connects the terminal chassis with the computer chassis.
AB	7	Signal ground or common return. This line establishes the common ground reference for the inter-change data and control lines.
BA	2	Transmitted data. This line is the connection between the terminal and the computer for the transfer of data from the terminal to the computer. When data is not being transferred, this line is held high (marking).
BB	3	Received data. This is the connection between the terminal and the computer for the transfer of data from the com-puter to the terminal.
CA	4	Request to send. This line is used to inform the computer that the terminal is ready to send data to the computer. When this signal is low, the terminal is in the receive mode and can receive data from the computer.
CB	5	Clear to send. This line is used to in-form the terminal that the computer is ready to receive data. When this signal is high the data is transferred from the terminal to the computer.

TABLE 7-5

Request to send Control

Request to send may be held in a spacing state or may be raised only when a transmission is to take place. This selection is made by means of a jumper configuration on the 12 pin IC pattern located directly above the baud rate switch and below IC position A11. A jumper between pins 6 and 7 on this IC pattern will hold request to send in the spacing state. A jumper between pins 5 and 8 will cause request to send to be controlled by the data transmission. See figure 7-5.

Optional Printer Port

The printer work configuration is selected by positions 1,2, and 3 of switch C13 on the logic board as described under "Word Configuration."

Printer Baud Rate Selection

The printer baud rate is determined by jumper pattern located positions A9 to A10 immediately above the 74150. To select the appropriate printer baud rate, a jumper is placed between two immediately opposite outside holes. With the board oriented so that the baud rate switch is facing you, the 75 baud position is the hole pair on the extreme right, and 19,200 is on the extreme left of the jumper pattern. See figure 7-6.

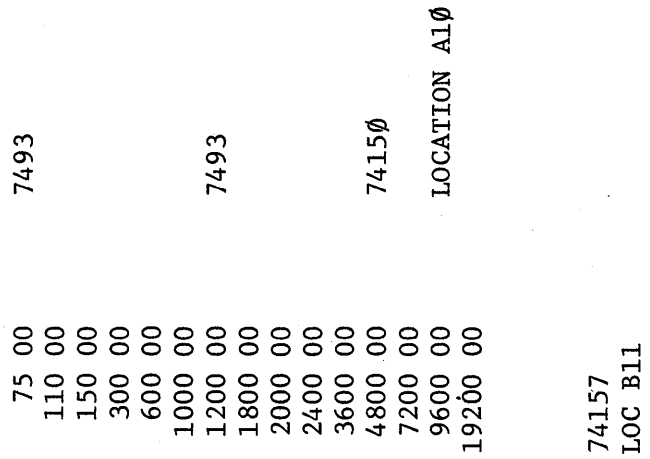


FIGURE 7-6

OTHER PRINTER CONTROLS

The printer port may be configured for external control by a printer busy or printer ready signal. If a printer busy signal is to be used, that is a spacing level on the input inhibits transmission of data out of the printer port, a jumper is installed between pins 2 and 11 of the IC pattern shown in figure 7-5. If a ready control is to be used, that is data transmission out of the printer port is inhibited when a marking level is on, the input control pin J3-20, a jumper is placed between pins 3 and 10 of the IC pattern shown in figure 7-5.

An internal time delay of two seconds is also provided to allow the printer time for the line feed and/or carriage return to take place. This time delay automatically activates any time during a print operation when the terminal completes sending all transmittable data on one line and moves to the next line to be sent. In order to use this internal time delay to inhibit transmitting data out of the printer port, the jumper between pin 2 and 11 must be installed along with a jumper between pins 1 and 12.

The internal time delay is also converted to RS232 levels and is available at pins 6 and 8 at the rear of the unit.

Pin	Signal
1	Chassis GND
2	Not used
3	Serial Printer Data
4	Not used
5	Not used
6	Printer time out
7	Signal Ground
8	Printer Time Out
9	Not used
10	"
11	"
12	"
13	"
14	"
15	"
16	"
17	"
18	"
19	"
20	Printer ready/Busy
21	Not used
22	"
23	"

Table 7-6. PRINTER PORT PIN ASSIGNMENT

The printer connector is located at the rear of the unit and is labeled "Printer Port".

Auxiliary Port Option

The auxiliary port provides a means of routing data from the line to an external device such as a printer. See the Features section of this manual. There are no jumper or selection option on the auxiliary port. The auxiliary port is located on the rear of the unit and is labeled "AUX PORT".

See Rear Panel Photo.

Rear Panel Switches and Controls

For the location of the rear panel switches and controls see Rear Panel Photo.

ON/OFF Switch

This two position switch controls the AC power to the unit and certain power-up and power-down sequences. Setting the switch to the ON position resets the circuitry in the IQ 120 and positions the cursor to home, and clears the display memory to unprotected nulls. This switch is located on the fan bracket on the rear of the unit. See Rear Panel Photo.

Brightness Control

This potentiometer controls the overall brightness of the CRT display. Brightness is usually adjusted so that the display raster (background) is barely visible or just below the point of visibility.

Contrast Control

This potentiometer controls the character brightness relative to the background. Contrast is usually adjusted after the brightness control.

BLOCK/FULL/HALF Switch

This three-position switch selects the mode of operation. The "B" position sets the block mode. The F and H positions select the appropriate full or half-duplex conversation mode.

Current Loop - RS232 Switch

On units which have current loop installed, this switch selects either current loop or RS232 operation through the main port. With the switch in the "CL" position, data is transmitted and received using current loop transmitters and receivers. With the switch in the position marked "RS", data is transmitted and received using RS232C mark and space levels.

Circuit Breaker

The circuit breaker is located on the fan bracket directly below the power ON/OFF switch. If excessive line current is drawn by the IQ 120 due to a malfunction the circuit breaker will trip causing the line current to be interrupted to the unit. The circuit breaker may be reset by pushing the red cylinder in.

WARNING: IF THE CIRCUIT BREAKER TRIPS, IT SHOULD NOT BE RESET UNTIL THE CAUSE OF THE TRIPPING IS CORRECTED.

IQ 120 Turn on Procedure

1. Insure the IQ 120 power cord is plugged into a grounded 115 vac outlet.
2. Set the ON/OFF switch on the rear of the IQ 120 to the ON position.
3. Wait approximately 20 seconds for the IQ 120 to warm up. The cursor should then appear at the home position with the rest of the screen clear.

NOTE: Turning the power switch on clears the display memory; therefore, if the display contains information which should be

transmitted to the remote computer or otherwise saved before turning the terminal OFF.

4. If the cursor does not appear after the warm-up period, depress the clear key. If this fails to produce the cursor, it is possible the brightness and/or contrast controls are misadjusted. They are adjusted as follows:

   a. Set the contrast control to the middle of its range.

   b. Turn the brightness control clockwise until the screen is bright, then reduce brightness slowly until the background is barely visible. The cursor should be present.

   c. Adjust brightness and contrast for desired presentation.

   d. If the cursor does not appear, make sure that the AC line cord is firmly plugged into the 115 vac line receptacle.