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Fast string-comparison routine serves the M6800

Thomas A Pickering
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The character-string subroutine in EDN Software Note #1 (Jan 5, 1978, pg 31) certainly proves useful. In our consulting work with the M6800, however, we use the subroutine shown here, which runs almost four times faster. This speed does exact a penalty: Because the stack pointer acts as a second index register, no interrupts are permitted.

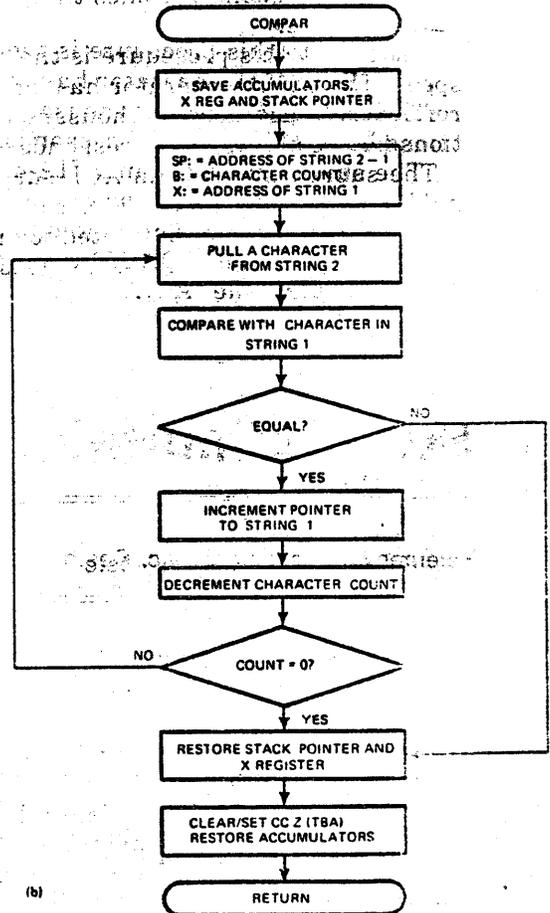
The key to the new COMPAR is the TBA (transfer B to A) instruction. Because the B register behaves like a counter, it will contain zero in the event of a successful string compare; otherwise it will be nonzero. The TBA sets the Z flag either up (good compare) or down so the calling program can branch accordingly.

Execution time for this subroutine is 23 machine cycles/character, compared with the 88 cycles/byte required by the original COMPAR subroutine. When you're testing a full 256-byte string, this difference can prove important. □

```

0000 0100 N      MA4 COMPAR
*
* STRING COMPARE SUBROUTINE
*
* ENTER WITH (X) = A PARA LIST OF 5 BYTES:
* A (STRING1)
* A (STRING2)
* CHAR COUNT
*
* ON RETURN IF CC Z IS SET THERE IS A MATCH
* NOTE: DISABLE INTERRUPTS WHILE THIS ROUTINE RUNS
*
0000 35      PSH A      SAVE ACCUMULATORS
0001 37      PSH J
0002 0F 0022 R  STS SPSAV  SAVE STACK POINTER
0003 0F 0024 R  STX XSAV   SAVE X-REGISTER
0004 AE 02      LUS 2,X   SP ← A(STRING2)
0005 34      DES       ADJUST SP
0006 E6 04      LDA d 4,X  LOAD CHAR COUNT
0007 E6 00      LDX 0,X   X ← A(STRING1)
*
000F 32      CMPI      GET A BYTE FROM STRING2
0010 A1 00      CMP A 0,X  COMPARE WITH BYTE IN STRING1
0011 26 04      BNE NOMCH NO MATCH
*
0014 04      INX       POINT TO NEXT CHAR IN STRING1
0015 0A      JEC 5     DECREMENT COUNT
0016 26 F7      BNE CMPI  DO ANOTHER COMPARISON
*
0016 BE 0022 R  NOMCH   RESUME SP
0017 FE 0024 R  RESUME X-REG
0018 17      TBA      SET/CLEAR CC Z
0019 13      PUL B     RESUME ACCUMULATORS
0020 27      PUL A
0021 29      RTS       ALL DONE
*
0022 0002      SPSAV  RMB 2  STACK POINTER TEMP SAVE
0024 0002      XSAV   RMB 2  REGISTER TEMP SAVE
*
END
    
```

(a)



(b)

Comparison subroutine (a) uses the stack pointer as a second index register to speed execution. A TBA instruction sets/clears condition code Z to allow conditional branching after the subroutine returns to the calling program (b).

Subroutine returns a random byte

Robert D Grappel
Hemenway Associates Inc, Boston, MA

Dozens of algorithms exist that produce pseudorandom numbers for games or more serious applications. These algorithms, however, furnish a finite numerical sequence, and the sequence's repetition might be objectionable. The algorithms also require a "seed" value, which must be varied if differing sequences must be generated.

In contrast, the subroutine presented here uses the reaction time of a human operator at a terminal as the source of randomness: The operator is prompted to press a key; the time required to respond becomes the source of the random value.

The key to this procedure is the computer's speed: Even if the operator has lightning-fast reflexes, the μ P executes thousands of instructions before the operator responds.

The subroutine uses an ACIA-driven terminal on a Motorola 6800 processor system. On entry, the operator is prompted to press a key; a monitor routine (PDATA) outputs the character string. The ACIA is then reset and reinitialized.

```

0001 0000 0000 N     NAR RANDOM
0002
0003
0004
0005
0006
0007 0000 8008 ACIA EQU 8008          ACIA ADDRESS OF TERMINAL INPUT
0008 0000 802F PDATA EQU 802F        PROMPT-OUTPUT ROUTINE ADDRESS
0009
0010 0000 0E 0010 R  RFRND LDA 8PROMPT  ISSUE USPK PROMPT
0011 0003 8D 807C JSR PDATA          POINT TO ACIA
0012 0006 2F 8008 LDR A 880          ACIA
0013 0007 2A 03 LDR A 880          ACIA
0014 0008 47 00 STA A 0,X          RESET ACIA
0015 000D 2A 15 LDA A 8815         INITIALIZE PIA
0016 000F 27 00 STA A 0,X          CHECK PIA STATUS ON INPUT
0017 0011 44 00 LOOP INR A 0,X          INCREMENT COUNTER
0018 0013 5C INC R
0019 0014 47 BSR A
0020 0015 74 FA BCC LOOP          LOOP UNTIL KEY PRESSED
0021
0022 0017 4A 01 LDA A 1,X          CLEAR CHARACTER
0023 0019 39 RTS
0024
0025 001A 4A PROMPT FCC "HIT ANY KEY"
0026 0025 000A FIB 8000A
0027 0027 0000 FIB 80000
0028 0029 04 FCB 44
0029
0030
0031
0032
0033
0034
0035
0036
0037
0038
0039
0040
0041
0042
0043
0044
0045
0046
0047
0048
0049
0050
    
```

The computer then loops while waiting for the key depression. When the ACIA status indicates an input, the character is read (clearing the ACIA), and the program returns the number of times it looped while waiting for the key depression. This number is effectively random and can assume any value between 0 and 256₁₀.

EDM

Subroutine return performs a computed jump

Robert D Grappel
Hemenway Associates Inc, Boston, MA

One problem that arises frequently in programming the 6800 μ P involves making a jump to an address which results from a computation. This jump is especially difficult if the index register is used to pass information. You can circumvent this problem with a self-modifying indexed-jump instruction, but this programming trickery makes understanding and debugging the code very difficult. A much cleaner and more efficient method uses a

```

LDA    A    JADDR    ; load desired jump address
LDB    B    JADDR+1
PSH    B
PSH    A
RTS
    
```

These 6800 instructions let you jump to a computed address.

subroutine-return (RTS) instruction. If you initialize the stack properly, such an RTS becomes an excellent computed jump.

The RTS is essentially a jump to an address which lies on the top of the system stack. Normally, a JSR (jump to subroutine) or BSR (branch to subroutine) instruction places a return address on the stack. However, you can stack addresses directly using the PSH (push) instruction.

Suppose that the A and B accumulators contain the address of the jump destination: A holds the high byte and B the low byte. (This address can result from calculations or other manipulations.) If the accumulators are pushed onto the stack, B followed by A, the effect is the same as that of a subroutine call. When an RTS is executed, the program unstacks the just-pushed address and jumps there. Thus, the program jumps to the address contained in A and B.

EDM

Implement a FIFO stack with software

Robert Grappel
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A first-in, first-out stack finds application wherever asynchronous processes must pass data. Hardware FIFO's are available, but if high speed is not required, you can readily program a FIFO stack. The technique is termed circular buffering because it uses an area of RAM in a circular fashion. The system stores data in the buffer and retrieves it sequentially until it reaches the end of the RAM area. The next element used is the first location in the buffer. Two pointers mark the data in the buffer: The head-pointer indicates the first available location, while the tail-pointer indicates the oldest data entry. As the system stores data, the head-pointer moves forward and loops around to the top of the buffer; the buffer is full when this pointer wraps around to meet the tail-pointer. Similarly, when the system extracts data from the buffer, the tail-pointer moves; the buffer is empty when it meets the head-pointer. Fig 1 shows the initialization, Fig 2 the pointer move, Fig 3 the push-data and Fig 4 the pull-data subroutines, coded for the M6800. □

```

0000 0000 N      NAM FIFO
          *
0000 070A R      BUFFER RMB 10  ARBITRARY LENGTH CIRCULAR BUFFER
000A 070A R      #BUFEND EQU *    END OF BUFFER AREA
000A 0002 R      HDPNT RMB 2     HEAD-POINTER
000C 0702 R      TLPNT RMB 2     TAIL-POINTER
          *
          *
000E CE 0000 R  INIT LDX #BUFFER  BEGIN INITIALIZATION
0011 FF 000A R      SIX HDPNT     INIT HEAD-POINTER
0014 FF 000C R      SIX TLPNT     INIT TAIL-POINTER
          *
          *
          *

```

Fig 1—Set up the buffer, head-pointer and tail-pointer before using the FIFO.

```

0017 08      MVEPTR INX      MOVE POINTER IN X-REG
0018 8C 000A R  CPX #BUFEND  BEYOND BUFFER?
001B 26 03      BNE DONE     NO, RETURN
          *
001D CE 0000 R  LDX #BUFFER  YES, RESET POINTER
          *
0020 39      DONE  RTS

```

Fig 2—This subroutine moves a pointer to the next location in the buffer. The system increments the pointer unless such a move would bring the pointer beyond the buffer. In that case it sets the pointer to the top of the buffer.

```

0021 FE 000A R  PUSH LDX HDPNT  GET HEAD-POINTER
0024 A7 00      STA A 0,X     STORE BYTE
0026 B0 0017 R  JSR MVEPTR   MOVE POINTER
0029 8C 000C R  CPX TLPNT   POINTERS MEET?
002C 26 02      BNE NOCAR    NO
          *
002E 0J      SEC             YES, SET CARRY BIT
002F 39      RTS
          *
0030 FE 000A R  NOCAR STX HDPNT NEW HEAD-POINTER
0033 0C      CLC             CLEAR CARRY
0034 39      RTS

```

Fig 3—Use this coding to place the contents of the A register in the buffer. If there is no room for the store, the system sets the carry bit before the return; otherwise it clears the carry bit.

```

0035 FE 000C R  PULL LDX TLPNT  GET TAIL-POINTER
0038 BC 000A R  CPX HDPNT   BUFFER EMPTY?
003B 27 0A      BEQ EMPTY    YES
          *
003D A6 00      LDA A 0,X     NO, GET BYTE
003F B0 0017 R  JSR MVEPTR   MOVE POINTER
0042 FF 000C R  STX TLPNT   NEW TAIL-POINTER
0045 0C      CLC             CLEAR CARRY BIT
0046 39      RTS
          *
0047 00      EMPT  SEC             SET CARRY
0048 39      RTS

```

Fig 4—This subroutine gets a byte from the buffer and returns it to the A register. If the buffer is empty, the subroutine sets the carry bit before the return; otherwise it clears the carry bit.

Share your experiences

Have you developed hardware that expands development-system capabilities? How about software (even games you've programmed for a specific system)? Hobby applications such as ham radio or robot-construction projects make interesting reading, too, and we solicit your inputs.

Hash coding

You can search a hash-coded table at speeds virtually independent of the number of items in that table. Here's how.

Jack Hemenway and Edward Teja,
Associate Editors

Along with the convenience of storing data in a computer's memory comes the problem of retrieving that data when you need it. The actual process of reading data from memory locations is no problem; rather, the trouble lies in organizing the storage process so that symbols are:

- Stored in unique locations
- Stored only once
- Stored quickly
- Retrieved quickly.

Meeting these needs requires making some design decisions. You could store data sequentially, for example, but retrieving a particular item in that case requires knowing the item's relative position in the series; if you know only the stored symbol itself, you must search for it linearly through the list—a time-consuming process. Alternatively, you could store the items in a table and index them.

What type of index would make sense in that case? Consider for a moment what an entry in an index is—a reference to another data item. Rather than generate this reference in a manner unrelated to the symbol itself, why not perform some operation on the stored symbol to produce its index entry? Better yet, why not make this operation actually produce the address of the symbol in the table? This process is termed hashing.

Finding the key

In hashing (or hash coding), the *key* is the portion of the stored symbol used to generate the needed address. It should be as small as possible (for convenience and simplicity), yet large enough to ensure that each symbol, when hashed, produces as unique an address as is practicable. (If two symbols produce the same address, the result is termed a *collision*.)

Every symbol consists of characters. To store the *i*th symbol in a collection, you must create a record (R_i). This record must be long enough to store the entire symbol; therefore, R_i can be divided into R_{i1} , R_{i2} , R_{i3} and so on, corresponding to the characters in the symbol: S_{i1} , S_{i2} , S_{i3} ... The usual procedure for storing a symbol collection provides enough table-entry space to accommodate the longest symbol; shorter symbol entries are

then padded, typically with blanks or nulls.

The algorithm that provides a symbol's *home address* in this process is termed the hashing function. If the first two characters of each symbol (S_{i1} and S_{i2}) constitute the key, for example, the hashing algorithm (H) is some function of those elements. The home address of S_i is thus defined by $H(S_{i1}, S_{i2})$.

Many types of algorithms can effectively hash-code symbols. Standard versions employ one of the following methods:

- Division—Divides the key by an integer n and uses the remainder to produce the home address.
- Random—Uses a pseudorandom number generator with the symbol's key as its seed. The first random number produced becomes the symbol's home address, after it's normalized.
- Midsquare—Multiplies the key by itself and masks out all but a middle k -bit field in the product; this field becomes the home address.
- Radix—Treats the key as a string of octal digits and converts them to base 10. A middle k -bit field of this number becomes the home address.
- Algebraic coding—Treats the key as a polynomial, divides it by a constant polynomial and uses the remainder to form the home address.
- Folding—Picks several k -bit fields from the n -bit key and adds them to produce the home address.
- Digit analysis—Performs a skewness test on each digit of the key, selecting the k best (least skewed) digits and deleting them, leaving the home address.

Building an assembler's symbol table

EDN faced the problem of generating a symbol table when writing a cross assembler (designated XA6809) to generate code for the 6809 μ P on a 6800. In this case, the symbol table must contain the labels used in a program being assembled. The assembler creates a record (R_i) corresponding to each label. Each time it encounters a label, it must find the corresponding record; if no such record exists, it must create one.

The location in which a label's record is stored is determined by the hashing function—sometimes also termed a mapping function or randomizing technique. Because it is hash coded, the symbol table must have a defined size; in XA6809, the assembler itself calculates

1447			* TABLE MANIPULATION ROUTINES FOR TABLES	1595			* FIND NEXT SLOT IN SYMTAB
1448			* SYMTAB AND MUTAB	1596			* SYMPTR: =SYMPTR+9 (MODULO NSYM)
1449				1597			
1450			* STORAGE LOCATIONS USED BY THE ROUTINES	1598	0B84 FF 04BA R	SYMPTR LDX	SYMPTR GET ACCURATE SLOT1
1451				1599	0B87 08	INX	SYMPTR: =SYMPTR+9
1452	0AC3 0002	PSTNO1 RMB 2	ADDRESS OF MNEFRONT	1600	0B88 08	INX	
1453	0AC5 0002	PSTNO2 RMB 2	ADDRESS IN THE TABLE	1601	0B89 08	INX	
1454	0AC7 0001	PCOUNT RMB 1	LENGTH OF MNEFRONT	1602	0B8A 08	INX	
1455	0AC8 0002	TBADD RMB 2	TABLE POINTER	1603	0B8B 08	INX	
1456	0ACA 0004	HSMBL RMB 4	SYMBOL TEMP LOC	1604	0B8C 08	INX	
1457	0ADD 0002	HKEYA RMB 2	HASHED CODE	1605	0B8D 08	INX	
1458	0AD2 0002	HKEYB RMB 2	TEMP LOC FOR HASHED CODE	1606	0B8E 08	INX	
1459	0AD4 0002	HSVA1 RMB 2	TEMP LOC FOR PTR	1607	0B8F 08	INX	
1460	0AD6 0002	HSVA2 RMB 2	TEMP LOC FOR PTR	1608			* BEYOND SYMTAB ?
1461				1609			
1462				1610			
1463			* STORE A SYMBOL IN SYMTAB	1611	0B90 BC 04AA R	CPI	SYMEND
1464			* ON ENTRY DESCRA CONTAINS ADDRESS OF	1612	0B93 26 03	BNE	NO
1465			* THE SYMBOL AND DESCRA CONTAINS THE LENGTH	1613	0B95 FE 04A0 R	LDX	SYMTAB
1466			* A STANDARD HASH CODED METHOD IS USED	1614	0B98 FF 04BA R	STX	SYMPTR
1467				1615	0B9B 39	RTS	SAVE PTR TO ENTRY
1468				1617			
1469	0A18 BD 0BAA R	STOSYM JSR	HASH GET HASHED KEY	1618			* DELETE LAST SYMBOL ENTERED
1470	0A0B FF 04BA R	STX	SYMPTR SAVE	1619	0B9C FE 04BA R	DELSYM	LDX SYMPTR
1471	0A0E BD 2092 R	JSR	HREF	1620	0B9F 84 20	LDA	A #820
1472	0A01 FE 04BA R	LDX	SYMPTR	1621	0BA1 C6 09	LDA	B #9
1473				1622			
1474			* SEE IF LOC(HKEYA) IS EMPTY	1623	0BA3 A7 00	DEL1	STA A 0,X
1475				1624	0BA5 08	INX	BLANK BYTE
1476	0AE4 A6 00	SYMA LDA	A 0,X GET FIRST CHAR	1625	0BA6 5A	DEC	B
1477	0AE6 81 20	CHP	A #820 BLANK ?	1626	0BA7 26 FA	BNE	DEL1
1478	0AE8 26 2F	BNE	SYMB NO	1627			
1479				1628	0B89 39	RTS	YES, RETURN
1480			* STORE SYMBOL IN SYMTAB	1629			* HASH SYMBOL TO PRODUCE A KEY
1481				1631			
1482	0AE4 FF 0AD4 R	STX	HSVA2 SAVE TABLE PTR	1632			
1483	0AED CE 0ACA R	LDX	#HSMBL POINT TO HSMBL	1633	0BAA CE 2020	HASH	LDX #82020
1484	0AFO CF 0AD4 R	STX	HSVA1 SAVE	1634	0BAD 1F 0ACA R	STX	HSMBL
1485	0AF3 C6 04	LDA	B #6 LOAD SYMBOL LENGTH	1635	0BBD FF 0ACC R	STX	HSMBL+2
1486				1636	0BB3 FF 0ACE R	STX	HSMBL+4
1487				1637			
1488			* DD TRANSFER	1638			* MOVE SYMBOL TO HSMBL
1489	0A05 FE 0AD4 R	SYMI LDX	HSVA1 POINT TO HSMBL	1639			
1490	0A06 A6 00	LDA	A 0,X GET CHAR	1640	0BB6 CE 0ACA R	LDX	#HSMBL
1491	0AFA 08	INX		1641	0BB9 FF 0AD4 R	STX	HSVA2
1492	0A0B FF 0AD4 R	STX	HSVA1 POINT TO NEXT CHAR	1642	0BBC FE 04B3 R	LDX	DESCRA
1493	0A0E FE 0AD4 R	LDX	HSVA2 POINT TO TABLE ENTRY	1643	0BBF FF 0AD4 R	STX	HSVA1
1494	0BD1 A7 00	INX	STORE CHAR IN SYMTAB	1644	0BC2 F6 04B5 R	LDA	B DESCRC
1495	0B03 08	INX		1645			
1496	0B04 FF 0AD4 R	STX	HSVA2 POINT TO NEXT POSITION	1646	0BC5 FE 0AD4 R	HASH1	LDX
1497	0B07 5A	DEC	B ALL DONE ?	1647	0BC8 A6 00	LDA	A 0,X
1498	0B08 26 EB	BNE	SYMI NO	1648	0BCA 08	INX	
1499				1649	0BCB FF 0AD4 R	STX	HSVA1
1500			* STORE LC AND SET INFO BYTE	1650	0BCE FE 0AD4 R	LDX	HSVA2
1501				1651	0BD1 A7 00	STA	A 0,X
1502	0B0A B6 04AR R	LDA	A LC GET LC	1652	0BD3 08	INX	
1503	0B0D A7 00	STA	A 0,X STORE	1653	0BD4 FF 0AD4 R	STX	HSVA2
1504	0B0F B6 04AC R	LDA	A LC+1 GET LC+1 BYTE OF LC	1654	0BD7 5A	DEC	B
1505	0B12 A7 01	STA	A 1,X STORE	1655	0BD8 26 EB	BNE	HASH1
1506	0B16 86 40	LDA	A #840 INFO BYTE =RELOC. DEFINED	1656			
1507	0B1A A7 02	STA	A 2,X	1657			* FOLD OVER HSMBL CREATING KEYA
1508	0B18 39	RTS	RETURN	1658			
1509				1659	0BDA FE 0ACA R	LDX	HSMBL
1510			* COMPARE HSMBL WITH ENTRY IN SYMTAB	1660	0BDD FF 0AD0 R	STX	HKEYA
1511				1661	0BE0 FE 0ACC R	LDX	HSMBL+2
1512	0B19 BD 0B6F R	SYMB JSR	SYNCHP COMPARE	1662	0BE3 FF 0AD2 R	STX	HKEYB
1513	0B1C 26 10	BNE	SYMB NO MATCH	1663	0BE6 CE 0AD0 R	LDX	#HKEYA
1514				1664	0BE9 BD 0E5 R	JSR	ADD16
1515			* ERROR, SYMBOL ALREADY IN TABLE	1665	0BEC FE 0ACE R	LDX	HSMBL+4
1516				1666	0BEF FF 0AD2 R	STX	HKEYB
1517	0B1E FE 04BA R	LDX	SYMPTR GET ADDRESS OF ENTRY	1667	0BF2 CE 0AD0 R	LDX	#HKEYA
1518	0B21 86 80	LDA	A #880	1668	0BF3 BD 0E5 R	JSR	ADD16
1519	0B23 AA 08	ORA	A 8,X	1669			* HKEYA: =REMAINDER OF HKEYA/NSYM
1520	0B25 A7 08	STA	A 8,X	1670			
1521	0B27 CE 0206	LDI	#820A LOAD ERROR#	1671			
1522	0B2A BD 10DE R	SYMB1 JSR	PRINT IT	1672	0BF8 B6 0AD0 R	LDA	A HKEYA
1523	0B2D 39	RTS	RETURN	1673	0BF9 F6 0AD1 R	LDA	B HKEYA+1
1524				1674	0BFE FE 04A2 R	LDX	NSYM
1525			* FIND ANOTHER SLOT IN SYMTAB FOR SYMBOL	1675	0C01 FF 0AD2 R	STX	HKEYB
1526				1676	0C04 CE 0AD2 R	LDX	#HKEYB
1527	0B2E BD 0B84 R	SYMB JSR	SYNCHP GET ANOTHER SLOT	1677	0C07 BD 0E8A R	JSR	DIV16
1528	0B31 BC 0AD0 R	CPI	HKEYA CHECKED ALREADY ?	1678	0C0A FF 0AD0 R	STX	HKEYA
1529	0B34 27 02	BEQ	NO YES, TABLE IS FULL	1679			* HKEYA: =HKEYA+9
1530				1680			
1531	0B36 20 AC	BRA	SYMA TRY AGAIN	1681			
1532				1682	0C0D 4F	CLR	A
1533	0B38 CE 0221	LDX	#8221 LOAD ERROR#	1683	0C0E C6 09	LDA	B #9
1534	0B3B 20 ED	BRA	SYMB1 PRINT IT & RETURN	1684	0C10 CE 0AD0 R	LDX	#HKEYA
1535			* ROUTINE TO COMPARE SYMBOL WITH ENTRY	1685	0C13 BD 0E86 R	JSR	HPV16
1536				1686	0C16 B7 0AD0 R	STA	A HKEYA
1537				1687	0C19 F7 0AD1 R	STA	B HKEYA+1
1538	0B6F FF 0AC3 R	SYNCHP STX	PSTNO1 SAVE PTR TO ENTRY	1688			* ADD IN BASE ADDRESS OF SYMTAB
1539	0B72 86 06	LDA	A #6	1689			
1540	0B74 B7 0AC7 R	STA	A PCOUNT PCOUNT: =L(SYMBOL)	1690			
1541	0B77 CE 0ACA R	LDX	#HSMBL	1691	0C1C FE 04A0 R	LDX	SYMTAB
1542	0B7A FF 0AC5 R	STX	PSTNO2 POINT TO HSMBL	1692	0C1F FF 0AD2 R	STX	HKEYB
1543	0B7D CE 0AC3 R	LDX	#PSTNO1 POINT TO PARMS	1693	0C22 CE 0AD0 R	JSR	ADD16
1544	0B80 BD 095E R	JSR	COMPAR COMPARE	1694	0C25 B0 0E5 R	LDX	HKEYA
1545	0B83 39	RTS		1695	0C28 FE 0AD0 R	LDX	ADD16
1546				1696	0C2B 39	RTS	

Fig 1—Hashing a symbol provides a memory address for storing that symbol—so long as there isn't another symbol already stored at that address.

this size during its first pass over the source code—the table occupies all available memory after the requisite macro tables have been set up.

The entire space assigned to the symbol table (SYMTAB) is filled with blanks (20_H) during initialization. Each table entry occupies nine bytes of table space:

SSSSSS First six characters of the symbol, padded with blanks as necessary

XX 2-byte address of the symbol

F One byte of bit flags, formatted as:
 Bit 7—Redefined symbol
 Bit 6—Relocatable symbol
 Bit 5—Macro name
 Bit 4—Common symbol
 Bit 3—External symbol

The hashing function produces a symbol's home address

Bit 2—Entry-point name
 Bit 1—Unused
 Bit 0—Unused.

Putting symbols in memory

Fig 1 shows the software used in the storing operation. The assembler uses a subroutine named STOSYM (store symbol) to put a symbol into the table. A pointer indicates the beginning of the string to be stored, and a variable named DESCRC contains that string's length. The subroutine then calls the hash routine (HASH) to produce an address from the string.

HASH moves the symbol's first six characters into a variable location—these characters form the key. (Because the assembler's syntax rules limit label lengths to a maximum of six characters, the entire symbol is the key, affording the greatest probability of each symbol's hashing to a unique address and thus avoiding collision.) If the symbol doesn't have six characters, HASH pads it with blanks to fill out the entry. The routine then uses the folding method to hash the key (Fig 2): It adds the symbol's first two bytes to its second two and adds that sum to the third byte pair, ignoring overflows. It divides this value by the number of entries possible in the table; the remainder of this division is then multiplied by nine (the size of each entry). The result is added to the symbol table's base address to produce the home address; this home address is then returned to STOSYM in the index register.

STOSYM checks the home address to ensure that it contains only blanks; if it does, STOSYM stores the symbol there, along with its value and flags. If the location is occupied, however, the symbol in question might have already been stored there. To test for this condition, a compare routine (COMPAR) compares the stored symbol with the one to be stored, indicating the result in the processor's condition codes.

If the stored symbol is not the same as the one to be stored, the two symbols are in collision. To handle this collision, another routine (SYMMOD) provides a new address—specifically, it moves the home address of the symbol to be stored nine bytes further through the table. If this new location is empty, the entry goes there; if it is occupied, COMPAR again compares the symbol stored in the location with the symbol to be stored, and if they are not the same, SYMMOD moves the home address nine more bytes through the table.

If SYMMOD reaches the end of the table before finding an unoccupied location, the home address wraps around to the starting location and an error message results. If the compare routine ever indicates that the stored symbol matches the one to be stored, a different error message is produced—any symbol can only be stored once, because program labels must be unique.

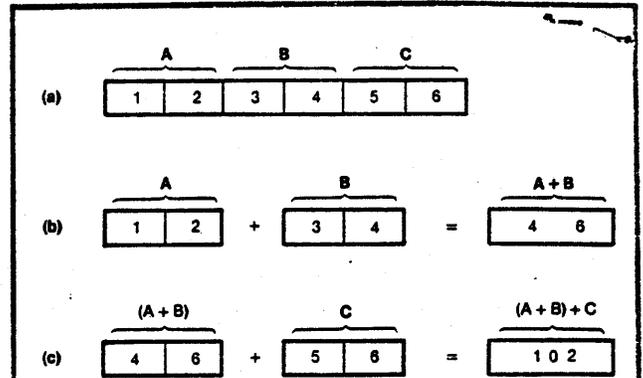


Fig 2—The folding method of generating a symbol's home address treats the symbol's 2-character key as three 16-bit binary numbers (a), hashed by adding the first two (b) and then adding the resulting sum to the third (c).

```

1546          * LOOK UP SYMBOL IN SYNTAB
1547          * ON ENTRY DESCRA CONTAINS ADDRESS OF SYMBOL
1548          * AND DESCRC CONTAINS THE LENGTH OF THE
1549          * SYMBOL
1550          * ON RETURN:
1551          * B=VALUE OF INFO BYTE
1552          * B=FF SYMBOL NOT FOUND
1553          * X=VALUE OF SYMBOL
1554          *
1555          *
1556          *
1557          *
1558          *
1559          *
1560          *
1561          *
1562          *
1563          *
1564          *
1565          *
1566          *
1567          *
1568          *
1569          *
1570          *
1571          *
1572          *
1573          *
1574          *
1575          *
1576          *
1577          *
1578          *
1579          *
1580          *
1581          *
1546      0B3D 8D 0BAA R   LKPSYM JSR   HASH   GET KEY
1547      0B40 FF 04BA R   STX   SYMPTR SAVE
1548      0B43 7D 04AD R   TST   PASS  PASS1?
1549      0B46 27 06      BEQ   LKPSM1 YES
1550
1551      0B48 8D 2092 R   JSR   XREF   GET KEY
1552      0B4B FE 04BA R   LDX   SYMPTR
1553
1554      0B4E A6 00      LKPSM1 LDA A 0, X
1555      0B50 81 20      CMP A #20  BLANK?
1556      0B52 26 03      BNE  LKPSM3 NO
1557
1558      *
1559      * ENTRY NOT IN SYNTAB
1560      0B54 C6 FF      LKPSM2 LDA B #FF  LOAD RC
1561      0B56 39      RTS
1562
1563      *
1564      * COMPARE SYMBOL WITH ENTRY IN SYNTAB
1565      0B57 BD 0B6F R   LKPSM3 JSR   SYNCHP  COMPARE
1566      0B5A 26 08      BNE  LKPSM4 NO MATCH
1567
1568      *
1569      * FOUND, EXTRACT INFO. AND VALUE
1570      0B5C FE 04BA R   LDX   SYMPTR  POINT TO ENTRY
1571      0B5F EA 08      LDA B 8, X  GET INFO BYTE
1572      0B61 E8 06      LDX   6, X  GET VALUE
1573      0B63 39      RTS
1574
1575      *
1576      * PROBE AGAIN FOR SYMBOL IN SYNTAB
1577      0B64 BD 0B64 R   LKPSM4 JSR   SYMMOD  GET NEXT KEY
1578      0B67 BC 0AD0 R   CPI   #KEYA  ALREADY CHECK'D?
1579      0B6A 2A E2      BNE  LKPSM1 NO, TRY AGAIN
1580      0B6C C6 FF      LDA B #FF   SET RC
1581      0B6E 39      RTS
    
```

Fig 3—This routine looks up a symbol in much the same way that the routine in Fig 1 stores one. Here, though, a match between the sought symbol and the stored one doesn't produce an error message.

What goes in must come out

To reverse the hash-coding process, a routine named LKPSYM (Fig 3) looks up a symbol in the table. This routine is called with the searched-for string's address in the pointer DESCRA and its length in DESCRC. LKPSYM operates like STOSYM, except that it expects COMPAR to find a match; it indicates such a match with a status code in accumulator B. When the symbol is found, the routine puts its address in SYMPTR (symbol pointer), and the routine XREF forms a cross-reference output block for the symbol.

Multitask μ P executive routine uses only six instructions

Here's a simple six-instruction subroutine that lets your 6800 microprocessor control several external processes simultaneously. To use it, organize your software as follows:

1. Set up a process-control block as shown for each process to be controlled.
2. Write a program for each process as if no other programs are running in the same microprocessor.
3. Insert JSR SPND instructions into each program at convenient points to allow other programs to run.

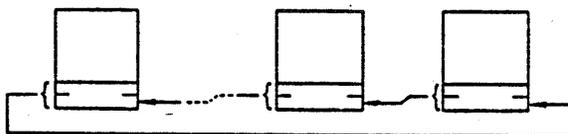
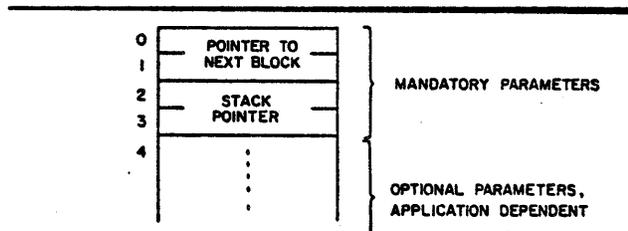
Whenever a process suspends itself by executing a subroutine jump to SPND, the SPND routine swaps the process-control block pointer (PCB) and the stack pointer to set up the next process. Then a simple return instruction causes the program for that process to start running again where it left off. Each process-control block contains at least two parameters: a pointer to the next control block and a stack pointer

A six-instruction executive routine

```

SPND LDX PCB    SET INDEX REGISTER TO CURRENT
                CONTROL BLOCK
        STS 2,X  SAVE CURRENT STACK POINTER
        LDX X   SET INDEX REGISTER TO NEXT CON-
                TROL BLOCK
        STX PCB  SAVE CONTROL BLOCK POINTER
        LDS 2,X  GET NEW STACK POINTER
        RTS     RETURN TO PROCESS
  
```

Process-control block



Each block points to the next in a circular list.

the current control block. The control blocks are arranged in a circular list so that SPND will automatically return to the first block after executing the last.

A sample program illustrates how process control

Start-up routine

```

* SET INDEX REG-
* ISTER TO FIRST
* CONTROL BLOCK,
* GET CORRESPONDING
* STACK POINTER,
* AND BEGIN EXECUTION:
*
START LDX PCB
      LDS 2,X-
      RTS
  
```

A sample program

```

* APPLICATION DEPENDENT
* PROCESS CONTROL BLOCK
* PARAMETERS:
*
MODE      EQU 4
STAT      EQU 5
BUFIN     EQU 6
BUFOUT    EQU 8
*
* FETCH A BUFFER. IF
* NO BUFFERS ARE AVAIL-
* ABLE, SUSPEND AND TRY
* AGAIN:
*
IDLE      JSR BUFGET
          BNE READY
          JSR SPND
          BRA IDLE
*
* PREPARE TO RECEIVE:
*
READY     LDX PCB
          CLR STAT,X
          LDAA #1
          STAA MODE,X
          JSR RCV
*
* SUSPEND. THEN, IF
* AN INPUT MESSAGE HAS
* BEGUN, GO TO INPUT.
* IF AN OUTPUT MESSAGE
* IS WAITING, GO TO
* OUTPUT. OTHERWISE,
* REPEAT:
*
LOOP      JSR SPND
          LDAA STAT,X
          BNE INPUT
          LDX BUFOUT,X
          BNE OUTPUT
          BRA LOOP
  
```

blocks and SPND instructions work together. Only the idle loop is shown. The complete program supervises an interrupt routine, which handles message flow to and from a teletypewriter. The program sets the teletypewriter port to receive, then waits for the interrupt routine to receive the first character. If an output message arrives first, the port is switched to output, and the message is printed on the teletypewriter. Notice that the program always suspends itself while waiting for something to happen.

All communication between background and interrupt levels occurs via the process-control block. **MODE**, for example, tells the interrupt routine whether to send or receive. **STAT** tells the background program that the interrupt routine has started or completed the message. **BUFIN** and **BUFOUT** are pointers to tell the interrupt routine where to store an input message or find an output message in microprocessor memory.

In a typical communications application, there might be several I/O ports, each having its own process-control block. Each control block may have a separate background program, or a single program may be shared by all control blocks. The sample program can be shared by multiple control blocks, because

- All data references are either to or through the control block.

- Each control block has its own return address stack.

Be careful with this multitask operation, however.

Remember:

1. Processes aren't suspended by a "time-slicing" interrupt, but must suspend themselves often enough to let other programs run.

2. Processes should suspend themselves only at points where it is safe to lose the register contents, since SPND doesn't restore any registers except the stack pointer. (If this is a problem, register-save-and-restore instructions can easily be added to the SPND routine.)

3. Interrupts may remain enabled continuously, but every control block's return-address stack should be large enough to accommodate every interrupt routine's worst-case requirements.

4. All control blocks and stacks as well as the-PCB pointer must contain proper initial values before starting the system. A brief start-up routine initiates normal operation.

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COMPARE TWO MEMORY AREAS

LABEL OPCODE OPERAND(S)

1 8 3

* THIS PROGRAM COMPARES TWO AREAS OF MEMORY BYTE FOR BYTE. *
 * IT IS INTENDED TO TEST PROGRAM LOADING AT 200H AGAINST *
 * THE SAME PROGRAM LOADED AT 2880H. IT THEREFORE SERVES *
 * AS A MEMORY TEST OR CAN BE USED TO COMPARE TWO PROGRAMS *
 * AGAINST EACH OTHER. WHEN AN UNEQUAL CONDITION IS FOUND *
 * LOCATION AND MEMORY CONTENTS ARE DISPLAYED AND PROGRAM *
 * EXITS TO MONITOR. TO CONTINUE, CORRECT THE BYTE IN ERROR*
 * AND RESTART THIS PROGRAM FROM LOAD ADDRESS. IT CAN BE *
 * RELOCATED ANYWHERE IN MEMORY, AND THE TWO COMPARE AREAS *
 * CAN BE RELOCATED ALSO. *

 ***** H. G. FRIEDMAN *****
 ***** FEBRUARY 12, 1981 *****

*EQUATES

*
 PRGRM EQU \$0200
 COPY EQU \$2880
 DEBUG EQU \$FE64
 PUTHX EQU \$FF02
 PUTCHR EQU \$FCBC
 BYTI EQU \$C0
 PTR1 EQU \$C2
 PTR1+1 EQU \$C3
 PTR2 EQU \$C4
 PTR2+1 EQU \$C5

	ORG \$4F00	RELOCATE AS REQUIRED		LDA \$20	LD A SPACE
	LDX #PRGRM	LD X REG W/FIRST ADDRESS		JSR PUTCHR	PRINT IT
	LDA 0,X	LD FIRST DATA BYTE		LDA PTR2	PRINT COMPARE ADDRESS
	STAA BYTI	SAVE IT		JSR PUTHX	HI ORDER
	INX	ADVANCE X POINTER		LDA PTR2+1	
	STX PTR1	SAVE IT		JSR PUTHX	LO ORDER
	LDX #COPY	LD X REG W/COMPARE ADDRESS		LDA \$60	CARRIAGE RETURN, LINE
TEST	LDA 0,X	LD COMPARE DATA BYTE		JSR PUTCHR	FEED
	CMPA BYTI	CIF =		LDA \$20	LD A SPACE
	BNE OUT	NO, GO EXIT		XRR RXXR	RRXX XX
	INX	ADVANCE X POINTER		LDAB #\$0B	LD COUNT
	STX PTR2	SAVE IT	LOOP	JSR PUTCHR	PRINT SPACE
	LDX PTR1	BEGIN NEXT COMPARE		DECB	
	LDA 0,X			BNE LOOP	PRINT 11 SPACES
	STAA BYTI			LDX PTR1	
	INX			DEX	ADJUST X POINTER
	STX PTR1	SAVE NEXT X POINTER		LDA 0,X	
	LDX PTR2	RESTORE NEXT COMPARE ADDRESS		JSR PUTHX	PRINT MEMORY CONTENTS
	LDA 0,X			LDA \$20	LD A SPACE
OUT	BRA TEST	LOOP TO DO AGAIN		LDAB #\$03	LD COUNT
	LDA PTR1	BEGIN EXIT ROUTINE	LOOP1	JSR PUTCHR	PRINT SPACE
	JSR PUTHX	PRINT HI ORDER ADDRESS		DECB	
	LDA PTR1+1	LD LO ORDER ADDRESS		BNE LOOP1	PRINT 3 SPACES
	SUBA #01	ADJUST POINTER		LDX PTR2	
	JSR PUTHX	PRINT LO ORDER ADDRESS		LDA 0,X	
				JSR PUTHX	PRINT MEMORY CONTENTS
				JSR DEBUG	EXIT TO MONITOR
				END	

PROGRAM GETCHR ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA	
0051	0847	20 D6	20 R@VR	BRA	GET1 NEXT CHARACTER
0052	0849	36	VT 36	GET6 PSH A	SAVE KEY VALUE
0053	084A	30	30	TSX	GET ENDMEM VALUE
0054	084B	A6 01	A6 D01	LDA A	1,X
0055	084D	CE 1000	CE E1000	LDX	#4096 SET LOOP FOR QUARTER SECOND
0056	0850	4D	4D	TST A	IF REPEAT, USE SIXTEENTH SECOND
0057	0851	27 03	27 R@VU	BEQ	GET7
0058	0853	CE 0400	CE E0400	LDX	#1024
0059	0856	DF 1A	VU DF D@A	GET7 STX	ENDMEM SAVE LOOP COUNT
0060	0858	32	32	PUL A	RESTORE KEY VALUE
0061	0859	36	36	PSH A	
0062	085A	FE FC64	FE E@%	LDX	KBDPIA GET KBD PIA ADDRESS
0063	085D	A1 00	A1 D00	CMP A	0,X IS KEY STILL DOWN
0064	085F	27 03	27 R@VV	BEQ	GET8 LOOP IF KEY STILL DOWN
0065	0861	4F	4F	CLR A	FLAG TO INDICATE KEY UP
0066	0862	20 05	20 R@VW	BRA	GET10
0067	0864	DE 1A	VV DE D@A	GET8 LDX	ENDMEM RESTORE LOOP COUNT
0068	0866	09	09	DEX	
0069	0867	26 ED	26 R@VU	BNE	GET7 LOOP WHILE KEY IS DOWN
0070	0869	97 1A	VW 97 D@A	GET10 STA A	ENDMEM SAVE KEY VALUE OR KEY-UP FLAG
0071	086B	30	30	TSX	GET UPPER/LOWER CASE FLAG
0072	086C	A6 02	A6 D02	LDA A	2,X
0073	086E	97 1B	97 D@B	STA A	ENDME1 SAVE CASE FLAG
0074	0870	32	32	PUL A	RESTORE KBD CHARACTER
0075	0871	31	31	INS	CLEAR OUT ENDMEM VALUE
0076	0872	31	31	INS	CLEAR OUT ENDME1 VALUE
0077	0873	2A 15	2A R@VC	BPL	GET14
0078	0875	81 41	81 D41	CMP A	#\$41 CHECK FOR UPPER CASE A TO Z
0079	0877	2D 11	2D R@VC	BLT	GET14
0080	0879	81 5A	81 D5A	CMP A	#\$5A
0081	087B	2E 03	2E R@VB	BGT	GET13
0082	087D	8B 20	8B D20	ADD A	#\$20 SHIFT UPPER CASE CHAR TO LOWER
0083	087F	39	39	RTS	
0084	0880	81 61	VB 81 D61	GET13 CMP A	#\$61 CHECK FOR LOWER CASE A TO Z
0085	0882	2D 06	2D R@VC	BLT	GET14
0086	0884	81 7A	81 D7A	CMP A	#\$7A
0087	0886	2E 02	2E R@VC	BGT	GET14
0088	0888	80 20	80 D20	SUB A	#\$20 SHIFT LOWER CASE CHAR TO UPPER
0089	088A	39	VC 39	GET14 RTS	
0090					
0091			END	END	

COLUMN 1 2 3 4 5 6 7
123456789012345678901234567890123456789012345678901234567890123456789012

0001				NAM	DUMBTER	
0002						
0003		=	4800	ORG	\$4800	
0004						
0005				TSMODE EQU	\$09	TERMINAL MODE--/16, 7 BIT, EVEN
0006		\$=	1C	CSRPTR EQU	\$1C	SCREEN CURSOR LOCATION
0007		C=	28	TEMP2C EQU	\$28	TWO-BYTE TEMP
0008		*=	38	ACIANO EQU	\$38	CASSETTE ACIA ADDRESS
0009		=	FC3D	CLEAR EQU	\$FC3D	CLEAR SCREEN
0010		I=	FC64	KBDPIA EQU	\$FC64	CONTAINS KBD PIA ADDRESS
0011		>=	FC8F	INSERT EQU	\$FC8F	EDIT A CHARACTER ON SCREEN
0012						
0013	4800	DE	38	GG DE D@*	INTLZX LDX	ACIANO GET TIMESHARING ACIA ADDRESS
0014	4802	86	13	86 D13	LDA A	#\$13 MASTER RESET ACIA
0015	4804	A7	00	A7 D00	STA A	0,X
0016	4806	86	09	86 D09	LDA A	#TSMODE SET ACIA--/16 7 BIT EVEN PAR.
0017	4808	A7	00	A7 D00	STA A	0,X
0018	480A	BD	FC3D	BD E@=	JSR	CLEAR CLEAR SCREEN
0019						
0020	480D	DE	1C	GH DE D@\$	BLINK LDX	CSRPTR BLINK SCREEN CURSOR
0021	480F	63	00	63 D00	COM	0,X SHIFT TO/FROM CURSOR BLOCK
0022	4811	CE	1800	CE E1800	LDX	#\$1800 LOAD BLINK COUNT
0023	4814	DF	28	DF D@C	STX	TEMP2C SAVE BLINK COUNT
0024	4816	DE	28	GI DE D@C	BLINK1 LDX	TEMP2C RESTORE BLINK COUNT
0025	4818	09		09	DEX	
0026	4819	27	F2	27 R@GH	BEQ	BLINK RESTART BLINK COUNTER
0027						
0028	481B	DF	28	GY DF D@C	ACIAIN STX	TEMP2C SAVE X REGISTER
0029	481D	86	01	86 D01	LDA A	#\$01
0030	481F	DE	38	DE D@*	LDX	ACIANO
0031	4821	A5	00	A5 D00	BIT A	0,X TEST RECEIVE REGISTER FULL
0032	4823	27	05	27 R@GZ	BEQ	KBDIN BRANCH IF NO ACIA INPUT
0033	4825	A6	01	A6 D01	LDA A	1,X GET INPUT CHAR
0034	4827	BD	FC8F	BD E@>	JSR	INSERT DISPLAY ACIA INPUT CHAR
0035						
0036	482A	FE	FC64	GZ FE E@I	KBDIN LDX	KBDPIA GET KEYBOARD PIA ADDR
0037	482D	86	40	86 D40	LDA A	#\$40 GET TEST MASK
0038	482F	A5	01	A5 D01	BIT A	1,X TEST FOR KEYBOARD CHAR
0039	4831	27	E3	27 R@GI	BEQ	BLINK1 LOOP IF NO KBD INPUT
0040	4833	DE	1C	DE D@\$	LDX	CSRPTR RESET BLINK CHAR
0041	4835	A6	00	A6 D00	LDA A	0,X
0042	4837	2A	02	2A R@HE	BPL	KBDIN1
0043	4839	63	00	63 D00	COM	0,X
0044	483B	FE	FC64	HE FE E@I	KBDIN1 LDX	KBDPIA GET KEYBOARD PIA ADDR
0045	483E	A6	00	A6 D00	LDA A	0,X GET KBD CHAR
0046	4840	27	0F	27 R@HH	BEQ	EXIT END IF 00 HEX
0047	4842	C6	02	HF C6 D02	ACOUT LDA B	#\$02
0048	4844	DE	38	DE D@*	LDX	ACIANO
0049	4846	E5	00	HG E5 D00	ACOT10 BIT B	0,X TEST SEND REGISTER FULL
0050	4848	27	FC	27 R@HG	BEQ	ACOT10 LOOP UNTIL EMPTY
0051	484A	A7	01	A7 D01	STA A	1,X SEND KBD CHAR
0052	484C	BD	FC8F	BD E@>	JSR	INSERT DISPLAY CHAR IN ASCII
0053	484F	20	BC	20 R@GH	BRA	BLINK CONTINUE MAIN LOOP
0054						
0055	4851	39		HH 39	EXIT	RTS
0056						
0057				END		END

PROGRAM CIRCLE ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA
0001				NAM CIRCLE
0002				*
0003				* CIRCLE--JANUARY 12, 1978 VERSION
0004				*
0005				* PROGRAMMED BY
0006				* JIM RAEHL, 943 BEGONIA, ESCONDIDO, CA 92027
0007				* (714) 746-3562 (714) 485-2580 (WORK)
0008				*
0009				* THIS PROGRAM IS TAKEN FROM AN ARTICLE ENTITLED
0010				* "SERENDIPITOUS CIRCLES" IN THE AUGUST 1977 ISSUE OF
0011				* BYTE MAGAZINE (P. 70). THE ORIGINAL PROGRAM USED A
0012				* DAC TO DISPLAY THE OUTPUT ON AN OSCILLOSCOPE. THIS
0013				* VERSION IS ADAPTED FOR THE SPHERE CRT BOARD.
0014				* INSTRUCTIONS ARE GIVEN IN BOXES IN THE PROGRAM TO
0015				* ADAPT IT TO A CRT8 OR GRAPHICS BOARD. THE ORIGINAL
0016				* PROGRAM WAS FOUND TO BE TOO DULL. I LIVENED IT UP
0017				* BY ALTERING THE 16-BIT X AND Y COORDINATE VALUES BY
0018				* A DETERMINED ALGORITHM--INCREMENT THE COORDINATE BY
0019				* A CONSTANT, AND THEN INCREMENT THE CONSTANT FOR MORE
0020				* VARIETY. I ALSO FOUND THAT PREVIOUS POINTS HAD TO BE
0021				* ERASED, OR THE SCREEN WOULD EVENTUALLY FILL UP.
0022				* THUS, ONLY THE 64 MOST RECENT POINTS ARE RETAINED.
0023				* IT WAS ALSO FOUND TO BE MORE INTERESTING IF THE RATE
0024				* OF DISPLAY WAS SLOWED DOWN.
0025				*
0026				
0027				*****
0028				*
0029				* CIRCLE DRAWING PROGRAM
0030				* WRITTEN BY WILLIAM F. GALWAY
0031				* 30 DEC 76
0032				* THE ALGORITHM USED IS AS FOLLOWS
0033				*
0034				* LOOP
0035				* X <- X - Y/2
0036				* Y <- Y + X/2
0037				* GOTO LOOP
0038				*
0039				*****
0040				*
0041				* SIXTEEN BIT ARITHMETIC IS USED ALTHOUGH ONLY
0042				* 5 BITS OF X AND 4 BITS OF Y ARE DISPLAYED.
0043				*****
0044				*
0045				* SOME GOOD STARTING VALUES FOR (X,Y) ARE
0046				* (7F00,0000)
0047				* (7F00,8100)
0048				* (7D00,7D00)
0049				* (7CF3,7CF3)
0050				*

PROGRAM CIRCLE ASSEMBLY LISTING

```

LINE  ADDR  OBJECT      SPHERE      MOTOROLA
0151
0152      * THE NEXT HIGHER POWER OF 2 TO GET THE SCREEN WIDTH.
0153      * MULTIPLY THE EXTRACTED RESULT BY THE NUMERATOR OF
0154      * THIS FRACTION. THE MULTIPLY IS DONE BY SHIFTING THE
0155      * EXTRACTED RESULT TO GET MULTIPLIES BY 2, AND ADDING
0156      * THE DESIRED PARTIAL PRODUCTS. THE RESULT OF THE
0157      * MULTIPLIES IS DIVIDED BY THE DENOMINATOR, WHICH MUST
0158      * BE A POWER OF 8. THE DIVIDE IS DONE BY RIGHT SHIFTING.
0159      *
0159      * DISPLAY ALGORITHM FOR CRT8
0160      *   POSITION = $E000 +
0161      *           ((TOP Y 5 BITS * 3 / 4 + 12) MOD 24)*80 +
0162      *           ((TOP X 7 BITS * 5 / 8 + 40) MOD 80)
0163      *
0164      *LOOP  LDA A  WK1      GET HI ORDER BYTE OF X
0165      *      ASR A              USE HIGH 7 BITS
0166      *      AND A  #$7F
0167      *      STA A  WK6      SAVE ORIGINAL EXTRACTED VALUE
0168      *      ASL A              MULTIPLY BY 4
0169      *      ROL A
0170      *      ADC B  #0        PUT OVERFLOW IN B
0171      *      ADD A  WK6      ADD ORIGINAL VALUE
0172      *      ADC B  #0        NOW FULLY MULTIPLIED BY 5
0173      *      ASR A              DIVIDE LOWER PART OF RESULT BY 8
0174      *      ASR A
0175      *      ASR A
0176      *      AND A  #$1F      GET RID OF SIGN PROPAGATION
0177      *      ASL B              SHIFT UPPER PART OF RESULT
0178      *      ASL B              TO ADD TO A
0179      *      ASL B
0180      *      ASL B
0181      *      ASL B
0182      *      ABA              ADD TOGETHER LOWER & UPPER PARTS
0183      *      ADD A  #40      **2—SHIFT ORIG TO 40TH LINE CHAR
0184      *      CMP A  #80      CHECK FOR OVERFLOW
0185      *      BLT  GLOOP      BRANCH IF NO OVERFLOW
0186      *      SUB A  #80      SHIFT OVERFLOW TO LINE FIRST HALF
0187      *
0188      *****
0189
0190      * DISPLAY ALGORITHM FOR CRT1
0191      *   POSITION = $E000 +
0192      *           ((TOP Y 4 BITS + HEX 8) MOD HEX 10)*32 +
0193      *           ((TOP X 5 BITS + HEX 10) MOD HEX 20)
0194
0195  0447  96 50      F 96 D@A      LOOP  LDA A  WK1      GET HI ORDER OF X
0196  0449  47        47        ASR A              USE HIGH 5 BITS
0197  044A  47        47        ASR A
0198  044B  47        47        ASR A
0199  044C  84 1F      84 D1F      AND A  #$1F
0200  044E  9B 64      9B D@R      ADD A  WK11      ADD HEX 10 TO TOP X 5 BITS

```


PROGRAM CIRCLE ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA	
0251	0458	D9 62	D9 D@Q	ADC B WK10	ADD HEX 8 TO TOP Y 4 BITS
0252	045A	C4 01	C4 D01	AND B #\$01	MOD HEX 10
0253	045C	84 E0	84 DE0	AND A #\$E0	
0254	045E	20 02	20 R@2	BRA ALOOP	
0255					
0256	0460	20 E5	1 20 R@F	BLOOP BRA LOOP	
0257					
0258	0462	FB FC38	2 FB EFC38	ALOOP ADD B \$FC38	ADD SCREEN BASE ADDRESS
0259	0465	9B 5A	9B D@I	ADD A WK6	ADD X VALUE
0260	0467	C9 00	C9 D00	ADC B #0	
0261	0469	DE 60	DE D@P	LDX WK9	GET 64TH PREVIOUS PT LOC
0262	046B	EE 00	EE D00	LDX 0,X	
0263	046D	37	37	PSH B	SAVE B
0264	046E	C6 20	C6 D20	LDA B #\$20	SPACE TO ERASE 64TH PREV LOC
0265	0470	E7 00	E7 D00	STA B 0,X	**5--CLEAR 64TH PREVIOUS POINT
0266	0472	33	33	PUL B	RESTORE B
0267	0473	DE 60	DE D@P	LDX WK9	
0268	0475	E7 00	E7 D00	STA B 0,X	SAVE CURRENT POINT LOCATION
0269	0477	A7 01	A7 D01	STA A 1,X	
0270	0479	EE 00	EE D00	LDX 0,X	PUT CURRENT LOC INTO X
0271	047B	86 6F	86 D6F	LDA A #\$6F	DISPLAY SMALL LETTER O
0272	047D	A7 00	A7 D00	STA A 0,X	DISPLAY THE POINT
0273	047F	DE 60	DE D@P	LDX WK9	
0274	0481	08	08	INX	NEXT PREVIOUS POINT TO CLEAR
0275	0482	08	08	INX	
0276	0483	9C 66	9C D@S	CPX WK12	WRAP AROUND TO BUFFER START
0277	0485	26 03	26 R@W	BNE FLOOP	IF AT END
0278	0487	CE 0070	CE E@T	LDX #PTBUF	BUFFER START LOC
0279	048A	DF 60	W DF D@P	FLOOP STX WK9	SAVE PTR TO BUFFER LOC
0280	048C	CE 0050	CE E@A	LDX #WK1	SET X TO POINT TO WORK AREA
0281					
0282					
0283					
0284	048F	E6 03	E6 D03	LDA B 3,X	B GETS LO Y
0285	0491	A6 02	A6 D02	LDA A 2,X	A GETS HI Y
0286	0493	47	47	ASR A	GET Y/2
0287	0494	56	56	ROR B	
0288	0495	40	40	NEG A	DO A 16 BIT NEGATE
0289	0496	50	50	NEG B	NEGATE LO ORDER
0290	0497	82 00	82 D00	SBC A #0	PROPAGATE CARRY
0291	0499	EB 01	EB D01	ADD B 1,X	GET X+(-Y/2) LO ORDER
0292	049B	A9 00	A9 D00	ADC A 0,X	THEN HI ORDER
0293	049D	E7 01	E7 D01	STA B 1,X	STORE LO X
0294	049F	A7 00	A7 D00	STA A 0,X	THEN HI X
0295	04A1	47	47	ASR A	GET X/2 HI ORDER
0296	04A2	56	56	ROR B	LO ORDER
0297	04A3	EB 03	EB D03	ADD B 3,X	ADD LO Y
0298	04A5	A9 02	A9 D02	ADC A 2,X	ADD HI Y WITH CARRY
0299	04A7	E7 03	E7 D03	STA B 3,X	SAVE LO Y
0300	04A9	D6 5E	D6 D@K	LDA B WK8	ADD Y BIAS TO AVOID FIXED PATT

* FIGURE NEXT POINT LOCATION

PROGRAM WORM ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA	
0101	E25D	09	09	DEX	
0102	E25E	5A	5A	DEC B	LOOP UNTIL LOWER PART MOVED
0103	E25F	26 F3	26 R@F	BNE OUTERL	
0104					
0105					* PRINT BOTTOM ADDRESS OF WORM
0106					
0107	E261	8D 02	8D R@J	BSR PRINT	PRINT ADDRESS ON SCREEN
0108	E263	20 25	20 R@I	BRA TOP	RELOCATE STACK
0109					
0110	E265	DF 00	J DF D00	PRINT STX \$00	SAVE ADDRESS TO PRINT
0111	E267	FE FC38	FE E@Y	LDX SCBEG	GET SCREEN ADDRESS
0112	E26A	96 00	96 D00	LDA A \$00	PRINT FIRST BYTE OF ADDRESS
0113	E26C	8D 02	8D R@K	BSR CNVT	
0114	E26E	96 01	96 D01	LDA A \$01	PRINT SECOND BYTE OF ADDRESS
0115	E270	16	K 16	CNVT TAB	SAVE BYTE TO PRINT
0116	E271	47	47	ASR A	MOVE LEFT DIGIT RIGHT
0117	E272	47	47	ASR A	
0118	E273	47	47	ASR A	
0119	E274	47	47	ASR A	
0120	E275	8D 01	8D R@L	BSR PNT	CONVERT LEFT DIGIT TO CHAR
0121	E277	17	17	TBA	CONVERT RIGHT DIGIT TO CHAR
0122	E278	84 0F	L 84 D0F	PNT AND A #\$0F	ISOLATE DIGIT TO PRINT
0123	E27A	8B 30	8B D30	ADD A #\$30	ADD CHAR BIAS
0124	E27C	81 3A	81 D3A	CMP A #\$3A	CHECK FOR A TO F
0125	E27E	2D 02	2D R@M	BLT PNT1	
0126	E280	8B 07	8B D07	ADD A #\$07	ADD A TO F EXTRA BIAS
0127	E282	A7 00	M A7 D00	PNT1 STA A 0,X	PRINT THE DIGIT
0128	E284	08	08	INX	NEXT PRINT POSITION
0129					
0130					
0131					* COVER TRACKS WITH SWI INSTRUCTIONS
0132	E285	86 3F	86 D3F	LDA A #\$3F	SOFTWARE INTERRUPT CODE
0133	E287	36	36	PSH A	
0134	E288	31	31	INS	RESTORE STACK POINTER
0135	E289	39	39	RTS	
0136					
0137					* PUT NEW TOP OF WORM ADDRESS IN STACK
0138					
0139	E28A	8D B2	I 8D R@B	TOP BSR BEGIN	NEW ADDRESS IN STACK
0140					
0141	E28C	39	X 39	WORME RTS	RETURN TO EXT MONITOR IF NOT WORM
0142					
0143			END	END	

COLUMN 1 2 3 4 5 6 7
 1234567890123456789012345678901234567890123456789012345678901234567890123456789012

PROGRAM CRTOUT ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA
0051	021E	36	SA 36	CRTOUT PSH A SAVE REGISTERS
0052	021F	37	37	PSH B
0053	0220	8D 6B	8D R@RB	BSR PSHX
0054	0222	DE 1C	DE D@C	LDX CSRPTR GET CURSOR ADDRESS
0055	0224	8D 07	8D R@SB	BSR CRT000 PRINT THE CHARACTER
0056	0226	DF 1C	DF D@C	STX CSRPTR SAVE NEW CURSOR ADDRESS
0057	0228	8D 77	8D R@RC	BSR PULX RESTORE REGISTERS
0058	022A	33	33	PUL B
0059	022B	32	32	PUL A
0060	022C	39	39	RTS
0061				*
0062				* (HT) HORIZONTAL TAB 8 SPACES
0063				*
0064	022D	81 09	SB 81 D09	CRT000 CMP A #\$09 CHECK FOR HORIZONTAL TAB
0065	022F	26 3E	26 R@TC	BNE CRT080
0066	0231	96 1D	96 D@D	LDA A CSRPT1 INCREMENT LINE POS TO MULT OF 8
0067	0233	8A 07	8A D07	ORA A #7
0068	0235	97 1D	97 D@D	STA A CSRPT1
0069	0237	96 60	96 D@N	LDA A LNCNTR INCREMENT CURSOR POS TO MULT OF 8
0070	0239	8A 07	8A D07	ORA A #7
0071	023B	97 60	97 D@N	STA A LNCNTR
0072	023D	DE 1C	DE D@C	LDX CSRPTR GET CURRENT CURSOR POSITION
0073	023F	D6 5C	D6 D@L	LDA B LINSIZ GET LINE LENGTH
0074	0241	5A	5A	DEC B LINE LENGTH - 1
0075	0242	11	11	CBA CHECK FOR END OF LINE
0076	0243	20 0E	20 R@SD	BRA CRT011 INCREMENT CURSOR POSITION
0077				
0078				
0079				*
0080				* NORMAL ASCII CHARACTER
0081				*
0082	0245	85 E0	SC 85 DE0	CRT010 BIT A #\$E0 TEST FOR CONTROL CHARACTER
0083	0247	27 19	27 R@TH	BEQ CRT110
0084	0249	A7 00	A7 D00	STA A 0,X STORE THE CHARACTER
0085	024B	08	08	INX NEXT CHARACTER POSITION
0086	024C	7C 0060	7C E@N	INC LNCNTR INCREMENT POSITION IN LINE
0087	024F	96 5C	96 D@L	LDA A LINSIZ CHECK FOR END OF LINE
0088	0251	91 60	91 D@N	CMP A LNCNTR
0089	0253	26 0C	SD 26 R@SE	CRT011 BNE CRT012
0090	0255	DF 1C	DF D@C	STX CSRPTR CURSOR IN SYNC W. TH LNCNTR
0091	0257	86 0D	TB 86 D0D	CRT015 LDA A #\$0D PRINT CARRIAGE RETURN
0092	0259	8D C3	8D R@SA	BSR CRTOUT
0093	025B	86 0A	86 D0A	LDA A #\$0A PRINT LINE FEED
0094	025D	8D BF	8D R@SA	BSR CRTOUT
0095	025F	DE 1C	DE D@C	LDX CSRPTR GET NEW CURSOR ADDRESS
0096	0261	39	SE 39	CRT012 RTS
0097				*
0098				* OTHER CONTROL CHARACTERS
0099				*
0100	0262	8A 40	TH 8A D40	CRT110 ORA A #\$40 ADD LETTERS BIAS TO CONTROL

PROGRAM CRTOUT ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA	
0151	02AA	31	31	INS	CLEAR X REG VALUE FROM STACK
0152	02AB	31	31	INS	
0153	02AC	36	UJ 36	PULX1 PSH A	STACK LOW RETURN ADDR BYTE
0154	02AD	96 86	96 D86	LDA A TEMPX2	STACK HIGH RETURN ADDR BYTE
0155	02AF	36	36	PSH A	
0156	02B0	96 66	96 D@Q	LDA A TEMPA	RESTORE A REGISTER
0157	02B2	39	39	RTS	
0158					
0159	02B3	20 90	UH 20 R@SC	CRT016 BRA CRT010	
0160					
0161				*	
0162				* (LF) LINE FEED	
0163				*	
0164	02B5	81 0A	SI 81 DOA	CRT030 CMP A #\$0A	CHECK FOR LINE FEED CHAR
0165	02B7	26 4C	26 R@SF	BNE CRT020	
0166	02B9	D6 60	D6 D@N	LDA B LNCNTR	GET POSITION IN LINE
0167	02BB	37	37	PSH B	SAVE POSITION IN LINE
0168	02BC	50	50	NEG B	
0169	02BD	DB 5C	DB D@L	ADD B LINSIZ	SUBT IT FROM LINE LENGTH
0170	02BF	08	SJ 08	CRT031 INX	INCREMENT TO END OF LINE
0171	02C0	5A	5A	DEC B	
0172	02C1	26 FC	26 R@SJ	BNE CRT031	
0173	02C3	9C 5A	9C D@K	CPX CRTEND	CHECK FOR SCREEN END
0174	02C5	26 25	26 R@SL	BNE CRT033	
0175	02C7	DE 58	DE D@J	LDX CRTBEG	
0176	02C9	7D 005E	7D E@M	TST SCRFLG	BRANCH IF WRAP AROUND
0177	02CC	27 1E	27 R@SL	BEQ CRT033	
0178				*	
0179				*	
0180	02CE	DF 84	TR DF D84	CRT32C STX TEMPX	SAVE CURRENT MOVE TO LOC
0181	02D0	D6 5C	D6 D@L	LDA B LINSIZ	GET LINE LENGTH
0182	02D2	4F	4F	CLR A	CLEAR UPPER LINE LENGTH BYTE
0183	02D3	DB 85	DB D85	ADD B TEMPX1	ADD LINE LENGTH TO MOVE LOC
0184	02D5	99 84	99 D84	ADC A TEMPX	
0185	02D7	97 86	97 D86	STA A TEMPX2	SAVE MOVE FROM LOC
0186	02D9	D7 87	D7 D87	STA B TEMPX3	
0187	02DB	DE 86	DE D86	LDX TEMPX2	GET MOVE FROM LOC
0188	02DD	9C 5A	9C D@K	CPX CRTEND	CHECK FOR LAST MOVE LOC
0189	02DF	27 09	27 R@SP	BEQ CRT32D	
0190	02E1	A6 00	A6 D00	LDA A 0,X	GET BYTE TO MOVE
0191	02E3	DE 84	DE D84	LDX TEMPX	RESTORE MOVE TO LOC
0192	02E5	A7 00	A7 D00	STA A 0,X	MOVE CHAR ONE LINE BACK
0193	02E7	08	08	INX	NEXT LOCATION TO MOVE
0194	02E8	20 E4	20 R@TR	BRA CRT32C	
0195	02EA	DE 84	SP DE D84	CRT32D LDX TEMPX	GET MOVE TO LOC
0196				*	
0197	02EC	DF 84	SL DF D84	CRT033 STX TEMPX	SAVE CURSOR LOCATION
0198	02EE	D6 5C	D6 D@L	LDA B LINSIZ	GET LINE LENGTH
0199	02F0	86 20	86 D20	LDA A #\$20	GET SPACE FOR BLANKING
0200	02F2	A7 00	SM A7 D00	CRT034 STA A 0,X	BLANK CURRENT SCREEN POSITION

COLUMN 1 2 3 4 5 6 7
123456789012345678901234567890123456789012345678901234567890123456789012

PROGRAM CRTOUT ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA	
0251	0335	DE 1C	DE D@C	LDX CSRPTR	GET CURSOR LOCATION
0252	0337	39	39	RTS	
0253				*	
0254				* (HOME) HOME CURSOR	
0255				*	
0256	0338	81 0C	TA 81 DOC	CRT061 CMP A #\$0C	CHECK FOR HOME CHAR
0257	033A	26 06	26 R@TE	BNE CRT100	
0258	033C	DE 58	DE D@J	LDX CRTBEG	GET SCREEN START LOCATION
0259	033E	7F 0060	7F E@N	CLR LNCNTR	POSITION COUNTER AT LINE START
0260	0341	39	39	RTS	
0261				*	
0262				* (DC1) UP ONE LINE	
0263				*	
0264	0342	81 11	TE 81 D11	CRT100 CMP A #\$11	CHECK FOR DC1 CHAR
0265	0344	26 0D	26 R@TI	BNE CRT120	
0266	0346	D6 5C	D6 D@L	LDA B LINSIZ	GET LINE LENGTH
0267	0348	9C 58	TF 9C D@J	CRT101 CPX CRTBEG	CHECK FOR SCREEN TOP
0268	034A	26 02	26 R@TG	BNE CRT102	
0269	034C	DE 5A	DE D@K	LDX CRTEND	CYCLE TO SCREEN BOTTOM, IF TOP
0270	034E	09	TG 09	CRT102 DEX	BACK ONE CHAR POSITION
0271	034F	5A	5A	DEC B	DECREMENT POSITION COUNTER
0272	0350	26 F6	26 R@TF	BNE CRT101	
0273	0352	39	39	RTS	
0274				*	
0275				* (RS) SET OPTION TO SCROLL	
0276				*	
0277	0353	81 1E	TI 81 D1E	CRT120 CMP A #\$1E	CHECK FOR RS CHARACTER
0278	0355	26 03	26 R@TI	BNE CRT130	
0279	0357	97 5E	97 D@M	STA A SCRLFG	
0280	0359	39	39	RTS	
0281				*	
0282				* (VS) SET OPTION TO WRAP AROUND	
0283				*	
0284	035A	81 1F	TJ 81 D1F	CRT130 CMP A #\$1F	CHECK FOR VS CHARACTER
0285	035C	26 04	26 R@TK	BNE CRT140	
0286	035E	7F 005E	7F E@M	CLR SCRLFG	CLEAR SCROLL FLAG
0287	0361	39	39	RTS	
0288				*	
0289				* (DC2) RIGHT ONE CHARACTER	
0290				*	
0291	0362	81 12	TK 81 D12	CRT140 CMP A #\$12	CHECK FOR DC2 CHARACTER
0292	0364	26 14	26 R@TN	BNE CRT045	
0293	0366	08	08	INX	INCREMENT CURSOR POSITION
0294	0367	7C 0060	7C E@N	INC LNCNTR	INCREMENT LINE POSITION
0295	036A	96 5C	96 D@L	LDA A LINSIZ	GET LINE LENGTH
0296	036C	91 60	91 D@N	CMP A LNCNTR	CHECK FOR LINE END
0297	036E	26 09	26 R@TL	BNE CRT141	
0298	0370	7F 0060	7F E@N	CLR LNCNTR	SET TO LINE POSITION 0 (START)
0299	0373	9C 5A	9C D@K	CPX CRTEND	CHECK FOR END OF SCREEN
0300	0375	26 02	26 R@TL	BNE CRT141	

COLUMN 1 2 3 4 5 6 7
12345678901234567890123456789012345678901234567890123456789012

PROGRAM CRTOUT ASSEMBLY LISTING

LINE	ADDR	OBJECT	SPHERE	MOTOROLA
0301	0377	DE 58	DE D@J	LDX CRTBEG CYCLE TO START, IF AT END
0302	0379	39	TL 39	CRT141 RTS
0303				*
0304				* (DEL) BACKSPACE AND DELETE (NORMALLY USES CRT040)
0305				* (BS) BACKSPACE AND DELETE
0306				*
0307	037A	81 7F	TN 81 D7F	CRT045 CMP A #\$7F TEST FOR DEL
0308				* USE FOLLOWING INSTRUCTION TO TREAT DEL AS REGULAR CHAR
0309	037C	27 A8	27 R@UC	BEQ CRT013
0310				* USE FOLLOWING INSTRUCTION TO TREAT DEL AS BACKSPACE
0311				* BEQ CRT040
0312	037E	81 08	81 D08	CMP A #\$08 TEST FOR BACKSPACE
0313	0380	26 07	26 R@SV	BNE CRT041
0314	0382	8D 09	SU 8D R@TM	CRT040 BSR CRT044 BACK UP ONE CHARACTER
0315	0384	86 20	86 D20	LDA A #\$20 BLANK OUT CURRENT CHARACTER
0316	0386	A7 00	A7 D00	STA A 0,X
0317	0388	39	39	RTS
0318				*
0319				* (DC4) BACK UP ONE CHARACTER
0320				*
0321	0389	81 14	SV 81 D14	CRT041 CMP A #\$14 CHECK FOR BACK ONE CHARACTER
0322	038B	26 99	26 R@UC	BNE CRT013
0323	038D	9C 58	TM 9C D@J	CRT044 CPX CRTBEG CHECK FOR START OF SCREEN
0324	038F	26 02	26 R@SW	BNE CRT042
0325	0391	DE 5A	DE D@K	LDX CRTEND USE END OF SCREEN IF AT START
0326	0393	96 60	SW 96 D@N	CRT042 LDA A LNCNTR CHECK FOR START OF LINE
0327	0395	26 04	26 R@SX	BNE CRT043
0328	0397	96 5C	96 D@L	LDA A LINSIZ RESTART AT END OF LINE
0329	0399	97 60	97 D@N	STA A LNCNTR
0330	039B	7A 0060	SX 7A E@N	CRT043 DEC LNCNTR DECREMENT POSITION ON LINE
0331	039E	09	09	DEX
0332	039F	39	PA 39	CRTEX RTS
0333				
0334			END	END

COLUMN 1 2 3 4 5 6 7
 12345678901234567890123456789012345678901234567890123456789012

SUBSET OF ASCII to PACKED BASE 40 and Back

Two complementary programs which follow are based on an algorithm which was written up in INTERFACE AGE magazine OCT. 1980, PP. 80-84 by David Veldof. The idea is to select a subset of Ascii code, in this case including capital letters, numbers zero thru nine, and four other characters (space, \$, period and minus sign). The Ascii, three bytes at a time, is packed into 16 bit words (see figure 1) giving a true 50% savings in storage space and possibly shortening I/O time especially if a slow peripheral device is used. I am currently using these routines to store 192 bytes of data in each disk sector which usually carries 128 bytes.

The most involved part of the programs is the handling of the Ascii in the event that the number of bytes is not exactly divisible by three. Also, the routines have been written to search for an end character (* which is Hex 2A) so as to allow any length Ascii file to be handled.

When less than three bytes remain to be converted, the one or two are just converted to base.40 but passed thru unpacked. Also, the first byte, if there are two left over, is complemented. These changes of format allow the unpacking program to know that the last few bytes before the end character must be unpacked differently. The complement was done so that no combination of two base 40 bytes could exist with the same value as some packed 16 bit combination.

There are many possible changes which can customize these routines. One could easily substitute characters for the four miscellaneous ones. The dollar sign can usually be part of the application program instead of being stored in the data file. The comma might thus be substituted for the \$. Of course, the choice of end character is up to the user; just let the program take this from ram instead of loading it immediate. Each application could specify the end character in that way. Fig. 4 shows an alternate scheme of allocating the base 40 character set but this "CAN CODE" only gets 39 characters instead of 40 because it uses zero differently. My version, by using zero for a space, makes some use of the 40th position.

The Base 40 to Ascii program calls the DIVIDE routine which sits in the V3N and most other proms which our users have. If it is no longer available to you in prom, just tack it at the end of the 16 bits to Ascii module.

Now to try the programs out:

Set up any areas for buffer 1 and 2 when you type in the programs.

```
A- place into buffer 2  00   temp
                       53   S
                       50   P
+ load                  48   H
                       45   E
  Ascii To              52   R
  BASE 40 at 200       45   E
                       2A   end of file
```

B-do 0200 control J

C-find the packed code in buffer 1 : 79 48 22 15 2A

- D- leave the packed code (or save it to tape or disk for later retrieval)
- E- load the packed base 40 to Ascii program
- F- do 200 control J NOTE THAT EITHER PROGRAM MAY BE LOADED ANYWHERE
IN RAM OR ROM BECAUSE RELATIVE ADDRESSING IS USED.
- G_ You should find the original Ascii code back in buffer 2.

Special note: It should be possible to pass a larger number of characters than the 40 if this is needed. Only 40 different ones will be packed but some infrequently used but very necessary characters could be encoded and passed thru imbedded in the packed code. The unpacking program would have to be similarly modified to test for these characters. It should be possible, but probably not really necessary, to have an extended version of these routines which would handle the entire Ascii character set but only pack the forty most commonly used characters. This would slightly reduce the density of the packed code while removing the limitations.

Please let me know if you find these routines useful.

Jeff

PACKING ALGORITHM

BASE 40 GETS 40

The following section summarizes the steps necessary to pack Base 40 characters three to a word.

1. Take the Base 40 character H and shift it three places to the left (multiply it by 8) and save this partial result.
2. Shift H two more places to the left (multiply it by 32) and add the saved partial result (equivalent to $H \cdot 40$). Save this as the sum.
3. Take M and add it to the sum (from step 2). Shift this quantity over three places to the left (multiply by 8) and save the partial result. Shift the quantity two more places to the left (multiply by 32) and add the partial result to it ($M \cdot 40$). Save this in sum.
4. Take the sum and add L to it. This gives you three packed Base 40 characters in one word.
5. Repeat the whole procedure from step 1 for the next group of three Base 40 characters.

Base 40 Character Set

Packed Character	Base 40 Equivalent
Space	0
A-Z	1 - 26
.	27
-	28
0-9	29
	30 - 39

Figure 1. Characters normally represented in Base 40.

Fig. 1

Fig-3

UNPACKING ALGORITHM

To summarize the steps necessary to unpack Base 40 characters:

1. Divide the packed characters (HML) by 40^2 . The quotient will be the unpacked high order.
2. Divide the remainder (from step 1) by 40. The quotient will be the unpacked middle character and the remainder will be the unpacked lower-order character.

We have now shown how to pack and unpack Ascii characters, assuming they are already expressed in their Base 40 equivalents. But how do we get them in their Base 40 equivalents?

Fig-2

can code conversion

HEX CAN	HEX CAN	HEX CAN
0	0	0
640 A	28 A	1 A
C80 B	50 B	2 B
1200 C	78 C	3 C
1900 D	A0 D	4 D
1740 E	C8 E	5 E
2580 F	F0 F	6 F
2420 G	118 G	7 G
2800 H	140 H	8 H
3840 I	168 I	9 I
3880 J	190 J	A J
4400 K	188 K	B K
4800 L	180 L	C L
5140 M	208 M	D M
5780 N	230 N	E N
5800 O	258 O	F O
6400 P	280 P	10 P
6A40 Q	2A8 Q	11 Q
7080 R	2D0 R	12 R
7600 S	2F8 S	13 S
7800 T	320 T	14 T
8340 U	348 U	15 U
8980 V	370 V	16 V
8F00 W	398 W	17 W
9600 X	3C0 X	18 X
9C40 Y	3E8 Y	19 Y
A280 Z	410 Z	1A Z
ABC0 0	438 0	1B 0
AF00 1	460 1	1C 1
B440 2	488 2	1D 2
B880 3	480 3	1E 3
C1C0 4	4D8 4	1F 4
C800 5	500 5	20 5
CB40 6	528 6	21 6
DA80 7	550 7	22 7
DAC0 8	578 8	23 8
E100 9	5A0 9	24 9
E740 :	5C8 :	25 :
ED80 .	5F0 .	26 .
F3C0 \$	618 \$	27 \$

NOTE
That
can
code
version
gets
only
34
USASCII
characters

Fig. 4

16 Bits PACKED ³⁴ BASE 40 TO Ascii

```

0200 DE LDX #5000
0203 DF STX 52
0205 DE LDX #2000
0208 DF STX 50
020A DE LDX 50
020C C6 LDAB#2A * Eof
020E A6 LDAAX00
0210 11 CBA
0211 26 BNE 05 0218
0213 DE LDX 52
0215 E7 STABX00
0217 39 RTS
0218 A6 LDAAX01
021A 11 CBA
021B 26 BNE 06 0228
021D A6 LDAAX00
021F 8D BSR 50 0281
0221 DE LDX 52
0223 A7 STAAAX00
0225 E7 STABX01
0227 39 RTS
0228 A6 LDAAX02
022A 11 CBA
022B 26 BNE 1C 0249
022D A6 LDAAX00
022F 81 CMPA#FA
0231 23 BLS 16 0249
0233 A6 LDAAX00
0235 43 COMA
0236 8B BSR 49 0281
0238 DE LDX 52
023A A7 STAAAX00
023C DE LDX 50
023E A6 LDAAX01
0240 8D BSR 3F 0281
0242 DE LDX 52
0244 A7 STAAAX01
0246 E7 STABX02
0248 39 RTS
0249 86 LDAA#06
024B 97 STAA 06
024D 86 LDAA#40
024F 97 STAA 07
0251 E6 LDABX00
0253 A6 LDAAX01
0255 08 INX
0256 08 INX
0257 0F STX 50
0259 8D BSR 59 0284
025B 8B BSR 24 0281
025D DE LDX 52
025F A7 STAAAX00
0261 96 LDAA 07
0263 C6 LDAB#2B
0265 D7 STAB 07
0267 D6 LDAB 06
0269 7F CLR 0006
026C 8B BSR 46 0284
026E 8B BSR 11 0281
0270 DE LDX 52
0272 A7 STAAAX01
0274 96 LDAA 07
0276 8D BSR 09 0281
0278 A7 STAAAX02
027A 08 INX
027C 08 INX
027E 08 INX
027F DF STX 52
0281 20 BKA 59

```

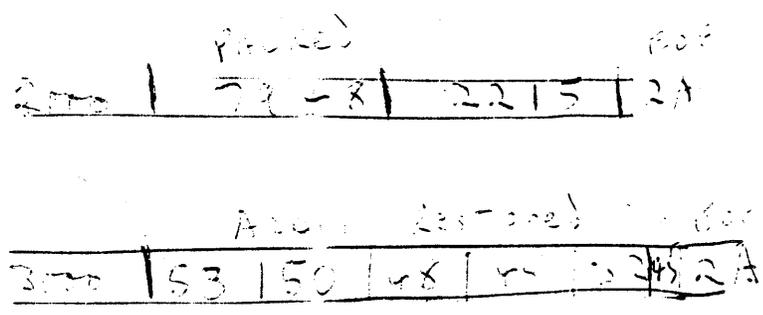
Setup
 0200-0203
 0205-0208
 020A-020C
 020E-0210
 0211-0213
 0215-0217
 0218-021A
 021B-021D
 021F-0221
 0223-0225
 0227-0228
 022A-022B
 022D-022F
 0231-0233
 0235-0236
 0238-023A
 023C-023E
 0240-0242
 0244-0246
 0248-0249
 024B-024D
 024F-0251
 0253-0255
 0256-0257
 0259-025B
 025D-025F
 0261-0263
 0265-0267
 0269-026C
 026E-0270
 0272-0274
 0276-0278
 027A-027C
 027E-027F

```

0281 81 CMPA#27
0283 2E BGT 28 02B0
0285 4D TSTA
0286 26 BNE 04 028C
0288 86 LDAA#20
028A 20 BRA 27 02B3
028C 81 CMPA#1B
028E 26 BNE 04 0294
0290 86 LDAA#24
0292 20 BRA 1F 02B3
0294 81 CMPA#1C
0296 26 BNE 04 029C
0298 86 LDAA#2E
029A 20 BRA 17 02B3
029C 81 CMPA#1D
029E 26 BNE 04 02A4
02A0 86 LDAA#2D
02A2 20 BRA 0F 02B3
02A4 81 CMPA#1E
02A6 2E BGT 04 02AC
02A8 8B ADDA#40
02AA 20 BRA 07 02B3
02AC 8B ADDA#12
02AE 20 BRA 03 02B3
02B0 7E JMP FF04
02B3 39 RTS
02B4 7E JMP FF0F

```

Access
 Divide
 routine
 in program



020A 0000

3 Bytes Ascii To 16 Bits BASE 40

35

```

0200 DE LDX #2000
0205 BF STX 50
0205 DE LDX #2FFF
0208 DE STX 52
020A A6 LDAAX01
020C B1 CMPA#2A * 0215
020E 26 BNE 05
0210 DE LDX 50
0212 A7 STAAAX00
0214 39 RTS
0215 B8 BSR 50 026F
0217 A7 STAAAX01
0219 A6 LDAAX02
021B B1 CMPA#2A * 0223
021D 26 BNE 07
021F E6 LDABX01
0221 DE LDX 50
0223 E7 STABX00
0225 A7 STAAAX01
0227 39 RTS
0229 B8 BSR 45 026F
022A A7 STAAAX02
022C A6 LDAAX03
022E B1 CMPA#2A * 0242
0230 26 BNE 10
0232 E6 LDABX01
0234 A6 LDAAX02
0236 DE LDX 50
0238 53 CBMB
0239 E7 STABX00
023B A7 STAAAX01
023D B6 LDAAX#2A * 0242
023F A7 STAAAX02
0241 39 RTS
0242 B8 BSR 20 026F
0244 A7 STAAAX03
0246 B8 BSR 5A 02A2
0248 A6 LDAAX01
024A 5F CLR B
024B AB ADDAX02
024D E9 ABCBX00
024F E7 STABX00
0251 A7 STAAAX01
0253 B8 BSR 40 02A2
0255 A6 LDAAX01
0257 5F CLR B
0258 AD ADDAX03
025A E9 ABCBX00
025C DE LDX 50
025E E7 STABX00
0260 A7 STAAAX01
0262 09 INX
0263 08 INX
0264 0F STX 50
0266 B2 LDX 52
0268 8F CLR X03
026A 08 INX
026B 08 INX
026C 08 INX
026D 20 DRA 99 020B

```

0215
026F
0223
0242
026F
02A2

```

026F B1 CMPA#20
0271 26 BNE 01 0274
0273 4F CLRA
0274 B1 CMPA#24 *
0276 26 BNE 02 027A
0278 B6 LDAAX#13
027A B1 CMPA#2E *
027C 26 BNE 02 0280
027E B6 LDAAX#1C
0280 B1 CMPA#2D -
0282 26 BNE 02 0286
0284 B6 LDAAX#1D
0286 B1 CMPA#40 @
0288 2F BLE 00 0292
028A B1 CMPA#5A Z
028C 2E BGT 04 0292
028E B0 SUBA#40 @
0290 20 DRA 0F 02A1
0292 B1 CMPA#2F /
0294 2F BLE 03 029E
0296 B1 CMPA#39 9
0298 2E BGT 04 029E
029A B0 SUBA#12
029C 20 DRA 03 02A1
029E 7E JMP FE64 * to 029E-10
02A1 39 RTS illegal character

```

```

02A2 B8 BSR 10 02C1
02A4 B8 BSR 10 02C1
02A6 B8 BSR 17 02C1
02A8 A6 LDAAX00
02AA 97 STAA 06
02AC A6 LDAAX01
02AE 97 STAA 07
02B0 B8 BSR 0F 02C1
02B2 B8 BSR 0D 02C1
02B4 A6 LDAAX01
02B6 E6 LDABX00
02B8 7B ABDA 07
02BA B7 ABCB 06
02BC A7 STAAAX01
02BE E7 STABX00
02C0 39 RTS
02C1 68 ASL X01
02C3 A6 LDAAX00
02C5 A2 ABCAX00
02C7 A7 STAAAX00
02C9 39 *** RTS

```

20	53	57	43	45	52	45	100
3000	7448	2215	RA				

Simple circuit and software replace PROM programmer for 6800-based systems

In the development of software for microprocessor-based systems; debugged software must often be transferred to PROM for later use in the system. It is preferable to write in the system's PROM directly from the system's RAM, instead of copying down the contents of the RAM and then writing them into an external PROM with a PROM programmer. The advantages of direct transfer are realized easily with just two transistors, a flip-flop and a few resistors, which connect a 2708/2704 PROM to the peripheral interface adapter (PIA) used in systems based on the 6800. The required programming can reside in the system monitor or in any other areas designated by the user.

The resident software (see listing) presents the address, data bits and the program pulse to the PROM through a 6820 PIA. Programming waveforms are created exactly as recommended by the PROM manufacturer. After the address and data are set up, one program pulse per address is applied to the PROM's program input (pin 18). One scan through all addresses constitutes a program loop. One hundred program loops are required as per the manufacturer's data sheet.

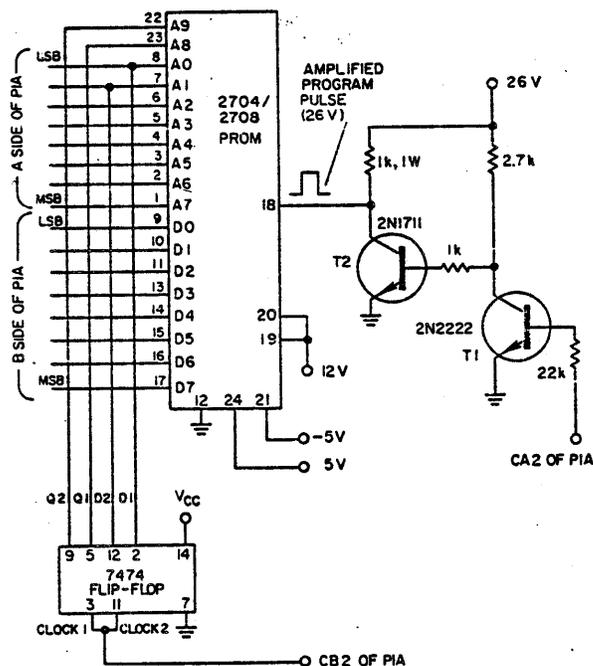
Before executing the program, the user must supply the starting address of the data source (RAM) and the starting and ending address where data are to be written (PROM), and must account for the data invert/normal option. The program terminates with an RTS instruction, which returns control to the monitor.

Transistors T_1 and T_2 (see schematic) amplify the program pulse transmitted by the 6800 to a 26-V level for the 2708/2704 PROM. The 7474 flip-flop expands the word length of port A and provides ten address bits simultaneously to the PROM. Data bits are presented to the PROM through Port B of the PIA. CA_2 and CB_2 of the PIA are defined as outputs: CA_2 supplies the program pulse, and CB_2 provides the flip-flop clock pulse.

The cost for all the additional hardware is about \$3—a negligible amount when compared to the cost of a microprocessor development system. The circuit and software have been tested only with a 6800

microprocessor system and a 2708/2704 PROM. However, any PROM should be programmable using this technique, if appropriate changes are made in the hardware and software.

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With only a few components, the 2704/2708 PROM connects to a 6800-system's peripheral interface adapter (PIA) for direct software transfer. The "A side" of the PIA (and the flip-flop) outputs address bits; the "B side" outputs data.

```

0001          * PIA INITIALISATION *
0002
0003      1000 4F          CLR A          :DEFINE A AND B SIDE OF PIA AS OUTPUT
0004      1001 97 C0      STA A          :CONTPL PORT A SIDE=00C0
0005      1003 86 FF      LDA A          :CONTPL PORT P SIDE=00C1
0006      1005 97 80      STA A          :OUTPUT PORT A SIDE=00F0
0007      1007 86 04      LDA A          :OUTPUT PORT E SIDE=0081
0008      1009 97 C0      STA A
0009      100F 4F          CLR A
0010      100C 97 C1      STA A
0011      100E 86 FF      LDA A
0012      1010 97 81      STA A
0013      1012 86 04      LDA A
0014      1014 97 C1      STA A
0015
0016          * MAIN *
0017      1016 5F          CLR B          :LCOF COUNTER INITIALISE
0018      1017 DE 00      LCOF2      LDX          :RAM START ADDR.AT 0000/0001
0019      1019 DF 07      STX          :PRESENT RAM ADDR.STORED
0020      101B DE 02      LDX          :PRCM START ADDR.AT 0002/0003
0021      101D DF 09      STX          :PRCM PRESENT ADDR.STORED
0022      101F 96 09      LCOF1      LDA A          :OUTPUT HIGH BYTE ADDR.CF FROM
0023      1021 97 80      STA A
0024      1023 86 3C      LDA A
0025      1025 97 C1      STA A          :CP2 PULSE GOES HIGH
0026      1027 8D 35      BSR          :250 MICROSECCND DELAY SUBROUTINE
0027      1029 86 34      LDA A          :CP2 PULSE GOES LOW
0028      102E 97 C1      STA A
0029      102D 96 0A      LDA A          :OUTPUT LOW BYTE ADDR.OF PRCM
0030      102F 97 80      STA A
0031      1031 DE 07      LDX          :RAM START ADDR.
0032      1033 A6 00      LDA A
0033      1035 7D 0006    TST          :TEST ADDR.0006 FOR DATA-NORMAL/INVERT
0034      1038 27 01      BFC          NORM      :DATA NCRMAL
0035      103A 43          COM A          :DATA INVERT
0036      103E 97 81      NCRM      STA A
0037      103D 8D 1F      BSR          :250 MICROSECCND DELAY SUBROUTINE
0038      103F 86 3C      LDA A          :CA2 PULSE GOES HIGH
0039      1041 97 C0      STA A
0040      1043 8D 26      BSR          :1MILLISECOND DELAY SUBROUTINE
0041      1045 86 34      LDA A          :CA2 PULSE GOES LOW
0042      1047 97 C0      STA A
0043      1049 8D 13      BSR          :250 MICROSECCND DELAY SUBROUTINE
0044      104B 08          INX          :INCREMENT RAM ADDR.
0045      104C DF 07      STX
0046      104E DE 09      LDX
0047      1050 08          INX          :INCREMENT RCM ADDR.
0048      1051 DF 09      STX
0049      1053 09          DEX
0050      1054 9C 04      CPX          :CHECK FOR PROM ADDR.AT 0004/0005
0051      1056 26 C7      BNE          LCOF1      :CHECK FOR LCOF END
0052      1058 5C          INC B          :INCREMENT LCOF COUNTER
0053      1059 C1 64      CMP B          :CHECK FOR 100 LCOFS
0054      105B 26 BA      PNE          LCOF2
0055      105D 39          RTS
0056
0057          *250 MICROSECCND DELAY SUBROUTINE*
0058      105E 7F 000B    CLR          :INITIALISE COUNTER FOR DELAY
0059      1061 7C 000B    LCOF3      INC
0060      1064 96 0E      LEA A
0061      1066 81 0F      CMP A
0062      1068 26 F7      BNE          LCOF3
0063      106A 39          RTS
0064
0065          *1 MILLISECOND DELAY SUBROUTINE*
0066      106B 7F 000B    CLR          :INITIALISECOUNTER FOR DELAY
0067      106E 7C 000E    LCOF4      INC
0068      1071 96 0E      LDA A
0069      1073 81 40      CMP A
0070      1075 26 F7      BNE          LCOF4
0071      1077 39          RTS

```

The programming required for direct transfer of debugged software from RAM to PROM can reside

in the system monitor or in any other areas designated by the user.

Adapting the M6800 processor for automatic telephone dialing

by Moshe Bram

Allied Chemical Corp., Automotive Products Division, Mount Clemens, Mich.

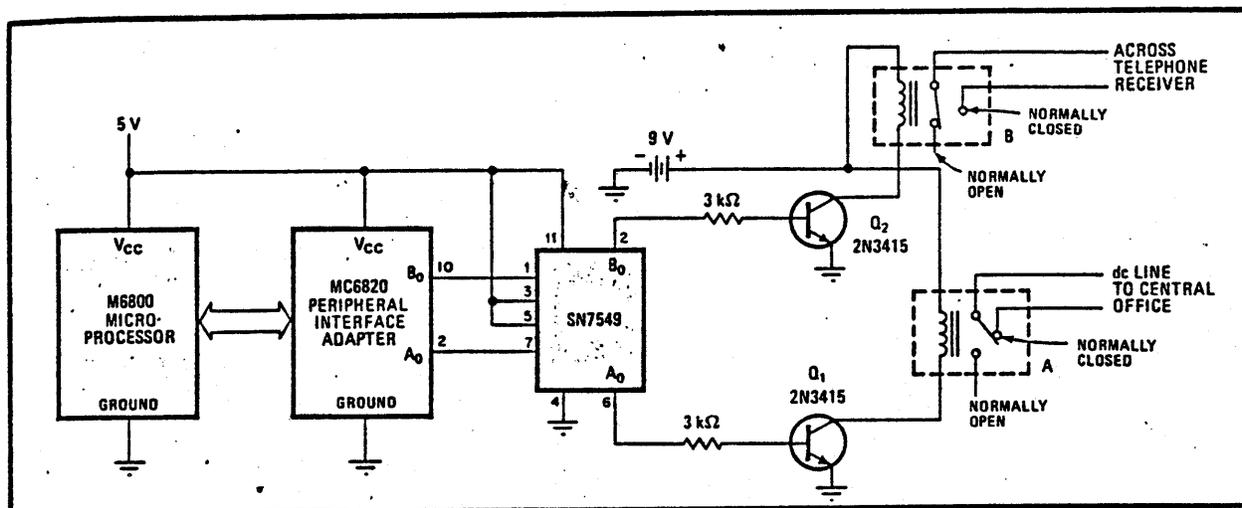
A short program and a simple interface for a rotary-dial telephone enables the well-known M6800 microprocessor to dial stored telephone numbers on command. The versatile microprocessor thus becomes a viable alterna-

tive to commercial automatic dialers, which essentially perform only one function and are expensive—chiefly because they are in great demand.

The program for the M6800 is divided into two sections, as shown in the table. The phone numbers are stored in the lower locations of memory, the dialing subroutine in the upper sections. The only limit to the number of phone numbers that can be stored is the amount of memory available to the system. The operation of the entire program is explained by the comments column of the table.

To access any number, the user (or a subroutine) simply initiates the program at, or routes the program to,

M6800 PROGRAM FOR AUTOMATIC DIALING			
Location	Object code	Source statement	Comments
0000	C6 X1	LDA B X1	Load accumulator B with the first digit of phone number (X ₁)
0002	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
0005	C6 X2	LDA B X2	Load accumulator B with the second digit X ₂
0007	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
000A	C6 X3	LDA B X3	Load accumulator B with the third digit X ₃
000C	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
000F	C6 X4	LDA B X4	Load accumulator B with the fourth digit X ₄
0011	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
0014	C6 X5	LDA B X5	Load accumulator B with the fifth digit X ₅
0016	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
0019	C6 X6	LDA B X6	Load accumulator B with the sixth digit X ₆
001B	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
001E	C6 X7	LDA B X7	Load accumulator B with the seventh digit X ₇
0020	BD 01C8	JSR 01C8	Jump to dial subroutine located at address 01C8
0023	3F	SWI	End of dialed number
	.	.	} Other numbers stored as required
	.	.	
01C8	86 FF	LDA A FF	Initial clearing of data direction and control registers of the PIA.
01CA	B7 8004	STA A 8004	
01CD	B7 8005	STA A 8005	
01D0	B7 8006	STA A 8006	
01D3	B7 8007	STA A 8007	
01D6	86 01	LDA A 01	
01D8	B7 8006	STA A 8006	
01DB	B7 8004	STA A 8004	A "HIGH" (1) is loaded into A ₀ & B ₀ of PIA
01DE	CE 18FF	LDX 09FF	
01E1	09	DEX	A counter is set allowing A ₀ & B ₀ to be high (1) during the count down.
01E2	26 FD	BNE FD	
01E4	4F	CLR A	Data line A ₀ goes low (0).
01E5	B7 8004	STA A 8004	
01E8	CE 18FF	LDX 09FF	A counter is set allowing A ₀ to be low (0) during the count down.
01EA	09	DEX	
01EC	26 FD	BNE FD	One cycle of pulse generation has been completed.
01EE	5A	DEC B	
01EF	26 E5	BNE E5	A branch instruction to generate the next pulse cycle is executed. Line B ₀ goes low (0) at the end.
01F1	B7 8006	STA A 8006	
01F4	C6 02	LDA B 02	A counter is set allowing a time interval between dialed digits.
01F6	CE FFFF	LDX FFFF	
01F9	09	DEX	A return from subroutine instruction is executed to load the next digit for dialing.
01FA	26 FD	BNE FD	
01FC	5A	DEC B	
01FD	26 F7	BNE F7	
01FF	39	RTS	



Command performance. Small program (see table) and simple interface adapt M6800 for automatic number dialing. PIA's output pulses are sent via relay A to central office, while telephone receiver is disabled by relay B to minimize annoying clicking sound in headset.

the location corresponding to the first digit of the number desired. For the sake of efficiency, program command time should be negligible with respect to the actual dialing time. Consequently, the command procedure should keep user interaction to a minimum—that is, it should be unnecessary to depress more than one key of an m-n matrix for each number desired.

Emanating from the 6820 peripheral interface adapter are seven groups of pulses corresponding to the number dialed (this may be extended to 10 groups or more if dialing into other area codes is contemplated). The program ensures that there is a suitable gap between each group of pulses so that the central office can differentiate between pulses belonging to separate digits.

The dial interface is a simple circuit connected between the PIA lines and the central office. It is

designed to open the normally closed dc line relay A for each output pulse from the PIA, thus transmitting the digit data to the office. The 7549 serves as a latch and buffer to transfer the PIA's dial-pulse information to switching transistor Q_1 , which has actual control of the relay. The output of port B_0 of the 7549 is high during the time the pulses are sent, and relay B is therefore closed in order to disable the headset receiver, minimizing the annoying clicking sounds that are heard in the receiver during dial-out.

The user is cautioned against connecting active-element relays, such as transistors, directly to the line. More likely than not, such an arrangement will require a small amount of power from the dc line to energize the active device, and even a load of only 2 milliamperes will be sufficient to cause trouble at the central office. □

Routine reverses data-storage order

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Computations such as digital convolutions, FFTs and DFTs require reversal of the order of the stored data when performed off line. Typically, you write the data out into a second memory block, but this approach requires enough extra memory to store the data twice—not a desirable situation in a μC system.

Another approach to the problem involves exchanging the data bytes between the first and last memory locations, then between the second and next-to-last, and so on, as in the accompanying code. Thus, if there are $k+1$ data bytes in the memory block, complete reversal requires $k/2$ (if $k+1$ is odd) or $(k+1)/2$ (if $k+1$ is even) exchanges.

Let the first memory location be m and the last

$m+k$. Note that there are $k+1$ memory locations in the block, containing $k+1$ data bytes. **EDN**

ENTER: LXI $\#m$	Index Register loaded with first address
LSP $\#m+k-1$	SP loaded with last-but-one address
LOADA: LDAA X	Data loaded into Acc A from the address pointed to by X
PULB	SP incremented by 1; B loaded from the memory location pointed to by this value of SP
STAB X	Exchange of data bytes takes place, and SP decremented by 1
PSHA	
INX	To get the next address from the top
DES	To get the next address from the bottom
CPX $\#n$	Compare X with n, where $n = m + \frac{k+1}{2}$ if $k+1$ is even, and $n = m + k/2$ if $k+1$ is odd
BNE LOADA	Repeat the exchange operations until all data bytes used, then
RTS	Return to main program

Save memory while reversing blocks of stored data by using this M6800 subroutine.

Multiplexed-memory technique doubles μP 's addressing capacity

Memory-map switching extends an 8-bit μP 's storage access to 128k—increasing application possibilities without sacrificing processing efficiency or capabilities.

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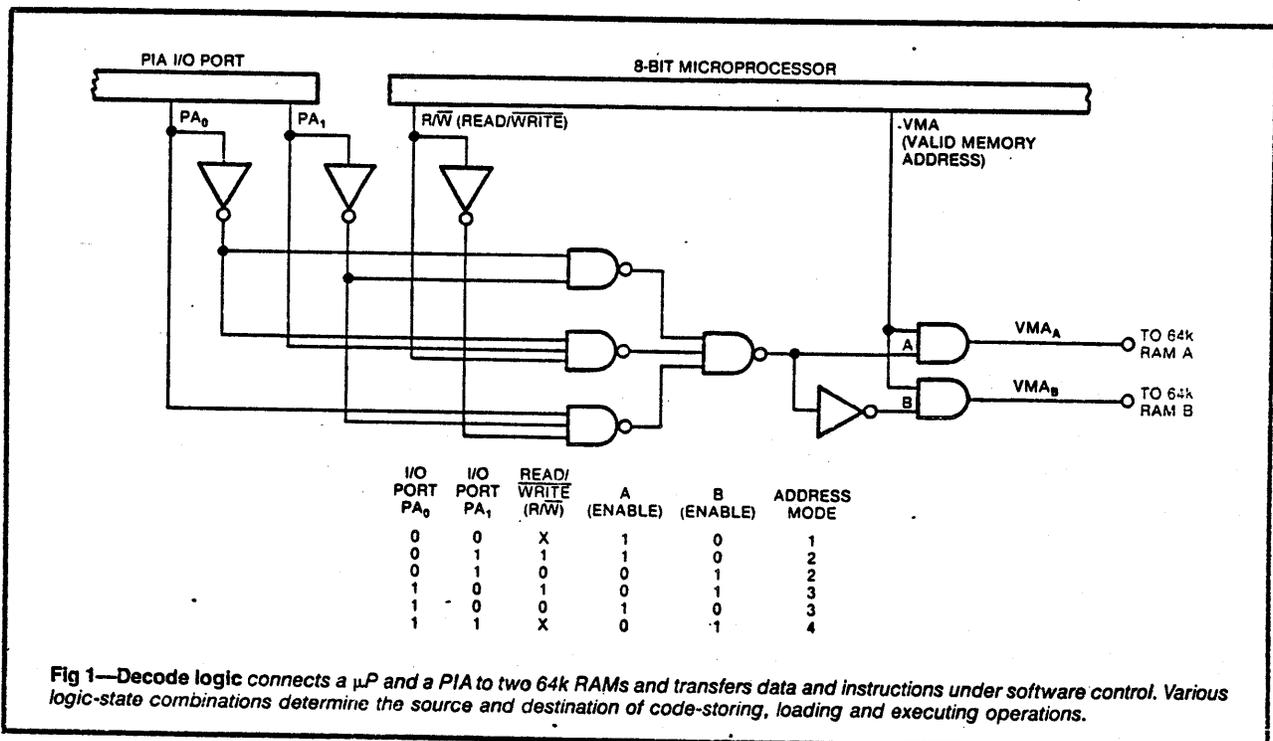
When an 8-bit μP 's 64k-byte memory-addressing capability begins to cramp your programming prospects, don't assume that you must necessarily upgrade to a 16-bit device. The software-directed dual memory-mapping approach described here allows you to expand an 8-bit μP 's addressing range to 128k bytes by multiplexing two 64k RAMs. This unified hardware/software approach lets you incorporate more processing functions and support more complex and efficient functions in an 8-bit system.

The dual-RAM mapping approach suits both long programs and short ones that need excessive buffer space during execution—two conditions that often occur in applications such as word processors, text editors and RAM/ROM testers. With enlarged memory, you can also overcome the size constraints of a

combined operating-system, I/O and control program. In fact, you can assign an entire 64k map to the operating system and control program and reserve the second map for the program buffer. This broad storage allocation permits you to add numerous program features without infringing on buffer space.

Simple concept demands design care

To implement the dual-memory-map approach, merely multiplex an 8-bit μP to two identical 64k RAMs. This seemingly elementary method requires careful consideration of several hardware/software design factors, however. At any instant, for example, the μP can access only one RAM; the entire workspace thus splits into two independent 64k blocks (memory maps). For proper hardware operation, the μP must retain each memory map's identity and correctly transfer control and data between maps. Software must



Dual mapping overcomes 8-bit μ P's memory limit

41

govern these map transfers and allow the μ P to access memory without loss of processing efficiency.

To satisfy these hardware/software design constraints, memory-map multiplexing calls for software-driven decode logic connected between the μ P's I/O port and two 64k RAMs (Fig 1). Although this particular hardware configuration relies on a 6800 μ P and a 6820 peripheral interface adapter (see box, "6800- μ P definitions"), the memory-map switching principles involved apply to most 8-bit μ P's with little modification.

In Fig 1, note that the μ P's Valid Memory Address (VMA) output, in conjunction with the decode logic, produces RAM-selector signals VMA_A and VMA_B . When VMA_A goes HIGH, the decode logic switches RAM A to the μ P; similarly, when VMA_B goes HIGH, RAM B comes under μ P control.

By storing data via a properly designated I/O port, the μ P selects one of four addressing modes:

- Mode 1—Load, execute and store code in RAM A
- Mode 2—Load and execute code from RAM A and store in RAM B
- Mode 3—Load and execute code from RAM B and store in RAM A
- Mode 4—Load, execute and store code in RAM B.

While Modes 1 and 4 concentrate on an individual RAM, Modes 2 and 3 direct the μ P to load programs from one memory map to the other as well as pass

6800- μ P definitions

Address bus (A_0 to A_{15})—Accesses memory and peripheral devices for μ P; a 16-bit, 3-state bus.

Data bus (D_0 to D_7)—Allows data to pass between memories and μ P's programmable registers; an 8-bit, 3-state, bidirectional bus.

Read/Write (R/W)—3-state output-control signal. When HIGH, it indicates that the CPU is reading PIA data from the data bus. When LOW, it indicates that the CPU is writing data onto the data bus for delivery to the PIA. Normal standby state is HIGH.

Valid Memory Address (VMA)—CPU output-control signal; goes HIGH whenever a valid address appears on the address bus. When either A or B enable or decode logic also goes HIGH, RAM A or RAM B switches into operation under μ P control.

6820 peripheral interface adapter (PIA)—Provides 16 pins configured as two 8-bit I/O ports (PA_0 to PA_7 and PB_0 to PB_7). Each I/O-port line operates as either input or output but does not support bidirectional data transfers. The PIA's 3-state, bidirectional data bus (D_0 to D_7) carries all transactions to and from the 6800 CPU.

Software mnemonics—

JMP—Jump to designated address

JSR—Jump to subroutine

ORG—Originate starting program location

LDAA—Load accumulator A

LDX—Load index register

RTS—Return from subroutine

STAA—Store accumulator A.

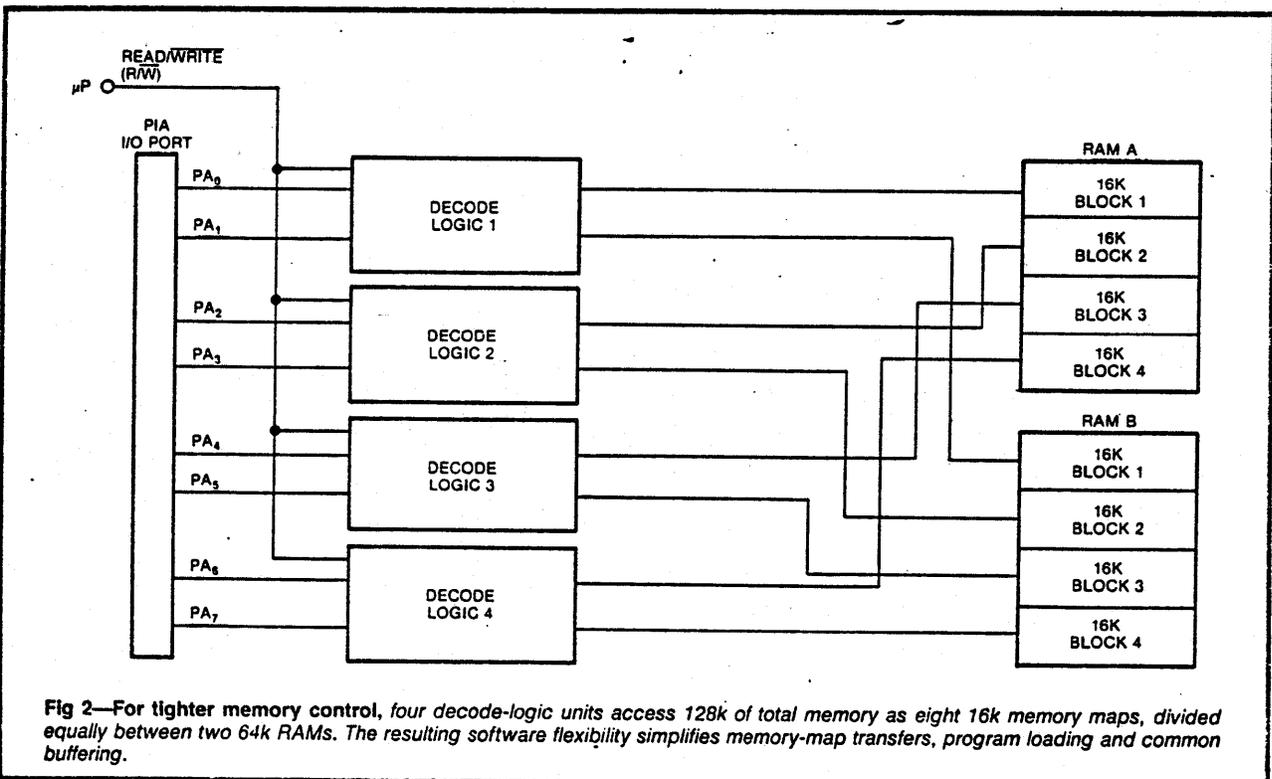


Fig 2—For tighter memory control, four decode-logic units access 128k of total memory as eight 16k memory maps, divided equally between two 64k RAMs. The resulting software flexibility simplifies memory-map transfers, program loading and common buffering.

6800 software transfer routines

The following routines prove useful if you implement the memory-mapped approach described in this article on a 6800- μ P-based system.

ORG \$F000 (RAM A or RAM B)

Location \$F000 lies within the user's program area; \$0000 represents the initial transfer-routine location. To change control from one map to another, the program jumps to the map-transfer routines (see example routines below).

LDX #ADDR

JSR TRNSFR

A TRNSFR routine transfers μ P control from one memory map

to another. It then proceeds to branch to the address stored in the index register. By branching, the subroutine call stores the last address on the program stack.

JMP RETURN

A RETURN routine also transfers μ P control from one memory map to another. It then proceeds to branch to the address stored in the program stack by executing an RTS statement.

Map-transfer routines:

ORG \$0000 (RAM A)

TRNSFR LDAA #03

STAA PIA0

ORG #0000 (RAM B)

TRNSFR LDAA #00

STAA PIA0

After one map's data accumulates in the PIA, control automatically transfers it to the other map. Operand PIA0 is dedicated to map transfers.

JMP 0,X

RETURN LDAA #03

STAA PIA0

RTS

JMP 0,X

RETURN LDAA #00

STAA PIA0

RTS

parameters between them. The Read/Write (R/W) line activates these latter two modes as follows: When the line goes HIGH, the μ P executes a read cycle and transfers code from one map into its CPU; when the line goes LOW, the μ P executes a write cycle and stores code in the other memory map (see box, "6800 software transfer routines").

The software aspect of dual-map switching yields several advantages: The μ P performs all relocations automatically; program parameters and control pass easily between maps; memory maps exchange at any time during the program's execution no matter which map or memory location resides in the CPU; and processing efficiency does not degrade.

Smaller maps offer program versatility

For even tighter memory control, you can subdivide the 128k of total memory into eight 16k memory maps, distributed as four maps in each 64k RAM (Fig 2). This subdivision mandates a fourfold increase in decode-logic hardware, but the advantages of increased software flexibility greatly outweigh the extra expense.

One application of this memory arrangement, for example, places a μ P's operating system, program stack and transfer routines in a common memory. In this manner, you eliminate most of the map-transfer software complexities.

Another application employs two operating systems with a common program buffer. In this example, you load a disc operating system into one 16k block of RAM A and a BASIC program into the corresponding block of RAM B. You can then readily transfer control from the low-level language to the high-level one, and vice versa. This loading technique also permits you to program a variety of complex operations within the

same buffer space. A variation on this approach provides a choice of program modes by allowing map or mode transfers by means of software or a set of hardware switches.

You can extend a μ P's addressing range even further by multiplexing address lines to switch several 64k memory blocks. With only a slight modification of the decode logic, you can thus structure the μ P to address 128k, 192k or 256k bytes. For such multiple-map switching, adapt the same hardware/software considerations utilized for the dual-map configuration.

In each case, keep track of the program stack in some common memory set aside for this purpose, because the stack-pointer register within the CPU does not change during map-transfer operations. Locating the stack in common memory permits access of the entire stack by subroutines in all memory maps. **EDN**

Author's biography

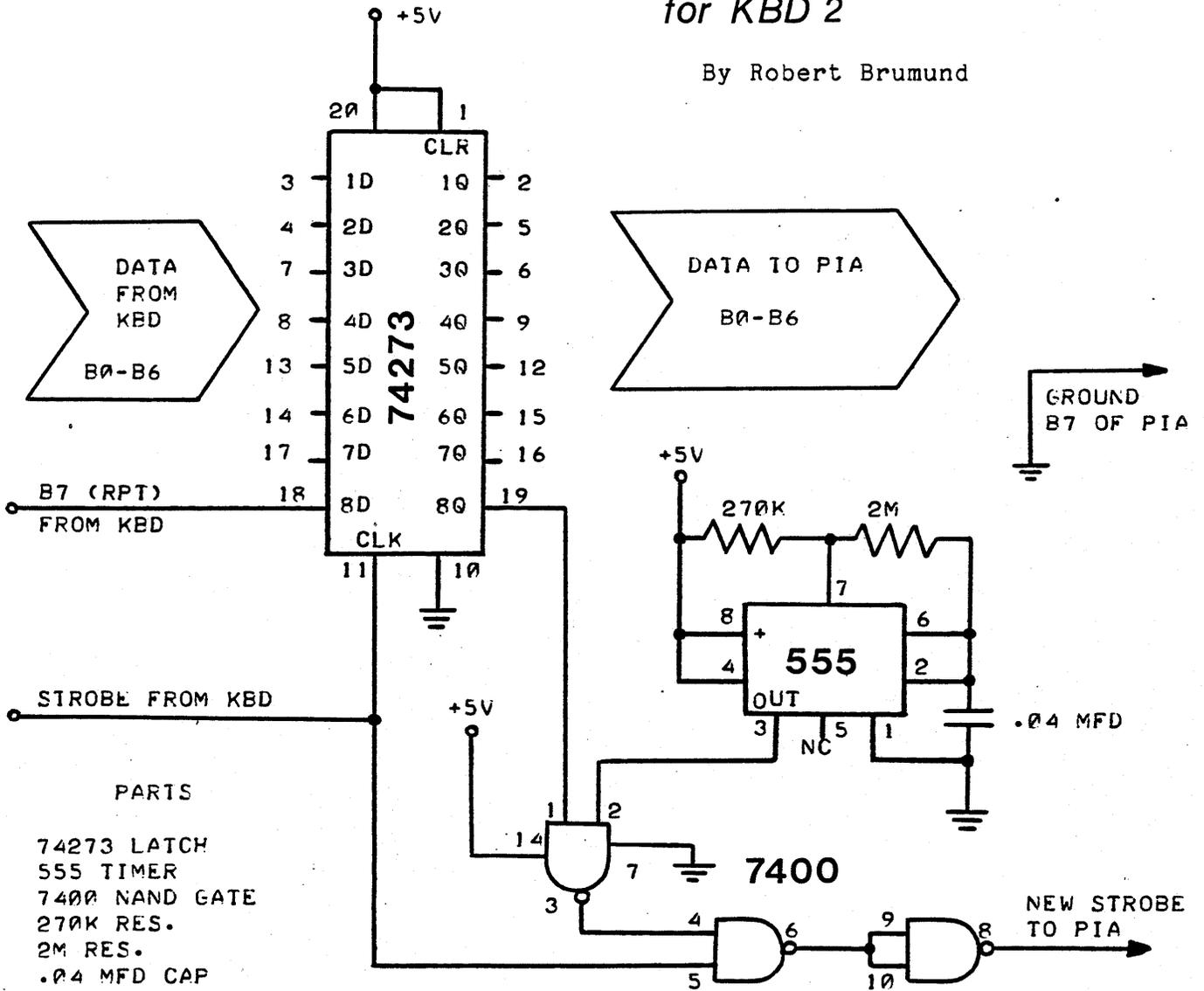
Stephen Strom, a design engineer engaged in micro-computer system development at Motorola Semiconductor Products Inc, Mesa, AZ, previously worked at Harris Corp and earned a BSEE at Carnegie-Mellon University. Stephen's hobbies include tennis, raquetball and carpentry.



Repeat Key / Data Latch

for KBD 2

By Robert Brumund



THE CIRCUIT MAY BE PLACED ANYWHERE BETWEEN THE KEYBOARD AND THE PIA.
 OPERATION: WITH THE REPEAT KEY DOWN, PRESS ANY CHARACTER KEY. THIS
 CHARACTER WILL THEN BE OUTPUTTED TO THE PIA AT THE RATE OF 6 PER SEC
 FOR AS LONG AS THE CHARACTER KEY IS KEPT DOWN.

Subject: Increased System Speed

The Sphere 300 Systems were designed with a basic clock cycle of 1.5 milli-seconds. This results in a 666KHz. clock, which is well below the specified maximum of the MC6800 CPU.

The major reason for the reduced clock rate is that 1702A proms were used. These have an access time of approximately 1 milli-second and therefore $\phi 2$ must be at least this long to allow operation.

One solution which Sphere chose to implement in the 500 systems was to slow down the $\phi 2$ only when the proms are accessed. There are several CPU board changes needed but an upgrade is feasible.

The second obvious solution was to replace the proms with a faster memory. A 2708 adapter was formerly available from Programma and it worked well.

Once the proms have been changed, the system will still not run above 1.2 milliseconds. The reason for this is in the memory write timing. The secret is in the 74123 which (both on CPU and MEM boards) disables the \overline{WE} signal while the data buss does not contain valid data. The present design has a delay of 355 Nano-seconds, which, when coupled with propagation delays, yields only 60 nano-seconds to write the data to the memory with a 500 Nano-second $\phi 2$. This can be modified by changing R1 on each MEM board from a 33K resistor to 12K. This will change the leading edge of the \overline{WE} signal to coincide with the worst case leading edge of the valid data (200 Nano-seconds after the $\phi 2$ leading edge). There is a corresponding resistor on CPU boards which may be changed for memory banks on a CPU board.

Charles Matteson
450 Stiles Deane Hwy.
Wethersfield, Connecticut

Editor's note: Most Sphere boards and replacement parts are still available at reasonable cost from Charles.

LISTING OF 1980-1981 ACTIVE SPHERE USERS

1	1	80	ASI MARKET RESEARCH	7655 SUNSET BLVD.	HOLLYWOOD CA.90046
2	110	80	JOHN BAYLIS	P.O. BOX 137	NSL UTAH 84054
3	6	80	BITS AN PIECEZ	P.O. BOX 23	WATERLOO 2017 AUSTRALIA
4	7	80	JEAN-FRANCOIS BOIVIN	1405 RUE IBERVILLE	MONTREAL CANADA H2K 3B2
5	9	80	SAM BRONSTEIN	9026 AUTOVILLE DR.	COLLEGE PARK MD. 20740
6	66	80	JEFFREY BROWNSTEIN D.D.S	2 TOR ROAD	WAPPINGERS NY. 12590 914 297-3950
7	116	80	ROBERT BRUMUND	2136 BEL AIR AVE.	SAN JOSE CA. 95128
8	96	80	DOUG CALLEY	RT 1 BOX 51 LEUPP BANK	FLAGSTAFF AZ. 86001
9	99	80	JIM CHIN	33-34 70TH ST.	JACKSON HEIGHTS NY. 11372
10	18	80	SCOTT D'AMRON	2123 SUFFIELD DR.	WINTER PARK FL.32789
11	22	80	LEROY DANNER	3900(3900-45TH STS.)#23	KENOSHA WI. 53140
12	21	80	OWEN DAVIS	710 WAIKIKI DR.	DES PLAINES IL.60016
13	24	80	JOSEPH DAVES	2510 BROADWAY	BIG SPRING TX. 79720
14	25	80	JOHN DEPPE	1201 2ND ST.	DELANCO NJ. 08075
15	28	80	R.S. DOWNS	ROUTE 7 BOX 211-A	RALEIGH NC. 27614
16	27	80	CARLYLE EASTMAN	6016 N.ARLINGTON	SAN PABLO CA. 94806
17	29	80	ROBERT ENNIS	9322 LAUREL	FONTANA CA. 92335
18	124	80	DAVID FRANKEL	2012 WEST ST. LOUIS DR.	KOKOMO IN. 46901
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20	38	80	CARL GECHNAUER	HIGHWAY 219 S. BOX 26	LAKE PARK IA. 51347
21	34	80	DAVID GHERSON	1745 RAVIZZA AVE.	SANTA CLARA CA. 95051
22	35	80	JOHN GIBBON	3 PUDDINGSTONE RD.	NORRIS PLAINS NJ. 07950
23	37	80	R.M. GRAINGER	RR NO.1 PRESCOTT	ONTARIO CANADA K0E 1T0
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26	117	80	ROBERT HATFIELD	821 HUNT ST.	ASHLAND KY. 41101
27	46	80	JOHN HEACOCK	4 STANFORD DR. #3A	BRIDGEWATER NJ. 08807
28	106	80	DR.GEORGE HORNER	80 DELAMERE AVE.	STRATFORD ONT.CANADA N5A 4Z5
29	42	80	JOHN IRSIK	1017 MICHIGAN	BEAUMONT CA. 92223
30	53	80	MICHAEL KOVIS	3810 MAIN STREET	STRATFORD CT. 06497
31	54	80	DAVID LAKE	243 W.SIRIUS	ANAHEIM CA. 92802
32	52	80	G.H. LATTA	RT. 3 SMYRNA RD.	SEARCY AR. 72143
33	58	80	DICK MASON	1037 PARK HILL LANE	ESCONDIDO CA. 92025
34	61	80	CHARLES MATTESON	450 SILAS DEANE HGWY.	WETHERSFIELD CT. 06109
35	60	80	TOM MEIER	401 N. LEVITT ST.	ROME N.Y. 13440
36	64	80	E.HUGH MELTON JR.	8314 UNIVERSITY DRIVE	RICHMOND VA. 23229
37	119	80	DAVID PAUL MOORE-DIRECTOR	COMPUTER CTR. QUINCY COLLEGE	QUINCY IL. 62301
38	95	80	DAVE PERRY	57 FOREST HILL ROAD	WEST ORANGE NJ. 07052
39	72	80	J.C. PIRTLE	P.O. BOX 537	AZLE TX. 76020
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41	79	80	WARREN REDDEN	RR 1 BOX 22	GYPSUM KS. 67448
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46	92	80	DR. HARRY SPAIN	382 BLUE RIDGE RD. HOLIDAY PARK	PITTSBURGH PA. 15239
47	83	80	DR. ROGER J. SPOTT	13975 CONNECTICUT AVE.	WHEATON MD. 20906 301 299 6030
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49	86	80	RICHARD THERIAULT	12120 'ARCHVEQUE	MONTREAL CANADA H1H 3C1
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51	91	80	WARREN WEIMER	23025 KINARD AVENUE	CARSON CA. 90745 213 835-9417
52	89	80	CHAN WAI YUNG	P.O. BOX K-2296	KOWLOON HONG KONG

N E X T I S S U E

The editors find it hard to believe there will ever be another SPHERE newsletter if there is nothing to print in it. Those of us left must do our parts in keeping the information flowing.

Send in anything you have....we would very much like to hear from those users who have not ever sent in material. After five years we know you must have been running something!

From now on we will produce a newsletter whenever there is enough material. The regular issue spacing of the past will not be possible with the current scarcity of contributions.

Our most generous Thank You's go to the Editors of EDN magazine, who allowed us to reprint some of the material in this issue.

The enclosed sequence provides for excellent user prompt for input statements in BASIC as it begins on the first dot and only accepts the desired number of characters. You must use two dots more than the number of characters requested.

```
100 PRINT "PATIENT'S FIRST NAME"
105 PRINT ".....";
110 PAT 7EFCFD
120 INPUT A$
130 IF LEN(A$)>10 THEN GOTO 100
140 PRINT A$
```

CSS BASIC accepts tapes of Peter Stark's 6800 Assembler (written in Basic). It should be easy to modify (add macros) but it runs slowly. Available from STAR KITS on cassette.