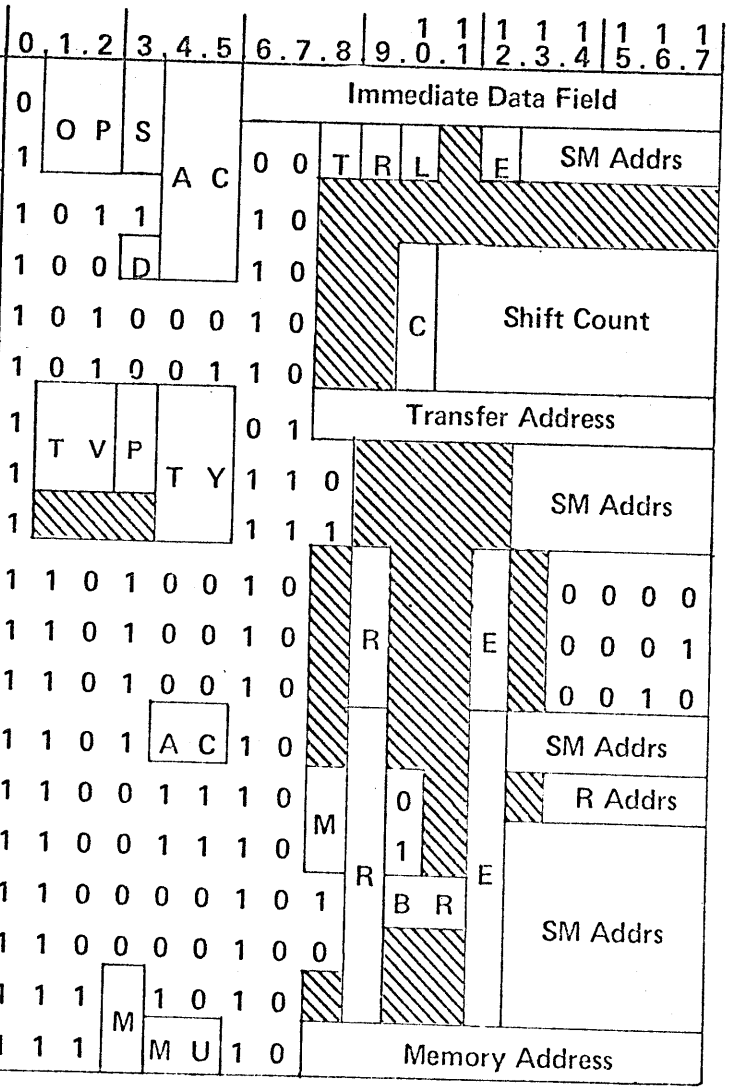
IOP
MINIFLOW
INSTRUCTIONS

(with control fields)



AC
00 All 3
01 AC1
10 AC2
11 AC3

OP
00 Add
01 And
10 Or
11 Pass

L
0 No Link
1 Link Carry in and Zero Test

S
0 Test Only
1 Load & Test

T
0 Set Engine PRI's
1 Set Target PRI's

TY
00 Transfer or Continue
01 Call or Continue
10 Transfer or Return
11 Transfer or Exit

TV
00 Always False
01 Carry False
10 Zero
11 CF or Zero

C
0 Use Shift Count Field
1 Use Shift Register Contents

D
0 Left
1 Right

P
0 Transfer if False
1 Transfer if True

R
0 Continue
1 Return

E
0 Continue
1 Exit

MU
*00 Active CPU Control Core
01 IOP Control Core
*11 Channel Registers or IOP Control Core if addr. > 77
*Active Channel Ptr ORed with bits 16 & 17 of Addr.

BR
00 AC1-2 Only
01 AC1-2 & DR 7-13, 18-35
10 AC1-2 & DR 0-6, 14-17
11 AC1-2 & Directive Register

M
0 Write
1 Read

SCRATCH MEMORY ASSIGNMENTS

OCTAL ADDRESS	LENGTH	WRITE DATA PATH	USE-DESCRIPTION- REMARK
00	18	YES	target location counter (sched. increments by 1)
01	18	YES	general purpose
02	18	YES	general purpose
03	18	YES	general purpose
04	7	YES	shift counter (bit 11 replicated into 0-10 on read)
05	3	ONLY	active channel (bits 16-17) & active CPU (bit 15)
06	2	YES	target CF (bit 16) and zero (bit 17) indicators
07	18		AC 3
10	18	YES	general purpose
11	18	YES	general purpose
12	18	YES	general purpose
13	18	YES	general purpose
14 to 17	0		AC Decode Options
20	7		directive reg 0-6
21	3		directive reg 7-9 (CF set on fetch if bit 7 is one)
22	4		directive reg 10-13 (zero set on fetch is not all zero)
23	4		directive reg 14-17
24	6		directive reg 18-23
25	6		directive reg 24-29
26	6		directive reg 30-35
27	18	YES	directive reg 18-35
30	0		may be read as all zero's
31	1		may be read as constant of one
32 to 37	0		spare

All fields read in right justified (to bit 17) and fill with leading zeros if not 18 bits long (except SM4 fills with 'sign', i.e. bit 11).