```
%       1.5     7/30/83
% SCSI DMA Control Microcode

#include "pal16r4"

%Inputs

#define /AEN     pin6
#define /DmaReq pin2
#define /XACK    pin3
#define /Out     pin4
#define EnWordMode      pin5
#define /Br      pin7
#define BClk     pin8
#define Reset    pin9

% Outputs

#define /WR_SS  pin19
#define /RD_SS  pin18
#define /MWTC   pin17
#define /MRDC   pin16
#define /State0 pin15
#define /State1 pin14
#define /Inc    pin13
#define /BrClr  pin12

% Equations

PALBEGIN

% This is a fairly complicated state machine.  The timing diagram
% should be consulted for an explanation.

/WR_SS  :=      {{ VCC }}
                / /MRDC * /XACK                 * / /Out

/RD_SS  :=      {{ VCC }}
                / /AEN * / /Br                  *   /Out
        +       / /RD_SS * /Inc                 *   /Out
% Must not be asserted unless Br is also asserted
% Then it is self-latching until the end of the cycle

/MWTC   :=      / /AEN  * / /Br * /XACK * /State0 *   /Out

/MRDC   :=      / /AEN  * / /Br * /XACK * /State0 * / /Out

/State0 :=      / /XACK   * /State1 * / /MWTC
        +       / /XACK   * /State1 * / /MRDC
        +       / /State0 * /State1

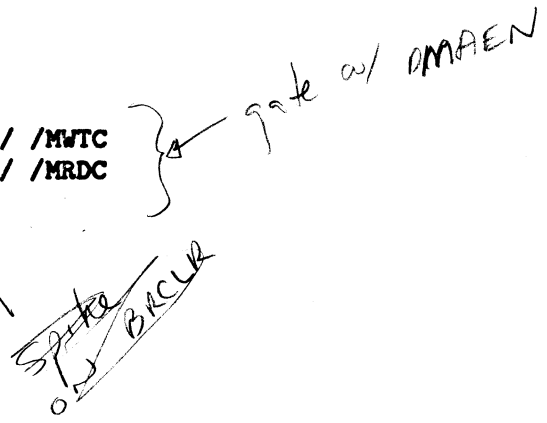
/State1 :=      / /State0 * /State1

/Inc    :=      {{ VCC }}
                / /State0 *   /State1
        +       / /State0 * / /State1 * EnWordMode
```

Hold active 100 ns longer.

```
/BrClr  :=      {{ VCC }}
                / /XACK * / BClk * / /MWTC
        +       / /XACK * / BClk * / /MRDC
        +       Reset

PALEND
```



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% Equations

PALBEGIN

% This is a fairly complicated state machine.  The timing diagram
% should be consulted for an explanation.

/WR_SS  :=      {{ VCC }}
                / /MRDC * /XACK                 * / /Out

/RD_SS  :=      {{ VCC }}
                / /AEN * / /Br                  *   /Out
        +       / /RD_SS * /Inc                 *   /Out
% Must not be asserted unless Br is also asserted
% Then it is self-latching until the end of the cycle

/MWTC   :=      / /AEN  * / /Br * /XACK * /State0 *   /Out

/MRDC   :=      / /AEN  * / /Br * /XACK * /State0 * / /Out

/State0 :=      / /XACK   * /State1 * / /MWTC
        +       / /XACK   * /State1 * / /MRDC
        +       / /State0 * /State1

/State1 :=      / /State0 * /State1

/Inc    :=      {{ VCC }}
                / /State0 *   /State1
        +       / /State0 * / /State1 * EnWordMode
```

```
/BrClr  :=      {{ VCC }}
                / /XACK * / BClk * / /MWTC
        +       / /XACK * / BClk * / /MRDC
        +       Reset

PALEND
```