```
%       1.4     6/27/83
% SCSI Multibus Interface Pal

#include "pal16l8"

% Inputs

#define s_a00           pin2
#define /sel            pin3
#define mrdc            pin4
#define mwtc            pin5
#define /s_dmaen        pin6
#define s_io            pin7
#define s_en16bit       pin9

% Outputs

#define /ce_word        pin17
#define /ce_byte        pin16
#define mb_ds           pin15
#define /p1_a00         pin14
#define /p1_bhen        pin13
#define /mb_in          pin12

PALBEGIN

/ce_word :=     {{ VCC }}       % (word access or lower byte) and (sel or dma)
                / /p1_bhen * / /sel     % we are the slave
        +         /p1_a00  * / /sel
        +       / /p1_bhen * / /s_dmaen % we are the master
% cope with the fact that in byte mode, the scsi only has the upper byte

/ce_byte :=     {{ VCC }}
                  /p1_bhen  * / /p1_a00 * / /sel % upper byte only and sel
        +         / s_en16bit * / /s_dmaen      % byte mode and dma

mb_ds    :=     {{ VCC }}
                / mrdc * / mwtc % De-Morganized sel*/s_dmaen*(mrdc + mwtc)
        +       /sel
        +       / /s_dmaen
% Don't acknowledge an internally-generated DMA cycle.

/p1_a00 :=      {{ / /s_dmaen }}
                / s_en16bit * / s_a00

/p1_bhen :=     {{ / /s_dmaen }}
                s_en16bit

/mb_in   :=     {{ VCC }}
                  /sel              * / s_io    % not slave, assume dma
        +       / /sel * / /s_dmaen * / s_io    % see i) and ii)
        +       / /sel *   /s_dmaen * / mrdc    % slave so use mrdc
% Buffer direction control:
%
% a) For a slave request, the direction information is not
%    available until the mrdc strobe comes along.
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%    The select signal is valid before this time, so it is
%    used to enable mrdc as the signal which controls the direction
%    of the data buffers.
%    In the case of a read, there is enough time to turn
%    the buffers around after the read strobe appears.
%    There may be momemtary contention for the internal bus
%    in this case.
% b) For a dma cycle, the Multibus will be idle before the AEN
%    is asserted, so it is okay to leave the buffers pointing out.
%    If select is not asserted, the buffers are turned in the direction
%    necessary for a DMA cycle, as determined by s_io.
%    It is possible for select to be asserted during a DMA cycle.
%    i) Since the Multibus has no address qualifier, if the board
%       is set to respond to Multibus address 000000, the select
%       signal will be asserted while the bus is idle.  The bus
%       will be idle momentarily during a DMA cycle, just before
%       the DMAEN signal is asserted.  In this case, the buffer
%       will be turned in the direction implied by the DMA transfer
%       (s_io) as soon as the DMAEN signal is asserted.  Momentary
%       contention for the internal bus may result, but things will
%       have settled down by the time that the Multibus write strobe
%       is asserted.
%    ii) If a DMA cycle is attempted which references a register
%       on the board, there will be an unavoidable contention.
%       The DMA cycle will time out, resulting in a bus error.
%
PALEND
```