

# **6100 Disk Controller User's Guide**

**PB6100-9001-02**



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## LIST OF EFFECTIVE PAGES

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## PREFACE

This manual contains sufficient information to enable the end user to install, test, and operate the System Industries 6100 Single Board Disk Controller.

The technical contents of this manual have been prepared based on the following assumptions of reader knowledge:

1. The reader should have a working knowledge of Digital Equipment Corporation PDP-11 processor hardware.
2. The reader should be familiar with disk structures and hardware.
3. The reader should be familiar with standard installation, power, grounding and peripheral cabling procedures.

The information in this manual is presented in five major sections. The contents of these sections are as follows:

Section 1.0	System Overview, describes 6100 board features, capabilities, and system configurations supported.
Section 2.0	Physical Description, describes and illustrates the 6100 Controller PCB.
Section 3.0	Functional Description, describes and illustrates the functional operation of the 6100 board.
Section 4.0	Installation, describes and illustrates the procedures required to install the 6100 board and cable the drives.
Section 5.0	Diagnostics, describes the diagnostics compatible with the 6100 Controller.

Other publications applicable to the 6100 Controller are as follows:

<b>Publication Number</b>	<b>Title</b>
N/A	PDP-11 Processor Handbook
EK-RM023-UG-002	DEC® RM02/3 Disk Subsystem User's Guide
64712400	CDC Flat-Cable Interface Specification for SMD, MMD, and CMD Families
64709300	CDC Product Specification for the Flat-Cable Interface Storage Module Drive Family
B03P-4580-0100B	Fujitsu M228X Fixed Disk Unit Customer Engineering Manual
83322200	CDC Storage Module Drive BK4XX, BK5XX Hardware Reference Manual
83322320	CDC Storage Module Drive BK6XX, BK7XX Hardware Reference Manual
PB9901-9001-01	System Industries Disk Drive User's Guide

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## 1.0 SYSTEM OVERVIEW

The System Industries 6100 Controller is a single board disk controller that allows for the exact emulation of the DEC PDP-11 series RM02/03/05 disk drive subsystem.

The controller interfaces to the PDP-11 UNIBUS by plugging into any standard, small peripheral controller hex interface slot of the backplane or an expansion box.

The controller allows for the control of up to four industry standard storage module drives .

### 1.1 Features

The controller includes the following standard features:

- DEC operating system software transparency
- DEC RM03 and RM05 media compatibility
- Four sector static RAM data buffering (2048 bytes)
- Header verification and CRC checking
- Overlapped seeks on all attached drives
- Dual port drive support
- Contiguous sector data transfers up to 64K words
- RPS look ahead
- Search command for disk rotational position synchronization
- Switch selectable device and vector addressing
- Switch selectable burst data error correction
- Internal microprocessor, data RAM, and register file tests
- DEC diagnostic compatibility

### 1.2 Configuration

The controller can be configured to support multiple disk drives by daisy-chaining. The controller can control up to four physical drives or eight logical drives. The drives currently supported by this controller are the SI 9762, 9766, and 9775, and SI 9784. The controller, when used with these drives, is software transparent.

#### 1.2.1 Software Compatibility

The Controller is software transparent when used as an RM03 with an SMD 80 megabyte disk drive or when used as an RM05 with an SMD 300 megabyte disk drive. The controller is also software transparent when used as RM03s with a 160 megabyte disk drive configured as two logical 80 megabyte disk drives or as RM05s with a 675 megabyte disk drive configured as two 300 megabyte disk drives.

The controller maintains transparent software compatibility when used with the following DEC operating systems:

- RSX-11M PLUS
- RSX-11M
- RSX-11D/IAS
- RSTS/E

### 1.2.2 Drive Configurations

The disk drive interface conforms to standard flat cable specifications for SMD drives of Control Data Corporation and System Industries. The SI 9775 drive may emulate two 9766 drives and the SI 9784 may emulate two SI 9762 drives. Table 1-1 lists the drive configurations supported. Figure 1-1 illustrates the disk/controller cabling. Figure 1-2 illustrates cabling for dual port configurations.

Table 1-1 Drive Configurations

DRIVE TYPE	CAPACITY MBYTE	DIRECT/MAPPED	MAX. NUMBER OF UNITS LOGICAL	PHYSICAL
SI 9762	80	Direct	4	4
SI 9784	160	Direct	4	4
SI 9784	160	Mapped (2×80)	8	4
SI 9766	300	Direct	4	4
SI 9775	675	Mapped (2×300)	8	4

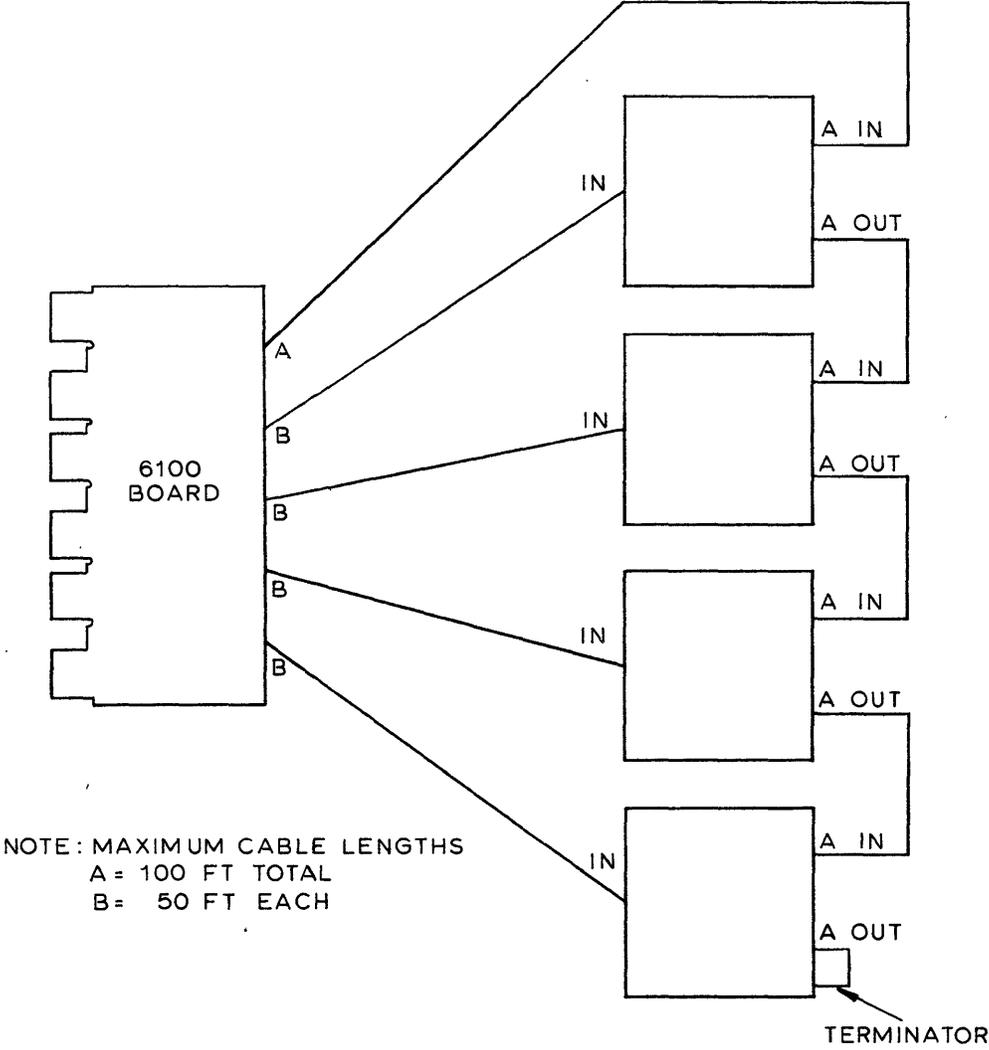


Figure 1-1. Disk Drive Configuration

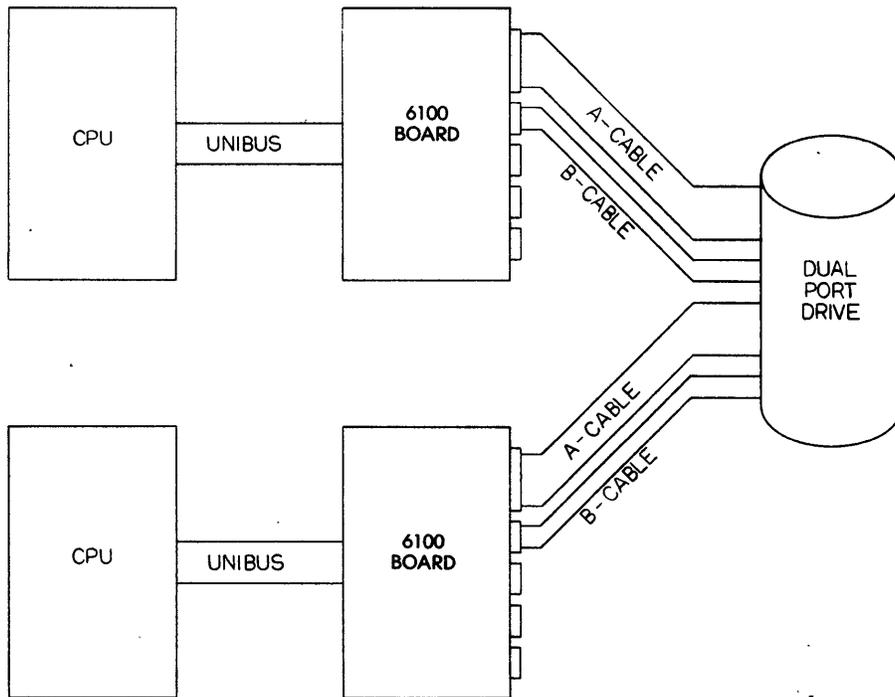


Figure 1-2. Dual Port Configuration

## 2.0 PHYSICAL DESCRIPTION

The controller is a standard, 16 by 9-inch, single hex-slot board, incorporating a unique high-speed bipolar microprocessor design that exactly emulates the DEC PDP-11 RM02 Controller. The board contains four DIP switches used for such functions as device and vector addressing. The board also contains one LED that is used for internal diagnostics. Refer to Section 4.0 for installation, cabling, and switch procedures.

### 2.1 Power Requirements

The following voltages are required to operate the controller.

+ 5 Vdc  $\pm$ 5% @ 11 Amps Maximum

-15 Vdc  $\pm$ 5% @ 0.7 Amps Maximum

### 2.2 Drive Interface

The disk drive interfaces to the controller board via two flat cables referred to as cables A and B.

#### 2.2.1 A-Cable

The A-cable is a 60-pin twisted pair flat cable that connects the first physical disk drive to the controller-board and is additionally used to daisy-chain disk drives.

#### 2.2.2 B-Cable

The B-cable is a 26-pin ribbon flat cable that is radially connected from each disk drive to one of the four B-cable connectors on the controller board.

### 2.3 Computer Interface

The following subsections describe the controller interface to the PDP-11 computer.

#### 2.3.1 UNIBUS Interface

The controller interfaces to the PDP-11 UNIBUS by plugging into any standard DEC Small Peripheral Controller (SPC) interface slot of the PDP-11 backplane.

#### 2.3.2 Device, Interrupt, and Address Configuration Switches

Device, interrupt vector, and register group addresses are all switch selectable. By setting these switches the controller can be configured to allow for the emulation and mapping of several devices, the establishment of the device interrupt vector, and the starting address of the controller's control register group.



## **3.0 FUNCTIONAL DESCRIPTION**

This section provides a brief description of the functional operation of the controller features. Figure 3-1 shows a simplified functional block diagram of the controller.

### **3.1 Priority Levels**

The controller's priority level is jumper selectable. Priority levels enable the controller to generate a processor interrupt request on one of the bus request levels, BR4 through BR7. Availability of the bus request is determined by receipt of a corresponding bus grant level, BG4 through BG7. Section 4.0 describes the priority level jumpering procedure. The controller is preset at a priority level of 5.

### **3.2 Overlapped Seeks**

Overlapped seeks may be performed on all attached drives. This capability is provided by maintaining separate registers in the register file for each logical drive. Seeks are issued as they are received if a data transfer is not currently active on any drive. When a data transfer is in progress, a seek command to another drive is issued when the end of a cylinder is detected.

### **3.3 Dual Port Drive Compatibility**

The controller can support dual port drives. This support is designed to be software transparent.

### **3.4 Contiguous Transfers**

Contiguous transfers of sector data allow up to 64K bytes to be transferred in response to a single drive command.

### **3.5 RPS Look-Ahead**

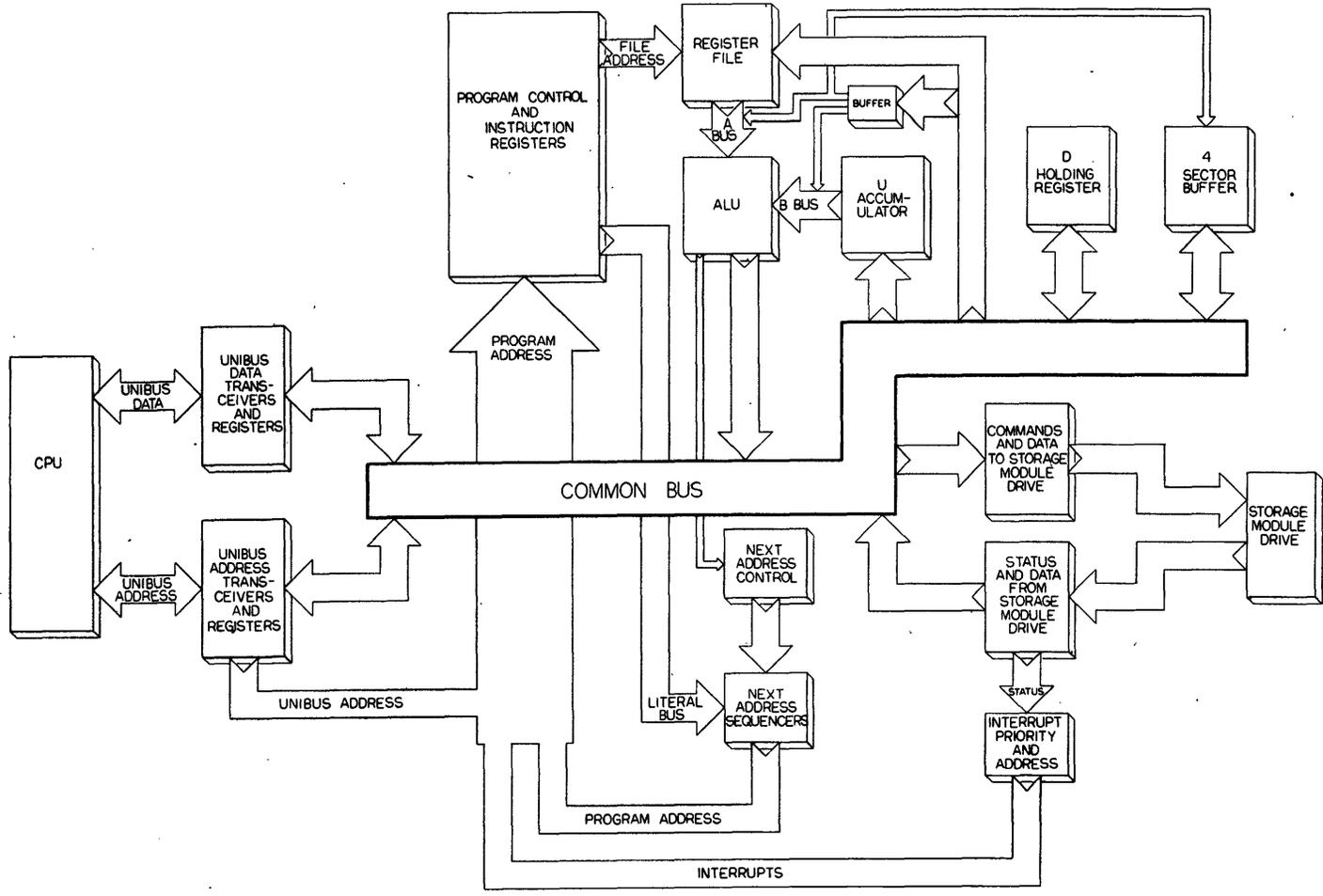
The RPS feature is compatible with DEC's look-ahead feature. The controller maintains a current sector count for each disk drive attached to it, this feature provides the programmer with a means of optimizing disk accesses by minimizing rotational delay.

### **3.6 Search Command**

The search command is compatible with the DEC RMOX search, and combines a seek with a search for the desired sector. This feature is used by the software to synchronize the disk rotational positioning with the issuing of data transfer commands.

### **3.7 Error Correction**

Burst and data error correction is accomplished by the use of the AMD Z8065 Burst Error Processor (BEP). The BEP detects all errors and allows for correction of error bursts up to 11 bits in length. The error information is loaded into the ECC registers (RMEC1 and RMEC2) and the correction can be made by the system software.



(SIMPLIFIED VERSION)

Figure 3-1. 6100 Block Diagram

An uncorrectable error is defined as any error field larger than the 11-bit burst. If an uncorrectable error is detected, a bit is set in the error register (RMER1) and the data transfer operation is aborted. The maximum delay time for correctable data errors is 2 milliseconds.

The controller's attempt to correct a burst data error is transparent to the operating system when the ECC switch (location 5L, switch 2) is set. Refer to Section 4.2.4 for a description of these switch settings.

### 3.8 Controller Registers

The controller communicates with the system's disk driver program via 19 registers located on the controller. The contents of these registers may be accessed by their UNIBUS address. A detailed description of the controller registers is contained in Appendix A and a register summary is contained in Appendix B. The registers and their UNIBUS addresses are shown in Table 3-1.

Table 3-1 Registers and UNIBUS Addresses

<b>Register</b>		<b>UNIBUS Address</b>
RMCS1	(Control and Status 1)	776700
RMWC	(Word Count)	776702
RMBA	(UNIBUS Address)	776704
RMDA	(Disk Address)	776706
RMCS2	(Control and Status 2)	776710
RMDS	(Drive Status)	776712
RMER1	(Error 1)	776714
RMAS	(Attention Summary)	776716
RMLA	(Look-Ahead)	776720
RMDB	(Data Buffer)	776722
RMMR1	(Maintenance 1)	776724
RMDT	(Drive Type)	776726
RMSN	(Serial Number)	776730
RMOF	(Offset)	776732
RMDC	(Desired Cylinder)	776734
RMHR	(Holding)	776736
RMMR2	(Maintenance 2)	776740
RMER2	(Error 2)	776742
RMEC1	(ECC Position)	776744
RMEC2	(ECC Pattern)	776746



## 4.0 INSTALLATION

This section describes the procedures required to install, cable, and set the four DIP switches on the controller. This section also contains procedures that may be required for modification of the PDP-11 and SMD disk drives.

### 4.1 Visual Inspection

Before attempting to install the controller board or perform cabling operations, a visual inspection of the controller board, cables, disk drives, and PDP-11 backplane must be performed to determine the following:

- All components on the controller board are in place, secure, and not cracked or broken
- Pin connections for A- and B-cables are not bent or broken
- Any jumper wires installed on the board are connected properly and securely
- A- and B-cables are not bent or cut, and pin receptacles are secure
- Disk drive(s) is (are) configured for 32 sectors
- Terminators are removed from all but the last disk drive
- Index and sector jumpers are set for B-cable
- Bus grant continuity jumper board is removed from the controller SPC slot

### 4.2 Switch Settings

The controller board has four DIP switches that must be checked and/or set to conform to specific installation requirements. The switch locations on the board are shown in Figure 4-1. Table 4-1 lists the switch name and type.

Table 4-1 Controller Switches

SWITCH	TYPE	BOARD LOCATION
Throttle Count	Two positions (SW1-SW2) of 9-position DIP switch	5L
Starting Address	Seven positions (SW3-SW9) of 9-position DIP switch	5L
Drive Type	Two 8-position DIP switches	12R, 12S
Interrupt Vector	One 10-position DIP switch	14P

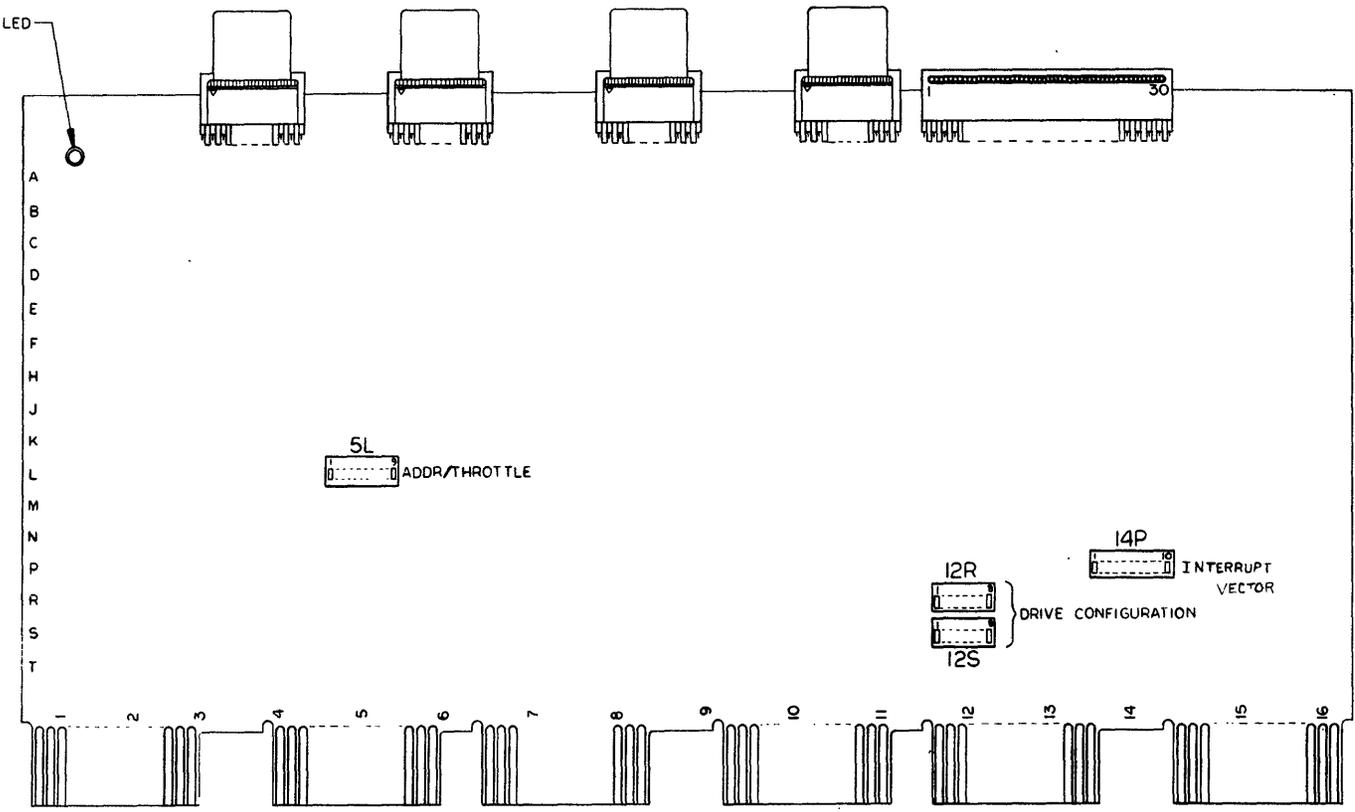


Figure 4-1. Controller Switches

### 4.2.1 DMA Throttle Count Switch

The throttle count switch determines how many words of data the controller will transfer, per NP request, onto the UNIBUS. The throttle count only uses switches 1 and 2 of the 9-position DIP switch at grid location 5L. Table 4-2 shows the throttle count switch settings.

Table 4-2 Throttle Count Switch Settings

SW1	SW2	DESCRIPTION
OFF	OFF	Throttle burst rate of 2 words per NP request. Simulates SACK.
OFF	ON	Throttle at microprogram control.
ON	OFF	Throttle at burst rate until SACK. If a higher priority request is received, the controller relinquishes the bus and asserts NPR.
ON	ON	Invalid setting.

Switch **ON**=0=closed

Switch **OFF**=1=open

### 4.2.2 Register Set Address Switch (CS1)

The register set address switch determines the starting address of the controller register group. The register set address switch uses switches 3 through 9 of the same DIP switch used for the throttle count switch. Table 4-3 describes the standard switch settings for normal operation.

Table 4-3 Register Set Address Switch Settings

REGISTER SET STARTING ADDRESS	12 SW3	11 SW4	10 SW5	09 SW6	08 SW7	07 SW8	06* SW9
776700	OFF	OFF	OFF	ON	OFF	OFF	OFF
OR 776300	OFF	OFF	OFF	ON	ON	OFF	OFF

**NOTE:** Selectable address range is 760000 to 777700

Switch **ON**=0=closed

Switch **OFF**=1=open

\*UNIBUS address

### 4.2.3 Drive Type Switches

Two 8-position DIP switches (at grid locations 12R and 12S) are used to determine the drive type emulation and mapping. Table 4-4 illustrates which switches correspond to which physical drive numbers, and Table 4-5 illustrates the drive types configured by those switches. Each of the four drive type switch settings is polled, regardless of whether or not a physical drive is attached.

#### NOTE

In a mapped or combined configuration, the logical drive numbers of some drives will not be the same as their physical drive numbers.

Table 4-4 Drive Switches

DRIVE NO.	SWITCHES
0	12R 5-8
1	12R 1-4
2	12S 5-8
3	12S 1-4

Table 4-5 Drive Type Switch Settings

SWITCH				EMULATION/MAPPING
8 4	7 3	6 2	5 1	
OFF	ON	ON	ON	RM03 80 Direct
OFF	ON	ON	OFF	RM03 160 Mapped
OFF	ON	OFF	ON	RM03 160 Direct
OFF	ON	OFF	OFF	RM03 300 Direct
OFF	OFF	ON	ON	RM03 675 Mapped
ON	ON	ON	ON	RM05 80 Direct
ON	ON	ON	OFF	RM05 160 Mapped
ON	ON	OFF	ON	RM05 160 Direct
ON	ON	OFF	OFF	RM05 300 Direct
ON	OFF	ON	ON	RM05 675 Mapped

NOTE: All other codes are reserved.

### 4.2.4 Interrupt Vector Switch

The interrupt vector switch is a 10-position DIP switch (located at grid location 14P) that sets the 3-digit octal word of the interrupt vector location. The standard interrupt vector location is 254 octal. Other disk interrupt vectors are defined in the DEC PDP-11 Peripherals Handbook. Table 4-6 shows the switch setting for the standard and alternate interrupt vectors.

Table 4-6 Standard Interrupt Vector Switch Settings

SWITCH	1	2	3	256 4	128 5	64 6	32 7	16 8	8 9	4 10
254 Octal	Reserved	ECC*	Spare	ON	OFF	ON	OFF	ON	OFF	OFF
150 Octal	Reserved	ECC*	Spare	ON	ON	OFF	OFF	ON	OFF	ON

Switch **ON**=0=closed

Switch **OFF**=1=open

\*Internal ECC Correction=**OFF**

External ECC Correction=**ON**

### 4.3 Installation of the Controller Board

The controller board can be installed in any PDP-11 Small Peripheral Controller (SPC) backplane hex slot. The following procedures should be followed to ensure proper installation.

#### CAUTION

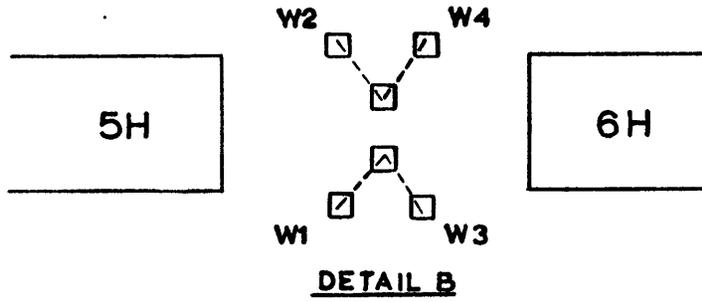
Be sure to power down the system before continuing with the installation procedure.

#### 4.3.1 Index and Sector Jumpers

The controller is normally configured to receive index/sector signals on the B-cable. For convenience under unusual circumstances, one (1) drive, and only one, can be allowed to transmit index/sector signals, via J-1 on the A-cable. In this case, that drive's B-cable must be connected to J-2 for proper controller operation. Additional drives whose B-cables are connected to J-3, J-4, or J-5 must have index/sector signals transmitted on their respective B-cables. The jumpers which allow index/sector selection between J-1 and J-2 are labeled W1 and W2 for J-2 and W3 and W4 for J-1. The jumpers will be either in W1, W2 or in W3, W4, but not both. They are located at 5H. See Figure 4-2.

#### 4.3.2 Priority Jumpers

Before physically installing the controller board, determine the priority level to be established. The controller board's standard priority level is set at 5. This priority level is etched on the PCB board (BR5 and BG5) at the factory. To change the priority level, the preset board etches must be cut and jumper wires installed (e.g., to change to a setting of BG4 from a setting of BG5, cut etches at W5-F, W6-L, and E-K, and add jumpers at W5-E, W6-K, and F-L). Refer to Table 4-7 for BR-BG priority jumper settings. Refer to Figure 4-2 for an illustration of jumper installation.



	W1	W2	W3	W4
J1 (A CABLE)	OUT	OUT	IN	IN
J2 (B CABLE)	IN	IN	OUT	OUT

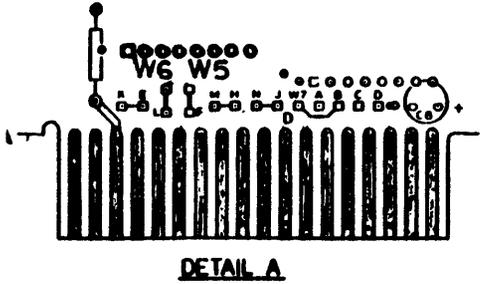
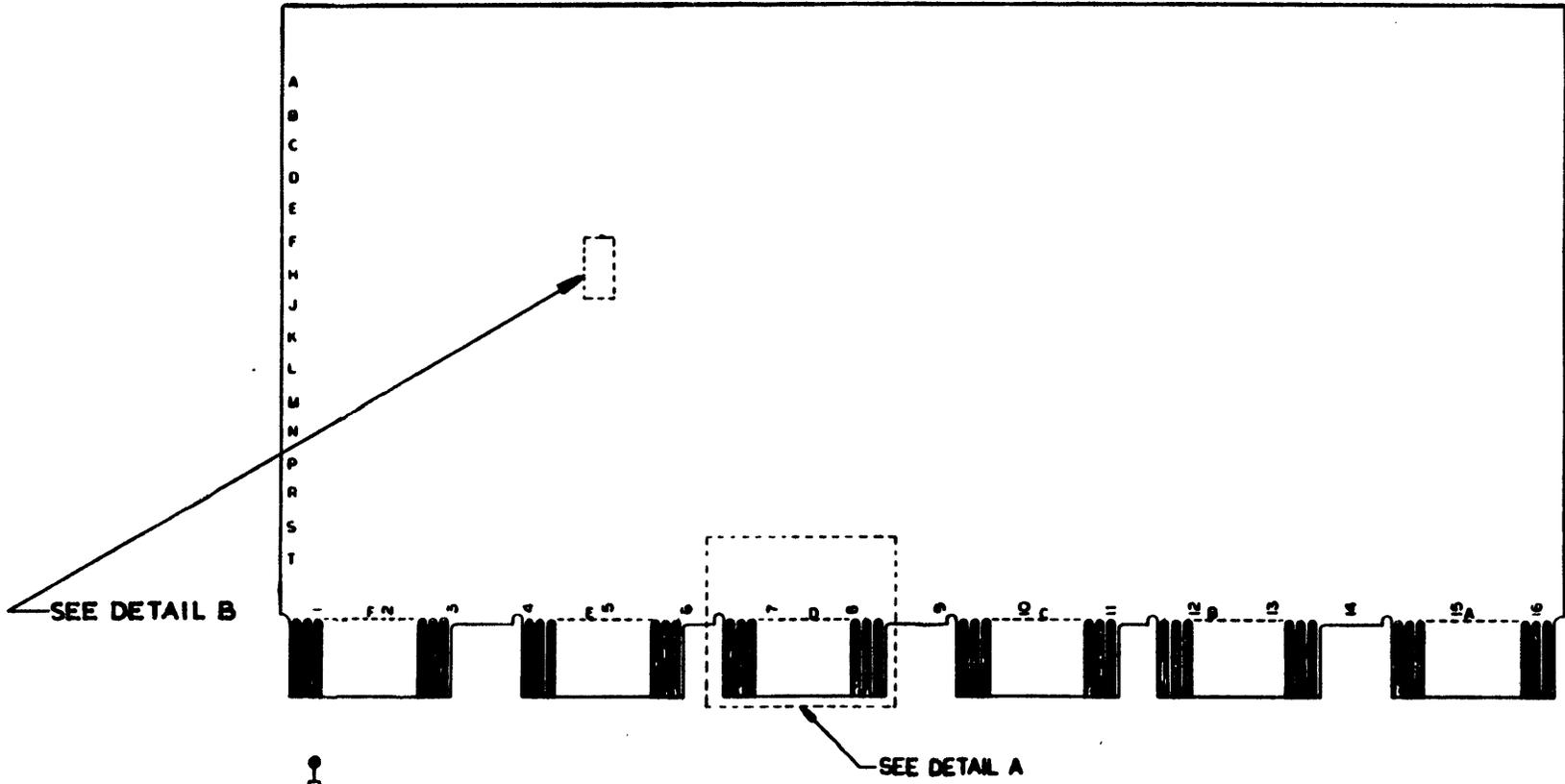


Figure 4-2. Priority Jumpers

Table 4-7 Priority Jumper Settings

LEVEL	JUMPER LOCATIONS				
BR4	W7-A				
BR5*	W7-B				
BR6	W7-C				
BR7	W7-D				
BG4	W5-E	W6-K	F-L	H-M	J-N
BG5*	W5-F	W6-L	E-K	H-M	J-N
BG6	W5-H	W6-M	F-L	E-K	J-N
BG7	W5-J	W6-N	F-L	E-K	H-M

\*BR5 - BG5 is standard feature and etched on PCB.

### 4.3.3 Nonprocessor Grant (NPG) Jumpers

The NPG *IN* signal on the wirewrap side of the PDP-11 backplane and the NPG *OUT* signal must not be jumpered together in the slot occupied by the controller board. Normally PDP-11 backplanes come with jumper wires installed. Similarly, all other NPG *IN* and NPG *OUT* pins must be connected through wire jumpers in all empty SPC slots. Figure 4-3 shows the pin location for the wirewrap side of the backplane.

When a DMA device (e.g., the 6100 Controller) is installed in an SPC slot of a backplane (type DD11-B or later), the wire from C01A1 to C01B1 must be removed from the slot.

## 4.4 Physical Installation of Controller Board

Before the controller board can be placed in the SPC slot, it may be necessary to remove the small board (bus grant continuity jumper board) in the slot. When all the foregoing procedures have been completed, the board may be physically installed. The board can be placed in any available SPC slot. The board is installed by pressing it firmly into the selected SPC slot with the component side facing in the same direction as the components on the other boards.

## 4.5 Drive Sector Count

The controller requires that the drives be set up for 32 sectors. Refer to the System Industries Disk Drive User's Guide for drives sector information.

## 4.6 Index and Sector Signal Configuration

The controller requires the continuous presence of drive index/sector signals on the B-Cable. Refer to the System Industries Disk Drive User's Guide for correct drive configuration for continuous (nongated) index/sector signals on the B-Cable.

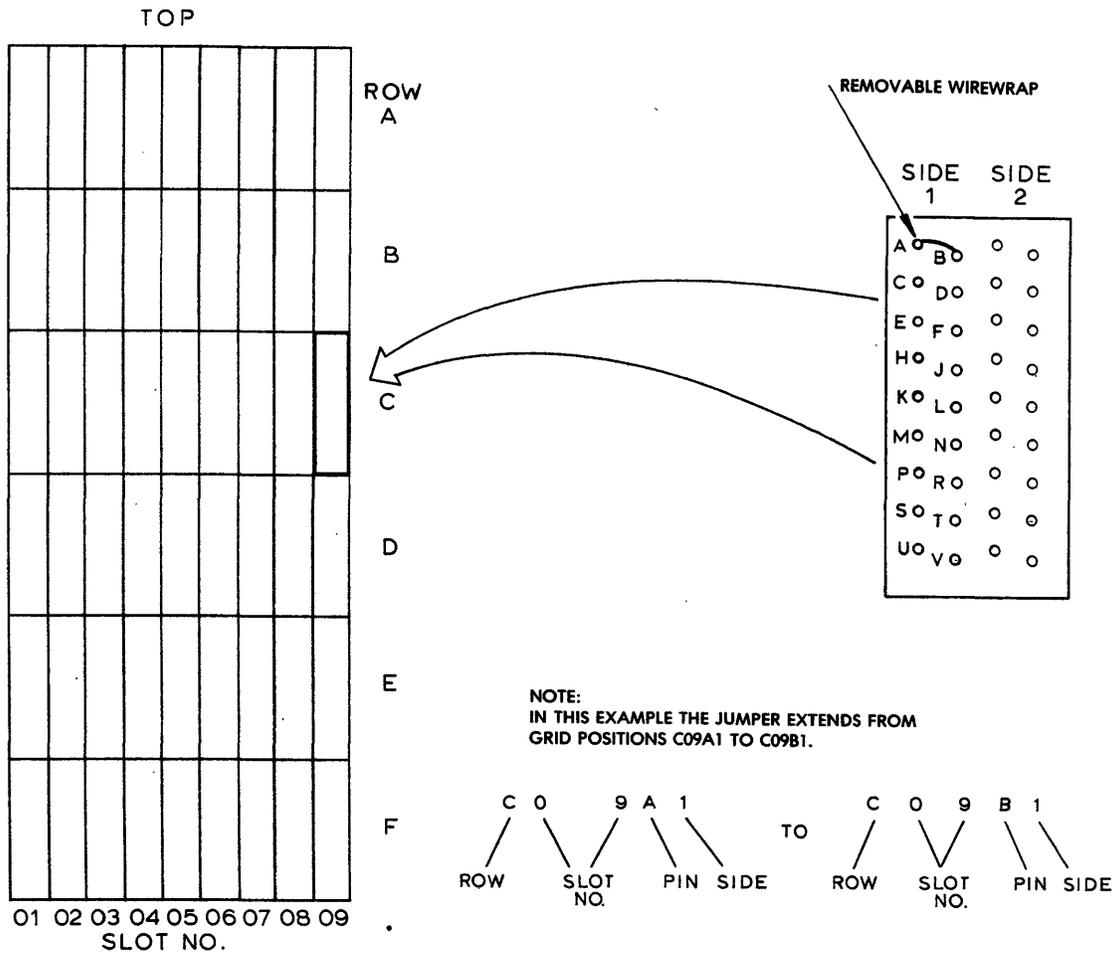


Figure 4-3. NPG Jumper Location

#### **4.7 Disk Drive Cabling**

Disk drives must be cabled correctly to insure proper transfer and retrieval of data. Figure 4-4 illustrates the correct placement of the A- and B-cables on the controller board. This subsection details the procedures necessary to connect System Industries drives in a daisy-chain configuration.

##### **NOTE**

When installing the cables, take care to ensure that pin one (1) on the controller is aligned through the cable(s) to pin one (1) on the drive(s).

In a daisy-chain configuration, each drive communicates to the controller through a discrete B-cable and a common A-cable. The A-cable is attached to connector J1. The free end of this cable is then attached to the first drive in the daisy-chain. One is connected between connector J2 on the controller board and the first drive in the daisy-chain. Additional B-cables are attached to the controller on connectors J3 through J5. The drive connected to J2 is designated as drive 0 and drives connected to J3 through J5 are designated as drives 1 through 3 respectively. The free end of each cable is attached to the disk drive as specified for each drive type.

##### **NOTE**

The total A-cable length must not exceed 100 feet and the maximum length of each B-cable must not exceed 50 feet.

Refer to System Industries Disk Drive User's Guide for cabling information for specific System Industries drives.

#### **4.8 Power-Up**

The system is now ready to be powered up. Refer to the PDP-11 Processor and System Industries Disk Drive manuals for exact power-up procedures.

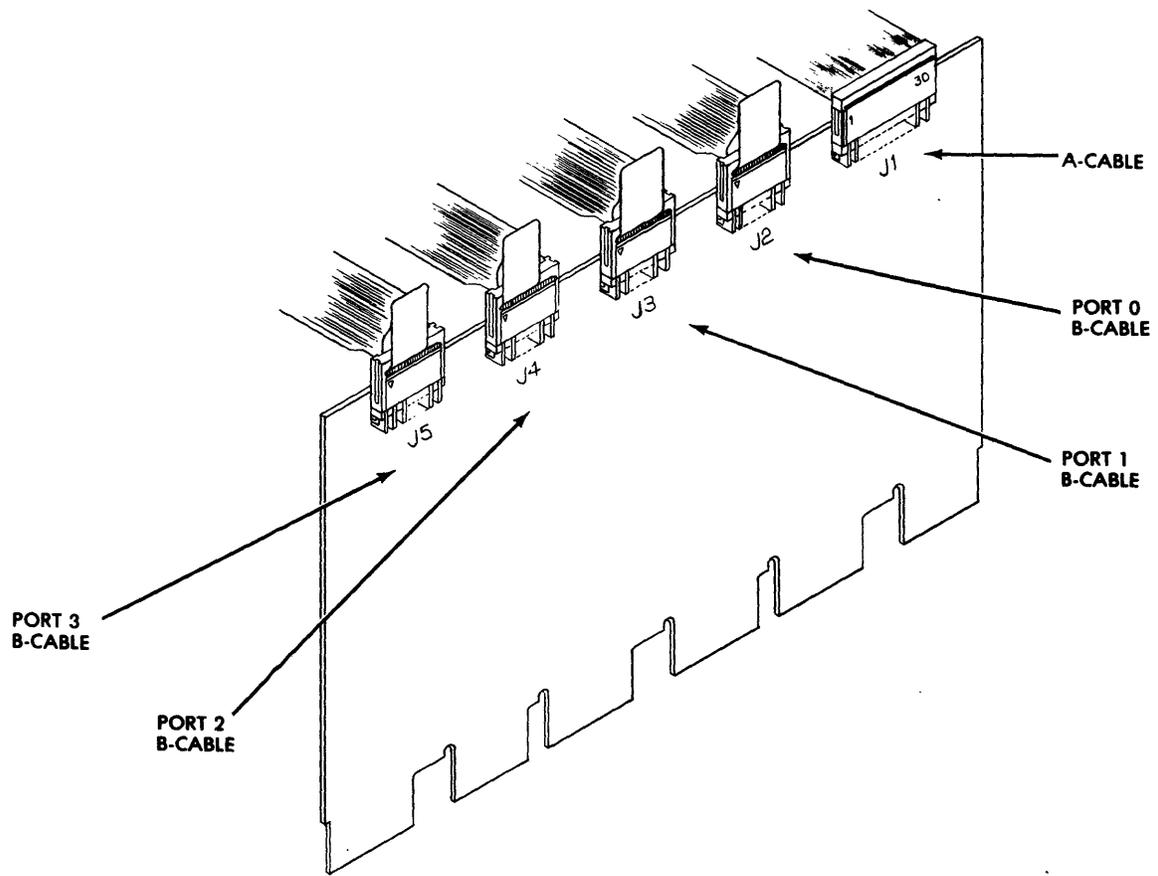


Figure 4-4. Controller Cable Placement

## 5.0 DIAGNOSTICS

The controller has internal diagnostics that are compatible with the DEC diagnostics listed in this section.

### 5.1 Internal Diagnostics

The controller contains in-PROM internal diagnostics. After power-up, the controller performs the following diagnostic tests:

1. Microprocessor self-test
2. Data RAM test
3. Register file test

During testing, the LED on the controller board is on. If the diagnostic tests indicate no failures, the controller turns the LED off. If there is a failure, the LED remains on, indicating a controller error.

### 5.2 System Industries Disk Exerciser

The System Industries disk exerciser program is EXOR11. This program is on a magnetic tape and is provided by System Industries with every 6100 Controller. When the program is loaded on the system, the title

TITLE JIMZAP — DISC EXERCISER V1.6  
EXOR11 6 - AUG - 1981

appears followed by the first program prompt. Possible prompts and responses are described in this section. The operator responds to the prompts by entering an octal number followed by a carriage return.

PROMPT	RESPONSE
FILL COUNT	10 for CRT, 0 or 2 for teletype (default is 4)
STATUS	Beginning address of status registers (default is 176700)
VECTOR	Interrupt vector number (default is 254)
ENTER TEST TO BE RUN	There are seven tests: bit 0 = format bit 1 = read entire disk bit 2 = read/write bit 3 = random read/write bit 4 = seek bit 5 = interrupt all tests = 77 (default is all tests)
ENTER PATTERN NUMBER	This prompt is printed only when read/write test is selected. There are five patterns: 0 = address of buffer location 1 = 133333 2 = 125252 3 = 177777 4 = 000000 (default is 0)

PROMPT	RESPONSE																											
ENTER RUN PARAMETERS	The run parameters are: bit 0 = short pass bit 1 = do not type errors bit 2 = format every pass bit 3 = halt on error bit 4 = loop on error bit 5 = do not type test names or pass numbers bit 6 = timeout switch (default is 0, format first pass and test all cylinders)																											
ENTER NUMBER OF CYLINDERS	This prompt is printed only when short pass is selected. Enter number of cylinders to test. (NO DEFAULT)																											
ENTER STARTING CYLINDER	This prompt is only printed when short pass is selected. Enter starting cylinder number. (NO DEFAULT)																											
DISKS TO TEST	There are seven possible units, enter the value number:  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Unit #</th> <th>Bit #</th> <th>Value</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>2</td></tr> <tr><td>2</td><td>2</td><td>4</td></tr> <tr><td>3</td><td>3</td><td>10</td></tr> <tr><td>4</td><td>4</td><td>20</td></tr> <tr><td>5</td><td>5</td><td>40</td></tr> <tr><td>6</td><td>6</td><td>100</td></tr> <tr><td>7</td><td>7</td><td>200</td></tr> </tbody> </table> (NO DEFAULT)	Unit #	Bit #	Value	0	0	1	1	1	2	2	2	4	3	3	10	4	4	20	5	5	40	6	6	100	7	7	200
Unit #	Bit #	Value																										
0	0	1																										
1	1	2																										
2	2	4																										
3	3	10																										
4	4	20																										
5	5	40																										
6	6	100																										
7	7	200																										

The operator always has control of the CPU from the console. The following commands are available.

- CTRL B = Boot (for boot options type "?")
- CTRL C = Restart at level 0
- CTRL D = Restart at level 0
- CTRL E = Restart at level 2
- CTRL F = Print cylinder, head, and sector
- CTRL H = Toggle halt on error
- CTRL L = Toggle loop on error
- CTRL N = Print current ECIB
- CTRL O = Toggle print error messages
- CTRL P = Print the ECIB table

CTRL Q = Proceed  
 CTRL R = Restart with same arguments  
 CTRL S = Halt  
 CTRL T = Toggle timeout flag  
 CTRL U = Toggle print pass number + test titles  
 CTRL X = Print all registers

#### RESTART ADDRESSES

1600 = Same as CTRL C  
 1604 = Same as CTRL R  
 1610 = Same as CTRL B

### 5.3 DEC Diagnostics

The controller is compatible with the following DEC formatters and diagnostics for 80 and 160 Mbyte (mapped) drives without modification:

PROGRAM NAME	EMULATION	DESCRIPTION
CZRMACO	RM03/RM02	Formatter
CZRMBBO	RM03/RM02	Performance Exerciser
CZRMECO	RM03/RM02	Functional Test 3, 2
CZRMFBO	RM03/RM02	Extended Drive Test
CZRMIBO	RM03/RM02	Drive Compatibility Test

The controller is compatible with the CZRMCB2 Functional Test 1 for RM03/RM02 with the following changes:

TEST	LOCATION	IS	CHANGE TO
11	12036	4	137
	12040	240	13110
36	24212	4	137
	24214	240	24776
41	26600	1007	407
53	32260	4	137
	32262	240	32646
61	35570	1406	406
64	37002	4	137
	37004	240	37362



## APPENDIX A

A register bit followed by an asterisk indicates a bit whose function differs from DEC definitions. Registers are referred to by their name and UNIBUS address.

### Control and Status 1 Register (RMCS1) (776700)

RMCS1 register is used to store the current disk command function code and operational status of the controller.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

Bit	Name	Type	Function
15	Special condition (SC)	Read only	Set when TRE or any drive ATA bit is set. Cleared by clearing the TRE or ATA conditions.
14	Transfer error (TRE)	Read/write	Set when one or more RMCS2 bits (08-15) are set, or a drive error occurs during a data transfer. Cleared by UNIBUS INIT, controller clear, loading a data transfer command with GO bit set, or by writing a 1 to this bit causing an error clear.
13*	MASSBUS control bus parity error (MCPE)	Read only	Set to 0 by controller.
12	Not used	—	Always read as 0.
11*	Drive available (DVA)	Read only	Set to 1 by controller.
10*	Port select (PSEL)	Read/write	Read/write for diagnostic purposes and has no effect on controller operation. Cleared by UNIBUS INIT, controller clear, or by writing a 0 in this bit.
09-08	A17-A16 UNIBUS address extension bits	Read/write	Upper extension bits of the RMBA register. Cleared by UNIBUS INIT, controller clear, or by writing 0 in these bit positions. Cannot be modified while controller is performing a data transfer.
07	Ready (RDY)	Read only	RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51-73) is written into RMCD1, RDY is reset. At the termination of the data transfer, RDY is set.

MASSBUS is a trademark of Digital Equipment Corporation.

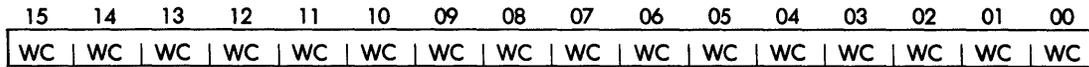
**RMCS1** (continued)

<b>Bits</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>					
06	Interrupt enable (IE)	Read/write	<p>IE is a control bit that can be set only under program control and enables an interrupt to occur when the following conditions are satisfied.</p> <ol style="list-style-type: none"> <li>1. Upon termination of a data transfer if IE is set when RDY becomes asserted.</li> <li>2. If SC, IE, and RDY are all asserted.</li> <li>3. If the program writes a 1 into IE and RDY at the same time.</li> </ol> <p>Cleared by UNIBUS INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.</p>					
05-01 00	F4-F0 and GO bit	Read/write	F4-F0 and the GO bit (00) are function (command) code control bits.					
	F4	F3	F2	F1	F0	GO	Octal	
	0	0	0	0	0	1	01	No operation
	0	0	0	1	0	1	05	Seek command
	0	0	0	1	1	1	07	Recalibrate
	0	0	1	0	0	1	11	Drive clear
	0	0	1	0	0	1	11	Drive clear
	0	0	1	0	1	1	13	Release (dual sort operation)
	0	0	1	1	0	1	15	Offset command
	0	0	1	1	1	1	17	Return to centerline
	0	1	0	0	0	1	21	Read-in preset
	0	1	0	0	1	1	23	Pack acknowledge
	0	1	1	0	0	1	31	Search command
	1	0	1	0	0	1	51	Write check data
	1	0	1	0	1	1	53	Write check header and data
	1	1	0	0	0	1	61	Write data
	1	1	0	0	1	1	63	Write header and data
	1	1	1	0	0	1	71	Read data
	1	1	1	0	1	1	73	Read header and data

The GO bit (RPCS1, bit 0) must be set to cause the controller to respond to a command. The GO bit is reset by the controller after command execution.

**Word Count Register (RMWC) (776702)**

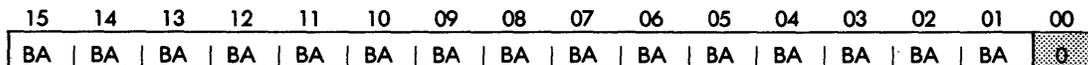
RMWC is the word count register. It is loaded by the program with the two's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 65,535 words can be transferred at one time.



Bit	Name	Type	Function
15-00	Word count (WC)	Read/write	Set by the program to specify the number of words to be transferred (two's complement form). Cleared only by writing zeros into all bits. RMWC is updated by the controller at the end of each complete sector transferred, or after each word of a sector of less than 256 words.

**UNIBUS Address Register (RMBA) (776704)**

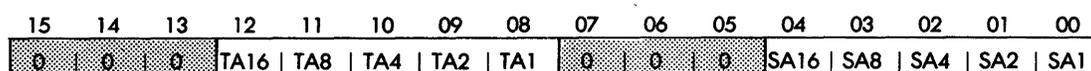
RMBA register is used to address the memory location in which a transfer is to take place. The RMBA register forms the lower 16 bits of the address that combine with bit-09 and bit-08 of the control register RMCS1 to create the 18-bit memory address. The register is loaded with the starting memory address by the program. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (bus address increment inhibit) bit (bit-03 of RMCS2) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address.



Bit	Name	Type	Function
15-01	UNIBUS address (BA)	Read/write	Loaded by the program to specify the memory address of a transfer. Cleared by UNIBUS INIT, or by controller clear. The RMBA register is incremented by 2 after each transfer of a word to or from memory.
0	Not used	—	Always read as 0.

**Disk Address Register (RMDA) (776706)**

RMDA register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the drive whose unit number appears in bits 00-02 of the status register RMCS2. Before a transfer, the RMDA register is loaded by the program with the address of the first block to be transferred. RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.



Bit	Name	Type	Function
15-13	Not used	Read/write	
12-08	Track address (TA)	Read/write	Set by the program to specify the track on which a transfer is to start. Cleared by read-in preset command. Updated by controller at the end of each sector.
07-05	Not used	Read/write	
04-00	Sector address (SA)	Read/write	Set by the program to specify the sector on which a transfer is to start. Cleared by read-in preset command. Updated by controller at the end of each sector.

**Control and Status 2 Register (RMCS2) (776710)**

RMCS2 register indicates the status of the controller and contains the drive unit number. The unit number specified in bits 00-02 of this register indicates which of the possible 4 physical or 8 logical drives is selected.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

Bit	Name	Type	Function
15*	Data late (DLT)	Read only	Set to 0 by controller.
14	Write check error (WCE)	Read only	Set when the controller is performing a write/check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set.  WCE causes TRE to be set. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCR bit is set. The memory address displayed in RPBA (and extension) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RPDB).
13	Parity error (UPE)	Read/write	Set if a UNIBUS parity error is detected during a write or write-check command. This bit may be set and cleared for diagnostic purposes by writing to it. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set.
12	Nonexistent drive (NED)	Read only	Set when the program reads or writes a register associated with a drive that does not exist, or is powered down. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. NED sets TRE.

**RMCS2** (continued)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
11	Nonexistent memory (NEM)	Read only	Set when the controller is performing a DMA transfer and the memory address specified in RPBA is nonexistent (does not respond to MSYN within 10 microseconds. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. NEM sets TRE. The RPBA contains the address+2 of the memory location causing the error.
10	Program error (PGE)	Read only	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. PGE sets TRE. The data transfer command code is inhibited from being written.
09	Missed transfer (MXF)	Read/write	Set if a data transfer command is loaded with ERR set in RMDS, or if DMA transfers between the UNIBUS and the controller's data buffer fail to complete. This bit may be set or cleared for diagnostic purposes by writing to it. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. MXF sets TRE.
08*	MASSBUS data bus parity error (MDPE)	Read only	Set to 0 by controller.
07	Output ready (OR)	Read only	Set by controller to indicate a word is in RPDB.
06*	Input ready (IR)	Read only	Set to 1 by controller.
05	Controller clear (CLR)	Write only	When a 1 is written into CLR bit, the controller and all drives are initialized. The following controller bits are cleared: RMCS1 bits 6, 8-10, 13-15, RMCS2 bits 0-5, 7-15, and RMBA. The following drive bits are cleared: RMER1, RMER2, RMCS1 bits 0-5, RMAS, RMEC2, and RMDS bits 14-15. A UNIBUS INIT command also causes controller clear to occur.

**RMCS2** (continued)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
04*	Parity test (PAT)	Read/write	PAT bit has no effect on 6100 operation. Cleared by UNIBUS INIT or controller clear.
03	UNIBUS address increment inhibit (BAI)	Read/write	When BAI is set, the controller will not increment the RMBA register during a data transfer. BAI bit cannot be modified while the controller is doing a data transfer (RDY negated).
02-00	Unit select (U2-U0)	Read/write	U2-U0 bits are written by the program to select a drive.  Cleared by UNIBUS INIT or controller clear.  The unit select bits can be changed by the program during data transfer operations without interfering with the transfer.

**Drive Status Register (RMDS) (776712)**

RMDS contains status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (00-02) of the RMCS2 register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	0	OM

Bit	Name	Type	Function
15	Attention active (ATA)	Read only	<p>An attention condition from a drive will set the ATA bit and the corresponding ATA summary bit in RPAS.</p> <p>ATA is cleared by UNIBUS INIT, controller clear, loading a command with the GO bit set, or, if no error conditions exists, writing a 1 in the RPAS register bit corresponding to the drive's unit number.</p> <p>An attention condition is caused by:</p> <ol style="list-style-type: none"> <li>1. any error in the error registers if               <ol style="list-style-type: none"> <li>a. GO bit set at completion of command,</li> <li>b. GO bit reset at occurrence of error</li> </ol> </li> <li>2. at completion of seek, search, recalibrate, offset or return to centerline</li> <li>3. MOL changes state.</li> </ol>
14	Error (ERR)	Read only	Set when either of the error registers RMER1 or RMER2 indicates a drive error. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing 0 in error registers.
13	Positioning in progress (PIP)	Read only	Set by drive when a positioning command is accepted. These commands are seek, offset, recalibrate, and search. The PIP bit is also set during implied seeks, mid-transfer seeks, and offset operations during a read. The bit is cleared when the function is completed.
12	Medium on-line (MOL)	Read only	Set for the drive upon the successful completion of the start-up cycle. Cleared when the drive is spun down or switched off. (This bit is set when unit-ready from the drive is asserted and cleared when it is deasserted.)

**RMDS** (continued)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
11	Write lock (WRL)	Read only	Set when last addressable sector on the disk pack has been tried or written.
10	Last block	Read only	Set when last addressable sector on the disk pack has been read or written.
09*	Programmable (PGM)	Read only	Set to 0 by controller.
08*	Drive present (DPR)	Read only	Set to 1 by controller.
07	Drive read (DRY)	Read only	Set at the completion of every command, data handling or mechanical motion.  Cleared at the initiation of a command.  If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the drive to accept a new command.  DRY is the complement of the GO bit except when the drive is nonexistent; then DRY is reset.
06	Volume valid (VV)	Read only	Set by the pack acknowledge or read-in preset command.  Cleared whenever drive cycles up from the OFF state and on controller power-up.  When reset, VV bit indicates drive went off-line then on-line, and a possible disk pack change.
05-01	Not used	-	Always read as 0.
00	Offset mode (OM)	Read only	Set when offset command is issued to drive. When set, and a read command is received, the offset is performed prior to the execution of the read.  Reset by any of the following actions: <ol style="list-style-type: none"> <li>1. Power-up</li> <li>2. Mid-transfer seek</li> <li>3. Read-in preset</li> <li>4. Write data or write header and data</li> <li>5. Return to centerline</li> <li>6. Write cylinder desired</li> <li>7. Recalibrate</li> </ol>

**Error Register #1 (RMER1) (776714)**

RMER1 contains the error status indicators for the drive whose unit number appears in bits 00-02 of the RMCS2 register. The logical OR of all the error bits in the RMER1 and RMER registers are written into bit 14 of the RMDS register.

Errors can be classified into two categories: Class A and Class B.

- Class A errors are handled at the completion of a non-data transfer command, or in the case of a data transfer command, at a sector boundary provided the run line is inactive.
- Class B errors cause the command to terminate immediately, or as soon as possible.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

Bit	Name	Type	Function
15	Data check (DCK)	Read/write	Set during a read operation when the ECC hardware has detected an ECC error after the ECC bytes have been looked at.  Cleared by a drive clear command, UNIBUS INIT, controller clear, or by writing 0 into the register.
14	Unsafe (UNS)	Read/write	Set when bit 7 (DVC) of RMER2 is set.  Cleared by drive clear, UNIBUS INIT, or controller clear.
13	Operation incomplete (OPI)	Read/write	Set if during a search or data transfer command the correct sector is not located.
12*	Drive timing error (DTE)	Read/write	Set to 0 by controller.
11	Write lock error (WLE)	Read/write	Set when the program attempts to issue a write command to a drive that has write-protect switch on.  Cleared by UNIBUS INIT, drive clear, controller clear, or by writing 0 into the register.
10	Invalid address error (IAE)	Read/write	Set when the address in the desired cylinder register (RMDC) or the disk address register (RMDA) is invalid and a seek, search or data transfer operation is initiated.

**RMER1** (continued)

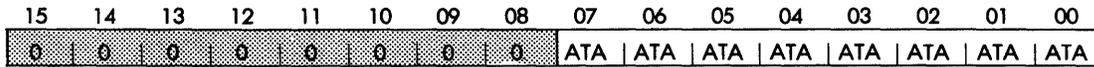
<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
09	Address overflow error (AOE)	Read/write	<p>Set when the desired cylinder register (RMDC) overflows during a read or write.</p> <p>Cleared by UNIBUS INIT, drive clear, controller clear, or by writing 0 into the register.</p> <p>Setting of this bit indicates that the desired cylinder address register has exceeded the maximum cylinder address.</p>
08	Header CRC error (HCRC)	Read/write	<p>Set if bit 10 (HCI) of RMOF is not set and the controller detects a CRC error in the header.</p> <p>Cleared by UNIBUS INIT, drive clear, controller clear or by writing 0 into the register.</p>
07	Header compare error (HCE)	Read/write	<p>Set if bit 10 (HCI) of RMOF is reset and one or more of the following occurs while reading the header:</p> <ol style="list-style-type: none"> <li>1. Bits 00-09 of the first header word do not match bits 00-09 of the desired cylinder address register (RMDC).</li> <li>2. Bits 10, 11, and 13 of the first header word are not zero.</li> <li>3. Bits 00-15 of the second header word do not match bits 00-15 of the desired track/sector register (RMDA).</li> </ol> <p>Cleared by UNIBUS INIT, drive clear, controller clear, or by writing 0 into the register.</p> <p>NOTE: Bits 14 and 15 must be set in the first header word or BSE will be set. Also, bit 12 of the first header word must be a 1 or FER will be set. However, these errors do not set HCE.</p>

**RMER1** (continued)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
06	ECC hard error (ECH)	Read/write	Set at the conclusion of the error correction procedure (bit 15 (DCK) of this register set and bit 11 (ECI) of RMOF not set), indicating that the error was an uncorrectable ECC error.  Cleared by UNIBUS INIT, drive clear, controller clear, or by writing 0 into the register.
05*	Write clock fail (WCF)	-	Set to 0 by controller.
04	Format error (FER)	Read/write	Set when reading a sector header if bit 10 (HCI) of RMOF is not set and bit 12 of the first header word is not set to a 1; or if bit 12 of RMOF is not set to a 1 and a data transfer command is executed.  NOTE: The controller words are in 16-bit word length mode only.  Cleared by drive clear, controller clear, UNIBUS INIT, or by writing 0 into the register.
03*	Parity error (PAR)	-	Set to 0 by controller.
02	Register modification refused (RMR)	Read/write	Set when a write is attempted to any drive register (except RMAS) while the GO bit is set.  Cleared by UNIBUS INIT, controller clear, drive clear, or by writing 0 into the register.
01*	Illegal register (ILR)	-	Set to 0 by controller.
00	Illegal function (ILF)	Read/write	Set when the function code in the control register is illegal and the GO bit is set.  Cleared by UNIBUS INIT, drive clear, controller clear, or by writing 0 into the register.

**Attention Summary Register (RMAS) (776716)**

RMAS allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in the RMDS register for the corresponding drive. When fewer than four drives are attached to the controller, the bits corresponding to the missing drives are always 0.



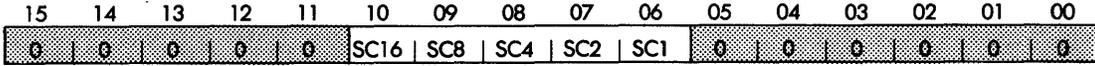
Bit	Name	Type	Function
15-08	Not used	-	Read as 0.
07-00	Attention active (ATA)	Read/write	Each ATA bit is set when the corresponding drive asserts its ATA bit.

All bits are cleared by UNIBUS INIT or controller clear. Individual bits are cleared by loading a function code with the GO bit set in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.

Each drive's ATA bit is displayed in bit 15 of RPDS. Each drive also responds in the bit position of RMAS register that corresponds to its unit number; e.g., drive 02 responds in bit position 02 of RMAS register.

**Look-ahead Register (RMLA) (776720)**

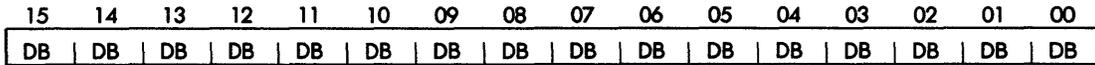
RMLA contains the count of the sector that is currently positioned under the heads. The value is represented as a binary number in bit locations 06-10, where bit 6 is the LSB. The maximum count for a 16-bit/word format is 31 and for an 18-bit/word format is 29.



Bit	Name	Type	Function
15-11	Not used	-	Read as 0.
10-06	Sector count (SC 1-16)	-	Set to correspond to the current sector count value. Reset by the index pulse.
05-00	Not used	-	Read as 0.

**Data Buffer Register (RMDB) (776722)**

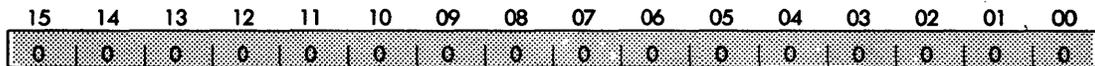
RMDB is used to monitor the data buffer and provide the bad data word as a result of a bad data compare operation.



Bit	Name	Type	Function
15-00*	Data buffer (DB)	Read/write	Contains the bad data word as the result of a data compare operation.

**Maintenance Register #1 (RMMR1) (776724)**

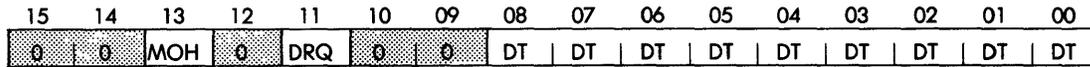
RMMR1 is not emulated.



Bit	Name	Type	Function
15-00	None	-	Set to 0 by controller.

**Drive Type Register (RMDT) (776726)**

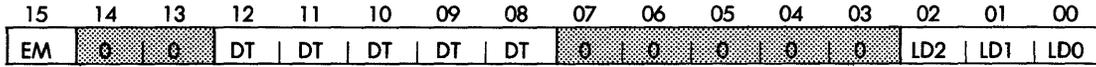
RMDT allows the program to distinguish between different classes of drives.



Bit	Name	Type	Function
15-14	Not used	-	Always read as 0.
13	Moving head (MOH)	Read only	Always read as 1, since drives are moving head devices.
12	Not used	-	Always read as 0.
11*	Drive request required (DRQ)	Read only	Set to 0 by controller.
10-09	Not used	-	Always read as 0.
08-00	Drive type (DT)	Read only	DT bits contain a number showing the drive type being emulated as set up by the switches on the controller (see RMSN).
	Drive Type		DT 08-00 (Octal)
	RM03		024 9762 disk drive - 80 Mbyte
	RM05		027 9766 disk drive - 300 Mbyte

**Serial Number Register (RMSN) (776730)**

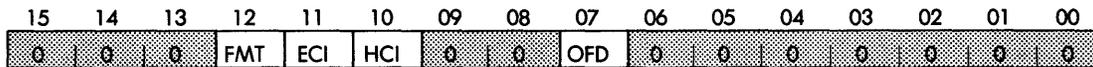
RMSN allows the program to identify the drives attached to the controller by providing a copy of the drive type switches and the drive port numbers.



Bit	Name	Type	Function
15	EM	-	0/1 = RM05/RM03 emulation.
14-13	Not used	-	Always read as 0.
12-08	DT	-	Drive type defined as: 0 0001 80 Mbyte drive 0 0011 300 Mbyte drive 0 1011 160 Mbyte drive 0 1101 160 Mbyte drive (mapped) 0 1110 675 Mbyte drive (mapped)
			NOTE: Other codes reserved.
07-03	Not used	-	Always read as 0.
02-00*	Drive Number		LD0-LD2 bits contain the logical drive number (0-7)

**Offset Register (RMOF) (776732)**

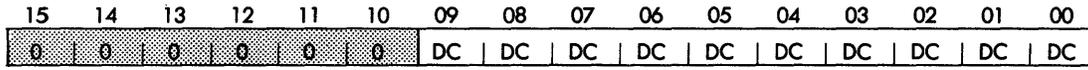
RMOF contains the positioner offsetting information supplied to the drive directly by the software operating system prior to issuance of the offset command. The drive has the ability to offset the positioner approximately 200 micro-inches from the track centerline in either direction.



Bit	Name	Type	Function
15-13	Not used	-	Always read as 0.
12*	Format (FMT)	Read/write	FMT bit must be set to a 1 by the program to use the controller for data transfer commands. When reading a header from the disk, the recorded bit is compared with this setting (i.e., compared with 1). If the bits do not compare, bit 4 of RMER1 (FER) is set.  Cleared by read-in preset or by writing a 0 to this bit.
11	Error correction inhibit (ECI)	Read/write	Set by program to inhibit error correction when an ECC error is detected.  Cleared by read-in preset command or by writing a 0 to this bit.
10	Header compare inhibit (HCI)	Read/write	Set by program to inhibit the reporting of header compare errors FER, BSE, HCE, and HCRC in RMER1.  Cleared by read-in preset command or by writing a 0 to this bit.
09-08	Not used	-	Always read as 0.
07	Offset direction (OFD)	Read/write	Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle.  The offset direction bit is valid if the following three conditions are met: 1. Read command is loaded into bits 0-5 of control register (RMCS1). 2. RMCS1 GO bit is set. 3. The offset mode bit (RMDS bit 00) is set.  Cleared by the same conditions that clear the OM bit (see RMDS), or by writing a 0 to this bit.
06-00	Not used	-	Always read as 0.

**Desired Cylinder Register (RMDC) (776734)**

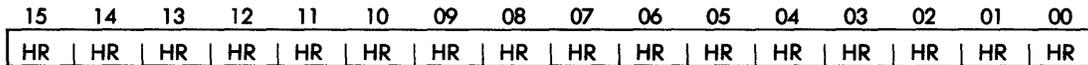
RMDC contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command.



Bit	Name	Type	Function
15-10*	Not used	-	Always read as 0.
09-00	Desired cylinder (DC)	Read/write	Set by the program to specify the required cylinder address. Cleared by read-in preset command. The IAE bit in RMER1 will be set if, when asserting the GO bit for a data transfer, seek or search command, this register contains an address larger than the maximum cylinder address on the drive.

**Holding Register (RMHR) (776736)**

RMHR provides no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading from this register, the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.



Bit	Name	Type	Function
15-00	Holding register (HR)	Read/write	<p>This register is used only by diagnostic software.</p> <p>When writing to this register, all bits remain unchanged and new information is lost.</p> <p>When reading this register, the complement of the register contents is read.</p> <p>When writing to any other drive register, this holding register is also written.</p> <p>When reading from any other drive register, the complement of the data is written to this holding register.</p>

**Maintenance Register #3 (RMMR2) (776740)**

RMMR2 register is not emulated by the 6100 and is preset by the controller to 11777 octal.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1

Bit	Name	Type	Function
15-00*	None	Read only	Set to 11777 (octal) by controller.

**Error Register #2 (RMER2) (776742)**

RMER2 contains detailed error status information and is primarily used for monitoring the electro-mechanical performance of the drive rather than the interface. All unsafe errors, with the exception of read/write unsafes, cause the drive to retract heads from the pack area; prevent a head load from occurring; de-elect all heads; and disable the read, write, recalibrate, seek, and offset commands.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0

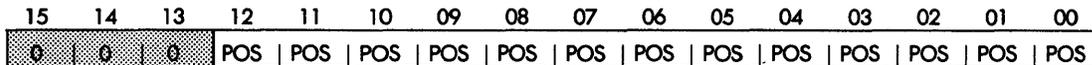
Bit	Name	Type	Function
15	Bad sector error (BSE)	Read/write	Set whenever the controller detects a 0 in bit 14 or 15 of the first header word and the HCI bit in RMOF is zero. Cleared by drive clear, UNIBUS INIT, controller clear, or by writing 0's to this register.
14	Seek incomplete (SKI)	Read/write	Set when a seek error occurs in the drive.
13*	Operator plug error (OPE)	-	Set to 0 by controller.
12	Invalid command (IVC)	Read/write	Set if either VV or MOL is not set (RMDS bits 6 and 12), and ERR (RMDS bit 14) is not set, and any command other than read-in preset, pack acknowledge, drive clear or NO-OP is received.
11*	Loss of system clock (LSC)	-	Set to 0 by controller.

**(RMER2)** (continued)

<b>Bit</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
10	Loss of bit clock (LBC)	Read/write	Set when a loss of the drive bit clock is detected. (The bit clock is derived from the read and servo clocks.)
09-08	Not used	-	Always read as 0.
07	Device check (DVC)	Read/write	Set when the drive fault line from the drive is asserted. This bit also sets bit 14 (UNS) in RMER1.  Cleared by drive clear, UNIBUS INIT, controller clear, or by writing 0's to this register.
06-04	Not used	-	Always read as 0.
03*	Data parity error (DPE)	-	Set to 0 by controller.
02-00	Not used	-	Always read as 0.

**ECC Position Register (RMEC1) (776744)**

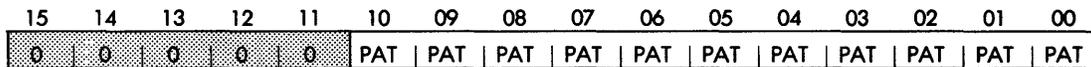
RMEC1 contains the exact location of an error burst within a field, following the completion of the error correction procedure. The drives have error correction code capabilities that detect and correct errors by reconstructing a portion of data. In the specified code word length, the ECC code corrects an error that fails within an 11-bit burst. Any errors outside the specified burst length are detected but not corrected. The ECC hardware, in this case, yields an ECC uncorrectable error. The drive logic contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.



Bit	Name	Type	Function
15-13	Not used	-	Always read as 0.
12-00	Position (POS)	Read only	Set by the ECC logic if a data check error occurred and the error is considered to be correctable (bit 6 of RMER1 is not set). These bits represent the binary address of the right-most bit of the error pattern in RMEC2, counting from the first data bit in the sector. (Note that the first data bit of the sector has a position address of 1 not 0.) If bit 6 (ECH) of RMER1 is set, or if bit 11 (ECI) of RMOF is set, the contents of this register are irrelevant.

**ECC Pattern Register (RMEC2) (776746)**

RMEC2 contains the actual error burst and the ECC position register (RMEC1) contains the address that determines the actual location of the error burst within the data field.



Bit	Name	Type	Function
15-11	Not used	-	Always read as 0.
10-00	Pattern (PAT)	-	<p>Set by the ECC logic if the detected error is correctable. The 11 pattern bits establish the error burst, where a 1 in the error pattern indicates a bit of the data in memory which is in error. The position of the least significant bit of the error pattern is determined by RMEC1.</p> <p>If bit 6 (ECH) of RMER1 is set, or if bit 11 (ECI) of RMOF is set, the contents of this register are irrelevant.</p> <p>Cleared by UNIBUS INIT, controller clear, or drive clear.</p>

## APPENDIX B

### Control and Status 1 Register (RMCS1) (776700)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A1	RDY	IE	F4	F3	F2	F1	F0	GO

### Word Count Register (RMWC) (776702)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC															

### UNIBUS Address Register (RMBA) (776704)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	0														

### Disk Address Register (RMDA) (776706)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	TA16	TA8	TA4	TA2	TA1	0	0	0	SA16	SA8	SA4	SA2	SA1

### Control and Status 2 Register (RMCS2) (776710)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

### Drive Status Register (RMDS) (776712)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	0	OM

### Error Register #1 (RMER1) (776714)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

**Attention Summary Register (RMAS) (776716)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA							

**Look-ahead Register (RMLA) (776720)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	SC16	SC8	SC4	SC2	SC1	0	0	0	0	0	0

**Data Buffer Register (RMDB) (776722)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB															

**Maintenance Register #1 (RMMR1) (776724)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Drive Type Register (RMDT) (776726)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DRQ	0	0	DT								

**Serial Number Register (RMSN) (776730)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EM	0	0	DT	DT	DT	DT	DT	0	0	0	0	0	LD2	LD1	LD0

**Offset Register (RMOF) (776732)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT	ECI	HCI	0	0	OFD	0	0	0	0	0	0	0

**Desired Cylinder Register (RMDC) (776734)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	DC									

**Holding Register (RMHR) (776736)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
HR															

**Maintenance Register #3 (RMMR2) (776740)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1

**Error Register #2 (RMER2) (776742)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0

**ECC Position Register (RMEC1) (176744)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	POS												

**ECC Pattern Register (RMEC2) (176746)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	PAT										



## **WARNING**

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the User's Guide, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case, the user, at his own expense, will be required to take whatever measures may be required to correct the interference.



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