REVISIONS					
EFFECTIVITY	AUTH	LTR	DESCRIPTION	DATE	APPROVED

CHANGE ACTIVITY PENDING, YES ☐ NO ☐

REV																										
SHEET	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
REV		B	B	B				B			B	B	B	B					B	B	B			B			
SHEET	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52
REV STATUS	REV							B	B					B	B						B						
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

UNLESS OTHERWISE SPECIFIED	CONTRACT NO.		
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH: .X = .1 .XX = .03 .XXX = .010 ANGLES = 0° 30'	SIGNATURE	DATE	**Telefile**
	DRAWN		
	CHECK		TITLE
	ENGR. BJP	9-30-77	T3281 Controller
	PROJ. ENGR. BJP	9-30-77	
DO NOT SCALE DRAWING	QUAL. ASSURANCE		SIZE: A — CODE IDENT NO.: 51360 — SPEC. NO.: SS-600-0064-1B
	RELIABILITY		
MATERIAL:	PROD. DESIGN		SCALE — REV — SHEET 1 OF 51
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1.0 SCOPE

This document describes the functional characteristics of the TELEFILE model T3281 controller. The controller is designed to provide a software transparent interface between Xerox Sigma series CPU I/O processors and a variety of high capacity disk drives. In addition, the controller is designed to provide the capability of assigning to the controller some of the functions presently performed by CPU software.

2.0 APPLICABLE REFERENCE DOCUMENTS

2.1	XDS 900973	XDS Sigma Computer Systems Interface Design Manual
2.2	XDS 903079A	Xerox Removable Disk Storage System Models 7275/7276
2.3	SS-600-0050-1A	Microprocessor Control Board Product Specification
2.4	SS-600-0051-1A	Writeable Control Store Product Specification
2.5	SS-600-0052-1A	Quad Port Data Buffer Product Specification
2.6	SS-600-0053-1A	Serializer/Deserializer/ECC Product Specification
2.7	SS-600-0054-1A	Data Encoder/Decoder Product Specification
2.8	SS-600-0055-1A	T3286 Disk Drive Interface Product Specification
2.9	SS-600-0056-1A	T328X Disk Drive Interface Product Specification
2.10	SS-600-0057-1A	T7902 Product Specification
2.11	SS-600-0058-1A	IFX/7902 Product Specification
2.12	SS-600-0059-1A	Processor Maintenance Panel Product Specification
2.13	SS-600-0060-1A	Tape Formatter Interface Product Specification - 6250 BPI
2.14	SS-600-0061-1A	Tape Formatter Interface Product Specification - 800/1600 BPI
2.15	SS-600-0062-1A	T3281/T3289 Interface Product Specification
2.16	SS-600-0063-1A	T3289 DASU Product Specification
2.17	SS-730-0002-1A	T7300 Series Magnetic Tape Controller Product Specification

3.0 GENERAL

3.1 GENERAL DESCRIPTION

The T3281 controller is a microprogrammable device designed to supply the required control and timing functions to interface a variety of disk drives to Xerox Sigma series CPUs. The controller design incorporates a writeable control store for

microprogram storage and the ability to interface to devices other than disk drives. These functions provide for additional capabilities of the T3281 beyond that of a disk controller. Features of the T3281 are described in the following paragraphs.

3.1.1 Software Transparency

The T3281 is programmed to emulate the Xerox 7275 disk controller whose characteristics are described in Reference 2.2. The order set, status bytes and other programming considerations for the T3281 are described in Section 4.0. Existing operational software for the Xerox 7275 will run on the T3281 when the system parameters have been adjusted for the number of sectors, heads and cylinders pertinent to the disk drives attached (3.2). The T3281 does not implement all the test modes of the Xerox 7275 and consequently will not run all of the existing diagnostic programs for the 7275. Diagnostic tests will be supplied by Telefile which will perform equivalent functional tests in a non test mode environment.

3.1.2 Micro Diagnostics

Diagnostic programs will be stored on a mini flexible disk and will be usable by the customer engineer to functionally test the controller and disk drives. Diagnostics may be run in-line with CPU operation on a time slice basis.

3.1.3 Error Correction

The T3281 will have the capability of correcting errors in data read from the disk drives. The correction algorithm implemented will correct any error burst not exceeding eleven bits in length. Correction of data, when in effect, will be transparent to the CPU/IOP. Data read from the disk will be buffered, inspected for error, and corrected if necessary prior to transmission to the IOP.

3.1.4 Error Detection

Besides the error detection and correction on the serial disk data described in 3.1.2 and the normal disk system error checks described in Section 4.0, error checks are incorporated on data paths throughout the controller. These include:

1. parity checks on writeable control store
2. CRC checks on mini disk data
3. parity checks on microprocessor I/O paths
4. parity checks on disk drive control interface where the attached device permits
5. single bit correction and multiple bit error detection on internal data buffer
6. parity checks on IOP data paths to the extent permitted by the connected IOP
7. parity checks on data serializer/deserializer.

3.1.5 Error Logging

Disk system errors may be stored in controller memory (3.1.10) or can be permanently recorded on a mini flexible disk. The controller provides the capability of allowing the CPU to read the contents of either disk error log (4.2.2.5, and 4.2.2.7).

3.1.6 Dual/Quad System Interfaces

All disk drives attachable to the T3281 have optional dual port features. Dual port systems with two host CPUs sharing the disk drives may be configured with the drives attached directly to the T3281 as illustrated in Figure 3-1. By using the T3289 Dual Access Switch Unit (2.16), quad port systems may be configured with four CPUs sharing the disk drives as illustrated in Figure 3-2. The T3281 controller will permit operation in single, dual or quad port system configuration without change to its basic microcode.

3.1.7 Disk Drive Intermix

The disk drives which may be attached to the T3281 are summarized in Section 3.2. The controller will support any combination of these drive types. The type of drive will be identified by functions contained on its interface module (3.3). When a drive is selected for operation, the controller microcode will obtain the drive type information from the interface module and automatically adjust to the address parameters, control protocol and timing requirements for the specified drive type.

3.1.8 Magnetic Tape Interface

The T3281 is designed to provide for an optional interface to magnetic tape drives (3.4). This interface may be added to the controller at any time by adding circuit cards, a tape formatter, and changing the microcode program disks. With this option installed, the controller has the capability of transferring data stored on the disks to magnetic tape either offline or online with respect to the CPU. When the transfer occurs online the controller time required will only be that necessary to read the data from the disk and buffer it. The controller is then returned to operation with the CPU and the transfer to the tape is controlled by the auxiliary processor. The data block size transferrable in one operation is dependent on the capacity of the data buffer in the controller (3.1.10).

3.1.9 Disk to Disk Transfer

The controller has the capability of providing disk to disk transfer (4.2.2.6). The transfer may be initiated by the CPU software, be accomplished offline with respect to the CPU or controlled by the auxiliary processor if the tape interface option (3.4) is installed.

3.1.10 Data Buffer

The controller incorporates a data buffer having a nominal capacity of 32KB and is expandable to 128KB in 32KB increments. This buffer permits connection of the T3281 to any Xerox Sigma series I/O processor and facilitates disk to disk and disk to tape data transfer without involving the I/O processor. Single bit error correction and multiple bit error detection are employed in the buffer hardware to insure the integrity of the data transmitted through it to the devices or I/O processor.

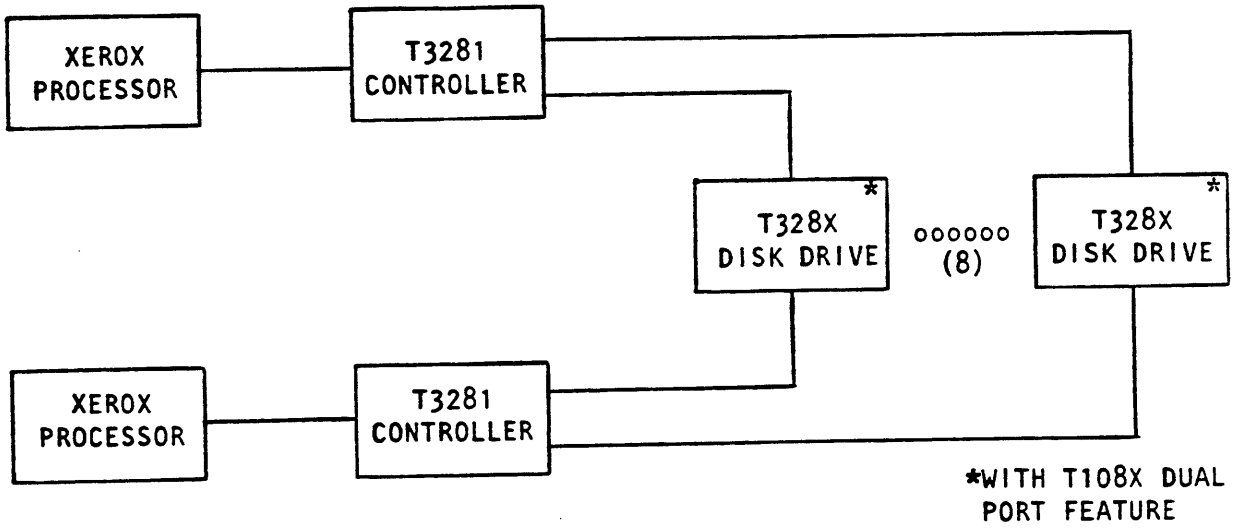

Figure 3-1. Dual Port System

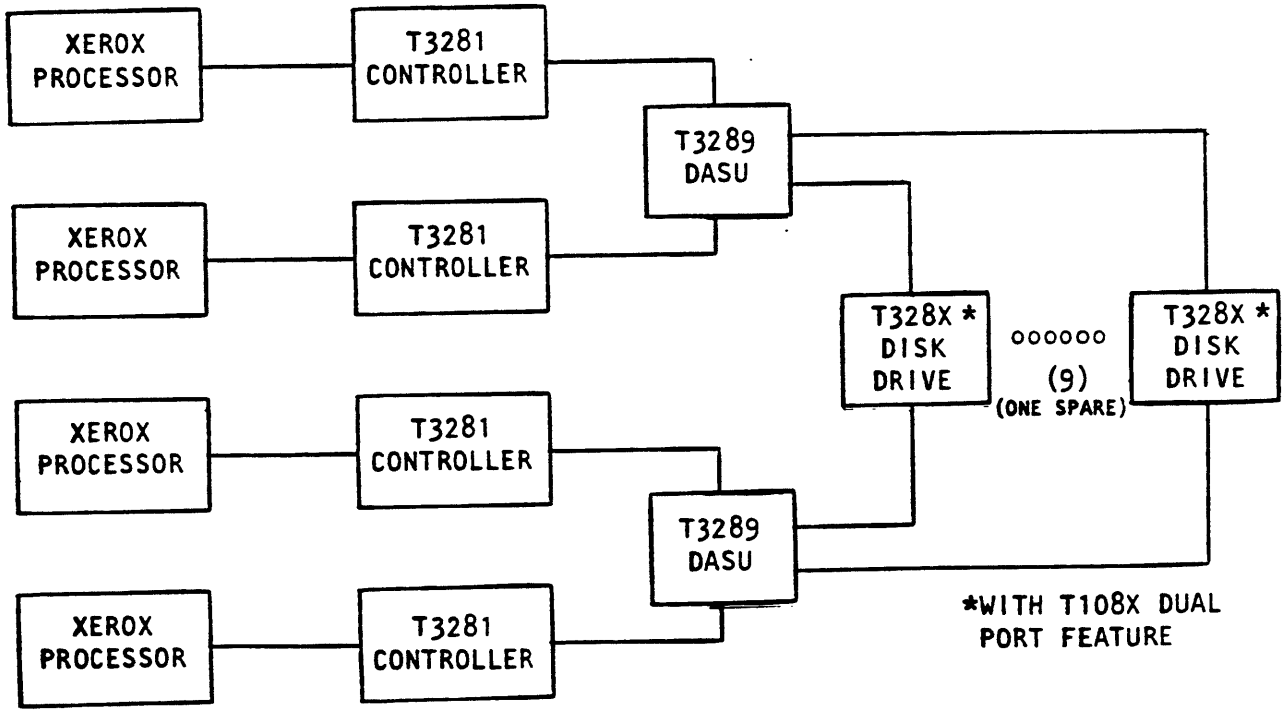

Figure 3-2. Quad Port System

	SIZE	CODE IDENT NO.	SPEC. NO.
Figure 3-1. Dual Port System Figure 3-2. Quad Port System	A	51360	SS-600-0064-1B
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3.2 DISK DRIVE SUMMARY

The T3281 controller will interface to a variety of disk drives in any mixture. The characteristics of these drives are summarized in Table 3-1. The drives are connected to the controller in a radial configuration with each drive having its own circuit interface, control and data cables (Figure 3-3). This electrical isolation permits maintenance on a drive or complete power down of a drive without any effect on any other drive.

3.3 CONTROLLER BLOCK DIAGRAM

The block diagram for the basic T3281 controller is shown in Figure 3-3. The components of the controller are briefly described in the following paragraphs.

3.3.1 Processor

The processor function used in the controller is a microcomputer designed for control purposes. The microcomputer features control oriented instructions which directly access variable length input/output and internal data fields. These instructions provide very high performance for moving and interpreting data. The microcomputer features:

1. 300 nanosecond instruction execution time
2. direct address capability up to 8192 twenty-five bit words of program memory
3. eight 8-bit general purpose registers
4. simultaneous data transfer and data edit in a single instruction cycle time
5. n way branch or n entry table lookup in two instruction cycle times
6. instructions operate on variable one-bit to eight-bit data formats in single instruction cycle time.

The microcomputer is the control element in the T3281 and will provide all control functions except those disk and IOP control and data functions whose required timing is equal to or less than three microcomputer cycle times. The microcomputer, for example, will not be involved in data transfer between the disk and the IOP except in an enabling and monitoring capacity. All data transfer related functions will be accomplished by wired logic.

Reference 2.3 provides a detailed description of the functional characteristics of the microcomputer and auxiliary functions contained on the processor module.

3.3.2 Writeable Control Store

The writeable control store (WCS) contains 8192 words of random access storage. Word length is 25 bits. The WCS is program storage only and may not be written into during normal program execution. All scratch pad operation is done in working storage contained on the processor module. The contents of the WCS are loaded during an initial program load (IPL) phase initiated by powering up the controller. During this time the microcomputer program is being executed from read only memory. On completion of the IPL function the microcomputer program will branch to WCS and further execution will be from there. Functional characteristics of the WCS are described in Reference 2.4.

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CHARACTERISTIC	DISK DRIVE TYPE			
	T3282	T3283	T3288	T3286
Capacity, (Moving Head) Bytes	174,423,040	269,562,880	71,546,880	272,906,540 289,963,200 983,040
Capacity, (Fixed Head) Bytes	-	-	-	1,044,480
Sectors/Head	11	17	17	(17) = 16 ONLY
Heads/Cyl	19	19	5	30
Cylinders	815	815	822	555
Data Rate	806 KB	1.209 MB	1.209 MB	1.198 MB
Rotation Speed	3600 RPM	3600 RPM	3600 RPM	3600 RPM
Access Times:				
Maximum	50 MS	50 MS	55 MS	50 MS
Average	28.5 MS	28.5 MS	30 MS	25 MS
Cylinder	7.0 MS	7.0 MS	10 MS	10 MS
Latency	8.33 MS	8.33 MS	8.33 MS	8.33 MS
Width	22 IN	19.25 IN	17.25 IN	44.5 IN
Depth	32 IN	34.0 IN	30.0 IN	32.0 IN
Height	47 IN	38.0 IN	38.0 IN	46.0 IN
Weight	550 LBS	550 LBS	190 LBS	980 LBS
Heat Dissipation	4450 BTU/HR	4450 BTU/HR	2500 BTU/HR	7100 BTU/HR
AC Power	208/230,3Ø 60HZ,30AMPS 1.2 KVA	208/230,3Ø 60HZ,30AMPS 1.2 KVA	115/220,1Ø 60HZ,12AMPS 0.8 KVA	208/230,3Ø 60HZ,60AMPS 2.3 KVA

Table 3-1. Disk Drive Characteristics

SIZE	CODE IDENT NO.	SPEC. NO.
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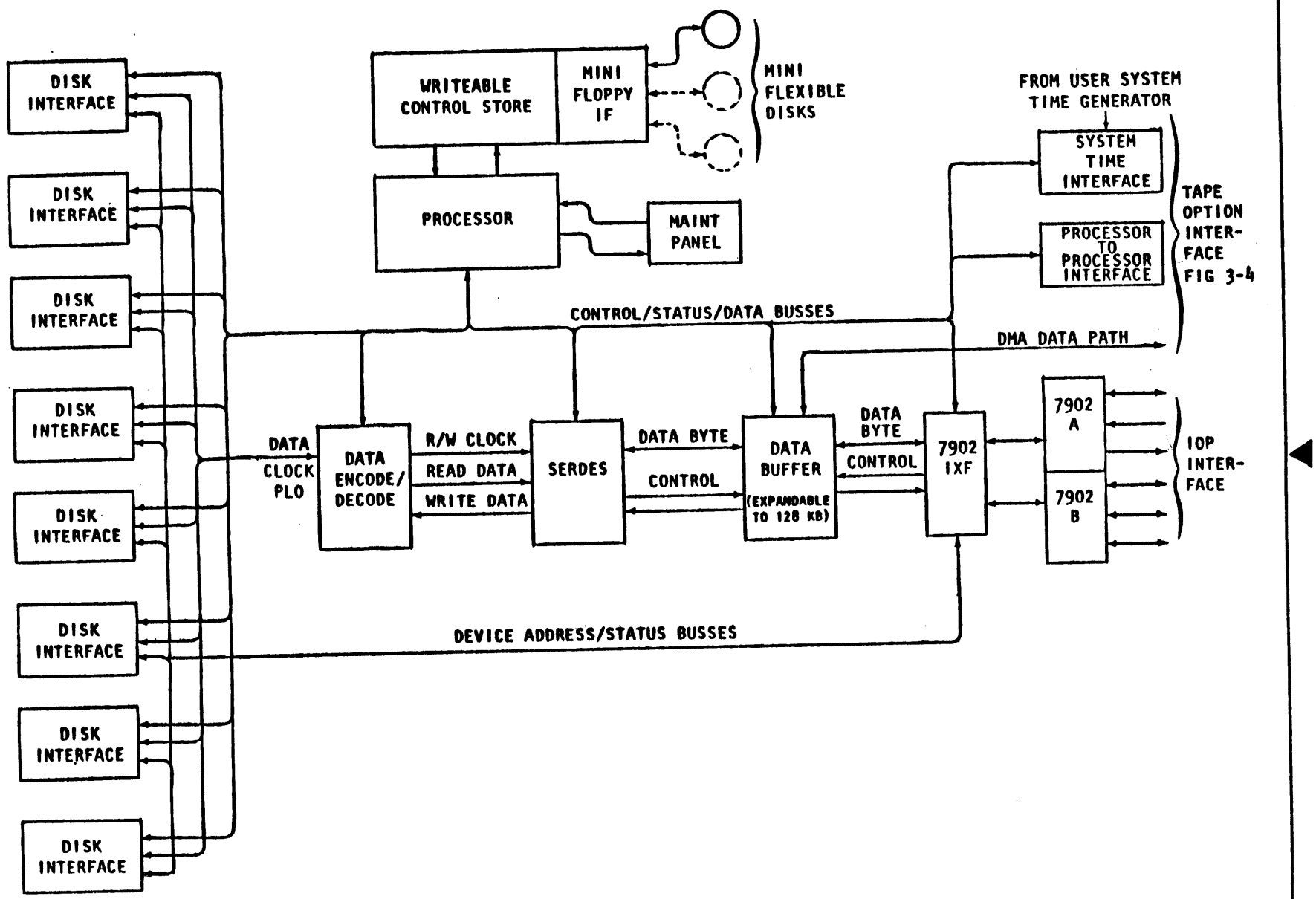

Figure 3-3. T3281 Controller

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3.3.3 Mini Flexible Disk (Floppy) Interface

This interface consists of a minimal set of hardware to provide adapting the microcomputer I/O system to the mini floppy interface and to provide data encoding and decoding functions. All other control and data generation functions are provided by microcomputer programs. Characteristics of this interface are described in Reference 2.4. The interface is capable of attaching to three mini flexible disks.

3.3.4 Mini Flexible Disk (Floppy)

The mini floppy disks provide permanent storage of controller operational programs and storage for logging of controller operational error status. Two disk drives will be required in the system if error logging is to be accomplished since writing will not normally be permitted on the primary program storage device.

Characteristics of the mini floppy disk drive are described below:

Recording method:	double frequency
Recording density:	2581 BPI (inner track) 1768 BPI (outer track)
Track density:	48 tracks per inch
Number of tracks:	40
Sectors per track:	one
Data transfer rate:	15.625 KB
Data capacity:	125K bytes
Rotational speed:	300 RPM ± 1%
Width:	5.75 inches
Height:	3.25 inches
Depth:	7.95 inches
Weight:	3.0 pounds

Write protection of the disk is accomplished by a photoelectric sensor which detects the presense or absense of a slot in the diskette which indicates a read only diskette. A line on the interface informs the processor program of a write protect condition.

3.3.5 Disk Interface

The disk interface provides hardware for interfacing the disk drive to the processor, the data transfer system, and to the IOP interface. The functions provided on the interface are:

1. receivers and drivers for the disk control and data lines
2. registers to hold control information generated by the processor
3. parity checking of the disk interface when implemented in the disk drive
4. sector counter, modifier bit store and sector window associated with on-sector interrupts
5. status bus to transmit disk drive status to the IOP interface when the drive is selected by I/O instructions generated by the host CPU
6. programmable (switch) functions to define the drive type and track characteristics.

Two drive interface module types will be available in the controller. One is peculiar to the T3286 drive, the other is pertinent to all other drive types shown in Section 3.2. The functional characteristics of these interface modules are described in Reference 2.8 and 2.9.

3.3.6 Data Encoder/Decoder

This module provides functions necessary for interfacing the NRZ data input/output of the serializer/deserializer to drives which require MFM data format. The module produces the clock to be used by the disk data system in the controller. Functions provided by the module include:

1. variable frequency oscillator
2. crystal controlled oscillator
3. data system clock source
4. MFM data decoding
5. MFM data encoding
6. missing data check circuitry
7. clock check circuitry

Characteristics of this module are described in Reference 2.7.

3.3.7 SERDES

This module provides functions pertinent to the transmission of data between the IOP and the disk. These include:

1. serialization of IOP data
2. deserialization of disk data
3. generation of error correction (check) bytes to be written on the disk
4. generation of error correction information for data read from the disk
5. synchronization of controller to disk read data
6. insertion of error burst in disk data to test properties of error correction algorithm.

Reference 2.6 describes the functional characteristics of this module.

3.3.8 Data Buffer

The data buffer provides a random access memory for buffering data transmitted between disk and other devices. The basic module contains 32KB of storage and has four DMA type data ports to provide data transmission paths between:

1. buffer and SERDES
2. buffer and IOP interface
3. buffer and tape interface
4. buffer and microprocessor

In addition, a data control path is provided to allow the processor to establish necessary control and address functions and to change and monitor the buffer contents. The data buffer capacity can be expanded in 32KB increments to a maximum of 128KB by adding modules. Characteristics of the basic data buffer module are described in Reference 2.5.

3.3.9 IOP Interface (7902)

The controller will interface to the Xerox IOP via two circuit modules which implement the functions of the Xerox 7902 Extended Device Subcontroller. The interface modules will contain a four-byte wide data interface and will meet protocol and timing requirements for the IOP interface as defined in Reference 2.1. Connection of the controller to the IOP will be via six Xerox ET10 cables. Functional characteristics of the 7902 modules are described in Reference 2.10.

3.3.10 IFX/7902 (7902 Adapter)

The IFX/7902 provides an adapter between the 7902 modules and the processor and data buffer in the controller. It provides:

1. control of data transmission between the 7902 and the data buffer
2. registers to hold status bytes set up by the processor
3. device selection and status response on I/O instructions generated by the Xerox CPU
4. monitoring of 7902 status by the processor
5. monitoring by the processor of order byte received from IOP
6. control by the processor of interrupt and order in calls

The functional characteristics of the IFX/7902 are described in detail in Reference 2.11.

3.3.11 Processor to Processor Interface

This function provides an interface between the I/O system of the primary processor in the controller and the I/O system of the auxiliary processor that is added to the controller when the magnetic tape interface option (3.4) is installed. This interface will permit the processors to transfer control and status information bilaterally in order to implement online or offline disk to tape data transfer. Characteristics of this interface are described in Reference 2.3.

3.3.12 System Time Interface

This interface allows the processor to monitor a set of up to 48 lines generated by a central system time function.

3.3.13 Maintenance Panel

The maintenance panel supplied with the T3281 controller allows the operator to observe, modify and control the execution of the microprogram running in the processor. The panel will allow the operator to:

1. display address, instruction and control busses in the processor
2. set program breakpoint on address
3. enter instructions or data from the panel
4. halt, single step or alter the program from the panel
5. start program execution from any address
6. set program loops
7. set program breakpoint on processor I/O address or data busses
8. call up and execute discrete diagnostic programs stored on a CE mini disk
9. observe results of CE test via status display
10. execute initial program load of writeable control store (identical to initial power up of controller)

The characteristics and functions of the individual switches and displays contained on the maintenance panel are described in Reference 2.12.

3.4 TAPE INTERFACE BLOCK DIAGRAM

The block diagram for the magnetic tape interface option is shown in Figure 3-4. The T3281 controller is designed to permit installation of either 800/1600 BPI or 6250 BPI tape systems in any combination. A maximum of two tape systems may be installed. The configuration shown, since it contains its own processor independent of that required for control of the disk drives, would allow disk to tape transfer to be accomplished on line with the Xerox CPU with minimum impact on the throughput of data between the IOP and the disks.

The auxiliary processor/writeable control store/mini flexible disk combination is identical to the functions described in Sections 3.3.1 through 3.3.4. The auxiliary processor controls and monitors the operation of the tape drives via the tape formatter interface. The processor will not be involved in tape data transfer in other than an enabling and monitoring capacity. Data transfer between the tape formatter interface and the data buffer in the controller will be controlled by wired logic.

The auxiliary processor communicates with the primary processor in the controller via the processor to processor interface described in 3.3.11. Control, address and status information required for acquisition of data from the disk will be transferred between the processors. If on line disk to tape transfer has been initiated, an order received from the IOP will be accepted and stacked for the time necessary to acquire the data from the disk and buffer it. The auxiliary processor will then control transfer of the data from the data buffer to the tape. Simultaneously, the IOP order can be processed by the primary processor in the controller.

The auxiliary processor monitors and controls the serial interface in order to receive commands or data from an operator console or send status or data to an operator console. The serial interface is RS232-C compatible and contains a universal asynchronous receiver/transmitter which is compatible with a wide range of baud rates and character sets. Provisions will be made for switching between two operator consoles. Characteristics of the serial interface are described in Reference 2.3.

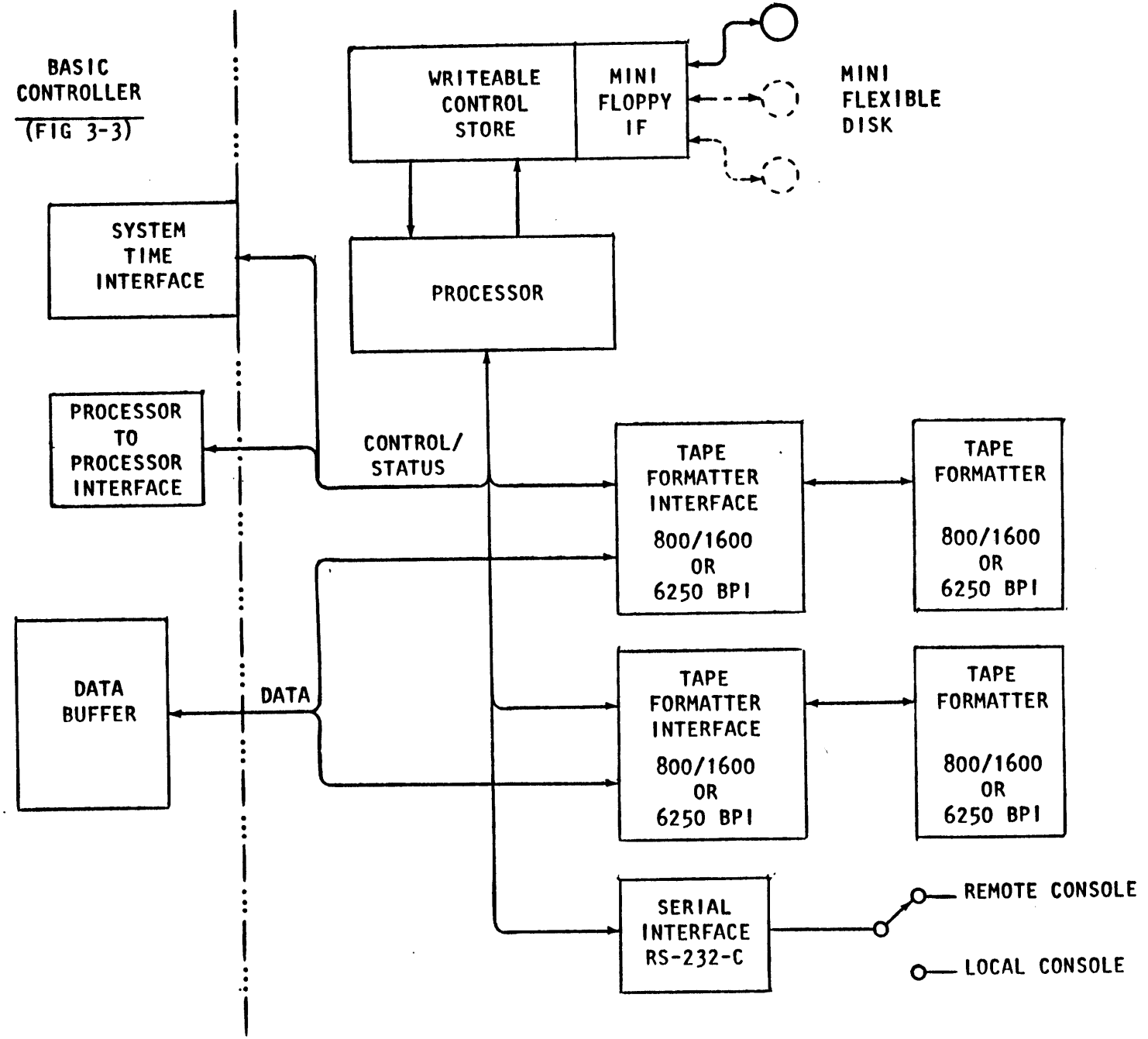

Figure 3-4. Tape Interface Option (Maximum Configuration)

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The tape formatter interface adapts the processor I/O system to the interface lines of the tape formatter for control and monitoring purposes and provides control of data transfer from the data buffer to the formatter. Two interfaces are provided, one for the 6250 BPI formatter and the other for the 800/1600 BPI formatter. The functional characteristics of these interfaces are described in Reference 2.13 and 2.14 respectively.

The tape formatters supply all control, data encoding and decoding, and error detection and correction functions necessary for reading and writing data on the magnetic tape. Their characteristics are defined in Reference 2.13 and 2.14.

Direct communication between the magnetic tape system and the Xerox Sigma IOP will be enabled by providing a second controller I/O address in addition to that described in 4.1.2 for the disk drives. Using this I/O address the T3281 will accept I/O commands, respond to device orders and present device status as a T7300 Magnetic Tape Controller. The functional characteristics of the T7300 are described in Reference 2.17.

This technique provides software transparent communication between the optional magnetic tape drives on the T3281 and the Xerox CPU IOP. The tape drives and the disk drives may not be operated simultaneously by the IOP.

4.0 PROGRAM INTERFACE

The following paragraphs describe the program interface between the T3281 controller and the Xerox Sigma CPU software.

4.1 GENERAL DESCRIPTION

4.1.1 I/O Commands

The controller will accept and respond to standard input/output commands:

1. Start Input/Output (SIO) - selects device and starts an input/output operation
2. Halt Input/Output (HIO) - selects device and halts an input/output operation
3. Test Input/Output (TIO) - selects device and returns status
4. Test Device (TDV) - selects device and returns status pertinent to device and last controller operation
5. Acknowledge Input/Output (AIO) - used to acknowledge I/O interrupts

4.1.2 Device Address

To select a device for any operation, the I/O instruction must contain an address specifying the device controller address and the device address. The T3281 is a multidevice controller; consequently, the controller address lies in the range 8_{16} through F_{16}, and device addresses in the range 0_{16} through E_{16}. Note that device address F_{16} is for the controller and can be used for any I/O instruction intended for the controller alone (SIO, HIO, TIO, and TDV).

For the fixed head option on the T3286 drive, two address techniques will be provided. The fixed head option may be addressed as separate devices with the device address differing only in the most significant bit from that of the movable head module on which it is installed, i.e. fixed head device addresses would lie in the range 8_{16} through E_{16}. This will limit the number of fixed head options installed to seven.

The second technique would treat all fixed head options as one integral fixed head disk, with one device address assigned. The processor would translate the address received during a Seek order to locate the proper sector on the proper disk drive.

4.1.3 Disk Pack Organization

4.1.3.1 Disk Pack Data Addressing

The T3281 is capable of interfacing to a variety of disk drives. The controller will, when addressing a drive, interrogate its interface module to determine the drive type and adjust its internal program to the required address range (sectors, head, cylinder) and the control timing requirements for the specific drive. This permits mixing different drive types on a single controller.

The address ranges for the drives which can be interfaced to the T3281 are tabulated in the following (decimal):

DRIVE	CYLINDER FIELD	HEAD FIELD	SECTOR FIELD
T3282	0-814	0-18	0-10
T3283	0-814	0-18	0-16
T3286	0-554	0-29	0-16
T3286	Fixed Head	0-59	0-16
T3288	0-821	0-4	0-16

0-15
0-15

4.1.3.2 Disk Pack Data Organization

Data is stored in groups of 1024 bytes. Each data group has a unique address composed of its device, cylinder, head, and sector number. Each data group is preceded by a header (4.1.3.3) containing the cylinder, head, and sector number for the group. The header is used for address identification and verification.

4.1.3.3 Headers

Before data can be written on the disk, special records called headers that identify the addresses of all data groups (sectors) must be written. The header data received from the IOP (see "Header Write (X'09')", 4.2.1.2) comprises a flaw byte; head, sector and cylinder addresses; and alternate head and cylinder addresses.

Headers are used in locating the desired data group (sector) and in address verification when successive data groups are written or read. Failure to acquire a given address results in a verification error. When the program detects a flawed track, it must write a flaw mark (X'FF') in the flaw byte in all sector headers of the track. A defective or flawed track is one in which an error has been consistently detected on successive write and then read operations. When the controller detects a flaw mark in a header, it terminates any read or write operation by indicating "unusual end". Note that the current sector address is not incremented for any unusual termination while the header is being read. Therefore, the alternate head and cylinder addresses are normally obtained from the "flawed header" by issuing a Header Read order (4.2.1.5) directly after the flaw is encountered. A new Seek order is not required in this case.

4.1.3.4 Check Characters

The controller computes and writes a seven byte check character at the end of each header and at the end of each sector data field. The algorithm used to generate these characters has error correcting properties permitting the use of the residue remaining in the generator after the check characters have been read, to be used in correcting an error burst of up to eleven bits in length occurring in the serial data stream read from the disk.

When a header is read, the controller recomputes the check characters and compares them with those read from the disk. Any difference causes one of the following:

1. if the header is being verified during a READ, WRITE, or CHECK WRITE order, an "unusual end" termination will occur.
2. if the header is being read during a HEADER READ or SENSE order, the data will be corrected prior to transmission to the IOP. If the data error is uncorrectable, then an "unusual end" termination will occur with the proper status bits set.

When the data area of the sector is read, the controller also recomputes the check characters and compares them with those read from the disk. If any difference occurs, the data, which has been buffered in the controller, will be corrected prior to transmission to the IOP. If the data is uncorrectable, the controller signals "transmission error" and not "unusual end" at termination.

4.1.3.5 Disk Address Update

Sector and head addresses are automatically incremented after a surface operation (Read, Write, etc.). The cylinder address is never automatically incremented. The program must issue a Seek order to cross cylinder boundaries to prevent an "unusual end" condition.

When the controller detects a flaw mark during a surface operation, automatic address incrementation is inhibited to allow for an immediate Header Read operation to obtain the alternate address.

4.1.3.6 CE Test Cylinder

Disk drives such as the T3286, which have non-removable media will have the last cylinder reserved for test purposes. When the drive is being operated in CE service mode, test operations may only occur on this cylinder.

4.2 DEVICE ORDERS

When the controller successfully completes the execution of an SIO instruction or a command chain, it makes a one-byte order-out service call to the IOP to obtain the I/O order for the next operation.

4.2.1 Basic Device Orders

The T3281 controller will implement a basic set of device orders which will duplicate the Xerox 7275 controller functions. The following list and subsequent description depicts this set of orders. Any other code, in this mode of operation, is treated as an invalid order, as is a detected order parity error, and terminates with "unusual end". Note that all orders to device address X'F' (except in a Condition Release Interrupt order or a Select Test Mode order) are rejected.

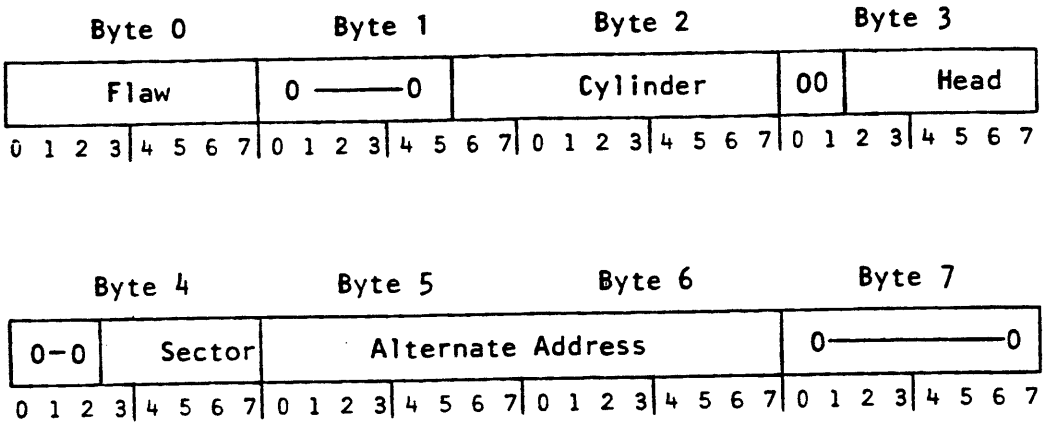
Order	Binary Representation Bit Positions 0	1	2	3	4	5	6	7	Hexadecimal Code
Header Write	0	0	0	0	1	0	0	1	X'09'
Seek	M	0	0	0	0	0	1	1	X'83',X'03'
Write	0	0	0	0	0	0	0	1	X'01'
Check-Write	0	0	0	0	0	1	0	1	X'05'
Header Read	0	0	0	0	1	0	1	0	X'0A'
Read 1	0	0	0	1	0	0	1	0	X'12'
Read 2	0	0	0	0	0	0	1	0	X'02'
Restore Carriage	M	0	1	1	0	0	1	1	X'B3',X'33'
Reserve	0	0	0	0	0	1	1	1	X'07'
Release	0	0	0	1	0	1	1	1	X'17'
Condition Release Interrupt	0	0	0	M	1	1	1	1	X'1F',X'0F'
Select Test Mode	0	0	0	1	0	0	1	1	X'13'
Sense	0	0	0	0	0	1	0	0	X'04'

The "M" represents a modifier bit that, when set, has specific meaning for any order in which it can appear.

4.2.1.1 Header Write X'09'

This order will be used to write the address area, or header of each sector on the disk pack. On reception of the order, the controller will request data to be transmitted from the IOP and will consider all subsequent data bytes as header information.

Header size is eight bytes. The header format is defined as follows:



where:

flaw - represents flaw byte and is written with all ones (X'FF') in every sector header of a track in which a flaw is detected. If there are no flaws, the flaw byte contains all zeros.

cylinder - represents current cylinder address.

head - represents current head address.

sector - represents current sector address.

alternate address - represents a field normally used to contain the address of an alternate cylinder and head to be used should this sector be marked flawed. (Set by software only.)

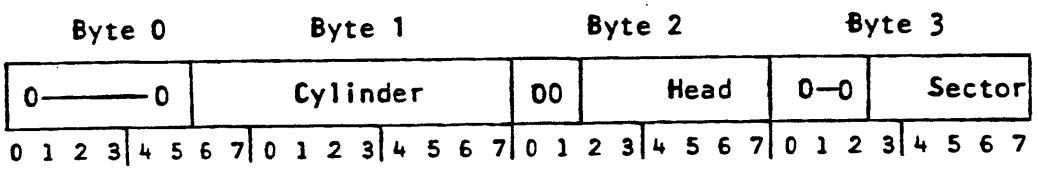
A single Header Write order can write a maximum of one cylinder of headers. Header writing continues until terminated by one of the following conditions:

1. "Count done" is signaled.
2. The device becomes "not operational". The Header Write terminates with an "unusual end".
3. The address increments to an out-of-bounds address; the head number is past the end of the cylinder. The programming error (bit 2) status of TDV is indicated and the Header Write is terminated with "unusual end".
4. A rate error (data overrun) is detected. The operation terminates with a "transmission error".
5. I/O Reset occurs or an HIO instruction is executed. The Header Write terminates without further communication to the IOP.

6. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" in the order-in and proceeds to the "ready" state. If the terminal order indicating IOP Halt occurs at the order-in, the controller proceeds to the "ready" state without further communication with the IOP.
7. An output data parity error is detected from the IOP. The Header Write is immediately terminated with a "transmission error".
8. A write-protect signal is received from the device. The Header Write terminates with an "unusual end".

4.2.1.2 Seek (X'83', X'03')

The Seek order causes the controller to request a four-byte disk address from the IOP, as illustrated below. The controller then directs any subsequent data transmission operation to begin at this address.



where:

cylinder - represents cylinder number and can be in the range 0≤cylinder≤ (4.1.3.1)

head - represents head number and can be in the range 0≤head≤ (4.1.3.1)

sector - represents sector number and can be in the range 0≤sector≤ (4.1.3.1)

Both seek forward and seek reverse operations are possible. The difference between any seek and successive seek is stored in bytes 14 and 15 of the data retrievable from the execution of a Sense order (4.2.1.12).

A byte count of less than four causes the controller to signal "incorrect length" in the appropriate status byte for the I/O instruction, without completing the Seek operation. If the byte count exceeds four, the Seek operation is performed using the first four bytes transferred; however, "incorrect length" is still signaled. In either case, an "unusual end" termination occurs.

When bit 0 (modifier bit) of the Seek order is set (X'83'), a device interrupt is initiated when the positioning system indicates positioning is complete (on-cylinder) or a Seek timeout error (i.e., positioning error--heads are retracted to sector zero) has occurred. The interrupt call is made at the beginning of the sector prior to the one specified by the Seek operation. If the call is not acknowledged before the beginning of the next sector, it is withdrawn until the next revolution of the disk.

The receipt of an SIO, HIO, TIO, or TDV instruction for another device causes the interrupt call to be withdrawn temporarily. However, if the controller is "busy" when the device signal is received, the interrupt call to the IOP is postponed until the controller is not "busy".

Seek orders can be issued successively to several devices, and each device will interrupt as it completes its operation. After the controller has sent the last communication to the device to initiate the Seek operation, it executes order-in to the IOP, and proceeds to the "ready" state. The device then stays "busy" until the heads are in position, even though it is not selected by the controller.

4.2.1.3 Write (X'01')

The Write order causes the controller to begin writing data on the file at the current disk (file) address. Note that if the specified byte count to be written is not a multiple of the sector record length, "incorrect length" is indicated and writing does continue with the remaining bytes of the sector written with zeros. Writing begins only after the header is read and the address verified, and continues until terminated by any of the conditions listed below:

1. Count done is signaled coincident with "end-of-sector" (i.e., after writing a record on a sector).
2. Count done was received, the remainder of the sector was written with zeros, and the check characters were written.
3. I/O Reset occurs or an HIO instruction is executed. Writing terminates and the controller immediately becomes "ready", without further communication with the IOP.
4. A terminal order indicating IOP Halt occurs in the order-in sequence; the controller becomes "ready" without further communication with the IOP.
5. An output data parity error is detected from the IOP; the operation terminates with "transmission error".
6. A data overrun is detected; the operation terminates with "transmission error".
7. The disk system becomes "not operational"; termination indicates "unusual end".
8. The controller head address increments past the end of the cylinder. The sector "unavailable" status bit (bit 2 of TDV status) is set to 1, and termination indicates "unusual end".
9. A header flaw mark, incorrect header parity, or a verification error is encountered. The current sector address is preserved (is not incremented). Termination indicates "unusual end".
10. A write-protect signal is received from the device; termination indicates "unusual end".
11. A terminal order indicating IOP Halt occurred before order-in; the controller indicates "unusual end" in the order-in and becomes "ready".

4.2.1.4 Check-Write (X'05')

The Check-Write order causes the controller to compare bytes read from disk storage with bytes received from the IOP. Check-write errors terminate the operation with "transmission error" at the completion of the sector. Note that if the byte count is not a multiple of the sector length, "incorrect length" is indicated.

The comparison continues until terminated by one of the following conditions:

1. Count done signal is received.
2. The disk pack system becomes "not operational". Check-writing terminates with an "unusual end" indication.
3. The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder.
4. A rate error is detected; check-writing terminates with a "transmission error".
5. Data bytes do not compare or an error is encountered in the data check character. The order-in indicates "transmission error".
6. I/O Reset occurs or an HIO instruction is executed. Check-writing terminates and the controller proceeds immediately to "ready" without further communication with the IOP.
7. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" in the order-in, and proceeds to "ready". If the terminal order indicating IOP Halt occurs within or after the order-in sequence, the controller proceeds to "ready" without further communication with the IOP.
8. The controller encounters a flaw mark or incorrect header parity in a header, or a verification error. The current disk (file) address is preserved (is not incremented).
9. The controller detects an IOP output parity error.
10. An output data parity error is detected from the IOP; the operation terminates with "transmission error".

4.2.1.5 Header Read (X'0A')

The Header Read order causes the controller to start reading headers beginning at the current disk address. The byte count must specify a multiple of the header record length (multiple of eight bytes). A maximum of one cylinder of headers may be read with one order. This maximum number is defined in 3.2 for the various devices attachable to the controller.

The Header Read continues until terminated by one of the following conditions:

1. Count done signal is received.
2. The device becomes "not operational". The Header Read terminates with an "unusual end" indication.
3. The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder. The illegal address fault (in byte 8, obtained with a Sense order) is indicated, and the Header Read operation terminates with "unusual end".
4. A rate error is detected. The Header Read operation terminates with "transmission error".
5. I/O Reset occurs or an HIO instruction is executed. Header Read terminates without further communication to the IOP.

6. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs before the order-in, the controller indicates "unusual end" in the order-in and proceeds to the "ready" state. If the terminal order indicating IOP HALT occurs at the order-in, the controller becomes ready without further communication with the IOP.
7. Detection of either a verification error or a header parity error terminates the operation with "unusual end" after the current record ("errored" header) has been transferred to the IOP with the current sector address preserved. Error correction will always be applied to the header data prior to transmission to the IOP. Any "unusual end" with header parity error status (TDV 7) will indicate that the data error is uncorrectable.
8. Detection of a flaw mark sets bit 1 of the TDV device status byte and reading continues.

4.2.1.6 Read 1 (X'12')

The Read 1 order causes the controller to begin reading bytes from the disk storage at the current disk address stored in the controller and to transmit the bytes to the IOP. Data read from the disk will be buffered and error correction applied at the end of the sector if necessary. Any data errors reported will be errors which are uncorrectable. Such errors will be reported as "transmission errors" and the order will terminate at the end of the sector in which the error occurred. "Incorrect length" is set in the operational status byte if the byte count is not a multiple of the sector record length (1024 bytes).

Prior to reading data from the sector and sending it to the IOP, the controller verifies the disk address by reading headers until it locates the one with the requested sector number. If a flaw mark is detected in any header, if a check byte error is detected, or if cylinder, sector, or head numbers do not compare with those stored in registers, then an "unusual end" occurs and no data is read. The pertinent TDV status bits are set to indicate a flaw mark, header check byte error, or verification error (see Table 4-3).

Reading is initiated at the start of the addressed sector and is continued until any of the following occur:

1. Count done signal is received coincident with the end of the sector and the check character has been read and compared.
2. Count done signal is received prior to the end of the sector. The controller reads the remaining bytes (but does not transmit them to the IOP), and reads and compares the check characters.
3. The disk pack system becomes "not operational". Reading terminates with an "unusual end".
4. The address increments to an out-of-bounds address; the incremented controller head number is past the end of the cylinder.
5. A rate error (data overrun) is detected. Reading terminates with a "transmission error".

6. The controller encounters a check character that does not successfully compare and the error correction process cannot correct the data to be transmitted to the IOP. Termination occurs at the end of the sector in error (for the Read 1 order described in this section , or is deferred until the count done signal is received, as described below for Read 2). At read termination, "transmission error" and not "unusual end" is set in the appropriate status byte for the I/O instruction.
7. I/O Reset occurs or an HIO instruction is executed. Reading terminates and the controller proceeds immediately to "ready" without further communication with the IOP.
8. IOP Halt is indicated to the controller. If the terminal order indicating IOP Halt occurs prior to the order-in, the controller indicates "unusual end" for the order-in and proceeds to "ready" without further communication with the IOP.
9. A verification error is encountered. The read operation is terminated with "unusual end", and the current file address is preserved (is not incremented).
10. The controller encounters a flaw mark or incorrect header parity in a header. The read operation is terminated with "unusual end" and the file address is not incremented.

4.2.1.7 Read 2 (X'02')

The Read 2 order causes the controller to read and transmit bytes to the IOP from the disk storage at the current disk address in the controller. Sector data check byte errors ("transmission error") are reported following the sector in which count done occurs. Otherwise, the operation is exactly as described in the previous section, "Read 1 (X'12')".

4.2.1.8 Restore Carriage (X'B3', X'33')

The Restore Carriage order causes the controller to issue return-to-zero signal to the addressed device; it is generally used when the exact location of the carriage becomes unknown. Internal registers are cleared, the heads are returned to cylinder zero, and no data bytes are transferred. An interrupt call is made at the beginning of the sector prior to sector zero if the order modifier bit is set (i.e., order code is X'B3'). A device interrupt is initiated when positioning is complete (4.5.2.4).

4.2.1.9 Reserve (X'07')

For a single-CPU system, the Reserve order causes the controller to select and reserve the designated device and then to release it. For a dual-CPU system, this order causes the responsible controller to select and reserve the designated device. Because an SIO instruction and all orders cause the controller to automatically select and reserve a device, the use of the Reserve order is superfluous. (See also "Multiple Access Considerations" in Section 4.6).

4.2.1.10 Release (X'17')

The release order causes the controller to issue a release control signal to the addressed dual access device, thereby releasing that device for use by the other controller. If the device has only a single access capability (i.e., remains reserved to channel A), the controller still executes the Release order; however, no useful operation results. (See also "Multiple Access Considerations" in Section 4.6.)

4.2.1.11 Condition Release Interrupt (X'1F, X'0F')

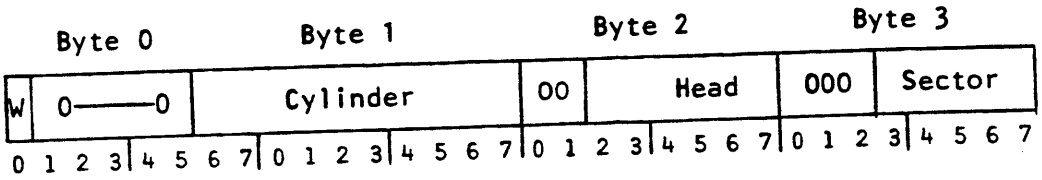
The Condition Release Interrupt order is meaningful only for dual access systems. When a controller receives a "released" signal (which means the other controller has released the device), a device interrupt occurs. If the order modifier bit is set (i.e., order code is X'1F') the controller makes an interrupt request (CIL) if it receives a "released" signal from any device. If the modifier bit is not set (X'0F'), a controller does not generate any release interrupts.

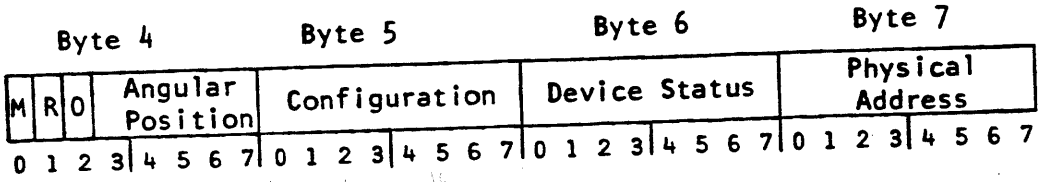
The program must use SIO device address X'F' to initiate this order, thereby permitting the Condition Release Interrupt mark in the controller to be set even if all devices are busy.

An HIO instruction with device address X'F' resets the release interrupt mark and any pending release interrupts. A reset signal received from the IOP, or an AIO, also resets the release interrupt mark.

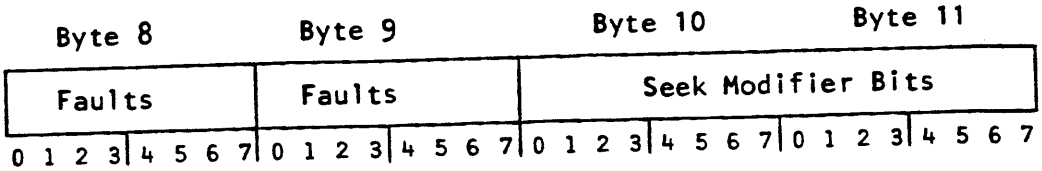
4.2.1.12 Sense (X'04')

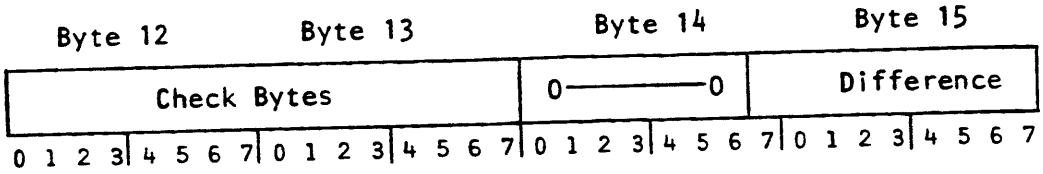
The Sense order causes the controller to transfer to the IOP up to 16 bytes of information that describe the controller's and device's current state. The sense orders are timed to be initiated at the start of a sector. This feature provides that approximately the time of one sector period elapses before the start of the next sector after the current angular position (sector position) is transferred to the IOP. The 16 bytes are described as follows:





SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0064-1B
SCALE	REV.	SHEET 27 OF





where:

W - represents write-protect bit. If set, this bit indicates the current address is write-protected.

cylinder - represents current ten-bit cylinder address stored in the device.

head - represents current head address stored in the device.

sector - represents current sector address stored in the device.

M - represents modifier bit. This bit is set when the arm is in motion. In this case, the file is inaccessible.

R - represents reserve/release mode. Bit 1, if set, indicates that "implicit reserve, explicit release" is in effect, and if reset (zero) indicates "implicit reserve and release" is in effect. (See "Multiple Access Operation" in Section 4.6.)

angular position - represents current angular position - a sector number. When angular position equals sector address, the data file can be accessed.

configuration - represents configuration data. Bit 0, if set, indicates the addressed device has the dual access feature. Bits 1-3 contain the device type code, i.e., 111_2 for T3286 drive. Bits 4-7 contain the device position address, which may differ from the logical address. This address denotes the cabling position of the device on the controller or switch unit.

device status - represents the diagnostic device status received from the device, as listed below. Except for the T3286 disk drive bits 4-7 of this byte will have no meaning since the interfaces to the drive do not have the functional status lines to generate these bits. For other drives, these bits will always be zero.

Bit	Meaning
0	Device fault (voltage drop occurred).
1	Write fault.
2	Head positioning fault (loss of on-cylinder).
3	Offset polarity (used for checking head alignment).
4	Air flow loss occurred.
5	Parity error detected on device ID byte sent from controller.
6	Spindle speed fault.
7	Positioning servo fault.

physical address - this byte contains an address that is hardwired in the disk drive and permits uniquely identifying the disk drive in a system error log.

faults - these two bytes contain diagnostic faults data that is described below. This information is contained within the controller and indicates various faults that resulted in "transmission errors" or "unusual end" terminations. These data are accumulative and are cleared only by execution of this Sense order or by manual reset.

Byte	Bit	Meaning
8	0	Check-write error.
8	1	Data check byte error.
8	2	IOP parity error.
8	3	Rate error (data overrun).
8	4	Head address incremented out of limits while attempting a Read or Write order.
8	5	Arm in motion error - Seek order received while device arm in motion.
8	6	Order parity error detected.
8	7	Test mode order error - invalid test mode or incorrect length of test data bytes.

Byte	Bit	Meaning
9	0	Seek address transfer verification comparison error detected during Seek, Read, Check-write or Write order.
9	1	Device "unavailable" operational error or "not operational" signal detected from device by the controller, or seek error during Read or Write sequence.
9	2	Head address verification error detected.
9	3	Sector address verification error detected.

Byte	Bit	Meaning
9	4	Cylinder address verification error detected.
9	5	Controller Overtemperature.
9	6	Channel address error detected.
9	7	Missing on-sector signal from device during multisector Read or Write operation; or missing read or write clock, command strobe, or status request acknowledgement from device.

Seek modifier bits - represent either Seek modifier bits, or Restore Carriage modifier bits. Bit 0 of byte 10 represents device address 0 and bit 6 of byte 11 represents device address X'E'. A "one" set in any bit position means an interrupt is pending when the device reaches "on-cylinder" (positioning is complete) or Seek timeout.

Check bytes - always zero. The T3281 controller generates a seven byte check character which is used in checking and correcting data. Since only two bytes are available in the sense order no data will be transmitted.

difference - represents the difference (absolute value) last computed by the controller during a Seek order execution. The least significant bit is bit 7 of byte 15.

4.2.1.13 Select Test Mode (X'13')

This order is provided for diagnostic use only. The order causes the controller to request two bytes of data from the IOP and puts the controller in test mode. The first data byte, byte 0, specifies the test mode (or modes) and forced error conditions under which the subsequent operations will be performed. The second data byte, byte 1, specifies the device type and the device diagnostic conditions. The test mode order bytes have the following format:

Byte 0 Bits								Function
0	1	2	3	4	5	6	7	
0	0	0	0	0	0	0	0	Invalid test order.
x	x	x	x	0	0	0	1	Enter buffer test mode.
x	x	x	x	x	0	1	0	Enter controller test mode.
x	x	x	x	x	1	0	0	Enter device test mode.
x	x	x	x	1	x	x	0	Enter incremental clock test mode. (Not implemented in T3281 controller.)
x	x	x	1	x	x	x	x	Force device I/O parity error.
x	x	1	x	x	x	x	x	Force read data error.
x	1	x	x	x	x	x	x	Force IOP input parity error.
1	x	x	x	x	x	x	x	Force IOP output parity error.

Byte 1 Bits	Function
0-4	Diagnostic test condition for the device.
5-7	Device type code: The bits will be set to 111 (7_{10}) for the T3286 disk drive. Required only for controller test mode.

The Select Test Mode order must be issued with device address X'F' (the controller address). The controller can be released from test mode by an HIO instruction or by manual reset.

The test mode functions implemented in the T3281 differ from those in the 7275 controllers in that:

1. No incremental clock test mode is implemented and this code will be treated as an invalid order.
2. In device test mode, the status response (TDV) of the various drives attachable to the T3281 will be different than those of the 7275 since the drive control and status interfaces are different.

Operation for the various test modes is described briefly in the following.

Buffer Test Mode

Buffer test mode allows testing of the data path between the IOP and the controller. The controller buffer can be filled by a Write order and read back to the IOP by a Read order. The controller indicates end-of-data after the last byte has been transferred. By using controller address X'F', no device is necessary to execute buffer test mode tests.

Controller Test Mode

Controller test mode allows testing of the controller without operating a device. All subsequent orders can be exercised in a normal mode; control signals to the device are blocked. For data-in type operations the byte counter simulates data; for write (data-out) operations the written data are lost. By using controller address X'F', no device is necessary to execute controller test mode tests.

Device Test Mode

Device test mode provides a means for performing special diagnostic tests of the device and controller. All normal interface and controller sequences are operative except that the device nonoperational state does not cause sequences to be terminated with "unusual end", nor does it prohibit use of an SIO instruction. These exceptions allow status to be collected from the device and device commands to be issued to the device while the device is nonoperative.

Force Device I/O Parity Error

This feature allows a diagnostic program to test the address decoding logic and error reporting of any device. A "one" in bit 3 of the test byte (byte 0) forces a parity error in the output address lines to the device.

Force Read Data Error

This test feature allows testing of the controller's check byte (parity) generation and detection, and its reporting logic. A "one" in bit 2 of the test byte forces a one-bit error in a read operation and disables the error correction mechanism. Bit positions 0 and 1 of the first byte of any sector being read is forced to a "zero" state. This condition occurs for either simulated data (Controller Test Mode) or data from the device (Device Test Mode). The forcing of data errors exercises the parity logic in the controller; a check byte error detection may be exercised.

Force IOP Input Parity Error

This feature allows a diagnostic program to test the controller's parity generator and computer reporting logic. A "one" in bit 1 of the test byte forces a zero on the parity line to the IOP.

Force IOP Output Parity Error

This feature allows a diagnostic program to test the controller's parity checking and reporting logic for data transfers from the IOP. A "one" in bit 0 of the test byte forces the simulation of a "one" on the parity line from the IOP.

4.2.2 Extended Order Set

Since the T3281 controller is a programmable device, it will be possible to add additional orders to the controller when host software is available to support them. The orders described in the following will be made available in the controller to provide:

1. moving some error recovery procedures from the host to the controller
2. extensive testing of the error correction capabilities of the controller by the host
3. allow recovery of data from sectors in which only the header is defective
4. provide device to device data transfer

4.2.2.1 Set Order Modifier Byte (X'21')

This order causes the controller to acquire and store one data byte from the IOP. The contents of the data byte will modify the controller operation for orders in which errors occur and will allow the controller to automatically accomplish some error recovery procedures which normally would be done by host software. The data byte has the form:

Bit 0 - Enable Auto Alternate Seek. If the bit is set and a flawed track is detected on any data order except Sense, the controller will attempt to read the alternate address from any header on the track. If not successful, the order will terminate with "unusual end" and proper status. If successful, the controller will seek to the alternate track and perform the data operation. The controller will store the original address and if the data operation overflows the sector count, the controller will increment the original head address and seek back to the original cylinder address. On no sector overflow the drive carriage arm will remain at the alternate cylinder. The automatic seek back to the original (head incremented) address will occur, however, on any succeding data order which overflows the sector count.

Bit 1 - Enable Auto Retry. This bit set will enable the controller to automatically retry the execution of the order if:

1) the order is Read 1 or Read 2 and an uncorrectable data error occurs
2) the order is Read 1, Read 2, Write or Check-write and a header verification error, flaw mark or header parity error occurs
3) any order is being executed and the device becomes non-operational.

The number of retrys permitted is defined by bits 4-7 of the byte. During the retry of data read, if the addressed device has carriage offset and data strobe control capability, the controller will execute the various offset/strobe combinations the number of times specified by bits 4-7 of the modifier byte.

Bit 2 - Inhibit ECC. This bit, when set, will inhibit the error correction mechanism on Read 1 and Read 2 orders. Sector buffering will not occur and data read from the disk will be transmitted to the IOP as it is acquired by the controller. Data error detection only will be in effect and any error will be reported as "transmission error".

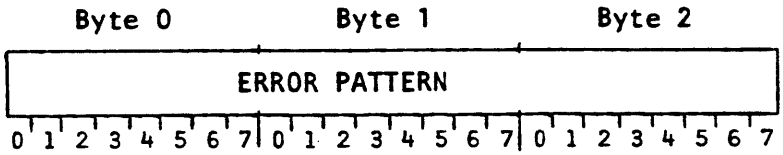
Bit 3 - Cylinder Boundary Crossover. This bit, when set, will allow the controller to increment the cylinder address and automatically initiate a seek when the head address increments past the end of the cylinder during a data order. The sector and head address will be cleared, TDV bit 2 will not be set and no "unusual end" termination will occur.

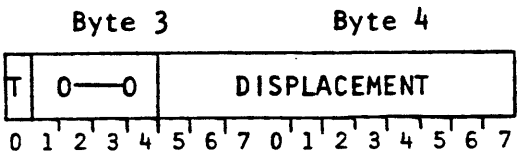
Bit 4-7 Number of Retries. These bits define the number of retries that may occur if bit 1 is set.

By using controller address X'F', no device is necessary to execute this order.

4.2.2.2 Insert ECC Error (X'23')

This order, only for diagnostic purposes, allows the host software to insert error bursts anywhere within the disk serial data stream in order to verify the integrity of the error correction mechanism in the controller. The order causes the controller to acquire five bytes of data from the IOP which have the following form:





Byte 0 through Byte 2 represent an error pattern in which any one represents an error bit. Any error pattern whose length is less than or equal to eleven contiguous bits is correctable. Any error pattern whose length is greater than eleven contiguous bits is uncorrectable. Three bytes are provided since an eleven bit burst may cross the boundaries of three data bytes from the disk.

T (byte 3, bit 0) controls the placement of the error pattern in the header or data area of the sector. T=0 allows the error burst to occur in the data area; T=1 places the error burst in the header area. The remainder of byte 3 and byte 4 represent a byte count displacement of the error burst from the start of the header or data area of the sector (i.e. the disk time at which the error burst starts).

During Write or Write Header orders, any one in the error pattern will toggle the corresponding bit written to the disk only and will not affect the bit entered into the check byte generator. During read operations the ones in the error pattern will toggle the corresponding bits written into the data buffer and the check byte generator. By using controller address X'F', no device is necessary to execute this order. Execution of this order enables insertion of the error burst on a succeeding read or write order.

4.2.2.3 IPL (X'20')

This order causes the controller to execute an initial program load of the writeable control store from the flexible disk program store in the same fashion as initial power up of the controller. It is intended for use only during host error recovery procedures where the disk system operation indicates an irrecoverable type of error. Device address X'F' must be used with this order.

4.2.2.4 Read Unverified (X'22')

This order permits recovery of data from sectors in which header verification errors or flaw marks exist. The order causes the controller to begin reading bytes from the disk at the current disk address stored in the controller and to transmit the bytes to the IOP. The order functions exactly as the Read 1 order except that no header

verification prior to the reading of data will be accomplished. Instead, the controller will find the index mark from the disk and then count sector marks until the mark defining the beginning of the addressed sector is found. The controller will then space over the header area and attempt to find a data sync byte within a specific time. If successful, reading of data proceeds as for the Read 1 order. If not successful, the controller will terminate with "unusual end" and verification error (TDV6) set.

Reading is continued until any of the terminating conditions for Read 1, with the exception of header verification related conditions, occur.

4.2.2.5 Select Flexible Disk (X'25')

This order causes the controller to request one byte of data from the IOP. The contents of the data byte define the flexible disk in the controller to be operated upon by succeeding orders. Device address X'F' must be used with the SIO that issues this order, and succeeding orders to the flexible disk must be chained to the Select order or must be initiated by a contiguous sequence of SIOs using device address X'F'. Any intervening SIO with device address other than X'F' will disable operation on the flexible disk until a new Select order is received.

Following the Select order, any of the data or positioning orders described in the preceding are valid for the flexible disk operation. No device interrupts will occur as a result of Seek or Restore orders since the controller will remain busy until the completion of the head movement. Data formats for some of the orders will be slightly different for the flexible disk:

1. Header Read/Header Write - All bytes will contain zeros except byte 3 and byte 4 which will contain track address and sector address respectively.

2. Seek - Byte 0 and byte 1 will contain zeros, byte 2 will contain track address, byte 3 is sector address.

3. Sense - The cylinder area is always zeros, remainder of data bytes are as described in 3.2.

4.2.2.6 Device to Device Transfer (X'27')

This order permits the controller to accomplish data transfer from one of the attached devices to another without any further action by the IOP or host CPU. The order causes the controller to request eight bytes of data from the IOP having the form:

Byte	Bit	Meaning
0	0	Transfer direction. Set indicates transfer from primary to secondary device.
	1→3	Secondary device type. Non-zero indicates device is other than disk drive.
	4→7	Secondary device address.

Bytes 1 through 4 are the seek address for the secondary device. The form of the data content is dependent on device type.

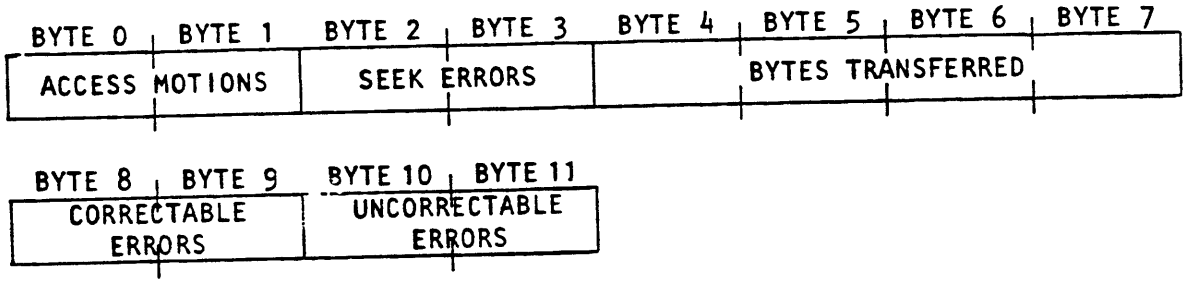
Bytes 5 through 7 define the data extent (number of sectors to be transferred).

The primary device is that addressed by the preceding SIO which initiated the order or the order chain in which the order occurs. This order provides even the simplest configuration of the T3281 with the capability of executing device to device transfer without involving the IOP.

4.2.2.7 Read and Reset Buffered Log (X'24')

This order causes the controller to transmit device error and usage statistical information to the IOP. The information is maintained on a device basis in the data buffer memory in the controller, and is updated after each controller operation on the device.

Controller address X'F' must be used with this order to permit execution regardless of the present state of the addressed device. On reception of the order the controller will request one byte of data from the IOP. The byte will contain the address (bits 4 through 7) of the device for which the order is to be executed. The controller will then send twelve bytes of data to the IOP having the following format:



where:

access motions - the number of head carriage movements executed on the device.

seek errors - the number of times that a commanded head carriage movement timed out or completed abonrmally.

bytes transferred - the cumulative number of bytes transferred between the IOP and controller.

correctable errors - the number of times that errors have occurred in data read from the disk but correction has been accomplished prior to transmission to the IOP.

uncorrectable errors - the number of times that errors have occurred in data read from the disk, were uncorrectable and retry was attempted.

Following transmission of the data to the IOP, the microprocessor will clear the controller memory locations for the addressed device prior to terminating the order via an order-in service call.

Incorrect length will be set if the number of bytes transmitted between the controller and IOP during this order is not exactly equal to thirteen.

4.2.2.8 Load Microcode (X'26')

This order permits the host to load microcode for non-standard user defined orders (or functional programs) from its main memory. The host must transmit 32KB of data to the controller in the format required for the WCS words. The data is buffered in the data buffer and is read from the buffer by the microprocessor prior to writing in the WCS to determine that no uncorrectable errors are detected by the buffer hardware. If no IOP or buffer errors are indicated the microcode will branch to ROM and execute an IPL function utilizing the data contained in the buffer. If less than 32KB are transmitted no data will be written in the WCS and the order will terminate with incorrect length and unusual end status.

In a minimal hardware configuration (32KB of data buffer) all disk seek address, error, and usage tables will be overwritten by this order. Also the data transmitted by the host must contain code for this order or for IPL (4.7.2.3) if further micro program initialization by the host is to be accomplished.

4.2.3 Extended Capabilities

The programability of the controller will allow added capabilities, depending upon the configuration of the hardware, beyond the extended order set described in 4.2.2. Some examples of extended capabilities which could be provided by the user or by Telefile through extended microcode are described in the following paragraphs.

4.2.3.1 Disk Pack Initialization

A stand alone microcode program could be used when the controller is off-line from the IOP to initialize the disk packs. The program will allow any or all packs to be initialized concurrently. Disk pack initialization would consist of the following steps:

1. writing and verifying headers
2. writing and verifying sensitive data patterns
3. flawing unusable tracks and assigning alternates
4. clearing the pack to zeros
5. writing a VTOC

A terminal connected to the controller can be used to output information concerning the state of the disk packs as initialization procedes.

4.2.3.2 Disk Pack Backup and Restore

If the tape option (3.4) is installed, the T3281, via extended microcode in the tape control processor, would be capable of saving selected disk packs on tape and restoring them from tape. The tape drive hardware format would meet with IBM standards for tape formatting. The tape label and record formats would be compatible with standards established by IBM or ANSI.

4.2.3.3 Journalization of Disk Pack Updates

If the tape option (3.4) is installed, the T3281, via extended microcode, would be capable of journalizing disk sector or track modifications onto tape. Programs could also be provided for running the journal tapes against a restored disk pack in order to make it current.

4.2.3.4 Relative Sector Address Mode

If host software is available to support it, the controller microcode could be modified to allow the host to address disk data by a relative sector number rather than a physical seek address. The controller would translate the binary relative address to cylinder, head and sector address and would automatically accomplish all seek, cylinder spanning and flawed track operations.

4.2.3.5 Logical Pack Access Protection

If host software is available to support it, the T3281 microcode could be modified to provide various degrees of access protection for each disk drive pack similar to that accomplished on the IBM 3350. These modes are:

1. enable diagnostic orders;
2. disable diagnostic orders but enable read, write and sense orders;
3. disable diagnostic and write orders but enable read and sense orders.

A new order (SET FILE MASK) would be added to the controller microcode which would acquire and store in the controller a byte of data for the addressed device. The data byte would define the above three modes in further processing of orders for the device.

4.2.3.6 Selective Disk Pack Format Modes

If host software is available to support it, the T3281 microcode could be modified to support disk track formats other than the 1024 byte sector format that presently exists.

4.2.3.7 Automatic Write Error Recovery

The controller microcode could be modified to perform a write check function following each disk write operation. If the write check function fails the controller would re-write the failing sectors from data in its buffer. If succeding write/write check operation fails, the order would terminate with unusual end status.

4.3 ORDER END CONDITIONS

At the termination of any order, the controller reports its condition at the termination via an "order-in" service connection to the IOP. The conditions reported, indicating "normal" or "unusual" (error) termination and errors in data transmitted, are described in the following.

4.3.1 Channel End Conditions

"Channel end" is signaled with each order-in. The order-in takes place after the occurrence of any of the following conditions:

1. "count done" signal received during a Sense order;
2. the controller executes a Seek order to a device;
3. the check character bytes are written in the last sector for a Write or Header Write order following a "count done" signal;
4. receipt of check character bytes of the last sector of a Header Read or Check-write order following a "count done" signal;
5. receipt and execution of a Restore Carriage, Release, Select Test Mode, or Condition Release Interrupt order;
6. detection of an IOP data-out parity error;
7. detection of data overrun (rate error);
8. after reading the check bytes during a Read 1 or Check-write order that has a "transmission error"; or
9. detection of an "unusual end" condition.

4.3.2 Unusual End Conditions

Unusual end is reported if errors are detected in device or controller operation during an order execution and always results in a TDV status bit being set to indicate a means of recovery. After an order is received, the detection of any of the following conditions causes the device to signal "unusual end" to the controlling system:

1. an out-of-range or illegal Seek address;
2. receipt of Seek order while arm in motion;
3. invalid order or order parity error;
4. device becomes "not operational" while the controller is "busy";
5. controller overtemperature condition

6. incorrect header parity, or a verification error for devices that use headers during a Read, Write, Check-write, or Header Read order operation. (The current address is not incremented.);
7. IOP Halt signaled by the IOP via a terminal order;
8. flaw byte encountered during a Read, Write, or Check-write order operation;
9. seek timeout (positioning error) occurs when controller receives a Seek, Read, Write, Check-write, Header Read, or Header Write order.
10. incorrect length on Seek, Header Read, or Sense order;
11. device interface error detected by controller;
12. Write-protect violation; or
13. control signal or address IOP error.

4.3.3 Transmission Error Conditions

The controller signals "transmission error" to the controlling system upon detecting any of the following conditions:

1. failure of an end-of-sector check bytes check during a Read or Check-write operation;
2. failure of data comparison during a Check-write operation;
3. data overrun (rate error); or
4. an IOP data-out parity error.

4.3.4 Incorrect Length Conditions

The controller detects "incorrect length" errors and reports them to the controlling system for any of the following conditions:

1. a byte count other than four was specified in a Seek order;
2. a byte count other than an integral multiple of the sector data record (1024 bytes) was specified for a Read, Write, or Check-write order;
3. a byte count other than a multiple of the sector header record (eight bytes) was specified for a Header Write or a Header Read order; or
4. a byte count of 0 or greater than 16 was specified for a Sense order.

4.4 STATUS RESPONSE

In response to an SIO, TIO, HIO, TDV, or AIO instruction, the controller will return status information depicting device/controller conditions at the time of the instructions. This information is described in the following paragraphs.

4.4.1 Condition Codes

When an I/O instruction is executed, condition code bits 1 and 2 are set to describe the general status of the addressed I/O device and controller. (Condition code 3 is also meaningful for an I/O instruction; when set, it means either the status returned in the registers is not reliable or the status has not been returned to the registers; when reset (zero), it means the status information is reliable. Note, however, that the device and controller do not influence CC3 - the IOP does.) Table 4-1 lists the CC1 and CC2 settings and their significance for the instructions.

I/O Instruction	CC1	CC2	Significance
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized, SIO not accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and device not "busy" when halt occurred.
	0	1	I/O address recognized and device "busy" when halt occurred.
	1	0	HIO not accepted; controller "busy" with device other than one addressed.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted.
	0	1	I/O address recognized, but SIO cannot be currently accepted.
	1	0	Not applicable.
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized.
	0	1	Device controller in test mode.
	1	0	Controller busy with a device other than one addressed.
	1	1	I/O address not recognized.
AIO	0	0	Normal interrupt recognition.
	0	1	Unusual condition*, interrupt condition, or controller is switched to a test mode.
	1	0	Not applicable.
	1	1	No interrupt recognition.

*An unusual condition is one in which the Seek timeout error, unusual end, or transmission error storage elements were set in the previous operation.

Table 4-1. Condition Codes for I/O Instructions

SIZE	CODE IDENT NO.	SPEC. NO.
A	51360	SS-600-0064-1B
SCALE	REV.	SHEET 41 OF

4.4.2 Device Status Byte

The device status byte returned to the IOP for any of the I/O instructions describes the status of the addressed device and its controller in more detail than do the condition code bits described in 4.4.1. The significance of each bit of the byte for each of the I/O instructions is described in Tables 4-2, 4-3 and 4-4.

The status returned for SIO, HIO, TIO and TDV instructions is relevant to the device addressed by the instruction. The status returned in response to the AIO instruction is relevant to the device generating the interrupt. The address of this device is returned to the IOP via the function response lines in response to the AIO.

4.4.3 Operational Status Byte

In addition to the information returned in the device status byte, the operational status byte generated at the end of each SIO, HIO, TIO and TDV instruction execution also provides indicators to the controlling system (see Table 4-5).

4.4.4 IOP Status Byte

In place of an operational status byte, an AIO instruction returns an IOP status byte in the same bit positions of the register. Table 4-6 summarizes the meanings of the settings of these bit positions.

4.5 I/O INTERRUPTS

4.5.1 Program I/O Interrupt Environment

The host program establishes an I/O interrupt environment by setting the flags in the second word of the IOP command doublewords in the command lists, and by using specified timeout delays within software timeout routines. The recommended software timeout delay for disk operations is a minimum of 2 seconds.

The following flags can be set to cause the controller to issue an I/O interrupt:

- ICE — Interrupt at Channel End. Set only in last command of a command list.
- IUE — Interrupt at Unusual End.
- HTE — Halt on Transmission Error.
- SIL — Suppress Incorrect Length. Set whenever the size of data transferred is not equal to the normal size for the operation (e.g., a Write operation with a byte count other than 1024). Thus an incorrect length indication is inhibited from causing an IOP Halt and a subsequent "unusual end" I/O interrupt.
- IZC — Interrupt at Zero Byte Count.

Bit Position	Function	Value	Meaning
0	Interrupt pending	1	Set if interrupt is pending (issued, but not acknowledged by an AIO instruction).
1,2	Device condition		Describes the current device condition as follows:
		00	Device "ready".
		01	Device "not operational".
		10	Device "unavailable" (reserved by other controller).
		11	Device "busy".
3	Mode	1	Always set to automatic mode.
4	Unusual end	1	Set if previous controller operation terminated with "unusual end".
5,6	Controller condition		Describes the current controller condition as follows:
		00	Controller "ready".
		01	Controller "not operational".
		10	Not applicable.
		11	Controller "busy".
7	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.

Table 4-2. Device Status Byte for SIO, TIO and HIO Instructions

Bit Position	Function	Value	Meaning
0	Error Corrected	1	Error Correction was successfully applied to data read from disk during block transmission. Data in core is valid.
1	Flaw detection	1	Flaw byte detected during Header Read, Write, Read, or Check-write.
2	Programming error	1	Invalid order detected; illegal address (address X'F' used for orders other than Select Test Mode or Conditional Release Interrupt); invalid Seek address; address incremented out of limits while attempting a Read or Write order; invalid test mode; Seek order received while arm was in motion; first six bits of Seek order were not zero; or incorrect length detected for Seek, Sense, Header Read, or Header Write order.
3	Write protection	1	Write-protect violation.
4	Parity error (IOP)	1	Order parity error detected; Seek address parity error detected; even parity received on a terminal order; or IOP detected on address parity error (channel address parity error).
5	Operational Error	1	Device interface error detected; missing an on-sector signal from device during a multisector Read or Write; missing Read or Write clock, command strobe, or status request acknowledgment from the device; detection of Seek address transfer verification comparison error during Seek, Read, or Write; device unavailable error or "not operational" signal detected from device by the controller; or a Seek error during a Read or Write.
6	Verification	1	Head address verification error detected; sector address verification error detected; or cylinder address verification error detected while reading a header.
7	Header check byte	1	Header check byte error.

Table 4-3. Device Status Byte for TDV Instruction

Bit Position	Function	Value	Meaning
0	Data overrun	1	Data overrun (rate error) has occurred during execution of the previous order.
1	Attention interrupt	1	Attention interrupt acknowledged.
2	Release interrupt	1	Release interrupt acknowledged.
3	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
4	On-sector interrupt	1	On-sector interrupt acknowledged. Note that either bit 4 or bit 6 can be set; both cannot be set.
5	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
6	Seek timeout error interrupt	1	Seek timeout error interrupt acknowledged. See note for bit 4. If bit 6 is set, program must issue a Restore Carriage order and retry the previous operation.
7	Power down interrupt	1	Power down interrupt acknowledged.

Table 4-4. Device and Controller Status Byte for AIO Instruction

Bit Position	Function	Value	Meaning
8	Incorrect length	1	Incorrect length condition has occurred.
9	Transmission data error	1	IOP or controller detected a parity error or data overrun in the transmitted information.
10	Transmission memory error	1	Memory parity error detected during a data I/O operation since last accepted SIO.
11	Memory address error	1	Nonexistent memory address detected during a chaining operation or a data I/O operation.
12	IOP memory error	1	IOP detected a memory parity while fetching a command.
13	IOP control error	1	IOP detected two successive Transfer in Channel commands.
14	IOP Halt	1	An error condition is detected that causes the IOP to issue a halt order to the addressed I/O device.
15	SIOP busy	0	Always zero for I/O instruction addressed to a MIOP.

Table 4-5. Operational Status Byte for SIO, HIO, TIO and TDV

Bit Position	Function	Value	Meaning
8	Incorrect length	1	Incorrect length condition has occurred.
9	Transmission data error	1	IOP or controller detected a parity error or data overrun in transmitted information.
10	Zero byte count interrupt	1	Zero byte count is detected and zero byte count flag is set.
11	Channel end interrupt	1	Device reports channel end to the IOP and the channel end flag is set.
12	Unusual end interrupt	1	IOP reports unusual end to the device and the unusual end flag is set; or the IOP signaled IOP Halt to the device controller.
13-15	Not assigned	-	Setting is inderminate; program should mask these bits.

Table 4-6. IOP Status Byte for AIO

4.5.2 Controller-Initiated Interrupts

The controller generates two types of interrupts. The first is the result of an IOP-generated interrupt to indicate unusual end, channel end, etc. The second type is device-initiated and indicates Seek or Restore Carriage completed, device released, or attention required. The IOP interrupts have priority over device-initiated interrupts. The controller "busy" condition has priority over a device interrupt.

Interrupts are cleared by an AIO or HIO instruction to device address X'F' or by I/O Reset. An AIO clears only one interrupt whereas the I/O Reset and the HIO with device address X'F' clear all interrupts by clearing all device interrupt flags. An HIO to the device initiating the interrupt clears the interrupt.

The various interrupts are discussed individually in the subsequent sections.

4.5.2.1 IOP-Initiated Interrupt

The IOP can set an interrupt call (CIL) by setting data bit 0 in a terminal order appended to a controller service connection (usually an "order in"). This interrupt is cleared by an AIO or HIO instruction or by I/O Reset. It has priority over any of the device interrupts described in the following.

4.5.2.2 Attention Interrupt

The attention interrupt indicates that an operator initiated condition exists at the device. A device initiates an attention interrupt by setting its attention flag. If the controller is not busy, it scans the devices for a device interrupt. If the controller receives a TDV, TIO, HIO, or SIO instruction for another device, the interrupt is temporarily removed until the instruction is completed. An AIO or HIO to the initiating device clears the attention interrupt.

4.5.2.3 Release Interrupt

A device initiates a release interrupt when it is released by another controller. The controller does not respond to any release signals from devices unless the Condition Release Interrupt order first enables the release interrupt logic. If a TIO, TDV, HIO, or SIO instruciton is issued to another device, the interrupt call is temporarily removed until the instruction is completed. An AIO or HIO to the interrupting device clears the interrupt.

4.5.2.4 On-Sector Interrupt

An on-sector interrupt indicates one of two things: a device has completed a Seek order or a Restore Carriage order (bit 4 of AIO status); or a Seek timeout has occurred (bit 6 of AIO status). The device signals on-sector to the controller when the heads are not in motion and the head is accessing the sector prior to the one addressed. Before the controller will generate an on-sector interrupt for any device, it must receive a Seek or a Restore Carriage order with the modifier bit set. An interrupt call (CIL) is set at the start of the sector prior to the one addressed by the order and is dropped at the start of the next sector if not cleared by an AIO

instruction. The CIL is reinitiated the next revolution, however. An on-sector interrupt is temporarily removed by a TIO, TDV, HIO, or SIO to another device. An AIO, HIO, or I/O Reset clears it. Please note that an AIO or HIO clears only the single interrupt, whereas I/O Reset also clears pending interrupts (CIL not set).

The on-sector interrupt has a window that is one sector ahead of the addressed sector. Thus it is possible for the condition code bits CC1 and CC2 of an AIO instruction to be set to a binary 11 configuration, indicating that no interrupt was recognized.

4.5.2.5 Power Down Interrupt

The power down interrupt indicates that a device that was in the "ready" state and available to the controlling system has been removed from the controlling system by removal of device power. The controller will scan the devices and will issue a power down interrupt if a device returns both the selected and on-line status false and at some prior time both signals were returned in the true state. If the controller receives a TDV, TIO, HIO or SIO instruction for another device, the interrupt is temporarily removed until the instruction is completed. An AIO or an HIO addressing the initiating device clears the interrupt.

4.6 MULTIPLE ACCESS OPERATION

There are three types of multiple access configurations possible:

1. a single CPU with two controllers sharing a device or devices;
2. dual CPUs sharing a device or devices, each through a separate controller;
3. four CPUs sharing a device or devices, each through a separate controller and controller pairs communicating with devices through T3289 dual access switch units.

In the first case (single CPU), the disk system is always in automatic release and "implicit reserve and release" is in effect. This means that the device is always selected and reserved upon acceptance of an SIO instruction, and is not released until the controller goes "ready". Please note that it is not released during command chaining or data chaining. For the Restore Carriage order and Seek order, the controller automatically releases the device when the carriage first starts movement.

This is when the controller is "ready" for another SIO; the device goes "on-cylinder" some time later. For other operations the controller automatically releases the device at the completion of each operation (at the time the controller goes "ready"). If a channel program is used that includes Seek and Read or Write orders, the device remains reserved throughout the operation; if a regular program is used that issues an SIO for each Seek and Read or Write order, the device is released between orders at channel end. Thus the Reserve and Release orders are not required and are effectively no-ops. If the Reserve and Release orders are used, they operate in this manner: an executed Release order first reserves the device and then issues a release.

In the second case (dual CPUs) the disk system is not in the automatic release and "implicit reserve, explicit release" is in effect. This means that the acceptance of the first SIO from either controller causes the pertinent controller to select and reserve the device, and that all orders automatically reserve the device. Thus the Reserve order is not required and is effectively a "no-op". The device remains reserved and must be explicitly released by some action: execution of a Release order, manual depression of I/O RESET or SYS RESET pushbuttons on the CPU control panel, switching of the reserving controller to off-line, or by power failure or shutdown in the reserving controller. The release interrupt is used to control the availability of the device to the two systems.

In the third case (quad CPUs) the disk system operates exactly as for the dual CPU case. The acceptance of the first SIO from any controller reserves the device to that controller. The device must be explicitly released by a Release order, actuation of I/O RESET or SYS RESET switches on the CPU control panel, switching of the reserving controller to offline, power failure or shutdown in the reserving controller, or a change of the control switches on the T3289 control panel to indicate that the device is no longer accessible by the reserving controller. On release of a device, the release interrupt is propagated to all non-reserving CPUs to indicate availability of the device.

5.0 PHYSICAL SPECIFICATIONS

5.1 DIMENSIONS

The T3281 controller is packaged in one cabinet. The cabinet dimensions are:

63 inches (nom) high
35 inches (nom) deep
23 inches (nom) wide

5.2 WEIGHT

The weight of the T3281 controller is 400 pounds.

6.0 ENVIRONMENTAL SPECIFICATIONS

6.1 OPERATING

The T3281 is capable of operating under the following environmental conditions:

1. Temperature $60^{\circ}F$ to $90^{\circ}F$
2. Relative Humidity 20% to 80% with no condensation

6.2 NON-OPERATING

The T3281 is capable of operating after experiencing the following non-operating environmental conditions:

1. Temperature -30°F to 150°F (ambient room air)
2. Relative humidity up to 90% with no condensation

6.3 HEAT DISSIPATION

Under normal operating conditions, heat dissipation for the T3281 will be 2000 BTU/hr.

6.4 COOLING

The T3281 will contain muffin fans to supply required cooling for its electronics and power supplies.

7.0 ELECTRICAL SPECIFICATION

Power requirements for the T3281 controller are:

Input Voltage:	115 VAC ±10% single phase
Line Frequency:	47 to 63 HZ
Current:	5 amps