

SYSTEMASTER II
TECHNICAL REFERENCE MANUAL

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PART ONE: GETTING STARTED

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CHAPTER 1 - INTRODUCTION TO THIS MANUAL

1.1 PURPOSE AND SCOPE

This manual was designed to explain everything you need to know to own, install, operate, evaluate, customize, or write software for the Teletek Systemaster II. Both introductory and advanced information on the hardware is included. This is a hardware manual only, and does not cover the use of any of the currently available software.

This manual is valid for Revision 2 boards.

1.2 ORGANIZATION

This manual consists of two main parts.

PART ONE: GETTING STARTED explains in simple terms how to configure and install your Systemaster II. The information is easy to read and avoids technical jargon as much as possible. If you just want to plug in your new board and start using it, this part is for you.

PART TWO: TECHNICAL INFORMATION covers the architecture of the Systemaster II in explicit detail. The information is by nature very technical. A much greater knowledge of electronics and computer terminology is assumed.

At the back of the manual, several appendices cover general information not required in the reading. A specification summary and a series of supplementary diagrams are included.

1.3 TERMINOLOGY AND CONVENTIONS

Throughout this manual, signal names that have a leading slash ("/name") represent active low signals on the CPU side of the S-100 bus. Signal names with a trailing asterisk ("name*") denote active low signals on the S-100 bus.

The terms "IEEE 696" and "S-100" apply to the same standard bus specification. They are used interchangeably throughout this manual.

Most of the abbreviations and part numbers used in this manual are defined in "Appendix E - Glossary".

1.4 RELATED DOCUMENTS

A bibliography is provided in the APPENDICIES section. The suggested literature will provide more complete information on the major integrated circuits used on this board.

CHAPTER 2 - INTRODUCTION TO THE SYSTEMASTER II

The Teletek Systemaster II is the next evolutionary step in Teletek's line of S-100 master processors. Systemaster II is an 8-bit, full function single board computer consisting of 85 integrated circuits on a four-layer S-100 board. At the heart of Systemaster II is the powerful Zilog Z80H microprocessor. High speed, high performance, and greater memory density are achieved on a standard-size S-100 board through use of the latest LSI support circuitry.

Systemaster II may be used as a dedicated single user computer or as a bus master in a multiprocessor/multitasking system. This flexibility is possible because the Systemaster II contains all of the features required for most applications. These features include:

- * 2 Serial ports.
- * 2 Parallel ports.
- * Flexible disk interface.
- * 64K or 128K bytes of dynamic RAM.
- * Reconfigurable EPROM pads for high density integrated circuits.
- * DMA capabilities, fully programmable.
- * Interrupt controller, 8 individual vectors.
- * Optional adapters for IEEE 488 or SCSI control.

With the above capabilities Systemaster II can provide high performance computing power in:

- * Word processing.
- * Data base management.
- * Dedicated industrial control.
- * Laboratory and instrumentation control.

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CHAPTER 3 - INSTALLATION

3.1 STANDARD INSTALLATION PROCEDURE

Installing the Systemaster II is straightforward. Most installations will require the following steps:

1. Inspect the Systemaster II for shipping damage.
2. Ensure that the Systemaster II is configured correctly.
3. Make any necessary hardware modifications.
4. Plug the board into the S-100 mainframe slot.
5. Attach the floppy drive cable.
6. Attach the local console cable.
7. Attach any other serial devices.
8. Attach any parallel devices.
9. Turn on and boot the system.
10. Make copies of operating system diskettes.
11. Configure the operating system.

3.2 VISUAL INSPECTION

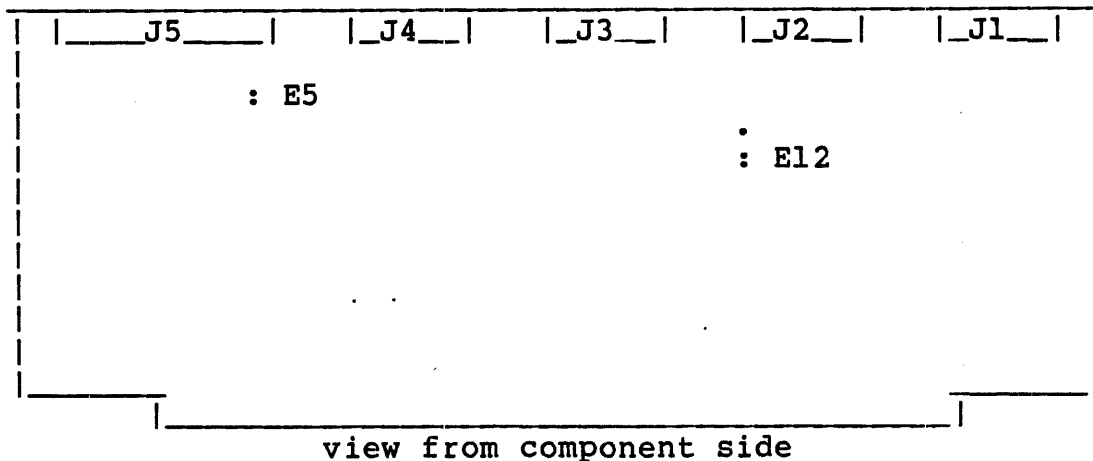
Upon receipt of the Systemaster II, check the shipping package for any signs of abuse while in transit. If you suspect that the package has been dropped or pierced, notify the shipping company immediately.

Inspect the circuit board for loose components, excessive moisture or anything that might not be normal. If any diskettes were shipped with the Systemaster II, check them for damage such as bending, or signs of a sharp object being placed against them. Diskettes are quite fragile and any damage to the media surface will render them inoperative. Again, notify the shipping company if you find any damage.

3.3 CORRECT CONFIGURATION?

With the component side of the board up and the connector facing you, verify that the following options are correct:

- E5 - These two option pins are used only while testing the floppy disk controller. For normal operation, the two pins should not be connected.
- E12 - These three option pins determine the source for the timing signal CPUCLK. On a 6 MHz board, the top two pins should be connected. On an 8 MHz board the bottom two pins should be connected.

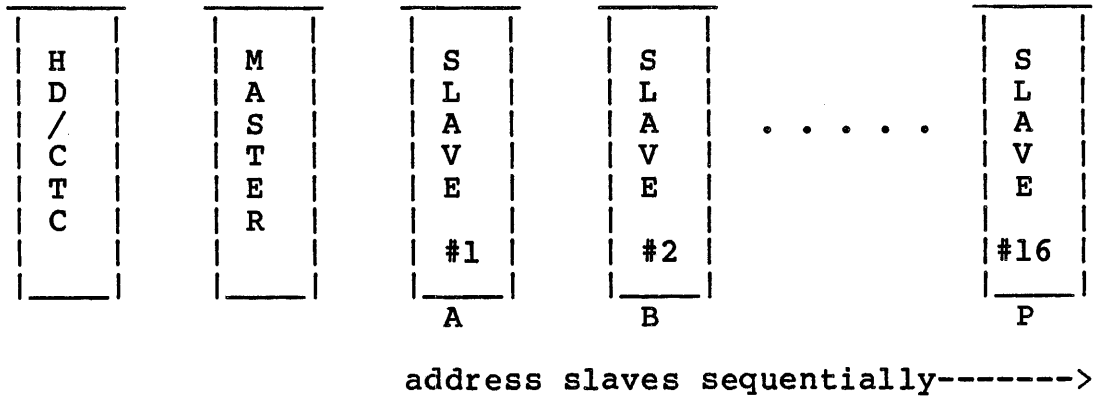


NOTE:

Any other modifications to your board will violate your warranty unless you have been authorized by Teletek to make those modifications.

3.4 BUS ORGANIZATION

Which slot you plug into is quite arbitrary unless you will be running six or more slaves and a hard disk controller such as Teletek's HD/CTC. To provide good bus flow and minimize bus noise in an application such as this, the following bus organization is recommended:



3.5 COOLING

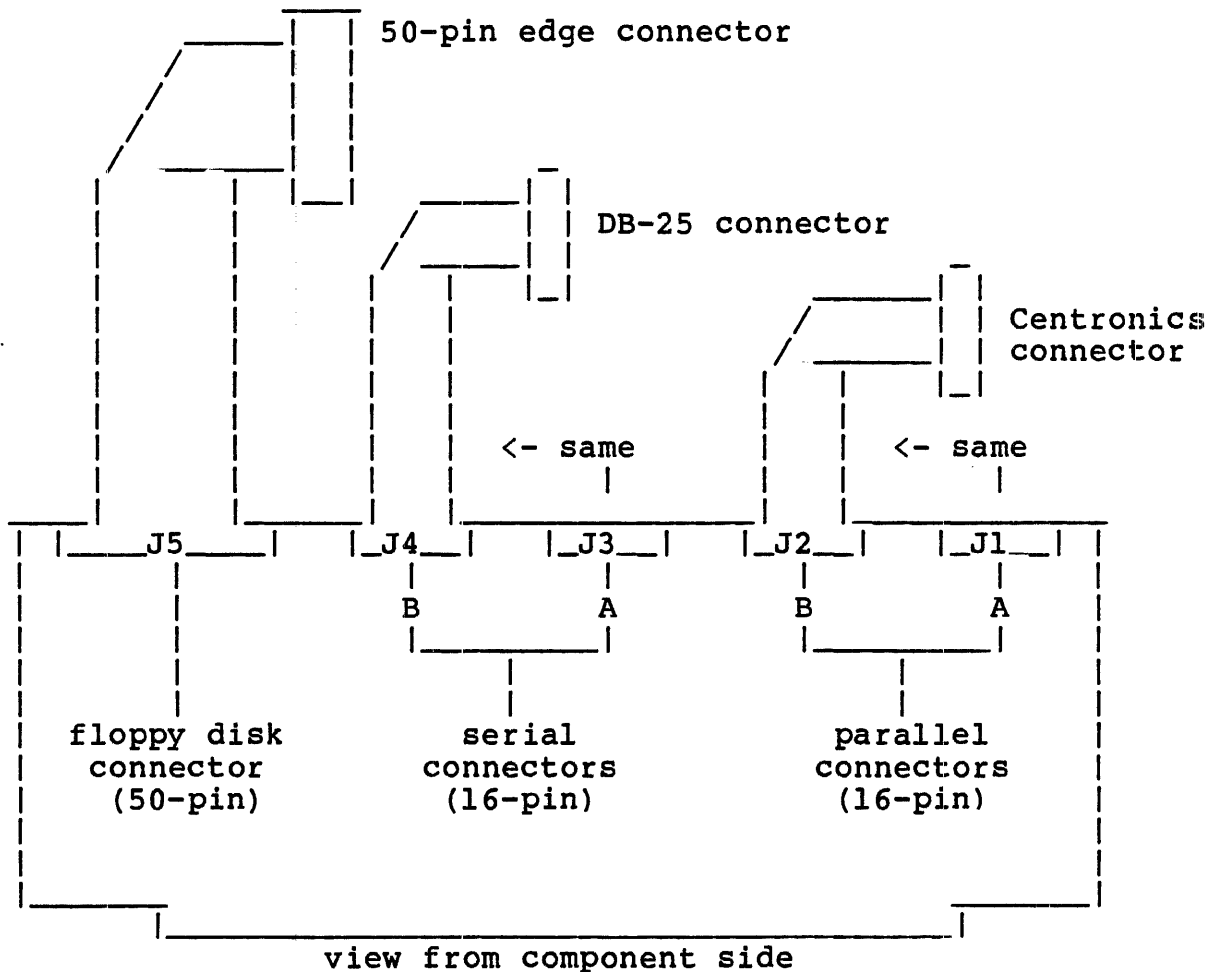
The Systemaster II needs to be in a well ventilated area due to the high density of integrated circuits on the board. Ideally, the board should be mounted vertically in a stream of air which is moving across its face. Ensure that the fan is close to the card cage for maximum cooling. Whatever the position, forced air cooling is mandatory.

3.6 PERIPHERAL CONNECTIONS

In most cases, the peripheral connections need only be flat ribbon cables with the appropriate crimp style connectors. The location of each of the header connectors is shown below and in "Appendix B - Board Layout Diagram". All these header connectors are male, allowing the use of similar female connectors on each of the cables. Make sure that pin 1 of each cable is toward the left edge of the board when the cable is installed

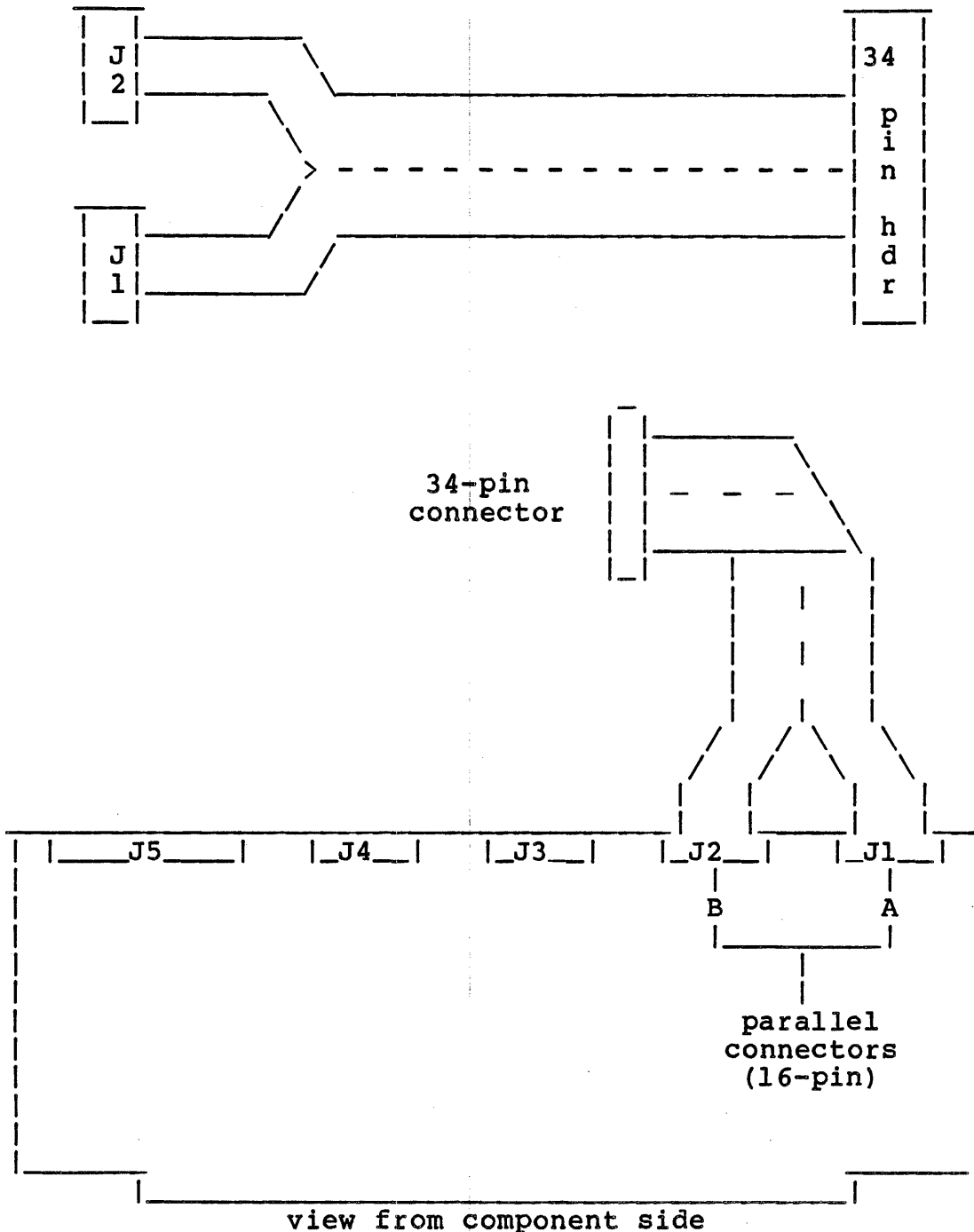
Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable. Too much tension may cause the cable to separate from its crimp connection and cause intermittent problems.

It is possible to order pre-assembled cables meeting your specifications directly from Teletek. Contact Teletek for pricing and shipping information.



Connector options

It is possible to configure the two 8-bit parallel ports into one 16-bit port. Depending on the application, it may be advantageous to build a split connector to accommodate this as shown:



3.7 PREPARING YOUR SOFTWARE

If you have not yet made backup copies of your software diskettes, do so now.

To configure your operating system, refer to the software documentation enclosed with your diskettes.

3.8 IN CASE OF TROUBLE

If the Systemaster II does not respond the first time it is connected, relax. Due to the complexity of the board there are many areas that may have inadvertently been overlooked. Take the time to read the manual thoroughly, especially the "Peripheral Connections" section. The following trouble-shooting guide lists the most common problems.

1. Are both your system and your console plugged in? Are they both turned on? Is your boot diskette in the correct drive? Is the drive door shut?
2. Check the console cable and verify the handshaking signals. Make sure the console is set at the proper baud rate.
3. If the Systemaster II was originally shipped without RAM, make sure the memory chips are installed correctly. Remember that the RAM devices must use the 128 cycle refresh mode in order to be compatible with the Systemaster II's refresh circuit.
4. Check the disk drive cable and the disk drive configuration. Has the write precompensation been correctly adjusted for your particular disk drives?
5. Have the correct options or modifications been added to the board for the operating system being used? Are you using an operating system designed to work on the Systemaster II?
6. If the console and cable are working properly, the correct RAM is installed, the diskette circuitry is configured properly, the correct hardware option modifications have been added, and the operating system has been correctly configured, the Systemaster II itself may be faulty. Try another Systemaster II if one is available. Otherwise, return the board to your dealer for check-out. (If you purchased your Systemaster II directly from Teletek obtain a Return Merchandise Authorization (RMA) number from the factory before shipping the board.)

PART TWO: TECHNICAL INFORMATION

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CHAPTER 10 - IEEE 696 (S-100) BUS INTERFACE

Although the S-100 bus interface has been a defacto standard since 1975, many compatibility problems have been solved by the recent (1982) adoption of the IEEE 696 standard specification. The following is a description of the IEEE 696 (S-100) signals as implemented on the Systemaster II.

10.1 POWER AND GROUND

Systemaster II has the following power requirements:

5 volts at 2.0 amps
+12 volts at 40.0 milliamps
-12 volts at 40.0 milliamps

Onboard voltage is regulated and power supply decoupling is provided both at the card edge and distributed throughout the board.

10.2 PERMANENT MASTER INTERFACE

Systemaster II is configured as a permanent master. This means that it can transfer device-dependent messages to and from all bus slaves. It is also responsible for generating the timing for all bus cycles. Another board in the system may become a temporary master by asserting the HOLD signal on the bus. Once the temporary master has completed its task, it must return control to the permanent master, in this case the Systemaster II.

Systemaster II echos all of its states to the bus by means of timing signals. Please note that the 8 MHz version makes no attempt to slow down to the 6 MHz maximum bus speed described in the IEEE standard specification. The only way to meet the IEEE maximum speed requirement with a faster CPU is by adding wait states and slowing down all transitions, all the time. This lowers the performance of the 8 MHz master by a significant percentage. Teletek chose to provide a full performance 8 MHz master for those applications which require this high speed. For applications which require the board to stay within the IEEE specifications, Teletek recommends the 6 MHz Systemaster II.

The following is a description of the Systemmaster II IEEE 696/S-100 interface signals.

10.2.1 Status Bus

The status bus consists of seven signals which identify the nature of the bus cycle in progress, and qualify the nature of the address on the address bus. Each of these seven signals are three-state lines which may be disabled by asserting the status disable signal SDSB* on the S-100 bus.

SMEMR	Memory read
SML	Operation code fetch
SINP	Input
SOUT	Output
SWO*	Write cycle
SINTA	Interrupt acknowledge
SHLTA	Halt acknowledge

10.2.2 Control Bus

The control bus consists of five output control signals (denoted by the lowercase p) and five input control signals.

The five output control signals determine the timing and movement of data during any bus cycle. These signals are typically monitored by slave or controller boards on the bus.

pSYNC	Start of new bus cycle
pSTVAL	Address and status are valid
pDBIN	Generalized read strobe
pWR*	Generalized write strobe
pHLDA	Hold acknowledge signal

The five input control signals allow bus slaves to request operations of the Systemmaster II and to synchronize the operation of the master with conditions internal to the slave.

RDY	Slave RDY
XRDY	Front panel RDY
INT*	Interrupt line
NMI*	Non-maskable interrupt line
HOLD*	Hold request

10.2.3 Address and Data Bus

Systemaster II provides the Z80's 16-bit address bus to the S-100 interface. This means that a linear addressing range of 64K bytes is possible. The refresh address functions of the Z80 may also be used by bus devices since the RFSH* (refresh) signal is also provided on the bus. The address lines are buffered by three state drivers which may be disabled by the S-100 address disable signal ADSB*.

A0 through A15 Address bus

Data transfers into Systemaster II pass through octal three state buffers. Systemaster II will only allow data onto its internal bus when qualified bus devices are detected and no onboard memory or I/O read is occurring.

DI0 through DI8 Input data bus

Data transfers out of the Systemaster II also pass through a three state driver which may be selectively disabled by bus devices using the data out disable signal DODSB*.

DO0 through DO8 Output data bus

10.2.4 Interrupt and Reset Functions

Bus devices that wish to use Systemaster II's vectored interrupt controller have access to five interrupt lines. The interrupt lines are connected to the 9519 and their use is at the user's discretion unless otherwise specified.

V10* through V14* Vectored interrupt lines

Systemaster II contains a power up clear/reset circuit that insures that the CPU and all logic are correctly initialized. A reset is generated automatically on power up or can be caused by a front panel reset. To insure a proper reset, whenever the board is powered down allow a minimum of 30 seconds before powering up again. This lets the reset circuit come to a known condition and be armed for a power up reset.

POC* Power on clear. Automatic on power up.

Slave Clr* Reset all slaves. Automatic on power up.

Reset* Master reset. Typically connected to a front panel reset switch.

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 CHAPTER 4 - CPU AND CONTROL LOGIC

The Systemaster II control logic consists of a Zilog Z80B or Z80H CPU, running at 6 MHz or 8 MHz respectively, and several bipolar and MOS LSI integrated circuits. Programmable logic arrays (PLAs) are used to reduce random logic and therefore pack more features onto the board.

 4.1 CLOCKS

All clocks are provided by two TTL crystal oscillators running at 16 MHz and 24 MHz (U23 and U30 respectively). The appropriate frequencies are derived at U24 (a 74LS393). Their values are as follows:

Mnemonic	Value
-----	-----
CPUCLK	8 MHz or 6 MHz
DMACLK	4 MHz or 3 MHz
FDCLK2M	2 MHz
FDCLK1M	1 MHz
PCLK	6 MHz

Since the clock inputs to the Z80 CPU and the DMA controller require strict levels typical of MOS devices, two HCT parts are used to guarantee the minimum and maximum clock level inputs to these devices. A 74HCT74 (U19) and a 74HCT00 (U20) provide the high speed rail to rail MOS clock interface to the DMA and CPU respectively. Any field replacement of these components must be with HCT devices. LS or S devices cannot provide the voltage levels and the transition times required by the MOS devices.

The Systemaster II is factory configured for either 8 or 6 MHz operation. If you change the operating frequency yourself, you must ensure that the correct clocks are chosen at jumper E12, the correct LSI controllers and components are installed and the correct board modifications are made. Contact Teletek for more information.

4.2 WAIT STATES

As technology advances, CPUs are breaking speed barriers and making more stringent demands of the support circuitry that surrounds them. Faster CPUs such as the Z80B and Z80H require faster memory and peripherals. Where faster support chips are either not available or prohibitively expensive, the CPU must be slowed down instead.

Wait states are a technique of stalling the CPU for a specific number of clock cycles.

Systemaster II uses wait states to slow down for RAM, EPROM and I/O operations. The following table gives the number of wait states for each operation:

Number of Wait States		
Operation	6 MHz	8 MHz
RAM	0	1
EPROM	2	3
I/O	2	2

1 wait state = 1 clock cycle
= 1 x CPUCLK
= 166.7 ns for 6 MHz
= 125.0 ns for 8 MHz

4.2.1 Memory Wait States

Memory wait states are provided by U36 (a 74LS164) and U28 (the FDC PLA). The 74LS164 is a shift register and is used to provide a variety of shifted /MREQ signals to be used as gates for different wait state lengths. Pin 3 (M1WS) is used to gate one wait state for RAM. Pin 5 (M3WS) provides the gate for three waits. The FDC PLA does an internal multiplex so that when RAM is active the correct number of wait states for RAM are inserted and when PROM is active, the correct number of wait states for PROM are inserted.

Memory wait state configuration is quite flexible. The Systemaster II is capable of providing up to eight wait states in individual combinations for RAM and EPROM. This is done by connecting the appropriate signal from U36 to pin 7 of the FDC PLA for RAM wait states or to pin 8 of the same PLA for PROM wait states.

When changing the Systemaster II from one speed to the other in the standard configurations, a different FDC PLA is required. Consult Teletek if your application requires this.

The following figures will help when calculating additional wait states. These figures are provided for general information only!

Critical Z80 Timing Parameters (no external delays considered) (times calculated with no wait states)		
Parameter	6 MHz	8 MHz
Memory Fetch (time from /M1)	203 ns	140 ns
Memory Read/Write (time from /MREQ)	203 ns	150 ns

4.2.2 I/O Wait States

I/O wait states serve to synchronize the CPU interaction with the ASCC, CIO, DMA and interrupt controller. Both the 6 and 8 MHz versions of Systemaster II use two I/O wait states, so no alterations are necessary to change from one speed to the other.

I/O wait states are generated by U38 (a 74LS164 shift register) and U17 (a 74LS32). Since the shift register provides seven usable taps, it is possible to add as many as seven wait states to I/O operations. However, while there is no limit on the maximum number of wait states, there is a required minimum for proper operation. Systemaster II requires two wait states. Fewer than two will not guarantee proper onboard device access.

If your application requires additional wait states, these can be added by replacing the signal going to U17 pin 13 with the proper tap output from U38. Refer to the following table and to "Appendix C - Schematic Diagrams".

I/O WAIT STATES FROM U38 TAPS

pin 5	2	wait states	(standard)
pin 6	3	" "	(optional)
pin 10	4	" "	"
pin 11	5	" "	"
pin 12	6	" "	"
pin 13	7	" "	"

4.3 I/O DECODER

I/O addresses for onboard devices are decoded by U44 (a 74LS138). Onboard I/O functions occupy four addresses per port, except for the CONTROL LATCH, which uses eight. Onboard I/O decoding is disabled for all non-I/O operations, effectively eliminating I/O noise. The following is a brief description of the decoded ports:

/CTL0	- Control 0
/CTL1	- Control 1
/CIOEN	- CIO ENable
/ASCCEN	- ASCC ENable
/UICEN	- Universal Interrupt Controller ENable
/FDCEN	- Floppy Disk Controller ENable
/DMAEN	- DMA ENable
/RWPORT	- Read Write PORT

4.4 I/O MAP

Onboard I/O devices occupy 32 consecutive addresses ranging from 00h to 1Fh, as shown in the table below. The remaining I/O addresses (20h to FFh) may be used for other boards such as slaves and disk controllers. When setting the address on other boards, make sure that none of the addresses conflict.

Onboard I/O Addresses	
Ports	Use
00h - 07h	Control Latch
08h - 0Bh	CIO (Z8536)
0Ch - 0Fh	ASCC (Z8531)
10h - 13h	UIC (9519)
14h - 17h	FDC (WD2797)
18h - 1Bh	DMA
1Ch - 1Fh	RWPORT
20h - FFh	not used onboard

4.5 CONTROL LATCH

Onboard control is implemented with U3, a 74LS259 addressable latch. The latch is bit addressable. This means that individual bits may be set or cleared without affecting the rest of the bits.

Writing a one or zero to an address between 00h and 07h sets or clears a bit as defined in the following table:

Address	Mnemonic	State	
-----	-----	-----	-----
00h	OFFBOARD	0= onboard RAM	1= offboard RAM
01h	BANK-0/1	0= bank 0	1= bank 1
02h	FDMOTOR	0= motor off	1= motor on
03h	FDSELO	-----v	
04h	FDSEL1	-----v v	

		0 0	= drive 0
		0 1	= drive 1
		1 0	= drive 2
		1 1	= drive 3
05h	FD-D/S	0= double density	1= single density
06h	FD-5/8	0= 5.25 inch	1= 8 inch
07h	/PROMEN	0= EPROM on	1= EPROM off

4.6 READ WRITE CONTROL PORT

One additional port is used for two special control signals. An I/O operation to any port between 1Ch and 1Fh will access this port.

Any write clears the parity error interrupt.

Any read brings in the status of the floppy drive Dual Side signal in bit 0. Bit 0 = 0 means the diskette is single sided. Bit 0 = 1 means the diskette is double sided

4.7 PROGRAMMABLE LOGIC ARRAYS (PLAs)

Rapid advances in semiconductor technology have resulted in ever larger and more powerful integrated circuits. One of the fruits of these advancements are PLAs - programmable logic arrays. PLAs are integrated circuits that can be programmed in much the same manner as PROMs. In brief, the PLA contains an array of OR and AND gates that can be selectively fused (connected) together to implement combinatorial functions. The result is that, once programmed, one PLA device may contain the equivalent of up to ten discrete MSI circuits.

Systemaster II makes use of PLAs to implement functions that would have required extensive discrete logic. Other reasons for using PLAs are:

- it is an easy way to program hardware
- hardware modification is easier
- the space savings is tremendous

The following paragraphs explain each of the four PLAs used on the Systemaster II and give their output signal definitions.

FDC PLA - The Floppy Disk Control PLA (U28) is used to provide drive selects and clock control to the floppy disk controller. It also gates onboard I/O decodes and generates memory wait states. Note: This PLA must be changed when the CPU speed is changed

Signals:

FDCCLK - Floppy Disk Controller CLock
DS0 - Drive Select 0
DS1 - Drive Select 1
DS2 - Drive Select 2
DS3 - Drive Select 3
/MWAIT - Memory WAIT states
/IOEN - I/O ENable

RAM PLA - The RAM PLA (U22) is used to initiate RAM access cycles, control bank switching, and keep track of all RAM operations. This PLA defines the common boundary and must be changed when the memory map is changed.

Signals:

/RAMOFF - Informs additional logic of type of onboard or offboard RAM access.
/BANK0SW - Control signal for enabling bank 0.
/BANK1SW - Control signal for enabling bank 1.
/REFRESH - Informs RAM logic of refresh.
/START - Begins RAM timing at the start of cycles.

WAIT PLA - The WAIT PLA (U35) is used to multiplex the proper wait signals to the CPU. It also generates RAM and EPROM select signals and RAM parity control.

Signals:

/ON - RAM transceiver control signal.
PDOUT - Gated parity data for input to parity IC.
/RAMRD - Parity read clock.
/WAIT - Combination of all the wait states.
A15 - CPU address 15
/PROMSEL - PROM select.

S-100 PLA - The S-100 PLA (U55) generates all the appropriate signals to the S-100 bus.

Signals:

SOUT - Output operation in progress
SINP - Input operation in progress
SMEMR - Generalized memory read
SINTA - Interrupt acknowledge in progress
SWO* - Generalized memory write
/STRB - Strobes S-100 cycle initiates
/PHLDA - Hold acknowledge in progress
DIDSB - Disable the input data buffers

Normally there will be no need to change PLAs unless you suspect that your board has a faulty device or you want to change to a faster CPU speed, different number of wait states, different size of common area, etc.

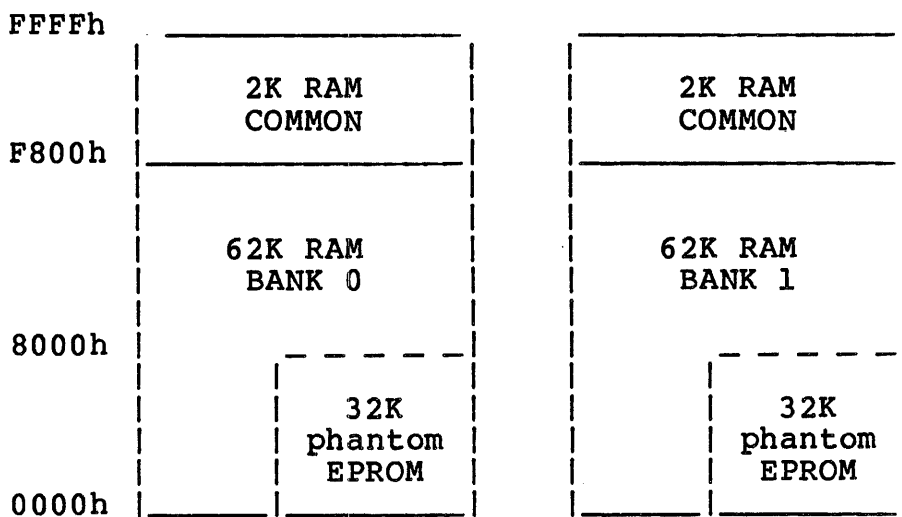
All of the PLAs on Systemaster II are available only from Teletek and should be handled with care to prevent static damage.

CHAPTER 5 - MEMORY

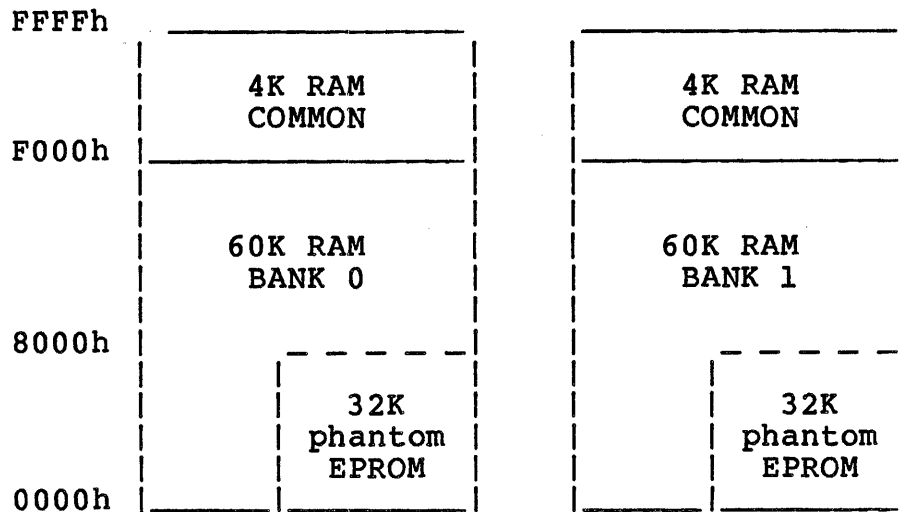
Systemaster II is designed with many storage features that make it ideal for single and multiuser environments.

5.1 MEMORY MAPS

5.1.1 Standard Memory Map



5.1.2 Optional Memory Map



5.2 RAM

Onboard memory is implemented with 64K x 1 dynamic RAM devices. These RAMs make use of the Z80 CPU refresh capabilities and hence are specified as having a 128 row/2 ms refresh cycle. A 6 MHz board requires 150 ns RAM devices, while an 8 MHz board requires 120 ns devices. If you substitute any RAM yourself, you must use devices of the correct refresh type and operating speed. (See "Appendix A - Specifications".)

5.2.1 Bank Control

Bank control is done with the BANK-0/1 and OFFBOARD bits of the control latch. There is no memory management hardware.

The RAM PLA determines a memory address called the common boundary. All writes and reads above the common boundary are directed to onboard memory, regardless of the state of the OFFBOARD control signal. Writes above the common boundary go to both onboard memory banks, resulting in duplicate copies of common at the top of each bank. Reads above the common boundary come from the onboard bank last selected with BANK-0/1.

Below the common boundary, memory accesses are more normal. If the OFFBOARD bit is set to zero, reads and writes act on the onboard bank last selected with BANK-0/1. If the OFFBOARD bit is set to one, reads and writes act on an offboard bank.

5.2.2 Parity Checking

An added feature of the Systemaster II is its use of parity as a memory error detection mechanism. The Systemaster II is set up to check for even parity, and because it has an even parity bus (8 bits), the operation is easy to understand.

Parity checking is done with U41 (a 74LS280) and each RAM bank has an individual RAM used to store parity information. The following action takes place when doing a write to RAM:

- If the byte to be written contains an even number of one bits, then the output of the parity checker is a zero. This zero is written to the parity RAM along with the byte, leaving the total number of one bits unchanged.
- If the byte to be written contains an odd number of one bits, then the output of the parity checker is a one. This one is written to the parity RAM along with the byte, making the total number of one bits even.

As you can see, any byte that does not contain an even number of ones is forced to be even by the parity checker. We can therefore be sure that all bytes written to RAM are of even parity. This means that if no errors occur to the data while in memory, every byte we read back will be even. If any byte is not even, the parity checker will detect the error. Additional support circuitry will then post the parity error interrupt.

5.2.3 Parity Initialization

There are no set procedures for initializing parity since this is strictly a hardware function. However, one traditional action is to write zeros to all of RAM and then read them back. This checks your RAM for bad cells and at the same time starts you out with a clean slate (all locations set to zero).

5.2.4 Parity Clear/Disable

The parity interrupt signal /PARINT is connected to request 0 of the interrupt controller. When necessary, this individual interrupt may be masked out in the interrupt controller, effectively disabling parity.

Once a parity error has been handled by an interrupt routine, the parity interrupt should be cleared by doing a dummy write to any address at /RWPORT (1Ch to 1Fh).

5.3 EPROM

EPROM operation on Systemaster II is very flexible. Upon power up or reset condition, the PROM is automatically enabled at location 0000h. In this condition, the memory map is partitioned with the lower 32K (0000h to 8000h) as PROM area. While the PROM is enabled, it is still possible to write to the RAM in the same address range as the PROM (the lower 32K). Writes to an address in the lower 32K will go to the RAM, while reads from the lower 32K come from the PROM. This switching is done automatically in hardware.

The PROM can be disabled under software control. This is done with the /PROMEN bit of the control latch. When the PROM is disabled, it is effectively removed from the memory map. This means that now the entire addressing range may be used to address RAM.

5.3.1 Density options

In the past, the size of onboard firmware has been limited by the size of the EPROM standard on the board. Systemaster II overcomes this limitation by providing a fully approved JEDEC EPROM socket with the capability to handle 2K to 32K devices (2716 to 27256). This means that custom firmware may be implemented in an appropriately sized EPROM by simply modifying the socket pads.

The diagram on the next page shows the JEDEC approved INTEL universal site for EPROMS which Systemaster II uses. It shows an EPROM whose pins on either side have different classifications. For example, to find the required signals for 2716s, simply read the 2716 column on either side. The illustration clearly shows which signals change between densities.

JEDEC APPROVED INTEL UNIVERSAL SITE FOR EPROMS

2	2	2	2	2				2	2	2	2	2
7	7	7	7	7				7	7	7	7	7
2	1	6	3	1				1	3	6	1	2
5	2	4	2	6				6	2	4	2	5
6	8										8	6

VPP	VPP	VPP			1	28				VCC	VCC	VCC
A12	A12	A12			2	27				/PG	/PG	A14
A7	A7	A7	A7	A7	3	26	VCC	VCC			A13	A13
A6	A6	A6	A6	A6	4	25	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	5	24	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	6	23	VPP	A11	A11	A11	A11	A11
A3	A3	A3	A3	A3	7	22	/OE	/OE	/OE	/OE	/OE	/OE
A2	A2	A2	A2	A2	8	21	A10	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	9	20	/CE	/CE	/CE	/CE	/CE	/CE
A0	A0	A0	A0	A0	10	19	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	11	18	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	12	17	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	13	16	D4	D4	D4	D4	D4	D4
GND	GND	GND	GND	GND	14	15	D3	D3	D3	D3	D3	D3

The standard Systemaster II is configured for a 2K EPROM. The table below lists the steps necessary to convert a standard board to accept an EPROM of a different size. (The locations of the "E" pads are shown in "Appendix B - Board Layout Diagram".)

EPROM	Disconnect	Connect
2732, 4K	E3-2 from E3-1	E3-2 to E3-3
2764, 8K	E3-2 from E3-1	E3-2 to E3-3
27128, 16K	E3-2 from E3-1 E2-3 from E3-1	E3-2 to E3-3 E2-2 to E2-3
27256, 32K	E3-2 from E3-1 E2-3 from E3-1 E1-2 from E1-1	E3-2 to E3-3 E2-2 to E2-3 E1-2 to E1-3

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CHAPTER 6 - CHARACTER INPUT/OUTPUT

Any computer is virtually useless unless you can communicate with it through some kind of interface. Once provided with such an interface, you can interact with the computer and program it to do useful work.

Systemaster II provides both serial and parallel interfaces that are completely reprogrammable and can be configured for a variety of applications.

6.1 ASCC SERIAL PORT CONTROLLER

Serial ports on the Systemaster II are controlled through a Zilog Asynchronous Serial Communications Controller (ASCC). The ASCC is a dual channel serial transmitter and receiver, and is an upgrade of the Zilog SIO. It provides two very powerful serial ports.

6.1.1 CPU to ASCC Interface

The CPU communicates with the ASCC via programmed I/O. The ASCC looks like four port addresses to the CPU. Each channel (A or B) has its own control register and its own data register. Internally, the ASCC contains 14 write registers and 7 read registers.

Each channel's write register set includes the following:

- 10 registers used for control
- 2 registers used for sync character generation
- 2 registers used for baud rate generation

Each channel's read register set is composed of:

- 4 registers used for status functions
- 2 registers used by the baud rate generator
- 1 register for the receive buffer

6.1.2 ASCC Software Interface

The ASCC contains two independent asynchronous serial channels. each with its own baud rate generator. Each channel has a set of internal read registers (RRx) and write registers (WRx), and two external ports called the control and data ports to access these registers. The control and data port addresses for the ASCC channels are shown below. Several of the internal ASCC registers are common to both channels and can be accessed through either channel's control port.

ASCC Port Addresses	

0Ch	Port B control
0Dh	Port B data
0Eh	Port A control
0Fh	Port A data

The ASCC internal registers are accessed in a two-step process, using a pointer register to address the internal register. To access a particular register, the pointer bits must be set by writing to WR0. WR0 is common to both channels and a write to either channel's control port will set the pointer bits in WR0. After the pointer bits are set, the next read or write operation with the selected channel's control port will access the desired internal register for that channel. After this read or write operation, the pointer bits are reset to zeros, and the next write to either control port will access WR0. If the state of the pointer bits is unknown, then a read from either channel's control port will reset them to zeros. Also, each channel's internal transmit data buffer register WR8 and internal receive data register RR8 can be accessed directly by a read or write operation with the desired channel's data port.

Each ASCC channel is initialized by writing a stream of bytes to the control port for that channel. This stream of bytes contains pointer register values followed by register content values for loading the internal registers needed to configure the channel's operation mode. A separate stream of bytes is send to each ASCC channel.

Each channel is initialized with respect to three areas:

- asynchronous mode format
- baud rate generation
- interrupt operation

The asynchronous mode configuration allows specification of the following parameters:

- 5, 6, 7 or 8 bits per character
- 1, 1.5 or 2 stop bits for transmitter
- Odd, even, or disabled parity generation
- Times 1, 16, 32 or 64 clock rates
- Hardware CTS*/DCD* handshaking via Auto Enables option
- Selection of transmit and receive clock sources from
 - RTxC* pin
 - TRxC* pin
 - Baud Rate Generator Output

Each channel contains a baud rate generator to provide the transmit and/or receive clock(s). The baud rate generator consists of a two-byte down counter and some multiplexing logic. Given an input clock source (either the PCLK pin or RTxC* pin), the baud rate generator will divide this source by the value in the baud rate Time Constant registers to produce a clock for the transmit and/or receive section. The PCLK pin is driven by a 6 MHz clock and the RTxC* pin is driven by a 24 MHz clock.

The ASCC allows vectored interrupts for all internal interrupting sources using the Vector-Includes-Status mode. In this mode, the base interrupt vector held in WR9 has certain bits modified to produce a response vector that identifies which internal interrupt source is being acknowledged. WR9 is common to both channels and can be accessed through either channel's control port. Each internal interrupt source in the ASCC can be enabled or disabled individually. The internal interrupt sources in the ASCC are as follows:

- Ch B Transmit Buffer empty
- Ch B External/Status Change
 - Zero Count of Baud Rate generator
 - DCD* pin transition
 - SYNC* pin transition
 - CTS* pin transition
 - Break detection
- Ch B Receive Character Available
- Ch B Special Receive Condition
 - Parity Error
 - Overrun error
 - Framing Error
- Ch A Transmit Buffer empty
- Ch A External/Status Change
- Ch A Receive Character Available
- Ch A Special Receive Condition

Usage Notes:

- The number of transmit stop bits can be selected but the receiver always checks for one stop bit.
- The ASCC contains both a receive data FIFO and a receive error FIFO so that receive errors can be stacked along with the associated receive characters. The act of reading the data pops both the data and error FIFOs. If status is needed it must be read before reading the data.
- The ASCC provides both Local-Loopback and Auto-Echo modes for diagnostic purposes.
- Each channel's baud rate generator output can be routed out to the associated TRxC* pin for diagnostic uses.
- Since the pointer bits in WR0 are always reset to zeros after an access, writes to WR0 and reads from RR0 can be done without first setting the pointer bits.
- When reading RR2, Channel A returns the base interrupt vector and Channel B returns a vector which includes status information.
- RR3, the interrupt pending register, can only be read from Channel A.
- All ASCC interrupt service routines should end with a RESET HIGHEST IUS command to the proper ASCC channel. In addition, if an error condition is present (such as Parity Error) then an ERROR RESET command should also be sent.
- The ASCC supports the generation of a BREAK signal in WR5, and detection of a break signal in RR0.
- WR5 controls the levels of the DTR* and RTS* pins on the ASCC device and at the serial connector if that is the function specified for those pins. These lines should be considered when handshaking problems are present.

6.1.3 Asynchronous and Synchronous Transfers.

The ability to transfer serial data to other computers and peripherals is one of the features that make Systemaster II a true single board computer. This is further enhanced by the ability to communicate with both asynchronous and synchronous protocols.

Asynchronous transmissions is defined as transmitting the smallest unit of data (one byte) independent of any other unit of data. Each byte is tagged with a start and a stop bit and also parity information. This type of transmission is used with slow speed devices such as terminals, printers and low speed modems. Systemaster II when equipped with the ASCC can provide all the intelligence needed for asynchronous transmissions in a variety of baud rates.

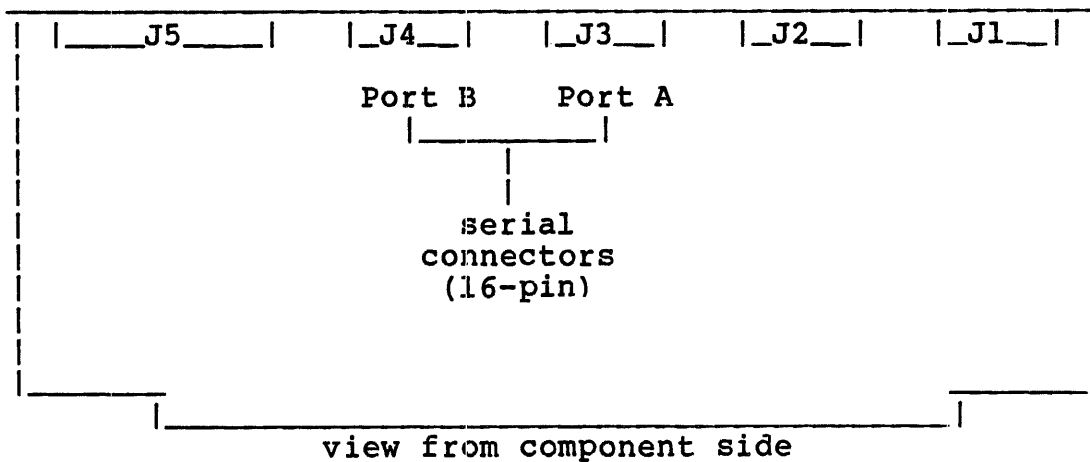
Synchronous transmissions are intended for high speed transfers as might be required when two computers are communicating. Synchronous transfers are a bit more complicated because they involve the transfer of a packet of bytes and special trailer and header characters depending on the protocol. Instead of transmitting a byte at a time, the data can now be packaged and transmitted in blocks at a very fast rate. This type of communications is also possible with Systemaster II. In order to do this, the ASCC is replaced with a SCC which is a part that handles synchronous protocols. Provisions for receiving a remote clock are provided onboard.

6.1.4 Serial Connectors

Systemaster II uses RS232-C to communicate serially to the outside world. RS232-C is a standard for connecting a defined set of wires from one computer to another or from computer to modem. The standard also defines the signal voltage transitions (+12 to -12) and the maximum distance (50 feet).

The ports on the ASCC are translated to RS232-C by U6 and U5 both of which are 75188 level translators. Signals coming from the connector are translated to TTL by U7 and U4 (75189s). The connectors on Systemaster II are 16-pin straight headers which are typically connected to a DB-25 connector through a ribbon cable. Pins on the DB-25 are aligned with the header by ensuring that pin 1 on the header plug is pin 1 of the DB-25.

Serial channels 0 and 1 are on connectors J3 and J4 respectively, as shown:



The following table shows the signal connections for each serial port and how they relate to the EIA pins. Both connectors have the same signal connections.

Header Pin	DB-25 Pin	EIA Signal	Direction from master
3	2	Transmitted data	In
5	3	Received data	Out
7	4	Request to send	In
9	5	Clear to send	Out
11	6	Data set ready	Out
13	7	Signal ground	
14	20	Data terminal rdy	In

The Systemaster II is considered a DCE (Data Communications Equipment) if you have problems communicating with another device make sure that the appropriate connections are made and that they are facing the correct direction.

6.2 CIO PARALLEL PORT CONTROLLER

Systemaster II provides two parallel ports controlled by a Zilog Counter/Timer and Parallel I/O Controller (CIO). The CIO is a parallel communications controller with additional interrupt and counter/timer capabilities.

6.2.1 CPU To CIO Interface

The CIO is I/O mapped and looks like four I/O ports to the Systemaster II as shown below:

CIO Port Address	

08h	Port C data
09h	Port B data
0Ah	Port A data
0Bh	Control

The CIO is operated at its full speed of 6Mhz. Communication with either a 6 or 8 MHz Systemaster II is ensured by dedicated logic that synchronizes both.

6.2.2 CIO Software Interface

The Z8536-CIO contains two 8-bit parallel ports, one 4-bit parallel port, three 16-bit counter/timers, and a set of internal registers to configure and control these parallel ports and counter/timers. The CIO has an external control port through which all internal registers are accessed. The CIO also has three external data ports, one for the data register associated with each parallel port.

Accessing the CIO internal registers is done with a state machine and a pointer register. The pointer register holds a value that addresses one of the CIO's internal registers. The state machine determines if accesses to the CIO control port are to the pointer register or to an internal register. The Zilog Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel I/O Unit Technical Manual gives a good discussion of the state machines operation. In general, after a reset operation the CIO is left in State 0. Reads from the control port in State 0 leave the state machine in State 0 and access the internal register currently addressed by the pointer register. Writes to the control port in State 0 update the pointer register and put the state machine into State 1. A read or write in State 1 accesses the internal register addressed by the pointer register and places the state machine back into State 0.

Each CIO parallel port or counter/timer is initialized by writing a stream of bytes to the control port. This stream of bytes contains pointer register values followed by register content values for loading the internal registers needed to configure the various operation mode.

The CIO supports a multitude of parallel port operating modes. The CIO parallel ports are used to support parallel printers and will be discussed in that context. Port A and Port B will each support one parallel printer. Port C provides the additional lines required to support handshaking. Port A and Port B allow specification of the following operating modes:

- Output Port with handshake modes
- Interlock Handshake
- Strobed Handshake
- Pulsed Handshake (in conjunction with Counter/Timer 3)
- Three-Wire Handshake
- Variable Deskew timing of the DAV handshake line
- Single or Double buffered mode
- Interrupts on one or two bytes
- Data line polarity
- Normal
- Inverted
- Data line drivers
- Normal Output
- Open Drain Output
- Pattern matching
- AND or OR matching
- Pattern Polarity (Normal/Inverted)
- Pattern Transition
- Pattern Match Mask
- Port A and Port B can be linked to operate as a 16-bit port

CIO interrupts are generated by Port A, Port B, and each of the three counter/timers. Each interrupt source has an associated control register and the CIO also has a Master Interrupt Control Register. Port A, and Port B each have a separate interrupt response vector. The counter/timers share one interrupt response vector. The CIO identifies the internal interrupt source being acknowledged by encoding status information into the returned interrupt response vector. At the end of any CIO interrupt service routine a RESET IUS command should be issued to the internal CIO source that generated the interrupt.

6.2.3 CIO Counter/Timers

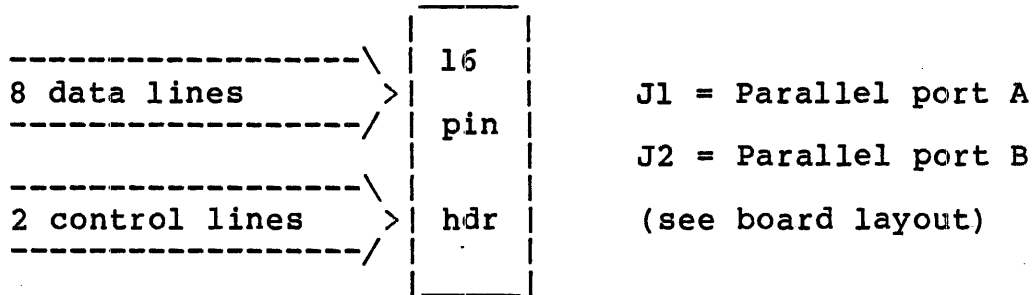
A added feature of the CIO is the provision of three independent 16-bit counter/timers. Each counter/timer is fully programmable for down count, time constant and mode of count.

Each of the CIO's three counter/timers allow the following operating modes to be specified:

- Continuous or Single-Cycle mode
- Output Waveform
- Pulse
- One-Shot
- Square-Wave
- Retrigger of counter in the middle of a countdown
- External access to
- Counter Output
- Counter Enable
- Count Input
- Trigger Input
- Gate Input
- Counter/Timer 1 (CT1) and Counter/Timer 2 (CT2) can be linked to form a 32-bit counter with the options of:
 - CT1's output gates CT2
 - CT1's output triggers CT2
 - CT1's output is CT2's count input

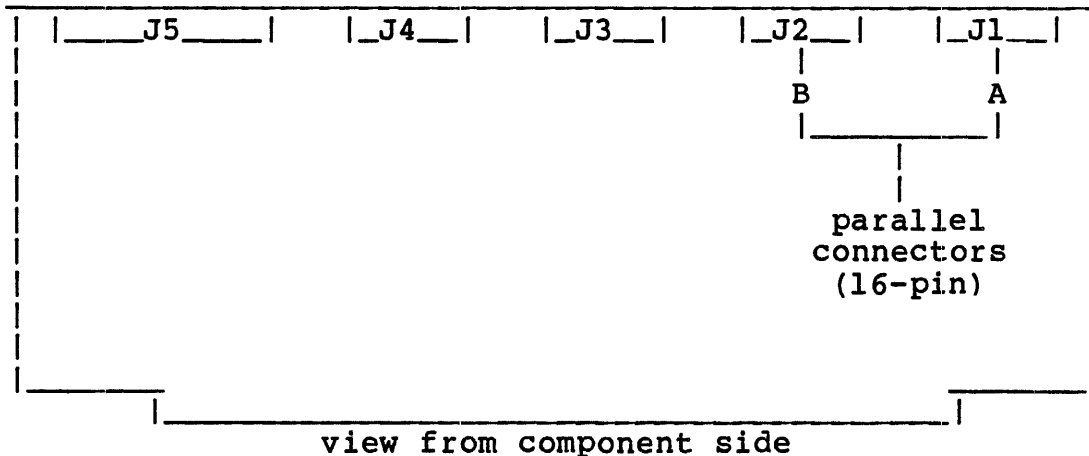
6.2.4 Parallel Connectors

The parallel ports on Systemaster II exit to the outside world through two 16-pin headers, each. in the following fashion:



As shown in the illustration, each port is configured (standard product) as an 8-bit output port with a data strobe and a acknowledge input. The typical devices attached to these ports are Centronics-type printers and peripherals. In most cases the cable required is a 16-conductor flat ribbon cable with a header plug on one end and a cinch connector on the other. An alternative to making your own cables is to order them from Teletek. The tables on the next page give the pinouts for each port and show their relation to the Centronics connector.

The following illustration shows the location of the parallel connectors.



Port A Signals

Signal Name	CIO pin	Header pin	Centronics pin
Port A data 0	33	15	2
Port A data 1	32	13	3
Port A data 2	31	11	4
Port A data 3	30	9	5
Port A data 4	29	7	6
Port A data 5	28	5	7
Port A data 6	27	3	8
Port A data 7	26	1	not used
/ACKINA	21	14	10
/DAVA	22	16	1
+5 volt		6	not used
Ground		8	19-30

Port B Signals

Signal Name	CIO pin	Header pin	Centronics pin
Port B data 0	8	15	2
Port B data 1	9	13	3
Port B data 2	10	11	4
Port B data 3	11	9	5
Port B data 4	12	7	6
Port B data 5	13	5	7
Port B data 6	14	3	8
Port B data 7	15	1	not used
/ACKINB	19	14	10
/DAVB	20	16	1
+5 volt		6	not used
Ground		8	19-30

It is important to note that the parallel ports are not buffered. This limits the distance that a peripheral can be located from the Systemaster II. This should not cause any problems as long as this distance is less than 15 feet. Should your application require longer cable lengths, Teletek recommends the addition of an external board containing single ended or differential drivers. Teletek's PPD board is available for this purpose.

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CHAPTER 7 - FLOPPY DISK INPUT/OUTPUT

Floppy disks are at present the most affordable and the most popular non-volatile storage medium in use with computers. As floppy densities rise and drive electronics become more sophisticated it is quite clear that the floppy subsystem will be with us for a long time.

7.1 DISK CONTROLLER

Systemaster II makes use of the latest technology in disk controllers by using the Western Digital WD2797-02 Floppy Disk Controller. This integrated circuit is very dense. The overall reliability of the floppy disk section is enhanced because this chip contains an internal data recovery circuit. Two external potentiometers and one trim capacitor are all that is required to adjust the circuit for operation with a large variety of disk drives.

7.2 CPU to FDC INTERFACE

The following are the floppy disk I/O port assignments:

FLOPPY DISK CONTROLLER PORT ASSIGNMENTS		
Address	Read	Write
-----	-----	-----
14h	Status	Command
15h	Track	Track
16h	Sector	Sector
17h	Data	Data
1Ch-1Fh	Sides	-

The first four ports are defined by the Western Digital WD2797 floppy disk controller. The last four addresses are the Read Write Control Port. (See section 4.6) Reading from any of the last four ports brings in the status of the floppy drive Dual Side signal on bit 0:

- Bit 0 = 0 The disk is single sided
- Bit 0 = 1 The disk is double sided

7.3 FDC SOFTWARE INTERFACE

The CPU communicates with the FDC (floppy disk controller) via programmed I/O reads and writes. All of the internal registers are programmed and checked for status in this manner. It is possible to poll the FDC for data transfers; however, the Systemaster II makes use of DMA and interrupts to maximize the transfer rate.

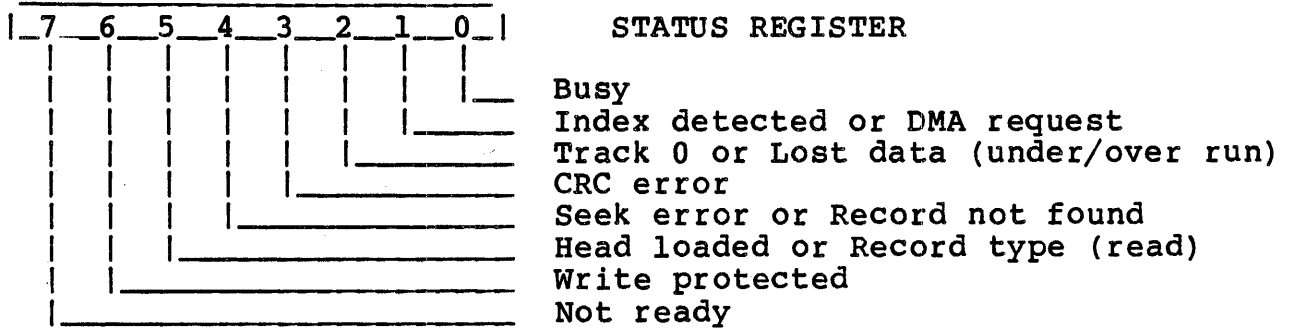
The FDC DMA request pin FDRQ is connected to the DMA RDY input. This signal is used by the FDC to request the initiation of a DMA transfer. The DMA is programmed to accept RDY as a high voltage level.

FDCINT is the FDC interrupt request signal that is used to post an interrupt to the 9519 controller. The 9519 accepts this signal as interrupt request #2 and uses the active low level option.

Other floppy disk drive control functions are implemented with an onboard control latch. These auxiliary control functions are drive select, disk density (FM or MFM), drive size (5.25 or 8 inch), and drive motor on/off. For more details on the control latch, see Section 4.4 of this manual.

7.3.1 Disk Controller Command Summary

(Programming Summary for WD 2797 FDC)



R1	R0	Step rate
0	0	3 or 6
0	1	6 or 12
1	0	10 or 20
1	1	15 or 30

length	Sector length
0	128 bytes
1	256 bytes
2	512 bytes
3	1024 bytes

Flag	Value	Action
E	0	No head load delay
	1	Delay 15/30 ms
H	0	Unload head
	1	Load head
L	0	Sector size times 2
	1	Normal sector size
M	0	Single sector
	1	Multiple sectors
U	0	Select disk side 0
	1	Select disk side 1
V	0	No verify
	1	Verify destination track

 FDC COMMANDS

Force interrupt > 1101 I3 I2 I1 I0

ACTION: terminate current command and interrupt on condition

INPUT: I0 not-ready to ready condition

I1 ready to not-ready condition

I2 every index pulse

I3 immediate interrupt

Rezero -----> 0000 H V R1 R0

(recalibrate)

ACTION: issues up to 255 step pulses until "zero" signal

OUTPUT: loads track with 0

Seek -----> 0001 H V R1 R0

INPUT: track register contains current track

data register contains track to seek

OUTPUT: track register contains new current track

Read address --> 11000 E 00

(read id)

OUTPUT: 6 bytes of data: 0 Track number

1 Side number

2 Sector number

3 Sector length

4,5 CRC 1 and 2

also puts track number in sector register

Read sector ---> 100 M L E U 0

INPUT: track register, sector register, side select

OUTPUT: sector data, status in status register

Write sector --> 101 M L E U 0

INPUT: track reg., sector reg., side select, sector data

OUTPUT: status in status register

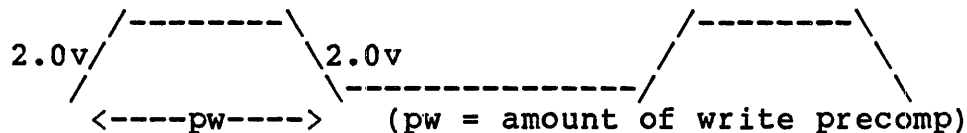
Write track ---> 11110 E U 0

(format track)

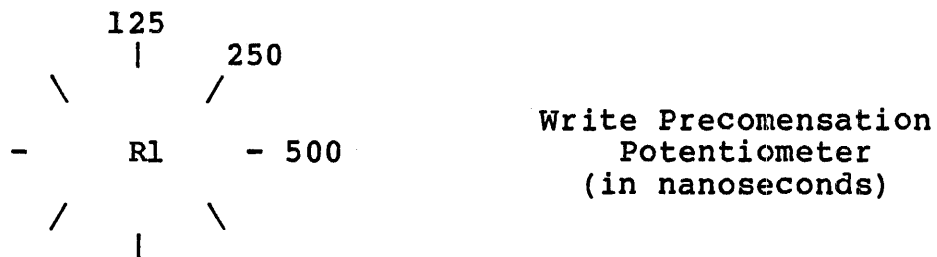
INPUT: selected track. all track format bytes

Write Precompensation Adjustment

1. Set /Test (pin 22) to a logic high. This is done by insuring that jumper E5 is out.
2. Strobe /MR (pin 19). On systems with front panel reset, simply reset. If your system does not have a front panel reset, momentarily short /MR to ground.
3. Set /TEST (pin 22) to a logic low. This is done by installing jumper E5.
4. Observe pulse width on WD (pin 31).
5. Adjust WPW (pin 33) for the desired precompensation value. This is done by monitoring the pulse width on pin 31 and adjusting pot R1 for the desired value. Measure the pulse width at TTL high levels.



It is possible to set the write precompensation even if you do not have an oscilloscope. Before each board leaves the factory, pot R1 is calibrated and has the three most common write precompensation settings marked on it. Simply refer to the drawing below and set the pot for the desired value. Note that the drawing is an approximation only; the location of the marks will vary from board to board



6. Set /TEST (pin 22) to logic high. This is done by removing the jumper at E5.

Data Separator Adjustment

1. Set /Test (pin 22) to a logic high. This is done by insuring that jumper E5 is out.
2. Strobe /MR (pin 19). On systems with front panel reset, simply reset. If your system does not have a front panel reset, momentarily short /MR to ground.

The disk controller must be adjusted for 8 inch double density. Once this is done the internal logic takes care of internal divides for the correct density and data rates. Therefore, it is very important that the size and density control bits are set correctly: FD-5/8 = 1, FD-D/S = 0. If these control signals are not correctly set, the test signals will be meaningless.

3. Set /TEST (pin 22) to a logic low. This is done by installing jumper E5.
4. Observe pulse width on TG43 (pin 29). Make all observations at TTL high levels.
5. Adjust pot R2 for 1/8 of the read clock (250 ns).
6. Observe frequency of DIRC (pin 16).
7. Adjust VCO trim pot C22 for the correct data rate (500 KHz).
8. Set /TEST (pin 22) to a logic high. This is done by removing the jumper at E5.

The following table is included for your convenience:

	5.25 inch		8 inch	
	FM	MFM	FM	MFM
Data Rate	125 Khz	250 Khz	250 Khz	500 Khz
Read Clock	8 us	4 us	4 us	2 us
1/8 of Read Clock	1 us	500 ns	500 ns	250 ns

**** WARNING ****

Ensure that jumper E5 is removed after all the adjustments have been made. While this jumper is installed the disk controller echoes its internal signals to several output pins including the data bus. This will definitely cause problems with the CPU.

7.5 DISK DRIVE INTERFACE

The drive interface consists mainly of signal conditioning logic. Signals to the drive are driven by high current sinking schottky drivers. Signals from the drive are received through schmitt devices which clean up the signal before it reaches the disk controller.

7.5.1 Drive Connector

The floppy disk controller interfaces to the disk drive via J5, a 50-pin header. The header conforms to the ANSI standard for 8 inch drives, as follows:

Ground Pin	Signal Pin	Signal
-----	-----	-----
1	2	/TG43
3	4	not used
5	6	not used
7	8	/TG43
9	10	/DS
11	12	not used
13	14	/SSO
15	16	not used
17	18	/HLD
19	20	/IP
21	22	/READY
23	24	not used
25	26	/DSEL0
27	28	/DSEL1
29	30	/DSEL2
31	32	/DSEL3
33	34	/DIR
35	36	/STEP
37	38	/WD
39	40	/WG
41	42	/TR00
43	44	/WPRT
45	46	/RRD
47	48	not used
49	50	/MOTOR

Connector J5 is a standard 50-pin header for 8 inch drives. To hook up 5.25 inch drives it will be necessary to transpose the signals to a 34-pin header. If you build this connector yourself make sure it conforms to the ANSI standard and refer to the schematics. Optionally, you may order an assembled and fully tested connector from Teletek.

7.4.2 Drive Signal Definition

The following is a brief description of the meaning and purpose of the drive interface signals. For a more explicit description of these signals, refer to the manual for your particular drives.

Signal	Direction	Meaning
/TG43	out	Track Greater than 43. An active low signal means a track above 43 is being accessed.
/DS	in	Double sided. An active low signal tells the controller the drive contains a double sided disk.
/SSO	out	Side Select Output. Selects either side of the diskette.
/HLD	out	Head Load. Controls the loading of the Read/ Write against the media.
/IP	in	Index Pulse. Informs the controller an index hole has been sensed.
/READY	in	Drive READY. This input indicates the drive is ready for access.
/DSEL0	out	Drive SElect 0. Selects drive 0.
/DSEL1	out	Drive SElect 1. Selects drive 1.
/DSEL2	out	Drive SElect 2. Selects drive 2.
/DSEL3	out	Drive SElect 3. Selects drive 3.
/DIR	out	DIRection. Controls the direction of the disk read/write heads.
/STEP	out	STEP Pulse. Moves the read/write heads one cylinder in either direction.
/WD	out	Write Data. Contains the MFM or FM encoded data being written to disk.
/WG	out	Write Gate. Informs the drive that a write operation is coming up.

/TR00	in	On TRack 00. Informs the controller that the heads are positioned over cylinder zero.
/WPRT	in	Write PRoTect. This signal informs the controller that the diskette in use is write protected.
/RRD	in	Read Raw Data. Contains the MFM or FM encoded data being read from disk.
/MOTOR	out	MOTOR control. Controls the drive motor. 0 = on. 1 = off.

7.4.3 Drive Configurations

Most floppy disk drives can be customized by the owner/user through the use of trace cuts, shunts, jumpers or switches. The supported customization options are described in the manual provided by the manufacturer of the floppy disk drive. Many of the options are purely personal preference; the factory settings are acceptable for use with the Systemaster II.

Three of the common floppy disk drive options are critical to the Systemaster II:

1. The Western Digital floppy disk controller checks the READY signal from a drive before selecting the side. For this reason, the drive must return the READY signal whenever a diskette is in the drive, regardless of the type of diskette and the side selected. Do not use READY qualified by the side selected and the number of sides. In other words, if a single sided diskette is in the drive and the second side is selected, the READY signal should be returned anyway.
2. The drive door should be locked with "HEAD LOAD".
3. The head should be loaded with the "HEAD LOAD" signal, not with the "SELECT" signal.

CHAPTER 8 - DIRECT MEMORY ACCESS (DMA)

Direct Memory Access (DMA) is a technique used to speed up data transfers. DMA operates by using a special controller that does only one thing, transfer data from one place to another. By using this dedicated controller it is not necessary to repeat CPU commands or read data into the CPU during a data transfer. Once the DMA is set up and started, the CPU "goes to sleep" while the DMA controller takes care of the transfer.

Systemaster II uses the Zilog Z80 DMA controller and makes full use of that chip's capabilities.

8.1 CPU to DMA INTERFACE

The DMA is I/O mapped at 18h to 1Bh. The CPU accesses the DMA chip's internal registers via I/O reads and writes. Internal register access is done with register base pointers.

8.2 DMA SUPPORT LOGIC

The DMA uses minimal support logic. The controller is operated at half of the CPU speed: 3 MHz on the 6 MHz board and 4 MHz on the 8 MHz board. No wait states are implemented on its RDY/WAIT line.

8.3 DMA CHANNELS

A DMA channel is essentially a transfer path with a source and a destination. The Z80 DMA is a single channel device; however, because its source and destination addresses are fully programmable, its performance is equal to or greater than that of most multichannel devices. On the Systemaster II, the possible transfer paths are:

- DMA to/from ASCC channels
- DMA to/from CIO channels
- DMA to/from floppy disks
- DMA to/from memory
- DMA to/from S-100 bus

(for slaves, hard disk controller, etc.)

8.4 DMA SOFTWARE INTERFACE

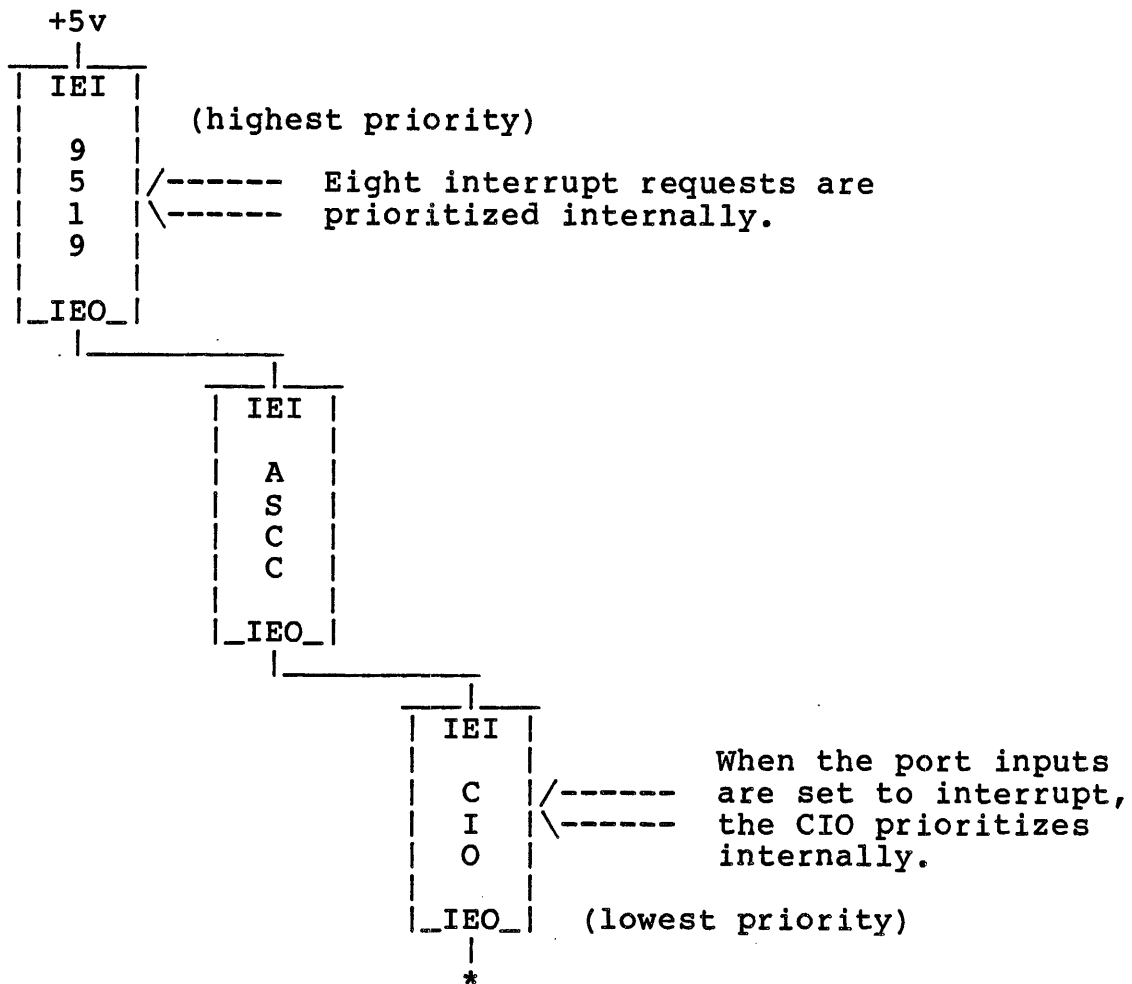
Operation of the DMA device is not trivial. As mentioned before, access to the internal registers is done with a pointer technique. Even the simplest transfer will require that most or all of the registers be loaded with a value. If you plan to write your own drivers, Teletek recommends that you purchase the Zilog Z80 DMA Technical Manual. See "Appendix D - Bibliography".

CHAPTER 9 - INTERRUPTS

9.1 INTERRUPT STRUCTURE

Prioritization of interrupt sources occurs in the following three areas:

1. The Z80 daisy-chain interrupt scheme implements interrupt priorities between actual hardware devices based on their physical location in the daisy-chain. This daisy-chain includes the AM9519 interrupt controller, the Z8531-ASCC, and the Z8536-CIO in that order with the AM9519 at the start of the daisy-chain as shown below.



2. The AM9519 prioritizes its 8 interrupt request inputs.
 - 74LS74 Parity Error Latch
 - WD2797 FDC interrupts
 - S-100 bus Vectored Interrupt Lines (V10-V14)
3. The Z8531-ASCC and Z8536-CIO each contain an internal daisy-chain which prioritizes interrupt sources internal to the particular device.

A device on the daisy-chain which has an interrupt under service will prevent any other devices further down the daisy-chain from posting interrupts. The CIO and ASCC will disable the lower daisy chain if either an Interrupt Under Service bit is set or the Disable Lower Daisy-chain (DLC) bit is set. The AM9519 will disable the lower daisy-chain if an interrupt is under service and its ISR bit is set. The AM9519 also disables the lower daisy-chain when the Master Mask control bit M7 in the mode register is set to 0, both disabling the lower daisy-chain and disarming the AM9519.

The table on the next page is a map of the interrupt structure hierarchy based on interrupt source priorities and listing all possible sources from the interrupting devices. During a Z80 mode 2 interrupt acknowledge cycle, the Z8531-ASCC and Z8536-CIO devices have the ability to alter a base interrupt vector response byte to indicate which internal interrupt source is being acknowledged (called Vector-Includes-Status mode). The bits that are modified in the base vector are listed in the <Status Vector> column. Note that the priorities of the internal interrupt sources in the ASCC and CIO do NOT correspond one-to-one with the modification of the base interrupt vectors.

Not all interrupting devices are used in Vector-Includes-Status mode, but vectors have been assigned and entries have been allocated in the interrupt vector table for all possible interrupt sources.

 Interrupt Priority Map

Source Device	Condition	Status Vector
<highest>		
9519-VI0	74LS74 Parity ERROR*	
VI1	available	
VI2	WD2797 INTRQ*	
VI3	S-100 - VI0	
VI4	S-100 - VI1	
VI5	S-100 - VI2	
VI6	S-100 - VI3	
VI7	S-100 - VI4	
Z8531-ASCC	Ch A Rx Special Cond.	----111x
	Ch A Rx Buffer Full	----110x
	Ch A Tx Buffer Empty	----100x
	Ch A EXT/STATUS	----101x
	Ch B Rx Special Cond.	----011x
	Ch B Rx Buffer Full	----010x
	Ch B Tx Buffer Empty	----000x
	Ch B EXT/STATUS	----001x
Z8536-CIO	Counter/Timer #3	-----00x
	Port A	----000x to ----111x
	Counter/Timer #2	-----01x
	Port B	----000x to ----111x
	Counter/Timer #1	-----10x
	Counter/Timer ERR	-----11x
<lowest>		

Each interrupt source in the AM9519 has its own interrupt response vector. There are base interrupt response vectors for each of the following ASCC or CIO interrupt sources:

- ASCC uses only one base vector
- CIO Port A base vector
- CIO Port B base vector
- CIO Counter/Timer base vector

9.2 INTERRUPT CONTROLLER

Systemaster II's interrupt capabilities are enhanced by the use of a programmable interrupt controller. The AM9519 Universal Interrupt Controller (9519 UIC) is an interrupt handling device that manages the masking, priority resolution and vectoring of up to eight interrupts.

9.2.1 CPU to UIC Interface

The 9519 UIC is I/O mapped at 10h to 13h. I/O ports 10h and 11h are tied to the 9519 data port and command/status port, respectively. The ports are duplicated at 12h and 13h.

Interrupt Controller Ports		
Address	Read	Write
-----	-----	-----
10h	Data	Data
11h	Status	Control

9.2.2 Interrupt Assignment

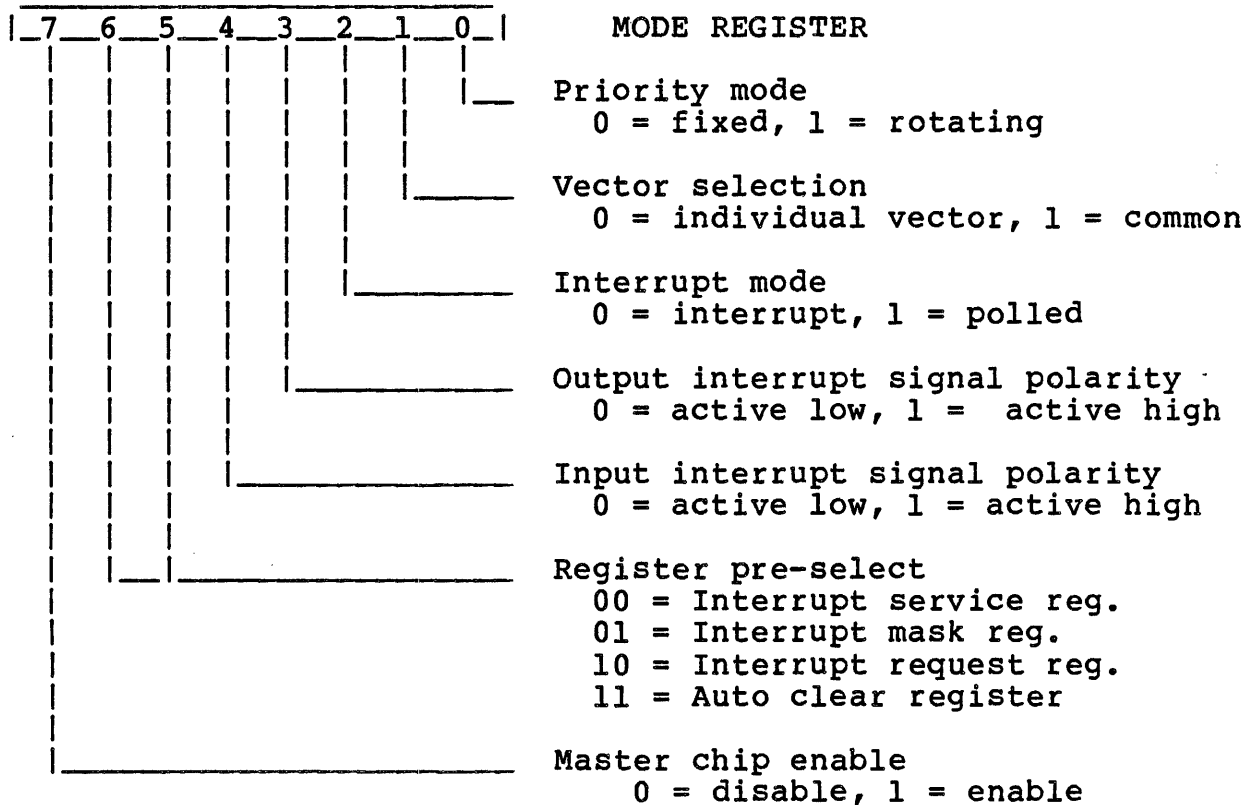
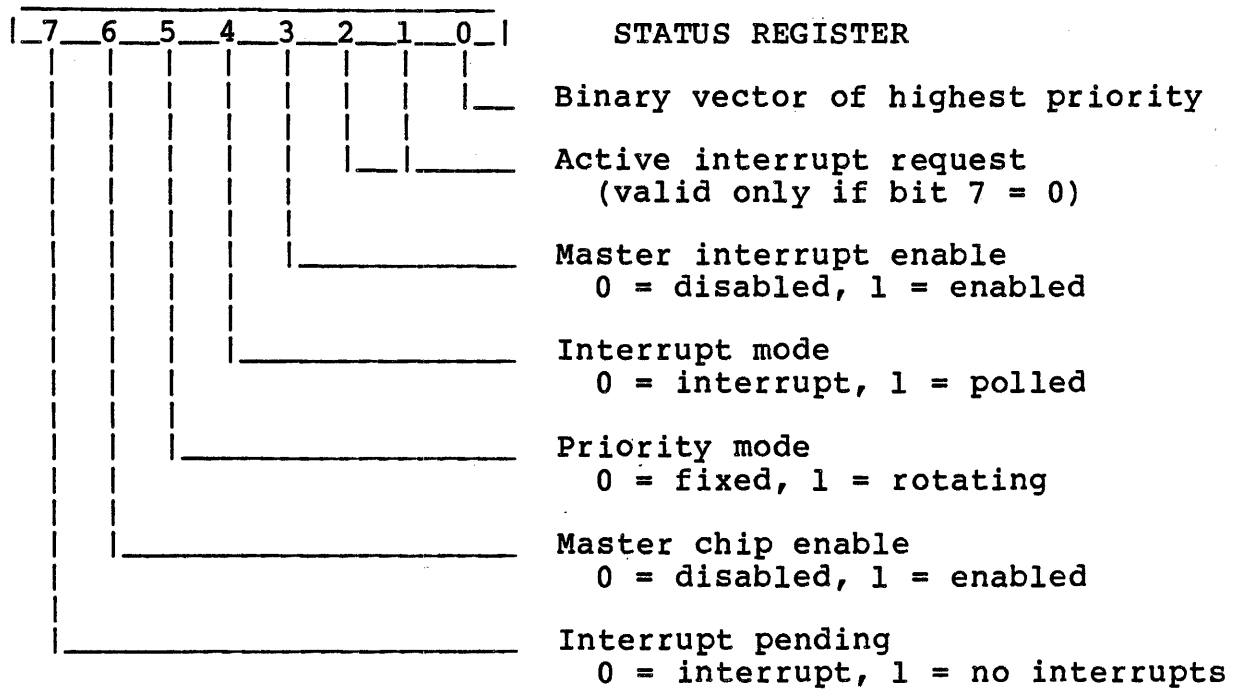
The interrupt request inputs of the 9519 are fully programmable for polarity: high or low. The Systemaster II uses active low polarity. The eight inputs are prioritized as follows:

IREQ0*	74LS74 Parity ERROR*
IREQ1*	available
IREQ2*	WD2797 INTRQ*
IREQ3*	S-100 - V10
IREQ4*	S-100 - V11
IREQ5*	S-100 - V12
IREQ6*	S-100 - V13
IREQ7*	S-100 - V14

9.2.3 UIC Software Interface

The 9519 Interrupt Controller must be enabled to receive interrupts from the Z8531 ASCC or the Z8536 CIO. If the 9519 is disabled, the lower daisy-chain will also be disabled, preventing interrupts from the lower priority interrupting devices.

9.2.4 UIC Register Bit Definitions



9.2.5 UIC Command Summary

0000 0000	Reset
0001 0000	Clear all IRR and IMR bits
0001 1xxx	Clear IRR and IMR bits xxx
0100 0000	Clear all IRR bits
0101 0000	Set all IRR bits
0100 1xxx	Clear IRR bit xxx
0101 1xxx	Set IRR bit xxx
0010 0000	Clear all IMR bits
0011 0000	Set all IMR bits
1011 0000	Preselect IMR for loading
0010 1xxx	Clear IMR bit xxx
0011 1xxx	Set IMR bit xxx
1100 0000	Preselect auto clear register for loading
111BY1 BY0xxx	Load BY1 and BY0 into interrupt response byte count (see table below) and preselect reponse memory xxx
0110 0000	Clear highest priority ISR bit
0111 0000	Clear all ISR bits
0111 1xxx	Clear ISR bit xxx
100x xxxx	Load mode register bits 4-0 with xxxxx
1010 xx00	Load mode register bits 6-5 with xx
1010 xx01	Load mode register bits 6-5 with xx and set mode register bit 7
1010 xx10	Load mode register bits 6-5 with xx and clear mode register bit 7

Interrupt response bytes

BY1	BY0	byte count
0	0	1
0	1	2
1	0	3
1	1	4

APPENDIX A - SPECIFICATIONS

CPU	Z80B (6 MHz) or Z80H (8 MHz)
SPEED	6 MHz: 0 wait states for all RAM cycles as well as all offboard memory acesses. 2 wait states (536 ns) for EPROM. 8 Mhz: 1 wait state for all RAM cycles as well as all offboard memory acesses. 3 wait states (525 ns) for EPROM.
MEMORY	RAM: Stacked 128K bytes dynamic RAM with parity, in two 64K banks. 128 cycle, 2 ms refresh rate required. 6 MHz board uses 150 ns devices. 8 MHz board uses 120 ns devices. EPROM: 28-pin socket defined for JEDEC approved INTEL universal site for EPROMS. 450ns, 2K device standard. Provisions for removing from memory map and automatic enable at 0000h upon power-up or reset.
PERIPHERALS	Two serial ports implemented with 6 MHz Zilog Z8531 ASCC. Both with full modem handshake. RS-232 drivers onboard. Two parallel ports implemented with 6 MHz Zilog Z8536 CIO. Ports can be configured for two full Centronics devices, optional SCSI or IEEE 488 ports, or multiprocessing communication.
CLOCK	Zilog CIO provides interrupt time clock for use as chronograph or multiprocessing timer.
FLOPPY DISKS	Support for 4 single/double sided, single/double density, 8 inch and 5.25 inch floppy disk drives. Implemented with Western Digital's WD2797-02.

DMA 1 DMA channel controlled by a Zilog DMA running at half the speed of the CPU: 3 MHz on the 6 MHz board and 4 MHz on the 8 MHz board. The hardware request is assigned to floppy for byte transfers.

INTERRUPTS Vectored interrupts provided by AMD9519A-1 for onboard devices. Interrupts are assigned for FDC, DMA and parity error. Five interrupt inputs are available on the S-100 bus for true vectored interrupt control.

BOARD Four layer board, 5.125" x 10.00", excluding edge connector. Solder masked. Silk screened.

POWER +5 volts @ 2.0 amps
 +12 volts @ 40 milliamps
 -12 volts @ 40 milliamps

COOLING Forced air cooling is required.

APPENDIX B - BOARD LAYOUT DIAGRAM

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APPENDIX C - SCHEMATIC DIAGRAMS

The schematic diagrams shown on the following pages are proprietary to TELETEK ENTERPRISES INC. and are copyrighted.

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APPENDIX D - BIBLIOGRAPHY

Zilog literature

The Z80B/Z80H Technical Manual
The Z8530 SCC Technical Manual
 (includes ASCC information)
The Z8536 CIO Technical Manual
The Z80 DMA Technical Manual

Available from:

 Zilog Incorporated
1315 Dell Avenue 99 South Bedford St.
Campbell, CA 95008 or Burlington, MA 01803
(408) 370-8120 (617) 273-4222

PLA literature

Monolithic Memories
2175 Mission College Blvd.
Santa Clara, CA 95050
(408) 970-9700

AM9519 literature

MOS Microprocessors and Peripherals Databook
Advanced Micro Devices
901 Thompson Place
P.O. Box 3453
Sunnyvale, CA 94088
(408) 732-2400

WD2797 literature

Western Digital
2445 McCabe Way
Irvine, CA 92714
(415) 941-0216

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 APPENDIX E - GLOSSARY

This glossary is a summary of the abbreviations used in this manual. It is intended only as a general reference for readers who have limited experience with computer hardware and the many abbreviations used to describe it. This is in no way a complete list of the jargon used in this manual.

Units

s	seconds	
ms	milliseconds	thousandths of a second
us	microseconds	millionths of a second
ns	nanoseconds	billionths of a second
K	kilobytes	multiples of <u>1024</u> bytes
KHz	kilohertz	thousands of cycles per second
MHz	megahertz	millions of cycles per second.

Industry Abbreviations

RAM	random access memory
ROM	read-only memory
PROM	programmable read-only memory
EPROM	erasable programmable read-only memory
EEPROM	electrically erasable programmable read-only memory
CPU	central processing unit
HCT	high speed CMOS technology
IC	integrated circuit
I/O	input/output
LS	low power shottky
PCB	printed circuit board
S	shottky
TTL	transistor-transistor logic

Generic Part Numbers

2716	2K x 8-bit EPROM
2732	4K x 8-bit EPROM
2764	8K x 8-bit EPROM
27128	16K x 8-bit EPROM
27256	32K x 8-bit EPROM
74HCT00	hex inverter
74HCT74	dual D latch
74LS32	quad OR gate
74LS164	8-bit parallel output serial shift register
74LS221	dual one-shot
74LS259	8-bit addressable latch
74LS280	parity checker/generator
74LS393	dual 4-bit counter

Manufacturer's Part Numbers

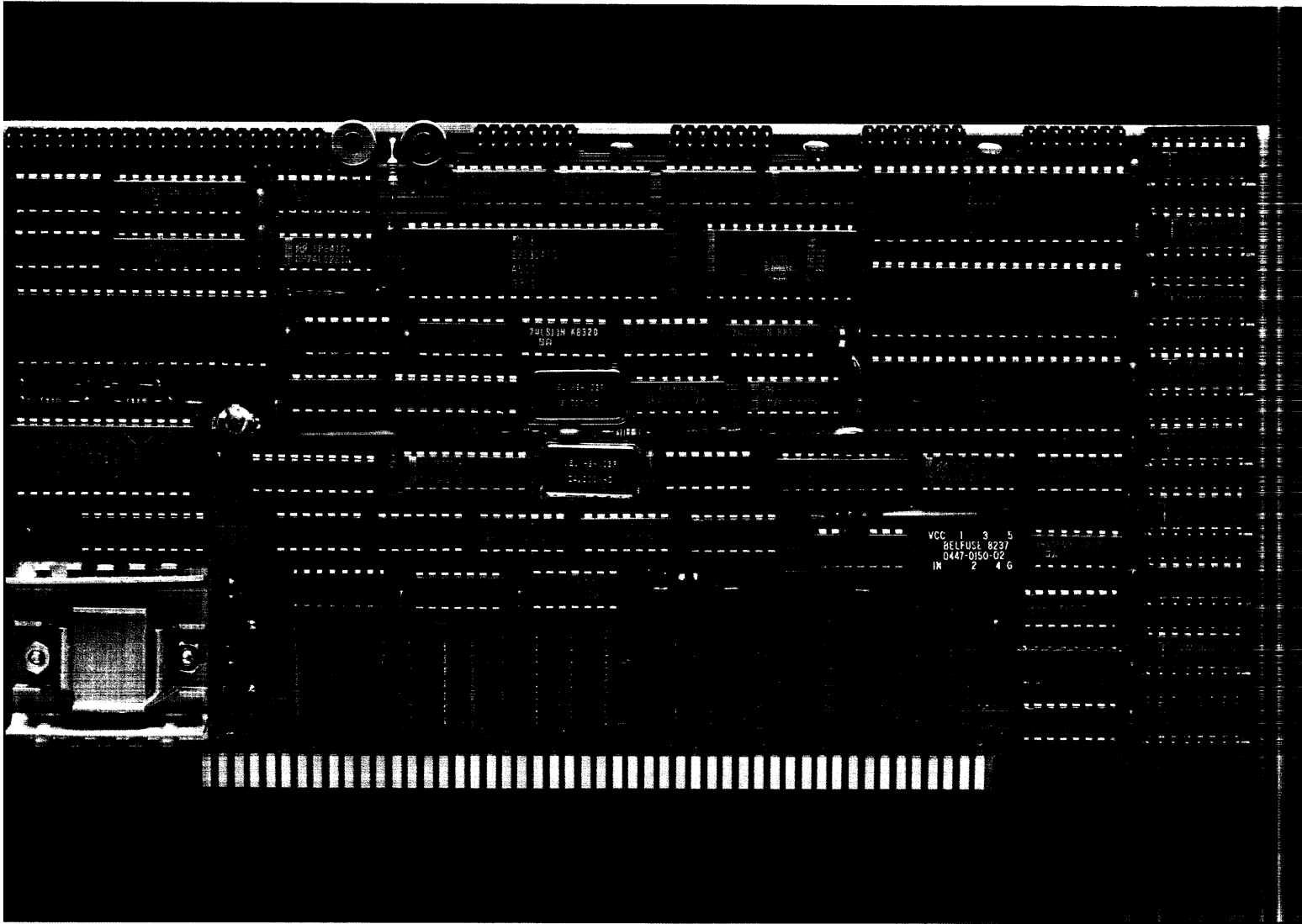
AM9519	Advanced Micro Devices Universal Interrupt Controller (UIC)
Z8536	Zilog Counter/Timer and Parallel I/O Unit (CIO)
WD2797	Western Digital Floppy Disk Controller (FDC)

Manufacturer's Abbreviations

ASCC	Zilog Asynchronous Serial Communication Controller
CIO	Zilog Counter/Timer and Parallel I/O Unit (Z8536)
UIC	Advanced Micro Devices Universal Interrupt Controller (AM9519)

Systemmaster II[®]

128K, 6/8 MHz



TELETEK 4600 Pell Drive
Sacramento, CA 95838
(916) 920-4600

Systemmaster II[®] Specifications

128K, 6/8 MHz

Design Philosophy

The Teletak Systemmaster II[®] is the next evolutionary step in our line of S-100 master boards. Our first introduction was the FDC-I in 1980 followed by the Systemmaster in April of 1982. Now, with a larger and more sophisticated end-user base, demand for faster systems, with more memory, is increasing. Teletak's response to this demand is the Systemmaster II[®], an ideal four-function master board for a single-user system, or a cost-effective high performance system controller/file server for a multi-user, multi-processing system, capable of supporting 8-bit and/or 16-bit slaves.

The Systemmaster II[®] is an 8-bit, four-function single board computer which fully conforms to the S-100/IEEE-696 standard.* The Systemmaster II[®] achieves optimum performance in multi-user systems when combined with SBC-I's, SBC-II's, or SBC 86/87's from Teletak. The Systemmaster II[®] will also support slave boards by other manufacturers when appropriate software drivers are provided.

CPU

Systemmaster II[®] has a Z80B microprocessor operating at 6 MHz in the standard configuration. An optional Z80H operating at 8MHz is also available. This flexibility in CPU speeds offers the system integrator the freedom to design a system with consideration for the cost versus performance issues.

RAM Memory

One row of stacked 64K DRAMs provide two 64K banks of parity checked RAM for a total of 128K of memory. The banks are software selectable and parity functions may be disabled. The RAM is optimized for use with CP/M 3.0 or TurboDOS 1.3 banked memory requirements.

ROM Memory

The JEDEC approved ROM layout is used on Systemmaster II[®]. That is, a 28 pin socket may be configured to handle the following devices: 2716, 2732, 2764, 27128 or 27256. This capability allows the user to run application firmware of up to 32K bytes. Memory space is maximized by providing the capability to enable or disable the ROM from the memory area. When this is done, the full 64K addressing range may be used for RAM. The ROM is automatically enabled upon power up or reset. The Systemmaster II[®] comes with 2K of ROM in the standard configuration.

Direct Memory Access (DMA) Controller

The Z80A DMA controller makes full use of memory speed by controlling high speed transfers onboard and over the bus. The flexibility of this device provides for "memory to I/O", "I/O

to memory" and "memory to memory" transfers. The hardware DMA request is dedicated to the floppy controller, however, software DMAs may be initiated for memory and I/O.

Serial Ports

Two RS232C serial channels are provided for communications with terminals and other serial devices. Both channels are full duplex at 50 to 19200 baud. Full modem handshake is provided for each channel, and baud rates to each port are software selectable. The standard configuration comes with a Zilog ASCC for asynchronous communications. An optional SCC may be substituted for synchronous protocols like SDLC. RS232 drivers are onboard, thus there are no paddle boards required, resulting in clean, neat packaging.

Parallel Ports

Systemmaster II[®] provides two independent 8-bit, bidirectional parallel ports. Parallel port control is provided by the Zilog CIO which supports various combinations of handshake and data transfers. In the standard configuration, both ports support Centronics interfaces. Both ports may be combined to form a 16-bit port.

An optional adapter may be attached that will enable the user to control test and lab instrumentation via IEEE-488 (GPIB) control, or convert the ports into a SCSI interface for control of hard disks and other devices.

Interval Clock

The CIO has three independent 16-bit counter/timers which are software controlled. One timer is used for a "tick clock" used in system management. The other two CTCs are available for software time related functions.

Interrupts

Systemmaster II[®] uses the Zilog mode 2 interrupts. The serial and parallel controllers are in an "interrupt daisy chain". The rest of the controllers are supported by an AMD9519 which provides eight individual programmable and vectored interrupts. The interrupts are assigned to the DMA, floppy disk, and parity functions while the remaining five interrupts are available for the S-100 bus. Providing true vectored interrupts to the S-100 bus will raise system efficiency by allowing interrupt driven communications to slaves and other devices on the bus.

Floppy Disk Control

Flexible disk control is managed by the Western Digital WD2797. This IC has an on-chip phase lock loop-data recovery circuit and prewrite compensation that provide high performance for the following capabilities:

- Single density (IBM 3740) or double density (System 34) data transfers under software selection and control.
- IBM diskette formatting capability.
- Simultaneous control of single or double sided drives.
- Simultaneous control of up to four 5.25" and/or four 8" drives.
- Multiple sector read/write.
- Automatic seek with verify.
- Software control of motor and media sense drive signals.
- Selectable sector sizes of 128K, 256K, 512K or 1024K bytes.
- CRC error detection.
- Programmable step rates for single density diskettes of:
 - 6ms, 12ms, 20ms, and 30ms.
- Programmable step rates for double density diskettes of:
 - 3ms, 6ms, 10ms, and 15ms.

Software

The Systemmaster II[®] is supported under both TurboDOS 1.3 and CP/M 3.0. A single, intelligent, on-board EPROM will boot either operating system from floppy or hard disk, providing convenience and ease of operation to the end user. The software dynamically determines the size, density, number of sides and number of tracks of each floppy disk in the system thereby increasing the user "friendliness" of the system. Extensive use of DMA, buffered console I/O and printer output, cache disk buffering and optional RAM Drive provide for high speed operation. The memory banking capability of the Systemmaster II[®] hardware is exploited to provide a TPA of over 63K under TurboDOS 1.3 and 60K under CP/M 3.0.

Utility programs to configure the system and to format, backup, and verify most kinds of disks are provided in addition to the standard utility programs available with each operating system. Teletak's popular Tape Utility, for archiving data to cartridge tape, is also supported under both operating systems.

(Specifications subject to change without notice)



SYSTEMASTER versus SYSTEMASTER II TurboDOS System Implementation Differences

OVERVIEW

Teletek's implementation of TurboDOS on the Systemaster II includes significant improvements in all areas of the software. Compared with the driver code for the original Systemaster (here called Systemaster I, for clarity), the code for Systemaster II is faster, smaller, more flexible, more modular, and generally easier to use. This document will highlight the most important differences.

FLOPPY DISKS

Two major improvements have been made to the Systemaster II TurboDOS floppy disk implementation: 5.25 inch mini-floppy disk support has been included, and all disk formats have been changed to be more flexible. Data exchange between systems is supported through the standard CP/M single density format and through all four standard TurboDOS formats.

The Systemaster II supports both 8 inch and 5.25 inch disk drives. Both sizes may be installed in the same system, allowing you to copy files from one size to the other. The system will cold-boot from either size. Once the operating system has been GENed for the particular drive mix being used, both the system and the diskette format program (SM2FMT) will automatically self-adjust as you switch between different size drives. Among other changes, the format program will present a menu appropriate to the size of the diskette selected for formatting.

You can now format diskettes with any of four sector sizes in either single or double density. You may also select the operating system (logical) disk parameters most suitable to your application. For example, you may increase or decrease the number of directory entries on a particular disk and that disk will remain compatible with all other Systemaster II disks, standard or non-standard. For your convenience, the most popular formats are simple menu choices in the format program. Other formats can be designed by selecting the custom format option.

The format program is set up standard for 77 tracks per side on 8 inch drives and 40 tracks per side on 5.25 inch drives; however the number of tracks for 5.25 inch drives is a patchable variable and may be changed with the TurboDOS MONITOR command. (The byte is at location 0104 hex when the format program is viewed from the MONITOR. The most common values are 23, 28 and 50 hex, for 35, 40 and 80 tracks per side, respectively.) Disks

FLOPPY DISKS (continued)

with different numbers of tracks may be mixed in the operating system with no difficulty. Note, however, that disks written with different track spacings may NOT be mixed between drives; disks written on a 48 tpi drive cannot be read on a 96 tpi drive, and vice versa.

All Systemaster II diskettes have at least one reserved track to allow them to be labeled with a format description. Parameters such as the number of tracks, the size of the sectors, and the number of directory entries are read from this label each time the disk is inserted, and are used to construct a temporary disk format table in the operating system. In addition to vastly increasing the flexibility of diskette formats and speeding the process of logging on each new diskette, this use of disk labels eliminates unused format tables from the operating system.

Due to the number of supported diskette formats, the memory savings from the elimination of disk tables is considerable. With two drive sizes, four sector sizes, two densities, two sides, and innumerable choices for block size, directory size and number of tracks, over 1200 different floppy disk formats are possible. Without the use of diskette labels, the tables for all these formats would require over 16K of system memory. With the use of disk labels, only 56 bytes are required.

The reserved track results in a loss of 4K to 8K of available data space on 8 inch floppy disks, when compared to similar formats for Systemaster I. Since most work is done on hard disks anyway, Teletek does not feel this should be a problem.

HARD DISKS

There are several major improvements in the HD/CTC drivers for Systemaster II over those designed for Systemaster I. These improvements include sector skewing, DMA data transfers, an optional interrupt driven protocol, and the ability to cold-boot the system directly from the hard disk.

The use of sector skewing in the new Systemaster II driver for HD/CTC (SM2HD) makes the hard disk format incompatible with the format used previously. However, compatibility between old and new systems is possible. To make a Systemaster II system compatible with an existing disk, the Systemaster II may use the generic hard disk driver (HDCTC). To make a non-Systemaster II system compatible with the new format, skewing can be added to the "HDCTC" driver by adding the following patch to the PAR file:

```
SKWTBL = 00,05,0A,0F,04,09,0E,03,08,0D,02,07,0C,01,06,0B
```

HARD DISKS (continued)

The interrupt driven protocol is selectively enabled by a patch parameter, allowing the standard HD/CTC hardware to be used with the new driver. Maximum system performance is obtained by modifying the HD/CTC for S-100 vectored interrupts and suitably setting the hard disk interrupt patch parameter.

All of these improvements together allow the system to read multiple hard disk sectors per disk rotation. Use a 1K disk buffer size in the TurboDOS operating system.

For more complete details on using the HD/CTC, including how to boot directly from the hard disk, read document C1014-A.02, "How to Optimize HD/CTC Performance with Systemmaster II". This document is available from Teletek.

SERIAL PORTS

Improvements in the serial port drivers include interrupt driven output buffers as well as interrupt driven input buffers, and a multi-channel serial communications manager.

The interrupt driven output buffers allow optimum data output to printers and terminals. Remember, TurboDOS does background multi-tasking. During the time a process is running it may send buffered data, and while the process is not running the data will continue to be sent from the buffer to the printer or terminal.

The multi-channel serial communications manager allows additional serial communications channels to be added to the system by writing additional drivers and linking them into the operating system. For example, the Teletek PSIO board could add an additional four communication ports to a system with the appropriate drivers. These additional communications ports would be directly accessible by the TurboDOS T-functions 34 through 40.

PARALLEL PORTS

The parallel ports include interrupt driven output buffers as described in the serial port section above.

NETWORK DRIVERS

The network drivers have been redesigned to allow DMA data transfers, optional interrupt protocol, and reentrant execution by multiple processes. Complete information may be found in document C1014-A.03, entitled "Systemmaster II Network Options". This document is available from Teletek.

TELETEK READ/WRITE DISK VERIFY UTILITY
for TurboDOS

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TVERIFY Command The TVERIFY command scans a disk for bad blocks, and marks them so that TurboDOS will avoid using them.

Syntax

```
TVERIFY {d:}
```

Explanation

The TVERIFY command tests every block on the disk identified by "d:". (If the "d:" parameter is omitted, TVERIFY will prompt you for a drive letter.) Each block is tested by first reading and saving the original data from the block, then writing any optional test patterns into the block and verifying each pattern, and finally re-writing the original data back into the block and verifying it. If bad blocks are detected, TVERIFY will tell you how many were encountered and will create a read-only directory entry under the name BLOCKS.BAD in the current user area to reserve the defective blocks and prevent their subsequent use by TurboDOS. The disk to be verified must be attached to the processor in which the command is executed. Use of the TVERIFY command is restricted to privileged log-ons only.

Up to eight test patterns may be used. These test patterns are suggested:

```
01010101  10101010  11001100  00110011  
11110000  00001111  11111111  00000000
```

If you enter 0 for the number of test patterns, the program reverts to a read-only verification like the VERIFY command supplied by Software 2000 on the TurboDOS distribution diskette.

The execution time for TVERIFY will vary greatly depending on the number of test patterns chosen and the size and speed of the drive. A read-only verify of a single density floppy usually completes in less than a minute. Testing all eight patterns on a 20 megabyte formatted hard drive may take as long as four hours.

TELETEK READ/WRITE DISK VERIFY UTILITY
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Example #1:

0A} TVERIFY B:How many test patterns would you like to use (0-8)? 0

Insert disk to be verified in drive B

Enter <CR> to begin verifying: [RETURN]Preparing to verify disk,
DO NOT INTERRUPT

Verifying blocks on drive: B

.....
Verify completed - 0 bad blocks found

0A}

Example #2:

0A} TVERIFY

Select disk to verify: B

How many test patterns would you like to use (0-8)? 2Input test pattern in binary (ie: 10101010, etc.): 00110011Input test pattern in binary (ie: 10101010, etc.): 11001100

Insert disk to be verified in drive B

Enter <CR> to begin verifying: [RETURN]Preparing to verify disk,
DO NOT INTERRUPT

Verifying blocks on drive: B

.....
Marking bad blocks in directory

Verify completed - 4 bad blocks found

0A}

TELETEK READ/WRITE DISK VERIFY UTILITY
for TurboDOS

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Error Messages

Non-privileged user
Unable to execute from bank 1
Unable to lockout verify drive
Verify drive not ready
Not enough memory for bad block list
Error marking bad blocks
Bad sector in disk directory

1.0 INTRODUCTION

The new Systemaster II TurboDOS system includes three different network options/drivers for use with different slave boards and different system requirements.

In the following section, each of the Systemaster II TurboDOS network options will be presented in detail. The required operating system modules and configuration parameters will be included.

The third section of this document will provide an example of how to implement a mixed SBC-I and SBC-II TurboDOS system.

The last section of this document will give some pointers on how to get the maximum performance out of the new network drivers provided with the Systemaster II.

Some of the configuration parameters will be presented as "xxxxx@". In these cases the true parameter name will be formed by substituting a letter (A, B, C, etc.) for the "@" on all parameters depending on what order the network drivers appear in the TurboDOS GEN file. For example, if a driver is the first network driver in the GEN file, all of its parameters will be of the form "xxxxxA" and the next network drivers parameters will be of the form "xxxxxB".

We will occasionally make reference to a "slave", this is one slave processor, not one slave board (eg: the SBC-II is two slaves but only one board).

Refer also to the Software 2000 TurboDOS IMPLEMENTOR'S GUIDE for complete descriptions of network configuration parameters built into the TurboDOS operating system.

2.1 Network option 1

The 'SM2MX2' network driver (network option 1 in the GEN and PAR files) supports both SBC-I and SBC-II slaves in mixed systems. This driver is basically the same as the network driver for the original Systemaster, and may be used with the standard Teletek TurboDOS slave boot proms. Changes from the Systemaster network driver were made to timing delay constants to allow for the faster processor on the Systemaster II.

This network driver supports a total of 16 slaves in the system. This includes combinations of SBC-I and SBC-II slaves however, the SBC-II slave currently will not work with this driver under TurboDOS 1.41 (only TurboDOS 1.3).

This driver uses a complicated hard-pollled network protocol and a poll routine to poll the slaves. This allows one network transaction to be in process at a time. This polled protocol makes this the slowest network driver option.

2.1.1 Modules required

The modules required in the Systemaster II operating system for this network option are:

'SM2MX2'	Systemaster II network driver
'@INT0' or '@INT9'	Only if SBC-I slaves are in system
'INT02' or 'INT92'	Only if SBC-II slaves are in system

The SBC-I slaves must use the 'NETSX1' slave network driver and the 'HNITS1' or 'HNITSB' initialization modules. The SBC-II slaves must use the 'NETSX2' slave network driver and the 'HNITS2' initialization module.

Standard SBC-I and SBC-II slave TurboDOS boot proms must be used.

2.1.2 Configuration parameters

The SM2MX2 driver has five patchable parameters as follows:

CKTNUM	This byte value is the circuit address/number that this network driver controls.
NMBSLV	This byte value between 1 and 16 (1-10 hex) is the number of slaves on this network circuit and the number of slaves the SM2MX2 is to service (1 per SBC-I and 2 per SBC-II).
SLVPAT	This 16 byte table is the slave port address table. It contains the base address for each slave on the network circuit.

SLVSST This 16 byte table is the slave file suffix character table. It contains one character for each slave, this character is appended to the filename "OSSLAVE" to identify the slave's download file ("OSSLAVEx.SYS").

TYPTBL This 16 byte table is the slave type table. For each slave it contains either a "1" for an SBC-I slave or a "2" for an SBC-II slave.

```

=====
-----< NETWORK OPTION 1 EXAMPLE PARAMETERS >-----
=====
CKTNUM = 0 <--- This is the only circuit
NMBSLV = 1 <--- There is only one slave

Slave system file suffix characters:
Slave --> ABCDEFGHIJKLMNOP
SLVSST = " " <--- Send "OSSLAVE.SYS" to
all slaves

Slave system type table:
Slave --> ABCDEFGHIJKLMNOP
TYPTBL = "1111111111111111" <--- All slaves are SBC-I's

Slave port assignments:
Slave --> A B C D E F G H
SLVPAT = 0B0,0B4,0B8,0BC,0C0,0C4,0C8,0CC
Slave --> I J K L M N O P
SLVPAT + 8 = 0D0,0D4,0D8,0DC,0E0,0E4,0E8,0EC
=====

```

2.2 Network option 2

The 'SM2NT1' network driver (network option 2 in the GEN and PAR files) supports up to 16 SBC-I slaves. This network driver is unique to the Systemaster II and utilizes additional hardware to provide a higher level of performance. Included among the improvements are DMA network data transfers, an optional interrupt driven network protocol, and the ability to handle multiple network transactions simultaneously. This driver requires new SBC-I boot proms and an optional "sky bus" connection cable (only needed if using the interrupt network protocol).

When using the interrupt driven protocol, the Systemaster II parallel ports are used as interrupt controllers to detect and service slave network requests. Each slave has its parallel B port bit #2 (SBC-1 J2 pin #8) connected to one of the Systemaster II parallel port bit lines by a "sky bus" connector cable. In systems with 1 to 8 slaves only the Systemaster II parallel B port is used, allowing the A parallel port to still be used for a parallel printer. More than 8 SBC-I slaves require both Systemaster II parallel ports for interrupt operation.

This network option may be combined with network option 3 to support mixed systems of SBC-I and SBC-II slave boards. In this configuration the slaves will each reside on their own circuit. The parameter examples for a mixed system will be given in section 3.0.

2.2.1 Modules required

The modules required in the Systemaster II operating system for this network option are:

'SM2NT1'	Systemaster II network driver
'SM2DMA'	Systemaster II DMA transfer support
'NT1INT'	ONLY if interrupt network protocol is used and "sky bus" cable is installed.

The SBC-I slaves must use the 'SBLNET' slave network driver and the 'SBLNIT' initialization module.

New SBC-I slave TurboDOS boot proms must be used with this network option.

Additionally, if the interrupt driven network protocol is used, a special "sky bus" connection cable must be used to connect the SBC-I's and the Systemaster II. The hardware interconnections between the SBC-1 slaves' B parallel ports and the Systemaster II's parallel ports follow on the next page.

Systemaster II CIO

Port-B

```

-----
PB0      J2-pin#15
PB1      J2-pin#13
PB2      J2-pin#11
PB3      J2-pin#9
PB4      J2-pin#7
PB5      J2-pin#5
PB6      J2-pin#3
PB7      J2-pin#1

```

SBC-1 Slave #nn
PIO Port-B bit #2 / J2 pin #8

```

-----
Slave A  /
Slave B  2
Slave C  3
Slave D  4
Slave E  5
Slave F  6
Slave G  7
Slave H  8

```

Port-A

```

-----
PA0      J1-pin#15
PA1      J1-pin#13
PA2      J1-pin#11
PA3      J1-pin#9
PA4      J1-pin#7
PA5      J1-pin#5
PA6      J1-pin#3
PA7      J1-pin#1

```

```

Slave I  /
Slave J  2
Slave K  3
Slave L  4
Slave M  5
Slave N  6
Slave O  7
Slave P  8

```

2.2.2 Configuration parameters

The SM2NT1 driver has five patchable parameters as follows:

- CKTNM@ This byte value is the circuit address/number that this network driver controls.
- NMBSL@ This byte value between 1 and 16 (1-10 hex) is the number of slaves on this network circuit and the number of slaves that SM2NT1 is to service (1 per SBC-I).
- SLVPA@ This 16 byte table is the slave port address table. It contains the base address for each slave on the network circuit.
- SLVSU@ This 16 byte table is the slave file suffix character table. It contains one character for each slave, this character is appended to the filename "OSSLAVE" to identify the slave's download file ("OSSLAVEx.SYS").
- SLVFL@ This byte value controls whether diagnostic slave boot messages are output to serial port A on the slave. If set to 00 in the PAR file, then no boot messages are displayed. Setting this parameter to 0F will display messages at 19200 baud and 0E will display messages at 9600 baud. All other values are indeterminate.

```

=====
-----< NETWORK OPTION 2 EXAMPLE PARAMETERS >-----
=====
      (note that this example assumes 'SM2NT1' is the first
        network driver in the GEN file)

CKTNUA =          0          <--- This is the first circuit
NMBSLA =          1          <--- There is only 1 SBC-I

      Slave system file suffix characters:
      Slave --> ABCDEFGHIJKLMNOP
SLVSSA =          "1111111111111111" <--- Send "OSSLAVE1.SYS" to
                                          all slaves

      Slave port assignments:
      Slave --> A   B   C   D   E   F   G   H
SLVPAA =          0B0,0B4,0B8,0BC,0C0,0C4,0C8,0CC
      Slave --> I   J   K   L   M   N   O   P
SLVPAA + 8 =      0D0,0D4,0D8,0DC,0E0,0E4,0E8,0EC

      Slave boot diagnostic message control:

SLVFLA =          0E <--- Display boot messages at 9600 baud
=====

```


2.3 Network option 3

The 'SM2NT2' network driver (network option 3 in the GEN and PAR files) supports up to 16 SBC-II slaves. This network driver is unique to the Systemaster II and, similar to network option 2, also provides a higher level of performance. Included among the improvements are DMA network data transfers and the ability to handle multiple network transactions simultaneously. This driver requires new SBC-II boot proms.

This network option may be combined with network option 2 to support mixed systems of SBC-I and SBC-II slave boards. In this configuration the slaves will each reside on their own circuit. The parameter examples for a mixed system will be given in section 3.0.

2.3.1 Modules required

The modules required in the Systemaster II operating system for this network option are:

'SM2NT2'	Systemaster II network driver
'SM2DMA'	Systemaster II DMA transfer support

The SBC-II slaves must use the 'SB2NET' slave network driver.

New SBC-II slave TurboDOS boot proms must be used with this network option.

2.3.2 Configuration parameters

The SM2NT2 driver has five patchable parameters as follows:

CKTNM@	This byte value is the circuit address/number that this network driver controls.
NMBSL@	This byte value between 1 and 16 (1-10 hex) is the number of slaves on this network circuit and the number of slaves that SM2NT2 is to service (2 per SBC-II).
SLVPA@	This 16 byte table is the slave port address table. It contains the base address for each slave on the network circuit.
SLVSU@	This 16 byte table is the slave file suffix character table. It contains one character for each slave, this character is appended to the filename "OSSLAVE" to identify the slave's download file ("OSSLAVEx.SYS").

SLVFL@ This byte value controls whether diagnostic slave boot messages are output to serial port A on the slave. If set to 00 in the PAR file, then no boot messages are displayed. Setting this parameter to a non-zero value will display messages at whatever baud rate the SBC-II slave hardware has been configured for.

=====
 -----< NETWORK OPTION 3 EXAMPLE PARAMETERS >-----
 =====

(note that this example assumes 'SM2NT2' is the first network driver in the GEN file)

CKTNUA = 0 <--- This is the first circuit
 NMBSLA = 2 <--- There is only 1 SBC-II
 but 2 slaves

Slave system file suffix characters:

Slave --> ABCDEFGHIJKLMNOP
 SLVSSA = "2222222222222222" <--- Send "OSSLAVE2.SYS" to
 all slaves

Slave port assignments:

Slave --> A B C D E F G H
 SLVPAA = 80,84,88,8C,90,94,98,9C
 Slave --> I J K L M N O P
 SLVPAA + 8 = 0A0,0A4,0A8,0AC,0B0,0B4,0B8,0BC

Slave boot diagnostic message control:

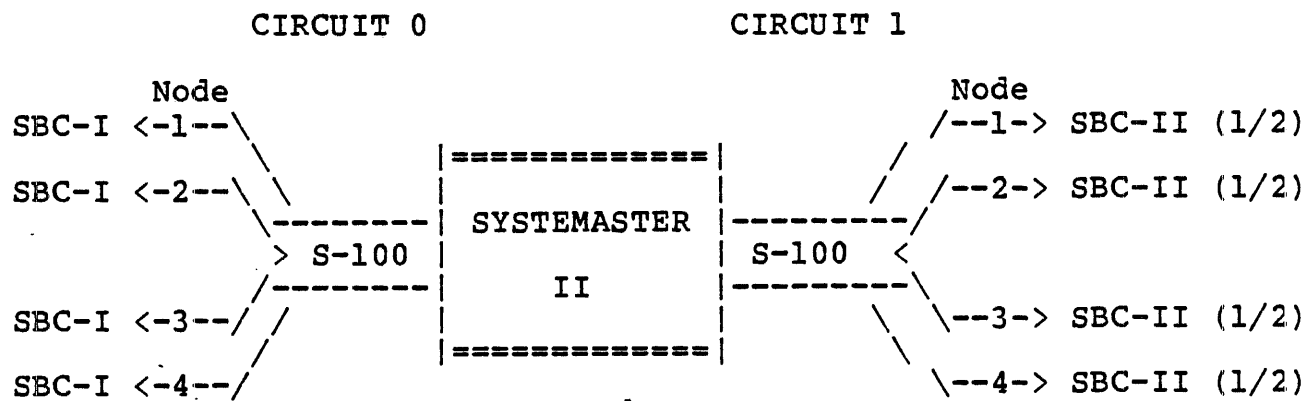
SLVFLA = OFF <--- Display boot messages

3.0 Mixed slave systems

In order to support mixed systems of SBC-I and SBC-II slaves with the new Systemmaster II network drivers it is necessary to configure the TurboDOS operating system with multiple network circuits. Each type of slave (SBC-I, SBC-II, etc.) will reside on it's own network circuit and have it's own circuit driver.

The system modules for a mixed system are the same as those detailed in the network option descriptions.

To illustrate a mixed slave system, we will use an example. Our example will include 2 SBC-II slave boards (4 slaves) and 4 SBC-I slave boards for a total of 8 system users. See the following illustration.



EXAMPLE MIXED SLAVE SYSTEM ILLUSTRATED

First in our example is an excerpt from the GEN file for the Systemmaster II:

```

;=====
;-----< NETWORK OPTION 2 >-----
;=====
;
SM2NT1      ;Fast SBC-I network driver
NT1INT     ;Fast SBC-I network interrupt support module
;
;=====
;-----< NETWORK OPTION 3 >-----
;=====
;
SM2NT2      ;Fast SBC-II network driver
;
;=====
;
SM2DMA     ;Systemmaster II DMA block transfer support routine
;
;=====
  
```

Before we go on to the PAR file for the Systemaster II, we would like to make a couple of observations from the GEN file.

The SBC-I network ('SM2NT1') will be assigned to 'CKTDRA' by TurboDOS and the SBC-II network ('SM2NT2') will be assigned to 'CKTDRB'. Likewise, all configuration parameters for 'SM2NT1' and 'SM2NT2' will take the form of 'xxxxxA' for 'SM2NT1' and 'xxxxxB' for 'SM2NT2'. This would change if the module order was different in the GEN file (ie: the modules were reversed).

The SBC-I network will be using the interrupt driven protocol and "sky bus". Note that we have also included the 'SM2DMA' DMA support module, this module MUST be included for either of these network drivers to work.

Now we present an excerpt from the PAR file for the Systemaster II:

```

;=====
; NETWORK PARAMETERS
;
NMBMBS =      10      ;Number of network mssg. buffers
NMBRPS =      08      ;Number of network reply buffers
NMB SVC =      08      ;Number of network server processes
;
NMBCKT =      02      ;Number of network circuits
CKTAST =      (0000),CKTDRA,(0100),CKTDRB
;
;=====
;-----< NETWORK OPTION 2 PARAMETERS >-----
;=====
;
CKTNUA =      0      ;network circuit number
NMBSLA =      4      ;number of network slaves
;
;      Slave system file suffix characters:
;      Slave --> ABCDEFGHIJKLMNOP
SLVSSA =      "1111111111111111"
;
;      Slave port assignments:
;      Slave --> A   B   C   D   E   F   G   H
SLVPAA =      0B0,0B4,0B8,0BC,0C0,0C4,0C8,0CC
;      Slave --> I   J   K   L   M   N   O   P
SLVPAA + 8 =   0D0,0D4,0D8,0DC,0E0,0E4,0E8,0EC
;
;      Slave boot diagnostic message control:
;
;-SLVFLA =      0F      ;display boot messages at 19200 baud
SLVFLA   =      0E      ;display boot messages at 9600 baud
;-SLVFLA =      00      ;do not display boot messages
;

```

example parameters continued on next page

```

;=====
;-----< NETWORK OPTION 3 >-----
;=====
;
CKTNUB =      01      ;network circuit number
NMBSLB =      4      ;number of network slaves
;
;      Slave system file suffix characters:
;      Slave --> ABCDEFGHIJKLMNOP
SLVSSB =      "2222222222222222"
;
;      Slave port assignments:
;      Slave --> A  B  C  D  E  F  G  H
SLVPAB =      80,84,88,8C,90,94,98,9C
;      Slave --> I  J  K  L  M  N  O  P
SLVPAB + 8 =   0A0,0A4,0A8,0AC,0B0,0B4,0B8,0BC
;
;      Slave boot diagnostic message control:
;
SLVFLB =      Off     ;display boot messages
;-SLVFLB =    00     ;do not display boot messages
;
;=====

```

Now a description of each of these parameters:

NMBMBS This parameter sets the number of network message buffers pre-allocated by TurboDOS. We have set it to twice the number of slaves as per TIG (the TurboDOS IMPLEMENTOR'S GUIDE).

NMBRPS This parameter sets the number of network reply packets pre-allocated by TurboDOS. We have set it equal to the number of slaves as per TIG.

NMBSVC This parameter sets the number of network server processes started by TurboDOS. We have set it equal to the number of slaves (8) as per TIG.

NMBCKT This is the number of network circuits. We set it to 2 because we have one circuit for SBC-I slaves and another circuit for SBC-II slaves.

CKTAST This table assigns the network addresses and the network drivers for each network circuit. We have two entries, one for each circuit. The first entry, '(0000),CKTDRA', is for the SBC-I circuit and gives the Systemaster II a network address of node 0 and circuit 0, to the SBC-I slaves. The second entry, '(0100),CKTDRB', is for the SBC-II circuit and gives the Systemaster II a network address of node 0 and circuit 1, to the SBC-II slaves. Note that 'CKTDRA' and 'CKTDRB' are assigned to the network drivers as shown in our GEN file discussion.

CKTNUA 'SM2NT1' will be circuit 0.
 CKTNUB 'SM2NT2' will be circuit 1.
 NOTE: These circuit numbers MUST match the high nibble of the 'CKTAST' entry for each network driver.

NMBSLA Number of slaves for 'SM2NT1' = 4 (1 per SBC-I).
 NMBSLB Number of slaves for 'SM2NT2' = 4 (2 per SBC-II).
 Note that 'NMBSLB' has been set to 4 even though we only have 2 SBC-II boards since each SBC-II board has two slaves.

SLVSSA Send 'OSSLAWE1.SYS' to all 'SM2NT1' slaves (SBC-I).
 SLVSSB Send 'OSSLAWE2.SYS' to all 'SM2NT2' slaves (SBC-II).

SLVPAA I/O port assignments for 'SM2NT1' slaves (1 per SBC-1).
 SLVPAB I/O port assignments for 'SM2NT2' slaves (2 per SBC-2).

SLVFLA We will send boot messages on 'SM2NT1' slaves.
 SLVFLB We will send boot messages on 'SM2NT2' slaves.

We have not included the disk and printer assignment tables for the Systemaster II since these tables are unchanged from a normal TurboDOS configuration. We will not include the GEN and PAR excerpts for the SBC-I either for the same reason, they do not change.

The GEN file for the SBC-II slave systems includes the 'SB2NET' slave circuit driver. Otherwise the SBC-II GEN file is the same. Now we present the PAR file excerpts from the SBC-II slave systems.

```

;=====
;-----< SBC-II NETWORK OPTION 3 >-----
;=====
;
NMBCKT      =      1          ;Number of network circuits
CKTAST      =      (0100),CKTDRA ;Circuit assignment table
DEFDID      =      (0100)     ;Default destination address
FWDTBL      =      (0001)     ;Message forwarding table

DSKAST      =      80,(0100),81,(0100),82,(0100),83,(0100)
DSKAST + 0C =      84,(0100),85,(0100),86,(0100),87,(0100)
DSKAST + 18 =      88,(0100),89,(0100),8A,(0100),8B,(0100)
DSKAST + 24 =      8C,(0100),8D,(0100),8E,(0100),8F,(0100)

PTRAST      =      80,(0100),81,(0100),82,(0100),83,(0100)
PTRAST + 0C =      84,(0100),85,(0100),86,(0100),87,(0100)
PTRAST + 18 =      88,(0100),89,(0100),8A,(0100),8B,(0100)
PTRAST + 24 =      8C,(0100),8D,(0100),8E,(0100),8F,(0100)

QUEAST      =      80,(0100),81,(0100),82,(0100),83,(0100)
QUEAST + 0C =      84,(0100),85,(0100),86,(0100),87,(0100)
QUEAST + 18 =      88,(0100),89,(0100),8A,(0100),8B,(0100)
QUEAST + 24 =      8C,(0100),8D,(0100),8E,(0100),8F,(0100)
    
```

;=====

Now a description of each of these parameters:

- NMBCKT Each slave is only connected to one network circuit at the present time.
- CKTAST This table assigns the network address and the network driver for our network circuit. We have one entry, '(0100),CKTDRA', and it gives the slave a network address of node x and circuit 01 (the node address is set up during slave initialization).
- DEFDID The 'DEFDID' (DEFault Destination IDentification) corresponds to the network address to send any requests not specifically addressed to a network node. In our example we have set this to the network address of the Systemaster II in relation to this slave (circuit number 1, node 0).
- FWDTBL The network forwarding table provides a link (read that "stepping stone") to network circuits that are not connected to this processor. In our example, the slave does not have direct access to network circuit number 0. Through the forwarding table the slave can get indirect access to circuit 0 by sending messages to circuit 1 and letting another network node (ie: the Systemaster II) forward the message. Our forwarding table entry, '0001', makes all references to circuit 0, the first byte, be forwarded through circuit 1, the second byte. Technically all other network address patches are not required if the forwarding table is patched, however for system efficiency, we suggest configuring them as shown here.
- DSKAST
PTRAST
QUEAST On the slave, these assignment tables all default to remote devices on network address 0000. For our example we need to change the default network address for all devices to network address 0100 since we are attached to circuit number 1.

4.0 Maximum system performance

The optimum performance will be obtained by:

1. Using the 'SM2NT1' network driver along with the 'NT1INT' interrupt support module for SBC-I slaves.
2. Using the 'SM2NT2' network driver for SBC-II slaves.
3. Using a number of network server processes equal to the number of slaves.
4. Use additional network circuits on the Systemaster II as in the following example:

```

;=====
; NETWORK PARAMETERS
;
NMBCKT =      04      ;Number of network circuits
CKTAST =      (0000),CKTDRA,(0000),CKTDRA,
              (0000),CKTDRA,(0000),CKTDRA
;
;=====

```

This will allow multiple slave transactions to be processed simultaneously instead of sequentially as shown by the two following illustrations.

```

|--Slave transaction 1---->|--Slave transaction 5---->
  |--Slave transaction 2---->|--Slave transaction 6---->
    |--Slave transaction 3---->
      |--Slave transaction 4---->

```

OVERLAPPED SLAVE TRANSACTION PROCESSING

```

|--Slave transaction 1---->|--Slave transaction 2---->

```

NON-OVERLAPPED SLAVE TRANSACTION PROCESSING

How to Use HD/CTC Options With Systemaster II

Systemaster II has a new hard disk driver that will allow the user to boot directly from a hard disk drive that is under the control of the Teletek HD/CTC or HDC. This document will explain the step by step procedure to achieve this goal.

The name of the new hard disk driver is "SM2HD". It will work only with Systemaster II. Note that, due to the changes in hard disk skewing, SM2HD is not compatible with the old HD/CTC driver. That is, if you format the hard disk with SM2HD, you will not be able to access to it if you switch back to the Systemaster and the HD/CTC driver. Another difference is that, with SM2HD, partitioning of the hard disk on a head basis is no longer available. SM2 has other advantages, however.

First, with the new driver access to the hard disk is via DMA thru THE SM2DMA module that must be included in the system generation. Second, if the hard disk you are using has a binary number of R/W heads (2, 4, 8 or 16), then you can take advantage of the fast divide routine. Third, you can implement interrupts on the hard disk controller for additional access speed.

The following paragraphs explain how to divide the hard disk into logical drives. Since most of the recent generation of hard disk drives employ the buffered track seek method, their firmware does not allow you to pull the R/W heads outside the data tracks upon power down. However, by dividing the disk drive into logical drives and setting one logical drive as a "power down" driver, you can get around this problem and assure yourself a trouble free hard disk drive operation. (more on this later)

In our typical system, we have Systemaster II, HD/CTC with 27 meg Rodime 240 5.25" hard disk drive, CDC 96 meg Phoenix hard disk drive with removable cartridge with a Konan SMD-200 controller, and three Qume DataTrack 8" floppy disk drives. We intend to use the Rodime drive as our system drive (logical drive) "A:". We would like to boot from hard disk drive "A:" without the aid of a floppy. The Phoenix drive is to be divided into 6 logical drives, "B:" thru "G:". The floppies are assigned to the logical drives "H:" thru "J:".

We will set up two different "SM2LOADx" files. If the suffix x is "A" it denotes that the system boots from logical drive "A:". And if the suffix x is "H" the system boots from logical drive "H:"

In setting up the "SM2LOADA.GEN" file we include :

```
SM2HD          ;System Master II driver for HD/CTC
               ;DSKDRA for TurboDOS disk assignment table
FDIVIDE        ;Fast divide routine, Rodime 204 has 8 heads
SM2DMA         ;Needed by SM2HD for DMA
$KONPNX        ;Konan/Phoenix driver, DSKDRB
WDFLPY2        ;New driver for floppy
SM1DST         ;Systemaster I floppy compatibility module
```

The Disk Assignment Table in "SM2LOADA.PAR" file is:

```
;      Disk assignments:
;
;      --A--      --B--      --C--      --D--
DSKAST      =      00,DSKDRA,05,DSKDRB,04,DSKDRB,03,DSKDRB
;
;      --E--      --F--      --G--      --H--
DSKAST+0C   =      02,DSKDRB,01,DSKDRB,00,DSKDRB,00,DSKDRB
;
;      --I--      --J--      --K--      --L--
DSKAST+18   =      01,DSKDRB,02,DSKDRB,0ff,(000),0ff,(000)
;
;      --M--      --N--      --O--      --P--
DSKAST+24   =      0ff,(000),0ff,(000),0ff,(000),01,DSKDRA
```

Note that, DSKDRA, the first disk driver in "SM2LOADA.GEN" file (SM2HD) has two logical drives. The logical drive "A:" and the power down drive "P:". The logical drives "B:" thru "G:" are on the second driver, DSKDRB or "\$KONPNX". And the floppies, drives "H:" thru "J:" are on the third driver, DSKDRB of "WDFLPY2".

The section relating to the floppy drives is as follows:

```
; FLOPPY DRIVER PARAMETERS
; 'WDFLPY2'
;
; This table defines the floppy drives to the driver.
; The high nibble defines the drive size (0 = 8 inch and
; 1 = 5.25 inch) and the low nibble defines the step rate.
;
; Drive step rates are:
;      8 inch drive          5.25 inch drive
;      -----
;      00 --> 3 ms.          10 --> 6 ms.
;      01 --> 6 ms.          11 --> 12 ms.
;      02 --> 10 ms.         12 --> 20 ms.
;      03 --> 15 ms.         13 --> 30 ms.
;      -----
;
;      0 1 2 3      ;floppy drive number
DRVDTBL =      00,00,00,00      ;all drives 8" with 3 ms. step
;
; 'MTRDLY' sets the delay time between starting the floppy drive
; motors and any disk access. This parameter is a number of
; system tics (1/60 of a second). The default is a 2 second
; delay.
;
;
```

```

MTRDLY = (078) ;2 second motor start delay
; ;2 sec * 60 ticks/sec = 120 ticks
; ;120 decimal = 78 hex
; ;Include it in paranthesis as it is a
; ;Define Word as opposed to Define Byte.

```

The section of the "SM2LOADA.PAR" relating to "SM2HD" and Rodime 204 hard Disk Drive is:

```

; HARD DISK DRIVER PARAMETERS
; 'SM2HD'
; (see also: the HD/CTC USER'S GUIDE)
;
; 'HDPOR' is the base input/output port address for the HD/CTC
;
;-HDPOR = 30 ;standard HD/CTC port address
;-HDPOR = 80 ;optional port addresses
;-HDPOR = 0B0
HDPOR = 0F0 ;Choose 0F0 as 30 thru 37
; ;are taken by $KONPNX
;
; 'HDINT' is the vectored interrupt assigned to the HD/CTC
;
; NOTE: The standard HD/CTC does not support vectored
; interrupts. Unless you have modified your HD/CTC
; for vectored interrupts, this patch MUST be 0.
;
;-HDINT = 0 ;use no interrupts (standard HD/CTC)
HDINT = 3 ;HD/CTC interrupt on S-100 pin 4
;-HDINT = 4 ; interrupt on S-100 pin 5
;-HDINT = 5 ; interrupt on S-100 pin 6
;-HDINT = 6 ; interrupt on S-100 pin 7
;-HDINT = 7 ; interrupt on S-100 pin 8
;
; 'HDSHFT' is a shift factor for use with the optional 'SM2HD'
; divide support routine, 'FDIVIDE'. Do not include
; this patch if 'FDIVIDE' is not included.
;
;---HDSHFT = 1 ;hard disk with 2 heads
;---HDSHFT = 2 ; 4 heads
HDSHFT = 3 ; 8 heads
; ;Rodime 204 has 8 heads
;---HDSHFT = 4 ; 16 heads
;

```

```

;      Physical disk parameters
;      for 27 meg Rodime 204 drive
;
HDOPTN  =      08      ;Options, write verification
HDDRVS  =      01      ;1 Hard disk drive
HDCYLS  =      140     ;320 Cylinders
HDHEDS  =      08      ; 8 R/W heads
HDSTEP  =      0       ;Cylinder step rate
HDSTEP - 1 =      0    ;  buffered 10 usec.
HDCST   =      01     ;Cylinder settling time, 1 ms.
HDWRCL  =      140    ;Low write current on cyl. #320
HDWRCL-2 =      (0)   ;Write precomp cylinder, all cylinders
;
;      Logical hard disk parameters
;
;      DRIVE 0 PARAMETERS
;
HDOBLK  =      84      ;Fixed media, 2k allocation block
HDORTK  =      (01)    ; 1 reserved tracks
HDOTK   =      09FF    ; 2559 Tracks
HDOBKS  =      27F8    ;10232 Blocks = ((2559-1)*8)/2)
HDODIR  =      20      ;2048 Directory entries
;
;      POWER DOWN DRIVE PARAMETERS
;
HD1BLK  =      83      ;Fixed media, 1k allocation block
HD1RTK  =      09FF    ;2559 Reserved tracks
HD1TK   =      0A00    ;2560 Tracks
HD1BKS  =      (08)    ;8 Blocks = ((2560-2559)*8)/1
HD1DIR  =      1       ;32 Directory entries
;

```

Note that the logical drive "A:" has one reserved system track and all the tracks of logical drive "A:" act as reserved tracks for the second logical drive on Rodime 204, "P:". In calculating the number of data blocks per logical drive, we calculate the total number of data tracks, multiply it with total number of blocks per track (8/2) or (8/1).

The CDC Phoenix and Konan SMD-200 controller parameters are:

```

;
;      CDC Phoenix/Konan SMC100/200 Controller Parameters
;
PNXDST  =      84      ;Fixed drive with 2k block size
PNXDIR  =      20      ;2048 directory entries
;

```

The above parameters are also included in the "SM2MSTR.GEN" and "SM2MSTR.PAR" files.

Since it is desired to bring the system up from logical drive "A:" we include the following patches in the "SM2LOAD.PAR" file.

```
; The following patch may be used to specify which disk to
; use when loading the system.
; 01 --> use drive A, 02 --> use drive B, etc.
;
LOADFN = 01 ;Get system from default drive
;
; The following patch is used to specify the filename to use
; when loading the system ('SM2MSTR.SYS').
;
LOADFN + 1 = "SM2MSTR ", "SYS"
;
```

Prepare the "SM2LOADH.GEN" file identical to the "SM2LOADA.GEN" file. The only difference between "SM2LOADA.PAR" and "SM2LOADH.PAR" files is that the latter has:

```
;
LOADFN =      08      ;Get system from default drive, H:
;
```

The next operation is to generate the SM2LOAD.COM and SM2MSTR.SYS files thru:

```
GEN SM2LOADA.COM
GEN SM2LOADH.COM
GEN SM2MSTR.SYS;U0FF00 K0F800
```

The next item is to prepare the "BOOTDST.PAR" file. For "direct booting" purposes we will treat the hard disk as if it was a single logical disk drive with a single reserved track. Thus the parameters in the "BOOTDST.PAR" file will look like this:

```
=====
;
;      SYSTEMASTER TURBODOS HD/CTC BOOT PROM
;      BOOT DISK SPECIFICATION TABLE
;
;      "BOOTDST.PAR"
;      1-7-85
;
=====
; ***** NOTE: There is no GEN file for the 'BOOTDST.COM'
;      Gen the 'BOOTDST.COM' as follows:
;
;      xA}GEN BOOTDST.COM<cr>      ;do normal GEN command
;      * BOOTDST<cr>              ;no GEN file, input name
;      * <cr>                      ;no other files so return
;      pass 1                      ; and GEN as usual
;      BOOTDS
;      pass 2
;      BOOTDS
;      processing parameter file.....
;
=====
;
;      HARD DISK PHYSICAL PARAMETERS
;
;      Number of cylinders per drive.
;
HDCYLS =      140      ;320 cylinders
;
;      Number of heads per drive.
;
HDHEDS =      08      ; 8 heads
;
```

```

;-----
;      HARD DISK LOGICAL PARAMETERS
;
;      Block size
;
HDBBLK  =      84      ;2k block size
;
;      Number of reserved tracks (MUST be at least 1)
;
HDBRTK  =      (01)   ;1 reserved track
;
;      Number of tracks on drive
;
HDBTK   =      0A00   ;2560 tracks
;
;      Number of allocation blocks
;
HDBBKS  =      27FC   ;10236 2k Blocks = ((2560-1)*8)/2)
;
;      Number of directory blocks
;
HDBDIR  =      20     ; 2048 directory entries
;
;=====

```

Generate the "BOOTDST.COM" file as described in the text.

We will now form a system diskette that boots from floppy drive "H:". Format a diskette using your generic system. Copy onto it the following files:

- SM2LOADH.COM
 - SM2LOADA.COM
 - SM2MSTR.SYS
- and your slave system files
that "SM2MSTR.SYS" looks for.
Then copy: SM2LOADH.COM as SM2LOAD.COM
onto that floppy.

Also include all other system COM files. Be careful not to write over the files that you have previously copied.

Turn off your system. Attach your hard disks, floppies etc. for final configuration. Insert the newly formed system disk into the first physical floppy drive and cold boot the system. When the system signs on attach yourself to the master processor:

MASTER

Reduce the buffers to minimum allowable limit by:

BUFFERS N2

Select the first bank:

BANK 0

Format your hard disk:

HDFMT

Since we have only one physical drive you have to specify drive "0" for the question asked. It will take approximately 10 to 12 minutes to format the hard disk. Next, you have to clear the directory and hash it thru via:

ERASEDIR A:

command and asking for the hashed directory. Teletek has an excellent program that is called "TVERIFY" that goes beyond the TurboDOS read only "VERIFY" command. You can specify up to 8 patterns to test the disk drive. If you have time, approximately 4 hours for 8 patterns on 20 meg formatted drive, please do so. See the separate TVERIFY documentation, DN: C-1750-A.00.

The very next operation ust be the placement of the "BOOTDST.COM" file onto system tracks:

BOOT BOOTDST.COM A:

Since the limited amount of code in the system "PROM" may have difficulty in locating "SM2LOAD.COM" among 2048 directory entries, you have to place that as one of the first files onto the hard disk drive "A:" by:

COPY SM2LOADA.COM 0A:SM2LOAD.COM

Note that the name change is necessary as you want to boot from the hard disk "A:" You may then copy "SM2MSTR.SYS" and the slave system files. Finally copy all your files onto the drive "A:". Do not forget to copy all of the user level 31 files if you are using password protection. To flush the disk buffers issue:

CHANGE *

Take out all the diskettes from floppies. Do a cold reset. The system will attempt to search the floppies for the "SM2LOAD.COM" file. Since it can not find it, it will look to the hard disk attached to the HD/CTC and if it finds a code in the system tracks, it will execute it. Booting up from hard disk may take up to 30 seconds after the reset button has been pressed because of the search priority assigned to the floppy. You may still use the floppies to bring up another system configuration.

Enjoy the floppy free system!

SYSTEMASTER II TURBODOS FLOPPY DISK DRIVER.

VERSION 2

This new version of the SYSTEMASTER II floppy driver supports optional modules to allow reading and writing different floppy disk formats.

The "SM1DST" module supports the 8 inch floppy disk formats used by the SYSTEMASTER TurboDOS system.

The "PCDST" module supports the 5.25 inch mini-floppy disk formats used by the IBM-PC. This module is for future use with 16-bit TurboDOS systems and will not currently serve any useful purpose since the file system and directory format used by the IBM-PC are totally incompatible with the TurboDOS file system and directory format.

To support non-SYSTEMASTER II disk formats do the following:

1. Replace the original "WDFLPY" driver with the new version included on this diskette.
2. Include the desired format support modules ("SM1DST" and/or "PCDST") in the "SM2MSTR.GEN" file.
3. Gen a new master operating system.

The SYSTEMASTER II will not be able to boot the system from these foreign disk formats but it will be able to read and write them once it is running.

CAUTION: In certain situations, SM2FMT (Systemaster II format program) running under WDFLPY2 and SM1DST may not be able to label the volume of the disk on floppy. The system will prompt the user with a FATAL ERROR message. If this should occur, please use "ERASEDIR" immediately on the drive in question. If ERASEDIR also reports an error, choose the "ABORT" option. At this point go back and re-execute SM2FMT program to format and label the diskette in question.

The Use Of Multi Circuits With Systemaster II

Systemaster II, with its super fast Z80H processor and new software drivers is capable of handling more than a single circuit as described in the TurboDOS manual. This documentation will explain how to implement these features. The standard release version of the Systemaster II files come with 4 different circuit drivers. These are:

- a. Hard Polled SBC-1 and SBC-2 driver,
- b. Interrupt Driven SBC-1 driver,
- c. Fast SBC-2 driver,
- d. SBC-86/87 driver

TurboDOS is capable of handling 255 circuits with up to 255 nodes (processors). The actual network topology is defined by a series of tables in each processor and define the network as "seen" from the viewpoint of each processor. These tables are:

1. NMBCKT
2. CKTAST
3. DSKAST
4. PTRAST
5. QUEAST
6. DEFDID
7. FWDTBL

The detailed description of each table is given in "TurboDOS 1.4 Z80 Implementor's Guide" pages 2-20 thru 2-22 and their default values in pages 2-7 thru 2-19.

In order to clarify these concepts let us pick a Systemaster II with:

- a. 2 serial printers A and B and a parallel printer C,
- b. 2 each hard polled SBC-1's
- c. 2 each interrupt driven SBC-1's
- d. SBC-2 board with two slaves thru fast driver.

First you should include the proper drivers for the slaves within "SM2MSTR.GEN" file. Towards the end of the file include:

```
SM2MX2      ;Standard combination driver    ..CKTDRA
@INT0       ;No boot message @INT9 displays 9600 baud msg.
SM2NT1      ;Fast SBC-1 network driver       ..CKTDRB
NT1INT      ;Interrupt support module
SM2NT2      ;Fast SBC-2 network driver       ..CKTDRC
SM2DMA      ;Needed by Interrupt Drivers
```

You do not need to modify PTRAST, QUEAST of the master if you are not going to use global printers on the slaves' local ports. Similarly the DSKAST table of the master does not need to be modified. However we need to modify the following labels:

NMBCKT = 03 ;Three network circuit drivers are being used

CKTAST = (0000),CKTDRA,(0200),CKTDRB,(0300),CKTDRC

Hard polled SBC-1's are assigned to node point 0 and they are reperedented by CKTDRA, as SM2MX2 is the first driver on the list. The interrupt driven SBC-1 driver, CKTDRB (SM2NT1 plus NT1INT), is assigned to node point 2. And the fast SBC-2 driver, CKTDRC (SM2NT2), is assigned to node point 3.

SLVFN = 'SM2SLAV ','SYS' ;Slave system file name

The labels of the the first driver, CKTDRA, are as follows:

CKTNUM = 0 ;Network circuit number
NBMSLV = 2 ;Number of network slaves on the circuit
SLVSST = 'BBBBBBBBBBBBBBBB' ;Slave suffix table
SLVPAT = 0B0,0B4,0B8,0BC,0C0,0C4,0C8,0CC,
0D0,0D4,0D8,0DC,0E0,0E4,0E8,0EC
TYPTBL = '1111111111111111' ;All SBC-1's

Similarly the second driver, CKTDRB, labels are:

CKTNUA = 2 ;Network circuit number
NMBSLA = 2 ;Number of slaves on this circuit
SLVSSA = 'IIIIIIIIIIIIIIIIII' ;Slave suffix table
SLVPAA = 40,44,48,4C,50,54,58,5C,60,64,68,6C,70,74,78,7C
SLAFLA = 0E ;Display boot message at 9600 baud, set at
;0F for 19.2k baud or 00 for no message.

The last circuit for SBC-2's, CKTDRC, will have the following labels:

CKTNUB = 3 ;Network circuit number
NMBSLB = 2 ;Number of slaves on this circuit
SLVSSB = '2222222222222222' ;Slave suffix table
SLVPAB = 80,84,88,8C,90,94,98,9C,0A0,0A4,0A8,0AC,0B0,0B4,0B8,0BC
SLAFLB = 0E ;Display boot message at 9600 baud, set at
;0F for 19.2k baud or 00 for no message.

Other parameters to be considered are:

NMBSVC = 06 ;Number of services, choose the same value
;as number of slaves
NMBMBS = 0C ;Number of message buffers
MAXMBS = 0C ;Put a lid on message buffers
NMBRPS = 06 ;Number or reply packets
MAXRPS = 06 ;Put a lid on reply packets

NMBUFS = 04 ;Number of disk buffers, increase it with
;BUFFER command

Next GEN the system file for Systemaster II. You may find that the above parameters may not leave enough TPA within the BANK 0 of the master to format DS/DD 8" diskette. The minimum TPA required to format 8" DS/DD diskette is around 17.5k. First try to reduce number and maximum number of message buffers and reply packets as well as number of disk buffers (minimum is 2). If still no luck, you may try to GEN another system with a single circuit driver that will secure you sufficient TPA and use that to format floppies.

Next, prepare the "SM2SLAVB" GEN and PAR files. Use "SM2LAV1" GEN and PAR files as a model. If you are using 128k slaves do not forget to include the "BNKMGR", "BNKREQ" and "SB1BNK" modules. Since CKTDRA will be using the hard polled driver, include the NETSX1 and HNTSBI modules; and comment out the SB1NET and SB1NT1 modules. If you are going to use a local spooling serial printer, include CTSLIST and DSPOOL. Within the PAR file you do not need to change the default values of the DSKAST since you will be using the circuit number 0. If the first three printers are on the master and a spooling local serial printer is assigned to the printer D, the PTRAST and QUEAST will be entered as follows:

```
PTRAST      =      80,(0000), 81,(0000), 82,(0000),  1,LSTDRA,
                Off,(0000),Off,(0000),Off,(0000),Off,(0000),
                Off,(0000),Off,(0000),Off,(0000),Off,(0000),
                Off,(0000),Off,(0000),Off,(0000),Off,(0000)

QUEAST      =      80,(0000), 81,(0000), 82,(0000),  0,(0000),
                Off,(0000),Off,(0000),Off,(0000),Off,(0000),
                Off,(0000),Off,(0000),Off,(0000),Off,(0000),
                Off,(0000),Off,(0000),Off,(0000),Off,(0000)
```

You do not need to change any other default value due to the fact that CKTDRA is assigned to the circuit number 0. Once these changes are made GEN the SYS file for the hard polled slaves.

Next prepare the "SM2SLAVI" GEN and PAR files, build a "Sky Bus" cable, (see Section 2 of Systemaster II TurboDOS Network Documentation, chapter 3.0 "Mixed Slave Systems") and secure "Interrupt PROMs" for the SBC-1 from Teletek. The particulars of this task are discussed in the article titled "Interrupt Drive SBC-1's With Systemaster II". Please read it carefully! Don't forget to change the PROMs on these slaves and alter the addresses of the slaves. You have to build a "Sky Bus" also.

The last task is to prepare "SM2SLAV2" GEN and PAR files. You'll also need to secure new PROMs for SBC-IIs from Teletek to be used with this driver. With the distribution diskette, you will find these drivers. In the "SM2SLAV2.GEN" file comment out NETSX2 module and include "SB2NET" and "RTCNU" modules. If spooling local printer D is desired include "CTSLIST" and "DSPOOL" modules also. Since the circuit assignment number has been changed from 0 to 3 we have to modify all the parameters that relate to "Network" in the "SM2SLAV2.PAR" file. Thus the "SM2SLAV2.PAR" file should include:

```

DSKAST      =      80,(0300),81,(0300),82,(0300),83,(0300),
                  84,(0300),85,(0300),86,(0300),87,(0300),
                  88,(0300),89,(0300),8A,(0300),8B,(0300),
                  8C,(0300),8D,(0300),8E,(0300),8F,(0300)

PTRAST      =      80,(0300), 82,(0300), 83,(0300),  1,LSTDRA,
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300),
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300),
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300)

QUEAST      =      80,(0300), 82,(0300), 83,(0300),  0,(0000),
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300),
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300),
                  0ff,(0300),0ff,(0300),0ff,(0300),0ff,(0300)

CKTAST      =      (0000),CKTDRA ;There is only one circuit on SBC-2
                                side
DEFDID      =      (0300)        ;Default destination master
FWDTBL      =      (0ffff)      ;No forwarding is required

```

When these changes are done generate the new "SM2SLAV2.SYS" file and copy it onto your boot disk with the rest of the SYSTEM files. Turn off the power. Change the PROMs on SBC-1's and SBC-2's. Attach the "Sky Bus" cable. Turn on the power and press reset. Enjoy the multi-circuit "System Master 2". Run some bench marks to appreciate its power.

Interrupt Driven SBC-Is

This documentation will explain how to get the extra performance out of SBC-1s networked with Systemaster II. With a minimum amount of expense you can increase the total system performance by at least 50%. If you are planning to use more than one type of slave with Systemaster II you should also refer to the article titled "Multi Circuits With Systemaster II."

The difference between a "hard polled" SBC-1 and an "interrupt driven" SBC-1 can be easily explained with a single waiter in a restaurant. The "hard polled" method is analogous to a waiter checking each table whether the service is desired or not. The "interrupt driven" method on the other hand is analogous to waiter providing the service when it is requested. It is needless to say that as the number of tables (services) increase the first method will suffer unnecessary delays whatever the speed of the waiter.

You may remedy the situation by increasing the amount of load a waiter can carry at one time (by increasing disk buffers, network services, message buffers etc.), but you will still feel the drop in the service. In order to implement the second method we have to come up with a way to attract the attention of the waiter (master server). The raising of the hand by the customer (slave processor) is done thru the bit number 2 of the parallel port B. Each customer (interrupt driven slave processor) is assigned to one of the parallel bits of the master server starting with the 8th bit of the parallel port B and ending with the 1st bit of parallel port A. It is obvious that if we use all bits available in two parallel ports, we can handle upto 16 interrupt driven slaves. Thus we need to make a cable that will connect the parallel port, 2nd bit of each interrupt driven slave to the individual bits of the parallel ports of the System Master II. This cable will connect B8 of System Master II to B2 of Slave 0, B7 of SM2 to B2 of Slave 1 etc.

A "Sky Bus" cable is required for this implementation as are interrupt SBC-1 boot proms. Documentation on the cable construction is given in the documentaiton Systemaster II TurboDOS Network Documentation.

Once these two items above are secured, the following changes are to be made in the .GEN and .PAR files of Systemaster II and SBC-1's. Assuming that we will be using only interrupt driven SBC-1's (please refer to the article on multiple circuits) your Systemaster II .GEN file should include:

```
SM2DMA      ;SM2 DMA block transfer support routine
SM2NT1      ;SBC-1 interrupt driver
NT1INT      ;Support module
```

You should cancel SM2MX2, @INT0, @INT9, INT02, and INT92 if you are using a single circuit. And in System Master II PAR file file you should set the following labels as:

```
NMBCKT = 01 ;Number of actual circuits
CKTAST = (0200),CKTDRA ;States that interrupt driver (SM2NT1)
is assigned to circuit 0200
SLVFN = 'SM2SLAV ','SYS';Slave system file
```

Under the network option for the interrupt driven slaves set the following labels as:

```
CKTNUA = 2 ;Network circuit number ( 2 for 0200)
NMBSLA = 1 ;Number of actual int. driven slaves
SLVSSA = "IIIIIIIIIIIIIIIIII" ;Suffix x of the SM2SLVx.SYS file
SLVPAA = 40,44,48,4C,50,54,58,5C,60,64,68,6C,70,74,78,7C
;Leave 0B0 thru 0EF to polled slaves
;and don't forget to address the slave
;at 40 hex.
SLVFLA = 0E ;Proper baud rate constant for boot
message 0F=19.2k, 0E=9600, 00=none
```

Also you may need to adjust NMBMBS, MAXMBS, NMBRPS, MAXRPS, and NMBSVC labels. Refer to the TurboDOS Implementor's Guide for their descriptions. When ready GEN a new Systemmaster II SYSTEM file.

Next you have to create "SM2SLAVI" GEN and PAR files using "SM2SLAV1" or "SM2SLAVB" as a model. You should cancel NETSX1 and HNITSB modules and use instead SB1NET and SB1NIT modules. The "SM2SLAVI.PAR" file needs to be slightly modified. Since we have changed the circuit number from default 000 to 200, DSKAST table needs to be altered from its default values:

```
DSKAST = 80,(0200),81,(0200),82,(0200),83,(0200),
84,(0200),85,(0200),86,(0200),87,(0200),
88,(0200),89,(0200),8A,(0200),8B,(0200),
8C,(0200),8D,(0200),8E,(0200),8F,(0200)
```

You need to alter PTRAST and QUEAST to reflect the circuit number change. Assuming that the slave GEN file includes CTSLIST and DSPPOOL modules to give it local serial printer D with spooling capability, the two tables will look like as given below:

```
PTRAST = 80,(0200), 82,(0200), 83,(0200), 1,LSTDRA,
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200),
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200),
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200)
```

```
QUEAST = 80,(0200), 82,(0200), 83,(0200), 0,(0000),
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200),
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200),
0ff,(0200),0ff,(0200),0ff,(0200),0ff,(0200)
```


You also need to alter three other labels as follows:

```
CKTAST      =      (0000),CKTDRA      ;As far as slave is concerned
                                         it has a single circuit
                                         numbered 0 whose name is
                                         SB1NET.
DEFDID      =      (0200)             ;This should be set to the
                                         network address of the
                                         master (Z80 Imp. Gui. 2-10).
FWDTBL      =      (0ffff)           ;No forwarding (Z80 Imp. Gui.
                                         2-12)
```

When done, place the files on your boot disk. Turn off the power. Attach the "Sky Bus" and change "PROM" on SBC-1. Make sure the slave is addressed at 40 hex. Turn on the power and press reset to cold-boot. Try out your favorite program. You will be wondering why you have not undertaken this simple project earlier. This is probably the biggest performance improvement per dollar spent on your Teletex system.

MODIFICATIONS REQUIRED ON HDC AND HD/CTC TO RUN IN INTERRUPT MODE
WITH SYSTEMASTER II

- (1) On solder side of board, cut trace to pin 73 and pin 96 of the S-100 connector.
- (2) On solder side of board cut trace to pin 12 of U-5.
- (3) On component side of board, locate U-20 (the 10 MHz oscillator). Below the lower right corner of the oscillator is a test point post. Just to the right of this post a trace runs to a feed through hole. Cut the trace going to the feed through hole.
- (4) On solder side of board, jumper pin 5 of U-4 to pin 10 of U-4.
- (5) On solder side of board, jumper pin 15 of U-5 to pin 8 of U-5.
- (6) On solder side of board, jumper pin 12 of U-5 to pin 13 of U-6.
- (7) On component side of board, jumper pin 4 of S-100 connector to the feed through hole described below:

On component side of board, locate U-5. Existing below U-5 are (5) traces. On the left is a wide trace. Moving to the right, there are (4) thin traces. The 1st thin trace runs to a feed through hole. Jumper pin 4 of the S-100 connector to this feed through hole.

- (8) Enable Jumper Option I. This option is located directly to the right of U4 on component side of board.

SM2 FLOPPY DRIVE CONFIGURATIONS

CONTENTS

Standard Height 8" Drives

Mitsubishi M2894-63B
Qume 842
Shugart SA800/801
Shugart SA850/851
NEC FD1160
SIEMENS FDD 200-8

Half Height 8" Drives

Mitsubishi M2896-63
QumeTrack 242
Shugart SA810/860
NEC FD1165
Tandon TM848

Mitsubishi M2894-63B
 8" STANDARD HEIGHT FDD

Designator	Description	Open	Short
PJ1	None		X
PJ2	READY (MODIFIED)	X	
PJ3	DOOR LOCK LATCH		X
PJ4	HEAD LOAD	X	
PJ5	ALTERNATE HEAD LOAD	X	
PJ6	HEAD LOAD LATCH		X
PJ7	STEPPER POWER		X
PJ8	SIDE SELECT		X
1B,2B, 3B,4B	SIDE SELECT USING DRIVE SELECT	X	
RR	RADIAL READY		X
RI	RADIAL INDEX		X
R	READY OUTPUT		X
I	INDEX OUTPUT		X
2S	TWO-SIDED OUTPUT		X
DC	DISK CHANGE OPTION	X	
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
A	LOAD HEADS W/O DRIVE SELECT	X	
E	NO FUNCTION	X	
Z	IN USE FROM DRIVE SELECT	X	
Y	IN USE FROM HEAD LOAD		X
S2	STANDARD SIDE SELECT		X
S3	OPTIONAL SIDE SELECT	X	
STM1	EXT STEPPER POWER	X	
STM2	STEPPER POWER ON		X
SF	INT SWITCH FILTER		X
NSF	W/O SWITCH FILTER	X	
HUD			X
HUN		X	
DLH			X
DLI		X	
F			X
DLM1			X
DLM2		X	
C			X
FG/SG ON			X
FG/SG OFF		X	

QUME 842
8" STANDARD HEIGHT FDD

Designator	Description	Open	Short
A	RADIAL HEAD LOAD		X
B	RADIAL HEAD LOAD	X	
X	RADIAL HEAD LOAD		X
Z	IN USE FROM DRIVE SELECT	X	
HL	STEPPER PWR FROM HEAD LOAD	X	
R	READY OUTPUT		X
I	INDEX OUTPUT		X
C	ALT INPUT - HEAD LOAD		X
D	ALT IN USE INPUT	X	
DC	DISK CHANGE OPTION	X	
2S	TWO-SIDED OUTPUT		X
DS	STEPPER PWR FROM DRIVE SEL		X
Y	IN USE FROM HEAD LOAD		X
DL	DOOR LOCK LATCH OPTION		X
RR	RADIAL READY		X
RI	RADIAL INDEX		X
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
D1,D2, D4,DDS	DRIVE ADDRESS SELECT	X	
B1,B2, B3,B4	SIDE SELECT USING DRIVE SELECT	X	
S1	SIDE SELECT USING DIR SEL	X	
S2	STANDARD SIDE SELECT		X
S3	SIDE SELECT USING DRIVE SEL	X	
T40	TEST TRACK 40	X	
HA	TEST ACTUATE HEAD LOAD	X	

SHUGART 800/801
8" STANDARD HEIGHT FDD

Designator	Description	Open	Short
T3,T4, T5,T6	TERMINATIONS		X
T1	DRIVE SELECT TERMIATOR		X
T2	RADIAL HEAD LOAD TERMINATOR		X
RR	RADIAL READY		X
R1	RADIAL INDEX		X
R	READY OUTPUT		X
I	INDEX OUTPUT		X
S	SECTOR OUTPUT		X
HL	STEPPER PWR FROM HEAD LOAD	X	
DS	STEPPER PWR FROM DRIVE SEL		X
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
D	ALT IN USE INPUT	X	
D1,D2, D4,DDS	DRIVE ADDRESS SELECT	X	
A	RADIAL HEAD LOAD		X
B	RADIAL HEAD LOAD	X	
X	RADIAL HEAD LOAD		X
C	ALT INPUT - HEAD LOAD		X
Z	IN USE FROM DRIVE SELECT	X	
Y	IN USE FROM HEAD LOAD		X
DC	DISK CHANGE OPTION	X	
NFO	NO FORCE OUT	X	
TS	TRUE FM DATA SEPARATION	X	
800	SOFT SECTOR OPTION		X
801	HARD SECTOR OPTION	X	

SHUGART SA850/851
8" STANDARD HEIGHT FDD

Designator	Description	Open	Short
5E	TERMINATIONS		X
1B,2B, 3B,4B	SIDE SELECT USING DRIVE SELECT	X	
RR	RADIAL READY		X
RI	RADIAL INDEX		X
R	READY OUTPUT		X
2S	TWO-SIDED OUTPUT		X
850/851	SECTOR OPTION	851	850
I	INDEX OUTPUT		X
S	SECTOR OUTPUT	X	
DC	DISK CHANGE OPTION	X	
HL	STEPPER PWR FROM HEAD LOAD	X	
DS	STEPPER PWR FROM DRIVE SEL		X
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
D	ALT IN USE INPUT	X	
M	MULTI-MEDIA OPTION		X
DL	DOOR LOCK LATCH OPTION	X	
A	RADIAL HEAD LOAD		X
B	RADIAL HEAD LOAD	X	
X	RADIAL HEAD LOAD		X
C	ALT INPUT - HEAD LOAD		X
Z	IN USE FROM DRIVE SELECT	X	
Y	IN USE FROM HEAD LOAD		X
S1	SIDE SELECT USING DIR SEL	X	
S2	STANDARD SIDE SELECT		X
S3	SIDE SELECT USING DRIVE SEL	X	
TS,FS	DATA SEPARATION OPTION	TS	FS
IW	WRITE CURRENT SWITCH		X
RS	READY STANDARD	X	
RM	READY MODIFIED		X
HLL	HEAD LOAD LATCH	X	
IT	IN USE TERMINATOR	X	
HI	IN USE FROM HEAD LD OR IN USE	X	
F	MMFM	X	
AF	FM OR MFM		X
NF	MMFM	X	

NEC FD1160
Standard Height 8" FDD

Option	Description	Position
P60	LED Display	FDL
P57	Step Motor Power	.C
P58	Write Protect	PRI
P53	Ready Status	N
P52	Head Load	HLS
P54, P55	Drive Select	(As Desired)
P51	Door Lock	DLD
P56	File Unsafe Inhibit	IFU
P59	Door Lock Hold	N

SIEMENS FDD 200-8
 8" STANDARD HEIGHT FDD

Designator	desription	Open	Short
RADIAL SELECT			X
RADIAL STEP		1	2
SS	SOFT SECTORING ENABLE		X
U			X
SE		X	
RD		X	
HD			X
4			X
L			X
J		X	
TE		X	
SE			X
HFRG		FR	HF
K		X	
14		X	
RR			X
RI			X
C		X	
3		X	
V		X	
E			X
7			X
8		X	
M		X	
10,12,18,20,22,24			X
BINARY SELECT 1-7			

MITSUBISHI M2896-63
8" HALF HEIGHT FDD

Designator	Description	Open	Short
JFG	FRAME GND/SIGNAL GND SHORT		X
JSG	FRAME GND/SIGNAL GND OPEN	X	
1B,2B, 3B,4B	SIDE SELECT USING DRIVE SELECT	X	
SE	EXT WRITE CURRENT SWITCH	X	
SI	INT WRITE CURRENT SWITCH		X
S	"KEEP OPEN"	X	
DC	DISK CHANGE OPTION	X	
2S	TWO-SIDED OUTPUT		X
IT	IN USE TERMINATOR		X
D	ALT IN USE INPUT	X	
HI	HEAD LOAD OR IN USE	X	
C	ALT INPUT - HEAD LOAD		X
I	INDEX OUTPUT		X
R	READY OUTPUT		X
S1	SIDE SELECT USING DIR SEL	X	
S2	STANDARD SIDE SELECT		X
S3	SIDE SELECT USING DRIVE SEL	X	
RS	READY STANDARD	X	
RM	READY MODIFIED		X
RFa	"KEEP PLUGGED"		X
RFb	"KEEP OPEN"	X	
MO	MOTOR ON FROM HEAD LOAD	X	
MS	MOTOR ON FROM DRIVE SELECT	X	
Z	IN USE FROM DRIVE SELECT	X	
NP	WRITE PROTECT DISABLE	X	
WP	WRITE PROTECT ENABLE		X
A	RADIAL HEAD LOAD		X
B	RADIAL HEAD LOAD	X	
X	RADIAL HEAD LOAD		X
BS0	"KEEP PLUGGED"		X
BS1	"KEEP OPEN"	X	
RI	RADIAL INDEX		X
RR	RADIAL READY		X
Y	IN USE FROM HEAD LOAD		X
V	DOOR LOCK FROM HEAD LOAD		X
HLL	HEAD LOAD LATCH	X	
DL	DOOR LOCK LATCH OPTION	X	

NOTE: IN ADDITION TO THE ABOVE CONFIGURATION, THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THE SYSTEMASTER-II.

1. ON COMPONENT SIDE OF THE SYSTEMASTER-II, CUT THE TRACE GOING TO PIN 9 OF U1.
2. ON THE SOLDER SIDE OF THE SYSTEMASTER-II, JUMPER PIN 9 AND PIN 7 OF U1 TOGETHER.

QUMETRACK 242
8" HALF HEIGHT FDD

Designator	Description	Open	Short
A	RADIAL HEAD LOAD		X
B	"		X
X	"	X	
Z	IN USE FROM DRIVE SELECT	X	
HL	STEPPER POWER FROM HEAD LOAD		X
R	ALTERNATE OUTPUT READY PAD		X
I	ALTERNATE OUTPUT INDEX PAD		X
C	ALTERNATE INPUT HEAD LOAD		X
D	ALTERNATE INPUT IN USE		X
DC	ALTERNATE OUTPUT DISK CHANGE	X	
2S	ALTERNATE OUTPUT TWO SIDED DISK		X
Y	IN USE FROM HEAD LOAD		X
DL	DOOR LOCK LATCH	X	
RR	RADIAL READY		X
RI	RADIAL INDEX		X
WP	INHIBIT WRITE WHEN WRITE PROTECT		X
NP	ALLOW WRITE WHEN WRITE PROTECT	X	
D1, D2, D4, DDS	DRIVE ADDRESS SELECT (UP TO 8 DRIVES)	X	
B1-B4	TWO, DOUBLE-SIDED DRIVE SELECT	X	
S1	HEAD SELECT OPTION	X	
S2	"		X
S3	"	X	
T40	TEST TRACK 40	X	
HA	TEST ACTUATE HEAD LOAD	X	
4, 6, 8, 10	ALTERNATE I/O PINS	X	
12, 16, 18, 24	"	X	
SF	SWITCH FILTER		X
P	STEPPER POWER (USED WITH HL)	X	

NOTE: IN ADDITION TO THE ABOVE CONFIGURATION, THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THE SYSTEMASTER-II.

1. ON COMPONENT SIDE OF THE SYSTEMASTER-II, CUT THE TRACE GOING TO PIN 9 OF U1.
2. ON THE SOLDER SIDE OF THE SYSTEMASTER-II, JUMPER PIN 9 AND PIN 7 OF U1 TOGETHER.

SHUGART SA810/860
8" HALF HEIGHT FDD

Designator	Description	Open	Short
U9	TERMINATION		X
SI	INT WRITE CURRENT SWITCH		X
SE	EXT WRITE CURRENT SWITCH	X	
TR	TRUE READY OUTPUT	X	
RTR	RADIAL TRUE READY	X	
2S	TWO-SIDED OUTPUT		X
DC	DISK CHANGE OPTION	X	
S1	SIDE SELECT USING DIR SEL	X	
S2	STANDARD SIDE SELECT		X
S3	SIDE SELECT USING DRIVE SEL	X	
1B,2B, 3B,4B	SIDE SELECT USING DRIVE SELECT	X	
D	ALT IN USE INPUT	X	
MS	MOTOR ON FROM DRIVE SELECT		X
MO	ALT INPUT MOTOR ON	X	
MMO	ALT INPUT MULTIPLEXED MO	X	
MD	MOTOR OFF DELAY		X
R	READY OUTPUT		X
RR	RADIAL READY		X
SR	READY STANDARD		X
MT	READY MODIFIED	X	
Y	IN USE FROM HEAD LOAD	X	
Z	IN USE FROM DRIVE SELECT	X	
PD	STEPPER POWER DOWN	X	
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
TS	DATA SEPARATION SELECT	X	

**In order to achieve proper operation of the door lock and in use LED, install a wire wrap jumper from MMO to Y1.

NOTE: IN ADDITION TO THE ABOVE CONFIGURATION, THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THE SYSTEMASTER-II.

1. ON COMPONENT SIDE OF THE SYSTEMASTER-II, CUT THE TRACE GOING TO PIN 9 OF U1.
2. ON THE SOLDER SIDE OF THE SYSTEMASTER-II, JUMPER PIN 9 AND PIN 7 OF U1 TOGETHER.

NEC FD1165
8" HALF HEIGHT FDD

Designator	Description	Position
DX1, DX2	DRIVE SELECT	AS DESIRED
DX3,DX4	"	"
HL	HEAD LOAD	1
RX	RADIAL READY	1
SS	SIDE SELECT	1
PR	WRITE PROTECT	1
FR	FILE UNSAFE	1
DR	DOOR LOCK	1
DL	"	1
DH	"	1
US	IN USE	1
RD	READ DATA	1
BS	BUSY LAMP	2
BU	"	2

TERMINATION ON LAST PHYSICAL DRIVE ONLY.

NOTE: IN ADDITION TO THE ABOVE CONFIGURATION, THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THE SYSTEMASTER-II.

1. ON COMPONENT SIDE OF THE SYSTEMASTER-II, CUT THE TRACE GOING TO PIN 9 OF U1.
2. ON THE SOLDER SIDE OF THE SYSTEMASTER-II, JUMPER PIN 9 AND PIN 7 OF U1 TOGETHER.

TANDON TM848
8" HALF HEIGHT FDD

Designator	Description	Open	Short
S1	SIDE SELECT USING DIR SEL	X	
S2	STANDARD SIDE SELECT		X
S3	SIDE SELECT USING DRIVE SEL	X	
1B,2B, 3B,4B	SIDE SELECT USING DRIVE SELECT	X	
PS	POWER SAVE		X
PS*	STEPPER POWER ON ALWAYS	X	
DS	STEPPER POWER FROM DRIVE SEL		X
HL	STEPPER POWER FROM HEAD LOAD	X	
M1	MOTOR DELAY ENABLE		X
M3	MOTOR CONTROL FROM SELECT	X	
M4	MOTOR CONTROL FROM HEAD LOAD		X ***
MOL	MOTOR CONTROL SIGNAL, LOW TRUE		X
MOH	MOTOR CONTROL SIGNAL, HIGH TRUE	X	
MC1,MC2, MC3,MC4	MOTOR CONTROL SELECT	X	
R	READY		X
TR	TRUE READY	X	
DL	LEVER LOCK	X	
D	ALT IN USE INPUT	X	
LL	IN USE, LATCHED	X	
NL	IN USE, NOT LATCHED		X
DC	DISK CHANGE OPTION	X	
2S	TWO-SIDED OUTPUT		X
WP	WRITE PROTECT ENABLE		X
NP	WRITE PROTECT DISABLE	X	
XC	EXT WRITE CURRENT SWITCH	X	
IC	INT WRITE CURRENT SWITCH		X
DM	DIAGNOSTIC MODE	X	

***NOTE - This drive monitors pin 18 (normally HEAD LOAD) for the MOTOR ON function. MOTOR ON requires a 165 msec minimum delay before R/W activity can begin.

NOTE: IN ADDITION TO THE ABOVE CONFIGURATION, THE FOLLOWING MODIFICATIONS ARE REQUIRED ON THE SYSTEMASTER-II.

1. ON COMPONENT SIDE OF THE SYSTEMASTER-II, CUT THE TRACE GOING TO PIN 9 OF U1.
2. ON THE SOLDER SIDE OF THE SYSTEMASTER-II, JUMPER PIN 9 AND PIN 7 OF U1 TOGETHER.