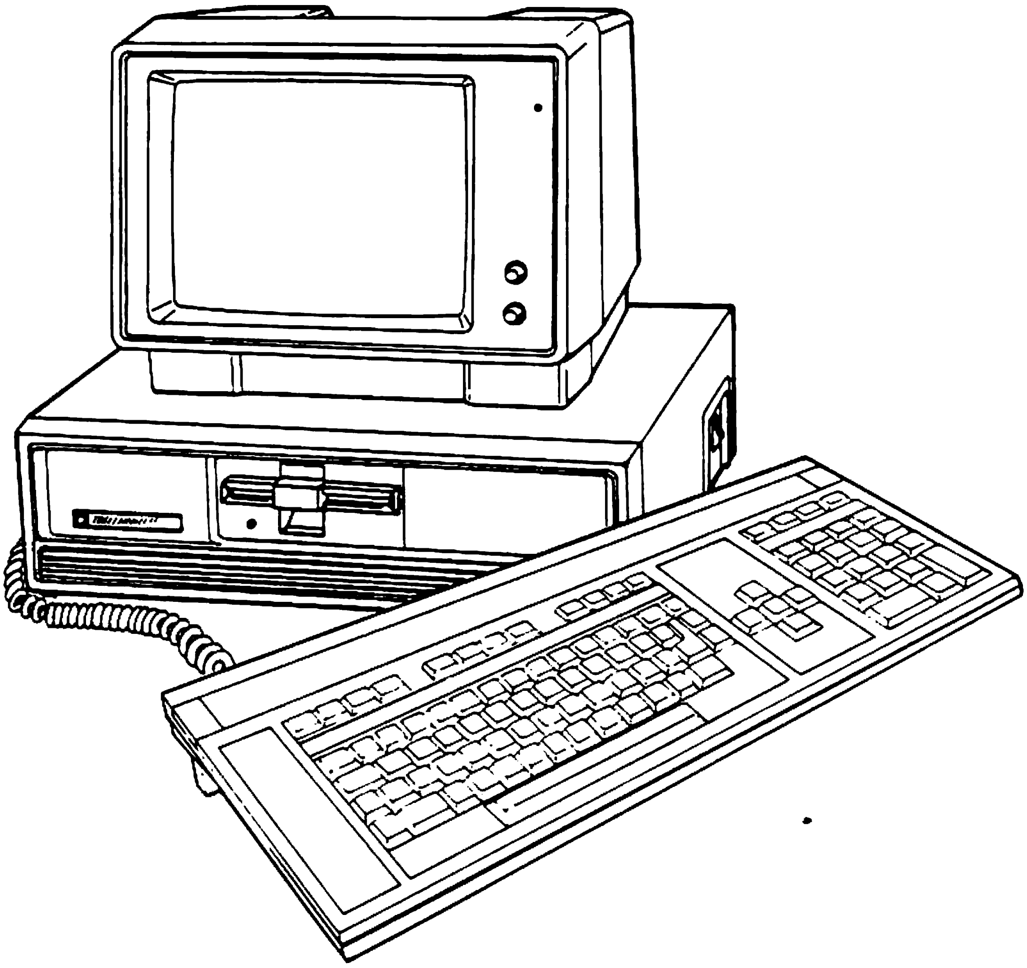
Texas Instruments Professional Computer



Technical Reference Manual

PRELIMINARY

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PREFACE

The Technical Reference Manual is designed to provide the software and hardware designer, and other technical persons with detailed information as to how the Texas Instruments Professional Computer is designed and how it functions.

This manual is divided into five major sections:

Section 1. Introduction - Provides a general description of the Texas Instruments Professional Computer, and identifies various configurations, options, and accessories.

Section 2. Hardware - Provides a detailed description of each component of the system, including options. This section also contains specifications for power and interface information. It provides hardware programming data such as coding tables, registers and signal pin-outs.

Section 3. Systems - Describes the ROM BIOS, interrupt vector lists, keyboard scan coding table, and a complete memory map.

Section 4. Assembly Drawings and Lists of Materials - Provides detailed drawings for all field replaceable assemblies and options. A List of Materials is provided with each assembly drawing for identification of all components and piece parts.

Section 5. Schematics - Provides logic diagrams and schematics for each component and field replaceable assembly of the Texas Instruments Professional Computer.

The Glossary contains a definition of technical terms used in this manual.

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Section 1

INTRODUCTION

The Texas Instruments Professional Computer system consists of three major units: the system unit, the keyboard, and the display unit. A number of options are available, such as 320-kbyte diskette drives, expansion memory to expand the system memory in 64-kbyte increments up to a total of 256 kbytes, a synchronous-asynchronous communications board, a Winchester disk drive option, an internal modem board, a graphics controller board, a clock and analog interface, and a high-resolution color display unit.

The system unit is the heart of the computer. In its basic configuration it contains the central processing unit (CPU) circuitry, floppy disk controller circuitry, a parallel printer port, power supply, a diskette drive, read-only memory (ROM), and 64 kbytes of dynamic random-access memory (RAM). A cathode-ray tube (CRT) controller board is standard equipment.

The system unit board is a large 361.95 x 215.9 mm (14.25 x 8.5 in) printed wiring board mounted horizontally on the bottom of the system unit chassis. The system unit board houses the microprocessor and control circuitry. It provides five sockets on an expansion bus for option boards plus an additional socket for a memory expansion option The system memory can be expanded in 64-kbyte increments to a total of 256 kbytes.

The 5 1/4-in diskette drive is a mass storage device for reading or writing data to a removable diskette. The standard diskette drive stores approximately 320-kbytes of data. The system unit provides space for the installation of a second diskette drive or a Winchester disk drive. The Winchester disk drive and controller option is available in 5-, 10-, or 15-megabyte capacities. The Texas Instruments Professional Computer uses double-density, modified frequency modulation (MFM) recording format.

Diskettes used with the Texas Instruments Professional Computer must be certified double-sided, dual-density, soft-sectored, 5 1/4-in diskettes.

The system unit power supply is a switching-type 160-watt (W) unit with three output levels. The supply is rated to support a system equipped with any combination of options.

The low-profile keyboard is designed for the operator's ease of use. The large, sculptured, typewriter-like, keyboard keys are used to enter alphanumeric data. The smaller numeric keypad can be used as a calculator. Between these two groups of keys is a cluster of five keys that controls the display cursor movement. Across the top of the keyboard are the twelve programmable function keys, which are arranged in three groups of four keys each. The features of the keyboard include:

* A sculptured, low-profile keyboard, which complies with the European 30-mm home row height requirements.

* An infinitely adjustable full-length tilt-bar, which has a range of positions from 5 degrees to 15 degrees to suit an individual user's preference.

* Tactile designed F and J keys, which let your fingers find the "home" position on the home row. A raised dot on the numeric keyboard number 5 indicates the center key on the pad and provides reassurance to the operator.

* A separate microprocessor on the keyboard, which converts keystrokes into character information. Separate keyboard diagnostics are conducted on every power-up.

The display unit may be either a monochrome or color unit, depending upon the system configuration. The standard CRT controller board furnished with the system unit supports either a color or monochrome display.

The graphics controller option is available in either one or three planes. It provides a resolution of 720 horizontal by 300 vertical picture elements (pixels) for a 60 hertz (Hz) system and a resolution of 720 horizontal by 350 vertical pixels for a 50 Hz system.

The synchronous-asynchronous communications (sync-async comm) board option provides both synchronous and asynchronous communications using an RS-232-C interface. It supports asynchronous data rates from 50 bits per second to as high as 19 200 bits per second.

The internal modem board option is available in two versions, either a 300-baud board providing Bell 103-compatible communication, or a 300/1200-baud board providing Bell 212A-compatible communications.

Section 2

HARDWARE

2.1 INTRODUCTION

This section describes the design and functions of the hardware for the Texas Instruments Professional Computer system. A block diagram of the system is shown in Figure 2-1.

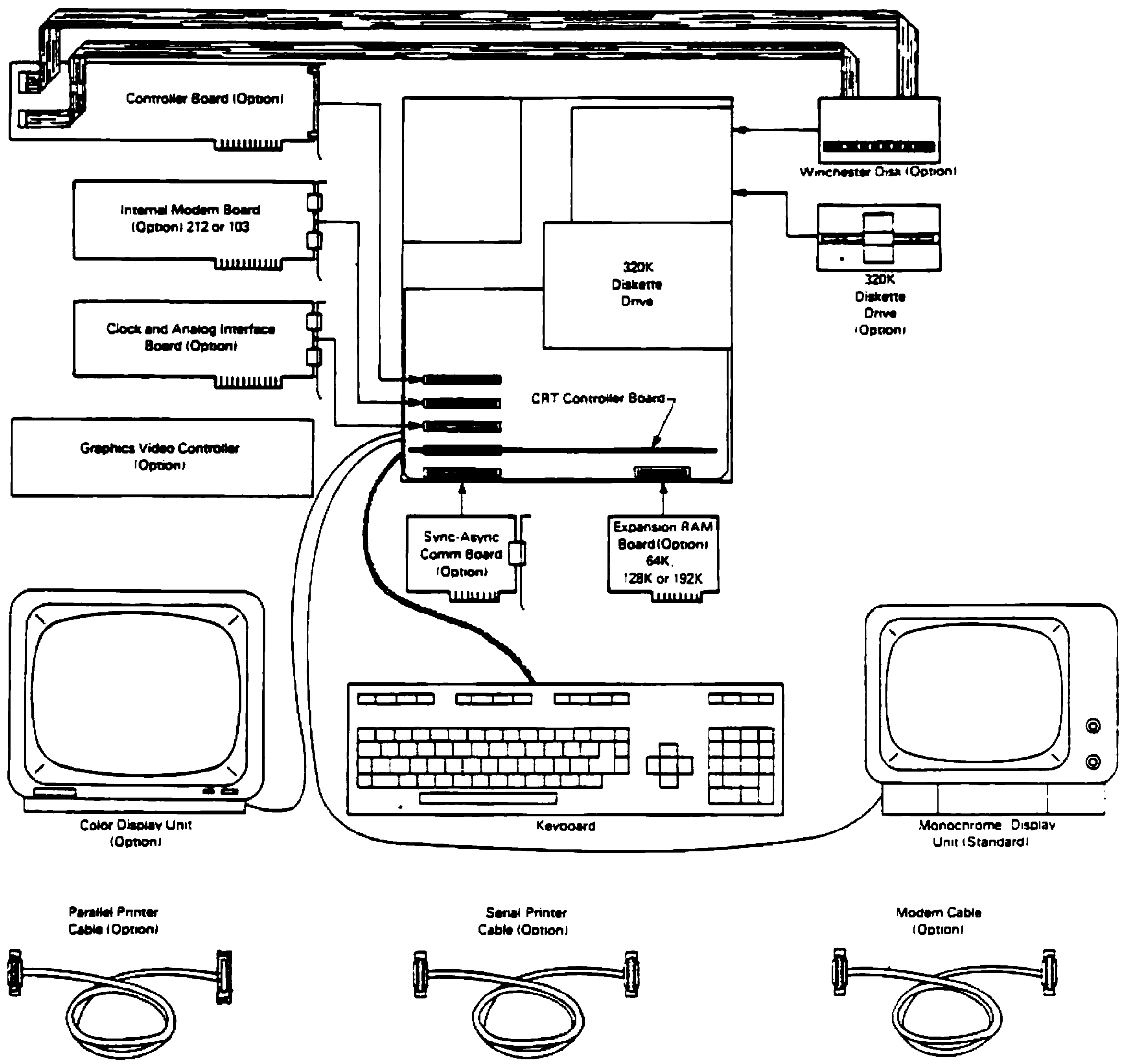


Figure 2-1 System Block Diagram

2.2 SYSTEM UNIT BOARD

The system unit board (contained within the system unit) is the heart of the computer. A block diagram of its operating parts is shown in Figure 2-2. The system unit board (also called the "motherboard") contains the following.

* System CPU
* 64 kbytes of RAM memory
* Memory control logic
* Input/Output (I/O) to the keyboard unit, printer port, and diskette drives
* Timing services
* Expansion bus for the CRT controller and options. Refer to Section 5, drawing 2223005, for logic diagrams.

2.3 SYSTEM CPU Dwg #2223005 Sh.5

The system CPU consists of one major component - an Intel 8088 central processor - and an optional Intel 8087 numeric coprocessor. Also included in the system CPU are the processor clock circuits, bus buffers and latches, and CPU status decoding and control line generation.

Because the 8088 and 8087 processors are designed to work together in such a way that they appear to attached components to be a single chip, it is easy to upgrade the system with an 8087 processor at a later time. From this point, the term CPU refers to both devices.

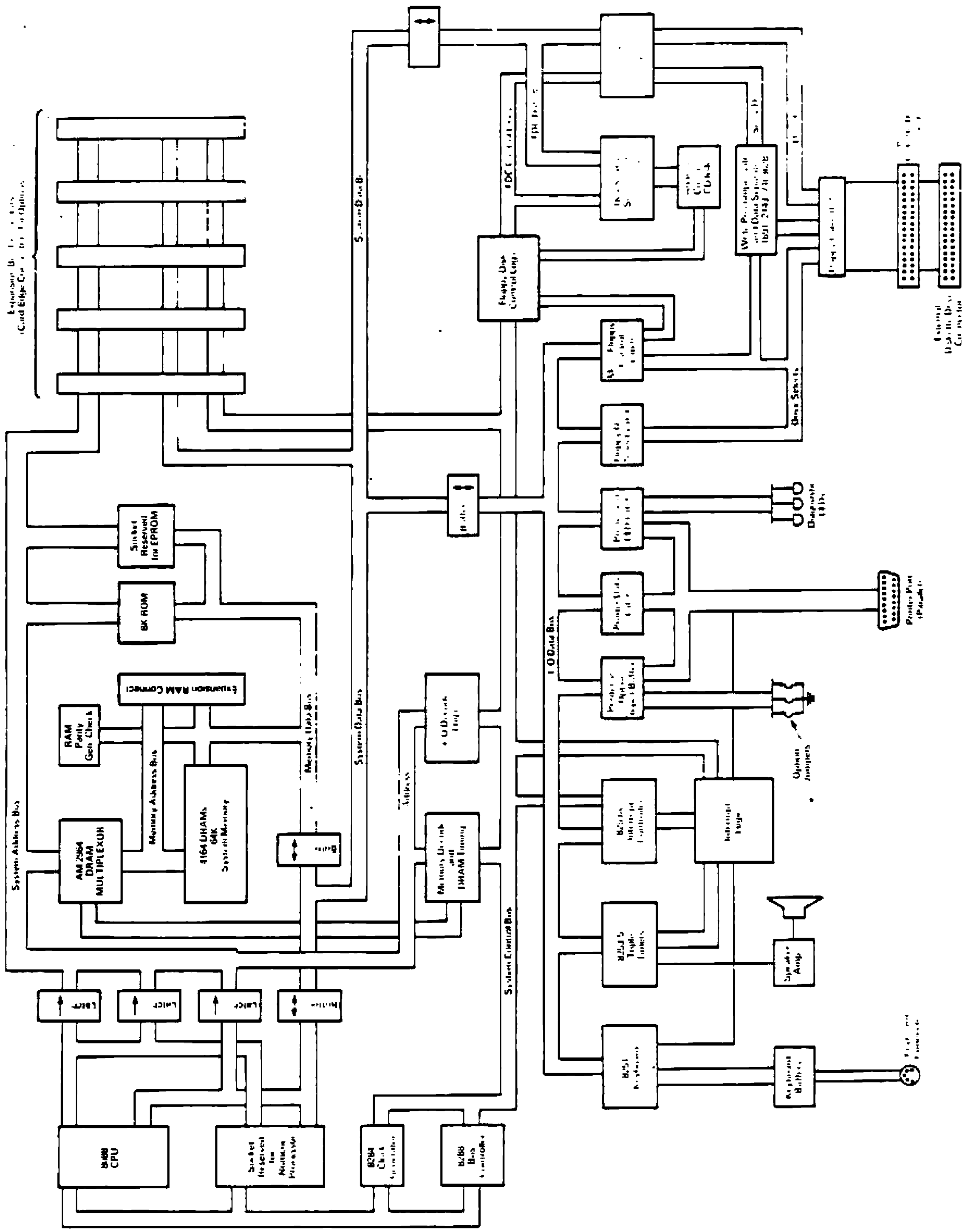


Figure 2-2 System Unit Board Block Diagram

2.3.1 CPU Bus Buffering

The CPU is designed to operate in the so-called "maximum" mode for this integrated circuit. (For additional information, see the Intel literature on the 8088 and 8087.) The CPU uses a multiplexed address and data bus in order to reduce the number of pins required on the processor chip. For this reason, and to provide adequate buffering for the address and data lines on the expansion bus, a set of address latches (U5, U6, U7) and a data bus buffer (U8) are provided as part of the CPU.

2.3.2 CPU Clock Generator

The CPU clock generator consists of an Intel-designed 8284 integrated circuit, a crystal and some discrete components. The crystal frequency is 15.0 megahertz (MHz) +/-0.01 percent. The 8284 (U4) divides the crystal frequency by 3 to obtain the CPU clock frequency of 5.0 MHz. The 8284 also contains synchronizing logic for the WAIT- line from the expansion bus and memory subsystem and the RESET- line from the power-good circuit.

2.3.3 CPU Bus Controller

The CPU bus controller chip (U3 8288) takes the status information from the processor and converts it into the lines MRDC- (memory read), AMWC- (advanced memory write), IORC- (I/O read), AIOWC- (advanced I/O write), INTA (interrupt acknowledge), DEN (data buffer enable), and DT/R (data buffer direction control). The DEN signal is qualified with the DMA (direct memory access) signal before it is used to prevent premature activation of the system bus buffers during a DMA operation.

A simple open-loop signature analysis (SA) arrangement is provided to check out the CPU. Connecting E17 and E18 with a jumper and resetting the system (power up) causes the processor to execute a OBFH opcode. The jumper disables the system data bus buffer U8, and the pullup resistors in U66 pull the bus up to a high state. The transistor Q1 pulls down data line AD6 to provide the "0" bit in the opcode. The processor then cycles through addresses FFFF0H to FFFFFH and 00000H to 0FFF0H during the SA loop due to the segmented architecture.

NOTE

> The symbol "H" and the term "hex" denote a hexadecimal address or value.

2.3.4 Reset Circuit

The power-good or reset detection circuit is designed to detect conditions where the power on the motherboard is not sufficient to provide reliable operation. This circuit monitors the 12-V power. This condition causes automatic restart in the event of a power dropout severe enough to affect the power supply but not enough to completely shut it down. A resistor/capacitor having a discharge transistor combination is used to ensure that any power-up or dropout causes the RESET line to be true for at least 3 milliseconds (ms).

2.3.5 Optional Numeric Coprocessor

The system unit board is designed to allow the addition of an 8087 numeric coprocessor integrated circuit (IC). Once the 8087 is inserted into the socket provided, the special ESCape instructions in the instruction stream are decoded by both the 8088 and the 8087. The 8088 does any memory access computations required and accesses the first byte of memory according to the instruction. The 8087, after decoding the instruction, "catches" the address generated by the 8088 for the memory access and requests the bus from the 8088 to finish accessing the memory as required. When the coprocessor is finished with the bus, it releases it to the 8088 which then continues with the next instruction. The hardware implements the WAIT instruction of the 8088 to allow synchronization with the 8087 when required.

2.4 SYSTEM UNIT INPUT/OUTPUT (I/O) SUBSYSTEM Dwg #2223005 Sh.3

The input/output (I/O) subsystem on the system unit board decodes the I/O addresses for all of the devices on the board. The various output latches and the input buffer are also components of the I/O subsystem.

In order to simplify the address decoding of the various I/O devices, only 10 of the available 16 bits of I/O address are decoded for all I/O devices. This means that a maximum of 1024 bytes of I/O are available. The system unit board uses 48 bytes of this space beginning at address 000H, which leaves 976 bytes available for the expansion bus. The system unit board devices that are decoded and their addresses within the CPU (central processor unit) I/O space are listed in Table 2-1.

Table 2-1 System Unit Board I/O Map

ADDRESS	DEVICE	BIT/USE
MAIN BOARD:		
00000	U47 Latch	0 Speaker timer enable
		1 Timer 1 interrupt enable
		2 Timer 2 interrupt enable
		3 Single-density (FM) enable
		4 Track greater than 1/2 (TG43)
		5 Diskette side one enable (FSID-)
		6 Diskette mode control (M1)
		7 Diskette mode control (M0)
00001	U48 Input buffer	0 Option jumper E1-E2
		1 Option jumper E3-E4
		2 Option jumper E5-E6
		3 Parity interrupt pending
		4 Printer port BUSY
		5 Printer port paper out
		6 Printer port printer selected
		7 Printer port NO fault
00002	U49 Latch	0-7 Printer port data outputs
00003	U50 Latch	0 LED 1 OFF
		1 LED 2 OFF
		2 LED 3 OFF
		3
		4 Parity interrupt enable
		5 Printer port not auto feed
		6 Printer port not strobe
		7 Printer port not initialized
00004	U51 Latch	0 Diskette Drive SELECT 1
		1 Diskette Drive SELECT 2
		2 Diskette Drive SELECT 3
		3 Diskette Drive SELECT 4
		4 Diskette Drive MOTOR 1
		5 Diskette Drive MOTOR 2
		6 Diskette Drive MOTOR 3
		7 Diskette Drive MOTOR 4

Table 2-1 System Unit Board I/O Map (continued)

ADDRESS	DEVICE	BIT/USE
MAIN BOARD (Continued):		
00005-0000F	Reserved	
00010	U44 8251 USART	Data Register
00011	U44 8251 USART	Control Register
00012-00013	Reserved	
00014	U45 8253 Timer	Counter 0
00015	U45 8253 Timer	Counter 1
00016	U45 8253 Timer	Counter 2
00017	U45 8253 Timer	Control register
00018	U46 8259A Interrupt controller	
00019	U46 8259A Interrupt controller	
00020	FDC Command register or RAM	
00021	FDC Track register	
00022	FDC Sector register or RAM reset	
00023	FDC Data register	
00024-0002F		Reserved
WINCHESTER CONTROLLER BOARD:		
00030	Winchester I/O port	INPUT: 0-7 Don't care. Data is held for each handshake cycle. OUTPUT: 0-7 Don't care. Data is latched til updated.
00031	Winchester reset register	READ: 0 Data request 1 Input/Output 2 Command/Data 3 Interrupt pending (Level 6) WRITE: 0-7 Don't care (Any write will do a RESET)

Table 2-1 System Unit Board I/O Map (continued)

ADDRESS	DEVICE	BIT	USE
WINCHESTER CONTROLLER BOARD (Continued):			
00032			Not used
00033			Interrupt Mask
		0	Status interrupt enable
		1	Data interrupt disable
FUTURE OPTIONS:			
00034-0003B			Reserved
0003C-0003F			Local Area Net I/O
00040-000BF			Reserved
CLOCK AND ANALOG INTERFACE:			
000C0	Clock/Analog Interface		
		0	End of conversion (EOC)(Active HIGH)
		1	Not used (tied LOW)
		2	Lightpen interrupt latch ON
		3	Battery low
		4	Switch 4
		5	Switch 3
		6	Switch 2
		7	Switch 1
000C1			Do not allow light pen interrupt (tri-state signal)
000C2			Allow light pen interrupt (Pass interrupt signal)
000C8			Joystick port X1 (Current sense)
000C9			Joystick port Y1 (Current sense)
000CA			Joystick port X2 (Current sense)
000CB			Joystick port Y2 (Current sense)
000CC			Analog input 4 (SW4) (Voltage sense)
000CD			Analog input 3 (SW3) (Voltage sense)
000CE			Analog input 2 (SW2) (Voltage sense)
000CF			Analog input 1 (SW1) (Voltage sense)

Table 2-1 System Unit Board I/O Map (continued)

ADDRESS	DEVICE	BIT/USE
CLOCK AND ANALOG INTERFACE (Continued):		
000D0		CLOCK CONTROL
		0 Address Bit 0 MSM5832 clock
		1 Address Bit 1 MSM5832 clock
		2 Address Bit 2 MSM5832 clock
		3 Address Bit 3 MSM5832 clock
		4 HOLD
		5 WRITE
		6 READ
		7 + or - 30 sec adjust
000D1-000D7		Reserved
000D8		Clock data (low nibble only)
000D9-000DF		Reserved
SYNC-ASYNC COMM BOARD:		
000E0-000E3	COMM Port 1 IR1	Interrupt Acknowledge
000E4		CHB Command
000E5		CHB Data
000E6		CHA Command
000E7		CHA Data
000E8-000EB	COMM Port 2 IR2	Interrupt Acknowledge
000EC		CHB Command
000ED		CHB Data
000EE		CHA Command
000EF		CHA Data
000F0-000F3	COMM Port 3 IR3	Interrupt Acknowledge
000F4		CHB Command
000F5		CHB Data
000F6		CHA Command
000F7		CHA Data
000F8-000FB	COMM Port 4 IR4	Interrupt Acknowledge
000FC		CHB Command
000FD		CHB Data
000FE		CHA Command
000FF		CHA Data
00100-003FF		Available for future products

Table 2-3 Printer Port Pinout

SIGNAL	RETURN	SIGNAL NAME	SOURCE	FUNCTION
1	19	DATA STROBE-	System	Data to be sampled when signal is LOW
2		DATA 1	System	Data output bit
3	20(21)	DATA 2	System	
4		DATA 3	System	
5	21(23)	DATA 4	System	
6		DATA 5	System	
7	22(25)	DATA 6	System	
8		DATA 7	System	
9	23(27)	DATA 8	System	
10		ACKNOWLEDGE-	Printer	Indicates that another char can be received
11	24(29)	BUSY	Printer	Indicates no data can be sent when HIGH
12		PAGE END	Printer	Indicates paper is out when HIGH
13		SLCT (ON LINE)	Printer	Indicates printer is on-line when HIGH
14		AUTO FEED-	System	Indicates printer is to linefeed on CR when LOW
15(32)		FAULT-	Printer	Indicates fault when LOW
16(31)	25(30)	INIT-	System	Resets printer when LOW
17(36)	18(33)	SELECTION-	System	Always LOW

2.4.3 Keyboard Port Sh #3 Dwg #2223005

The keyboard port is implemented as a universal asynchronous receiver-transmitter (UART) for serial data transmission between the system unit and the keyboard. Data received by the UART will always generate an interrupt to the interrupt controller. The transmit ready line will not generate an interrupt unless the transmitter in the UART is enabled. Note that the keyboard port interrupt is ORed with the "interrupt request 7" line from the numeric coprocessor.

The receive data signal is conditioned with a SN75189A line receiver with a slowdown capacitor so that the signal is more immune to transients. This receiver also has a hysteresis of approximately 1 V centered around 1.4 V, which improves the noise immunity. The transmit data line is buffered by a SN75189A buffer to provide a good voltage swing and drive to the keyboard cable. This buffer consists internally of an output transistor with a 2-kilo ohms (kohms) pull-up resistor.

In order to allow improved diagnostics, the device service routine (DSR) line on the universal synchronous/asynchronous receiver transmitter (USART) is connected to the keyboard connector through a SN75189A buffer. The transmit data line is connected to the DSR line at the keyboard to allow detection of a disconnected or defective keyboard.

The input clock to the transmit section is 19 531.25 Hz, which when divided by 64 is suitable for a baud rate of 305. The input clock for the receiver is 156 250 Hz, which when divided by 64 is suitable for a baud rate of 2441. These baud rates are close enough to the standard 300- and 2400-baud rates to allow system test equipment to simulate a keyboard having standard equipment.

2.4.4 Timers U45 Sheet #3 Dwg #2223005

The 8253-5 counter/timer IC provides three, separate timing units. In this system, one is used as a programmable speaker oscillator, and the other two are programmable interval timers.

The speaker timer is clocked by a square wave of 1.25 MHz. With the ability to divide by uyp to 65 536, the output frequency can go as low as 19 Hz. The high input frequency causes the output tones to be more musically accurate. The speaker timer clock is internally gated with the speaker enable (SPKEN) signaler enable) which is an output of latch ~~U45~~ U45. This signal allows the interruption of tones without a reprogramming of the timer.

The second timer (Timer A) is used in system-timing applications and as a real-time clock. It generates an interrupt on the rising edge of the timer output if the enable line (address 0 bit 1) is set to a HIGH. Toggling this line LOW resets the interrupt; holding this line low disables the interrupt completely. The level of the interrupt is

Table 2-5 Motherboard Memory Map

ADDRESS	DEVICES	
DYNAMIC RAM:		
00000-0FFFF	64-kbytes motherboard RAM	
10000-1FFFF	64-kbytes expansion RAM board Bank 1	
20000-2FFFF	64-kbytes expansion RAM board Bank 2	
30000-3FFFF	64-kbytes expansion RAM board Bank 3	
40000-BFFFF	Expansion bus memory	
CRT CONTROLLER:		
C0000-C7FFF	Graphics RAM Bank A	
C8000-CFFFF	Graphics RAM Bank B	
D0000-D7FFF	Graphics RAM Bank C	
D8000-DDFFF	Reserved	
DE000-DE7FF	Active character memory	
DE800-DEFFF	Phantom character memory	
DF000	Bit 0	Misc input buffer, BLUE feedback, read only
	Bit 1	Misc input buffer, RED feedback, read only
	Bit 2	Misc input buffer, GREEN feedback, read only
	Bit 3	Misc input buffer, interrupt pending, read only
DF001-DF00F	Misc input buffer	
DF010-DF01F	Graphics RED palette latch, write only	
DF020-DF02F	Graphics GRN palette latch, write only	
DF030-DF03F	Graphics BLU palette latch, write only	
DF040-DF7FF	Reserved	

TABLE 2-5 MOTHORBOARD MEMORY MAP

ADDRESS	DEVICES
00000 => 0FFFF	64-KBYTES MOTHORBOARD RAM
10000 => 1FFFF	64-KBYTES EXPANSION RAM BOARD BANK 1
20000 => 2FFFF	64-KBYTES EXPANSION RAM BOARD BANK 2
30000 => 3FFFF	64-KBYTES EXPANSION RAM BOARD BANK 3
	256-KBYTES
40000 => 4FFFF	64-KBYTES EXPANSION RAM
50000 => 5FFFF	64-KBYTES EXPANSION RAM
60000 => 6FFFF	64-KBYTES EXPANSION RAM
70000 => 7FFFF	64-KBYTES EXPANSION RAM
	512-KBYTES
80000 => 8FFFF	64-KBYTES EXPANSION RAM
90000 => 9FFFF	64-KBYTES EXPANSION RAM
A0000 => AFFFF	64-KBYTES EXPANSION RAM
B0000 => BFFFF	64-KBYTES EXPANSION RAM
	768-KBYTES
C0000 => C7FFF	32-KBYTES GRAPHICS RAM BANK A
C8000 => CFFFF	32-KBYTES GRAPHICS RAM BANK B
D8000 => D7FFF	32-KBYTES GRAPHICS RAM BANK C
D8000 => DBFFF	16-KBYTES RESERVED
DC000 => DDFFF	2-KBYTES RESERVED
DE000 => DE7FF	2-KBYTES CHARACTER MEMORY
DE800 => DEFFF	2-KBYTES CHARACTER ATTRUBUTE MEMORY
DF000 => DF00F	16- BYTES MISC INPUT BUFFER
DF010 => DF01F	16- BYTES RED PALLETTE LATCH
DF020 => DF02F	16- BYTES GREEN PALLETTE LATCH
DF030 => DF03F	16- BYTES BLUE PALLETTE LATCH
DF040 => DF3FF	960-BYTES RESERVED
DF400 => DF7FF	1-KBYTES RESERVED
DF800 => DF80F	16- BYTES ATTRIBUTE LATCH
DF810 => DF81F	16- BYTES CRT CONTROLLER REGISTERS
DF820 => DF82F	16- BYTES MISC OUTPUT LATCH
DF830 => DF83F	16- BYTES
DF840 => DFBFF	960-BYTES RESERVED
DFC00 => DFFFF	1-KBYTES RESERVED
E0000 => E3FFF	16-KBYTES RESERVED FOR SPEECH STORAGE
E4000 => E7FFF	16-KBYTES RESERVED FOR SPEECH STORAGE
E8000 => EBFFF	16-KBYTES RESERVED
EC000 => EFFFF	16-KBYTES RESERVED
F0000 => F3FFF	16-KBYTES RESERVED
F4000 => F5FFF	8-KBYTES ROM SPACE (CLOCK/ANALOG INTERFACE)
F6000 => F7FFF	8-KBYTES ROM SPACE (LOCAL AREA NET OPTION BOARD)
F8000 => F9FFF	8-KBYTES ROM SPACE (WINCHESTER CONTROLER)
FA000 => FBFFF	8-KBYTES ROM SPACE
FC000 => FDFFF	8-KBYTES ROM SPACE
FE000 => FFFFF	8-KBYTES SYSTEM ROM

Table 2-5 Motherboard Memory Map continued

ADDRESS	DEVICES
DF800-DF80F	Attribute latch
DF810	CRT controller address register, write only
DF811	CRT Controller status register, read only
DF812	CRT Controller address register, write only
DF813	CRT Controller address register, write only
DF814-DF81F	Reserved
DF820	
	Bit 7 Misc output latch, interrupt enable
Bit 6	Misc output latch, alphanumerics screen enable

OTHER PERIPHERALS:

DF821-DFFFF	Reserved
E0000-E7FFF	Reserved for speech storage RAM
E8000-F3FFF	Reserved

ROM USAGE:

F4000-F5FFF	8K ROM space(Clock/Analog Interface)
F6000-F7FFF	8K ROM space(Local Area Net Option Board)
F8000-F9FFF	8K ROM space(Winchester Controller)
FA000-FBFFF	8K ROM space(Reserved)
FC000-FDFFF	8K ROM space, 1 wait state (XU62)
FE000-FFFFF	8K system ROM, 1 wait state (U63)

2.6.2 Memory Control Logic Sh#1 + Sh#2

The motherboard expansion memory is separated from the main system data bus by a bidirectional buffer (U61) in order to provide sufficient drive and margin to the data transfers. Decoding and timing for the ROMs is done by a combination of the memory hard array logic (HAL) chip HAL16R4 (U28) and the 74LS139 decoder (U53). Because ROMs and EPROMs (erasable programmable read-only memories) are generally slow devices, a wait state is added to all accesses to these devices.

The ROM access times are listed in Table 2-6.

Table 2-6 ROM Access Times

FUNCTION	TIME REQUIRED (In Nanoseconds)
CS- ROM access	410
ROM address access	577

2.6.2.1 I/O Wait States. The HAL chip also contains the logic to add a wait state to all I/O accesses made by the CPU. The wait state is necessary because many of the I/O devices operate too slowly when the system buffer and setup and decode times are included. With the wait state, the control lines are active approximately 600 nanoseconds (ns).

2.6.2.2 Memory Refresh Logic. The RAM refresh logic is designed to operate synchronously with the accesses to the RAM memory. Refresh cycles are begun only when a RAM memory cycle is not in progress. This implies that the RAM refresh can occur at the same time as accesses to other system memory (ROMs) or I/O space. Each time a refresh cycle begins, a refresh timer (one-shot U29) starts. When it times out, it provides the signal to begin another refresh cycle. This timer is set to 15 us maximum to allow for the worst-case refresh-request latency. To maintain the contents of the RAM under worst-case conditions, the refresh must occur at least 128 times within 2 ms. (The average refresh timing is once per 15.625 us). The worst-case latency for a refresh request is about 600 ns.

Once a refresh cycle has begun, it must be completed (including the precharge) before the next cycle. If a RAM access cycle is started before the refresh cycle is completed, the HAL state machine will put the CPU into a wait state until the refresh operation is completed. In the worst case, this delay could mean extending the normal memory access time by four wait states, or 800 ns.

Assuming a refresh timer value of 14 us and an average 600-ns slowdown of the CPU, the refresh overhead is about 4.3 percent average or 5.7 percent worst case.

2.6.2.3 CAS and Address Multiplexer Switch. The address multiplexer control (SWM) is produced by a delay line off of the row address strobe input (RASI-) line. This SWM ensures an adequate row address hold time (40 ns) and still operates the RAM quickly enough to finish the access within the system cycle time.

The column address strobe input (CASI-) timing depends on whether the cycle is a read or a write. If the cycle is a read, the CASI- signal is taken off of the delay line 20 ns after the SWM signal (ACAS-). This delay provides an adequate column address setup time to the RAM and still gives fast RAM access. If the cycle is a write, then the CASI- signal is taken from the falling edge of the system clock, which is about 150 ns after the occurrence of RASI-. This delay allows time for the data from the processor to propagate through the data buffers and the parity generator chip (U31 74LS280).

To control the generation of the CASI- pulse, flip-flop U33 is timed with the system clock (CLK-), samples the delay line (ACAS-), and is reset by the memory read (MRDC-) signal. The output of the flip-flop is then logically ANDed (U34) with the ACAS- signal to generate the actual CASI- signal. To prevent the generation of a CASI- pulse during refresh, flip-flop U33 is held in the preset state during a refresh by the refresh row address strobe (RRAS-) line. This forces the output of OR gate U34 (CASI-) to a high level.

2.6.2.4 Parity Generation and Checking. The parity generator/checker chip (74LS280) generates a "1" to the parity RAM bit whenever there is an even number of "1"s in the data byte being written. This is done by using a separate data bus on the parity RAM chip and using a pullup resistor to provide a high on its output whenever it is not driving the output line (as in a write cycle). The parity data is then taken from the "odd sum" output of the parity generator and used to write to the RAM.

By using this method of parity checking, an attempt to read from non-existent RAM memory does not result in a parity error. This method is preferable because system software sometimes "feels" for memory <u>not</u> present in order to determine the size of system memory.

When the RAM is read, all of the data bits and the parity bit are presented to the generator/checker and the parity output is sampled at the end of the read cycle. If the parity is bad, flip-flop U33 is set to interrupt the CPU if enabled. Note that once set, this flip-flop must be reset by software before additional interrupts can be given. If the enable bit (addr 3 bit 3) is held low, then no parity interrupts(PINT) are generated. In order to distinguish the parity interrupt from other NMIs, the PINT line is fed to U48 (address 1 bit 3) to allow testing by software.

2.6.2.5 Memory Control State Machine. The memory control is driven by an array logic device which is set up as a state machine (HAL16R4 U28). The memory control state machine logic is given in Table 2-7. This device has four outputs equipped with a set of clocked flip-flops and four outputs, which are direct combinations of the inputs. Note that the AND of the terms on a line ORed with the AND of terms on other lines results in low-going outputs. This occurs either directly, on those outputs without registers, or after the clock on those outputs with registers.

Table 2-7 Memory Control State Machine Logic - HAL16R4

INPUTS

Outputs	MRD-	MWR-	RFRQ	XA19	XA18	RMX-	IORC-	AIOWC-	RASI-	XWAIT-	MDEN-	RMSEL-	RFSH-	RRAS-	SY-	SX-	
RASI-	L	.	.	L	L	.	.	.	.	.	.	.	H	.	H	.	MEMORY READ
or	.	L	.	L	L	.	.	.	.	.	.	.	H	.	H	.	MEMORY WRITE
or	.	.	.	.	.	.	.	.	.	.	.	.	L	L	.	.	REFRESH
or	.	.	.	.	.	.	.	.	.	.	.	.	L	L	.	.	all other OR terms
XWAIT-	L	.	.	L	.	.	.	.	.	.	.	.	L	.	.	.	REFRESH+READ RF1, 2, 3
or	L	.	.	L	.	.	.	.	.	.	.	.	.	.	L	.	REFRESH+READ RF3, 4
or	.	L	.	L	.	.	.	.	.	.	.	.	L	.	.	.	REFRESH+WRITE RF1, 2, 3
or	.	L	.	L	.	.	.	.	.	.	.	.	.	.	L	.	REFRESH+WRITE RF3, 4
or	.	.	.	H	H	L	.	.	.	.	.	L	.	.	.	H	ROM READ/WRITE
or	.	.	.	.	.	.	L	.	.	.	.	.	.	.	.	H	I/O READ
or	.	.	.	.	.	.	.	L	.	.	.	.	.	.	.	H	I/O WRITE
MDEN-	.	.	.	.	.	.	.	.	L	.	.	.	H	.	H	.	RAM READ/WRITE
or	L	.	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM READ
or	.	L	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM WRITE
or	.	.	.	.	.	.	L	L	.	.	.	.	.	.	.	.	all other OR terms
RMSEL-	L	.	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM READ
or	.	L	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM WRITE
or	.	.	.	.	.	.	L	L	.	.	.	.	.	.	.	.	all other OR terms

THE FOLLOWING FOUR OUTPUTS HAVE FLIP-FLOPS

Outputs	MRD-	MWR-	RFRQ	XA19	XA18	RMX-	IORC-	AIOWC-	RASI-	XWAIT-	MDEN-	RMSEL-	RFSH-	RRAS-	SY-	SX-	
RFSH-	H	H	H	.	.	.	.	.	.	.	.	.	.	.	H	.	RFSH RF1 NO MEM CYC
or	.	.	H	H	.	.	.	.	.	.	.	.	.	.	H	.	RFSH RF1 NO RAM CYC
or	.	.	.	.	.	.	.	.	.	.	.	.	L	.	H	.	REFRESH RF2, 3
or	.	.	.	.	.	.	.	.	.	.	.	.	L	.	H	.	all other OR terms
RRAS-	.	.	.	.	.	.	.	.	.	.	.	.	L	.	.	.	REFRESH RF2, 3, 4
or	.	.	.	.	.	.	.	.	.	.	.	.	L	.	.	.	all other OR terms
SY-	.	.	.	.	.	.	.	.	.	.	.	.	L	L	.	.	REFRESH RF3, 4
or	.	.	.	.	.	.	.	.	.	.	.	.	L	L	.	.	all other OR terms
SX-	L	.	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM READ WAIT CUTOFF
or	.	L	.	H	H	L	.	.	.	.	.	.	.	.	.	.	ROM WRITE WAIT CUTOFF
or	.	.	.	.	.	.	L	.	.	.	.	.	.	.	.	.	I/O READ WAIT CUTOFF
or	.	.	.	.	.	.	.	L	.	.	.	.	.	.	.	.	I/O WRITE WAIT CUTOFF
or	.	.	.	.	.	.	.	L	.	.	.	.	.	.	.	.	all other OR terms

The signal RASI- activates RAS- out of the AM2964B RAM address multiplexer. The signal XWAIT- puts the processor into a wait state. The signal MDEN- activates the motherboard memory system data buffer. The signal RMSEL- selects access to the ROMs. The signal RFSH- controls the AM2964B address multiplexer to put the refresh address out. The signal RRAS- indicates that a refresh RAS is in progress. The signal SY- is used internally to the HAL to indicate refresh states. The signal SX- is used internally to the HAL to cut off the wait state to the CPU after one cycle.

A timing diagram of the memory system, shown in Figure 2-3, indicates the major operations of the memory system.

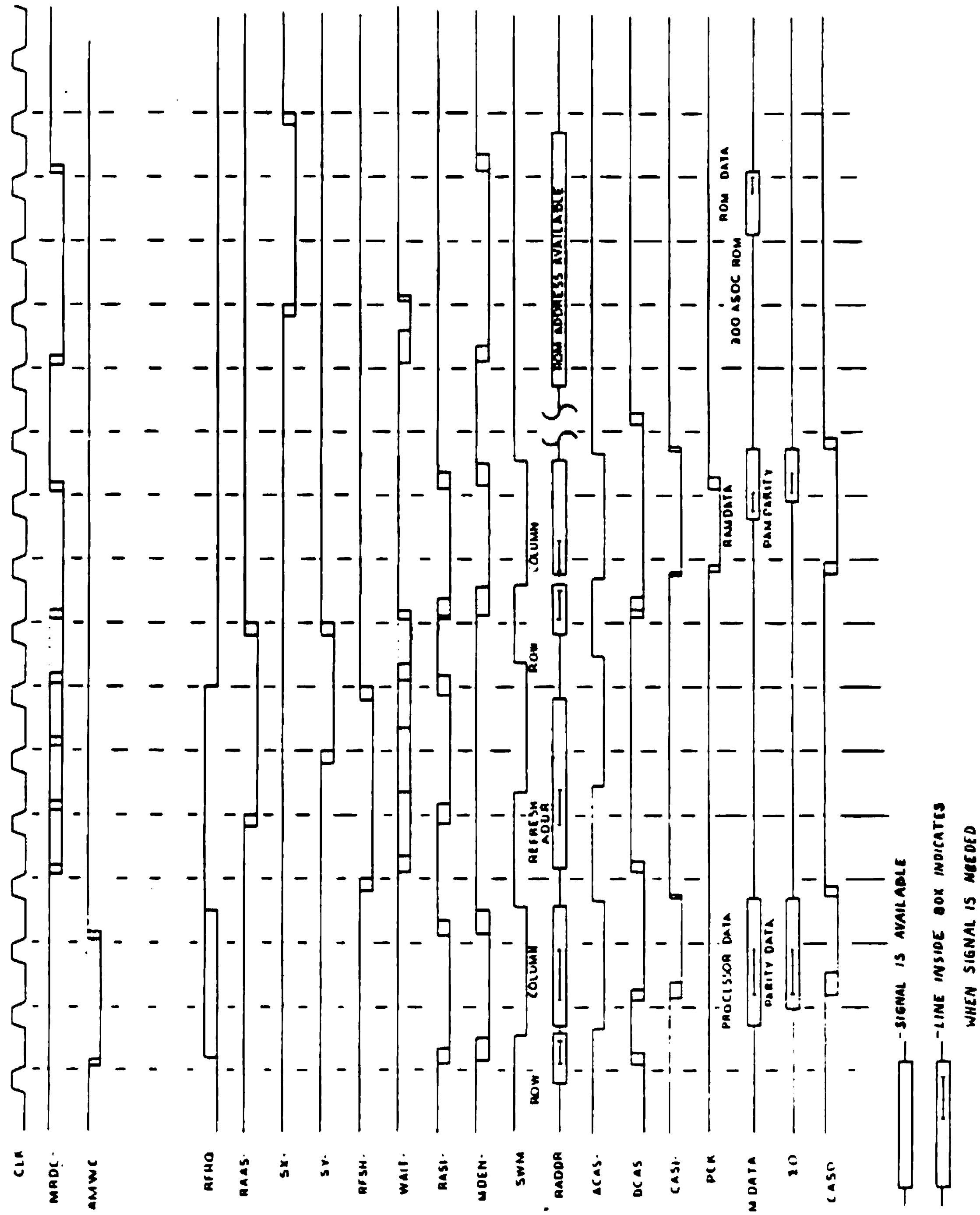


Figure 2-3 Memory System Timing Diagram

2.7 EXPANSION BUS Sh #1 Dwg # 2223005

The expansion interface bus allows the addition to the system of standard and option devices. Five expansion bus connectors are provided. The expansion bus pin-outs are given in Table 2-8.

The expansion interface bus allows memory-mapped or I/O-mapped devices to be added to the system in a straightforward way. The bus supports devices requiring interrupts for efficient operation. The system does not provide Direct Memory Access (DMA) hardware, because devices that require direct memory access have their own special-purpose hardware.

Table 2-8 Expansion Bus Pin-outs

PIN	SIGNAL	PIN	SIGNAL
A01	NMI-	B01	GROUND
A02	DATA 7	B02	RESET
A03	DATA 6	B03	+5 V power
A04	DATA 5	B04	IR0 (interrupt 0)
A05	DATA 4	B05	No connection (bussed)
A06	DATA 3	B06	No connection (bussed)
A07	DATA 2	B07	-12 V power
A08	DATA 1	B08	DMA- (CPU enable)
A09	DATA 0	B09	+12 V power
A10	WAIT-	B10	GROUND
A11	LOGIC GROUND	B11	AMWC- (memory write)
A12	ADDRESS 19 (MSB)	B12	MRDC- (memory read)
A13	ADDRESS 18	B13	AIOWC- (I/O write)
A14	ADDRESS 17	B14	IORC- (I/O read)
A15	ADDRESS 16	B15	No connection (bussed)
A16	ADDRESS 15	B16	No connection (bussed)
A17	ADDRESS 14	B17	No connection (bussed)
A18	ADDRESS 13	B18	No connection (bussed)
A19	ADDRESS 12	B19	No connection (bussed)
A20	ADDRESS 11	B20	PCLK (5-MHz clock)
A21	ADDRESS 10	B21	IR6 (interrupt 6)
A22	ADDRESS 9	B22	IR5 (interrupt 5)
A23	ADDRESS 8	B23	IR4 (interrupt 4)
A24	ADDRESS 7	B24	IR2 (Interrupt 2)
A25	ADDRESS 6	B25	IR1 (interrupt 1)
A26	ADDRESS 5	B26	No connection (bussed)
A27	ADDRESS 4	B27	RFSH (refreshing)
A28	ADDRESS 3	B28	ALE (address latch)
A29	ADDRESS 2	B29	+5 V power
A30	ADDRESS 1	B30	OSC (15-MHz clock)
A31	ADDRESS 0 (LSB)	B31	GROUND

2.7.1 Expansion Bus Signal Descriptions

* NMI-. The non-maskable interrupt signal is driven by one of the expansion boards to interrupt the system processor. Its normal use is to indicate a system parity error condition. This line is pulled low by an open collector large-scale integration (LSI) device when driven by an expansion board.

* DATA 0-7. These bidirectional signals carry the data between the processor, memory, I/O, and the expansion interface. These lines are active high. They can be tri-stated by use of the DMA- line.

* WAIT-. This signal indicates when a device in the system or expansion bus is to hold or is holding the system processor in order to extend the length of a memory refresh or I/O cycle. When a slow device is addressed on the expansion bus, the signal can assert this line low in order to extend the time to complete a cycle. An expansion board, which takes over the bus, must monitor this line when accessing memory or I/O devices within the system. (This line should never be held low longer than 10 processor clock cycles.) This line is pulled low by an open collector, LSI device when driven by an expansion board.

* ADDRESS 0-19. These lines are normally driven by the system processor to address memory and I/O devices within the system. They can be tri-stated by use of the DMA- line. They can be driven by an expansion bus board by asserting the CPU ENABLE line low. These lines are active high. Only XA0 - XA9 are used for I/O addressing.

* RESET. This line resets or initializes system logic on power-up or during a power failure. This signal is active high. RESET is generated by a power supply monitoring device. During power brownouts or other times that the 12-V line drops below 11.1 V, the RESET line is activated immediately and returns low 3 ms after regulation has resumed. This will allow for unattended restarts.

* INTERRUPT 0-6. These lines signal the processor that an I/O device requires attention. In the event of several devices requiring service at the same time, the device asserting the lowest-numbered line gets serviced first. These lines are active high.

* DMA- (CPU enable). This line, when asserted low by an expansion board, causes the processor to give up the system busses and enter a wait state. This allows an expansion board to implement DMA or another processor. When asserting this line, the expansion board must wait until the system

busses are inactive (i.e., when MWRITE, MREAD, IOWRITE, IOREAD are all inactive). When deasserting CPU enable, the expansion board must first wait until the bus has been inactive for two processor clock cycles, assert the WAIT- line, deassert the CPU enable line, and continue to hold the WAIT- line for one additional clock cycle. This will allow the system processor to correctly execute its next bus cycle.

* AMWC- or MWRITE- The memory write signal is normally driven by the system processor. It indicates that the information on the data bus should be written to memory at the address given on the address bus. This signal is active low. It can be tri-stated by use of the DMA- line. This signal can be driven by an expansion bus board after the CPU enable line is asserted.

* MRDC- or MREAD- The memory read signal is normally driven by the system processor and indicates that the memory addressed by the address bus should be placed on the data bus. This signal is active low. It can be tri-stated by use of the DMA- line. This signal can be driven by an expansion bus board after the CPU enable line is asserted.

* AIOWC- or IOWRITE- The I/O write signal is normally driven by the system processor. It indicates that the I/O device addressed by the address bus should accept the data on the data bus. This signal is active low. It can be tri-stated by use of the DMA- line. This signal can be driven by an expansion bus board after the CPU enable line is asserted.

* IORC- or IOREAD- The I/O read line is normally driven by the system processor. It indicates that the I/O device addressed by the address bus should place its data on the data bus. This signal is active low. It can be tri-stated by use of the DMA- line.

* PCLK - processor clock. This is the system clock. It is a one-third division of the OSC clock and has a period of 200 ns (5.0 MHz). The clock has a duty cycle of 37.6 percent (+/-3.0 percent).

* RFSH or refreshing. This line indicates that a memory refresh cycle is taking place. It is positive true. When this signal is asserted all expansion bus activity is ignored.

* ALE - address latch. This line indicates when the processor is placing a valid address on the address bus. The address is valid on the falling edge of this signal. This signal cannot be tri-stated, and it should not be used by any device accessed by an expansion bus DMA controller.

* OSC (clock). This signal describes a high-speed clock with

a 66.7-ns period (15.0 MHz). It has a 50-percent duty cycle.

2.7.2 Expansion Bus Loading and Driving Requirements

The expansion bus is designed to drive five expansion boards. Each board may have no more than two LSI/TTL input loads on any one line of the bus. Open collector outputs, which drive the bus, should be able to sink 12 mA at 0.5 V. Data bus drivers should be able to sink 24 mA at 0.5 V and source 3 mA at 2.4 V and 15 mA at 2.0 V. Drivers for the interrupt lines IR0-IR6 should be able to source 1 mA at 3.5 V and sink 1 mA at 0.5 V. Drivers for the address and control bus in a DMA application should be able to sink 20 mA at 0.5 V and source 5 mA at 2.4 V.

2.7.3 Memory Timing on Expansion Bus

The memory bus cycles can be lengthened in integral multiples of the CLK cycle time (200 ns) by the use of the WAIT- line. Figure 2-4 provides the timing relationships of the expansion bus memory interface.

2.7.4 Direct Memory Access from Expansion Bus

The expansion bus interface has the minimum facility required to implement a form of direct memory access (DMA). This section describes some of the design requirements of an expansion board that would use this facility.

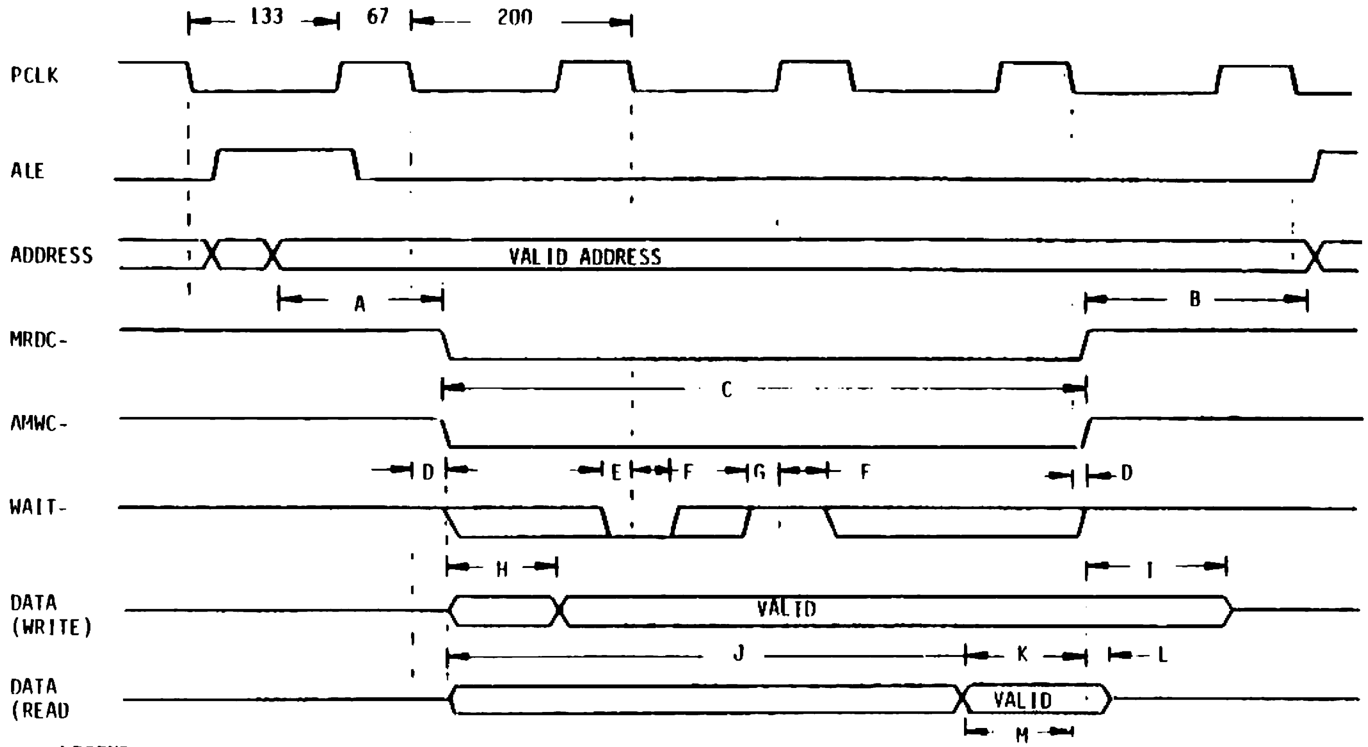
The DMA designed into the system can be used to access memory on the motherboard or standard option RAM board and any additional memory or I/O devices interfaced through the expansion bus. The DMA facility can not be used to access I/O devices located on the motherboard.

A board that implements DMA must simulate the processor with respect to the timing of input and output signals in order for the proper operation of the system. This implies specific phase relationships with the processor clock (PCLK) and the ability to recognize WAIT- signals from the memory or other peripherals.

The following discussion relates to the DMA timing diagram shown in Figure 2-5.

* PCLK: The 5.0-MHz processor clock has a 37.6-percent duty cycle. All signals are synchronous to this clock.

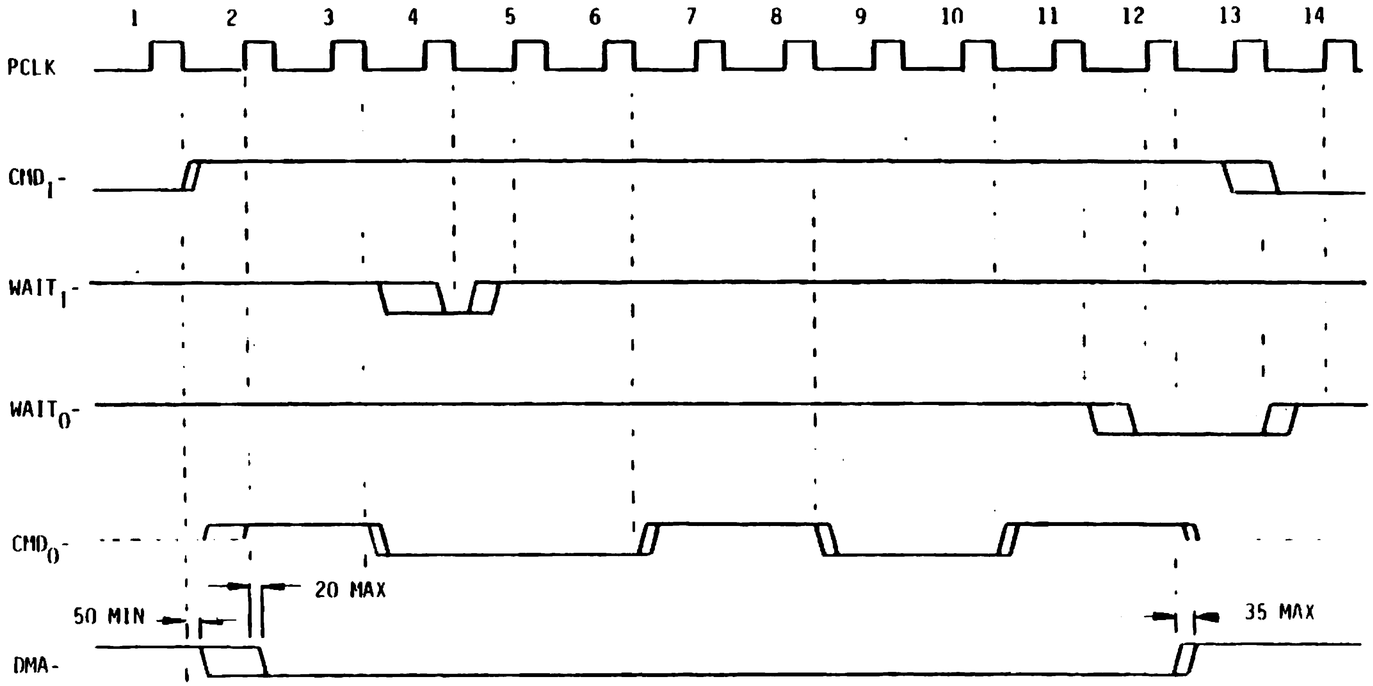
* CMDi-: Command input to the DMA controller. This signal is the logical "OR" of the expansion bus signals MRDC-, AMWC-, IORC-, and AIOWC-.



LEGEND:

A)	ADDRESS SETUP TO COMMAND	72 MIN		
B)	ADDRESS HOLD FROM COMMAND	176 MIN		
C)	COMMAND ACTIVE	575 MIN	375 MIN (WITHOUT WAIT STATE)	
D)	COMMAND DELAY FROM PCLK	35 MAX	10 MIN	
E)	WAIT - ACTIVE SETUP	40 MIN		
F)	WAIT - HOLD	0 MIN		
G)	WAIT - INACTIVE SETUP	50 MIN		
H)	DATA VALID AFTER AMWC - ACTIVE	120 MAX		
I)	DATA HOLD AFTER AMWC - INACTIVE	108 MIN		EXPANSION BUS
J)	REQUIRED ACCESS TIME FROM MRDC - INACTIVE	515 MAX	315 MAX	
K)	DATA SETUP TO MRDC - INACTIVE	77 MIN		MEMORY INTERFACE
L)	DATA HOLD FROM MRDC - INACTIVE	-4 MIN		
M)	DATA SETUP TO PCLK LOW	50 MIN		TIMING DIAGRAM

Figure 2-4 Expansion Bus Memory Interface Timing Diagram



$WAIT_I$-, $WAIT_0$-, CMD_0- MUST MEET THE SPECIFICATIONS SHOWN ON THE MEMORY INTERFACE AND I/O INTERFACE TIMING DIAGRAMS.

CMD_X- = ANY ONE OF THE BUS SIGNALS: AMWC-, MWRC-, IORC-, AIOWC-.

Figure 2-5 DMA Timing Diagram

* CMDo-: Command output from the DMA controller. This can be any one of the command signals to the expansion bus (MRDC-, AMWC-, IORC-, AIOWC-).

* WAITi-: The expansion bus WAIT- signal, which is monitored by the DMA controller during DMA command cycles to determine when to lengthen the command cycle.

* WAITo-: The expansion bus WAIT- signal as driven by the DMA controller at the end of a DMA sequence.

* DMA-: This line causes the expansion bus control signals (MRDC-, AMWC-, IORC-, AIOWC-), the address lines (A0-A19), and the CPU data bus lines (D0-D7) to go to the tristate mode and the processor to be put into a "WAIT" state.

To initiate a DMA sequence, the controller must monitor the bus for an end to all activity. The signal that shows the bus activity is CMDi-. The CMDi- signal is monitored until it goes inactive (HIGH). The DMA- signal is then set active on the bus. The DMA- signal must be set active within the interval from 50 ns after the falling edge of PCLK to 20 ns after the rising edge of PCLK in order to prevent glitches on the expansion bus command lines. The command out lines may be driven to the high state immediately on the activation of DMA-. The address lines from the DMA controller should not be driven until 30 ns after the DMA- line goes active in order to prevent bus collisions. In Figure 2-5 this sequence is shown in states 1 and 2.

For proper operation of memory and other devices, a minimum of two clock cycles must separate commands on the bus. Therefore, the DMA controller should not activate a command output until the second falling edge of PCLK after DMA- is made active. Figure 2-5 shows CMDo- going low after the falling edge of state 3.

Once a command is begun from the DMA controller, the controller must monitor the WAIT- input line for a possible wait state. This line should be latched on the falling edge of PCLK during CMDo- active. If it is inactive (high), the end of the command cycle is indicated If it is active (low), then the cycle should be extended by an additional PCLK period and the WAIT- should be monitored again. There is no hardware in the system that limits the number of wait states which could occur, but no peripheral or memory device is expected to insert more than ten wait states in any command cycle Two DMA cycles are shown in Figure 2-5. One cycle contains a wait state (t4, t5, t6) and one does not (t9, t10). Note that the successive cycles are two PCLK cycles apart.

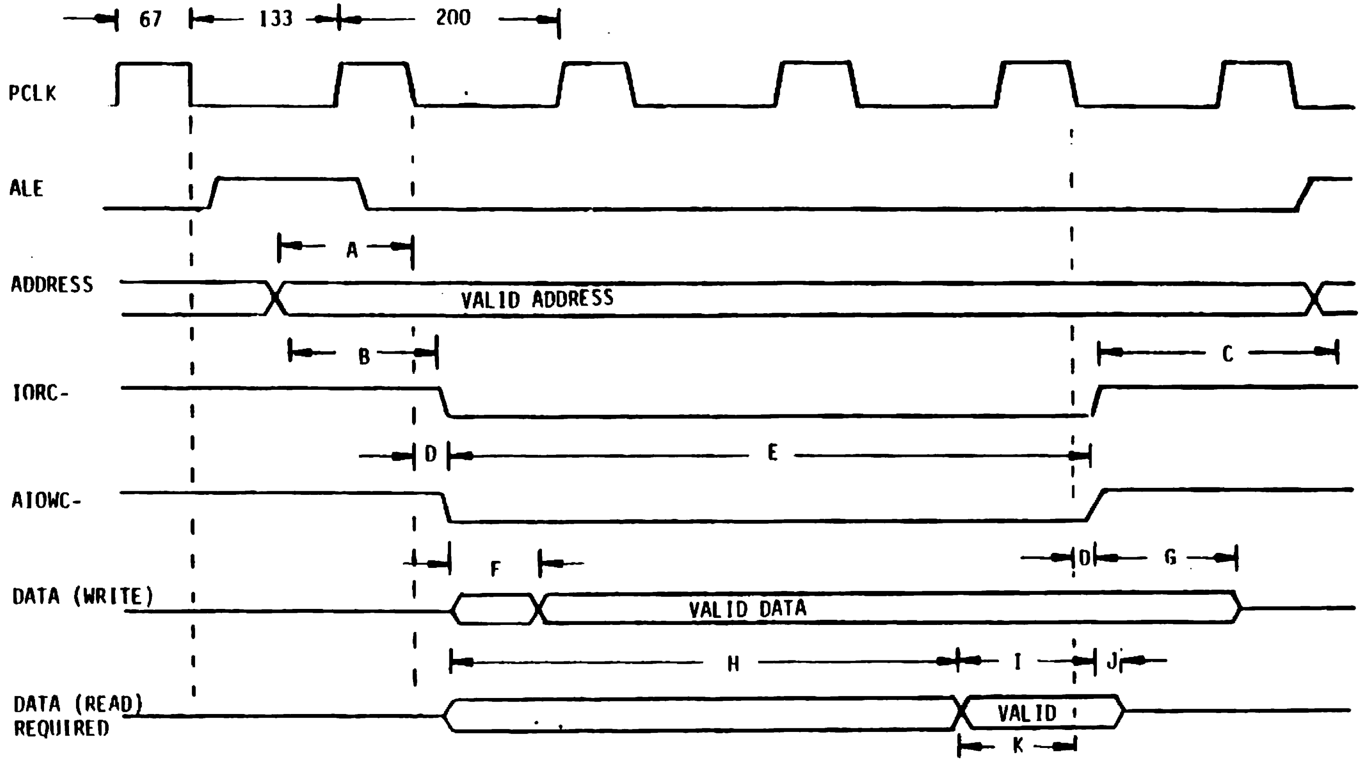
When the DMA controller is ready to give up the bus, it should assert the WAIT- line itself on the falling edge of PCLK after the last command cycle. On the next rising edge of PCLK, the DMA- line should be made inactive and the control and address lines from the DMA controller should be tristated. The tristate action should occur within 30 ns after the DMA- line is made inactive. The WAIT- line should be made inactive on the second falling edge of PCLK after it is made active. This will ensure that the first command cycle of the CPU is at least two full PCLK cycles long. Figure 2-5 shows this sequence in states 11 to 14.

Memory refresh occurs transparently through a controller that meets the above requirements. The number of consecutive DMA command cycles which can be run is not limited except by the system software requirements.

It may be desirable for a DMA controller to provide 4.7-kohm pull-up resistors on the bus command lines if the tristate action does not overlap in order to prevent glitches on those lines. Pull-ups should not be required on the address or data lines, as these do not affect logic states without the command lines. Note that the address and data setup and hold times for the controller should meet or exceed the specifications for the expansion bus running under the processor even if the DMA sequence must be padded with extra clock cycles to accomplish this.

2.7.5 I/O Timing On Expansion Bus

The following information is provided to show the expansion bus timing for standard I/O cycles. Note that this timing includes the one wait state that the motherboard always includes on I/O cycles The system bus I/O timing relationships are shown in Figure 2-6.



LEGEND:

A)	ADDRESS SETUP TO PCLK LOW	62 MIN	
B)	ADDRESS SETUP TO AIWOC- OR IORC-	72 MIN	
C)	ADDRESS HOLD AFTER AIOWC- OR IORC-	176 MIN	
D)	COMMAND DELAY FROM PCLK	35 MAX	10 MIN
E)	ACTIVE IORC- OR AIORC- TIME	575 MIN	
F)	DATA VALID FROM AIOWC- LOW	120 MAX	
G)	DATA HOLD AFTER AIOWC- HIGH	108 MIN	
H)	REQUIRED ACCESS TIME FOR IORC-	515 MAX	
I)	REQUIRED DATA SETUP TO RISING EDGE OF IORC-	85 MIN	
J)	REQUIRED DATA HOLD AFTER RISING EDGE OR IORC-	-4 MIN	
K)	REQUIRED DATA SETUP TO PCLK LOW	50 MAX	

Figure 2-6 Expansion Bus I/O Interface Timing Diagram

2.8 FLOPPY DISK CONTROLLER SUBSYSTEM Sh#4 Dwg #2223005

The floppy disk controller subsystem consists of a floppy disk controller IC (FD1793-02), a floppy disk support logic IC (WD1691), and a pulse delay IC (WD2143), all of which are made by Western Digital. It also has a voltage-controlled oscillator (VCO), one-half of a 74LS221 one-shot, two 2114 static RAMs used as a sector buffer and addressed by a CMOS 4040 counter, a programmable array logic (PAL) IC used for decoding and control operations, and miscellaneous logic used for the timing and buffering of signals.

The subsystem consists of several sub-subsections, including:

* The disk controller IC
* The sector buffer
* The data write precompensation circuit
* The data separator
* The floppy drive (or diskette drive) cable interface.

2.8.1 Floppy Disk Controller

The floppy disk controller (FDC) is the FD1793-02 chip. This IC is responsible for serial/parallel data conversion, locating sectors on the disk, seeking the diskette drive, and other high-level functions. A complete description of the FD1793-02 chip can be found in the literature available from Western Digital. The input clock to the controller is at 1.0 MHz to provide the correct data rate for standard 5-1/4-in diskettes. Since the clock is divided down from 15.0 MHz in U20, the duty cycle is 467 ns low, 533 ns high.

2.8.2 Sector Buffer

Data transmitted from or to the diskette drive during a read or write operation must occur as fast as 23 us per byte or 32 us per byte nominal for double-density operation. In order to allow proper operation of the diskette drive while other processor operations are occuring, a sector buffer that can operate independently of the processor for the duration of a sector read or write is implemented This buffer consists of a 1 kbyte x 8 static RAM (2 x 2114), a counter to address the RAM sequentially, and control logic and a bus buffer to allow the CPU and the FDC to access the buffer.

2.8.2.1 Sector Buffer Modes. The buffer has four basic operating modes controlled by two bits (M0, M1) in the latch U47. These modes are as follows:

LATCH U47 BITS M1	M0	MODE OR FUNCTION
1	1	FDC reads RAM and writes data to diskette.
1	0	FDC reads diskette and writes data to RAM.
0	0	CPU reads or writes RAM sequentially.
0	1	CPU reads or writes the FDC directly.

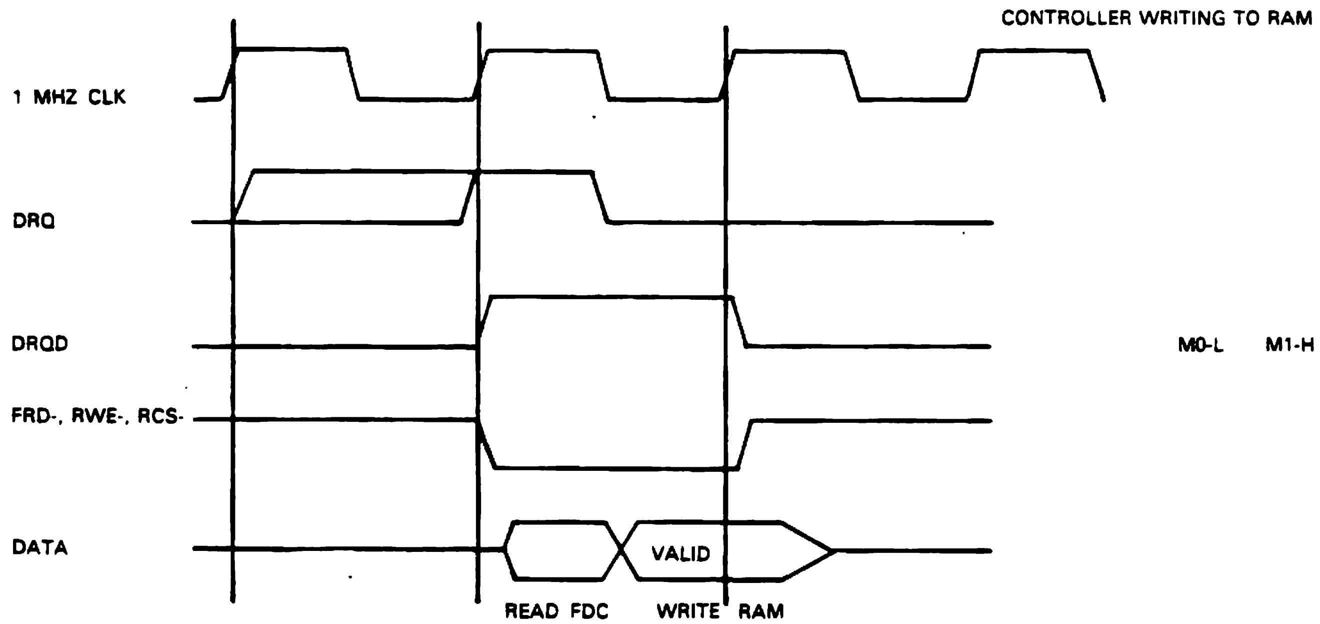
The counter that addresses the buffer is automatically incremented after each access of the RAM by either the CPU or FDC. The CPU can reset the address counter to set up a fixed starting address within the RAM by writing to the FDC sector register while the M1, M0 bits are set to 0,0. This does not affect the FDC itself, because the FDC can be accessed by the CPU only in mode 0,1.

The control logic for the sector buffer is provided by the PAL and by a flip-flop, which is used to provide a 1-us FDC clock-synchronized signal derived from the FDC data request (DRQ) line. This signal is used by the PAL to generate the read or write command for the FDC when the sector buffer is in modes 1,1 or 1,0. The DRQ line from the FDC is made active by the FDC whenever a byte is required in a sector write or when a byte is ready during a sector read.

Other signals to control the RAM and the counter are derived from this logic and the CPU signals as given in Table 2-9. The timing diagram shown in Figure 2-7 defines the usage of these signals. Note that the outputs go low (L) when the AND of terms on a line and the OR of the terms on a second line are true.

Table 2-9 Programming for the HAL10L8 Device

Output:	IORQ-	XA1	XA0	M1	M0	DRQD	IORC-	AIOWC-	FLCS	DEN-	COMMENT	
YA0	.	.	L	L	H	.	.	.	L	.	CPU <---> FDC	MODE 0,1
or	.	.	.	.	.	.	L	L	.	.	unused	
YA1	.	L	.	L	H	.	.	.	L	.	CPU <---> FDC	MODE 0,1
or	.	.	.	.	.	.	L	L	.	.	unused	
FRD-	.	.	.	L	H	.	L	.	L	.	CPU <-- FDC	MODE 0,1
or	.	.	.	H	L	H	.	.	.	.	FDC --> RAM	MODE 1,0
FWR-	.	.	.	L	H	.	.	L	L	.	CPU --> FDC	MODE 0,1
or	.	.	.	H	H	H	.	.	.	.	FDC <-- RAM	MODE 1,1
RWE-	.	L	.	L	L	.	.	L	L	.	CPU --> RAM	MODE 0,0
or	.	.	.	H	L	H	.	.	.	.	FDC --> RAM	MODE 1,0
RCS-	L	L	.	L	L	.	.	.	L	.	CPU <--> RAM	MODE 0,0
or	.	.	.	H	.	H	.	.	.	.	FDC <--> RAM	MODE 1,X
RRST-	.	H	L	L	L	.	.	L	L	.	RESET COUNTER	MODE 0,0
or	.	.	.	.	.	.	L	L	.	.	unused	
FDEN-	L	L	.	L	L	.	.	.	L	.	CPU <--> RAM	MODE 0,0
or	.	.	.	L	H	.	.	.	L	L	CPU <--> FDC	MODE 0,1



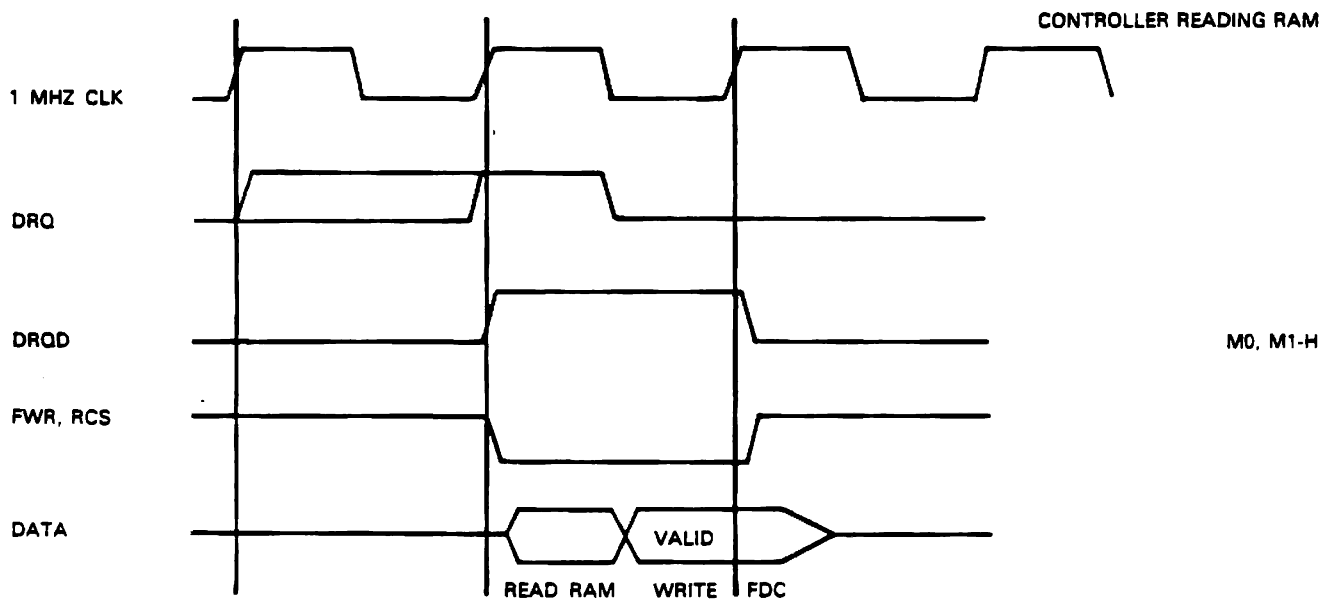


Figure 2-7 Floppy Disk Timing Diagrams

2.8.3 Floppy Disk Controller Write Precompensation

Disk write precompensation is required when writing double-density data using modified frequency modulation (MFM) in order to reduce the "bit shift", which results when certain data patterns are written on the magnetic media. Unless the bit shift is compensated for, it moves the read data transitions outside of the range where the read circuitry can properly detect them. The bit shift problem gets progressively worse as data bits are stored closer together on the disk (as track length gets shorter toward the center of the disk). The ideal situation is to adjust the write hardware gradually to compensate for the bit shift as the track number increases. However, a compromise solution provides results that are nearly as good. The method used is to leave all compensation turned off while the head is over the outer half of the disk. When the head is over the inner half of the disk, a compromise precompensation is turned on. As the number of tracks on a disk drive could be either 40 or 80, the choice of the halfway point is left up to software (which checks for the type of drive installed). This is why the TG43 signal is controlled by U47, not the FDC. (TG43 - Track Greater than 43 - is historically the halfway point for an 8-in diskette drive.)

The amount of precompensating bit shift is controlled by the adjustment of R19, which controls the write pulsewidth through U15, the WD2143 IC. The precompensation should be set at about 200 ns while monitoring pin 1 of the WD2143 IC during a write operation.

The direction of bit shift is controlled by the FDC signals EARLY and LATE. These signals cause the WD1691 to select the tap along the WD2143 (adjustable delay line), which is appropriate for the bit pattern being written. If precompensation is not needed on outer tracks, the TG43 signal inhibits the precompensation process.

Because single-density frequency modulation (FM) encoded data does not require precompensation, the FD1691 also disables the precompensation when the double density signal (DDEN-) is inactive (high).

2.8.4 Data Separator

The data separator is comprised of two parts: clock recovery and separation of the data from the clock. The actual separation of data and clock signals takes place in the FD1793-03 FDC. The 1691 contains the digital circuits necessary to implement a phase-locked loop (PLL) with the 74LS628 chip providing the VCO and the external components providing the loop filter. The one-shot U29 is used to shorten and stabilize the pulsewidth of the incoming read pulses so that the PLL and data recovery operations operate properly during the lockup interval.

The purpose of the PLL is to provide a continuous clock locked in a specific phase relationship with transitions in the incoming data. For this system the falling edge of the RDDATA- signal should be nearly centered on the high or low pulse of the RCLK signal.

When the adjustments are made correctly the PLL should be able to lock up to an incoming pulse train with a range of frequencies from 217 kHz to 294 kHz (+/-15 percent) within 150 us. The pulses should be low going (2 us maximum applied to the RDDATA- input - P9 pin 30) and the DDEN- line must be low.

Because of the analog nature of the PLL circuits, the power supply voltage to the VCO and the loop filter is regulated with a linear regulator. The regulator prevents any digital noise present on the 5-V supply from interfering with the operation of the PLL.

Note that the data separator is capable of working with either single-density (FM) or double-density (MFM) data, and the choice is controlled by the DDEN- line.

2.8.5 Floppy Disk Controller Alignment

To adjust the write precompensation and data separator circuits, perform the following steps.

NOTE

> Alignment of the floppy disk controller requires access to potentiometers and locations on the system unit board normally located underneath the left diskette drive and, therefore, inaccessible without partial disassembly of the system unit. Before attempting to align this circuitry, the system unit board must be either partially or completely removed from the system unit chassis. Extreme caution must be used to prevent the system unit board from contacting the chassis during alignment.

1. Insert a diagnostics diskette in the left drive and close the door.

2. Place the system unit ON/OFF switch in the ON position. Following the power-up self-test, the diagnostics menu is displayed.

3. Monitor the RDDATA- line at pin 11 of U14 to make certain it is inactive (high). If the diskette drive read logic is permitting noise, or extraneous low level on the RDDATA-

line, it may be necessary to disconnect the plug attached to J9 (the diskette drive control/data connector cable) on the system unit board (motherboard). With RDDATA- high, the PU and PD- outputs from the WD1691 are forced to a tristate condition.

4. The voltage on the PUMP line must be checked and adjusted to 1.4 Vdc. Attach a digital VOM with a high (greater than 5 megohms) input impedance to pin 13 or 14 (they are tied together) of U14 (WD1691). Adjust R17 for 1.4 Vdc, +/- 5 percent (between 1.33 and 1.47 Vdc)

5. The VCO line must now be checked for accuracy. Attach a 30-mHz (or higher) oscilloscope to pin 16 of U14 (WD1691). Use a 10X probe, internal trigger, 0.2-Vdc/Div. vertical, 0.1-us/Div. timebase. Adjust R18 for a square wave of 2.0-mHz +/- 5 percent (between 1.90 and 2.10 mHz).

6. Recheck the 1.4-Vdc reading at pin 13 or 14 to make certain that adjustment of R18 did not cause a change. Readjust if necessary.

7. The advanced diagnostics must be entered by pressing both the CTRL and A keys at the same time.

8. The drive alignment test must performed by selecting KEYBOARD, then key in:

   FLOTST TEST=ALIGN DRIVE=(enter 1,2,3, or 4)

9. Remove the diagnostics diskette and insert a blank, or "scratch", diskette into the appropriate diskette drive.

10. Turn on write data by keying in menu selection W.

11. Turn on write precompensation by keying in menu selection P.

12. Attach a 10X oscilloscope probe to U14 pin 5. Trigger positive slope, 0.2-Vdc/Div. vertical, 0.1-us/Div. timebase. The waveform is visible only when the computer is writing data to a diskette. Adjust R19 for a positive pulsewidth of 750 ns. This adjustment results in a write pulsewidth of 187.5 ns.

NOTE

If R19 is set to near its maximum value, the write pulsewidth will be very long (the length of an entire sector write). Adjustment of R19 must only be made when appropriate test equipment is monitoring the pulsewidth.

2.8.6 Diskette Drive Interface

The diskette drives are interfaced through a series of buffers and receivers that allow the use of low-impedance ribbon cables to connect the signals from controller to drive. This system implements two connectors for the drives. All signals driven by the controller except for the SID1- signal have separate drivers for each connector. The receivers with their terminating pull-up resistors are shared between the two connectors.

The connector P9 is designed to interface to a 34-conductor ribbon cable that has two, 34-pin, card-edge connectors, one for each of two diskette drives mounted inside the system unit chassis. Since there is always one diskette drive installed in the system unit, it is normally mounted on the left side (as viewed by a user). This drive should be strapped for SELECT on pin 10 (drive 0). The select line and all common lines except pin 32 (side select) should be terminated at this drive.

The other drive in the box (if present) should be strapped for SELECT on pin 12 (drive 1) with only the select line terminated. When two drives are installed, a terminating resistor must be installed on the right-hand drive (drive 1) only.

NOTE

> The floppy disk controller and individual diskette drive logic signals assign drives using the convention of: DRIVE ZERO, DRIVE 1, DRIVE 2, and DRIVE 3 (for a four-drive system). The diagnostics diskette uses a different convention: DRIVE 1, DRIVE 2, DRIVE 3, and DRIVE 4 for a four-drive system. Operating systems may use yet another convention, such as DRIVE A, DRIVE B, DRIVE C, and DRIVE D. Care must be used to avoid using the incorrect drive designator.

The second connector on the main printed wiring board (PWB) P13 is designed to interface to a 40-wire ribbon cable terminated with a 37-pin, D-type connector (which may be installed by the user) mounted on the back panel of the chassis. All lines used must be terminated in the external diskette drives.

If additional diskette drives are planned, all diskette drives must be of the same type. That is, all must be either 320-kbyte drives (double-sided, 48 tracks per inch (tpi)) or all must be 640-kbyte drives (double-sided, 96 tpi). A jumper on E1 to E2 selects 320-kbyte drives. No jumper selects 160-kbyte drives. A jumper on E3 to E4 selects 640-kbyte drives. A jumper may be on either E1-E2 or E3-E4, but not both.

The drives should all be strapped for head load with motor on if they are equipped with head load solenoids. Head load solenoids are not needed for proper operation of the diskette drives.

The signals STEP, DIRC, WG, and WDOUT are buffered by the 74LS244 in order to drive the two standard 7416 loads. This buffer is necessary because the 1793 and 1691 are capable of driving only one TTL load. The input signals WRITEPROT-, INDEX-, TRK00-, and RDDATA- are buffered by the 74LS244 to provide a small amount of hysteresis and more static protection than the MOS-device inputs provide.

The pin-outs for the internal and external diskette drive connectors on the motherboard are given in Table 2-10 and Table 2-11, respectively.

Table 2-10 Internal Diskette Drive Connector Pin-out

SIGNAL	RETURN	SIGNAL NAME	SOURCE	FUNCTION
2	1		NC*	
4	3		NC	
6	5		NC	
8	7	INDEX-	DRIVE	Indicates index hole
10	9	SELECT 1-	SYSTEM	Drive select 1
12	11	SELECT 2-	SYSTEM	Drive select 2
14	13		NC	
16	15	MOTOR ON-	SYSTEM	Drive motors ON
18	17	DIRECTION-	SYSTEM	Step IN/OUT direction
20	19	STEP-	SYSTEM	Step IN/OUT command
22	21	WRITE DATA-	SYSTEM	Serial data to drive
24	23	WRITE GATE-	SYSTEM	Enables writing to drive when low
26	25	TRACK 00-	DRIVE	Indicates head is over track 00 when low
28	27	WRITE PROT-	DRIVE	Indicates diskette is write-protected
30	29	READ DATA-	DRIVE	Serial data from drive
32	31	SIDE 1-	SYSTEM	Side select (0,1 = High, Low)
34	33		NC	

* NC means not connected

To connect external diskette drives, a short cable assembly with a 40-pin connector links J13 on the system unit board with a (recommended) 37-pin d-type connector on the back panel of the system unit. Table 2-11 gives the 40-pin J13 signals. D-type connector pin numbers are in parentheses ( ).

Table 2-11 External Diskette Drive Connector Pinout

SIGNAL	RETURN	SIGNAL NAME	SOURCE	FUNCTION
2 (1)	1(20)		NC*	
4 (2)	3(21)		NC	
6 (3)	5(22)		NC	
8 (4)	7(23)		NC	
10 (5)	9(24)		NC	
12 (6)	11(25)	INDEX-	DRIVE	Indicates index hole
14 (7)	13(26)	MOTOR 3-	SYSTEM	Drive motor 3 enable
16 (8)	15(27)	SELECT 4-	SYSTEM	Drive select 4
18 (9)	17(28)	SELECT 3-	SYSTEM	Drive select 3
20(10)	19(29)	MOTOR 4-	SYSTEM	Drive motor 4 enable
22(11)	21(30)	DIRECTION-	SYSTEM	Step IN/OUT direction
24(12)	23(31)	STEP-	SYSTEM	Step IN/OUT command
26(13)	25(32)	WRITE DATA-	SYSTEM	Serial data to drive
28(14)	27(33)	WRITE GATE-	SYSTEM	Enables write when low
30(15)	29(34)	TRACK 00-	DRIVE	Indicates head is over track 00 when low
32(16)	31(35)	WRITE PROT-	DRIVE	Indicates diskette is write-protected
34(17)	33(36)	READ DATA-	DRIVE	Serial data from drive
36(18)	35(37)	SIDE 1-	SYSTEM	Side select (0 = High)
38(19)	37		NC	
40	39		NC	

* NC means not connected

P1(KEYBOARD) The keyboard is a fairly simple subassembly. The keyboard electronics functions include:

* Scanning the key matrix
* Decoding new keys depressed by the operator
* Transmitting data to the system unit
* Receiving commands from the system unit
* Performing N-key rollover
* Implementing a software switchable repeat-action function
* Locking/unlocking the keyboard
* Performing a set of self-diagnostics

2.8.7 Encoding Keystrokes

The encoder detects valid keyswitch state changes, looks up the proper key code, and transmits the keycode as an 11-bit stream to the system unit. Each key causes either one or two bytes to be transmitted, based on the status of the SHIFT, ALT, CAPS LOCK, and CTRL keys. For specific details on the byte definitions, refer to Section 3, subsection 3.1, "Keyboard DSR."

2.8.8 Transmission

Transmission from the keyboard to the system unit is done at a rate of 2440 baud +/- 1.50 percent. The keyboard transmits when one of two conditions is met.

* When a valid key depression has been detected, or
* When a system command is understood and acted upon

In the case of a key depression, the proper keycode byte or bytes are sent across the keyboard transmit line in response to the user depression of a key. (Refer to Section 3, subsection 3.1, "Keyboard DSR," for details on keycodes.) In some cases repeat-action transmissions may also be required following key depression.

In the case of response to a system unit command, the keyboard transmits the proper response code to the system unit to indicate that the action required has been taken. System unit commands and keyboard responses are given in Table 2-12.

Table 2-12 Keyboard Commands and Responses

SYSTEM UNIT COMMAND	CODE (HEX)	KEYBOARD RESPONSE CODE (HEX)	MEANING
Perform a power-up self-test and install default parameters	00*	70	Self-Test OK
		71	Keyboard ROM error
		72	Keyboard RAM error
Turn typamatic ON	01*	70	
Turn typamatic OFF	02	70	
Lock keyboard	03	70	
Unlock keyboard	04*	70	
Keyclick ON	05**	70	
Keyclick OFF	06**	70	
Reset (same as 00)	07	70	Self-Test OK
		71	Keyboard ROM error
		72	Keyboard RAM error
Return Version	08	70, 73	(two-byte code)

* Indicates default parameters
** Keyclick requires hardware modification. It is not presently supported.

NOTE

In Table 2-12, the Code column gives the codes entered on the keyboard. The Keyboard Response Code column gives the code sent by the keyboard microprocessor. The keyboard responds to every valid command. Typically, the self-test "OK" code 70 is returned to the system unit (except in the case of a failure during self-test). If the system unit command is ignored (for reasons such as parity error, unknown command, start bit error, or other error), a response code is not returned. In such a case, the system unit retries the command.

2.8.9 Power

The keyboard connection includes a 12-Vdc line. This line is locally regulated on the keyboard to 5 Vdc (to prevent voltage drops and electrostatic discharge (ESD) problems).

2.9 CRT CONTROLLER BOARD

The CRT controller board drives either a monochrome analog or a color TTL display. As a stand-alone option, the controller provides one page of high-resolution (80 columns x 25 lines) alphanumeric display. This board also provides the signals required by the addition of an optional, graphics video controller piggyback board. The addition of the board makes the Texas Instruments Professional Computer a complete alphanumerics and raster graphics system. No physical distinction exists between color and monochrome; the board provides both eight-level gray scale and eight-color RGB (Red, Green, Blue) outputs. Color is determined by the monitor used. Figure 2-8 shows a block diagram of the alphanumeric CRT controller board. Refer to Section 5, drawing 2223011, for logic diagrams.

2.9.1 Display Characteristics

The display characteristics are as follows;

* A 7 x 9 character in a 9 x 12 cell
* Twenty-five lines of 80 characters
* A resolution of 720 pixels horizontally x 300 pixels vertically
* A horizontal scan rate of 19 200 lines per second
* A vertical scan rate of 60 (50 frames per second)
* A dot rate of 18.0000 MHz

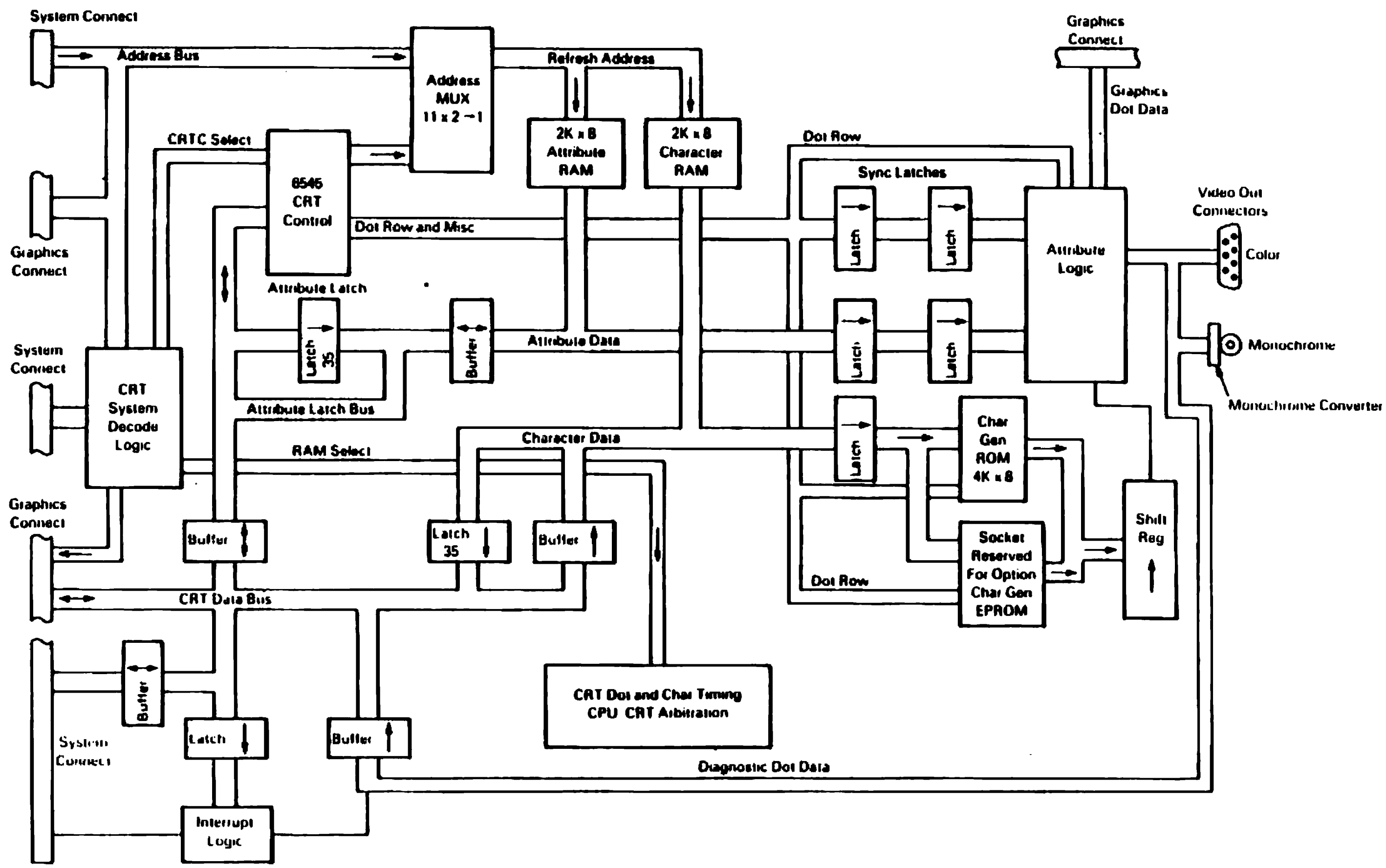


Figure 2-8 Alphanumeric CRT Controller Board Block Diagram

2.9.2 Attributes

The controller's video memory is organized as 2 kbytes x 16 bits. The first eight bits convey character information. The second eight bits select the following attributes on a character basis:

* Bit 0, Intensity Level 1 (BLUE)
* Bit 1, Intensity Level 2 (RED)
* Bit 2, Intensity Level 4 (GREEN)
* Bit 3, Character Enable
* Bit 4, Reverse
* Bit 5, Underline
* Bit 6, Blink
* Bit 7, Alternate character set

NOTE

The three intensity bits (bit 0 through bit 2) determine the gray scale intensity level and the RGB outputs for color. Thus, hi/norm video in monochrome is handled by a one-of-eight intensity select instead of a high-intensity bit.

To access the attributes, the software writes an attribute latch with the value of the attribute for all characters subsequently written to the screen as long as no screen read is done.

When any character on the screen is read, its attributes are copied to the attribute latch where they are read by a subsequent latch read operation.

This method of handling the attributes allows the software to do "block moves" of screen data from one screen area to another with the attributes of each character moving with the character.

2.9.3 Character Sets

The video controller contains a 4K character generator ROM, which provides for 256 characters. A socket is provided to allow for optional 2K or 4K ROM/EPROM, which can expand the character set to a maximum of 512 characters. Attribute bit 7 selects the expanded character set.

2.9.4 Cursor

The cursor can be programmed to be blinking or non-blinking, reverse-video block or underlined. The display of the cursor is handled by the hardware through a special set of registers in the controller. These registers allow the software to position the cursor anywhere on the screen (or off the screen if no visible cursor is desired).

2.9.5 Scrolling

The hardware supports character line scrolling in four directions by maintaining a "screen start" register. When the software determines a need for a scroll, it changes the value of this register by one line, causing the screen to appear to jump by one line. The scrolling operation always affects all of the screen, that is, it is not possible to scroll one region without affecting another.

Since the controller is equipped with only 2 kbytes of screen memory, scrolling results in a "wrap" of the original top line of screen contents to the bottom of the screen. Therefore, the software is required to clear the top line of the screen (or bottom) before the scroll-up (or -down) operation. To simplify programming of the line clear operation, the 2 kbytes of memory is phantomed over a 4-kbyte address space.

When a status line is implemented, it must be done in software. That is, during scroll operations, the status line must be moved to its new position in memory before the screen-to-memory correspondence is changed by writing the "screen start" register.

2.9.6 Video Connector

The video connector located on the rear edge of the printed circuit board is a standard, 9-pin, female, D-type connector. The signals available on this connector are given in Table 2-13. All signals are at standard TTL levels.

Table 2-13 Color Video Connector Pin-out

PIN	FUNCTION
1	Ground
2	Logic ground
3	RED video
4	GREEN video
5	BLUE video
6	Logic Ground
7	NC (no connection)
8	Horizontal drive (NEGATIVE TRUE)
9	Vertical drive (POSITIVE TRUE)

The alphanumeric-CRT controller board contains the following subsystems.

* CRT controller (CRTC) IC
* Memory/screen arbitration logic
* Memory address decode logic
* Character sets and attribute logic
* Processor interrupt logic

2.9.7 CRT Controller IC (6545A-1)

The CRTC IC(6545A-1) provides the logic to generate the horizontal and vertical synchronizing signals, display blanking during retrace, screen memory addressing during screen refresh, cursor coincidence logic, and start of screen display registers for use in scrolling.

2.9.7.1 CRTC Programming. The CRTC contains seventeen registers that must be set up appropriately before operation of the board can begin. To access these registers, the CPU must first write the address of the register to be accessed into the CRTC address register. When writing to or reading (where appropriate) the data register, the information is accessed according to the address latched in the address register.

The values given in Table 2-14 assume a character rate (SWM-) of 2.0 mHz, 12 lines per character block, 25 rows on the screen, 24 character times of horizontal blanking (12.0 us), 20 line times of vertical blanking (1.04 ms) for a 60-Hz refresh rate. When a 50-Hz refresh rate is used, the second set of values apply.

Table 2-14 CRTC Programming Values

CS-	RS	R/W-	ADD	REGISTER NAME	VALUE 60 Hz	VALUE 50 Hz
H	X	X	X	Not selected		
L	L	L	X	Address register		
L	L	H	X	Status register		
L	H	L	0	Horizontal total chars-1	103	103
L	H	L	1	Horizontal displayed chars	80	80
L	H	L	2	Horizontal sync position	84	84
L	H	L	3	VSYNC width, HSYNC width	39H	39H
L	H	L	4	Vertical total rows-1	24	25
L	H	L	5	Vertical adjust lines	20	20
L	H	L	6	Vertical displayed rows	25	25
L	H	L	7	Vertical sync position	25	25
L	H	L	8	Mode control	00H	00H
L	H	L	9	Scan lines per row-1	11	13
L	H	L	10	Cursor start line and BLINK	40H	40H
L	H	L	11	Cursor end line	11	13
L	H	L	12	Display start address HIGH	00H	00H
L	H	L	13	Display start address LOW	00H	00H
L	H	X	14	Cursor position address HIGH	00H	00H
L	H	X	15	Cursor position address LOW	00H	00H
L	H	H	16	Light pen position add HIGH		
L	H	H	17	Light pen position add LOW		

2.9.8 CRT Screen/CPU Arbitration

The CRT controller arbitration logic is designed to allow the programmer to have free access to the CRT screen with little overhead time caused by arbitration conflicts. To achieve this end, the refresh memory and its control logic are designed to allow for two complete memory cycles between each character displayed on the screen. One cycle accesses the character for display, the other is available to the CPU for read or write operations. In this way, the CPU must wait at most less than two display character times for access to the memory. Since a character time is 500.8 ns and the CPU clock is 200 ns, a synchronization delay may also occur. The total time for a worst-case CPU access would be 1.0 us with the usual access time being 600 ns (3 to 0 wait states).

The logic that generates this arbitration scheme is implemented with a counter (which also counts the 9 dots per character) and a programmable array logic (PAL) having internal registers and feedback from the outputs. These parts are used to implement a small alphanumerics state machine that provides the control outputs for the RAM and buffer control and the wait state control for the CPU. The counter identifies the state within the display cycle of the state machine by inputs to the PAL. The internal PAL registers define other states used during the CPU read and write cycles. The other inputs to the PAL are RD-, WR-, CSEL-(character select), ATSEL-(attribute select). These inputs define what type of cycle the CPU is executing.

The outputs from the PAL are COE- and CWE-, the RAM output enable and write enable control; AEN-, the attribute bus buffer enable; AOE-, the attribute latch output enable; ACK-, the attribute latch clock; MIE-, the character bus input buffer enable; SWM-, the signal that switches the RAM address multiplexer from the CRTC to the CPU; and WAIT-, the CPU wait control line.

The states that the counter goes through are 8, 9, 10, 11, 12, 13, 14, 15, 0, and repeat.

The window, when read data from the video RAM is available, is rather short. Therefore, a latch(U10) is included to capture and hold the data for the CPU until the end of the CPU read cycle. This latch is clocked when read data is available from the RAM by the ACK line which also clocks the attribute latch. The output is enabled onto the local bus by a combination of CSEL- and RD-.

2.9.8.1 CRT Arbitration PAL. The CRT arbitration PAL programming is given in Table 2-15. In the comment column, the states that are generated by the AND of inputs are listed according to the counter state number. Note that the outputs go LOW when the AND of all the listed conditions on a line are true OR if the same is true on another line.

The timing produced by the alphanumerics state machine for typical cycles is shown in Figure 2-9.

Table 2-15 Alphanumerics State Machine PAL

Output:	X1	X2	X4	LD-	RD-	WR-	CSEL-	ATSEL-	SWMUX	MIE-	CWE-	COE-	AEN-	ACK-	AOE-	WAIT-	Comment
SWMUX	.	.	L	.	.	.	.	.	.	.	.	.	.	.	.	.	S8, 9, 10, 11, 12 X4 DELAYED
or	.	.	L	.	.	.	.	.	.	.	.	.	.	.	.	.	all other terms
MIE-	L	L	L	H	.	L	L	.	.	.	.	.	.	.	L	L	S9 RAM WRITE BEGINS
or	.	.	.	.	.	.	.	.	.	.	L	.	.	.	.	.	S10, 11, 12 RAM WRITE CONT.
or	.	.	.	.	.	.	.	.	.	.	L	.	.	.	.	.	all other terms
CWE-	L	L	L	H	.	L	L	.	.	.	.	.	.	.	L	L	S9 RAM WRITE BEGINS
or	H	L	L	H	.	L	L	.	.	.	L	.	.	.	.	.	S10 RAM WRITE CONTINUES
or	L	H	L	H	.	L	L	.	.	.	L	.	.	.	.	.	S11 RAM WRITE CONTINUES
or	.	.	H	L	.	.	.	.	.	.	.	.	.	.	.	.	all other terms inactive
COE-	.	.	H	.	.	.	.	.	.	.	.	.	.	.	.	.	S13, 14, 15, 0 SCREEN REFRESH
or	.	L	L	H	L	.	L	.	.	.	.	.	.	H	.	L	S9, 10 RAM READ
or	.	.	.	.	L	.	L	.	.	.	.	.	L	.	.	.	S10, 11, 12 RAM READ CONT.
or	.	.	H	L	.	.	.	.	.	.	.	.	.	.	.	.	all other terms inactive
AEN-	L	L	L	H	.	L	L	.	.	.	.	.	.	.	L	L	S9 RAM WRITE BEGIN
or	.	.	.	.	.	.	.	.	.	.	L	.	.	.	.	.	S10, 11, 12 RAM WRITE CONT.
or	.	L	L	H	L	.	L	.	.	.	.	.	.	H	.	L	S9, 10 RAM READ
or	.	H	L	H	L	.	L	.	.	.	.	.	L	.	.	.	S11, 12 RAM READ
or	.	.	H	L	.	.	.	.	.	.	.	.	.	.	.	.	all other terms inactive
ACK-	H	H	L	H	L	.	L	.	.	.	.	.	L	.	.	.	S12 RAM READ
or	L	.	.	.	.	L	.	L	.	.	.	.	.	.	.	.	WRITE ATTRIBUTE LATCH.
or	.	.	H	L	.	.	.	.	.	.	.	.	.	.	.	.	all other terms inactive
AOE-	L	L	L	L	.	L	L	.	.	.	.	.	.	.	H	L	S8 RAM WRITE
or	.	.	.	.	.	L	L	.	.	.	.	.	.	.	L	.	S9 till NOT WRITE.
or	.	.	.	.	L	.	.	L	.	.	.	.	.	.	.	.	READ ATTRIBUTE LATCH.
or	.	.	.	.	L	.	L	.	.	.	.	.	.	L	.	.	S13 til not read
or	.	.	.	.	L	.	L	.	.	.	.	.	.	.	L	.	S13 til not read
WAIT-	.	.	.	.	.	L	L	.	.	.	.	.	.	.	H	.	RAM WRITE BEFORE S9
or	.	.	.	.	L	.	L	.	.	.	.	.	H	H	.	.	RAM READ BEFORE S9
or	.	.	H	L	.	.	.	.	.	.	.	.	.	.	.	.	all other terms inactive

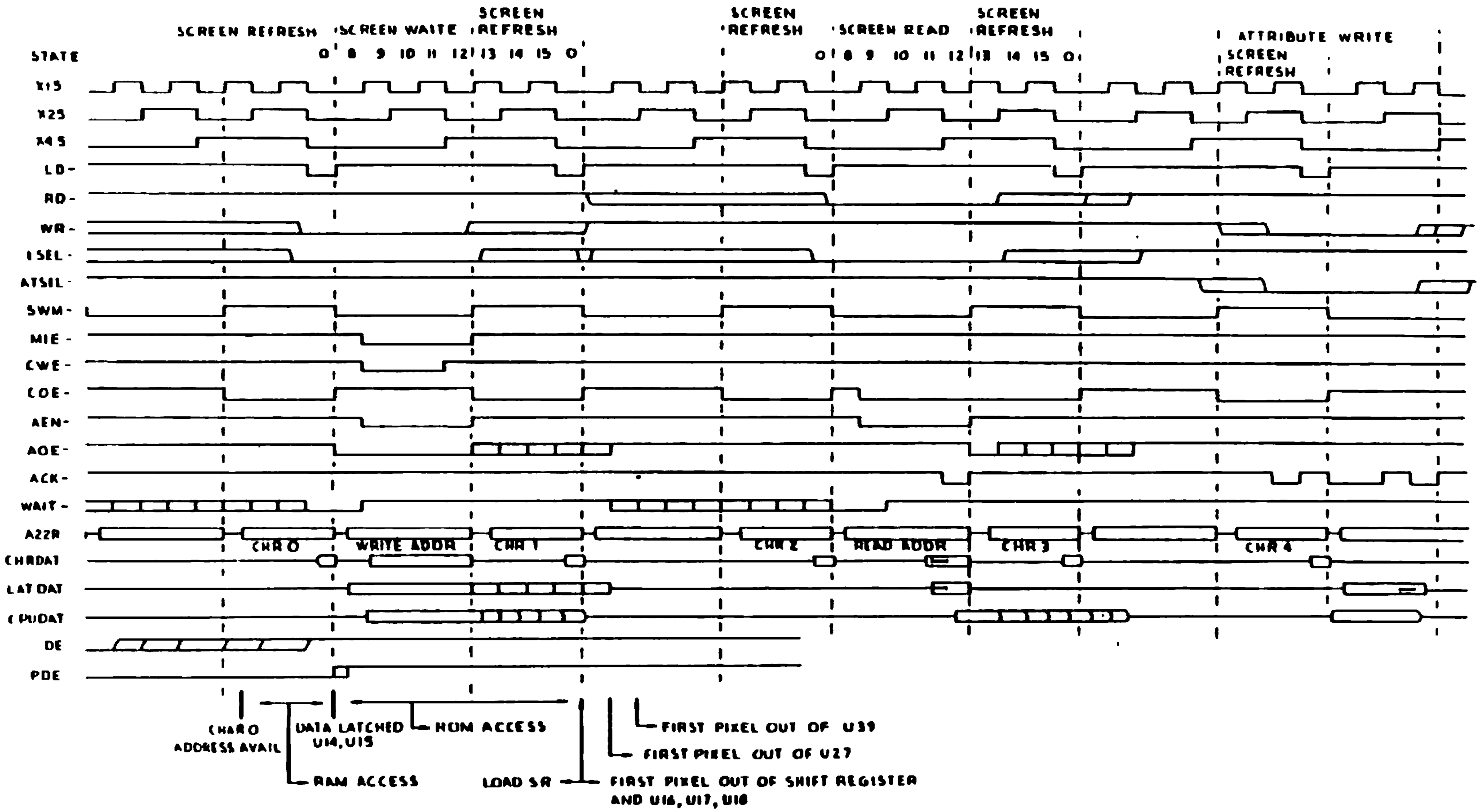


Figure 2-9 Alphanumerics State Machine Timing Diagram

2.9.9 CRT Address Decode

The address decode for the CRT subsystem, both alphanumerics and graphics, is handled by the CRT controller board. All of the screen data is mapped into the processor memory address space including the assorted latches and I/O ports.

The decoding is done within three ICs: a HAL10L8 PAL, one-half of a 74LS20, and a 74LS155 decoder. The PAL produces the following signals:

* RD-, a decoded and buffered read control.
* WR-, a buffered and decoded write control.
* ZBEN-, the master expansion bus buffer enable.
* XBEN-, the secondary bus buffer enable.
* CSEL-, the alphanumerics screen memory select.
* GSEL-, the graphics screen memory select.
* CR/AT-, a control signal that selects the half of the 74LS155 that decodes the CRTC and the attribute latch.
* XSEL-, a control signal that selects the half of the 74LS155 that decodes the graphics latches and miscellaneous input buffer.

The XBEN- signal also develops an enable clock for the CRTC by inverting and delaying the signal to provide the required setup time for the 6545a-1 CRTC (90 ns). The CRTE (CRT enable) signal has a pulsewidth of >266 ns, thus satisfying the requirement of the CRTC. The other setup and hold times are easily met.

The 74LS155 is used to decode the following signals: ATSEL-, the attribute latch select; CRTSEL-, the CRTC chip select; LAT-, a signal which when combined with WR- clocks the interrupt enable and screen enable latches. The other half of the 74LS155 decodes the three graphics board latches and the buffer enable for miscellaneous inputs. The address space that each of these devices occupies is shown in Table 2-16.

Table 2-16 CRT System Memory Map

ADDRESS		DEVICE
C0000-C7FFF		Graphics RAM Bank A
C8000-CFFFF		Graphics RAM Bank B
D0000-D7FFF		Graphics RAM Bank C
D8000-DDFFF		Unusable
DE000-DE7FF		Active character memory
DE800-DEFFF		Phantom character memory
DF000	bit 0	Misc input buffer, BLUE feedback, read only
DF000	bit 1	Misc input buffer, RED feedback, read only
DF000	bit 2	Misc input buffer, GREEN feedback, read only
DF000	bit 3	Misc input buffer, interrupt pending, read only
DF010		Graphics RED palette latch, write only
DF020		Graphics GRN palette latch, write only
DF030		Graphics BLU palette latch, write only
DF800		Attribute latch
DF810		CRTC address register, write only
DF811		CRTC status register, read only
DF812		CRTC registers write access, write only
DF813		CRTC registers read access, read only
DF820	bit 7	Misc output latch, interrupt enable
DF820	bit 6	Misc output latch, alphanumerics screen enable

PAL coding is given in Table 2-17. Note that the output is LOW when the AND of all the conditions on a line is true OR when the conditions on a second line are true.

Table 2-17 Alphanumeric Decoding PAL

Output:	MRDC-	AMWRC-	A1516-	A19	A18	A17	A14	A13	A12	A11	COMMENT
ZBEN-	L	.	.	H	H	L	.	.	.	.	CRT SPACE READ
or	.	L	.	H	H	L	.	.	.	.	CRT SPACE WRITE
XBEN-	L	.	L	H	H	L	H	H	H	H	CRTC/ATT READ
or	.	L	L	H	H	L	H	H	H	H	CRTC/ATT WRITE
RD-	L	.	.	H	H	L	.	.	.	.	CRT SPACE READ
or	L	L	.	.	.	.	.	.	.	.	inactive term
WR-	.	L	.	H	H	L	.	.	.	.	CRT SPACE WRITE
or	L	L	.	.	.	.	.	.	.	.	inactive term
GSEL-	.	.	H	H	H	L	.	.	.	.	GRAPHIC ACCESS
or	L	L	.	.	.	.	.	.	.	.	inactive term
CSEL-	.	.	L	H	H	L	H	H	L	.	CHARACTER ACCESS
or	L	L	.	.	.	.	.	.	.	.	inactive term
CR/AT-	.	.	L	H	H	L	H	H	H	H	CRTC/ATT ACCESS
or	L	L	.	.	.	.	.	.	.	.	inactive term
XSEL-	.	L	L	H	H	L	H	H	H	L	EXTRA I/O WRITE
or	L	.	L	H	H	L	H	H	H	L	EXTRA I/O READ

2.9.10 Character Set and Attribute Logic

The output of the RAM (both character and attribute) is latched up at the end of each screen refresh access cycle by a pair of 74LS374s (U14, U15). This allows a full character cycle time (500.8 ns) to access the character ROM and EPROM and set up to the dot shift register. The required ROM access time is 452.8 ns. In order to allow the character set to include the ability for block graphics, bit 7 out of the ROMs is used to indicate that the leftmost and rightmost character dots are to be copied to the left and right character cell border dots. The character ROMs should be programmed with active low data, that is, if a dot is to appear, it should be programmed to a zero.

Figure 2-10 shows some sample characters. Note that the reverse video block and the cursor affect the entire 9 x 12 character cell, and that the underline appears on row 11. In order to allow a reasonable appearing underline, cursor, and reverse video, the lowercase letters with descenders should only drop one dot line below the level of the other characters.

```
                         COPIED WHEN BIT 7 IS LOW
                         +++         +++   +++         +++
                         ! !         ! !   ! !         ! !
                         ! 6 5 4 3 2 1 0 !   ! 6 5 4 3 2 1 0 !

     R0                  . . . . . . . . .   . . . . . . . . .
     R1                  . . X X X X X . .   . . . . . . . . .
     R2                  . X . . . . . X .   . . . . . . . . .
     R3                  . X . . . . X X .   . . X X X . X . .
     R4                  . X . . . X . X .   . X . . . X X . .
     R5                  . X . . X . . X .   . X . . . . X . .
     R6                  . X . X . . . X .   . X . . . . X . .
     R7                  . X X . . . . X .   . . X X X . X . .
     R8                  . X . . . . . X .   . . . . . . X . .
     R9                  . . X X X X X . .   . X . . . . X . .
     R10                 . . . . . . . . .   . . X X X X . . .
     R11 UNDERLINE       X X X X X X X X X   . . . . . . . . .
```

Figure 2-10 Sample Character Font Definition

2.9.10.1 Attribute Interaction. The attributes available for use with the character display can be used in any of the 128 possible combinations. The following paragraphs explain what happens when several attributes are active at once.

The attributes have a priority in their effects, and the highest priority attributes affect all attributes having a lower priority. The order of priority is as follows.

Highest	Color attributes - RED, BLUE, GREEN
	Reverse video and cursor
	Character enable
	Blink
Lowest	Underline

For example, when both the underline and blink attributes are set, both character and underline would blink. When the character enable is set to disable, no character or underline or blinking activity is present. When the reverse video is set with blink, the character goes on and off with the background lighted and the foreground dark blinking. When the character enable is set to disable and reverse video is set, the entire cell is lit (according to the color attributes).

The color attributes define the characteristics of the "light" portion of the character, that is, either the color (when a color monitor is used) or the intensity (when a monochrome monitor is used).

When the graphics board is used with the alpha board, the graphics screen "shows through" the "dark" portion of the alphanumeric character display.

2.9.10.2 Attribute Hardware. The attribute logic design is of the "pipeline" type because the activity of the attributes must occur with dot timing precision, which is within 55 ns. In order to get data from a latch through several levels of logic and setup into the next latch, some SCHOTTKY logic is used. The attribute data from the RAM latches is latched again by two 74S175s (U16, U17). This latching allows for the one character delay through the character ROM and provides tightly timed outputs to the logic. The cursor (CUR) and display enable (DE) lines are also delayed twice to keep them synchronous with the other information (U18).

Propagation delay through the logic could cause timing skews greater than a dot time, so the outputs of the first level of logic are re-latched one dot time later. After going through the second level of logic (MUX U20), they are latched again for presentation to the video outputs (U39 74S174).

The red, blue, and green outputs are buffered by a 74LS244 before being sent to the 9-pin connector. The color outputs and composite sync are buffered by a 74S00, which has an isolated power supply, and are combined by a resistor network and buffered by a transistor to make up the composite video output. The mapping of colors to intensity in the composite video output is shown in Table 2-18.

Table 2-18 Color Map

CODE	COLOR	COMPOSITE OUT (In Volts)
COMPOSITE SYNC		0.47
000	BLACK	0.78
001	BLUE	0.88
010	RED	0.97
011	MAGENTA	1.07
100	GREEN	1.18
101	CYAN	1.28
110	BROWN	1.37
111	WHITE	1.47

The alphanumerics display can be blanked to black by setting the CRT ENABLE bit in the miscellaneous output latch to a low. The board enters this state on power-up.

2.9.11 CRT Interrupt

The CRT controller board contains logic that allows it to generate an interrupt during the vertical interval. This interrupt is used by the processor when doing scrolls with a status line or other operations that need to be done during the vertical blanking interval. The interrupt is enabled by setting the interrupt enable bit in the miscellaneous latch to a high. When vertical blanking occurs, the CPU non-maskable interrupt is caused and the interrupt pending bit is set allowing it to be read from the miscellaneous buffer. To reset the interrupt, the interrupt enable bit must be set low.

2.9.12 Diagnostic Loopback

To assist in a low level of diagnostic capability, the three color outputs are looped back to the miscellaneous input buffer to allow them to be read by the CPU. By the use of programming involving careful timing from the vertical interval, the CPU can check the action of the attribute bits and graphic board palette circuits.

2.10 GRAPHICS VIDEO CONTROLLER BOARD

The graphics video controller board is designed to operate with the CRT controller board. It is physically mounted in a piggyback fashion on the CRT controller board and all its connections are to the CRT controller board. A block diagram of the graphics video controller board is shown in Figure 2-11. Refer to Section 5, drawing 2223063, for logic diagrams.

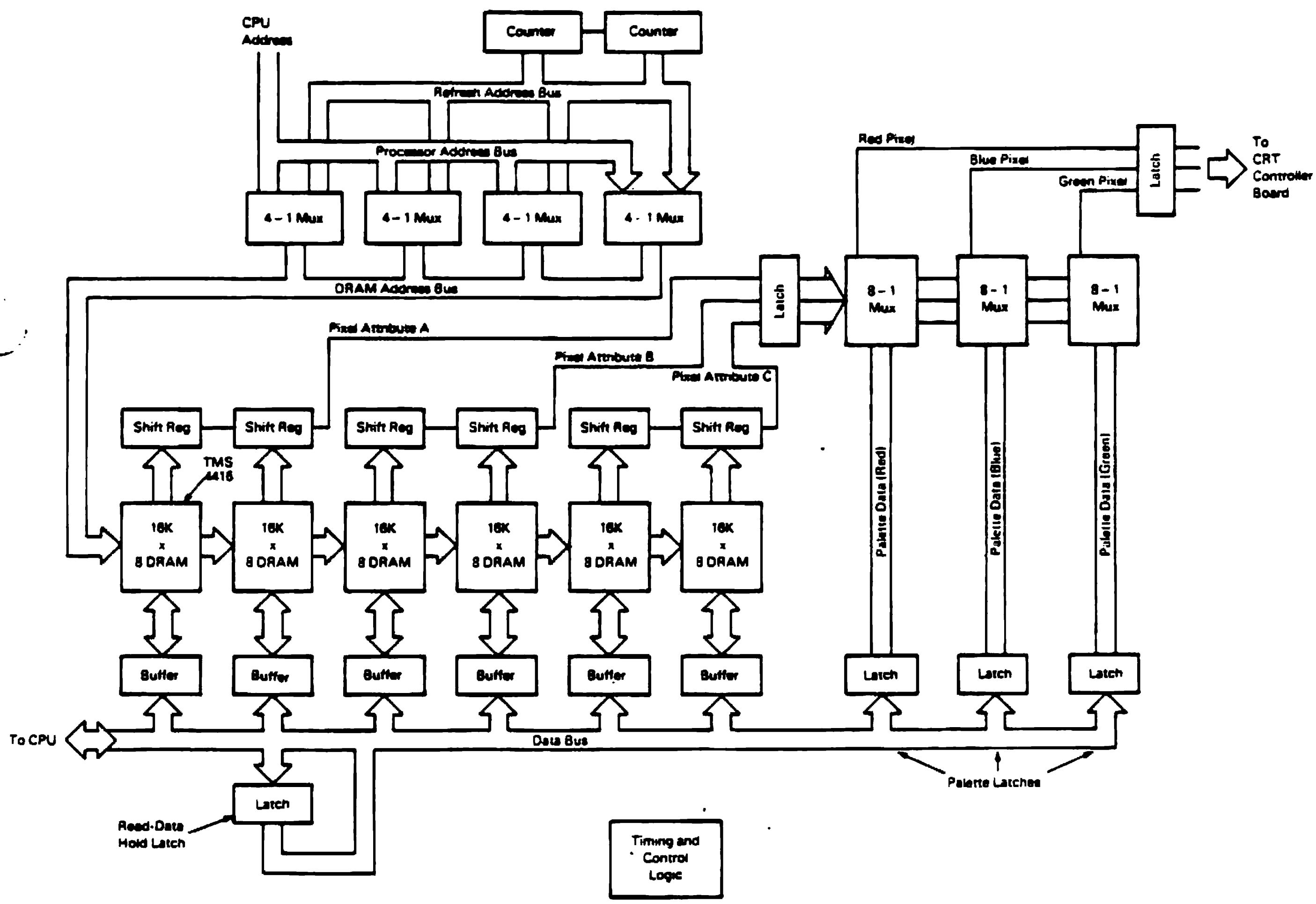


Figure 2-11 Graphics Video Controller Board Block Diagram

The graphics video controller board implements the same number of pixels (720 horizontal x 300 vertical) on the screen as does the alphanumerics board. Each pixel can contain a maximum of three attribute bits (labeled A, B, and C), which are converted by a palette lookup table to three colors - red, blue, and green.

2.10.1 Graphics Palette

The palette for the graphics video controller board is designed to map the pixel attribute bits to the three color outputs. Three 8-bit latches contain the mapping information for the attributes. The three latches correspond to the three colors, as shown in Figure 2-12.

```
     B plane value          1 1 1 1 0 0 0 0
     C plane value          1 1 0 0 1 1 0 0
     A plane value          1 0 1 0 1 0 1 0

    Latch bit addressed     7 6 5 4 3 2 1 0


     BLUE latch value   -----+
     RED latch value    ---+ :                  MONOCHROME
     GREEN latch value -+  : :        COLOR     INTENSITY
                        :  : :
                        1  1 1        White       7 max
                        1  1 0        Yellow      6
                        1  0 1        Cyan        5
                        1  0 0        Green       4
                        0  1 1        Magenta     3
                        0  1 0        Red         2
                        0  0 1        Blue        1 min
                        0  0 0        Black       0 OFF
```

Figure 2-12 Color Palette

Figure 2-13 shows the latch values to be programmed if the three attributes A, B, and C map directly to green, red, and blue.

```
Example 1                             ATTRIBUTE  COLOR
                  +-----------          111      White
                  ¦ +---------          110      Yellow
                  ¦ ¦ +-------          101      Cyan
                  ¦ ¦ ¦ +-----          100      Green
                  ¦+----------          011      Magenta
                  ¦¦¦+--------          010      Red
                  ¦¦¦¦¦+------          001      Blue
                  ¦¦¦¦¦¦¦+----          000      Black
GREEN latch       10101010
RED latch         11110000
BLUE latch        11001100
      A B C       ¦¦¦¦¦¦¦¦
      1 1 1 -----+¦¦¦¦¦¦¦
      1 1 0 -------+¦¦¦¦¦
      1 0 1 ---------+¦¦¦
      1 0 0 -----------+¦
      0 1 1 ------+ ¦ ¦ ¦
      0 1 0 --------+ ¦ ¦
      0 0 1 ----------+ ¦
      0 0 0 ------------+
```

```
Example 2                                 (GOOD FOR FLAGS)

     Background is black
     Flag background is blue          (A plane)
     RED has priority over blue       (B plane)
     WHITE has top priority           (C plane)

                                      ATTRIBUTE   COLOR
                  +-----------          111       White
                  ¦ +---------          110       Red
                  ¦ ¦ +-------          101       Blue
                  ¦ ¦ ¦ +-----          100       Black
                  ¦+----------          011       Black
                  ¦¦¦+--------          010       Black
                  ¦¦¦¦¦+------          001       Black
                  ¦¦¦¦¦¦¦+----          000       Black
GREEN latch       11001100
RED latch         11111100
BLUE latch        11001110
      A B C       ¦¦¦¦¦¦¦¦
      1 1 1 -----+¦¦¦¦¦¦¦
      1 1 0 -------+¦¦¦¦¦
      1 0 1 ---------+¦¦¦
      1 0 0 -----------+¦
      0 1 1 ------+ ¦ ¦ ¦
      0 1 0 --------+ ¦ ¦
      0 0 1 ----------+ ¦
      0 0 0 ------------+
```

Figure 2-13 Palette Programming

2.10.2 Pixel Addressing

The pixels are mapped into the processor's memory space such that a group of 16 adjacent pixels of a single attribute bit are contained within a single word. The words of pixels are mapped into a continuous string of 45 words for every row. One unused word occurs at the logical end of each row. The entire screen takes up a block of 32 768 memory locations of which 27 600 are actually used (which corresponds to 736 x 300/8). The three attribute sections are located in three, adjacent, 32-kbyte blocks of memory. Note that when a 50 Hz screen refresh rate is used, (350 displayed lines) then 32 200 bytes of the block are used. Figure 2-14 shows examples of pixel addressing.

```
      Example:  Pixel in top left corner of screen.

                      ADDRESS   BIT  0123456789ABCDEF

     Attribute A;     0C0000H    0   X...............
     Attribute B;     0C8000H    0   X...............
     Attribute C;     0D0000H    0   X...............

      Example:  Second line down, 123 from left margin.

     ((2 x 736) + 123) / 16 = 99   remainder 11
       99 x 2 = 198 = 0C6H

                      ADDRESS   BIT  0123456789ABCDEF

     Attribute A;     0C00C6H   11   ...........X....
     Attribute B;     0C80C6H   11   ...........X....
     Attribute C;     0D00C6H   11   ...........X....
```

Figure 2-14 Examples of Pixel Addressing

2.10.3 Timing and Synchronization

The graphics video controller board uses the same dot clock used by the CRT controller board to generate its other internal timing. To synchronize the pixel outputs from the two boards, the display enable (DE) signal from the CRT controller board is monitored. If the DE signal has been low for a long period of time, the graphic board assumes that the scan is in the vertical interval and resets the graphic memory and scan counters to zero when DE goes high again. When the DE signal is low for short periods of time, as in horizontal retrace, the scan counters are stopped, thus making the last pixel on a line adjacent to the first pixel on the following line. During the vertical interval when DE is low for a long period of time, the counters are restarted after a time-out to continually refresh the dynamic RAM.

The graphics video board is designed to allow the CPU essentially free access to screen memory. During a single screen display cycle, the hardware can access the refresh memory two times - once to read the data for screen display, and once for the CPU to read or write data if needed. To allow sufficient time for this access, a display cycle accesses 16 adjacent pixels of three attribute bits each These are read in parallel and loaded into three 16-bit shift registers for display. After the memory has been read for screen display, the CPU access cycle is started when a read or write cycle is requested. The memory accessed is broken up into one of six separate bytes by properly decoding the enabling of bus buffers and write enable signals to the memory.

Dynamic memory is used on the graphics video board because of the large amount of memory required. The memory chips are organized into 16k x 4 bits and are packaged in an 18-pin, dual inline package (DIP). The 8 address lines are multiplexed into 256 row addresses and 64 column addresses to get to the 16-k locations in the memory. The addresses to the RAM also need to be multiplexed between the CPU and the refresh counter. This four-way multiplexing is done by four 74LS153 dual 4-to-1 multiplexers (U33 through U36).

The timing for the graphics board is shown in Figure 2-15. The timing is generated by a 4-bit counter(U39 type 74LS63) and a logic array (U41 type HAL16R8A-1). The refresh counter start or stop logic and reset logic are provided by a counter (connected as a one-shot) and two gating circuits (U40 74LS163, U44 74LS00, U45 74LS04).

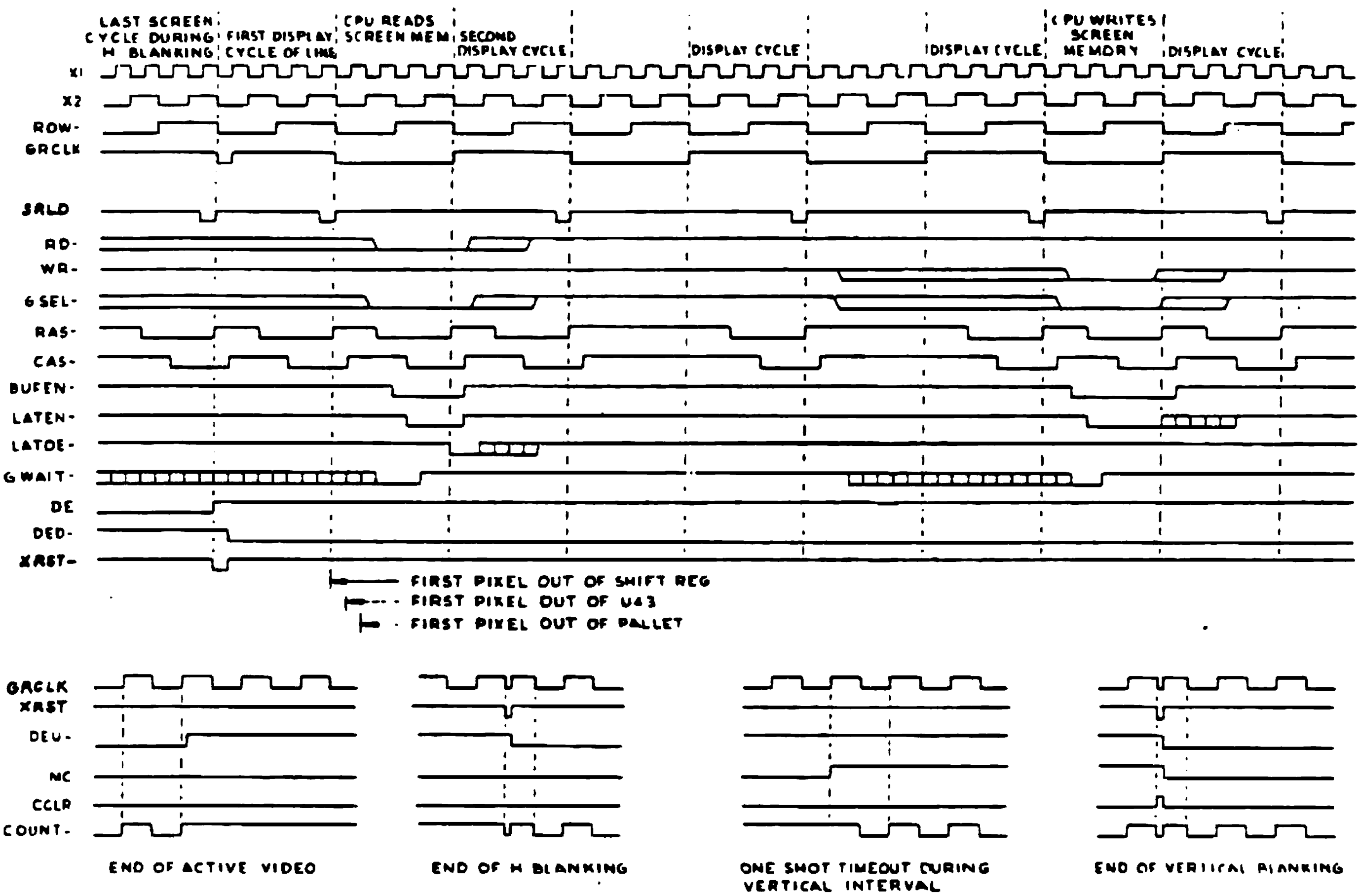


Figure 2-15 Graphics Video Controller Timing Diagram

2.10.4 Graphics Logic Array Program

Programming for the logic array is given in Table 2-19. Note that the output goes LOW when the AND of all the terms on a line OR the AND of all the terms on some other line is true.

Table 2-19 Programming for the Graphics State Machine HAL

Output:	RD-	WR-	GSEL-	DE	X1	X2	ROW-	GRCLK	LATEN-	LATOE-	RAS-	CAS-	BUFEN-	SRLD-	GWAIT-	DED-	Comment
LATEN-	L	.	L	.	.	.	H	L	.	.	L	.	.	.	.	.	READ S5, 6, 7, 8
or	.	L	L	.	.	.	.	L	.	.	.	.	L	.	.	.	WRITE S3
or	.	L	L	.	.	.	.	.	L	.	.	.	.	.	.	.	WRITE S4 till not write
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs inactive
LATOE-	L	.	L	.	H	H	H	L	.	.	L	.	.	.	.	.	READ S8
or	L	.	L	.	.	.	.	.	.	L	.	.	.	.	.	.	READ S9 till not read
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs inactive
RAS-	.	.	.	.	L	H	L	H	.	.	.	.	.	.	.	.	REFRESH SCREEN S11
or	.	L	L	.	.	L	L	.	.	.	.	.	L	.	.	.	WRITE S3
or	L	.	L	.	L	H	L	L	.	H	.	.	.	.	.	.	READ S3
or	.	.	.	.	H	H	L	.	.	.	L	.	.	.	.	.	CPU S4, REF S12
or	.	.	.	.	.	L	H	.	.	.	L	.	.	.	.	.	CPU S5, 6, REF S13, 14
or	.	.	.	.	L	H	H	.	.	.	L	.	.	.	.	.	CPU S7, REF S15
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	inactive term
CAS-	.	.	.	.	.	.	H	.	.	.	L	.	.	.	.	.	S13, 14, 15, 0, 5, 6, 7, 8
or	.	.	.	.	.	.	H	.	.	.	L	.	.	.	.	.	all other ORs.
BUFEN-	L	.	L	.	.	.	.	L	.	.	L	.	.	.	.	.	READ S4, 5, 6, 7, 8
or	.	L	L	.	H	L	L	L	H	.	.	.	.	.	.	.	WRITE S2
or	.	L	L	.	.	.	.	L	.	.	.	.	L	.	.	.	WRITE S3, 4, 5, 6, 7, 8
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs inactive
SRLD-	.	.	.	.	L	H	H	H	.	.	.	.	.	.	.	.	S15
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs inactive
GWAIT-	L	.	L	.	.	.	.	.	H	H	.	.	.	.	.	.	READ
or	.	L	L	.	.	.	.	.	H	.	.	.	.	.	.	.	WRITE
or	L	L	.	.	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs inactive
DED-	.	.	.	H	.	.	.	.	.	.	.	.	.	.	.	.	DELAYED DE
or	.	.	.	H	.	.	.	.	.	.	.	.	.	.	.	.	all other ORs.

2.11 SYNCHRONOUS-ASYNCHRONOUS COMMUNICATIONS BOARD

This subsection describes the functions and theory of operation of the synchronous-asynchronous communications (sync-async comm) board Figure 2-16 is a block diagram of the sync-async comm board. Refer to Section 5, drawing 2223096, for logic diagrams.

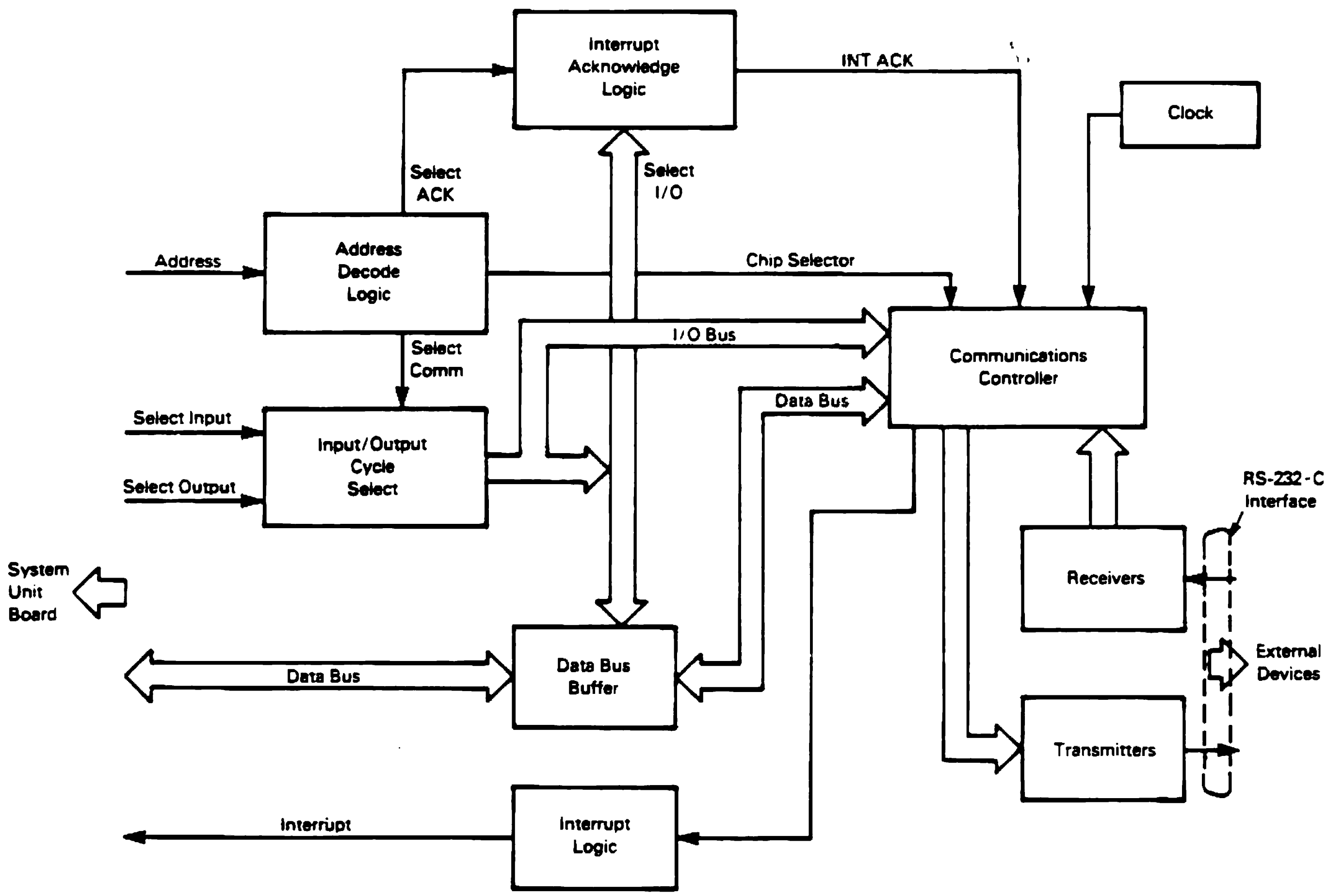


Figure 2-16 Sync-Async Comm Board Block Diagram

The sync-async comm board is designed around the Zilog Z8530 Serial Communications Controller (SCC). This device automatically handles async protocols as well as most sync protocols, including bit-oriented protocols such as synchronous data link control (SDLC) and high-level data link control (HDLC). Cyclic redundancy check (CRC) is an automatic function and can be included in any transmission. For detailed information, refer to the Zilog data manual.

2.11.1 Sync-Async Comm Board System Interface

Most of the components on the board are involved in handling the interface between the system bus and the Z8530. Of special note is the logic used to generate the interrupt acknowledge (INTACK) signal required by the Z8530 in response to an interrupt request. The INTACK- signal is generated with the help of software rather than being related to the system interrupt acknowledge signal. This condition is due to the setup time required by the part and the fact that the system expansion bus does not provide for expanding the number of interrupt levels.

To generate the INTACK- signal, the software does a AIOWC- (write) to the I/O address for interrupt acknowledge and then does a IORC- (read) from the same address. The data received on this read is the interrupt vector from the Z8530.

The AIOWC- signal clears U5B causing the INTACK- signal to the Z8530 to become active. When the IORC- occurs the vector from the 8530 is gated onto the data bus. The rising edge of IORC- clocks U5B to the inactive state to release the INTACK-.

The address selection logic is composed of the U3 (74LS139) decoder and several additional gates to qualify the address. This logic is designed to allow the board to be selected at four different address locations (see Figure 2-17), allowing multiple communications boards in the system. As with other I/O devices for this bus, only 10 of the address lines are decoded. U3 provides two decoded outputs, INTCS- and SCCCS-, for use on the board. These signals are used to activate the INTACK logic and Z8530 respectively. They are "OR"ed together to provide the board select (BDCS) signal, which in combination with the "AND" of IORC- and AIOWC- (IORQ) is used to enable the bus buffer U7.

The other logic on the system side of the board is used to delay the read and write commands to the SCC in order to meet the address and data setup and the hold time requirements of the part. The signal IORQ is connected to the input of U5A (74LS74 flip-flop) and the clock input is connected to the system CLK line. The rising edge of the clock occurs 133 ns after the IORC- or AIOWC- signal occurs. The output of U5a is gated with IORC- and AIOWC- to delay the start of the SCCRD- and SCCWR- signals. The clear input to U5a is connected to BDCS to allow the SCCRD- and SCCWR- signals to occur only when the board is selected.

In order to reset the Z8530 SCC, both the SCCRD- and SCCWR- lines must be held active together. This holding is provided by U6c and U6d which "OR" in the RESET signal from the bus with the SCCRD- and SCCWR- lines.

The interrupt output from the SCC is inverted and buffered by U4c and goes to a set of stake pins to determine the interrupt level at which the board is operated.

2.11.2 Sync-Async Comm Board Baud Rate Generation

The crystal oscillator on the board is operated at 4.9152 MHz and is divided by 2 to provide a clock for the SCCs internal baud-rate generators. The value to program for the generation of a specific baud rate is shown in Table 2-20.

Table 2-20 Sync-Async Comm Board Baud Rate

BAUD RATE	ASYNC VALUES	PERCENTAGE OF ERROR	SYNC VALUES	PERCENTAGE OF ERROR
19 200	2	0.000	62	0.000
9 600	6	0.000	126	0.000
7 200	9	-3.030	169	-0.196
4 800	14	0.000	254	0.000
3 600	19	1.587	339	0.098
2 400	30	0.000	510	0.000
2 000	36	1.053	612	0.065
1 800	41	-0.775	681	-0.049
1 200	62	0.000	1022	0.000
600	126	0.000	2046	0.000
300	254	0.000	4094	0.000
200	382	0.000	6142	0.000
150	510	0.000	8190	0.000
134.5	569	0.001	9134	0.001
110	696	0.026	11169	-0.001
75	1022	0.000	16382	0.000
50	1534	0.000	24574	0.000

2.11.3 Sync-Async Comm Board Addresses

The board addresses for the four possible ports are given in Table 2-21.

Table 2-21 Sync-Async Comm Board Port Addresses

PORT	ADDRESS	FUNCTION
PORT 1	00E0	Interrupt Acknowledge
INTERRUPT IR0 (PIN 8)	00E4	CHB Command
	00E5	CHB Data
	00E6	CHA Command
	00E7	CHA Data
PORT 2	00E8	Interrupt Acknowledge
INTERRUPT IR1 (PIN 48)	00EC	CHB Command
	00ED	CHB Data
	00EE	CHA Command
	00EF	CHA Data
PORT 3	00F0	Interrupt Acknowledge
INTERRUPT IR2 (PIN 50)	00F4	CHB Command
	00F5	CHB Data
	00F6	CHA Command
	00F7	CHA Data
PORT 4	00F8	Interrupt Acknowledge
INTERRUPT IR4 (PIN 46)	00FC	CHB Command
	00FD	CHB Data
	00FE	CHA Command
	00FF	CHA Data

2.12 WINCHESTER DISK DRIVE AND CONTROLLER

The Winchester disk drive and controller board option consists of a controller board, cable and hardware, and a 5-, 10-, or 15-megabyte Winchester drive.

2.12.1 Register Assignments

The register assignment for the Winchester controller is given in Table 2-22.

Table 2-22 Winchester Controller I/O Port Assignment

HEX ADDRESS	FUNCTIONS IN	FUNCTIONS OUT
0030	Data IN port	Data OUT port
0031	Status register	RESET
0032	Not used	Not used
0033	Not used	Interrupt mask

An IN function sets data from the Winchester controller board and drives it onto the computer's I/O expansion bus. Conversely, an OUT function sets data from the computers I/O expansion bus onto the Winchester disk controller board.

For byte definitions of the registers, refer to the I/O memory map given in Table 2-1.

2.12.1.1 Data Input Port. Disk read data and controller sense bytes are passed through this register to the computer. The data is held for each handshake cycle. The configuration is as follows:

I/O Port Address	7 (MSB)	6	5	4	3	2	1	0 (LSB)
0030	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

2.12.1.2 Data Output Port. Command bytes and disk data are passed through this register to the controller. Data is latched until updated by the CPU. The bit arrangement is as follows:

I/O Port Address	7 (MSB)	6	5	4	3	2	1	0 (LSB)
0030 (write)	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

2.12.1.3 Controller Status Register. Stores the controller status Enables the CPU to read the status of the controller and monitor its operation. The controller status byte is defined as follows:

I/O Port Address	7 (MSB)	6	5	4	3	2	1	0 (LSB)
0031 (read)	Don't care	Don't care	Don't care	Don't care	Don't care	COMMAND /DATA	INPUT/ OUTPUT	DATA REQUEST

2.12.1.4 Reset Port. Resets the controller. Any write to port 0031 does a reset. Reset must clear all error status, abort all operations, and place the Winchester controller in the command receive mode. The byte definition is given as follows:

I/O Port Address	7 (MSB)	6	5	4	3	2	1	0 (LSB)
0031 (write)	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care

2.12.1.5 Interrupt Mask. A two-bit field which determines the interrupts to be serviced by the CPU. The interrupt mask byte definition follows:

I/O Port Address 0033	MSB 7	6	5	BIT NUMBER 4	3	2	1	LSB 0
	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	DATAt INTR. ENABLE	STATUS INTR. ENABLE

2.12.1.6 Error Status Byte. This byte is a special case that is only available after a command has been completed. The controller indicates that this byte is available by setting the I/O and C/D bits with DRQ. A definition of the error status byte follows:

I/O Port Address 0030 (read)	MSB 7	6	5	BIT NUMBER 4	3	2	1	LSB 0
	Don't care	Don't care	Drive No.	Don't care	Don't care	Don't care	Error bit	Don't care

2.12.2 Bit Definition for Registers and Ports

Table 2-23 provides definition of bits for the Winchester controller registers and ports.

Table 2-23 Bit Definition for Controller Registers and Ports

DATA BIT	LOGICAL STATE: Data true ; data high ; logical one >= 2.4 V	Data false ; data low ; logical zero <= 0.7 V
DATA 0-7 READ or WRITE	DATA BIT = ONE	DATA BIT = ZERO
DATA REQUEST	Commands, status, or data ready to be transferred to or from controller.	No command, status, or data transfers to or from controller.
INPUT/ OUTPUT-	Data or status is read from the controller by the CPU.	Data or commands are written TO the controller by the CPU.
COMMAND/ DATA-	When INPUT/OUTPUT- is high, STATUS is sent to the CPU. ************************** When INPUT/OUTPUT- is low, COMMANDS are sent to the controller	When INPUT/OUTPUT- is high, DATA is sent to the CPU. ************************** When INPUT/OUTPUT- is low, DATA is sent to the controller
INTERRUPT PENDING	An interrupt (level 6) has been sent to the CPU.	No interrupt pending.
STATUS INTERRUPT ENABLE	This lets the controller interrupt the CPU when it has finished the current command, and is ready to return the status byte.	No status interrupt permitted.
DATA INTERRUPT ENABLE	This lets the controller interrupt the CPU when data needs to be read from or written to the controller.	No data interrupt permitted.

2.12.3 Controller Status Bit Combinations

Table 2-24 gives all valid controller status bit combinations.

Table 2-24 Valid Bit Combinations for Controller Status

COMMAND/ DATA	INPUT/ OUTPUT	DATA REQUEST	MEANING OF PATTERN
0	0	0	Not valid
0	0	1	A data byte may be sent FROM the CPU TO the Winchester controller. The controller waits for data to be written.
0	1	0	Not Valid
0	1	1	A data byte may be sent TO the CPU FROM the Winchester controller. Again, the controller waits until read.
1	0	0	Not valid
1	0	1	Command bytes may be sent TO the Winchester controller FROM the CPU.
1	1	0	Not valid
1	1	1	A status byte may be sent FROM the Winchester controller TO the CPU.

2.12.4 Normal Command Sequence Operation

Figure 2-17 depicts the logical flow of the controller functions.

```
                    ***************
                    *  START      *
                    ***************
                           !
                           V
+--------------------------+--------------------------+
! Reset the Winchester controller                     !
!         ( write to port 31 )                        !
+--------------------------+--------------------------+
     WAIT1                 !
     -------------------->!
                           V
+--------------------------+--------------------------+
!    Read status port (0031)                          !
!                                                     !
+--------------------------+--------------------------+
                           !
                           V
                           *
                         *   *
                       *  Is   *
                     * REQUEST   *   NO
                   *    ACTIVE?    *------> WAIT1
                     *           *
                       *       *
                         *   *
                           * YES
                           !
                           V
                           *
                         *   *
                       *       *
                     *  COMMAND  *  NO               < HARDWARE >
                   *    MODE?      *-----------> <  FAULT    >
                     * ( C/D=1,  *
                       * I/O=0)*
                         *   *
                           *
                           !
                           V
                      < OUTPUT >
```

Figure 2-17 Controller Operational Flowchart

```
                      < OUTPUT >
                          |
                          V
+-------------------------+-------------------------+
|    OUTPUT COMMAND BYTES TO CONTROLLER             |
|           ( write to port 0030 )                  |
+-------------------------+-------------------------+
                          |
                          |<--------------+
                          V               |
                          *               |
                        *   *             |
                      * DATA  *           |
                    *   MODE?   *   NO    |
                  *  ( C/D=0 )   *------>--+
                    *           *
                      *       *
                        *   *
                          *
                          |
                          V
+-------------------------+-------------------------+
|   WRITE OR READ CONTROLLER DATA                   |
|        ( read/write to port 0030 )                |
+-------------------------+-------------------------+
                          |
                          |<------------+
                          V             |
                          *             |
                        *   *           |
                      * STATUS*         |
                    * OUTPUT    *   NO  |
                  *     MODE?    *------+
                    * (I/O=1,   *
                      * C/D=1)*
                        *   *
                          *
                          |
                          V
+-------------------------+-------------------------+
|   READ STATUS FROM PORT 0030                      |
|                                                   |
+-------------------------+-------------------------+
                          |
                          |
                          V
                    < END LOOP >
```

Figure 2-17 Controller Operational Flowchart, Continued

```
                  < END LOOP >
                       !
                       V
                       *
                     *   *
                   *  DID  *
                 * AN ERROR  *    NO
               *    OCCUR?     *----> < WAIT1 >
                 *           *
                   *       *
                     *   *
                       *
                       !
                       !
                       V
+----------------------+----------------------+
!   DO REQUEST STATUS COMMAND AND              !
!       DECODE ERROR                           !
+----------------------+----------------------+
                       !
                   ********
                   * END  *
                   ********
```

Figure 2-17 Controller Operational Flowchart, Concluded

2.12.5 Winchester Hardware Theory of Operation

The Winchester controller is addressed by the 8088 as a block of four I/O ports: Hex 0030 to 0033. I/O reads are indicated by the bus signal IORC, and I/O writes are indicated by the bus signal AIOWC-

The controller can generate an interrupt to the host under the following conditions.

* When data is ready to be read from or written to the controller.
* When the operation is completed, and the controller is requesting a status read (C/D-=1, I/O=1).

Both of the interrupt conditions can be individually disabled. When the interrupt is active, the computers interrupt line 6 is held high until it is cleared by a read to the controller status register.

2.12.5.1 On Board EPROM/ROM. The controller has a 4K x 8 bit EPROM/ROM. This device is addressed in memory space at address OFBOOOH and contains the driver routines for the controller. The output of the EPROM/ROM drives the data bus through a tri-state buffer when addressed. Access times on either the EPROM or the ROM are not greater than 350 ns.

2.12.5.2 Commands and Command Testing. The computer sends a six-byte block to the controller to specify the operation. This block is the device control block (DCB). Table 2-25 defines the DCB.

Table 2-25 Device Control Block Bit Diagram

Byte	7	6	5	4	3	2	1	0
0	COMMAND CLASS			OPCODE				
1	LOGICAL UNIT NUMBER			HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	INTERLEAVE OR NUMBER OF BLOCKS (note 2)							
5	CONTROL FIELD							

NOTES:
1. Refer to subparagraph 2.12.5.6, "Logical Address".
2. Interleave factor for FORMAT, CHECK TRACK, and READ ID command

2.12.5.3 Explanation of Bytes in the Device Control Block. The six bytes which comprise the device control block are defined as follows

BYTE	DEFINITION
0	Bits 7, 6 and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command.
1	Bits 7, 6 and 5 identify the logical unit number (LUN). Bits 4 through 0 contain logical disk address 2.
2	Bits 7 through 0 contain logical disk address 1.
3	Bits 7 through 0 contain logical disk address 0 (LSB).
4	Bits 7 through 0 specify the interleave or block count.
5	Bits 7 through 0 contain the control field.

2.12.5.4 Control Field Detailed Description. The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The following listing defines the bits of the control byte. The step options are encoded in control byte 5 of the command descriptor. The encoding is done with bits 0 through 3 as follows:

DESCRIPTION	BIT 3	BIT 2	BIT 1	BIT 0
Default 3-ms step rate	0	0	0	0
Seagate ST506 (MLC2)	0	0	0	1
Tandon fast step	0	0	1	0
Texas Instrument fast step	0	0	1	1
200-us buffered step	0	1	0	0
70-us buffered step	0	1	0	1
30-us buffered step	0	1	1	0
15-us buffered step	0	1	1	1
Olivetti 2 ms/step (561)	1	0	0	0
Olivetti (562) fast step (1.1 ms typical)	1	0	0	1
Spare (for future use)	1	1	1	1

Refer to the drive manufacturer's manual in configuring the drive for fast-, or buffer-step options. In cases where the drive is hardware-configured for fast step, all commands which require seek option selection must use the fast-step option for that drive.

NOTE

The step option bits (3 through 0) are mutually exclusive and only one option should be selected in any given configuration.

Bits 4-5 are reserved for future use.

If bit 6 is a 1, during a read sector command, the failing sector is not re-read on the next revolution before attempting correction. This bit should be set to 0 for normal operation.

Bit 7 disables the four retries by the controller on all disk- access command. Set this bit only during the evaluation of the performance of a disk drive. This bit should be set to 0 for normal operation.

2.12.5.5 Command Completion Status Byte. At the end of a command, the controller returns ONE completion status byte to the computer to indicate if an error occurred during command execution. The REQUEST SENSE STATUS COMMAND must be issued if the error bit is set to determine the cause of the error. The format of the completion status byte is :

I/O Port Address 0030 (read)	MSB 7	6	5	BIT NUMBER 4	3	2	1	LSB 0
	Don't care	Don't care	Drive No.	Don't care	Don't care	Don't care	Error bit	Don't care

2.12.5.6 Logical Address (HIGH, MIDDLE AND LOW). The logical address of the drive is computed by using the following equation.

Logical Address = (CYADR x HDCYL + HDADR) x SETRK + SEADR

Where: CYADR = Cylinder address
HDADR = Head address
SEADR = Sector address
HDCYL = Number of heads per cylinder
SETRK = Number of sectors per track

2.12.5.7 Sector Interleaving. Variable sector interleaving is supported by the disk controller. When any format command is issued any interleave value up to the number of sectors-per-track minus may be passed in the device control block (DCB byte 4). The interleave factor may be adjusted for maximum system performance when transferring multiple sectors of data. Interleaving allows logical continuous sectors of data on a given track to be mapped onto nonadjacent physical sectors. An interleave factor of 5, for instance, means that every fifth physical sector is transferred as the next continuous logical sector of data. It does not mean that five sectors of data are transferred on one revolution. If the CPU cannot transfer the full sector of data during the sector interleave time available, then the controller has to wait a full revolution before the next logical sector can be read from the disk. If this happens, the interleave factor is too low and should be increased until an increase in operating system speed is noticed.

In order to take full advantage of the interleaving feature of the controller, the operating system should perform multiple-sector data transfers. If single-sector transfers are employed, the difference in speed with various interleave factors may not be noticeable.

2.12.6 Detailed Description of Commands

The commands fall into eight classes, 0 through 7; only classes 0 and 7 are used. Class 0 commands are data, non-data transfer, and status commands. Classes 1 through 6 are reserved. Class 7 commands perform diagnostics. Each command is described in the following paragraphs. The command description includes class, opcode, and format. "Dont care" bits are shown as "unused".

2.12.6.1 TEST DRIVE READY Command. This command selects a particular drive and verifies that the drive is ready. The following diagram shows the format of the device control block for this command:

Byte	BIT NUMBER							
	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0	0
1	0	0	DRIVE	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

The TEST DRIVE READY command can be used with overlapped seeks to determine when a drive has completed seeking before issuing the next command. If the drive is still seeking, the status byte at the end of the command indicates an error, and the sense status indicates "drive still seeking" (type 0 error, code 8). A sequence of TEST DRIVE READY commands can thus be used to determine when the drive is ready for the next command.

2.12.6.2 RECALIBRATE DRIVE Command. This command positions the read/write (R/W) arm to track 000. Bit definitions for this command are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0	1
1	0	0	DRIVE	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

2.12.6.3 REQUEST SENSE STATUS Command. The computer must send this command immediately after it detects an error. The command causes the Controller to return four bytes of drive and controller status. the formats of these four bytes are shown after the DCB. When an error occurs on a multiple-sector data transfer (read or write), the REQUEST SENSE STATUS command returns the logical address of the failing sector in bytes 1, 2 and 3. If the REQUEST SENSE STATUS command is issued after any of the Format commands or the CHECK TRACK FORMAT command, the logical address returned by the controller points to one sector beyond the last track formatted or checked if there was no error. If there was an error, the logical address returned points to the track in error. Table 2-26, Table 2-27, Table 2-28, and Table 2-29 list the error codes. Definitions of these bytes follow:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	1	1
1	0	0	DRIVE	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

<u>Sense Bytes Returned.</u> The address valid bit (bit 7) in the error code byte is relevant only when the previous command required a logical block address; in this case it is always returned as a 1; otherwise it is set to 0. For instance, if a RECALIBRATE command is followed immediately by a REQUEST SENSE STATUS command, the address valid bit could be returned as 0 since the command does not require a logical block address to be passed in its DCB. The format for the sense bytes returned are as follows:

Byte	BIT NUMBER							
	7	6	5	4	3	2	1	0
0	ADDRESS?	0	ERROR TYPE		ERROR CODE			
1	0	0	DRIVE	HIGH ADDRESS (see note)				
2	MIDDLE ADDRESS (see note)							
3	LOW ADDRESS (see note)							

NOTE: Refer to paragraph 2.12.5.6, "Logical Address".

Table 2-26 Type 0 Error Codes, Winchester Disk

HEX CODE	DEFINITION
0	The controller detected no error during the execution of the previous operation.
1	The controller did not detect an index signal from the drive.
2	The controller did not get a SEEK COMPLETE signal from the drive after seek operation.
3	The controller detected a write fault from drive during last operation.
4	After the controller selected the drive, the drive did not respond with READY signal.
5	Not used.
6	After stepping maximum number of cylinders, controller did not receive track 00 signal from the drive.

Table 2-27 Type 1 Error Codes, Controller Board

HEX CODE	DEFINITION
0	ID Read Error: The controller detected an ECC error in the target ID field on the disk.
1	Data Error: The controller detected an uncorrectable ECC error in the target sector during a read operation.
2	Address Mark: The controller did not detect the target address mark (AM) on the disk.
3	Not used.
4	Sector Not Found: The controller found the correct cylinder and head, but not the target sector.
5	Seek Error: The controller detected an incorrect cylinder or track, or both.
6	Not used.
7	Not used.
8	Correctable Data Error: The controller detected a correctable ECC error in the target data field.
9	Bad Track: The controller detected the bad track flag during the last operation.
A	Format Error: During a check-track command, the controller detected one of the following: 1) track not formatted 2) wrong interleave 3) ID ECC error on at least one (1) sector

Table 2-28 Types 2 and 3 Error Codes, Command and Miscellaneous

HEX CODE	TYPE	DEFINITION
0	2	Invalid Command: The controller has received an invalid command from the hot
1	2	Illegal Disk Address: The controller detected an address that is beyond the maximum range.
0	3	RAM Error: The controller detected a data error during the RAM sector buffer diagnostic.
1	3	Program Memory Checksum Error: During its internal diagnostic, the controller detected a program-memory checksum error.
2	3	ECC Polynominal Error: During the controllers internal diagnostic, the hardware ECC generator failed its test.

2.12.7 Error Codes

The following is a summary of the error codes returned as the result of the REQUEST SENSE STATUS command.

NOTE: The ADDRESS VALID bit (bit 7) may or may not be set and is not included here.

Table 2-29 Error Code Summary

ERROR CODE (HEX)	MEANING
00	No error detected (command completed ok).
01	No index detected from disk drive.
02	No seek complete from disk drive.
03	Write fault from disk drive.
04	Drive not ready after it was selected.
05	Not used.
06	Track 00 not found.
07-0F	Not used.
10	ID field read error.
11	Uncorrectable data error.
12	Address mark not found.
13	Not used.
14	Target sector not found.
15	Seek error.
16-17	Not used.
18	Correctable data error.
19	Bad track flag detected.
1A	Format error.
1B	Not used.
1C	Illegal (direct) access to an alternate track.

TABLE 2-29 ERROR CODE SUMMARY (continued

ERROR CODE (HEX)	MEANING
1D	On a FORMAT ALTERNATE TRACK command, the track is already assigned, or is flagged as bad track.
1E	When the controller attempted to access an alternate track from a spared track, the alternate track was not flagged as an alternate.
1F	On a FORMAT ALTERNATE TRACK command, the bad track equaled the alternate track.
20	Invalid command.
21	Illegal disk address.
22-2F	Not used.
30	Ram diagnostic failure.
31	Program memory checksum error.
32	ECC diagnostic failure.
33-3F	Not used.

2.12.8 FORMAT DRIVE Command

This command formats all sectors with ID and data fields according to the selected interleave factor, and writes 6C hex into data fields. The controller formats from the starting address, which is passed in the command, to the end of the disk.

If bit 5 of control byte 5 of the command block is set on the format command (OPCODE 04), the sector buffer is used as the data pattern written on the disk data fields).

The WRITE SECTOR BUFFER command can be issued before the format command to initialize the sector buffer. Byte definitions are as follows:

Byte	BIT NUMBER 7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	0	0	0	INTERLEAVE FACTOR (note 2)				
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:
1. Refer to paragraph 2.12.5.6, "Logical Address".
2. Factors are 1 to 31 for 256-byte sector and 1 to 16 for 512-byte sector.

2.12.9 CHECK TRACK FORMAT Command

This command checks the format on the specified track for correct ID and interleave. The command does not read the data field. The byte configuration is as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	0	0	0	INTERLEAVE FACTOR (note 2)				
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:
1. Refer to subparagraph 2.12.5.6, "Logical Address".
2. Factors are 1 to 31 for 256-byte sector and 1 to 16 for 512-byte sector.

2.12.10 FORMAT TRACK Command

The FORMAT TRACK Command reformats the track, eliminating all references to bad and alternate tracks. Also, if bit 5 of control byte 5 of the command block is set, then the sector buffer is used as the data pattern in the data fields, otherwise the command writes 6C hex in the data fields. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	0	0	0	INTERLEAVE FACTOR (note 2)				
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:
1. Refer to paragraph 2.12.5.6, "Logical Address".
2. Factors are 1 to 31 for 256-byte sector and 1 to 16 for 512-byte sector.

2.12.11 FORMAT BAD TRACK Command

This command formats a specified track, setting the bad sector flag in the ID fields. No data fields are written. The byte definitions are as follows:

Byte	BIT NUMBER 7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	1
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	0	0	0	INTERLEAVE FACTOR (note 2)				
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:
1. Refer to paragraph 2.12.5.6, "Logical Address".
2. Factors are 1 to 31 for 256-byte sector and 1 to 16 for 512-byte sector.

2.12.12 READ COMMAND

Starting with the sector address given in this command, the controller reads a specified number of sectors. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	BLOCK COUNT							
5	RETRY?	note 2	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:
1. Refer to paragraph 2.12.5.6, "Logical Address".
2. If an ECC error is found when this bit is set in the READ command retry the command.

2.12.13 WRITE Command

This command writes the specified number of sectors, starting with the initial sector address contained in the DCB. Each sector of data can be either 256 or 512 bytes long. The sector size is jumper selectable. Byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0
1	0	0	DRIVE	HIGH ADDRESS (see note)				
2	MIDDLE ADDRESS (see note)							
3	LOW ADDRESS (see note)							
4	BLOCK COUNT							
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTE: Refer to paragraph 2.12.5.6, "Logical Address".

2.12.14 SEEK Command

This command initiates a seek to the track specified in the DCB. The drive must be formatted. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1
1	0	0	DRIVE	HIGH ADDRESS (see note)				
2	MIDDLE ADDRESS (see note]							
3	LOW ADDRESS (see note)							
4	U N U S E D							
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTE: Refer to paragraph 2.13.5.6, "Logical Address".

2.12.14.1 Overlap Seeks with Buffered Step Drives. For drives employing buffered seeks, SEEK commands can be overlapped. After the controller issues a SEEK to the drive, it returns a completion status, not waiting for the drive to complete the SEEK. If the return status shows no error, then the SEEK was issued correctly. If there is an error, then the SEEK was not issued. After transfering the status, another command can be issued to either drive. If a new command is received for a drive with an outstanding SEEK, then the controller waits, with BUSY active, for the SEEK to complete before executing the new command (except the TEST DRIVE READY command). There is no time-out condition in the controller, waiting for the buffered-step SEEKS to complete.

2.12.15 INITIALIZE DRIVE CHARACTERISTICS Command

This command enables the user to configure the controller to work with drives that have different capacities and characteristics. However, both Winchester drives must be of the same manufacturer and model number.

After the computer sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters Some of the parameters occupy two bytes; all two-byte parameters are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

C = Maximum number of cylinders (2 bytes)
H = Maximum number of heads (1 byte)
W = Starting reduced write current cylinder (2 bytes)
P = Starting write precompensation cylinder (2 bytes)
E = Maximum ECC data burst length (1 byte)

When the controller is powered up or reset, the default values listed below are set.

Maximum number of cylinders = 153
Maximum number of heads = 4
Starting reduced write current cylinder = 128
Starting write precompensation cylinder =64
Maximum ECC data burst length = 11 bits

The parameter for the maximum ECC burst length defines the length of a burst error in the data field that the controller is to correct. The burst length is defined as the number of bits from the first error bit to the last error bit. For example, if the controller detects a 5-bit ECC error and the erroneous data appears as C5 (1100 0101) before correction, it could appear as D4 (1101 0100) after the correction. However, if the CPU has set the maximum ECC burst length at 4 bits, the controller might flag this data as uncorrectable. This is a type 1, code 1 error.

Byte definitions for the INITIALIZE DRIVE CHARACTERISTICS command are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	0	0
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.15.1 Drive Parameter Bytes. These bytes are passed to the controller after the INITIALIZE DRIVE CHARACTERISTICS command has been issued:

Byte	7	6	5	4	3	2	1	0
0	MAXIMUM NUMBER OF CYLINDERS: MSB							
1	MAXIMUM NUMBER OF CYLINDERS: LSB							
2	0	0	0	0	MAXIMUM NUMBER OF HEADS			
3	STARTING REDUCED WRITE CURRENT CYLINDER: MSB							
4	STARTING REDUCED WRITE CURRENT CYLINDER: LSB							
5	STARTING WRITE PRECOMPENSATION CYLINDER: MSB							
6	STARTING WRITE PRECOMPENSATION CYLINDER: LSB							
7	0	0	0	0	MAXIMUM ECC DATA BURST LENGTH			

2.12.16 READ ECC BURST ERROR LENGTH Command

This command transfers one byte to the CPU. This byte contains the value of the ECC burst length that the controller detected during the last Read command. This byte is valid only after a correctable ECC data error, type 1, code 8. Byte definitions are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	0	1
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.17 FORMAT ALTERNATE TRACK Command

FORMAT ALTERNATE TRACK formats the header fields of the "bad track" with the alternate track information (assigned by the CPU). The alternate track is formatted to identify it as an alternate. The command byte definitions for FORMAT ALTERNATE TRACK are as follows:

Byte	BIT NUMBER 7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	0
1	0	0	DRIVE	HIGH ADDRESS (note 1)				
2	MIDDLE ADDRESS (note 1)							
3	LOW ADDRESS (note 1)							
4	0	0	0	INTERLEAVE FACTOR (note 2)				
5	RETRY?	0	(Note 3)	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTES:

1. Refer to paragraph 2.12.5.6, "Logical Address".

2. Interleave factor is 1 to 31 for 256 byte sectors and 1 to 16 for 512 byte sectors.

3. If this bit is set, the data in the existing sector buffer is used to fill the data field. If this bit is cleared, the data field is written with 6C hex.

The interleave byte (4) is programmed the same as in the FORMAT command, and is used on the alternate track. If bit 5 of control byte (5) is set, the data in the existing sector buffer is used to fill the data field. If not set, the data field is written with 6C hex. After issuing the command, the controller asks for the following 3 bytes. These bytes point to the CPU-assigned alternate logical address. Again the sector address is ignored.

2.12.17.1 Assigned Alternate Address Data Block. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	0	0	0	HIGH ADDRESS (see note)				
1	MIDDLE ADDRESS (see note)							
2	LOW ADDRESS (see note)							

NOTE: Refer to paragraph 2.12.5.6, "Logical Address".

2.12.17.2 Alternate Track Assignment. The assignment of alternate tracks and the lockout of bad tracks has to be done by the computer. Bad areas on the disk are labeled defective on a track basis by issuing a FORMAT BAD TRACK command (Command code 07). One procedure for assignment and handling of alternate tracks is as follows:

1. The entire disk drive is formatted by issuing a FORMAT DISK command (Command code 04) starting at logical track 000. If an error occurs during formatting, then a REQUEST SENSE STATUS command should be issued. If a format error is indicated, bytes 1, 2, and 3 of the returned status gives the address of the bad track and a FORMAT BAD TRACK command (command code 07) should be issued to the track. A new FORMAT command is then issued to format the rest of the disk starting at one track beyond the bad track. If any other errors occur during the subsequent formatting, the above process should be repeated until the entire disk is formatted.

2. A RECALIBRATE command is issued (Command code 01) to position the heads over track 000.

3. All sectors on the disk are read to see whether any uncorrectable ECC errors have occurred in the data. The FORMAT command places a 6C hex pattern in the data fields of all sectors and the computer program can optionally verify this data pattern after the data is read into memory. However, verifying the data byte-for-byte is not normally necessary since the error detection and correction circuitry flags all uncorrectable errors. If a large block of host memory is available, multiple sector reads can be issued to speed up the verify process.

4. When an uncorrectable error is found, a FORMAT BAD TRACK command (Command code 07) is issued to the failing track which writes a bad track flag into all identifier fields. Whenever this track is subsequently accessed, an error results and the sense status which follows indicates an error code 19 hex.

Whenever a user program accesses the disk, it should not be allowed by the operating system to issue a READ or WRITE command to the alternate tracks. The disk controller has no way of knowing when an alternate track is being read. The alternate tracks are sometimes assigned at the end of the disk (highest track numbers) but they may be assigned to any tracks so long as the track label is maintained by the computer. In general, if four tracks are reserved as alternates, they should be adequate for all disk drives currently available given the error correction capability of the controller; however, it is recommended that the system programmer consult the disk drive manual for the hard defect specifications.

2.12.17.3 Alternate Address Protocol. After receiving the command and the assigned alternate, the controller does the following.

1. Seeks to "alternate assigned track" and verifies it is not already an assigned alternate track, or flagged bad track. If the track has already been assigned as an alternate or is flagged "BAD", then error code ID hex is given and the command is aborted. This usually implies that the computer is attempting to assign two (2) bad tracks to the same alternate track.

2. Formats the track as an assigned alternate track.

3. Seeks to the "bad track" and formats the header as a spare track pointing to the assigned alternate.

NOTE

Data fields on both the bad track and alternate track are destroyed.

Using the FORMAT ALTERNATE TRACK Command

1. The controller must be initialized to include the alternate tracks cylinder and head ranges.

2. Note that, with alternate tracks, the entire disk is not available to the system. Generally the disk space is fixed in the system software, which can be assigned as alternates when needed.

   The number of spare tracks is dependent on drive size and number of defects allowed by the drive manufacturer. Generally this is 1 spare track for each 50 to 100 tracks.

3. Procedure for use is to:

   * Format the entire disk, including spare tracks

   * Verify the disk.

   * Assign each media defect an alternate track.

   * Assign alternate tracks for drive manufacturer's list of defects.

4. In system operation, the alternate tracks are invisible to the host. The controller automatically seeks to the assigned alternate track when an access is made to a flagged defective track. "Consecutive" accesses to a flag track does not result in reseeking to the alternate track. The controller maintains position on the alternate track.

5. Direct access (seeking to, or attempted data transfer) to an alternate track results in an error code IC hex, and no data transfer takes place.

2.12.18 WRITE SECTOR BUFFER Command

This command is used to fill the sector buffer with a host given data pattern. No transfer of data takes place between the drive and the controller The command accepts 256 or 512 bytes (depending on sector size jumper) of data, and stores it in the sector buffer. The byte definitions are as follows:

Byte	BIT NUMBER							
	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1	1
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.19 READ SECTOR BUFFER Command

This command sends 256 or 512 bytes of data (depending on sector size jumper) to the CPU from the sector buffer. The byte definitions are as follows:

Byte	BIT NUMBER							
	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	1	0	0	0	0
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.20 RAM DIAGNOSTICS Command

This command performs a data pattern test on the RAM buffer. The byte definitions are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	0	0
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.21 DRIVE DIAGNOSTICS Command

This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and verifies sector 0 of all the tracks on the disk. The controller does not perform any write operations during the command; it is assumed that the disk has been previously formatted. The byte definitions for the command are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	1	1
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

2.12.22 CONTROLLER INTERNAL DIAGNOSTICS Command

This command causes the controller to perform a self-test. The controller checks its internal processor, data buffers, ECC circuitry, and the checksum of the program memory. The controller does not access the disk drive. The byte definitions are as follows:

Byte	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	1	0	0
1	unused	unused	unused	unused	unused	unused	unused	unused
2	unused	unused	unused	unused	unused	unused	unused	unused
3	unused	unused	unused	unused	unused	unused	unused	unused
4	unused	unused	unused	unused	unused	unused	unused	unused
5	unused	unused	unused	unused	unused	unused	unused	unused

2.12.23 READ LONG Command

This command transfers the target sector and four bytes of data ECC to the CPU. If an ECC error occurs during the read, the controller does not attempt to correct the data field. This command is useful in recovering data from a sector that contains an uncorrectable ECC error. It is also useful during diagnostic operations. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	0	1
1	0	0	DRIVE	HIGH ADDRESS (see note)				
2	MIDDLE ADDRESS (see note)							
3	LOW ADDRESS (see note)							
4	BLOCK COUNT (see note)							
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTE: Refer to paragraph 2.12.5.6. "Logical Address".

2.12.24 WRITE LONG Command

This command transfers a sector of data and four appended ECC bytes to the disk drive. During this write operation, the computer supplies the four ECC bytes instead of the usual hardware- generated ECC bytes. This command is useful only for diagnostic operations. The byte definitions are as follows:

Byte	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1	0
1	0	0	DRIVE	HIGH ADDRESS (see note)				
2	MIDDLE ADDRESS (see note)							
3	LOW ADDRESS (see note)							
4	BLOCK COUNT							
5	RETRY?	0	0	0	STEP 3	STEP 2	STEP 1	STEP 0

NOTE: Refer to paragraph 2.12.5.6 "Logical Address".

2.12.25 Diagnostics and Error Correction

2.12.25.1 Execution of Diagnostics. Since all of the diagnostics are not executed by the computer on power-up, it is suggested that they be called by the CPU in the following order:

1. CONTROLLER INTERNAL DIAGNOSTICS (Command code E4). This diagnostic tests all the logical and decision-making capability of the controller as well as the program memory checksum and the error detection and correction circuits (ECC). Execution of this diagnostic ensures that the controller can communicate with the computer.

2. RAM DIAGNOSTICS (Command code E0). This command verifies that the sector buffer is operational by writing, reading, and verifying various data patterns to and from all locations.

3. If the parameters of the connected drives are different than the default parameters, the new configuration must be sent to the controller using the INITIALIZE DRIVE CHARACTERISTICS (Command code 0C) before the DRIVE DIAGNOSTIC command is executed.

4. Before the DRIVE DIAGNOSTICS is executed, the computer should continuously issue a TEST DRIVE READY command (Command code 00) to the controller with the appropriate time-out until the drive becomes ready.

5. DRIVE DIAGNOSTIC (Command code E3). This diagnostic issues a RECALIBRATE to the disk drive and then steps though all tracks verifying the ECC on the identifier fields of the first sector of each track. If this diagnostic passes, it implies that the disk has been formatted and that the first ID field of each track is good.

2.12.25.2 Error Correction Philosophy. Since the typical error-correction time of the controller is approximately 50 ms and greater than the time for one revolution of the disk, the sector in error is optionally re-read (if bit 6 is not set in byte 5 of the READ command DCB) on the next revolution during a Read command. In most cases, the error is soft and does not reappear on the re-read. This initial re-read of the failing sector is over and above the retry count passed in the DCB (bit 7, byte 5).

The retry count on errors is preset to 4 by the controller each time a sector has been read successfully. On a multiple-sector transfer if an uncorrectable error was detected but subsequently found to be correctable on a retry, the retry count is reset to 4 before the next sector is read from the disk.

2.12.25.3 Sector Field Description. The format of the sector configuration is given and the information fields in those sectors are identified in the following listing:

FIELD	NUMBER OF BYTES	FIELD DESCRIPTION
AM	4	Address mark
GAP1	9	Zero byte gap
SYNC	1	ID sync byte
GAP2	2	ID zero byte gap
COM	1	ID compare byte
CYLH	1	Cylinder high (MSB)
CYLL	1	Cylinder low (LSB)
HEAD	1	Head number
SEC	1	Sector number
FLAG	1	Flag byte
ZER	1	Zero byte
ECC	4	ID ECC bytes
GAP3	16	Zero byte gap
SYNC2	1	Data field sync byte
GAP4	2	Data field zero byte gap
DATA	512	Data field
ECC2	4	Data field ECC bytes
GAP5	43	Inter-record zero gap

The track layout for the 512 bytes/sector, 17 sectors/track is given in Table 2-30.

Table 2-30 512-Bytes-Per-Sector Format

BYTE	7 (MSB)	6	5	4	3	2	1	0 (LSB)
1-4	ADDRESS MARK							
5-13	0	0	0	0	0	0	0	0
14	ID SYNC BYTE							
15-16	0	0	0	0	0	0	0	0
17	ID COMPARE BYTE							
18	CYLINDER NUMBER (MSB)							
19	CYLINDER NUMBER (LSB)							
20	HEAD NUMBER							
21	SECTOR NUMBER							
22	FLAG BYTE							
23	0	0	0	0	0	0	0	0
24-27	ID ERROR CORRECTION CODE BYTES							
28-43	0	0	0	0	0	0	0	0
44	DATA FIELD SYNC BYTE							
45-46	0	0	0	0	0	0	0	0
47-558	512 BYTES DATA							
559-562	DATA FIELD ERROR CORRECTION CODE BYTES							
563-605	0	0	0	0	0	0	0	0

Track Capacity = 10416

```
 10285  =  17 sectors of 605 bytes/sector
  +131  =  Speed tolerance gap
 -----
 10416
```

605 bytes/sector including ID and overhead

2.12.26 Specifications - Controller Board

The Winchester controller board specifications are given in Table 2-31

Table 2-31 Winchester Controller Board Specifications

Environmental Parameters:

	OPERATING	STORAGE
Temperature	10 $^\circ$C(32 $^\circ$F) to 40 $^\circ$C(131 $^\circ$F)	-10 $^\circ$C(-40 $^\circ$F) to 60 $^\circ$C(167 $^\circ$F)
Relative Humidity (@ 40 $^\circ$F wet bulb temp., no condensation)	10% to 90%	10% to 90%
Altitude	Mean sea level to 10 000 feet	Mean sea level to 45 000 feet

Power Requirements:

VOLTAGE	RANGE	CURRENT
+5.0 Vdc	4.75 to 5.25 Vdc	2.5 A maximum 2.0 A typical
-12.0 Vdc	-10.8 to -13.2 Vdc	66.0 mA maximum 48.0 mA typical

2.12.27 Electrical Interface

This paragraph specifies the electrical interface requirements for the 5 1/4-inch Winchester disk drive.

All Winchester controller boards shall use header assemblies interchangable with the AMP type 87215-7 for the 20-pin connectors (to J2/P2), and type 1-87215-7 for the 34-pin connector (to J1/P1). The connector layout is shown in Figure 2-18.

```
 --------------+                                                +-----------
  WINCHESTER   !                                                ! Winchester
    CONTROLLER !                                                ! disk drive
      BOARD    !             Ribbon cable to                    !
               !   +--+        Winchester drive         +--+    !
         ------!   !  !=========*  *===============!   !   +-+
AMP header    [!-- !  ! AMP      *  *          AMP !   !   !-
assembly      [!-- !  !receptacle *  *      ribbon !   !   !-
type 87215-7  [!-- !  !connector   *  *  connector !P2!    !- J2
or equivalent [!-- !  !type        *  *       type !   !   !-
              [!-- !  !88377-4     *  *    88373-6 !   !   !-
              [!-- !  !or equiv.   *  *  or equiv. !   !   !-
              [!-- !  !==============*  *==========!   !   +-+
         ------!   +--+       20-pin ribbon cable   +--+    !
               !                                            !
               !                                            !
               !                                            !
               !                                            !
               !                                            !
               !             Ribbon cable to                !
               !               Winchester drive         +--+!
         ------!   +--+=========*  *===============!   !   +-+
              [!-- !  !                             !   !  !-
AMP header    [!-- !  ! AMP      *  *          AMP !   !   !-
assembly      [!-- !  !receptacle *  *      ribbon !   !   !-
type 1-87215-7[!-- !  !connector   *  *  connector !P1!    !- J1
or equivalent [!-- !  !type        *  *       type !   !   !-
              [!-- !  !88377-6     *  *    88373-3 !   !   !-
              [!-- !  !or equiv.   *  *  or equiv. !   !   !-
              [!-- !  !                            !   !   !-
              [!-- !  +==============*  *==========!   !   +-+
         ------!   +--+       34-pin ribbon cable   +--+    !
               !                                            !
 --------------+                                            +-----------
```

Figure 2-18 Control and Data Cabling

2.13 CLOCK AND ANALOG INTERFACE BOARD

This subsection describes the operations of the clock and analog interface board. This board contains logic for interfacing a light pen to the computer system and a ROM, which is programmed with the driver routines for the board.

2.13.1 Description

The board is composed of three separate and distinct sections: The analog input section, the real-time clock section, and the light pen section. The system block diagram is shown in Figure 2-19, and the timing diagram in Figure 2-20.

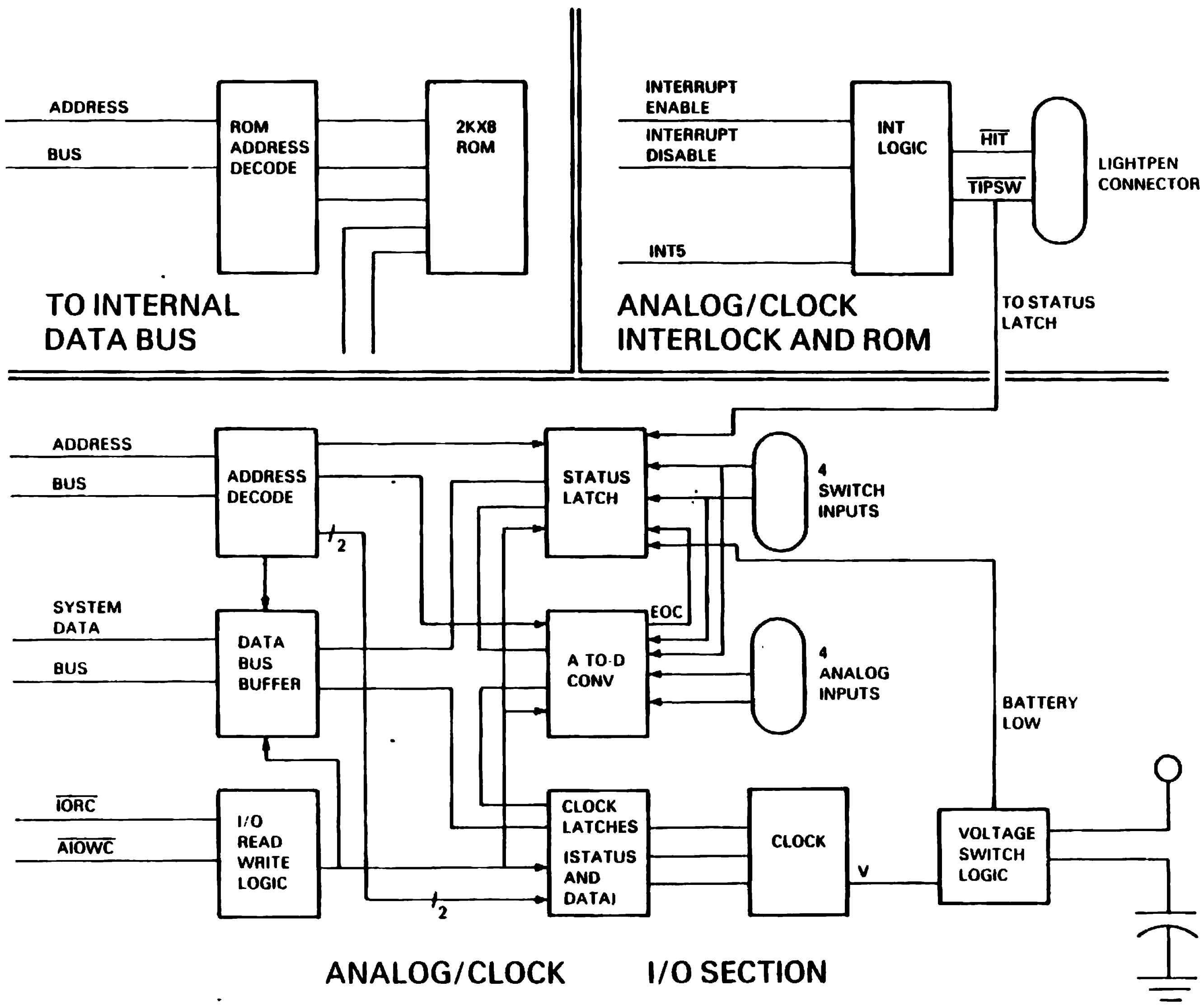
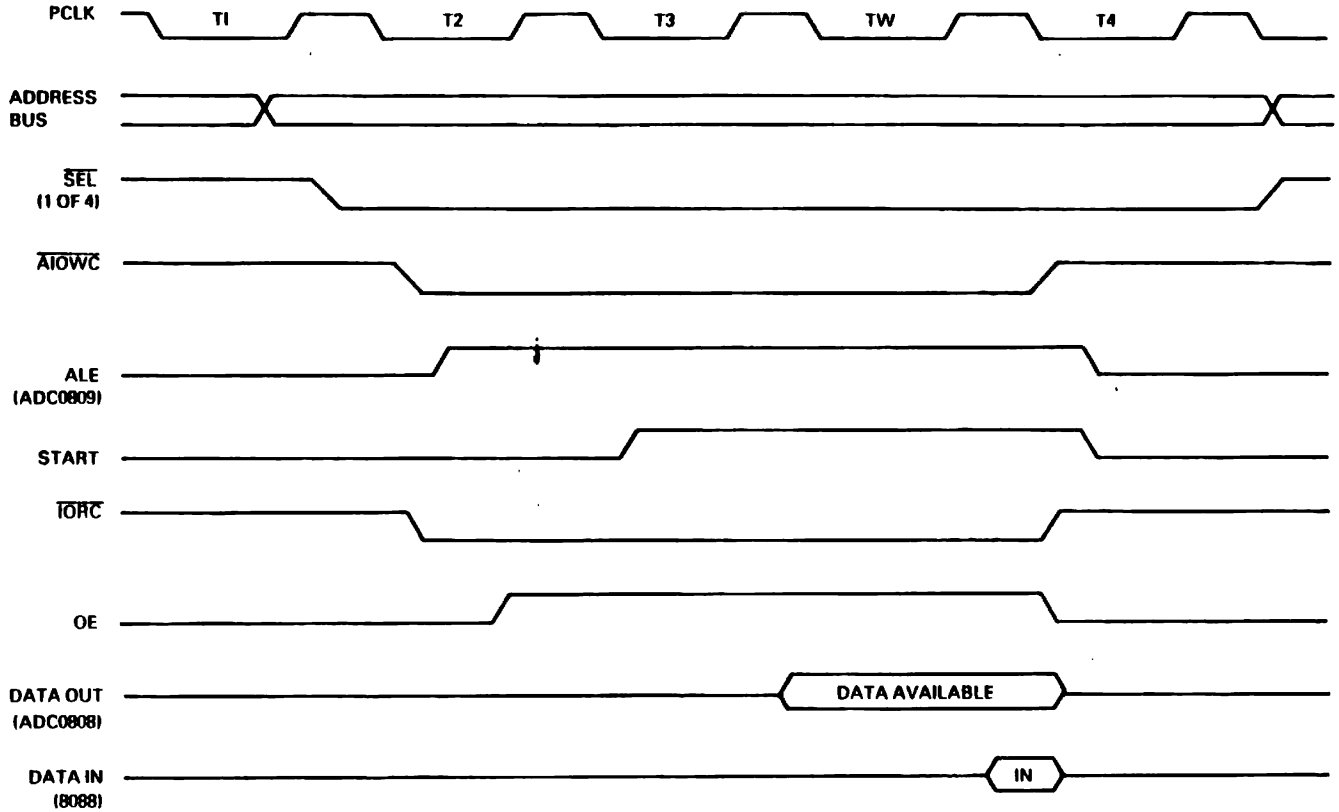


Figure 2-19 Clock and Analog Interface Block Diagram



CLOCK AND ANALOG INTERFACE TIMING DIAGRAM

Figure 2-20 Clock and Analog Interface Timing Diagram

2.13.2 Analog Input

The analog input converter section is basically designed as a game controller. Allowable game controller configurations include one or two joysticks, up to four paddle controllers, and up to four switches. The switches SW1-SW4 are semi-debounced by the simple resistance-capacitance (RC) circuit consisting of a 0.047-uF capacitor to ground and a 1-kohm resistor to +5 V. The switch signal is fed into the status latch along with an end of conversion (EOC) signal from the analog to digital converter (ADC) and the low battery signal from the clock section. The outputs of the status latch U8 are tri-stable. The (tri-stated) outputs are allowed to follow the inputs until the latch is selected by an access to location C0H. The latches are continued in a high-impedance state until the I/O read signal is asserted. This prevents the contents of the latch from being gated onto the bus during a memory cycle. The latch also contains a bit indicating the state of the light pen interrupt signal and a bit indicating the state of the tip switch on the light pen.

The ADC used is an eight input channel ADC0808. This part can multiplex eight analog input signals into one selected digital output signal. The analog channel is selected by a write into location C8H-CFH. This write also generates the timing required to run the ADC0808. First, the inverted falling edge of the AIOWC- signal (near the start of the cycle) clocks the state of the ADCSEL- signal to the Q- output of U7A. Therefore, the ADCSEL- signal goes high only during a write to a location in the ADCSEL- address space. This signal is used to generate ALE to the ADC0808. This signal is also tied to the D input of U7B. This is clocked through about 100 ms later on the next falling edge of PCLK from the system bus. The signal generated by U7B is the START signal for the ADC0808. Both U7A and U7B are set to a low output on the first high clock after AIOWC- goes inactive.

From this point on, the conversion is automatic. It takes less than 70 us to complete the conversion, at which time the EOC signal is raised. The state of this signal can be monitored by reading the status latch U8.

NOTE

> The EOC signal should not be considered valid until 4 us after the write to the ADC0809. The EOC signal is normally high, and does not go low until that length of time after receiving the convert command. Once the conversion is indeed complete, the data can be read from location C8H.

To initialize the analog to digital conversion from the four analog inputs, write to the locations indicated for the corresponding analog input channel.

Channel 0 (X1): Write to C8H.
Channel 1 (Y1): Write to C9H.
Channel 2 (X2): Write to CAH.
Channel 3 (Y2): Write to CBH.

For extra flexibility, the switch inputs are also connected to the inputs of the ADC. This means another four analog channels are available to the user if the switches are not present. (Although the switch state can be read by converting the proper channel, this technique takes much longer than reading the status latch.) The conversion addresses for the switch input lines are as follows:

Channel 4 (SW4): Write to CCH.
Channel 5 (SW3): Write to CDH.
Channel 6 (SW2): Write to CEH.
Channel 7 (SW1): Write to CFH.

The ADC is used for two different types of conversion. Channels 0, 1, 2, and 3 are used as current-sensing converters. U25 converts a current input level to a voltage output, which is fed to the inputs of the ADC. Channels 4, 5, 6, and 7 are used as straight voltage inputs. Therefore, the user has a choice of analog current inputs or analog voltage inputs. Most joysticks are set up as current-controlling devices. Switches are both voltage- and current-controlling devices.

2.13.3 Clock

The most complex section is that used to control the clock, U14. Due to speed limitations, this part must be set up in a series of steps. The parameters used to set up the clock are stored in latch U10. U10 is located at I/O space D0H. Data to be written to the clock is stored in latch U11. U11 is located at I/O space D8H. The following examples help explain the operations involved.

2.13.3.1 Operation. To write data to any one of the clock's internal registers:

1. Write the byte 1X to location D0H. This raises the HOLD line and leaves the rest of the control lines low. The bottom four bits of this control word contain the specific address within the clock. The clock set-up addresses are given in Table 2-32.

Table 2-32 Clock Set-Up Addresses

Address	Register	Meaning
x0	S1	Units of seconds
x1	S10	Tens of seconds
x2	Mi1	Units of Minutes
x3	Mi10	Tens of minutes
x4	H1	Units of hours
x5	H10	Tens of hours d2=1 for PM, d2=0 for AM d3=1 for 24 hr format d3=0 for 12 hr format
x6	W	Week
x7	D1	Units of days
x8	D10	Tens of days d2=1 for 29 days in month 2 d2=0 for 28 days in month 2
x9	Mo1	Units of months
xA	Mo10	Tens of months
xB	Y1	Units of years
xC	Y10	Tens of years

2. Write the data for the data registers in the clock to location D8H.

3. Wait for at least 150 us. This is the MINIMUM allowed set-up time. To be safe, wait for from 200 to 250 us (to correct any hidden timing problems in the software wait loops).

4. Write the byte 3X to location D0H. Note that this X is the same as that in step 1. This byte continues the state of the address lines and the HOLD line, while raising the WRITE line to the clock.

5. Wait for at least 1 us (about two instruction cycles - try using two NOPs (NO OPERATION - assembly language steps) in the code after step 4).

6. Write the byte 1X to location D0H. This lowers the WRITE line, but keeps all other lines in the same state.

7. For another write, wait for 1 us (2 NOPs), write 1Y to location D0H (where Y is the new address), write the new data to port D8H, wait for 0.5 un (1 NOP cycle), and return to step 4. If this was the last write, go to step 8.

8. Write the byte 00 to location D0H. This lowers the HOLD

line and completes the cycle.

Once set, the clock should not require resetting more than once or twice a year.

To adjust time by 30 seconds:

1. Write 80H to location D0H.

2. Wait for 32 ms.

3. Write 00 to location D0H.

Refer to the MSM5832 data sheets for details on this feature.

To read any register on the clock:

1. Write 1X to location D0H. This raises the HOLD line. X indicates the address to be read. Refer to Table 2-33.

2. Wait at least 150 us.

3. Write 5X to location D0H. This maintains the HOLD line, and raises the READ line. This is the same X as that in step 1.

4. Wait for at least 6 us.

5. Read from location D8H. The valid data is in the bottom four bits of the byte returned.

6. To perform another read, pick the new address for X and go to step 3. If this was the last read, write 00 to location D0H.

It can readily be seen that the read is much easier than the write. This is good, because a read is performed at least once during every system power-up.

2.13.3.2 Battery Backup. The clock is a CMOS device and has battery backup. The CS input on the clock is connected to Vcc. The function of this pin is to put the clock into the powerdown mode. When the power supply voltage goes down, the CS pin is grounded. This forces the clock into the powerdown state, at which time it draws power from the battery BT1. This 3-V lithium battery is rated at 170 milliampere-hours (mAH). At the low current levels and the given typical system on-times, it should provide backup power for several years. The battery is a GE 2320 or equivalent. This battery fits into a battery holder on the clock and analog interface board Replacement batteries of this type are available at many retail electronics outlets. The GE battery is UL listed.

NOTE

Care must be taken to ensure that the operating conditions specified by the battery manufacturer are met. Read and follow the instructions furnished with the battery.

The diode D1 is a low-voltage-drop diode used to isolate the battery from the system during power-up. The circuit Q1-Q2 isolates the rest of the system from the battery during periods of powerdown. This set-up prevents the battery from being back-biased during power-up and prevents it from trying to power the entire system during powerdown times.

The comparator changes state from high output to low output when the battery voltage drops below 2.6 V during power-up. The low battery signal is latched into the status latch and should be checked occasionally so that the operator can be flagged during low-battery-voltage operation.

For the safety of factory personnel and the end user, the lithium battery is not connected until after the board has been tested sufficiently to assure that no defects exist in the battery switching circuitry. Once the tests are completed, a jumper is installed connecting E8 to E9. This adds the battery to the rest of the board, and makes the board ready for use.

2.13.4 Light Pen

The light pen section is by far the simplest, consisting only of a single NOR gate and an interrupt latch. When the tip of the pen is depressed, the signal TIPSW- goes low. When the light detector in the tip of the light pen is activated by the CRT beam, the signal HIT- goes low. These signals are applied to the inputs of NOR gate U4A. The output of U4A is the INT signal. This signal is active only when the TIPSW- and the HIT- signals are both active (low). The INT signal is positive-true. The rising edge of INT is used to clock a TRUE signal to the output of flip-flop U17A. This signal (INTFF) is used to interrupt the processor. The interrupt is software switchable to be either tri-stated or active on INT5. The interrupt is tri-stated by a read from I/O location C1H. The interrupt is turned on (allowed) by a read from I/O location C2H. The access to location C1H clears flip-flop U17B. Accesses to location C2H set the flip-flop. The output of this flip-flop is tied to the control input of tri- state buffer U21A. Note that allowing the interrupt does not necessarily mean making the interrupt line high. Also, the status of the interrupt latch may be polled by an access to the status latch The interrupt flip-flop is cleared by a processor access to I/O location C0H. This INT signal (clock for U17A) is also cabled to the connector provided on the CRT controller board for light pen signals by header pins E1 and E2. Both pins provide the INT signal.

2.13.5 Connectors

On the back of the board are two connectors, a 9-pin and a 15-pin, D-type subminiature connector. The 9-pin connector connects the light pen and the 15-pin connects the analog/button inputs. A pin-out of each connector is given in Table 2-33

Table 2-33 Pin-out - Analog Interface

1. 15-pin, D-type subminiature connector J1

Pin	Signal	Pin	Signal
1	+5 V	9	+5 V
2	SW1	10	SW3
3	ANA1	11	ANA3
4	GND	12	GND
5	GND	13	ANA4
6	ANA2	14	SW4
7	SW2	15	+5 V
8	+5 V		

2. 9-pin, D-type subminiature connector J2

1	GND	2	GND
3	HIT-	4	TIPSW-
5	CHASSIS GND	6	GND
7	+5 V	8	+12 V
9	NC *		

* Not connected

2.13.6 ROM

This board contains a 2K x 8-bit ROM, which is programmed with all of the necessary driver routines. The ROM can be accessed by the system controller and provides the software necessary to drive the clock and analog input devices. This device can be replaced with a 4K or 8K device by cutting and jumpering on the printed wiring board. The ROM is located at F4000H.

Section 3

DEVICE SERVICE ROUTINES

3.1 ROM INTERFACE INFORMATION

This section provides the hardware and software designer with information on writing software for compatibility with future products and on interfacing with the hardware of the Texas Instruments Professional Computer. The interface information includes interrupt vectors, system memory maps, and ROM usage. The system ROM contains instructions for hardware device control of the principal I/O devices in the system unit.

The functions described are implemented with code in the system ROM, and thus are available to all users of the system regardless of which disk operating system (DOS) is in use. The user must be careful, however, to avoid causing any conflicts with the operating system's use of these same functions.

These functions are typically accessed through the use of the 8088 software interrupt mechanism. Each major device service routine (DSR) such as keyboard, display, and disk, has its own unique vector. Individual functions of a DSR are accessed by placing an "opcode" in register AH and executing an INT (interrupt) instruction of the applicable type. This scheme allows easy replacement of all or part of any of the DSRs by simply patching the interrupt vector to point to the user-written code. An example of this is the manner in which MS-DOS adds support for a serial printer .

3.2 WRITING SOFTWARE FOR COMPATIBILITY WITH FUTURE PRODUCTS

The software you develop for this product undoubtedly represents a large investment of your time and money. Making changes and releasing new versions of software is usually difficult and expensive, and should be avoided. This guide is provided to help you in creating software that can be used with future hardware products of Texas Instruments.

3.2.1 Compatibility Levels

In order for the software to work on more than one hardware product, there must be compatibility at certain levels. The following are compatibility levels:

3.2.1.1 Operating System. Software that interfaces at the operating system level is compatible only with products of other manufacturers using the same operating system. These products may include those of other manufacturers.

3.2.1.2 System ROM Interface. Software that interfaces with the Texas Instruments-supplied system ROMs through the interface vectors is compatible with hardware products having the same functional characteristics. These products may differ in physical or electrical characteristics from the standard Texas Instruments product. Programs compatible at this level or at the DOS level are more likely to be compatible with future products.

3.2.1.3 Hardware Interface. Programs that use the hardware directly (for example, input or output to hardware addresses), are least likely to be usable in another Texas Instruments Professional Computer system.

3.2.2 Areas of Hardware Compatibility

Texas Instruments recognizes that the system ROM interface is not sufficient for all applications. Products using the advanced capabilities of the hardware cannot be restricted to usage of this interface. The following subsections describe the hardware compatibility that can be expected in future subsystems or subsystems accessed from ROM only.

3.2.2.1 Alphanumeric CRT. The alphanumeric CRT is well supported by the system ROM. It may be desirable to have the program access the screen directly in order to speed processing or to implement windows or horizontal scrolling. Direct screen access to the alphanumeric CRT screen should be restricted to the "attribute latch" and to the actual memory buffer for the screen located at hexadecimal address ODEOOOH (the "H" represents hexadecimal). Before using the screen directly, these programs should issue a Clear Screen function call to ensure that the hardware is set up for direct access.

No program, while using the screen directly, should use the ROM functions to put any data on the screen. Undesirable hardware functions can occur.

All operations on the cursor should use the ROM interface calls. This will ensure that possible redesigning of the cursor logic does not prevent the program from running.

3.2.2.2 Graphics CRT. The graphics screen is not supported by the system ROM; therefore, all graphics screen functions must go directly to the hardware. Note that this graphics screen size depends on the setting of the 50-Hz/60-Hz jumper on the system board. With the jumper set to 60 Hz, the resolution is 720 x 300; when the jumper is set to 50 Hz, the resolution is 720 x 350.

To simplify modification, all routines that access the graphics hardware should be arranged in a modular fashion, and hardware-specific constants should be given symbolic names.

Texas Instruments will endeavor to keep future graphics hardware fully compatible, or as a superset of the current hardware.

3.2.2.3 Disk Subsystem. The disk subsystem is fully supported in the system ROM, with the exception of the ability to FORMAT floppy disks. For normal operations, direct access to any of the disk hardware should not be necessary. Texas Instruments will supply qualified software vendors with an object module that can be used to provide the format function.

3.2.2.4 Keyboard System. The keyboard system is fully supported in the system ROM. Direct access to the keyboard interface should not be necessary for any normal operations. Future keyboard scan codes and their translations will maintain such compatibility.

3.2.2.5 Interrupt Controller. The interrupt controller system is used by the system ROM but is not supported in a fashion usable by software writers. In future products, Texas Instruments will attempt to keep the same interrupt levels, usage, and hardware addresses for accessing the device. However, the constants used to access this hardware should be symbolic to facilitate modification.

3.2.2.6 System Timers and Speaker. The system ROMs contain vectors to allow interception of the 25-ms timer interrupts by other software. The extra timer cannot be set up and used because it is reserved for use by Texas Instruments software products.

The speaker or bell is well-supported by the system ROM and should not be accessed directly .

3.2.2.7 Parallel Printer Port. The parallel printer port system is fully supported in the system ROM. Direct access is available during normal operations.

3.2.2.8 Serial Communications. The serial communications hardware is not directly supported by the system ROM. To ensure future compatibility, Texas Instruments does not intend to change this hardware.

3.2.2.9 Analog Interface. The analog interface adapter is supported by its ROM. Direct access to the adapter interface hardware should not be necessary for normal operations.

3.3 SYSTEM ROM INTERRUPT VECTOR USAGE

The system ROM uses several interrupt vector locations in the first 1 kbyte of memory. These vector locations are used for hardware interrupts, interfaces to the ROM functions, and other usage as given in Table 3-1. The vectors marked with an asterisk (*) are actually used by the ROM. The other vector locations cause a "WILD" interrupt if vectored to, and the usual display will be "** SYSTEM ERROR ** - 1042". Any of these vectors can be changed by the disk operating system (DOS) or by applications software. Table 3-1 gives vector usage in terms of "interrupt type," which is the number used in an INT instruction. The actual absolute address of the vector can be calculated by multiplying the interrupt type by 4. For example, the keyboard print screen interrupt vector (type 5EH) would be a double word at 0:0178H.

NOTE

The symbol "H" denotes a hexadecimal value.

Table 3-1 System Interrupt Vector Usage

VECTOR	DESCRIPTION	REFERENCE FOR DETAILS:
00	Divide-by-zero trap	8088 documentation
01	Single-step trap	8088 documentation
02*	Non-maskable interrupt	8088 documentation
03	Break (single-byte) software interrupt	8088 documentation
04	Overflow trap	8088 documentation
05-1F	(Reserved by Intel)	8088 documentation
20-3F	(Reserved by Microsoft for MS-DOS)	MS-DOS documentation
40	8259 interrupt 0	
41	8259 interrupt 1	
42	8259 interrupt 2	
43*	8259 interrupt 3 (Timer 1)	
44	8259 interrupt 4	
45	8259 interrupt 5	
46*	8259 interrupt 6 (Disk controller)	
47*	8259 interrupt 7 (Keyboard USART)	
48*	Speaker DSR interface	Subsection 3.5
49*	CRT DSR interface	Subsection 3.7
4A*	Keyboard DSR interface	Subsection 3.9
4B*	Parallel port DSR interface	Subsection 3.10
4C	Clock and analog interface board	
4D*	Disk DSR interface	Subsection 3.8
4E*	Time-of-day clock DSR interface	
4F*	System configuration call	Subsection 3.1
50*	Fatal software error trap (**)	
51*	Restart timing event (**)	
52*	Cancel timing event (**)	
53*	SVC interface subroutine (**)	
54*	Activate task subroutine (**)	
55-56	(Reserved for future use) (**)	
57*	CRT mapping vector	Subsection 3.7
58*	System timing, 25 ms (time slicing)	Subsection 3.3.2
59*	Common interrupt exit vector (ROM)	Subsection 3.3.1
5A*	System timing, 100 ms (timing serv.)	Subsection 3.3.2
5B*	Keyboard mapping vector	Subsection 3.11.15
5C*	Keyboard program pause key vector	Subsection 3.11.15
5D*	Keyboard program break key vector	Subsection 3.11.15
5E*	Keyboard print screen vector	Subsection 3.11.15
5F*	Keyboard queueing vector	Subsection 3.11.15

* Vector actually used by ROM.
** Texas Instruments only.

Table 3-1 System Interrupt Vector Usage (Continued)

VECTOR	DESCRIPTION			REFERENCE FOR DETAILS
60	System ROM	DS Pointer	(180H)	Subsection 3.4
	(F400:A000)	DS Size	(182H)	Subsection 3.4
61	Factory ROM	DS Pointer	(184H)	Subsection 3.4
	(F400:0000)	DS Size	(186H)	Subsection 3.4
62	Option ROM	DS Pointer	(188H)	Subsection 3.4
	(F400:2000)	DS Size	(18AH)	Subsection 3.4
63	Option ROM	DS Pointer	(18CH)	Subsection 3.4
	(F400:4000)	DS Size	(18EH)	Subsection 3.4
64	Option ROM	DS Pointer	(190H)	Subsection 3.4
	(F400:6000)	DS Size	(192H)	Subsection 3.4
65	Option ROM	DS Pointer	(194H)	Subsection 3.4
	(F400:8000)	DS Size	(196H)	Subsection 3.4
66	Memory size (in paragraphs)			Subsection 3.5.1
	Outstanding interrupt count (in paragraphs)			Subsection 3.5.1
	Installed drive types (byte)			Subsection 3.5.1
67	Extra system configuration (config. word 1)			Subsection 3.5.2
*	Extra system configuration (config. word 2)			Subsection 3.5.2
E0-E3***	(Reserved by Digital Research for CP/M)			CP/M documentation

* Vector actually used by ROM.
*** CP/M is a trademark of Digital Research Incorporated.

NOTE: The data segment (DS) pointers associated with the system interrupt vectors are explained in subsection 3.4, "System ROM Usage of RAM."

3.3.1 Common Interrupt Exit Vector

All interrupt service routines in the ROM and Texas Instruments Applications programs use this common exit by executing a long jump (LONG JMP) to the routine pointed to by this vector. This routine restores the stack and commonly used registers, decrements the outstanding interrupt counter, sends the EOI command to the interrupt controller, and returns to the interrupted code with an IRET. This routine is normally in ROM, but a real-time operating system (OS) can patch it so that all interrupt service routines exit through the operating system. Since the interrupt structure is complex (due to interaction between the shared interrupts and the requirement for a common exit point), the potential user should contact Texas Instruments prior to installing an interrupt service routine.

Since all interrupt service routines (ISR) have limited internal stacks, no ISR is allowed to use more than four levels (8 bytes) of stack. Three levels are required by the interrupt itself, which pushes the CS, IP, and Flags. The fourth allowed level is used to push the users DS, after which SS:SP is changed to an internal stack. For this reason, any limited-size stacks must always leave at least four levels free (if interrupts are enabled) to accommodate a possible interrupt.

3.3.2 Timer Interrupts

The system timer "ticks" every 25 ms. The ISR for this timer is located in the ROM, and it processes events such as disk motor time-outs and date/time-keeping. At two points during this interrupt service routine, software interrupts are performed to allow the user to access the timing services. One interrupt occurs every count (every 25 ms), and the other occurs every four counts (100-ms intervals). Normally, these interrupt vectors point to an IRET instruction in the ROM. The user can patch one or both of the vectors to point to his own routines. These routines are free to use the AX, BX, DI, and ES registers, but they must preserve any other registers used. The stack used is the internal stack of the timer interrupt service routine and it is limited in depth. If the user does not re-enable interrupts (the INT instruction disabled them), there are eight levels (16 bytes) of stack available. If the interrupts are re-enabled, the user has only four levels (8 bytes) available. If more stack size is required, the user can switch to an internal stack of the required size (plus eight bytes to allow for higher priority interrupts).

It must be remembered that any routines installed in this manner are executing at the interrupt level, and interrupts must not be disabled for any length of time. Any unnecessary time spent in these routines will directly affect system efficiency. Further, the user must comprehend the case in which some other mechanism (such as a timing event in the handler or "routine" in the operating system) has patched the timing vectors and installed its own routines. Instead of ending the routine with an IRET instruction, a long jump should be made to the original vector address (the original vector must be saved when the user routine is installed.)

3.4 SYSTEM ROM USAGE OF RAM

The two (8K) ROM sockets on the system unit board are addressed at absolute addresses FC000H (option) and FE000H (main). Because the ROM code is linked such that its code segment is F400H, the first location of the system ROM can be described in segment:offset notation as F400:A000H. This code segment was chosen so that other ROMs can be addressed with the same code segment as the system ROM, and thus, they can access the ROM routines as NEAR instead of FAR. This feature would typically be used only by an option ROM program that uses more than one ROM. It should not be used to access system ROM routines, since possible version changes in the ROMs could cause incompatibility problems. The ROM code defines a total of six possible ROM locations on 8-kbyte boundaries, which are given in Table 3-2. The last two are the system unit board sockets; the others are on option boards For example, the Winchester disk controller has its own ROM.

Table 3-2 ROM Locations

ABSOLUTE ADDRESS	CODE SEGMENT	COMMENTS
F4000H	F400:0000H	Reserved for factory use
F6000H	F400:2000H	
F8000H	F400:4000H	
FA000H	F400:6000H	
FC000H	F400:8000H	Option ROM socket on system unit board
FE000H	F400:A000H	System ROM socket on system unit board

Each ROM has a separate RAM data area assigned to it. These data areas "float" and may be accessed by the pointers/sizes located in the interrupt vector area (the first 1 kbytes of memory described previously). Therefore, the ROM does not need a dedicated area in RAM. The data area can be moved by copying a data area and updating the pointer. The ROM never sees the change, since each ROM accesses its data areas according to the pointers. Because the pointers and data areas are initialized at boot time by the ROMs themselves, in a base system only the system ROM data area pointer is used. Most application programs do not require this information, which is primarily used by the operating system. Contact Texas Instruments for additional information if you need to use a ROM or move the ROMs' data areas.

In the current implementation, the system ROM data area is about 400 bytes located at 40:0000H. This is moved at MS-DOS boot time to its final location at 120:0000H.

3.5 SYSTEM CONFIGURATION FUNCTION CALLS

This subsection describes the system configuration function calls. There are two separate types of configuration information.

The first type is easily accessed and returns most of the information required for most applications programs. The second type is additional information usable for systems programs and routines. There are two methods for accessing each type of information.

* Function calls that return the information in a register.

* Function calls that return the address of the information. This method is intended for use at the system level for changing the configuration of devices set by software.

3.5.1 System Configuration Function

This function is used to determine the installation status of certain system options. It is invoked by executing an INT 4FH instruction.

Upon return, register BX contains the size of contiguous RAM (starting at 00000H) in paragraphs (16-byte blocks). A 128-kbyte system, for example, would return 2000H in BX.

Register AX contains the system configuration word, which reflects the installation status of various system options. The bits of the word are defined as given in Table 3-3.

Table 3-3 System Configuration Word-Bit Definition

BIT	DEFINITION
0*	Diskette drive 0 (internal) installed
1	Diskette drive 1 (internal) installed
2	Diskette drive 2 (external) installed
3	Diskette drive 3 (external) installed
4	E1-E2 jumper (indicates Drive A is double-sided)
5	E3-E4 jumper (indicates Drive A has 96 tpi)
6	E5-E6 jumper (indicates a 50-Hz system)
7	Winchester disk controller installed
8	Serial Port 1 installed
9	Serial Port 2 installed
10	Serial Port 3 installed
11	Serial Port 4 installed
12	Graphics RAM bank A installed
13	Graphics RAM bank B installed
14	Graphics RAM bank C installed
15	Clock/analog board installed

* Bit 0 is the least-significant bit, and a statement is true if its corresponding bit is a 1.

3.5.2 Extra System Configuration Function

This function is used to determine the installation status of system options not covered in the standard system configuration call. Whereas the standard system configuration call returns a word containing the information necessary for most applications, the extra system configuration function is used primarily for systems programming applications.

The extra system configuration function is invoked by placing a 0BH in register AH and executing an INTerrupt 48H. Upon return, register AL contains the drive type byte (AH is undefined). BX contains extra system configuration word 1, and CX contains extra system configuration word 2. The bits of extra system configuration word 1 are defined in Table 3-4.

Table 3-4 Extra System Configuration Word 1 (BX)

BIT	DEFINITION
0*	8087 Numeric Coprocessor is installed
1	\
2	!
3	!
4	> RESERVED
5	!
6	!
7	/
8	
9	!
10	!
11	!
12	> RESERVED
13	!
14	!
15	/

* Bit 0 is the least-significant bit, and a statement is true if its corresponding bit is a 1.

Word 2 (in CX) is currently undefined, but is reserved for later expansion.

The drive-type byte defines the types of the installed diskette drives. This information, combined with the "installed drive" vector in the standard system configuration word, yields complete information about the drives in the system. At power-up, the drive A definition jumpers (E1 - E2 and E3 - E4) are read. This information is returned as a two-bit value. Register AL contains the two-bit configuration code for all four of the diskette drives. The drive byte (in AL) looks like this:

7	6	5	4	3	2	1	0
Drive D		Drive C		Drive B		Drive A	

Each two-bit field is defined as follows:

0	0	-	Single-sided 40 track
0	1	-	Double-sided 40 track
1	0	-	Single-sided 80 track
1	1	-	Double-sided 80 track

The operating system uses this drive byte to properly format, copy, and use diskette files. It is possible to mix drive types in one system (for example, one single-sided and one double-sided drive) by setting the drive-type byte with the pertinent information; but, this is NOT recommended. Mixed-drive type systems are confusing to work with, and users frequently find the wrong diskettes inserted, often with data lost.

3.5.3 Get Pointer to System Configuration

This function is invoked by placing a 09H in register AH and executing an INTerrupt 48H. On return, ES contains the segment, and BX contains the offset of the standard system configuration word (hereafter, the notation for this is ES:BX). This function is intended to be used by system software, which has a need to change the configuration information. Although an application program may access the information in this manner, the configuration must not be changed.

3.5.4 Get Pointer to Extra System Configuration

This function is invoked by placing a 0AH in register AH and executing an INTerrupt 48H. On return, ES:BX points to the extra system configuration information, formatted as follows:

```
ES:[BX-3]=(word) Size of memory in 16 byte-blocks
ES:[BX+0]=(byte) Drive-type byte
ES:[BX+1]=(word) Extra system configuration word 1
ES:[BX+3]=(word) Extra system configuration word 2
```

This function is intended to be used by system software that has a need to change the configuration information. Although the an application program can access the information in this manner, the configuration must not be changed.

3.6 GENERAL-PURPOSE ROM FUNCTIONS

The following paragraphs describe the use of some general-purpose functions, summarize the ROM interface interrupts, and explain ROM's usage of RAM.

3.6.1 Delay

This function causes a delay, in milliseconds, of the value placed in register CX. To invoke the function, place the delay value in CS, 05H in AH, and execute an INT 48H. The delay is only approximate and may be used wherever a rough software delay is required. All registers except CX are preserved.

3.6.2 CRC Calculation

This function calculates the cyclic redundancy check (CRC-16) value for a specified block of memory. It is invoked by placing the address of the memory block in ES:BX, the size of the block in BP, and the value 06H in AH, then executing an INT 48H. On return, DX contains the CRC value; if DX=0000, the Z-flag is set. For memory blocks that follow the convention of the CRC being the last word in the block, this routine allows easy CRC checking. First, the CRC of the memory block is calculated, with the size of the block set to 2 less than the actual size. The CRC word is then written to the last word of the block. Subsequently, the CRC of this block may be checked by calling this function with the actual size of the memory block (including the previously calculated CRC). By definition, the CRC result of this block is zero (if the CRC matches the data) and the Z-flag is set; otherwise, the CRC fails and the Z-flag is reset. All registers are used except DI, SI, and DS (ES remains unchanged.)

3.6.3 Print ROM Message

This function is used to display a ROM CS-relative message. It is invoked by placing the offset of the zero-terminated message in SI, 07H in AH, and executing an INT 48H. This function is used by the option ROMs, since all the ROMs share a common CS. It is not a general-purpose routine.

3.6.4 Display System Error Code

This function is used to display a system error in the standard format

** System Error** - xxxx

It is invoked by placing the error code (the xxxx value in the displayed message above) in BX, placing the value 08H in AH, and executing an INT 48H.

3.7 SPEAKER DEVICE SERVICE ROUTINE

This subsection describes the speaker device service routine (DSR) and the functions it provides to the system or application programs that use it. The functions are:

* Sound the speaker
* Get speaker status
* Set speaker frequency
* Speaker ON
* Speaker OFF

The speaker DSR functions are located in the system ROM and are accessed through the software interrupt mechanism of the 8088 microprocessor. The desired function is chosen by placing an opcode in register AH and executing an INT 48H instruction. All registers are preserved except AX.

3.7.1 Sound the Speaker - AH = 0

This function turns the speaker on (at the current frequency) for the length of time specified in register AL. Time is measured in 25-ms increments. For example, a value of 40 in AL causes the speaker to sound for 1 second. Timing is handled in the ROM with the result that the request turns on the speaker, starts the timer, and immediately returns to the user. The sound continues until timed out by the ROM code. If there is need to synchronize with the sound or simply to know when sound is turned off, use the Get Speaker Status (AH=1) function.

3.7.2 Get Speaker Status - AH = 1

This function returns the status of the speaker in the Z-flag. If the speaker is currently enabled (sound), the Z-flag is 0. If the speaker is currently disabled (no sound), the Z-flag is 1. This function can be used to find out when a sound requested with the Sound the Speaker (AH=0) function has been completed.

3.7.3 Set Speaker Frequency - AH = 2

This function sets the frequency of the speaker. Normally this function should be called only when the speaker is disabled. The value in CX is used to set the frequency of the timer that drives the speaker. The input frequency of the timer is 1.25 MHz, and the value in CX is used as a divider for this frequency. For example, the system beep routine (800 Hz) uses a value of 1563 Hz (1 250 000 Hz / 800 Hz = 1563 Hz).

3.7.4 Speaker ON - AH = 3

This function is used to enable the speaker (turn on the sound). The speaker remains on until it is turned off by either (1) the Speaker OFF (AH=4) function or (2) by the ROM timing routine, as a result of either the Sound the Speaker (AH=0) function or a normal system beep.

3.7.5 Speaker OFF - AH = 4

This function performs the reverse of the speaker ON (AH=3) function by disabling the speaker (turning off the sound).

3.8 TIME-OF-DAY CLOCK DSR

This subsection describes the time-of-day clock DSR and the functions it provides to the system or application programs that use it. The functions are: (1) set the date, (2) set the time, and (3) get the date and time.

The clock DSR consists of routines to set and read the time of day and date information kept by the timing services of the system ROM. At power-up, the time is set to 00:00:00.00, and the date is set to 0000. These can be reset by system or user programs. Once set with a valid time, the clock keeps the correct time with a 1/10-sec resolution. The time is kept in 24-hr format and the date is simply a cumulative count of days since the clock was started. As a matter of convenience (for MS-DOS), the date is specified as the number of days since January 1, 1980. For example, the date value for September 10, 1982, is 983.

The three clock functions are located in the system ROM and are accessed through the software interrupt mechanism of the 8088 microprocessor. The desired function is chosen by placing an opcode in register AH and executing an INT 4EH instruction. All registers are preserved except AX and any other registers in which information is returned.

3.8.1 Set the Date - AH = 0

This function sets the date to the value in the BX register. The date is simply a count of days since the clock was started. The count is incremented when the hour rolls over from 23 to 00.

3.8.2 Set the Time - AH = 1

This function sets the time as follows:

CH = Hours (00 - 23)
CL = Minutes (00 - 59)
DH = Seconds (00 - 59)
DL = Hundredths of seconds (00 - 99)

It is the user's responsibility to make sure the values passed are within the ranges specified. These values are not range checked and may be set to represent a meaningless time. The time eventually counts into the normal sequence, however.

3.8.3 Get the Date and Time - AH = 2

This function returns the current date in register AX and the current time in registers CX/DX in the formats described previously.

3.9 CRT DSR

This subsection describes the CRT DSR and the functions it provides to the system or application programs that use it. The major functions are (1) video mode control, and (2) character handling.

The CRT DSR functions are located in the system ROM and are accessed through the use of the 8088 software interrupt mechanism (essentially an address-independent subroutine call). The typical user of this DSR would be the OS-dependent BIOS, which resides on a particular OS disk and is loaded into RAM during disk boot. The desired function is chosen by placing an opcode in register AH. The CRT opcodes and functions are given in Table 3-5. Various CRT functions require parameters to be passed in specific registers in addition to AH. Once register AH and the parameter registers are set up, the user can execute an INT 49H and the specified function is performed. During this interrupt, all registers are preserved except AX, CX, and DX.

Table 3-5 CRT DSR Opcodes and Functions

OPCODE	FUNCTION
00H	(Null function)
01H	Set cursor type
02H	Set cursor position
03H	Read cursor position
04H	(Null function)
05H	(Null function)
06H	Scroll text block
07H	Scroll text block
08H	Read character and attribute at current cursor position
09H	Write character and attribute at current cursor position
0AH	Write character only at current cursor position
0BH	(Null function)
0CH	(Null function)
0DH	(Null function)
0EH	Write ASCII teletype
0FH	(Null function)
10H	Write block of characters at current cursor with attribute
11H	Write block of characters only at current cursor
12H	Set entire screen to specified attribute(s)
13H	Clear text screen and home the cursor
14H	Clear graphics screen
15H	Set TTY status line beginning
16H	Set attribute latch to specified attribute(s)
17H	Read physical display begin pointer
18H	Print TTY string

3.9.1 Set Cursor Type - AH = 01H

This function allows an application to define the starting and ending scan line for the cursor and its characteristics (either blinking or no cursor). Required input for this function is described in Figure 3-1.

```
      +-------------------------------+
 CH = | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 1
      +-------------------------------+
        |   |   |  |    |   |   |   |
not used<-+  |   |  +----> bits 4 through 0 start scan line of cursor
            |   |
            +---+-------> bits 6 and 5 indicate the cursor type:
                              00 = no blink
                              01 = no cursor
                              10 = fast blink
                              11 = slow blink

      +-------------------------------+
 CL = | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte 2
      +-------------------------------+
        |   |   |  |    |   |   |   |
        |   |   |  +----> bits 4 through 0 end scan line of cursor
        |   |   |
        +---+---+-------> bits 7 through 5 not used

      (Valid values for scan line are 0 through 11 decimal)
```

Figure 3-1 Byte Definition - Set Cursor Type

3.9.2 Set Cursor Position - AH = 02H

NOTE

The user should be aware that screen coordinates are based upon the 0,0 coordinate being located at the upper left-hand corner of the display. All routines that require a coordinate parameter use this convention. The screen will look to the user as if he were working with the absolute value of fourth quadrant coordinates of a two-dimensional coordinate system.

This function causes the cursor (of the current type) to be set at the specified x,y (column/row) coordinate of the display.

Required input for this function is as follows:

DH = X (columns) coordinate (valid values are 0 through 79 decimal)

DL = Y (rows) coordinate (valid values are 0 through 24 decimal)

3.9.3 Read Cursor Position - AH = 03H

This function returns the current position and type of the cursor as shown in the output displayed. Note that, due to the "phantom" 81st column position of the cursor (see Mode Behavior, paragraph 3.7.9.10, "CRT TTY Mode Behavior"), there exists a special case of reading the cursor position. This is the case when a character has been written in the last column of the screen with a TTY write. At this moment, the cursor position can be read (it is in the 81st column of the last line, which is not visible until another character is written because the screen has not scrolled yet) and will be returned as column 0 and row 25, which is invalid input to the Set Cursor Position (AH=02H) routine. Output from the Read Cursor Position routine is as follows:

DH, DL = x, y (column/row) location of the cursor

CH, CL = current cursor type (see paragraph 3.9.1, "Set Cursor Type - AH=01H" for values)

3.9.4 Scroll Text Block - AH = 06H and 07H

The ROM contains only one general purpose "scroll" routine, which handles both upward and downward scrolls. When the destination coordinates are less than the source coordinates, the scroll is up and to the left; when the destination coordinates are greater than the source coordinates, the scroll is down and to the right.

The scrolling functions allow an application program to specify a block of text and cause it to be moved or copied to another location on the screen. Specifying a scroll with blanking causes the source text to be blanked as it is moved. The user should note that during this process the source character is read to a temporary register and its location is blanked. Then the character is rewritten to its destination location. This provides for a nondestructive move in the event that the source and destination locations are the same and blanking is specified. This implementation comes from the idea that in scrolling the user is concerned with the end result, which is that the data being moved or copied is preserved in its destination location. Required input for this function is as follows:

AL = 0 (Blank out source text) This would be a move block.
AL = >0 (Don't blank source text) This would be a copy block.

(DH, DL) = Source begin column/row location

(BH, BL) = Destination begin column/row location

CH = Column length of block (Valid values are 1 through 80 decimal)

CL = Line length of block (Valid values are 1 through 25 decimal)

The source text block boundaries in (x, y) coordinates are as follows:

Upper left = (DH, DL)
Upper right = (DH + CH , DL)
Lower left = (DH , DL + CL)
Lower right = (DH + CH , DL + CL)

The following items further describe the scrolling routines and explain the sequence of operation.

* The smallest logical block of text is considered to be a sentence. Therefore, with this scrolling capability, the user could specify a block to be a sentence. This may (or may not) wrap to a new line and "unwrap" as it is moved (or copied) to its destination (that is, the column length parameter would bypass line boundaries and pick up characters from the next line). The user should note that this is quite effective when the line length is equal to 1 but might cause unwanted block movement when the line length is greater than 1.

* Boundary checking for the scrolling routine is done on a character basis as the characters are being moved. When a scroll down is in progress, the scroll copies the last character in the source block to the last character position in the destination block. The processing is backwards through the blocks while checking character positions for out-of-bound characters. This means that in the scroll-down action, no scroll takes place if any destination position lies beyond the end of the screen. Asymmetrically, when a scroll up is in progress, the scroll copies the first character in the source block to the first character position in the destination block. The scroll proceeds forward, through the blocks, while checking character positions for out-of-bound characters. In the scroll-up action, the scroll takes place until it reaches a source character position that lies beyond the end of the screen.

* When scrolling with blanking is requested by the user, the state of the attribute latch is preserved with the same state as on entry. The attributes of the character follow the character as it is moved on the screen, and the blanked area is written with the default attributes (that is, high intensity for monochrome monitor, and white for color monitor).

* When scrolling without blanking is requested by the user, the state of the attribute latch is set to the attribute of the last character that was scrolled (that is, the attribute of the first character of the source block if scrolling down, or the attribute of the last character of the source block if scrolling up).

3.9.5 Read Character/Attribute at Cursor Position - AH = 08H

This function returns a character and its associated attribute from the current cursor position on the screen as follows. See (paragraph 3.9.9.7) "Set Attribute - AH = 16H", for a description of the attributes supported, and attribute values.

AH = Attribute value

AL = Character read

NOTE

The attribute latch is left set to the attribute that is returned.

3.9.6 Write Character/Attribute at Cursor Position - AH = 09H

This function enables the writing of a character with the given attribute at the current cursor position. (The attribute latch is left set to the attribute specified in register BL.) The user can specify a count and cause the character to be written a given number of times starting at the cursor's current position. This function does not increment the cursor automatically, and the cursor remains at its current position while the characters are written in succession from that location. If an application uses this method of writing characters, it is assumed that the application is also handling cursor positioning and, thus, no cursor movement is implemented. The user should note that control characters (CR, LF, etc.) are not executed as such when using this function and their symbols are printed on the display. The required input for this function is as follows:

AL = Character to write

BL = Attribute of character(s)
(See paragraph 3.9.9.7 "Set Attribute - AH=16H")

CX = Number of times to write it

3.9.7 Write Character at Cursor Position - AH = 0AH

This function is similar to the preceeding function except that the character being written takes on the attributes of the attribute latch which is left over from the last CRT call. See paragraph 3.9.6, "Write Character/Attribute at Cursor Position - AH=09H" for the function behavior The required input for this function is as follows:

AL = Character to write

CX = Number of times to write it

3.9.8 Write ASCII Teletype - AH = 0EH

This function allows for TTY output to the screen from application programs. Writing begins at the current cursor position, and the cursor is advanced automatically to its next position on the screen (See CRT TTY Mode Behavior, paragraph 3.9.9.10, for further details). The screen is scrolled automatically if need be (that is, writing past the end of the screen)* and the control characters CR, LF, BS, and BEL are executed instead of written. (NOTE: If a status region is currently being implemented, a scroll occurs on the line previous to the start of the status region as if that line were the end of the screen.) The characters written with this function will take on the attributes of the previously written character, since the attribute latch contents remain unchanged. The required input for this function is as follows:

AL = Character to write

3.9.9 Additional Functions

The following is a set of "extra" functions, which have been provided to give the user added screen I/O capability.

3.9.9.1 Write Block of Characters at Cursor With Attribute - AH = 10H. This function allows the user the ability to write a given block of data to the screen starting at the current cursor position. This ability will allow for less screen I/O overhead in the event an application program has a "known" contiguous block of data that is to be written to the screen. "Known" is taken to mean the block is in a given contiguous area of memory with a given length. As with the Write/Character Attribute at Cursor Position (AH=09H) function, the cursor is not automatically incremented. The required input for this function is as follows:

AL = Attribute(s) of characters
(See paragraph 3.9.9.7, "Set Attribute (AH=16H)" function for values)*

DX = Segment location of character block

BX = Offset location of character block

CX = Block length **

3.9.9.2 Write Block of Characters Only at Cursor Position- AH = 11H. This function is similar to the preceeding function except that the attribute parameter is not specified. The characters take on the attribute(s) of the attribute latch left over from the last CRT call. The required input for this function, with the exception of the attribute (AL = Don't care) parameter, is as follows:

AL = Attribute(s) of characters (See paragraph 3.9.9.7, "Set Attribute (AH=16H)" function for values)*

DX = Segment location of character block

BX = Offset location of character block

CX = Block length **

* The attribute(s) specified is in effect for the entire block and the attribute latch is left set to the attribute specified in register AL.

** This routine "clips" any characters that do not fit on the screen (i.e., characters are written until the end of screen is reached and all other characters are lost/not written). In order not to lose characters, the user should make sure that the cursor is located in a position such that the number of character positions from the cursor to the end of screen is greater than or equal to the block length.

3.9.9.3 Change Screen Attribute(s) - AH = 12H. This function allows the user to specify attribute(s) that affect all of the characters on the display. This routine does not change the position of any characters on the screen. Examples are to blink the entire screen or reverse video the entire screen. The required input for this function is as follows:

AL = Attribute(s) to use (See paragraph 3.9.9.7, "Set Attribute (AH=16H)" function)

NOTE: The attribute latch is set to the attribute specified in register AL on exit.

3.9.9.4 Clear Text Screen and Home the Cursor - AH = 13H. This routine allows the user to clear the text screen and home the cursor (that is, send the cursor to 0,0 coordinates). This function "erases" any data contained in the status region but leaves the status region implementation in effect.

The required input for this function is as follows:

No input required other than AH = 13H (function number)

3.9.9.5 Clear Graphics Screen(s) - AH = 14H. This function allows the user to clear the graphics screen. Required input for this function is as follows:

No input required other than AH = 14H (function number)

3.9.9.6 Set TTY Status Region Beginning - AH = 15H. This function allows the user to specify the beginning line on the screen, which is to be considered as the status region. This is useful in defining a status region of one or more lines. This region remains in effect until it is cleared or reset. During TTY writes and subsequent scrolls, this area remains intact and everything above this line scrolls as necessary. In order to write to this area, the user should read and save the current cursor position, locate the cursor within the status region, use one of the write character functions (not the TTY write), and then restore the cursor to its original position. Required input for this function is as follows:

CH = 0 (must always be zero)

CL = Start line of status region (Valid values are 0 through 24) *
A value of zero (0) for the start line will reset the status region implementation.

* If an attempt is made to set a status region beginning line that does not occur after the current line of the cursor, no status line is implemented. The text from the start line (specified in CL) to the end of the screen is considered to be the status region.

3.9.9.7 Set Attribute(s) - AH = 16H. This function allows the user an alternate method with which to control the following attribute(s).

* Intensity levels 1, 2, and 3 (Blue, Red, and Green)
* Character enable/disable
* Reverse/normal video
* Underline
* Blink
* Alternate character set

This function sets the attribute latch with the specified attribute(s) and subsequent characters written to the screen take on this attribute(s). Note that this function, in combination with a Write Character (either block or single) at Cursor Position (AH=0AH) function has the same effect as the Write Character/Attribute (either block or single) at Cursor Position (AH=09H) function. Note also that the attribute latch remains set to the attribute specified in register BL.

The required input for this function is shown in Figure 3-2.

```
BL = Attribute(s) to set

     (BL is used in order to distinguish to the user
      the difference between this function and the
      Change Screen Attributes (AH=12H) function)

   7 6 5 4 3 2 1 0
   _ _ _ _ _ _ _ _
  |_|_|_|_|_|_|_|_|
   | | | | | | | |
   | | | | | | | +-> Intensity level 1 (Blue)
   | | | | | | +---> Intensity level 2 (Red)
   | | | | | +-----> Intensity level 3 (Green)
   | | | | +-------> Character enable   (2nd dominant) *
   | | | +---------> Reverse video  (1st dominant) *
   | | +-----------> Underline
   | +-------------> Blink
   +---------------> Alternate character set
```

* The user should realize that although more than one attribute can be specified, certain combinations do not make sense (i.e., if Character Enable Attribute is set to a zero, then the character will not appear nor will any of the other attributes except for reverse video). In this manner, for example, the user could have a reversed video, underlined, blinking, red character. Also, by mixing the intensity (color) bits the user can get various levels of intensity (or colors) for a given character.

Figure 3-2 Byte definition - Set Attributes

3.9.9.8 Get Physical Display - Begin Pointer - AH = 17H. This function is used to return the physical display-begin pointer to an application. Logically, the display-begin is always at 0,0, but there is a physical address (offset) associated with the beginning of the display that changes from time to time as the screen is scrolled, cleared, or otherwise changed. This routine returns that offset address relative to the CRT memory area whose segment address is DE00H. The screen memory is a 2000-byte contiguous block of RAM. Once the starting location of this block is known to the application, any character on the screen can be accessed. For example, the last character on the screen is located at (DE00H: display- begin +2000) and the 80th character on the screen (top line, last character on the line)is located at (DE00H:display-begin + 80). This returns the display begin pointer as follows:

DX = 16-bit display-begin pointer (offset)

Example: DX = 0 implies that the first character on the display resides in memory location DE00:0000H

DX = 150H implies that the first character on the display resides in memory location DE00:0150H

3.9.9.9 Print TTY String - AH = 18H. This function allows the user to have a contiguous string of characters, of a given length, located in a code segment to be printed in a TTY-fashion starting at the current cursor position. As with the write TTY function, this routine executes the control characters CR, LF, BS, and BEL and scrolls the screen if necessary. Required input for this function is as follows:

BX = Address (offset) of the string*

Where: (BX) byte 0 = length of the string
(BX) byte 1 = first character of the string

* The user's code segment address is obtained from the stack and therefore does not need to be passed as a parameter.

3.9.9.10 CRT TTY Mode Behavior. The following is a brief description of the behavior of the CRT when used in the TTY mode as well as its behavior when being used in "mixed" modes. The user should read this information carefully, especially if the user mixes non-TTY functions with TTY functions.

Internally, the CRT DSR implements a "phantom" 81st column on each line which in reality is the first column of the following line. This "phantom" column occurs when a character is written in the 80th column of the current line with a TTY write. At this point, if a carriage return (<CR>) command is issued, the cursor moves from the 81st column of the current line back to the first column of the current line. However, if the cursor is in the 81st column and the user reads the cursor position, it is returned as (current line plus 1 line and column 0), not (current line and column 81). The user must be aware of this if he is attempting to restore a cursor position which logically came from the 81st column. At this point the TTY mode is disturbed and the cursor will be restored logically to the first column of the next (a logically new) line. The "Set Cursor Position (AH=02H)" function has no concept of an 81st column. Although the first column position has only one physical location, it can be interpreted as two different logical locations, depending on the current CRT action (mode).

3.9.9.11 Custom Encoding of the CRT. The user may wish to do some custom encoding of the characters being displayed to the CRT. For this reason, a CRT "mapping" capability has been provided to allow applications to intercept characters and CRT actions (if need be) and to encode them as desired.

Upon entry to the CRT DSR a software interrupt is executed, typically used to re-map characters to the screen, which points to an IRET instruction. An application program can reprogram this vector to intercept calls to the CRT DSR, thereby "taking over" the CRT. This capability typically is used to scan through some table which might for instance convert English characters to German characters. However, this capability can also be used to intercept "function calls" (that is, scroll, attribute handling, etc.) and allow an application to encode custom CRT functions. The user should be careful when using this capability however, because it might disturb the data structures of the CRT DSR.

NOTE

When using this capability, it is imperative that the user restore the vector to its original value upon completion of use or the system could "go away".

Once the user's mapping routine has been entered, he can use all registers except ES, DS, and BP unless he saves them and restores them upon exit. When using this mapping feature, the user must first look at the opcode in register AH to determine if it is in fact a write character request. If so, he must also preserve register AH and the registers associated with that function which contain certain parameters. For example, if the user wished to map all "$" symbols to the international currency symbol, his routine would monitor register AH on each call to the CRT DSR. If it contained a write character opcode he would then look at register AL. If register AL contained a 24H (ASCII code for a "$" symbol), he would change that register to an A7H (ASCII code for the international currency symbol). All registers are preserved, but register AL has been changed as described.

3.10 DISK DSR

Table 3-6 describes the functions supported by the Texas Instruments Professional Computer disk device service routines. Detailed descriptions for each function are given.

Table 3-6 Disk DSR Opcodes and Functions

CODE	DESCRIPTION
00H	Reset disk system
01H	Return status code (for last operation)
02H	Read sectors
03H	Write sectors
04H	Verify sector CRCs
05H	Null operation (format track)
06H*	Verify data
07H*	Return retry status
08H*	Set standard Disk Interface Table (DIT)for unit
09H*	Set DIT address for unit
0AH*	Return DIT address for unit
0BH*	Turn off diskette drive motors.

* These functions are primarily for the use of system-level software and utilities

3.10.1 Reset Disk System - 00H

Input: AH = 00H

Output: AH = 00H

This function causes the disk system to restore itself to a known state. What this function does for each type of device supported varies with the requirements of the device and the device-dependent software. In general, the function causes the disk controller(s) to be re-initialized prior to their next use.

3.10.2 Return Status Code - 01H

Input: AH = 01H

Output: AH = 00H
AL = Status code for last disk I/O operation
CF = 0 (No change)

Not all disk DSR functions are I/O operations (this one, for instance). A status is returned in AH for each function, but the status of the last I/O request is always retained for later access (via this function), if desired.

3.10.3 Read Sectors - 02H

Input: AH = 02H
AL = Number of sectors to transfer
CH = Cylinder number
CL = Sector number
DH = Track (i.e., surface or side) number
DL = Drive number
ES:BX = Segment: offset of buffer

Output: AH = I/O status code (see paragraph 3.10.12, "Status Codes")
AL = Number of unprocessed sectors
ES:BX = Segment:offset of the last sector processed

This function reads data from the disk. ANY NUMBER of sectors can be transfered subject to memory boundary limitations (The segment's 64K boundary and disk boundaries cannot be crossed.)

"Last sector processed" means exactly that. Even if the read was in error, the data is transferred to memory.

3.10.4 Write Sectors -03H

Input: AH = 03H
AL = Number of sectors to transfer
CH = Cylinder number
CL = Sector number
DH = Track (i.e., surface or side) number
DL = Drive number
ES:BX = Segment:offset of buffer

Output: AH = I/O status code (see paragraph 3.10.12, "Status Codes")
AL = Number of unprocessed sectors
ES:BX = segment:offset of the last sector processed

This function writes data to the disk. ANY NUMBER of sectors can be transfered subject to memory boundary limitations. (The segment's 64K boundary and disk boundaries cannot be crossed.)

"Last sector processed" means exactly that. If the write is in error, ES:BX point to the data which the DSR is attempting to transfer.

3.10.5 Verify Sector CRCs - 04H

Input: AH = 04H
AL = Number of sectors to transfer
CH = Cylinder number
CL = Sector number
DH = Track (i.e., surface or side) number
DL = Drive number
ES:BX = Segment:offset of buffer

Output: AH = I/O status code (see paragraph 3.10.12, "Status Codes")
AL = Number of unprocessed sectors
ES:BX = Segment:offset of the last sector processed

This function verifies the CRCs of the specified sectors. Because this function is handled like an I/O function, ES:BX must be set as though a transfer is to take place although no data is actually transferred. ANY NUMBER of sectors may be processed subject to memory boundary limitations. (The segment's 64K boundary and disk boundaries cannot be crossed.)

"Last sector processed" has little meaning in this case as this function does not actually transfer data.

3.10.6 Verify Data - 06H

Input: AH = 06H
AL = Number of sectors to process
CH = Cylinder number
CL = Sector number
DH = Track (i.e., surface or side) number
DL = Drive number
ES:BX = Segment:offset of buffer

Output: AH = I/O status code (see paragraph 3.10.12, "Status Codes")
AL = Number of unprocessed sectors
ES:BX = On error, segment:offset of WORD in error

This function verifies disk data against data in memory. ANY NUMBER of sectors can be processed subject to memory boundary limitations (The segment's 64K boundary and the disk boundaries cannot be crossed.)

3.10.7 Return Retry Status - 07H

Input: AH = 07H

Output: AH = 00H
AL = Soft error status of last I/O operation

This function is similar to the Return Status Code (01H) function. It returns the "soft" error status of the last operation. Soft error refers to an error that did not recur when the last operation was retried.

3.10.8 Set Standard Disk Interface Table - 08H

Input: AH = 08H
AL = Standard DIT number (Valid values are 0 through 3)
DL = Diskette drive number (Valid values are 0 through 3)

Output: AH = Error status (see paragraph 3.10.12, "Status Codes")

(NOTE: This function is provided for the use of operating system software.)

Disk interface tables (DITs) are data structures that contain the information used by the device-independent part of the DSR to interface with the device-dependent code for a specific disk device.

This function allows one to set up a diskette drive to one of four standard configurations by setting that drive's DIT. The standard DIT numbers are defined as follows:

NUMBER	DESCRIPTION
0	Single side, 48 tpi, 8 sectors/track, 512-byte sectors
1	Single side, 96 tpi, 8 sectors/track, 512-byte sectors
2	Double side, 48 tpi, 8 sectors/track, 512-byte sectors
3	Double side, 96 tpi, 8 sectors/track, 512-byte sectors

3.10.9 Set DIT Address for Drive - 09H

Input: AH = 09H
DL = Disk drive number (Valid value is 0 through 7)
ES:BX = Segment:offset of DIT for drive

Output: AH = Error status (see paragraph 3.10.12, "Status Codes")

(NOTE: This function is provided for the use of operating system software.)

Disk interface tables (DITs) are data structures that contain the information used by the device-independent part of the DSR to interface with the device-dependent code for a specific disk device.

This function allows one to set any disk to a configuration other than the four standard configurations. This is the mechanism by which dynamic linking of disk drives to the system is accomplished.

3.10.10 Return DIT Address for Drive - 0AH

Input: AH = 0AH
DL = Disk drive number (Valid value is 0 through 7)

Output: AH = Error status (see paragraph 2.13.5, "Error Codes")
ES:BX = Segment:offset of DIT for drive

(NOTE: This function is provided for the use of operating system software.)

Disk interface tables (DITs) are data structures that contain the information used by the device-independent part of the DSR to interface with the device-dependent code for a specific disk device.

This function allows the user to access a drive's DIT for information and verification purposes.

3.10.11 Turn OFF All Diskette Drives - 0BH

Input: AH = 0BH

Output: AH = 0

(NOTE: This function is provided for the use of operating system software.)

Under normal operation the diskette drive motors are left ON for a period of time following a read or write operation to save time waiting for the motor to come up to speed. Some applications, notably diagnostics, require a function to ensure that the motors are not running.

3.10.12 Status Codes

All functions return a status code in register AH and an error flag in CF. If the carry condition is set (CF = 1), then an error has occurred and AH contains the error code. If the no-carry condition is set (CF = 0), no error has occurred and AH always contains a zero (0). The error codes are given in Table 3-7.

Table 3-7 Error Codes

VALUE	DESCRIPTION
00H	No error
80H	Timeout - drive not ready or hardware failed
40H	Seek failed - track not found
20H	Controller hardware failed
10H	CRC error
08H	Data request error - controller failure
04H	Record (sector) not found
02H	No data - bad disk format
01H	Command error - bad opcode or parameter
03H	Disk write protected
05H	Data did not verify
09H	I/O transfer crosses 64-kbyte boundary

3.11 KEYBOARD DSR

This subsection describes the keyboard DSR and the functions it provides to the system or application programs that use it. It also shows the various codes returned by the DSR for the standard configuration of the keyboard.

The keyboard DSR functions are located in the system ROM and are accessed through the 8088 software interrupt mechanism (essentially an address-independent subroutine call). The typical user of the keyboard DSR is the operating system-dependent BIOS, which resides on a particular operating system diskette and which is loaded into RAM during disk boot.

The functions described herein access a buffer that is controlled by the keyboard interrupt service routine. All encoding and any special handling (described in subsequent paragraphs) occurs in the interrupt service routine. All discussions of keyboard mapping vectors refer to actions occurring during the servicing of the keyboard hardware (not software) interrupt.

The desired function is chosen by placing an opcode in register AH and executing an INT 4AH. All registers except AX are preserved. The following functions are included in the keyboard DSR.

3.11.1 Initialization Logic

The code for this function is automatically executed during power-up or reboot and is not directly available to the user. It performs diagnostics on the keyboard hardware, sends to it the required initialization sequences, and initializes the DSR internal data areas.

3.11.2 Read Keyboard Input - AH = 0

This function reads and removes the current character (if any) from the keyboard buffer. The character value is returned in register AX. If there is no character ready, the DSR will wait until one is received before it returns to the caller. This character has already been fully encoded (refer to Table 3-8). Normally, the encoded ASCII character is returned in register AL, and register AH contains 00. If AL = 0, then the coded value in AH corresponds to one of the various function keys (Refer to Table 3-9.

3.11.3 Read Keyboard Status - AH = 1

This function determines whether a character is ready at the keyboard without having to actually read it. If no character is waiting, it returns with the Z-flag set (=1). If the Z-flag is reset (=0), a character is available to be read. The character value is returned in AX, but is not removed from the keyboard buffer.

3.11.4 Read Keyboard Mode - AH = 2

This function determines the current mode of the keyboard. The mode value is returned in register AL in the format shown in Figure 3-3 The definition of the byte is as follows.

```
 ---------------------------------
 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0 !   <--- Reg AL
 ---------------------------------
   !   !   !   !   !   !   !   !
   !   !   !   !   !   !   !   ---   1 = Control key depressed
   !   !   !   !   !   !   !
   !   !   !   !   !   !   -------   1 = Alternate key depressed
   !   !   !   !   !   !
   !   !   !   !   !   -----------   1 = Shift key depressed
   !   !   !   !   !
   !   -------------------------     0000   (always zero)
   !
   -----------------------------     1 = Caps lock key depressed
```

Figure 3-3 Byte Definition - Keyboard Modes

Because the "mode" applies to the last character typed and not necessarily to the one at the front of the queue, this function returns valid information only if the keyboard buffer contains one or less characters. In order to use this function, the key should be read normally, then a status check made to make sure the buffer is empty. If the buffer is empty at this point, the mode may be read.

3.11.5 Flush Keyboard Buffer - AH = 3

This function is used to "flush" (empty) the keyboard type-ahead buffer. It simply resets the queue pointers, which effectively empties the buffer.

3.11.6 Keyboard Output - AH = 4

This function sends the keyboard command in AL directly to the keyboard, with appropriate handshaking. Upon return, the Z-flag has the status of the operation. If the Z-flag (ZF) is set (=1), the command was performed correctly; otherwise (ZF=0), an error was made. The keyboard commands sent by the CPU are given in Table 3-8

Table 3-8 Keyboard Commands

AL	FUNCTION PERFORMED
00	Perform a powerup reset and install default parameters
01*	Turn repeat-action feature ON
02	Turn repeat-action feature OFF
03	Lock the keyboard
04*	Unlock the keyboard
05	Turn keyclick ON**
06*	Turn keyclick OFF**

* Indicates the default parameters.
** Keyclick requires hardware modification. It is not presently supported.

3.11.7 Put Character Into Keyboard Buffer - AH = 5

This function places the 16-bit value in BX directly into the keyboard buffer. On return, if the Z-flag is reset (=0), the character was placed in the buffer (this is the normal case). If the Z-flag is set (=1), the buffer was full, and the character was not placed in the buffer (it is still in BX). A subsequent Read Keyboard Input (AH=0) function call retrieves this character (assuming the buffer was empty to start with, and no keys have been typed on the keyboard.) Any 16-bit value can be placed into the buffer, but unless the user has some explicit application that understands "strange" characters from the keyboard, it is recommended that only standard characters generated by the keyboard be used. The format for the characters is the same as that given in the Read Keyboard Input function.

To place a normal ASCII character into the buffer, the function call should be made with the character value in BL and zero in BH. To place function keys into the buffer, the function call should be made with the extended function value in BH, and zero in BL. (Refer to Table 3-9 and Table 3-10).

This function can be useful in situations where a program needs to make characters that appear to have been typed in at the keyboard. Two examples of this follow.

* An application can ensure that the operating system printer "echo" feature is disabled by inserting a CTRL N into the buffer during initialization. The operating system sees this as just another key and turns off the echo.

* Many operating systems lack a chaining feature, and this function may be used to provide one. Immediately before a program terminates, characters can be placed into the keyboard buffer (a flush operation is recommended first) to simulate a command being typed at the keyboard. When the program terminates, the operating system takes over, reads the keyboard buffer, and performs that command (which could invoke a second program, effectively "chaining" programs).

3.11.8 General Keyboard Layout

The outline of the keyboard and the key position numbers associated with each key are shown in Figure 3-4. These are the scan codes sent from the keyboard and are used internally by the keyboard DSR to encode the key. Note that the keys marked with "***" (mode keys) are not in the actual matrix and do not generate a scan code.

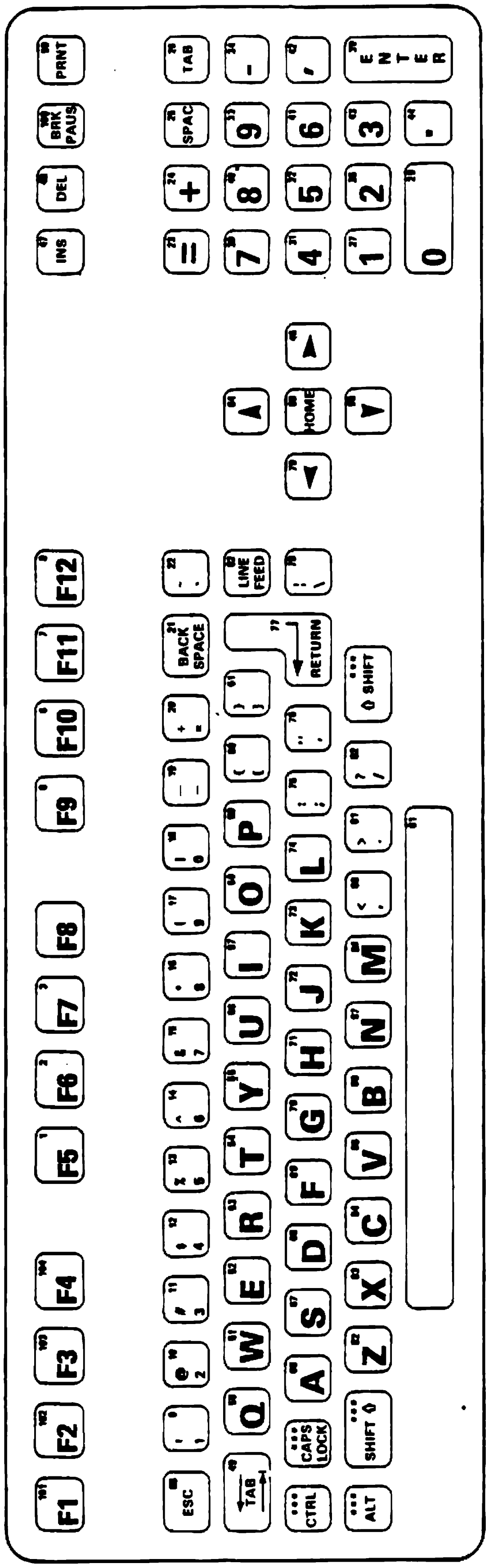


Figure 3-4 General Keyboard Layout Showing Scan Codes

3.11.9 Character Codes

Table 3-9 lists the character and extended function codes returned by the keyboard DSR. The modes are handled internally to the keyboard DSR and the returned code reflects the mapping shown in this table.

General notes to Table 3-9:

1. Key # is shown in Figure 3-4.

2. In each column, both the "graphic" and the hex value of the character are given in the form: GGG HH.

3. Entries consisting of "--- --" indicate that the combination is suppressed within the keyboard DSR.

4. Entries consisting of "xxx **" indicate special handling in the form of direct action by the keyboard DSR. (For details, see paragraph 3.11.14, "Special Handling")

5. Normal (ASCII) characters are returned in register AL with the Key # in AH.

6. Entries consisting of "xxx yy*" are returned with AL=0 and the indicated value (yy) in AH.

Table 3-9 Standard Keyboard Character Codes

KEY #	NORM		SHIFT		CONTROL		ALT		COMMENTS
01	f5	3F*	sf5	58*	cf5	62*	af5	6C*	F5
02	f6	40*	sf6	59*	cf6	63*	af6	6D*	F6
03	f7	41*	sf7	5A*	cf7	64*	af7	6E*	F7
04	f8	42*	sf8	5B*	cf8	65*	af8	6F*	F8
05	f9	43*	sf9	5C*	cf9	66*	af9	70*	F9
06	f10	44*	sf10	5D*	cf10	67*	af10	71*	F10
07	f11	45*	sf11	08*	cf11	0A*	af11	0C*	F11
08	f12	46*	sf12	09*	cf12	0B*	af12	0D*	F12
09	1	31	!	21	---	--	alt1	78*	
10	2	32	@	40	Fnul	03*	alt2	79*	
11	3	33	#	23	---	--	alt3	7A*	
12	4	34	$	24	---	--	alt4	7B*	
13	5	35	%	25	---	--	alt5	7C*	
14	6	36	^	5E	RS	1E	alt6	7D*	
15	7	37	&	26	---	--	alt7	7E*	
16	8	38	*	2A	---	--	alt8	7F*	
17	9	39	(	28	---	--	alt9	80*	
18	0	30	)	29	---	--	alt0	81*	
19	-	2D	_	5F	US	1F	alt-	82*	
20	=	3D	+	2B	---	--	alt=	83*	
21	BS	08	BS	08	DEL	7F	---	--	BACK SPACE
22	`	60	~	7E	---	--	---	--	
23	=	3D	=	3D	=	3D	pf1	8C*	NUM =
24	+	2B	+	2B	+	2B	pf2	8D*	NUM +
25	SP	20	SP	20	SP	20	pf3	8E*	NUM SPACE
26	HT	09	Bktab	0F*	HT	09	pf4	8F*	NUM TAB
27	1	31	1	31	1	31	---	--	NUM 1
28	---	--	---	--	---	--	---	--	(unused)
29	0	30	0	30	0	30	---	--	NUM 0
30	CR	0D	CR	0D	CR	0D	---	--	NUM ENTER
31	4	34	4	34	4	34	---	--	NUM 4
32	5	35	5	35	5	35	---	--	NUM 5
33	9	39	9	39	9	39	---	--	NUM 9
34	-	2D	-	2D	-	2D	---	--	NUM -
35	2	32	2	32	2	32	---	--	NUM 2

Table 3-9. Standard Keyboard Character Codes (Continued)

KEY #	NORM		SHIFT		CONTROL		ALT		COMMENTS
36	---	--	---	--	---	--	---	--	(unused)
37	---	--	---	--	---	--	---	--	(unused)
38	---	--	---	--	---	--	---	--	(unused)
39	7	37	7	37	7	37	---	--	NUM 7
40	8	38	8	38	8	38	---	--	NUM 8
41	6	36	6	36	6	36	---	--	NUM 6
42	,	2C	,	2C	,	2C	---	--	NUM ,
43	3	33	3	33	3	33	---	--	NUM 3
44	.	2E	.	2E	.	2E	---	--	NUM .
45	Ptogl	72*	***	**	---	--	---	--	(PRINT)
46	C-rt	4D*	sC-rt	8A*	cC-rt	74*	aC-rt	4E*	RIGHT ARROW
47	Ins	52*	sIns	28*	cIns	29*	aIns	2A*	INSERT
48	Del	53*	sDel	38*	cDel	39*	aDel	3A*	DELETE
49	HT	09	Bktab	0F*	HT	09	---	--	TAB
50	q	71	Q	51	DC1	11	altQ	10*	
51	w	77	W	57	ETB	17	altW	11*	
52	e	65	E	45	ENQ	05	altE	12*	
53	r	72	R	52	DC2	12	altR	13*	
54	t	74	T	54	DC4	14	altT	14*	
55	y	79	Y	59	EM	19	altY	15*	
56	u	75	U	55	NAK	15	altU	16*	
57	i	69	I	49	HT	09	altI	17*	
58	o	6F	O	4F	SI	0F	altO	18*	
59	p	70	P	50	DLE	10	altP	19*	
60	[	5B	{	7B	ESC	1B	---	--	
61	]	5D	}	7D	GS	1D	---	--	
62	LF	0A	LF	0A	cLF	75*	aLF	4F*	LINE FEED
63	Ppau	**	Pbrk	**	---	--	---	--	(BREAK/PAUSE)
64	C-up	48*	sC-up	88*	cC-up	84*	aC-up	49*	UP ARROW
65	ESC	1B	ESC	1B	ESC	1B	---	--	ESC
66	a	61	A	41	SOH	01	altA	1E*	
67	s	73	S	53	DC3	13	altS	1F*	
68	d	64	D	44	EOT	04	altD	20*	
69	f	66	F	46	ACK	06	altF	21*	
70	g	67	G	47	BEL	07	altG	22*	

Table 3-9. Standard Keyboard Character Codes (Concluded)

KEY #	NORM		SHIFT		CONTROL		ALT		COMMENTS
71	h	68	H	48	BS	08	altH	23*	
72	j	6A	J	4A	LF	0A	altJ	24*	
73	k	6B	K	4B	VT	0B	altK	25*	
74	l	6C	L	4C	FF	0C	altL	26*	
75	;	3B	:	3A	---	--	---	--	
76	'	27	"	22	---	--	---	--	
77	CR	0D	CR	0D	CR	0D	---	--	RETURN
78	\	5C	¦	7C	FS	1C	---	--	
79	C-lf	4B*	sC-lf	8B*	cC-lf	73*	aC-lf	4C*	LEFT ARROW
80	Home	47*	sHome	86*	cHome	77*	aHome	85*	HOME
81	SP	20	SP	20	SP	20	SP	20	SPACE bar
82	z	7A	Z	5A	SUB	1A	altZ	2C*	
83	x	78	X	58	CAN	18	altX	2D*	
84	c	63	C	43	ETX	03	altC	2E*	
85	v	76	V	56	SYN	16	altV	2F*	
86	b	62	B	42	STX	02	altB	30*	
87	n	6E	N	4E	SO	0E	altN	31*	
88	m	6D	M	4D	CR	0D	altM	32*	
89	,	2C	<	3C	---	--	---	--	
90	Ptogl	72*	***	**	---	--	---	--	PRINT
91	.	2E	>	3E	---	--	---	--	
92	/	2F	?	3F	---	--	---	--	
93	---	--	---	--	---	--	---	--	(unused)
94	Del	53*	sDel	38*	cDel	39*	aDel	3A*	(DELETE)
95	Ins	52*	sIns	28*	cIns	29*	aIns	2A*	(INSERT)
96	C-dn	50*	sC-dn	89*	cC-dn	76*	aC-dn	51*	DOWN ARROW
97	---	--	---	--	---	--	---	--	(unused)
98	---	--	---	--	---	--	---	--	(unused)
99	---	--	---	--	---	--	---	--	(unused)
100	Ppau	**	Pbrk	**	---	--	---	--	BREAK/PAUSE
101	f1	3B*	sf1	54*	cf1	5E*	af1	68*	F1
102	f2	3C*	sf2	55*	cf2	5F*	af2	69*	F2
103	f3	3D*	sf3	56*	cf3	60*	af3	6A*	F3
104	f4	3E*	sf4	57*	cf4	61*	af4	6B*	F4

3.11.10 Extended Codes

The "extended" codes (non-ASCII codes) represent special function keys on the keyboard. They are distinguished by register AL being 00 upon returning from a Read Keyboard (AH=),1,or 2) function call, in which case the extended code is in register AH. They are in a range of codes (00H-FFH) that includes normal ASCII and they are given in Table 3-10.

Table 3-10 Extended Function Codes

MSD / LSD	0	1	2	3	4	5	6	7	8
0	Pbrk	altQ	altD	altB	f6	C-dn	cf3	af9	alt9
1	Ppau	altW	altF	altN	f7	aC-dn	cf4	af10	alt0
2		altE	altG	altM	f8	Ins	cf5	Ptogl	alt-
3	Fnul	altR	altH		f9	Del	cf6	cC-lf	alt=
4		altT	altJ		f10	sf1	cf7	cC-rt	cC-up
5		altY	altK		f11	sf2	cf8	cLF	aHome
6		altU	altL		f12	sf3	cf9	cC-dn	sHome
7		altI			Home	sf4	cf10	cHome	
8	sf11	altO	sIns	sDel	C-up	sf5	af1	alt1	sC-up
9	sf12	altP	cIns	cDel	aC-up	sf6	af2	alt2	sC-dn
A	cf11		aIns	aDel		sf7	af3	alt3	sC-rt
B	cf12			f1	C-lf	sf8	af4	alt4	sC-lf
C	af11		altZ	f2	aC-lf	sf9	af5	alt5	pf1
D	af12		altX	f3	C-rt	sf10	af6	alt6	pf2
E		altA	altC	f4	aC-rt	cf1	af7	alt7	pf3
F	Bktab	altS	altV	f5	aLF	cf2	af8	alt8	pf4

3.11.11 Keyboard Modes

In the standard keyboard, the mode keys have the effect shown in Table 3-9. The latching (push-push) CAPS LOCK key affects the alphabetic keys (50-59, 66-74, and 82-88 on the standard keyboard) by forcing the SHIFT mode. Normally the alphabetic keys produce lowercase characters, and the SHIFT key temporarily causes them to be uppercase. When the CAPS LOCK mode is invoked (CAPS LOCK key latched down), the alphabetic keys produce uppercase and the SHIFT key has no further effect (on the alphabetic keys).

In the standard encoding, there is no valid combination of mode keys except for CTRL/ALT/DEL, which is used for system reset. If more than one mode key is pressed at once, only one will be recognized. The precedence is as follows: Highest is ALT, then CTRL, then SHIFT (and CAPS LOCK).

Simultaneously depressing the CTRL, ALT, and DEL keys results in the keyboard DSR initiating the equivalent of a system power-up reboot. It is handled internally to the DSR and does not return a code. This function is "hardwired" and cannot be disabled.

The ALT key has a special use, which allows the user to enter any character code (00H-0FFH) from the keyboard. If the ALT key is held down, and the decimal value of the desired character is typed on the NUMERIC KEYPAD with three keystrokes, the value is returned directly through the Read Keyboard Input (AH=0) function to the application as a normal character. If less than three digits are typed, the next non-ALT key struck forces the currently accumulated ALT/NUM value (due to the first 1 or 2 keystrokes) to be sent. Note that if the first 1 or 2 keystrokes were the zero key, the next key struck sends its normal character, since the zero adds nothing to the ALT/NUM value, but is just a "place-keeper". If more than three keys are struck, the accumulated value is sent and a new three-keystroke sequence is started.

3.11.12 Type-Ahead Buffer

The DSR implements a circular type-ahead queue, which is capable of buffering up to 15 keystrokes (each keystroke is 2 bytes). If the queue is filled, any further characters entered at the keyboard cause the system beeper to sound. The Flush Keyboard Buffer (AH=3) function causes the queue pointers to be reset, which effectively empties the buffer.

3.11.13 Repeat-Action Feature

If the repeat-action feature (the default)is enabled, all keys are repeat action at a 15-cps rate after an initial delay of 1/2 second. Repeat-action characters are ignored if the queue currently contains more than one pending character The result of this is that the application does not have to worry about the repeat-action "coasting" problem; that is, if the application does not or cannot read the keyboard input faster than the repeat-action rate, the undesired repeat-action characters are not queued and the keyboard does not get ahead of the application.

3.11.14 Special Handling

This section deals with functions handled by the keyboard DSR itself. There are several cases in which immediate reaction is required (for example, pausing the output routine so a fast-scrolling screen can be read). Most of these functions are implemented with the software interrupt facility of the 8088.

Each of the defined interrupt vectors points to some default piece of code that either does nothing (a single IRET instruction) or performs some system function. An application program may change these interrupt vectors in order to gain direct access to a function, but the application is responsible for preserving the original contents of the vector and restoring it before terminating and returning to the system. Note that the application routine, if used, must end with an IRET (or the equivalent "RET 2", which allows flags to be passed).

The stack used is the internal stack of the keyboard interrupt service routine and only 10 levels (20 bytes) of stack are available to the user's routine. Note that interrupts are disabled when the user routine is entered (due to the INT instruction). They should be re-enabled immediately unless it is necessary for them to be disabled. Registers AX, BX, CX, DI, and ES may be used (information is passed in AX); any others must be preserved. If the available stack is not large enough, then the routine should switch to an internal stack of sufficient size (plus eight bytes for possible interrupts). Also, the routine is executed as a part of the keyboard interrupt service routine, which means that no other keystrokes are accepted until the user routine finishes and returns. The normal way to communicate with the outside world (outside the service routine) is to set a flag, and to watch for the flag in the application. For example, this is how the BREAK function is implemented in MS-DOS. For these reasons, control should not be retained by the user's routine unless a complete system initialization is to be performed.

3.11.15 User-Available Interrupts

The following is a summary of the software interrupts performed by the keyboard DSR that may be used by application programs. The interrupts are presented in the order that they are executed. The number in parentheses, the "interrupt type", is used in an INTerrupt instruction The absolute address of the corresponding vector is the interrupt type times 4. As an example, the address of the keyboard mapping vector is 5BH x 4 = 16CH. Note that any of the special key interrupt functions can be bypassed by re-encoding the key code as described in paragraph 3.11.21, "Custom Encoding". The keyboard DSR interrupts are:

1. Keyboard Mapping Interrupt (5BH)

2. Program Pause Interrupt (5CH) *

3. Program Break Interrupt (5DH) *

4. Print Screen Interrupt (5EH) *

5. Keyboard Queueing Interrupt (5FH)

* These Interrupts occur after internal encoding.

3.11.15.1 Keyboard Mapping. This interrupt is performed each time a key is pressed, but before it is encoded, which allows the user to encode the key. When the user encodes the key, the DSR places the key code in the queue and performs Keyboard Queuing (5FH) Interrupt; otherwise, the DSR encodes the key, checks for the special keys, and then queues the key code, causing the Keyboard Queuing Interrupt. Use of this Interrupt in re-mapping the keyboard is described in paragraph 3.11.21, "Custom Encoding".

3.11.15.2 Program Pause. Pressing the (unshifted) BRK/PAUS key causes a software interrupt and allows the user to perform an action or return a key code. It will return an extended code (see Table 3-O) to the caller if desired. At system power-up, the vector is set up such that the PAUS key sequence causes a screen hold, which stops a fast-scrolling screen. An application program can change the interrupt vector in order to support a pause function of its own, but the program is responsible for remembering the original vector and restoring it before terminating. The Carry flag determines the action of the keyboard DSR upon return from the software interrupt. If the Carry flag is set, the DSR does nothing else and simply exits. If the Carry flag is reset, then the character value in AX is placed into the queue. Before the software interrupt is executed, the Carry flag is reset and the extended code for the Program Pause function is placed in AX. Therefore, if an IRET instruction is used to return instead of the default ROM pause routine, the DSR returns the Program Pause function code to the application. Note that since the Carry flag is used to pass information, the IRET instruction must be simulated with "RET 2" if the user needs to return with Carry set. (The IRET instruction restores flags to their pre-interrupt state.)

3.11.15.3 Program Break. Pressing the (shifted) BRK/PAUS key causes a software interrupt and allows the user to perform an action or return a key code. It can be set to return an extended code (see Table 3-9) to the caller, if desired. During power-up initialization, this interrupt vector is set up to point to an IRET instruction so that the BRK key sequence is ignored other than returning the break code. An application program can change the interrupt vector in order to support a break function of its own. However, the program is responsible for preserving the original contents of the vector and restoring it before terminating. The encoding/software-interrupt technique is the same as that described in paragraph 3.11.15.2, "Program Pause".

3.11.15.4 Print Screen. Pressing the SHIFT and PRNT keys causes yet another software interrupt. The user can perform an action or return a key code. This normally vectors to an IRET instruction within the ROM. The DSR checks the Carry flag upon return, as described in the Program Pause and Program Break interrupts (paragraphs 3.11.15.2 and 3.11.15.3, respectively). Before the interrupt is executed, the Carry flag is set, so if the routine consists only of an IRET, the key is effectively ignored. This can be (and is, by MS-DOS BIOS) patched to vector to an actual Print Screen routine. This routine executes as a part of the keyboard interrupt service routine and, thus, cannot be interrupted by another keystroke.

3.11.15.5 Keyboard Queueing. This software interrupt occurs every time a character, whether encoded by the DSR oar by the user, is placed in the type-ahead buffer. Its intended use is to enable a real-time OS task to know when there is a character to be read. The user has the option of not having a keycode queued (ignoring the key). See paragraph 3.11.15.1, "Keyboard Mapping" for Keyboard Queuing interrupt conditions.

3.11.16 Custom Encoding

Facilities are available to allow an application program to encode the keyboard for itself, if necessary. Every time a key is pressed on the keyboard, one or two key codes are sent from the keyboard to the DSR. (For details see paragraph 3.11.17Keyboard Interface Protocol). Each time a key code (not including the mode key codes, which are handled internally) is received, a software interrupt is performed. Normally the interrupt vector points to an IRET instruction, but an application program can reprogram the vector to intercept these key codes, if necessary. Since everything comes through this vector, the application can completely take over (except for the system reset combination CTRL/ALT/DEL). The routine that intercepts the key codes typically scans through some tables to encode its special keys and execute an "RET 2" instruction when done. Note that in this situation it is especially critical that the application restores the vector to its original value after completion or the system will crash when the special encoding routine is written over.

When the software interrupt is performed (from the keyboard interrupt service routine), the keyboard scan code is in AL, the mode byte is in AH (see Figure 3-3 for modes), and the Carry flag is set (=1). If, upon return from the interrupt, the Carry flag is reset (=0), then the normal encoding of the key code is bypassed and the values in AL and AH are placed directly into the type-ahead buffer. This is useful for changing the standard encoding of the keyboard. If the Carry flag is set, and the value of AL is returned as 0FFH, the keystroke is ignored entirely, and nothing is placed in the buffer. This is useful in situations where the Special Handling routine (paragraph 3.11.14) performs some function directly and does not need to send a character. Note that since this is a software interrupt, the IRET instruction must be simulated with "RET 2" in order to pass flags back.

3.11.17 Keyboard Interface Protocol

Each time a key is pressed on the keyboard, a byte representing the key position is sent to the keyboard DSR. If the state of the mode keys (the SHIFT, ALT, CAPS LOCK, and CTRL keys) has changed since the last keystroke, the key position byte is preceded by a byte showing the current status of the mode keys.

The first byte (mode byte) is sent only if it has changed since the last transmission. It is never sent without being followed by the second byte. Also, since the mode is not allowed to change during the repeat-action key function, the mode byte is never sent during a repeat-action key transmission.

Note that the second byte contains a repeat-action key bit. This bit is set to 1 during a repeat-action key transmission, and reset to 0 during a non-repeat-action transmission. If the key is still pressed after a 1/2-second delay, the code is sent again, this time with bit 7 = 1. This bit is used by the keyboard to suppress the repeat-action key function when necessary. All communication with the keyboard is asynchronous, serial, 8-data-bit, 1 stop-bit, even parity. The keyboard transmits its data at 2440 bps and receives its commands at 300 bps.

Although the two bytes have similar formats, as shown in Figure 3-5, they may be distinguished by the fact that the mode key status byte has all ONEs in bits 3-6.

```
 ------------------------------------
 ! 8 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0 !     FIRST BYTE
 ------------------------------------      (Not always sent)
   !   !   !   !   !   !   !   !   !
   !   !   !   !   !   !   !   !   -----> Control
   !   !   !   !   !   !   !   !
   !   !   !   !   !   !   !   ---------> Alternate
   !   !   !   !   !   !   !
   !   !   !   !   !   !   -------------> Shift
   !   !   !   !   !   !
   !   !   ---------------------------> = 1111 (denotes 1st byte)
   !   !
   !   -------------------------------> Caps lock (Uppercase)
   !
   -----------------------------------> Parity


 ------------------------------------
 ! 8 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0 !     SECOND BYTE
 ------------------------------------
   !   !   !   !   !   !   !   !   !
   !   !   !   !   !   !   !   !   !
   !   !   ---------------------------> Scan Code
   !   !
   !   -------------------------------> Repeated Character
   !                                       (Repeat-action keys)
   !
   -----------------------------------> Parity
```

Figure 3-5 Byte Definition - Keycode

The keyboard understands several commands which are detailed in the Keyboard Output (AH=4) function, and the keyboard (normally) acknowledges each command.

The codes sent by the keyboard are given in Table 3-9 through scan code 104 (68 hex). The scan codes from 69H through 6FH are spares and may be assigned in the future, although the size of the standard encoding tables does not comprehend this. Codes 70H through 72H are status codes returned by the keyboard in response to commands: 70H is normal command acknowledge status, 71H indicates internal RAM failure, and 72H indicates internal ROM failure. Codes 73H-77H are unused and codes 78H-7FH are taken up by the encoding for the mode key status byte.

3.12 PARALLEL PRINTER PORT DSR

This subsection describes the parallel printer port DSR and the functions it provides to the system or application programs that use it.

The printer DSR provides routines with which to implement a "Centronics-compatible" parallel port interface. It enables the user to output characters, get printer status, and initialize the printer . It is capable of interfacing to most printer s with a Centronics-compatible interface.

The printer DSR functions are located in the system ROM and are accessed through the software interrupt mechanism of the 8088 microprocessor. The desired function is chosen by placing an opcode in register AH, zeros in register DL (see explanation of register DL in paragraph 3.12.4, "Use Under an Operating System") and executing an INT 4BH instruction. All registers are preserved except AH, which always returns with the printer status (see paragraph 3.12.3, "Return Printer Status - AH=2, DL=0." The following functions are available:

3.12.1 Output Character To Printer - AH = 0, DL = 0

This function sends the character in AL to the printer port. The BUSY signal from the printer is checked before sending the character. If the printer is still busy after about 0.33 sec, the DSR sets the time-out bit in the status byte (in AH) and returns; otherwise, it returns with the time-out bit reset. Any abnormal conditions on the status signals from the printer causes the printer to go BUSY and time-out occurs if the printer sets FAULT, PAPER OUT, or NOT SELECT. It also sets BUSY, causing a time-out to occur.

In general, it is not desirable to rely on the time-out of the printer output routine for normal use. It is a software loop and causes the application to "hang" during the time-out period. The preferable method is to have the application watch the BUSY signal through the printer status call and implement its own time-out (if desired) under its own control. This is especially important when using the DSR from the printer task of a real-time OS. Therefore, the normal sequence to print a character is:

```
REPEAT
    INTerrupt 4BH with AH = 2 and DL = 0 (see paragraph 3.10.3,
    "Return Printer Status"[paragraph 3.10.3]).
UNTIL
    STATUS = NOT BUSY
END

INTerrupt 4BH with AH = 0, DL = 0 and AL = <character>
IF STATUS = (time-out)
THEN
    <handle the error>  (FAULT or PAPER OUT or (NOT SELECTED))
END
```

(Refer to Figure 3-6 for byte definition of Return Printer Status.)

3.12.2 Initialize Printer - AH = 1, DL = 0

This function activates the INIT signal on the interface causing the printer to perform the equivalent of a power-up reset. The specific action taken is printer-dependent (refer to the appropriate printer manual). The system software activates this signal only once, at actual system power-up (not CTRL/ALT/DEL reset).

3.12.3 Return Printer Status - AH = 2, DL = 0

This function reads the printer status port and returns the information in register AH. This is the same information as that returned after the Output Character to Printer (AH=0, DL=0) and Initialize Printer (AH=1, DL=0) functions. The bits of AH are encoded as shown in Figure 3-6.

```
 ---------------------------------
 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
 ---------------------------------
   |   |   |   |   |   |   |   |
   |   |   |   |   |   |   |   ------- TIME OUT (on busy)
   |   |   |   |   |   |   |
   |   |   |   |   ----------------       (not used)
   |   |   |   |
   |   |   |   -------------------- BUSY
   |   |   |
   |   |   ------------------------ PAPER OUT
   |   |
   |   ---------------------------- SELECTED (ON LINE)
   |
  --------------------------------- FAULT
```

Figure 3-6 Byte Definition - Return Printer Status

3.12.4 Use Under an Operating System

One of the features of using the software interrupt technique to interface with the ROM routines is that a DSR can be enhanced or replaced by patching its interface interrupt vector. Under MS-DOS, for example, the serial printer support emulates the ROM's parallel printer functions. The printer interface is implemented by patching a small routine "in front of" the printer interrupt vector. This routine looks at register DL to determine the desired printer. If DL=zero, then a jump to the ROM routine is made, and the user is unaware of the patch. If DL=1, however, then AH is decoded to perform the appropriate function on the serial printer. Since the serial support emulates the status returned by the ROM's parallel routines, again the user is not aware of the operation, except for the fact that he set DL. Note that some operating systems may not require register DL to be anything. In the MS-DOS case, however, the DSR was extended in a manner that DL must be specified. As this is not necessarily the case with other operating systems, refer to the appropriate documentation for the operating system used.

3.13 WINCHESTER DSR

The register assignment for the Winchester controller is given in Table 3-11.

Table 3-11 Winchester Controller I/O Port Assignment

HEX ADDRESS	IN FUNCTION	OUT FUNCTION
0030	Data IN port	Data OUT port
0031	Status register	RESET
0032	Not used	Not used
0033	Not used	Interrupt mask

An IN function sets data from the Winchester controller board and drives it onto the computers I/O expansion bus. Conversely, an OUT function sets data from the computers I/O expansion bus onto the Winchester disk controller board.

3.13.1 Byte Definitions

The following are byte definitions for the Winchester controller registers and ports. (Additional information may be found in subsection 2.13, "Winchester Disk Drive and Controller.")

3.13.1.1 Controller Status Register. This byte stores the controller status. It enables the computer to read the status of the controller and monitor its operation. Bits of the controller status byte are defined as follows.

```
 ---------------------------------
 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0 !   <--- I/O Port address 0031H (READ)
 ---------------------------------
   !   !   !   !   !   !   !   !
   !   !   !   !   !   !   !   ---   1 = Data Request
   !   !   !   !   !   !   !
   !   !   !   !   !   !   -------   1 = Input/output
   !   !   !   !   !   !             0 = Output
   !   !   !   !   !   -----------   1 = Command,
   !   !   !   !   !                 0 = Data
   !   !   !   !   ---------------   1 = Pending interrupt
   !   !   !   !
   -------------------------------       Don't care
```

3.13.1.2 Reset Port. This byte resets the controller. Any WRITE to port 0031H resets the controller. Bits of the reset port byte are defined as follows.

```
 ---------------------------------
 ! 7 ! 6 ! 5 ! 4 ! 3 ! 2 ! 1 ! 0 !  <--- I/O Port address 0031H (WRITE)
 ---------------------------------
   !   !   !   !   !   !   !   !
   -----------------------------       Don't care
```

3.13.1.3 Interrupt Mask. A two-bit field in this byte determines the interrupt to be serviced. Bits of the interrupt mask byte are defined as follows.

```
 ---------------------------------
 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   <--- I/O Port address 0033H (READ)
 ---------------------------------
   |   |   |   |   |   |   |   |
   |   |   |   |   |   |   |    ---   1 = Status interrupt enable
   |   |   |   |   |   |   |
   |   |   |   |   |   |    -------   1 = Data interrupt enable
   |   |   |   |   |   |
   -------------------------------        Don't care
```

3.13.1.4 Error Status Byte. This byte is a special case that is only available after a command has been completed. The controller indicates that this byte is available by setting the I/O and C/D bits with DRQ. Bits of the error status byte are defined as follows.

```
 ---------------------------------
 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   <--- I/O Port address 0030H (READ)
 ---------------------------------
   |   |   |   |   |   |   |   |
   |   |   |   |   |   |   |    ---       Don't care
   |   |   |   |   |   |   |
   |   |   |   |   |   |    -------   1 = Error bit
   |   |   |   |   |   |
   |   |   |    -------------------       Don't care
   |   |   |
   |   |    -----------------------   1 = Drive number
   |   |
   -------------------------------        Don't care
```

3.13.2 WINCHESTER ROM

The Winchester ROM is designed to interface to the system ROM software, specifically, the system disk DSR. It is located on the Winchester controller board, but is addressed by the system processor. It's address, as determined by the hardware, is 0F8000H. The convention locates the ROM at the address (as seen by the software) of 0F400:4000H.

The ROM contains software to interface to the system ROM disk DSR and to drive the Winchester controller. It also contains additional software to allow booting the system from the Winchester disk, formatting the disk, and running diagnostics (power-up and advanced) on the controller and disk.

3.13.2.1 Limitations. The DSR and other utilities provided by the system ROM limit the types of Winchester drives which can be used by the system. The limits are as follows;

* X x Y cylinders per drive. where $1 < X < 256$ and $1 < Y < 15$.
* 16 surfaces per drive.
* 17 sectors per track.
* 512 bytes per sector.
* 255 error retries
* 11-bits error burst length

Most of the routines within the ROM are driven by data structures which describe the type of drive completely. The system is powered up assuming the following drive parameters;

153 cylinders
4 surfaces
125 first track of reduced write current
64 first track of write precompensation
1 error retry
11-bit error burst length
3-millisecond step option

If the default parameters are not correct for the type of drive in use, the Initialize Winchester disk system option call must be done to setup the correct parameters. Note that the system can always boot the first sector with the default parameters.

3.13.3 System Interface

The ROM is initialized to the system when it is called after power-up test by the system ROM. The system ROM will have tested the Winchester disk controller ROM to guarantee that it is functioning properly before calling it. To allow the system ROM to test and call it, the Winchester disk controller ROM contains a header defining the size of the ROM, the ROM's entry point, a version number, and an identification message preceded by the message length.

The entry point called by the system ROM is required to do any device dependent initialization and, optionally, to boot the system from the device which the called ROM serves. For the Winchester disk, the operations are as follows.

* Setup the ROM's RAM area in the system and set the device installed bit in the system configuration word.
* If the caller has passed the "do not boot" flag (OFFFFH in register DX), return control to the caller. Otherwise, (O in

register DX) continue.

* If the user has entered an "ESC" character from the keyboard, return control to the system ROM (boot from the diskette).

* Otherwise, display the Winchester disk controller ROM signon message and execute the controllers powerup tests.

* Test all ROMs with a lower priority than the Winchester disk controller ROM and then call them with the "do not boot" flag set (DX = 0FFFFH) to allow them to do any initialization of associated hardware.

* Read in the boot sector from the disk, check it for usability, and jump to the code in the boot sector.

* If any errors occur in the above area, control is returned to the system ROM.

3.13.3.1 System RAM usage. The Winchester disk ROM uses 30 kbytes of RAM in the system RAM area. This RAM is allocated after RAM used by other previously called ROMs in a single data block pointed to by a word in the system vector area. The data structure of this vector area is given in Table 3-12

Table 3-12 Controller Usage of RAM

ADDRESS	USER	VALUE
0000:0180	SYSTEM ROM U63	RAM SEGMENT ADDRESS FOR ROM @ F400:A000
0000:0182	SYSTEM ROM U63	LENGTH OF RAM SEGMENT IN BYTES
0000:0184	F400:0000 ROM	RAM SEGMENT ADDRESS FOR ROM @ F400:0000
0000:0186	F400:0000 ROM	LENGTH OF RAM SEGMENT IN BYTES
0000:0188	F400:2000 ROM	RAM SEGMENT ADDRESS FOR ROM @ F400:2000
0000:018A	F400:2000 ROM	LENGTH OF RAM SEGMENT IN BYTES
0000:018C	WINDISK ROM	RAM SEGMENT ADDRESS FOR ROM @ F400:0000
0000:018E	WINDISK ROM	LENGTH OF RAM SEGMENT IN BYTES (30H)
0000:0184	F400:6000 ROM	RAM SEGMENT ADDRESS FOR ROM @ F400:6000
0000:0186	F400:6000 ROM	LENGTH OF RAM SEGMENT IN BYTES
0000:0184	OPTION ROM U62	RAM SEGMENT ADDRESS FOR ROM @ F400:8000
0000:0186	OPTION ROM U62	LENGTH OF RAM SEGMENT IN BYTES

All accesses to the Winchester disk controller RAM area are through the segment pointer at 0000:018CH. Note that since the Winchester disk controller ROM is located at in segment 0F400H, that the segment pointer location can also be reached from the code segment at address 0F400:C18CH.

The segment pointer allows the Winchester disk controller RAM area to be located anywhere, but care must be taken if the area is moved after the system is initialized. If this is done, the Winchester disk system must be reinitialized with the Winchester disk option call "0" (Initialize System) after the RAM area is moved and the vectors are set to the new values. This can be accomplished by passing the new segment address in DS and 000CH as the pointer to the initialization data (see paragraph 3.13.6.1, "Initialize Winchester Disk System").

3.13.4 Power-up Testing

The Winchester disk controller is tested to determine if it is working properly by using it's own internal diagnostics, the controller diagnostic, and the RAM diagnostic. Failures are reported as system errors 11xx where xx indicates the error received. If an error occurs, control is returned to the system ROM.

3.13.4.1 Booting from the Winchester. The next step after power-up testing of the controller is to go through the Winchester Boot sequence. Only drive 4 (E: for MSDOS) can be booted. If drive 5 is connected to the controller, it can be used for data only.

The first thing the boot procedure does is to poll the drive for the "ready" condition. If the drive is not ready (as would be true after power on) the ROM routines will wait about 30 seconds for the ready condition. If the user presses the "ESC" key at any time during this wait, control will be returned to the system ROM.

3.13.4.2 Error Recovery. The error recovery procedures depend on the error. For hardware controller errors (time-outs), the controller is reset and no retries are attempted. A hardware error code will be returned from the disk DSR.

For disk drive errors (seek incomplete, write fault etc), no retries are reported and the disk DSR will return the hardware error code.

For read data operations, if the data is correctable, it is corrected and no error is reported directly. A DSR "Read Soft Retry Status" will report this error.

For uncorrectable errors, retries are done with a restore before each retry. If the retry does not succeed, the data buffer is filled with "CCH" when the data cannot be read at all, or the uncorrected data if it can be read but contains an ECC error.

For other operation errors, retries are done with a restore before each retry.

3.13.5 Error Reporting

The disk DSR is capable of reporting only a few errors. The power-up boot can report more but not all. Table 3-13 is a listing of errors reported by the disk controller and the codes reported by the DSR.

Table 3-13 Winchester DSR Error Codes

	REPORTED ERROR		CONTROLLER ERROR	
	20H	Hardware failure	01H	No index detected
	20H	Hardware failure	02H	No seek complete
	20H	Hardware failure	03H	Write fault
	20H	Hardware failure	04H	DRIVE NOT READY during operation
	20H	Hardware failure	06H	Track 00 not found
	10H	CRC error	10H	ID field read error
	10H	CRC error	11H	Uncorrectable data error
	02H	Disk format error	12H	Address mark not found
	04H	Record not found	14H	Record not found
	40H	Seek error	15H	Seek Error
	00H	No error (on RETURN)	18H	Correctable data error
	10H	CRC error (soft stat)	18H	Correctable data error
	01H	Command error	19H	Bad track flag detected
	02H	Disk format error	1AH	Format error
	01H	Command error	1CH	Illegal access to alternate track
*	01H	Command error	1DH	Illegal track for format alt. usage
	02H	Disk format error	1EH	Expected alternate track, isn't
*	01H	Command error	1FH	Alternate track = bad track
*	01H	Command error	20H	Invalid Command
*	01H	Command error	21H	Illegal disk address
*	20H	Hardware failure	30H	RAM diagnostic failure
*	20H	Hardware failure	31H	Program memory checksum error
*	20H	Hardware failure	32H	ECC diagnostic failure

* These errors should NEVER be encountered by the DSR.

The errors which could be reported during booting are the controller errors shown in Table 3-13 and Table 3-14. All errors reported by boot have the format "SYSTEM ERROR - 11xx", where "xx" is the error code.

Table 3-14 Displayed Error Codes

All errors will have the following message displayed:

** SYSTEM ERROR - 11xx **

Where the xx is the EXTENDED ERROR, listed below.

EXTENDED ERROR	EXPLANATION
33H	Status error on REQUEST SENSE STATUS command
40H	Time-out rx while waiting for WRITE DATA mode
41H	READ MODE rx while waiting for WRITE DATA mode
42H	COMMAND MODE rx while waiting for WRITE DATA mode
43H	STATUS MODE rx while waiting for WRITE DATA mode
44H	WRITE MODE rx while waiting for READ DATA mode
45H	Time-out rx while waiting for READ DATA mode
46H	COMMAND MODE rx while waiting for READ DATA mode
47H	STATUS MODE rx while waiting for READ DATA mode
48H	WRITE MODE rx while waiting for COMMAND mode
49H	READ MODE rx while waiting for COMMAND mode
4AH	Time-out rx while waiting for COMMAND mode
4BH	STATUS MODE rx while waiting for COMMAND mode
4CH	WRITE MODE rx while waiting for STATUS mode
4DH	READ MODE rx while waiting for STATUS mode
4EH	COMMAND MODE rx while waiting for STATUS mode
4FH	Time-out rx while waiting for STATUS mode
51H	Disk not ready
52H	CRC error
53H	Seek error
54H	Sector-not-found error
55H	Disk (unknown) error (controller failure)
56H	Not a TI system disk
57H	Disk format error
58H	Bad boot sector CRC or bad controller
59H	SYSTEM ROM version doesn't support Winchester

3.13.6 Hardware Interface Routines

This interface to the Winchester disk system is provided to allow additional functions to be implemented in a straightforward way. The calls are meant to provide a method of interfacing with the hardware in a manner that is more or less hardware independent.

This interface is used by doing a long "call" through the first double word in the Winchester disk controller ROM's RAM area. The opcode for the operation should be in register AH. Other registers' usage is explained with each operation. A useful method of doing this many times is shown below.

```
WINROM DD   00000000                    ;LOCAL PLACE TO STORE VECTOR
                                        ;TO ROM.
       ...

       PUSH ES                          ;THIS CODE IS RUN FIRST
       XOR  AX,AX
       MOV  ES,AX
       MOV  ES,ES:WORD PTR 18CH         ;GET WINCH RAM SEGMENT INTO ES
       LES  AX,ES:DWORD PTR 0000        ;GET VECTOR FOR WINCH ROM
       MOV  WORD PTR WINROM+2,ES        ;SAVE IN OUR DATA AREA
       MOV  WORD PTR WINROM,AX          ;
       POP  ES

       .....

       MOV  AH,OPCODE                   ;SET OPCODE INTO AH
       CALL WINROM                      ;GO DO THE OPERATION
```

The operations available from this entry point are explained in the following paragraphs.

3.13.6.1 Initialize Winchester Disk System.

OPCODE: AH = 00H
ENTRY: DS:SI = POINTER TO DATA BLOCK

OFFSET	VALUE/USE
00H	(WORD) SECTOR SIZE IN BYTES
02H	(BYTE) TRACK SIZE IN SECTORS
03H	(BYTE) NUMBER OF SURFACES
04H	(BYTE) NUMBER OF CYLINDERS ON DISK
05H	(BYTE) NUMBER OF ERROR RETRIES
06H	(WORD) REDUCED WRITE CURRENT CYLINDER
08H	(WORD) WRITE PRECOMP START CYLINDER
0AH	(BYTE) STEP OPTION
0BH	(BYTE) ERROR BURST CORRECTED LENGTH

EXIT: AL = ERROR CODE
USED: AX, BX

This operation tells the disk subsystem what type of Winchester drive is being used. It sets up the hardware and software data structures so that a user can just call the DSR to use the drive.

3.13.6.2 Check Winchester ROM Version.

OPCODE: AH = 01H
ENTRY: NONE
EXIT: AX = BCD ROM VERSION NUMBER
USED: AX

EXAMPLE: IF ROM IS V1.23 THEN AX WILL RETURN 0123H

This operation returns the Winchester ROM version number. This is often useful for software compatibility checks.

3.13.6.3 Request Controller Error Sense.

```
OPCODE:    AH = 02H
ENTRY:     DS:SI = ADDRESS OF SIX BYTE DATA BLOCK
EXIT:      AL = ERROR CODE
           Z = SET IF NO ERROR
           DATA BLOCK CONTAINS WHAT CONTROLLER RETURNED.
USED:      AX,CX,SI,DI
```

This operation gets error information from the controller and returns an error code. If the controller hardware is broken, appropriate error codes are returned.

3.13.6.4 Send Winchester Controller Command.

```
OPCODE:    AH = 03H
ENTRY:     DS:SI = ADDRESS OF SIX BYTE DATA BLOCK CONTAINING
           COMMAND AND OTHER DATA (SEE HARDWARE SPEC)
EXIT:      AL = ERROR CODE IF C FLAG IS SET
           Z = SET, C = RESET IF NO ERROR
           Z = SET, C = SET IF TIMEOUT
           Z = RESET, C = SET IF IMPROPER CONTROLLER MODE.
USED:      AX,CX,SI
```

This operation sends a command to the controller. It does not wait for a response.

3.13.6.5 Get Data From the Winchester Controller.

```
OPCODE:    AH = 04H
ENTRY:     ES:DI = ADDRESS OF BUFFER TO RECEIVE DATA
           CX = NUMBER OF BYTES OF DATA TO GET
EXIT:      AL = ERROR CODE IF C FLAG IS SET
           Z = SET, C = RESET IF NO ERROR
           Z = SET, C = SET IF TIMEOUT
           Z = RESET, C = SET IF IMPROPER CONTROLLER MODE
USED:      AX,CX,DI
```

This operation waits for the controller to provide data and then puts it in to the users buffer. It will wait about 1 second before returning a time-out error. If the controller is in the COMMAND or STATUS state, an appropriate error code is returned.

3.13.6.6 Write Data to the Winchester Controller.

```
OPCODE:    AH = 05H
ENTRY:     ES:DI = ADDRESS OF DATA BUFFER TO TRANSMIT
           CX = NUMBER OF BYTES OF DATA TO PUT
EXIT:      AL = ERROR CODE IF C FLAG IS SET
           Z = SET, C = RESET IF NO ERROR
           Z = SET, C = SET IF TIMEOUT
           Z = RESET, C = SET IF IMPROPER CONTROLLER MODE
USED:      AX, CX, DI
```

This operation waits for the controller to ask for data and then writes from the users buffer to the controller. It will wait about 1 second before returning a time-out error. If the controller is in the command or status state, an appropriate error code is returned.

3.13.6.7 Get Status from Winchester Controller..

```
OPCODE:    AH = 06H
ENTRY:     NONE
EXIT:      AL = ERROR CODE IF C FLAG IS SET
           Z = SET, C = RESET IF NO ERROR
           Z = SET, C = SET IF TIMEOUT
           Z = RESET, C = SET IF CONTROLLER MODE IS NOT STATUS
           Z = RESET, C = RESET IF STATUS INDICATES CONTROLLER
           HAS AN ERROR.
USED:      AX, CX
```

This operation waits for the status return from the controller. It will wait about 1 second before returning a time-out error. If the controller is in the COMMAND or data transfer state, an appropriate error code is returned.

3.13.6.8 Get and Compare Data From the Winchester Controller.

```
OPCODE:    AH = 07H
ENTRY:     ES:DI = ADDRESS OF BUFFER TO RECEIVE DATA
           CX = NUMBER OF BYTES OF DATA TO GET
EXIT:      AL = ERROR CODE IF C FLAG IS SET
           Z = SET, C = RESET IF NO ERROR
           Z = SET, C = SET IF TIMEOUT
           Z = RESET, C = SET IF IMPROPER CONTROLLER MODE
           Z = RESET, C = RESET IF DATA DOES NOT COMPARE
           IF NO COMPARE, DI TO THE MISCOMPARED DATA
USED:      AX, CX, DI
```

This operation waits for the controller to provide data and then compares it with the data in the user's buffer. If the data does not compare, the data pointer (DS:DI) is set to point to the data address that does not compare. After a wait of about 1 second the controller returns a time-out error. If the controller is in the COMMAND or STATUS state, an appropriate error code is returned.

3.13.6.9 Enable Data and Status Interrupt from Controller.

```
OPCODE:    AH = 08H
ENTRY:     NONE
EXIT:      NONE
USED:      AX
```

This operation enables the Winchester controller interrupts to the system bus. Note that this operation does not enable the system interrupts from the interrupt controller or the processor interrupt.

3.13.6.10 Enable Status Interrupt from Controller.

```
OPCODE:    AH = 09H
ENTRY:     NONE
EXIT:      NONE
USED:      AX
```

This operation enables the Winchester controller interrupts to the system bus. Note that this operation does not enable the system interrupts from the interrupt controller or the processor interrupt.

3.13.6.11 Disable Data and Status Interrupt from Controller.

```
OPCODE:   AH = 0AH
ENTRY:    NONE
EXIT:     NONE
USED:     AX
```

This operation disables the Winchester controller interrupts to the system bus. Note that this operation does not disable the system interrupts from the interrupt controller or the processor interrupt.

3.13.6.12 Poll for Controller Request.

```
OPCODE:   AH = 0BH
ENTRY:    NONE
EXIT:     Z = SET IF REQUEST IS NOT ACTIVE
          Z = RESET IF REQUEST IS ACTIVE
USED:     AX
```

This operation can be used to determine when the controller is ready for "COMMAND", "STATUS", "DATA IN" or "DATA OUT".

3.13.6.13 Format a Track.

```
OPCODE:   AH = 0CH
ENTRY:    DL = DRIVE NUMBER (4,5)
          DH = INTERLEAVE FACTOR
          CX = LOGICAL TRACK NUMBER TO FORMAT
     The drive parameters must have been set using OP 0.
EXIT:     AL = ERROR CODE, 0 IF OK.
          CX = TRACK NUMBER OF ERROR IF THERE IS AN ERROR
USED:     AX,BX,CX,DX,SI,DI
```

This operation can be used by formatting routines to format a track on the Winchester disk. The drive parameters must have been set up by a call to operation "0". The logical track number can be found by multiplying the cylinder number by the number of surfaces and adding in the surface number. The interleave factor is typically 12 or 13 for optimum use of the DSR to read sequential sectors. The error code returned is the controller error code with extentions for such conditions as time-outs. Note that this operation always does a RESTORE operation before the track format, so it is slow to format a disk.

3.13.6.14 Format an Alternate Track.

```
OPCODE:    AH = 0DH
ENTRY:     DL = DRIVE NUMBER (4,5)
           DH = INTERLEAVE FACTOR
           CX = LOGICAL TRACK NUMBER TO FORMAT
           BX = LOGICAL TRACK NUMBER of ALTERNATE
      The drive parameters must have been set using OP 0.
EXIT:      AL = ERROR CODE, 0 IF OK.
           CX = TRACK NUMBER OF ERROR IF THERE IS AN ERROR
USED:      AX,BX,CX,DX,SI,DI
```

This operation can be used by formatting routines to map a bad track to an alternate track. The drive parameters must have been set up by a call to operation "0". The logical track number can be found by multiplying the cylinder number by the number of surfaces and adding in the surface number. The interleave factor is typically 12 or 13 for optimum use of the DSR to read sequential sectors. The error code returned is the controller error code with extensions for such conditions as time-outs.

3.13.6.15 Format a Track as Bad.

```
OPCODE:    AH = 0EH
ENTRY:     DL = DRIVE NUMBER (4,5)
           DH = INTERLEAVE FACTOR
           CX = LOGICAL TRACK NUMBER TO FORMAT
      The drive parameters must have been set using OP 0.
EXIT:      AL = ERROR CODE, 0 IF OK.
           CX = TRACK NUMBER OF ERROR IF THERE IS AN ERROR
USED:      AX,BX,CX,DX,SI,DI
```

This operation can be used by formatting routines to format a track that has a defect so that read operations will not miss the defect. The drive parameters must have been set up by a call to operation "0". The logical track number can be found by multiplying the cylinder number by the number of surfaces and adding in the surface number. The interleave factor is typically 12 or 13 for optimum use of the DSR to read sequential sectors. The error code returned is the controller error code with extentions for such conditions as time-outs. Note that this operation always does a restore operation before the track format.

3.13.6.16 Check the Track Format.

```
OPCODE:   AH = 0FH
ENTRY:    DL = DRIVE NUMBER (4,5)
          DH = INTERLEAVE FACTOR
          CX = LOGICAL TRACK NUMBER TO CHECK
      The drive parameters must have been set using OP 0.
EXIT:     AL = ERROR CODE, 0 IF OK.
          CX = TRACK NUMBER OF ERROR IF THERE IS AN ERROR
USED:     AX,BX,CX,DX,SI,DI
```

This operation can be used by formatting routines to check a track for proper format. This routine does not report errors for tracks which have been formatted as bad tracks or alternate tracks unless the ID fields are incorrect. The drive parameters must have been set up by a call to operation "0". The logical track number can be found by multiplying the cylinder number by the number of surfaces and adding in the surface number. The interleave factor is typically 12 or 13 for optimum use of the DSR to read sequential sectors. The error code returned is the controller error code with extentions for such conditions as time-outs.

3.13.6.17 Format a Winchester Drive.

```
OPCODE:   AH = 10H
ENTRY:    DL = DRIVE NUMBER (4,5)
          DH = INTERLEAVE FACTOR
          CX = LOGICAL TRACK NUMBER TO BEGIN FORMAT
      The drive parameters must have been set using OP 0.
EXIT:     AL = ERROR CODE, 0 IF OK.
          CX = TRACK NUMBER OF ERROR IF THERE IS AN ERROR
USED:     AX,BX,CX,DX,SI,DI
```

This operation can be used by formatting routines to format a winchester drive. The drive parameters must have been set up by a call to operation "0". The logical track number can be found by multiplying the cylinder number by the number of surfaces and adding in the surface number. The interleave factor is typically 12 or 13 for optimum use of the DSR to read sequential sectors. The error code returned is the controller error code with extentions for such conditions as time-outs. If an error occurs during the drive formatting operation, register CX will return the track in error. If the formatting operation must be completed, increment the track number and call the routine again. This might be necessary if a drive defect fell directly on an address mark or ID field.

3.13.6.18 Dump Data From the Winchester Controller.

```
OPCODE:   AH = xxH
ENTRY:    CX = NUMBER OF BYTES OF DATA TO READ
EXIT:     AL = ERROR CODE IF C FLAG IS SET
          Z = SET, C = RESET IF NO ERROR
          Z = SET, C = SET IF TIMEOUT
          Z = RESET, C = SET IF IMPROPER CONTROLLER MODE
USED:     AX, CX
```

This operation waits for the controller to provide data and then reads and ignores it. It will wait about 1 second before returning a time-out error. If the controller is in the COMMAND or STATUS state, an appropriate error code is returned.

Section 4

ASSEMBLY DRAWINGS AND LISTS OF MATERIALS

This section contains assembly drawings and lists of materials applicable to the Texas Instruments Professional Computer.

Drawings not available in time for printing:

Color Display Unit	2223219
Winchester Disk Controller	2223220
Parallel Test Plug Assembly	2223276
PWB, Parallel Test Plug	2223277
Configuration, Diskette Drive	2223279
Power Cord AC	0996289
Communications Loopback Plug	2207985

2223003 | 1

NOTES UNLESS OTHERWISE SPECIFIED

[1] MAXIMUM COMPONENT HEIGHT ABOVE THE BOARD SHALL BE 12.7 IN AREA INDICATED, 15.7 ALL OTHER AREAS

[2] MAXIMUM LEAD LENGTH BELOW THE BOARD SHALL BE 3.90

[3] MARK APPROPRIATE DASH NUMBER AND REVISION LETTER IN SPACE INDICATED PER PROCESS 3

[4] MARK SITE/DATE CODE AND SERIAL NUMBER IN SPACE INDICATED PER ITEM 100 PARAGRAPH 4.C AND PROCESS 3

5 CAUTION THIS ASSEMBLY AND CERTAIN COMPONENTS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE. OPERATOR AND EQUIPMENT GROUND AND PACKAGING IS REQUIRED. STATIC SENSITIVE COMPONENTS ARE: U1 THRU U67

6. INSTALL ITEM 98 (QTY 4) TO E2, E4, E6 & E20 (SINGLE PIN ONLY)

[7] APPLY ITEM 114 (LOCKTITE SEALANT) AFTER INSTALLATION OF ITEMS 95 AND 111 ON SCREW END

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	CN 493819 (D)	5-28-81	M Bush
	(1) LM UPDATE		
B	CN493821(E)	6-29-81	M Bush
	(1) IT 60 WAS QTY 3 (2) IT 60A WAS CR1, CR2, CR3 (3) IT 46 WAS PN 2211109-2 (4) IT 12 WAS PN 2220400-2 (5) ADD IT 103 & 104		
C	CN 497847 (D)	8-3-81	M Bush
	(1) UPDATE LM (2) CREATE -5001 LM (3) ADD DASH NUMBER CHART		
D	CN 502163 (D)	8-17-81	M Bush
	(1) LM UPDATE		
E	CN476090 (B) LAMB	10-4-82	M Bush
	(1) CHNG PER ENG REDESIGN		
F	CN 502198 (D)	11-1-81	M Bush
	(1) LM UPDATE (2) CHNG PER ENG SPEC		

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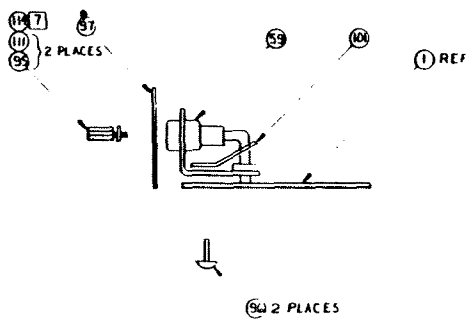


VIEW A
SH 2 (D-5)

PART NUMBER	DESCRIPTION
2223003-5001	MOTHERBOARD-PEGASUS, AUTO INSERT
2223003-0001	MOTHERBOARD-PEGASUS

CONVERSION CHART	
mm	INCHES
0.25	.010
0.5	.02
1.5	.06
3.90	.154
12.7	.50
15.7	.62
86.36	3.40
184.15	7.25

SEQ NO	IDENT	SPEC	NO	ADDITIONAL	NOTES
3	MARK	902-01	01	HGT 1.5 CLR WHT, (CAT 4)	3 4
2	SLDR	127-01	00	HAND SOLDER	
1	SLDR	124-02	00	WAVE SOLDER	
	PROCESS		CLASSIFICATION		

PROCESSES – FOR CORRELATION TO GOVT AND SPECIFICATIONS SEE TI DRAWING 7200

REV STATUS OF SHEETS		
REV	F	F
SH	1	2

TEST PROC	2223270-0001						
ASSEMBLY	2223003-0001	A	B	C	D	E	F
PWB	2223004-0001	B	B	B	C	C	E
DIAGRAM	2223005-0001				A	A	A

QTY 3	QTY 2	QTY 1	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

NEXT ASSY	USED ON
2223038	8755

APPLICATION

UNLESS OTHERWISE SPECIFIED

THIRD ANGLE PROJECTION

TEXAS INSTRUMENTS

SI-METRIC

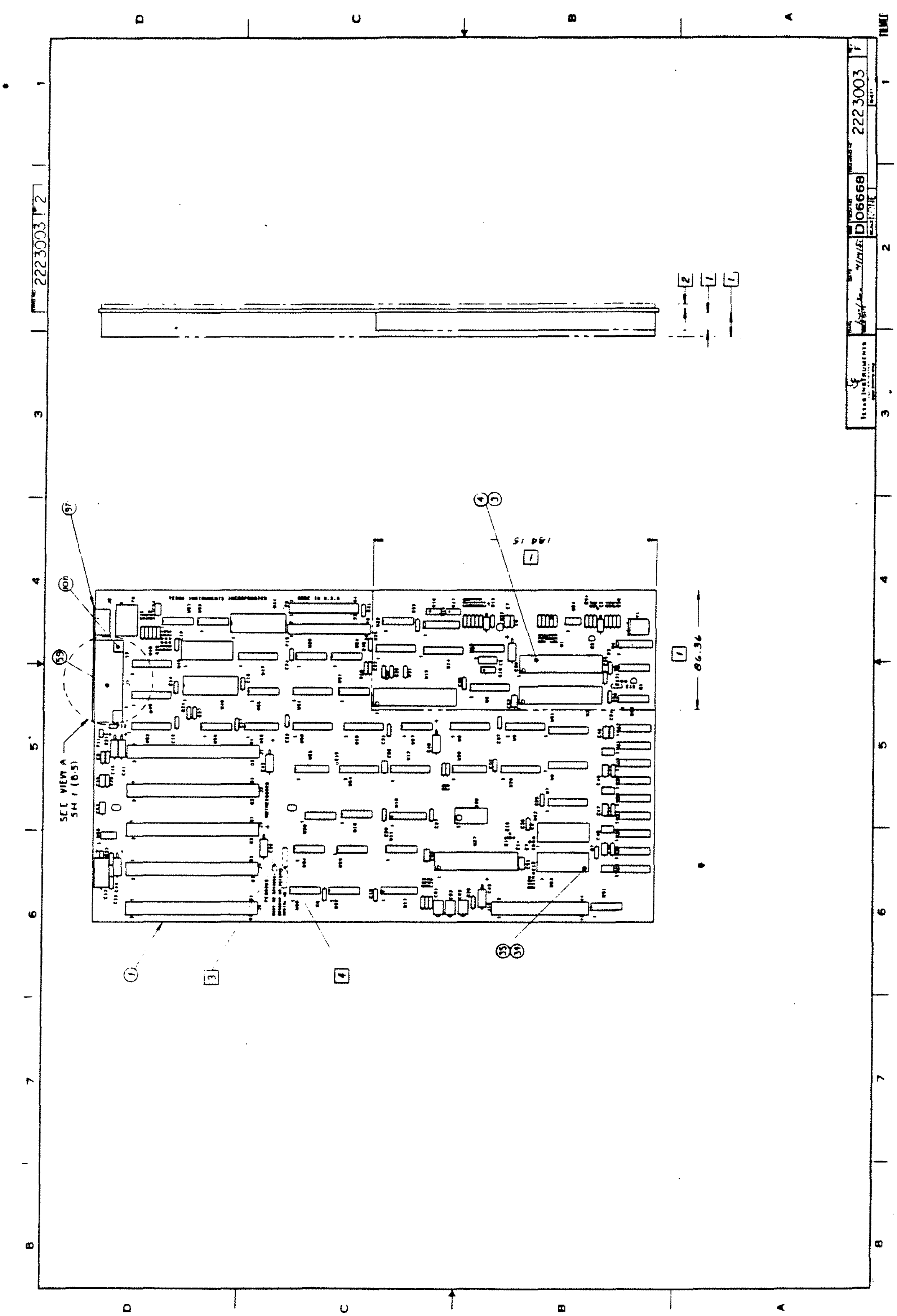
MOTHERBOARD-PEGASUS

SIZE D | FSCM NO 06668 | DRAWING NO 2223003

SCALE NONE | SHEET 1 OF 2

320

ILM


2223003
D06668
TEXAS INSTRUMENTS
SEE VIEW A
SH 1 (B-5)
84.36
194.15

LIST OF MATERIALS

11/24/82

PART NUMBER   REV   DESCRIPTION...............................
2223003-0001   F   MOTHERBOARD - PEGASUS

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0002	00001.000	2223005-0001	DIAGRAM,LOGIC, MOTHERBOARD	EA
0004	00002.000	2210188-0018	SOCKET,DIP,40-PINS,LOW PROFILE SEE T -I DRAWING	EA
0004A			XU1,XU2 SEE T -I DRAWING	
0009	00001.000	2210835-0010	CRYSTAL,15.00 MHZ,HC-18/U MOD CASE SEE TI- DRAWING	EA
0009A			Y1 SEE TI- DRAWING	
0013	00005.000	2211342-0016	CONN,CARD-EDGE,31 DUAL POS,NO EARS SEE TI- DRAWING	EA
0013A			J1,J2,J3,J4,J5 SEE TI- DRAWING	
0014	00001.000	0996166-0005	HEADER,SOCKET,SHORT SOLDER T 6 CIRCUITS AMP - 350827-1	EA
0014A			P6 AMP - 350827-1	
0024	00001.000	2210704-0001	IC,LS280,9-BIT ODD/EVEN PARITY GEN/CHK V-LIST-LS280 BURN-IN	EA
0024A			U31 V-LIST-LS280 BURN-IN	
0026	00001.000	2210293-0003	DELAY MODULE, TAPPED, 3NS RISE TIME MAX SEE TI- DRAWING	EA
0026A			U30 SEE TI- DRAWING	
0032	00001.000	2211342-0015	CONN,CARD-EDGE,22 DUAL POS,NO EARS SEE TI- DRAWING	EA
0032A			J10 SEE TI- DRAWING	
0035	00002.000	2210188-0016	SOCKET,DIP,24-PIN,LOW PROFILE SEE T -I DRAWING	EA
0035A			XU62,XU63 SEE T -I DRAWING	
0041	00001.000	0996151-0005	HEADER,17 PINS PER ROW,STRAIGHT,DBL ROW 5935-0900-000	EA
0041A			P9, 5935-0900-000	
0042	00001.000	0996151-0002	HEADER,20 PINS,STRAIGHT,DOUBLE ROW 22526--65611-140	EA
0042A			P13 22526--65611-140	
0043	00001.000	0996151-0008	HEADER,PIN,3 PINS, STR. DOUBLE ROW 022526-65611-106	EA
0043A			E1-E6 022526-65611-106	
0044	00004.000	2211348-0002	HEADER,1-ROW 2-POS,100 CENTER GOLD SEE TI- DRAWING	EA
0044A			E17-E18,E19-E20,J11-J12 SEE TI- DRAWING	
0054	00001.000	2211079-0006	IC, +5 VOLT REGULATOR,BURN-IN SEE TI- DRAWING	EA
0054A			U22 SEE TI- DRAWING	
0058	00001.000	2220495-0001	CONN,PCB-MTG,5 FEMALE CONTACTS,RT ANGLE SEE TI- DRAWING	EA
0058A			J8 SEE TI- DRAWING	
0059	00001.000	2220488-0003	CONNECTOR,RECEPTACLE,PCB,25-PINS SEE TI- DRAWING	EA
0059A			J7 SEE TI- DRAWING	
0060	00001.000	0972537-0003	DIODE,LED RED RT ANGLE 072619-550-0406	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2223003-0001	F	MOTHERBOARD - PEGASUS

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0060A			CR1	
			072619-550-0406	
0078	00001.000	0972227-0014	RESISTOR, 100K VARIABLE-CERMET ELEMENT	EA
			032997-3292W-1-104	
0078A			R17	
			032997-3292W-1-104	
0079	00001.000	0972227-0013	RESISTOR, 50000 OHM, 22-TURN TRIMMER	EA
			SEE TI- DRAWING	
0079A			R18	
			SEE TI- DRAWING	
0080	00001.000	0972227-0009	RES,VAR, 5000 OHMS,1/2 WATT, CERMET	EA
			032997-3292W-1-502	
0080A			R19	
			032997-3292W-1-502	
0083	00001.000	0972927-0025	CAPACITOR,82PF 500V 5% FIX,MICA DIELECTR	EA
			MIL -CMR05E820-JOD	
0083A			C5	
			MIL -CMR05E820-JOD	
0089	00001.000	0972763-0021	CAP.,FIXED,AXIAL LEAD,.047 UF,+80%,-20%	EA
			1632-0000-000	
0089A			C11	
			1632-0000-000	
0090	00001.000	2211700-0002	CAP, 220UF, 6.3V, 20%	EA
			SEE TI- DRAWING	
0090A			C12	
			SEE TI- DRAWING	
0093	00002.000	2211878-0002	TRANS,MPS6602,NPN,COMPLEMENTRY DRIVER	EA
			SEE TI- DRAWING	
0093A			Q1,Q2	
			SEE TI- DRAWING	
0095	00002.000	0532348-0401	STUD, EXTENSION-CRES	EA
0096	00002.000	0972446-0013	RIVET,.116 DIA 5/16 LG DOME HD ALUM	EA
			- - -000	
0097	00001.000	2223036-0001	PLATE,KEYBOARD PLUG	EA
			1678-3036-009	
0098	00004.000	0972487-0001	JUMPER PLUG,CONNECTOR BLACK	EA
			5935-0900-000	
0100	00001.000	0994396-0001	PROC., SITE/DATE CODE AND SERIALIZATION	EA
0101	00001.000	0235728-0125	TAB TIN PL BRS STUD DIA.130X.032 THK	EA
			AMP -42822-2	
0103	00001.000	0972537-0004	LED,YELLOW,RT ANG PCB MTG,2.3V,5.0VR	EA
			SEE TI- DRAWING	
0103A			CR2	
			SEE TI- DRAWING	
0104	00001.000	0972537-0002	DIODE,LED GREEN RT ANGLE	EA
			072619-550-0206	
0104A			CR3	
			072619-550-0206	
0110	REF	2223270-0001	SPECIFICATION,UNIT TEST-MOTHERBOARD	EA
0111	00001.000	0411100-0070	LOCKWASHER #4 INTERNAL TOOTH CRES	EA
			QPL - MS35333-70	
0113	AR	0411435-0408	TAPE,INSULATION,ELECT.1/4 IN	RL
			MMM - 56-1/4	
0114	AR	0415804-0005	SEALING COMPOUND,ANAEROBIC-BLUE GRADE C	OT
0999	00001.000	2223003-5001	MOTHERBOARD - PEGASUS - AUTO INSERT	EA
			1254-3004-005	
9999	00001.000	0239999-9999	COST, SHRINKAGE	EA

LIST OF MATERIALS

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PART NUMBER	REV	DESCRIPTION...........................
2223003-5001	F	MOTHERBOARD - PEGASUS - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	2223004-0001	PWB MOTHERBOARD	EA
			1669- -000	
0003	00001.000	2220419-0001	IC,MICROPROCESSOR,CPU	EA
			SEE TI- DRAWING	
0003A			U1	
			SEE TI- DRAWING	
0005	00001.000	2220424-0001	IC,MICROPROCESSOR BUS CONTROLLER	EA
			SEE TI- DRAWING	
0005A			U3	
			SEE TI- DRAWING	
0006	00001.000	2220414-0001	IC,TTL,CLOCK GENERATOR AND DRIVER	EA
			SEE TI- DRAWING	
0006A			U4	
			SEE TI- DRAWING	
0007	00003.000	2210720-0001	IC,LS373,OCTAL D-TYPE LATCHES	EA
			V-LIST-LS373 BURN-IN	
0007A			U5,U6,U7	
			V-LIST-LS373 BURN-IN	
0008	00004.000	2210702-0001	IC,LS273,OCTAL,D-FLIP-FLOP W/COM CLOCK	EA
			V-LIST-LS273 BURN-IN	
0008A			U47,U49,U50,U51	
			V-LIST-LS273 BURN-IN	
0010	00001.000	2220435-0001	IC,PROGRAMMABLE INTERRUPT CONTROLLER	EA
			SEE TI- DRAWING	
0010A			U46	
			SEE TI- DRAWING	
0011	00001.000	2220412-0001	IC,USART,PROG.COMMUNICATION INTERFERENCE	EA
			SEE TI- DRAWING	
0011A			U44	
			SEE TI- DRAWING	
0012	00001.000	2220626-0001	IC,MOS,16-BIT PRGMBL INTERVAL TIMER	EA
			SEE TI- DRAWING	
0012A			U45	
			SEE TI- DRAWING	
0015	00001.000	2210653-0001	IC,LS138,3-TO-8 LINE DECODER	EA
			V-LIST-LS138 BURN-IN	
0015A			U55	
			V-LIST-LS138 BURN-IN	
0016	00001.000	2210654-0001	IC,LS139,DUAL 2-TO-4 LINE DECODER	EA
			V-LIST-LS139 BURN-IN	
0016A			U53	
			V-LIST-LS139 BURN-IN	
0017	00001.000	2223052-0002	ROM,SYSTEM DECODE HAL12L6	EA
0017A			U54	
0018	00000.000	2211984-0007	IC,DMPAL12L6NC	EA
			SEE TI- DRAWING	
0018A			*U54,ALTERNATE FOR ITEM 17	
			SEE TI- DRAWING	
0019	00001.000	2211102-0001	IC,F4071BPCOR,QUAD,2-INPUT,4071-BURN-IN	EA
			SEE TI-DRAWING	
0019A			U58	
			SEE TI-DRAWING	
0020	00002.000	0972141-0057	NETWORK,RES. 4.7 K OHM 2 % 14 PIN DIP	EA
			BEC - 899-1-R4.7K	
0020A			U60,U66	
			BEC - 899-1-R4.7K	
0021	00001.000	2220445-0001	IC,DYNAMIC MEMORY CONTROLLER	EA
			SEE TI- DRAWING	
0021A			U27	
			SEE TI- DRAWING	
0022	00001.000	2223053-0001	ROM,MEMORY CONTROL, HAL16R4A	EA
			1669- -000	

LIST OF MATERIALS

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PART NUMBER   REV   DESCRIPTION...........................
2223003-5001   F   MOTHERBOARD - PEGASUS - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0022A			U28 1669- -000	
0023	00000.000	2211984-0011	IC,PMPAL16R4NC SEE TI- DRAWING	EA
0023A			*U28,ALTERNATE FOR ITEM 22 SEE TI- DRAWING	
0025	00001.000	2210689-0001	IC,LS221,DUAL ONE-SHOT V-LIST-LS221 BURN-IN	EA
0025A			U29 V-LIST-LS221 BURN-IN	
0027	00001.000	2210608-0001	IC,LS10,TRIPLE,3-INPUT NAND V-LIST-LS10 BURN-IN	EA
0027A			U9 V-LIST-LS10 BURN-IN	
0028	00001.000	2210614-0001	IC,LS20,DUAL,4-INPUT NAND V-LIST-LS20 BURN-IN	EA
0028A			U32 V-LIST-LS20 BURN-IN	
0029	00001.000	2210621-0001	IC,LS32,QUAD,2-INPUT OR V-LIST-LS32. BURN-IN	EA
0029A			U34 V-LIST-LS32 BURN-IN	
0030	00003.000	2210631-0001	IC,LS74,DUAL D FLIP-FLOP W/PSET & CLR V-LIST-LS74 BURN-IN	EA
0030A			U21,U33,U65 V-LIST-LS74 BURN-IN	
0031	00009.000	2211118-0005	IC,64K X 1-BIT RAM,350 NSEC,READ CY TIME	EA
0031A			U35,U36,U37,U38,U39	
0031B			U40,U41,U42,U43	
0033	00004.000	2210695-0001	IC,LS245,OCTAL BUS,XCIVER,3ST.OUTPUT V-LIST-LS245 BURN-IN	EA
0033A			U8,U12,U52,U61 V-LIST-LS245 BURN-IN	
0034	00001.000	2223064-0001	ROM,SYSTEMS SEE TI- DRAWING	EA
0034A			U63 SEE TI- DRAWING	
0036	00001.000	2220415-0001	IC,FLOPPY DISK CONTROLLER,PLASTIC SEE TI- DRAWING	EA
0036A			U13 SEE TI- DRAWING	
0037	00001.000	2220421-0001	IC,FLOPPY DISK SUPPORT LOGIC - - -000	EA
0037A			U14 - - -000	
0038	00001.000	2220418-0001	IC,FOUR PHASE CLOCK GENERATOR SEE TI- DRAWING	EA
0038A			U15 SEE TI- DRAWING	
0039	00001.000	2223054-0002	ROM FLOPPY SYSTEM CONTROL	EA
0039A			U19	
0040	00000.000	2211984-0006	IC,BLANK PROGRAMMABLE ARRAY OF GATES SEE TI- DRAWING	EA
0040A			*U19,ALTER FOR ITEM 39 SEE TI- DRAWING	
0045	00001.000	2211771-0001	IC,SN74LS628N,EXTERNAL, TEMPERATURE COMP SEE TI- DRAWING	EA
0045A			U16 SEE TI- DRAWING	

LIST OF MATERIALS

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PART NUMBER	REV	DESCRIPTION............................
2223003-5001	F	MOTHERBOARD - PEGASUS - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0046	00002.000	2211126-0001	IC, 1K X 4 BIT STATIC RAM - - -000	EA
0046A			U17,U18 - - -000	
0047	00001.000	0972999-4040	NETWORK 4040 -SEE TI DRAWING	EA
0047A			U11 -SEE TI DRAWING	
0048	00001.000	2210667-0001	IC,LS163,SYNC 4-BIT BINARY CNT,SYNC CLR V-LIST-LS163 BURN-IN	EA
0048A			U20 V-LIST-LS163 BURN-IN	
0049	00002.000	0222222-7416	NETWORK SN7416N -SN7416N	EA
0049A			U23,U24 -SN7416N	
0050	00001.000	2211059-0001	IC,7407N3,HEX/BUF/DVR,BURN-IN SEE TI- DRAWING	EA
0050A			U26 SEE TI- DRAWING	
0051	00002.000	2210694-0001	IC,LS244,OCTAL BUF/LINE DRIVER/RECEIVER V-LIST-LS244 BURN-IN	EA
0051A			U25,U48 V-LIST-LS244 BURN-IN	
0052	00001.000	2210604-0001	IC,LS04,HEX INVERTERS V-LIST-LS04 BURN-IN	EA
0052A			U10 V-LIST-LS04 BURN-IN	
0053	00001.000	2210727-0001	IC,LS393,DUAL,4-BIT BINARY COUNTER V-LIST-LS393 BURN-IN	EA
0053A			U56 V-LIST-LS393 BURN-IN	
0055	00001.000	0222225-2311	NETWORK LM311N,SN72311P SEE - TI DRAWING	EA
0055A			U64 SEE - TI DRAWING	
0056	00001.000	2211349-0001	IC,SN75189AN3, QUAD LINE RECEIVERS SEE TI- DRAWING	EA
0056A			U57 SEE TI- DRAWING	
0057	00001.000	0996304-0001	IC,LM386,AMPL,PWR,AUDIO	EA
0057A			U59	
0061	00004.000	0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM 1640-2132-000	EA
0061A			R10,R11,R34,R6 1640-2132-000	
0062	00005.000	0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0062A			R7,R8,R40,R41,R37 ROH - R-25	
0063	00003.000	0972946-0085	RES FIX 6.8K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0063A			R26,R27,R28 ROH - R-25	
0064	00003.000	0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0064A			R23,R24,R25 ROH - R-25	
0065	00004.000	0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM ROH - R-25	EA
0065A			R4,R21,R38,R45 ROH - R-25	

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223003-5001 F MOTHERBOARD - PEGASUS - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0067	00001.000	0972946-0017	RES FIX 10.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0067A			R22	
			ROH - R-25	
0068	00003.000	0972946-0105	RES FIX 47 K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0068A			R13,R14,R20	
			ROH - R-25	
0069	00001.000	0972946-0037	RES FIX 68.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0069A			R15	
			ROH - R-25	
0070	00003.000	0972946-0072	RES FIX 2.0K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0070A			R5,R3,R39	
			ROH - R-25	
0071	00001.000	0539370-0364	RES FIX FILM 604 OHM 1% .25 WATT	EA
			COR - NA55	
0071A			R12	
			COR - NA55	
0072	00008.000	0972946-0045	RES FIX 150 OHM 5 % .25 W CARBON FILM	EA
			SEE TI- DRAWING	
0072A			R29,R30,R31,R32	
			SEE TI- DRAWING	
0072B			R43,R44,R46,R47	
			SEE TI- DRAWING	
0073	00002.000	0972946-0058	RES FIX 510 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0073A			R1,R2	
			ROH - R-25	
0074	00001.000	0972946-0049	RES FIX 220 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0074A			R33	
			ROH - R-25	
0075	00001.000	0972934-0010	DIODE,1N755A 7.5 V 5% SIL VOLT REG	EA
			QPL - 1N755A	
0075A			CR4	
			QPL - 1N755A	
0076	00001.000	0539370-0465	RES FIX FILM 6.81K OHM 1% .25 WATT	EA
			COR - NA55	
0076A			R35	
			COR - NA55	
0077	00001.000	0539370-0441	RES FIX FILM 3.83K OHM 1% .25 WATT	EA
			COR - NA55	
0077A			R36	
			COR - NA55	
0081	00001.000	0972757-0019	CAP,FIXED CER 3300PF 10% 50V	EA
0081A			C3	
0082	00001.000	0418356-2353	CAP FIX 0.68 MF 50V 10% TANTALUM SOLID	EA
			QPL -M39003/1-2353	
0082A			C4	
			QPL -M39003/1-2353	
0084	00001.000	0972757-0009	CAP FIX CER 470PF 10% 50V	EA
0084A			C8	
0085	00001.000	0972924-0021	CAP FIX TANT SOLID 1.0 MFD 10 % 50 VOLT	EA
			QPL -M39003/1-2356	
0085A			C2	
			QPL -M39003/1-2356	
0086	00001.000	0972757-0043	CAPACITOR,15PF,10%,50WVDC,CERAMIC	EA
			SEE TI- DRAWING	

LIST OF MATERIALS

11/24/82

PART NUMBER   REV   DESCRIPTION..........................
2223003-5001   F   MOTHERBOARD - PEGASUS - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0086A			C1	
			SEE TI- DRAWING	
0087	00001.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS	EA
			004222-MC105E103Z	
0087A			C9	
			004222-MC105E103Z	
0088	00012.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	
0088A			C7,C10,C46,C47,C48,C49	
			COR CA-C03Z5U104Z050A	
0088B			C50,C51,C52,C53,C54,C55	
			COR CA-C03Z5U104Z050A	
0091	00027.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL	EA
			COR CA-C02Z5U102Z100A	
0091A			C6,C13,C14,C15,C16,C17,C18	
			COR CA-C02Z5U102Z100A	
0091B			C19,C20,C21,C22,C23,C24,C25	
			COR CA-C02Z5U102Z100A	
0091C			C26,C27,C28,C29,C30,C31,C32	
			COR CA-C02Z5U102Z100A	
0091D			C33,C34,C35,C36,C37,C57	
			COR CA-C02Z5U102Z100A	
0092	00008.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT	EA
			QPL -M39003/1-2304	
0092A			C38,C39,C40,C41,C42,	
			QPL -M39003/1-2304	
0092B			C43,C44,C45	
			QPL -M39003/1-2304	
0102	00001.000	2210600-0001	IC,LS00,QUAD,2-INPUT NAND	EA
			V-LIST-LS00 BURN-IN	
0102A			U67	
			V-LIST-LS00 BURN-IN	
0105	00001.000	0972946-0035	RES FIX 56.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0105A			R42	
			ROH - R-25	
0106	00002.000	0972757-0001	CAP,FIXED CERAMIC 100 PF 10% 50V	EA
			UC -C51C101K	
0106A			C56,C58	
			UC -C51C101K	
0107	00001.000	0972946-0083	RES FIX 5.6K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0107A			R48	
			ROH - R-25	
0108	00001.000	0972946-0047	RES FIX 180 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0108A			R16	
			ROH - R-25	
0109	00001.000	0972934-0011	DIODE,1N756A 8.2 V 5% SIL VOLT REG	EA
			QPL - 1N756A	
0109A			CR5	
			QPL - 1N756A	
0112	00001.000	0972946-0093	RES FIX 15K OHM 5% .25 W CARBON FILM	EA
			ROH - R-25	
0112A			R9	
			ROH - R-25	

NOTES UNLESS OTHERWISE SPECIFIED

[1] MAXIMUM COMPONENT HIEGHT ABOVE THE BOARD SHALL BE 9.6

[2] MAXIMUM LEAD LENGTH BELOW THE BOARD SHALL BE 2.3

[3] MARK APPROPRIATE REVISION LETTER IN SPACE INDICATED PER PROCESS 3

[4] MARK SITE DATE CODE AND SERIAL NUMBER IN SPACE INDICATED PER ITEM 44 PARAGRAPH 4.0 AND PROCESS 3

5. CAUTION THIS ASSEMBLY AND CERTAIN COMPONENTS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE. OPERATOR AND EQUIPMENT GROUND AND PACKAGE IS REQUIRED. STATIC SENSITIVE COMPONETS ARE: U1 THRU U39, Y1 AND Q1

[6] WIRE FROM VIDEO JACK (ITEM 56) MUST ATTACH TO J43 AS SHOWN PER PROCESS 2

[7] AS FOLLOWS: REWORK REQUIRED FOR PWB REV "*" AND "A" AND "E"

(7A) ON COMPONENT SIDE, CUT ETCH CONNECTED TO U18 PIN 1

(7B) ON CONDUCTOR SIDE, CUT ETCH CONNECTED TO U27 PIN 1

(7C) USING (ITEM 95) JUMPER U17 PIN 1 TO THE FEED THRU BELOW U27 AS SHOWN (COMP SIDE)

(7D) USING (ITEM 95) JUMPER FROM U27 PIN 1 TO U39 PIN 1 (COMP SIDE)

(7E) PLACE MYLAR TAPE (ITEM 96) ON BOTTOM OF CONNECTOR (ITEM 41) AS INDICATED

(7F) MARK NUMBER "2" IN SPACE INDICATED PER PROCESS 3 (COND SIDE)

(7G) ADD JUMPER ITEM 95 FROM C2 TO J41 PINS 19 AND 20 AS INDICATED (COND SIDE)

(7H) MARK PWB WITH (C) ON CONDUCTOR SIDE NEXT TO BOARD NUMBER

[8] BEND TAB (ITEM 56) 45° FROM OPTION PLATE (ITEM 55) AS INDICATED

[9] REMOVE AND DISCARD 2 PANHEAD SCREWS INSTALLED IN (ITEM 41) PRIOR TO ASSEMBLY

[10] APPLY ITEM 103 (LOCTITE C SEALANT) TO TO ENDS OF ITEM 100 (STUDDED STANDOFF) AFTER INSTALLATION

DWG NO 2223009 SH 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
E	CN 502186 (B) E. DeLeon	10 14 82	M Bail
	(1) REDRAWN PER ENGINEERING REDESIGN		
F	CN 502178 (D) Bav	11 4 82	M Bail
	(1) LM UPDATE (2) SH 2 Z 8-2 DELE IT'S 54 & 56		
	(3) FID ADD NOTE 7H		

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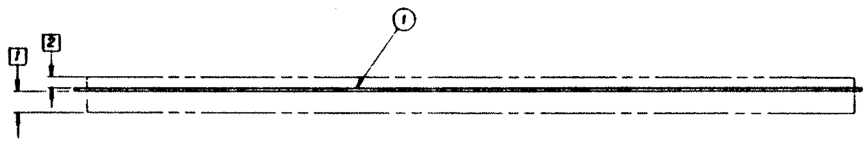
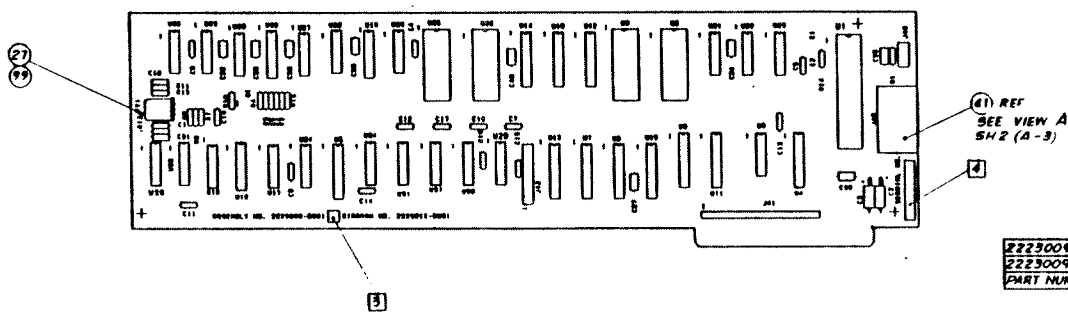




2223009-5001	ALPHA CRT CONTROLLER, AUTO INSERT
2223009-0001	ALPHA CRT CONTROLLER
PART NUMBER	DESCRIPTION

3 QTY	2 QTY	1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

SEQ NO	IDENT	F SPEC	NO	ADDITIONAL	NOTES
3	MARK	902-01	01	HGT 1.5 CLR WHT (CAT 4)	3 4
2	SLDR	127-01	00	HAND SOLDER	6
1	SLDR	124-02	00	WAVE SOLDER	

PROCESS / CLASSIFICATION

PROCESSES — FOR CORRELATION TO GOVT AND SPECIFICATIONS SEE TI DRAWING 726461

REV LEVEL BLOCK

TEST SPEC	2223271-0001	*	*
ASSEMBLY	2223009-0001	E	F
PWB	2223010-0001	B	B
DIAGRAM	2223011-0001	A	A

REV STATUS OF SHEETS

REV	F	F
SH	1	2

NEXT ASSY	USED ON
2223051	8755
2223050	8755

APPLICATION

UNLESS OTHERWISE SPECIFIED

HOLE TOLERANCE

THIRD ANGLE PROJECTION

DR	Carlos Lasi... 9-20-82
	MIKE BIEHL 6-8-82
	GRAY McCORD 6-10-82
	GRAY McCORD 6-10-82
	RALPH J CAPAN 6-10-82
	SUSAN BRIDGEN 6-10-82
	MIKE R. WOLF 6-11-82

TEXAS INSTRUMENTS INCORPORATED

SI-METRIC

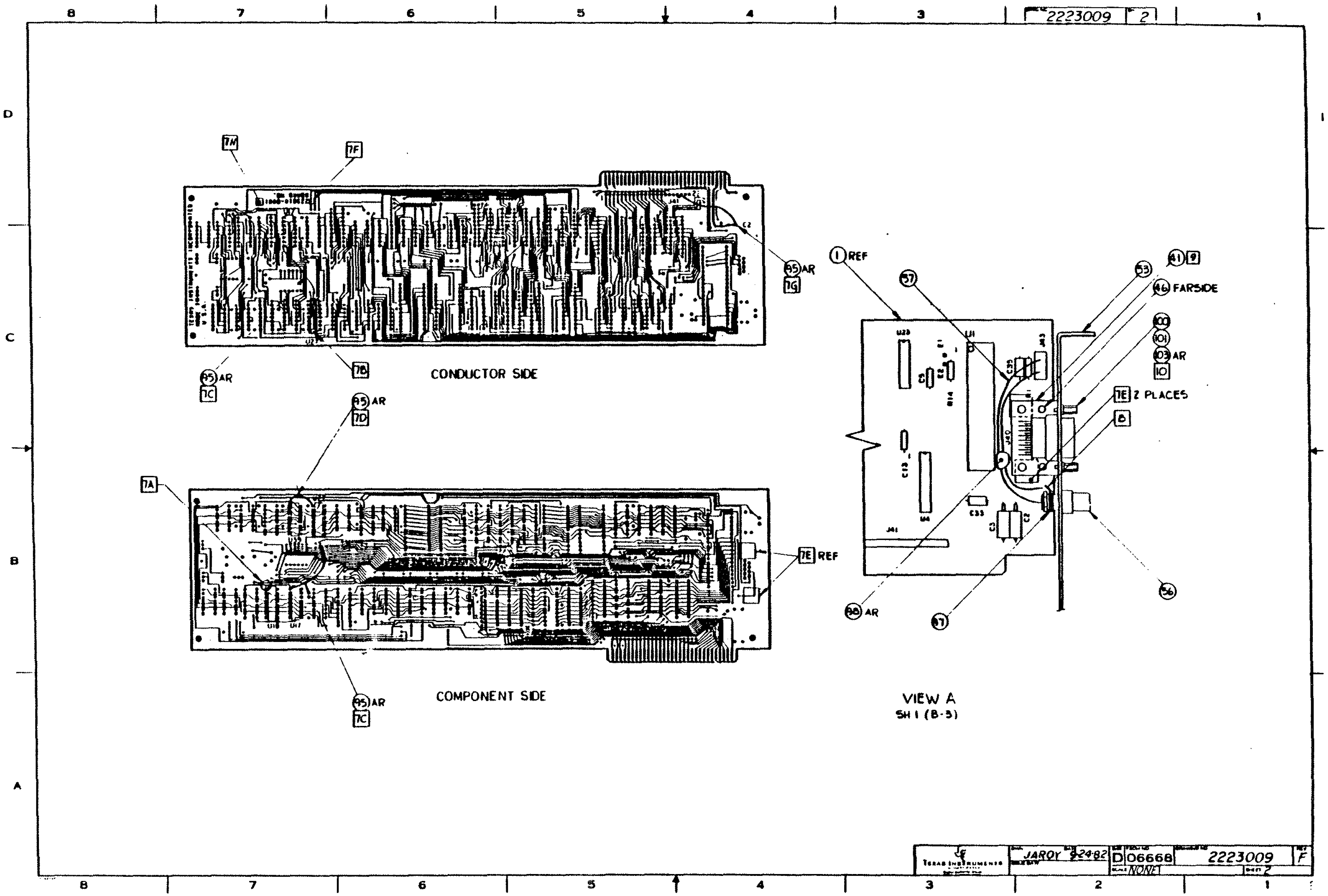
ALPHA CRT CONTROLLER

SIZE D FSCM NO 06668 DWG NO 2223009

SCALE NONE SHEET 1 OF 2

320

LM / CC


2223009
2
CONDUCTOR SIDE
COMPONENT SIDE
VIEW A
SH 1 (B-5)
REF
FARSIDE
2 PLACES
7E REF
AR
TEXAS INSTRUMENTS
JAROY
9-24-82
D 06668
2223009
NONE
F

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION.........................
2223009-0001 F ALPHA CRT CONTROLLER

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0002	REF	2223011-0001	LOGIC,DIAGRAM,ALPHA CRT CONTROLLER	EA
0025	00001.000	2210727-0001	IC,LS393,DUAL,4-BIT BINARY COUNTER V-LIST-LS393 BURN-IN	EA
0025A			U38 V-LIST-LS393 BURN-IN	
0027	00001.000	2210835-0004	CRYSTAL,18 MHZ,HC-18/U WITH GND LEAD SEE TI- DRAWING	EA
0027A			Y1 SEE TI- DRAWING	
0028	00001.000	2211878-0002	TRANS,MPS6602,NPN,COMPLEMENTRY DRIVER SEE TI- DRAWING	EA
0028A			Q1 SEE TI- DRAWING	
0038	00002.000	0418356-2305	CAPACITOR,TANTALUM,6.8UF,20 7%,35V SEE TI- DRAWING	EA
0038A			C2,C3 SEE TI- DRAWING	
0041	00001.000	2220488-0001	CONNECTOR,RECEPTACLE,PCB,9-PINS SEE TI- DRAWING	EA
0041A			J40 SEE TI- DRAWING	
0043	00001.000	2210970-0005	CONN. 22-POS.,PC BD, SINGLE ROW,.100 CNT SEE TI- DRAWING	EA
0043A			J41 SEE TI- DRAWING	
0044	REF	0994396-9901	PROCEDURE,SITE & DATE CODE SERIALIZATION	EA
0045	00001.000	2211047-0002	CONNECTOR,RECEPTACLE,2-ROW,11-POSITION SEE TI- DRAWING	EA
0045A			J42 SEE TI- DRAWING	
0046	00002.000	0972446-0012	RIVET,.116 DIA 3/16 LG DOME HD ALUM -75021-0406	EA
0053	00001.000	2273033-0003	PLATE,OPTION BOARD,9-POSITION 1678-3333-007	EA
0056	00001.000	2220629-0001	AUDIO JACK,PANEL MNTNG,ROUND BASE,.185" 1254- -000	EA
0057	AR	0935172-3488	WIRE,UL 1430/3317,22AWG,GRA/YEL 1650-0000-000	FT
0095	AR	0996563-0001	WIRE,30AWG SOLID,KYNAR,INSULATED,BROWN 071124-BR212/1-30-	FT
0096	AR	0411435-0408	TAPE,INSULATION,ELECT.1/4 IN MMM - 56-1/4	RL
0097	00001.000	0411100-0074	LOCKWASHER 1/4 INTERNAL TOOTH CRES QPL - MS35333-74	EA
0098	AR	0996069-0003	ADH,SOLID,THRMPLSTC 25# BAG ANAEROBIC PERSAL-917-6302	EA
0099	00001.000	2211540-0001	FOAM, .35X.50X.05,POLY, ADHESIVE BACKED SEE TI- DRAWING	EA
0100	00002.000	0532348-0401	STUD, EXTENSION-CRES	EA
0101	00002.000	0411100-0070	LOCKWASHER #4 INTERNAL TOOTH CRES QPL - MS35333-70	EA
0102	REF	2223271-0001	SPECIFICATION,UNIT TEST-ALPHA CRT	EA
0103	AR	0415804-0005	SEALING COMPOUND,ANAEROBIC-BLUE GRADE C	QT
0999	00001.000	2223009-5001	ALPHA CRT CONTROLLER - AUTO INSERT 1254-3010-005	EA
9999	00000.750	0239999-9999	COST, SHRINKAGE	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223009-5001	F	ALPHA CRT CONTROLLER - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2223010-0001	PWB,ALPHA CRT CONTROLLER	EA
			1669- -000	
0003	00001.000	2220443-0002	IC,CRT CONTROLLER,2 MHZ CLOCK RATE	EA
			SEE TI- DRAWING	
0003A			U1	
			SEE TI- DRAWING	
0004	00002.000	0996952-0005	IC,2K X 8-BIT STATIC RAM,150NS,PLASTIC	EA
			SEE TI- DRAWING	
0004A			U2,U3	
			SEE TI- DRAWING	
0005	00001.000	2223060-0001	LOGIC ARRAY,HAL10L8	EA
			1669- -000	
0005A			U4	
			1669- -000	
0006	00001.000	2223058-0001	LOGIC ARRAY,HAL16R8	EA
			1669- -000	
0006A			U5	
			1669- -000	
0007	00001.000	2210660-0001	IC,LS155,DUAL 2-LINE TO 4-LINE DECODER	EA
			V-LIST-LS155 BURN-IN	
0007A			U6	
			V-LIST-LS155 BURN-IN	
0008	00003.000	2210695-0001	IC,LS245,OCTAL BUS,XCIVER,3ST.OUTPUT	EA
			V-LIST-LS245 BURN-IN	
0008A			U7,U8,U9	
			V-LIST-LS245 BURN-IN	
0009	00004.000	2210721-0001	IC,LS374,OCTAL D-TYPE FLIP-FLOP	EA
			V-LIST-LS374 BURN-IN	
0009A			U10,U11,U14,U15	
			V-LIST-LS374 BURN-IN	
0010	00003.000	2210764-0001	IC,S175,QUAD,F/F,DOUBLE RAIL OUTPUT	EA
			V-LIST-S175 BURN-IN	
0010A			U16,U17,U27	
			V-LIST-S175 BURN-IN	
0011	00002.000	2210694-0001	IC,LS244,OCTAL BUF/LINE DRIVER/RECEIVER	EA
			V-LIST-LS244 BURN-IN	
0011A			U12,U13	
			V-LIST-LS244 BURN-IN	
0012	00001.000	2210669-0001	IC,LS166,8-BIT PARALLEL/SERIAL INPUT	EA
			V-LIST-LS166 BURN-IN	
0012A			U19	
			V-LIST-LS166 BURN-IN	
0013	00003.000	2210662-0001	IC,LS157,QUAD 2-LINE TO 1-LINE DATA SELE	EA
			V-LIST-LS157 BURN-IN	
0013A			U21,U22,U23	
			V-LIST-LS157 BURN-IN	
0014	00001.000	2210761-0001	IC,S163,SYNCHRONOUS 4-BIT COUNTER	EA
			V-LIST-S163 BURN-IN	
0014A			U24	
			V-LIST-S163 BURN-IN	
0015	00001.000	2223065-0001	ROM,CHARACTER GENERATOR	EA
			- - -000	
0015A			U25	
			- - -000	
0016	00002.000	2210631-0001	IC,LS74,DUAL D FLIP-FLOP W/PSET & CLR	EA
			V-LIST-LS74 BURN-IN	
0016A			U28,U29	
			V-LIST-LS74 BURN-IN	
0017	00001.000	2210649-0001	IC,LS125,QUAD BUS BUFFER W/3-STATE OUTPU	EA
			V-LIST-LS125 BURN-IN	
0017A			U30	
			V-LIST-LS125 BURN-IN	
0018	00001.000	2210614-0001	IC,LS20,DUAL,4-INPUT NAND	EA
			V-LIST-LS20 BURN-IN	

LIST OF MATERIALS

11/24/82

PART NUMBER 2223009-5001 REV F

DESCRIPTION ALPHA CRT CONTROLLER - AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0018A			U31 V-LIST-LS20 BURN-IN	
0019	00001.000	2210749-0001	IC,S86,QUAD,2-INPUT EXCLUSIVE OR V-LIST-S86 BURN-IN	EA
0019A			U32 V-LIST-S86 BURN-IN	
0020	00001.000	2210740-0001	IC,S10,TRIPLE,3-INPUT POSITIVE AND V-LIST-S10 BURN-IN	EA
0020A			U33 V-LIST-S10 BURN-IN	
0021	00001.000	2210621-0001	IC,LS32,QUAD,2-INPUT OR V-LIST-LS32 BURN-IN	EA
0021A			U34 V-LIST-LS32 BURN-IN	
0022	00001.000	2210735-0001	IC,S00,QUAD,2-INPUT NAND V-LIST-S00 BURN-IN	EA
0022A			U35 V-LIST-S00 BURN-IN	
0023	00001.000	2210738-0001	IC,S04,HEX INVERTERS V-LIST-S04 BURN-IN	EA
0023A			U36 V-LIST-S04 BURN-IN	
0024	00001.000	2210604-0001	IC,LS04,HEX INVERTERS V-LIST-LS04 BURN-IN	EA
0024A			U37 V-LIST-LS04 BURN-IN	
0029	00001.000	0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0029A			R1 ROH - R-25	
0030	00001.000	0972946-0074	RES FIX 2.4K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0030A			R2 ROH - R-25	
0031	00002.000	0972946-0066	RES FIX 1.1K OHM 5% .25 W CARBON FILM ROH - R-25	EA
0031A			R3,R10 ROH - R-25	
0032	00001.000	0972946-0091	RES FIX 12 K OHM 5% .25 W CARBON FILM ROH - R-25	EA
0032A			R4 ROH - R-25	
0033	00001.000	0972946-0076	RES FIX 3.0K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0033A			R5 ROH - R-25	
0034	00001.000	0972946-0084	RES FIX 6.2K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0034A			R6 ROH - R-25	
0035	00006.000	0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0035A			R7,R8,R9,R11,R14,R16 ROH - R-25	
0036	00002.000	0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0036A			R12,R13 ROH - R-25	
0037	00001.000	0972757-0009	CAP FIX CER 470PF 10% 50V	EA
0037A			C1	
0039	00014.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS 004222-MC105E1037	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION
2223009-5001	F	ALPHA CRT CONTROLLER - AUTO INSERT

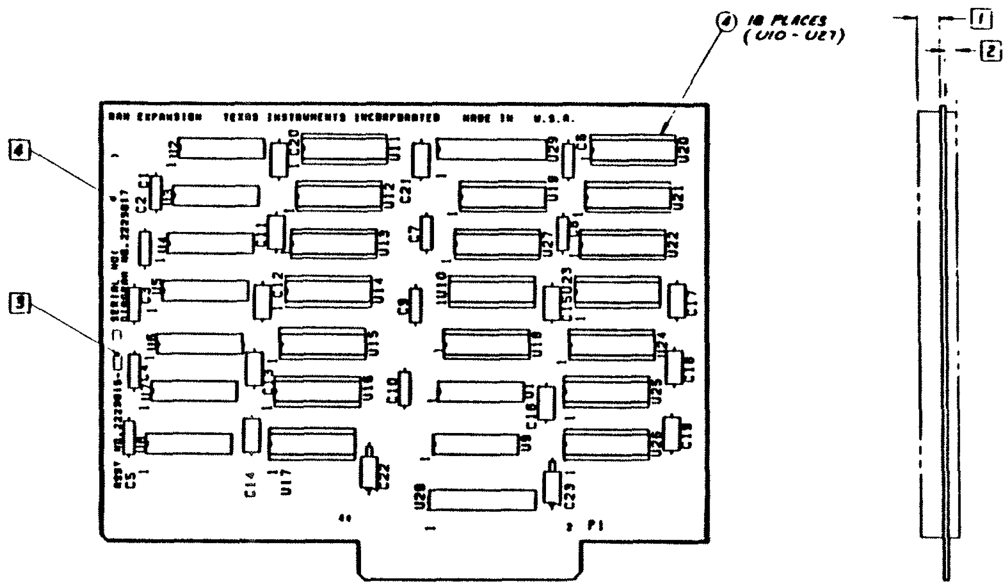
ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0039A			C4,C5,C7,C8,C9,C10,C11,C12 004222-MC105E103Z	
0039B			C13,C14,C15,C16,C17,C18 004222-MC105E103Z	
0040	00010.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL COR CA-C03Z5U104Z050A	EA
0040A			C27,C30,C31,C32,C33,C34 COR CA-C03Z5U104Z050A	
0040B			C35,C38,C39,C40 COR CA-C03Z5U104Z050A	
0047	00002.000	2210763-0001	IC,S174,HEX,FLIP-FLOP,SINGLE RAIL OUTPUT V-LIST-S174 BURN-IN	EA
0047A			U18,U39 V-LIST-S174 BURN-IN	
0049	00001.000	2210759-0001	IC,S157,QUAD,2/1 LINE SELECT/MULTIPLEXER V-LIST-S157 BURN-IN	EA
0049A			U20 V-LIST-S157 BURN-IN	
0050	00001.000	0972946-0079	RES FIX 3.9K OHM 5 % .25 W CARBON FILM ROH - R-25	EA
0050A			R15 ROH - R-25	

2223015

REV	DESCRIPTION	DATE	APPROVED
A	LM UPDATE	4-30-82	
B	LM UPDATE	4-30-82	
C	CN 493816 (D) (1) LM IT 4A DES WAS U10 THRU U27	5-21-82	M Bail
D	CN 497899 (D) (1) LM UPDATE	8-9-82	M Bail
E	CN 500532 (D) (1) LM UPDATE (2) ADD NOTE 6	9-11-82	M B

NOTES UNLESS OTHERWISE SPECIFIED

1. MAXIMUM COMPONENT HEIGHT ABOVE THE BOARD SHALL BE 19.00
2. MAXIMUM LEAD LENGTH BELOW THE BOARD SHALL BE 1.78
3. MARK APPROPRIATE DASH NUMBER AND REVISION LETTER IN SPACE INDICATED PER PROCESS 3
4. MARK SITE DATE CODE AND SERIAL NUMBER IN SPACE INDICATED PER ITEM 9 PARAGRAPH 4 AND PROCESS 3
5. CAUTION THIS ASSEMBLY AND CERTAIN COMPONENTS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE. OPERATOR AND EQUIPMENT GROUND AND PACKAGE IS REQUIRED. STATIC SENSITIVE COMPONENTS ARE : U1 THRU U29
6. ITEM 5 1221118-0004 INSTALLED IN XU10 THRU XU18 ON DASH 2 ONLY AND XU10 THRU XU27 ON DASH 3 ONLY. (SOCKETS NOT POPULATED ON DASH 1)



CONVERSION CHART	
mm	INCHES
0.25	.010
0.5	.02
1.5	.06
1.78	.070
19.00	.748

PART NO.	TITLE
2223015 - 5003	EXPANSION RAM (192K) AUTO INSERT
2223015 - 5002	EXPANSION RAM (128K) AUTO INSERT
2223015 - 5001	EXPANSION RAM AUTO INSERT
2223016 - 0003	EXPANSION RAM (192K)
2223015 - 0002	EXPANSION RAM (128K)
2223015 - 0001	EXPANSION RAM

SEQ NO	PROCESS IDENT	PROCESS F SPEC	CLASSIFICATION NO	CLASSIFICATION ADDITIONAL	NOTES
3	MARK	902 - 01	01	HGT 1.5 CLR WHT (CAT 4)	3 4
2	SLDR	127 - 01	00	HAND SOLDER	
1	SLDR	124 - 02	00	WAVE SOLDER	

PROCESSES — FOR CORRELATION TO GOVT AND SPECIFICATIONS SEE TI DRAWING 72440

		A	B	C	D	E
ASSEMBLY	2223015 - 0001	A	B	C	D	E
PWB	2223016 - 0001	*	*	*	*	A
DIAGRAM	2223017 - 0001	*	*	*	*	*

NEXT ASSY	USED ON
2223051	8755
2223050	8755

APPLICATION

PARTS LIST

TEXAS INSTRUMENTS INCORPORATED

SI-METRIC

RAM EXPANSION

D 06668 2223015

SCALE NONE

LM

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223015-0001 F EXPANSION RAM

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0002	REF	2223017-0001	SCHEMATIC,EXPANSION RAM	EA
0004	00018.000	2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	EA
			SEE T -I DRAWING	
0004A			XU10,XU11,XU12,XU13,XU14	
			SEE T -I DRAWING	
0004B			XU15,XU16,XU17,XU18,XU19	
			SEE T -I DRAWING	
0004C			XU20,XU21,XU22,XU23,XU24	
			SEE T -I DRAWING	
0004D			XU25,XU26,XU27	
			SEE T -I DRAWING	
0006	00001.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL	EA
			COR CA-C02Z5U102Z100A	
0006A			C5	
			COR CA-C02Z5U102Z100A	
0007	00001.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	
0007A			C19	
			COR CA-C03Z5U104Z050A	
0008	00002.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT	EA
			QPL -M39003/1-2304	
0008A			C22,C23	
			QPL -M39003/1-2304	
0009	REF	0994396-0001	PROC., SITE/DATE CODE AND SERIALIZATION	EA
0101	00001.000	2223015-5001	EXPANSION RAM -AUTO INSERT	EA
			1254-3016-006	
9999	00000.500	0239999-9999	COST, SHRINKAGE	EA

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223015-0002 F EXPANSION RAM (128K)

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0002	REF	2223017-0001	SCHEMATIC,EXPANSION RAM	EA
0003	00009.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW	EA
			TMS416-4-15NL	
0003A			U10,U11,U12,U13,U14,U15,U16	
			TMS416-4-15NL	
0003B			U17,U18	
			TMS416-4-15NL	
0004	00018.000	2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE	EA
			SEE T -I DRAWING	
0004A			XU10,XU11,XU12,XU13,XU14	
			SEE T -I DRAWING	
0004B			XU15,XU16,XU17,XU18,XU19	
			SEE T -I DRAWING	
0004C			XU20,XU21,XU22,XU23,XU24	
			SEE T -I DRAWING	
0004D			XU25,XU26,XU27	
			SEE T -I DRAWING	
0006	00001.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL	EA
			COR CA-C02Z5U102Z100A	
0006A			C5	
			COR CA-C02Z5U102Z100A	
0007	00001.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223015-0002 E EXPANSION RAM (128K)

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0007A			C19 COR CA-C03Z5U104Z050A	
0008	00002.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT QPL -M39003/1-2304	EA
0008A			C22,C23 QPL -M39003/1-2304	
0009	REF	0994396-0001	PROC., SITE/DATE CODE AND SERIALIZATION	EA
0101	00001.000	2223015-5002	EXPANSION RAM (128K)-AUTO INSERT 1254-3018-001	EA
9999	00000.500	0239999-9999	COST, SHRINKAGE	EA

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223015-0003 E EXPANSION RAM (192K)

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0002	REF	2223017-0001	SCHEMATIC,EXPANSION RAM	EA
0003	00018.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW TMS416-4-15NL	EA
0003A			U10,U11,U12,U13,U14,U15,U16 TMS416-4-15NL	
0003B			U17,U18,U19,U20,U21,U22,U23 TMS416-4-15NL	
0003C			U24,U25,U26,U27 TMS416-4-15NL	
0004	00018.000	2210188-0012	SOCKET,DIP,16-PINS,LOW PROFILE SEE T -I DRAWING	EA
0004A			XU10,XU11,XU12,XU13,XU14 SEE T -I DRAWING	
0004B			XU15,XU16,XU17,XU18,XU19 SEE T -I DRAWING	
0004C			XU20,XU21,XU22,XU23,XU24 SEE T -I DRAWING	
0004D			XU25,XU26,XU27 SEE T -I DRAWING	
0006	00001.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL COR CA-C02Z5U102Z100A	EA
0006A			C5 COR CA-C02Z5U102Z100A	
0007	00001.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL COR CA-C03Z5U104Z050A	EA
0007A			C19 COR CA-C03Z5U104Z050A	
0008	00002.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT QPL -M39003/1-2304	EA
0008A			C22,C23 QPL -M39003/1-2304	
0009	REF	0994396-0001	PROC., SITE/DATE CODE AND SERIALIZATION	EA
0101	00001.000	2223015-5003	EXPANSION RAM (192K)-AUTO INSERT 1254-3020-001	EA
9999	00000.500	0239999-9999	COST, SHRINKAGE	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223015-5001	E	EXPANSION RAM -AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2223016-0001	PWB,EXPANSION RAM 1669- -000	EA
0003	00009.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW TMS416-4-15NL	EA
0003A			U1,U2,U3,U4,U5,U6,U7,U8,U9 TMS416-4-15NL	
0005	00002.000	2220360-0002	IC,OCTAL DRAM DRIVER, 3-STATE OUTPUTS SEE TI- DRAWING	EA
0005A			U28,U29 SEE TI- DRAWING	
0006	00009.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL COR CA-C02Z5U102Z100A	EA
0006A			C1,C2,C3,C4,C6,C7,C8,C9,C10 COR CA-C02Z5U102Z100A	
0007	00011.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL COR CA-C03Z5U104Z050A	EA
0007A			C11,C12,C13,C14,C15,C16,C17 COR CA-C03Z5U104Z050A	
0007B			C18,C20,C21 COR CA-C03Z5U104Z050A	

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223015-5002	E	EXPANSION RAM (128K)-AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2223016-0001	PWB,EXPANSION RAM 1669- -000	EA
0003	00009.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW TMS416-4-15NL	EA
0003A			U1,U2,U3,U4,U5,U6,U7,U8,U9 TMS416-4-15NL	
0005	00002.000	2220360-0002	IC,OCTAL DRAM DRIVER, 3-STATE OUTPUTS SEE TI- DRAWING	EA
0005A			U28,U29 SEE TI- DRAWING	
0006	00009.000	0972763-0001	CAPACITOR,.001UF 50V FX CERAMIC DIEL COR CA-C02Z5U102Z100A	EA
0006A			C1,C2,C3,C4,C6,C7,C8,C9,C10 COR CA-C02Z5U102Z100A	
0007	00010.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL COR CA-C03Z5U104Z050A	EA
0007A			C11,C12,C13,C14,C15,C16,C17 COR CA-C03Z5U104Z050A	
0007B			C18,C20,C21 COR CA-C03Z5U104Z050A	

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2223015-5003	E	EXPANSION RAM (192K)-AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	2223016-0001	PWB,EXPANSION RAM 1669- -000	EA
0003	00009.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW TMS416-4-15NL	EA
0003A			U1,U2,U3,U4,U5,U6,U7,U8,U9 TMS416-4-15NL	
0005	00002.000	2220360-0002	IC,OCTAL DRAM DRIVER, 3-STATE OUTPUTS SEE TI- DRAWING	EA
0005A			U28,U29 SEE TI- DRAWING	
0006	00009.000	0972763-0001	CAPACITOR,.001UF 50V EX CERAMIC DIEL COR CA-C02Z5U102Z100A	EA
0006A			C1,C2,C3,C4,C6,C7,C8,C9,C10 COR CA-C02Z5U102Z100A	
0007	00010.000	0972763-0025	CAPACITOR,.10UF 50V EX,CERAMIC DIEL COR CA-C03Z5U104Z050A	EA
0007A			C11,C12,C13,C14,C15,C16,C17 COR CA-C03Z5U104Z050A	
0007B			C18,C20,C21 COR CA-C03Z5U104Z050A	

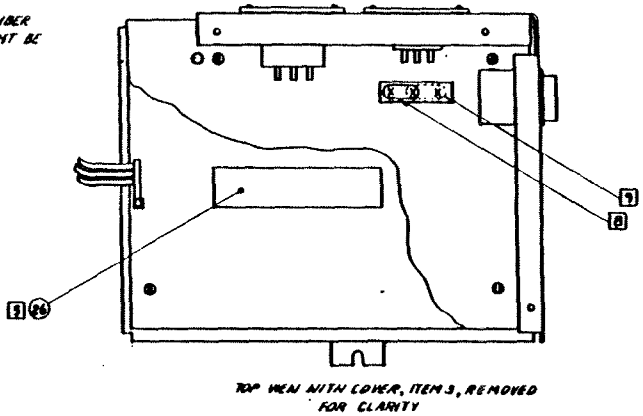
2223037 | 1

REVISIONS

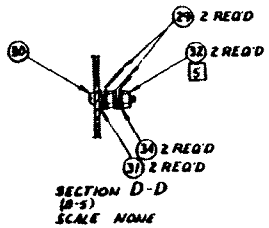
REV	DESCRIPTION	DATE	APPROVED
F	CN 501607 (D) [illegible]	10-[illegible]	[illegible]
	(1) CHNG PER ENG SPEC		
G	CN485049 (D) FRUNTON(!		
	ON ALL LM'S ITEM 12 PIN WAS 0912969-0005, ALSO ITEM 12 QTY WAS 1.000		

NOTES UNLESS OTHERWISE SPECIFIED

1. WIRES ARE TWISTED PAIR
2. HAND SOLDER PER PROCESS 1
3. LOCATE LABEL ITEM 26 APPROXIMATELY IN MIDDLE OF COVER ITEM 3
4. MARK APPROPRIATE T.I. PART NUMBER WHERE INDICATED. MARKING MUST BE PERMANENT AND LEGIBLE
5. TORQUE TO 1.7 ± 0.2 NM
6. TORQUE TO 0.7 ± 0.1 NM
7. TORQUE TO 0.9 ± 0.1 NM
8. VOLTAGE SELECTOR JUMPER: LEFT HAND POSITION IS 115V
9. VOLTAGE SELECTOR JUMPER: RIGHT HAND POSITION IS 220V

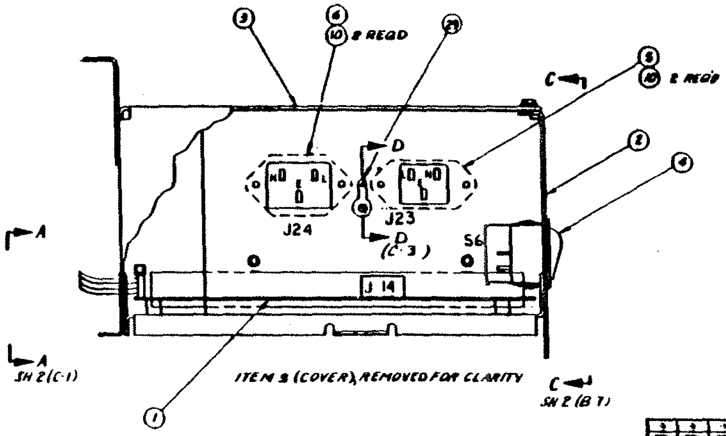


TOP VIEW WITH COVER, ITEM 3, REMOVED FOR CLARITY



SECTION D-D
(B-5)
SCALE NONE

CONVERSION CHART	
mm	INCHES
0.7 ± 0.1 NM	6 ± 1 INLB
0.9 ± 0.1 NM	8 ± 1.0 INLB
1.7 ± 0.2 NM	15 ± 2 INLB



PART NO	DESCRIPTION
~~2223037-0003~~	~~POWER SUPPLY ASSY, 100~~ (INACTIVE)
2223037-0002	POWER SUPPLY ASSY, INTERNATIONAL
2223037-0001	POWER SUPPLY ASSY, 115V

1	SLOR	127-01	00	HAND SOLDER
SEQ NO	IDENT	P-SPEC	NO	ADDITIONAL
	PROCESS			CLASSIFICATION

NOTES 2

REV STATUS OF SHEETS: REV G F; SH 1 2

PARTS LIST

TEXAS INSTRUMENTS

SI-METRIC

POWER SUPPLY ASSY

NEXT ASSY	USED ON
2223038	8755

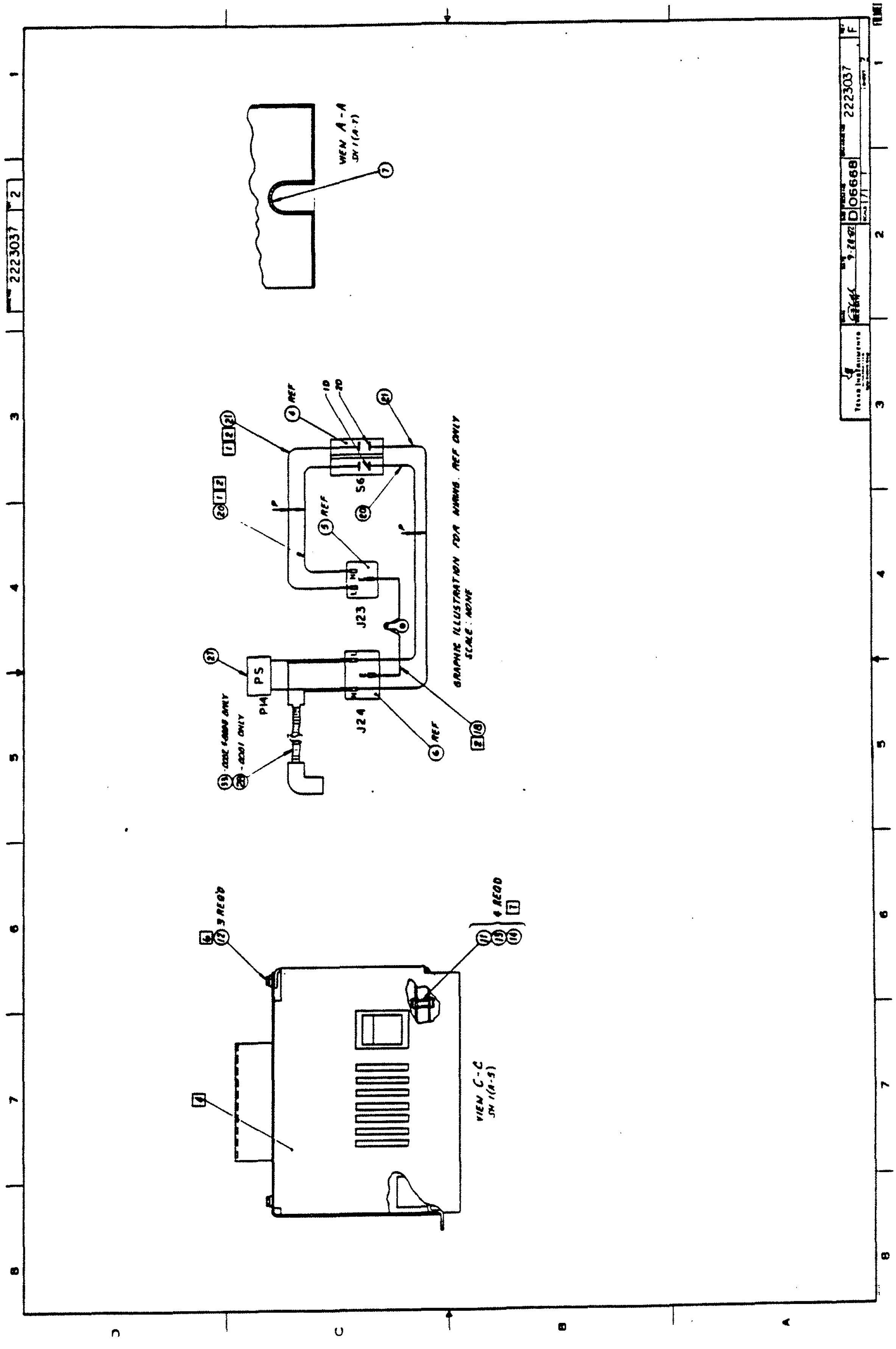
APPLICATION

D 06668 2223037

SCALE 1/1 SHEET 1 OF 2

300

LM



2223037
VIEW A-A
GRAPHIC ILLUSTRATION FOR WIRING. REF ONLY
SCALE: NONE
S6
J23
J24
PS
P14
VIEW C-C
D 06668

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..........................
2223037-0001	F	POWER SUPPY ASSY-115V DOMESTIC

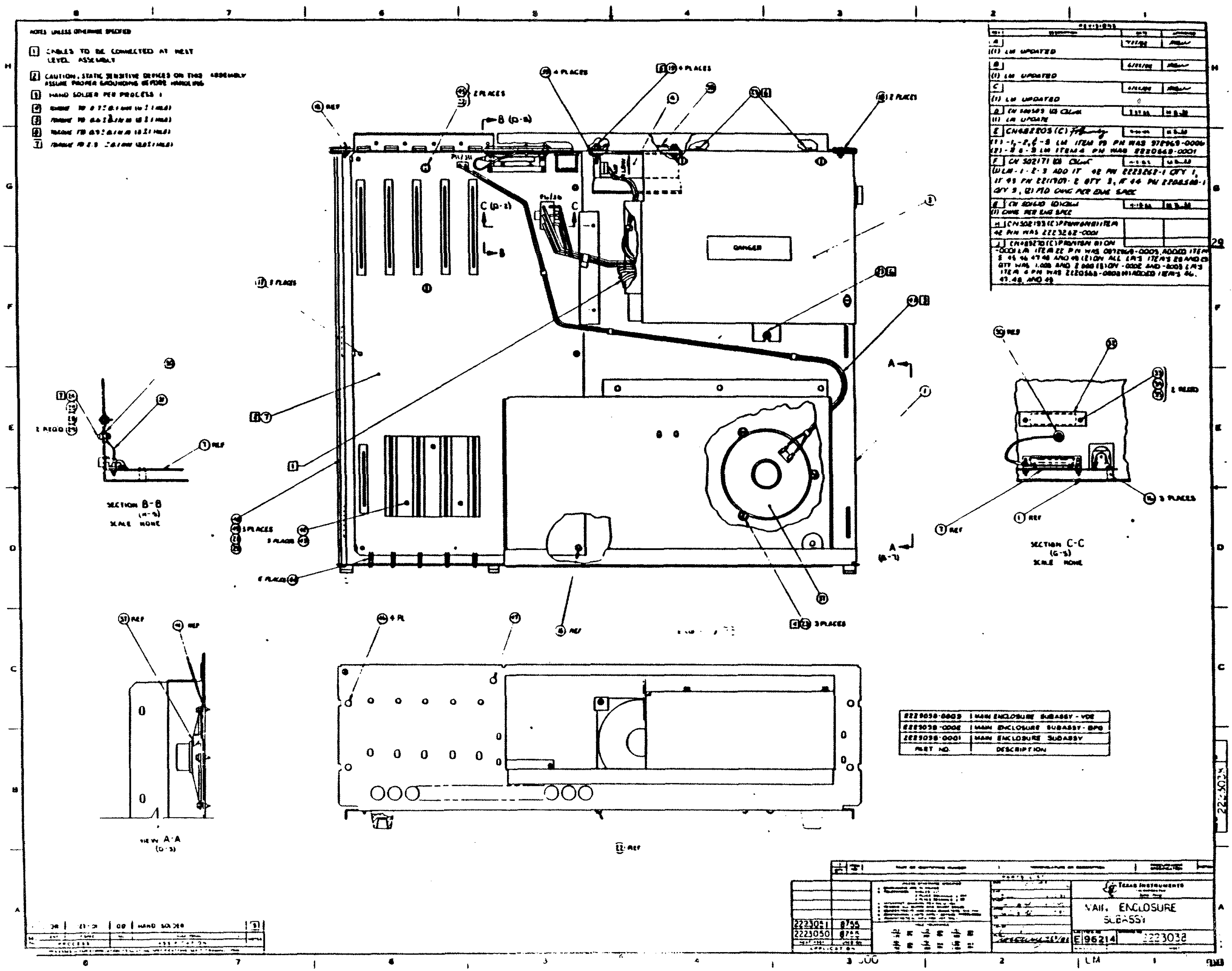
ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	2223091-0001	POWER SUPPLY, PEGASUS SEE TI- DRAWING	EA
0002	00001.000	2223025-0001	CHASSIS,POWER SUPPLY 1678-3025-006	EA
0003	00001.000	2223026-0001	COVER,POWER SUPPLY 1678-3026-006	EA
0004	00001.000	2211949-0001	SWITCH,ROCKER,DPST,10A,250V SEE TI- DRAWING	EA
0005	00001.000	0996260-0001	RECEPTACLE,3-PIN AC PWR SCT -EAC-301	EA
0006	00001.000	2220485-0001	RECEPTACLE,AC POWER,FEMALE,3 PIN - - -C00	EA
0007	00000.500	0418082-0001	GROMMET, PLASTIC, EDGING	EA
0010	00004.000	0972831-0004	RIVET,1/8X.275,TUBULAR,STEEL,BLIND 019738-1821-0410	EA
0011	00004.000	0972988-0041	SCREW 8-32 X .250 PAN HEAD CRES	EA
0012	00003.000	0972969-0005	SCREW #6-20 X 3/8 LG THD PL HEX WASHER	EA
0013	00004.000	0411101-0059	LOCKWASHER # 8 EXTERNAL TOOTH CRES QPL - MS35335-59	EA
0014	00004.000	0416622-0024	WASHER #8 FLAT QPL - AN960C8L	EA
0018	00000.500	0996286-4458	WIRE,19-STRAND #20 GRN/YELLOW UL-1430 SEE TI- DRAWING	FT
0020	00001.400	0935172-5488	WIRE,UL 1430/3317,18AWG,GRA/YEL 1650-0000-000	FT
0021	00001.400	0935172-5088	WIRE,UL 1430/3317,18AWG,GRA/BLK 1650-0000-000	FT
0025	00000.000	2223000-0001	POWER SUPPLY, 115V 1254-1000-000	EA
0025A			*MAY BE USED AS AN 1254-1000-000	
0025B			*ALTERNATE TO ITEM 1 1254-1000-000	
0026	00001.000	2207869-0001	LABEL,WARNING HIGH VOLTAGE 1234-1869-000	EA
0027	00001.000	2223088-0001	CABLE ASSY,POWER RCPT TO PWR SUPPLY BD ----------000	EA
0028	00001.000	2220641-0001	FAN CORD ASSEMBLY,5 INCH,PVC SEE TI- DRAWING	EA
0029	00001.000	2210066-0006	LUG,RING TONGUE,TAPE MTD,#6,RED,22-16 000779-2-31879-2	EA
0030	00001.000	0972988-0030	SCREW 6-32 X .500 PAN HEAD CRES	EA
0031	00002.000	0411027-0806	WASHER,#6 FLAT,CRES,.156 X .375 X .049 QPL - MS15795-806	EA
0032	00002.000	0411115-0064	NUT,PLAIN 6-32 UNC-2B HEX CRES QPL - MS35649-264	EA
0034	00002.000	0411101-0058	LOCKWASHER #6 EXTERNAL TOOTH CRES QPL - MS35335-58	EA

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223037-0002 F POWER SUPPLY ASSY,INTERNATIONAL

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION.............................	UM
0001	00001.000	2223091-0001	POWER SUPPLY, PEGASUS SEE TI- DRAWING	EA
0002	00001.000	2223025-0001	CHASSIS,POWER SUPPLY 1678-3025-006	EA
0003	00001.000	2223026-0001	COVER,POWER SUPPLY 1678-3026-006	EA
0004	00001.000	2220637-0001	ROCKER SWITCH FOR EUROPEAN ASSEMBLIES SEE TI- DRAWING	EA
0005	00001.000	0996260-0001	RECEPTACLE,3-PIN AC PWR SCT -EAC-301	EA
0006	00001.000	2220485-0001	RECEPTACLE,AC POWER,FEMALE,3 PIN - - -000	EA
0007	AR	0418082-0001	GROMMET, PLASTIC, EDGING	EA
0010	00004.000	0972831-0004	RIVET,1/8X.275,TUBULAR,STEEL,BLIND 019738-1821-0410	EA
0011	00004.000	0972988-0041	SCREW 8-32 X .250 PAN HEAD CRES	EA
0012	00003.000	0972969-0005	SCREW #6-20 X 3/8 LG THD PL HEX WASHER	EA
0013	00004.000	0411101-0059	LOCKWASHER # 8 EXTERNAL TOOTH CRES QPL - MS35335-59	EA
0014	00004.000	0416622-0024	WASHER #8 FLAT QPL - AN960C8L	EA
0018	00000.500	0996286-4455	WIRE,19-STRAND #20 GRN/YELLOW UL-1430 SEE TI- DRAWING	FT
0020	00001.400	0935172-5488	WIRE,UL 1430/3317,18AWG,GRA/YEL 1650-0000-000	FT
0021	00001.400	0935172-5088	WIRE,UL 1430/3317,18AWG,GRA/BLK 1650-0000-000	FT
0025	00000.000	2223000-0002	POWER SUPPLY-BPO 1254-2000-000	EA
0025A			*MAY BE USED AS AN 1254-2000-000	
0025B			*ALTERNATE TO ITEM 1 1254-2000-000	
0026	00001.000	2207869-0001	LABEL,WARNING HIGH VOLTAGE 1234-1869-000	EA
0027	00001.000	2223088-0001	CABLE ASSY,POWER RCPT TO PWR SUPPLY BD ----------000	EA
0029	00001.000	2210066-0006	LUG,RING TONGUE,TAPE MTD,#6,RED,22-16 000779-2-31879-2	EA
0030	00001.000	0972988-0030	SCREW 6-32 X .500 PAN HEAD CRES	EA
0031	00002.000	0411027-0806	WASHER,#6 FLAT,CRES,.156 X .375 X .049 QPL - MS15795-806	EA
0032	00002.000	0411115-0064	NUT,PLAIN 6-32 UNC-2B HEX CRES QPL - MS35649-264	EA
0033	00001.000	2223048-0001	CABLE ASSY,INT'L FAN CORD ----------000	EA
0034	00002.000	0411101-0058	LOCKWASHER #6 EXTERNAL TOOTH CRES QPL - MS35335-58	EA


NOTES UNLESS OTHERWISE SPECIFIED
CABLES TO BE CONNECTED AT NEXT LEVEL ASSEMBLY
CAUTION, STATIC SENSITIVE DEVICES ON THIS ASSEMBLY ASSURE PROPER GROUNDING BEFORE HANDLING
HAND SOLDER PER PROCESS 1
SECTION B-B
SCALE NONE
SECTION C-C
(G-5)
SCALE NONE
VIEW A-A
(D-3)
DANGER
2223038-0003 MAIN ENCLOSURE SUBASSY - VDE
2223038-0002 MAIN ENCLOSURE SUBASSY - BPS
2223038-0001 MAIN ENCLOSURE SUBASSY
PART NO.
DESCRIPTION
TEXAS INSTRUMENTS
MAIN ENCLOSURE SUBASSY
E96214
2223038
2223021
2223050

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..........................
2223038-0001	G	MAIN ENCLOSURE,SUBASSY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00001.000	2223024-0001	CHASSIS,TERMINAL 1678-3024-008	EA
0003	00001.000	2223037-0001	POWER SUPPY ASSY-115V DOMESTIC 1669-1037-000	EA
0004	00001.000	2220632-0001	FAN,115 VAC,29 CFM,13 W,TUBEAXIAL SEE TI- DRAWING	EA
0007	00001.000	2223003-0001	MOTHERBOARD - PEGASUS 1254-3003-005	EA
0016	00003.000	2211907-0005	SPACER,PCB,.31"BODY,NYLON,HOLE/#6 SCREW SEE TI- DRAWING	EA
0017	00003.000	2220484-0001	SUPPORT,PC BOARD,SELF-MOUNT - - -000	EA
0018	00002.000	2220487-0001	SPEEDNUT,J-TYPE,WITH T-NUT - - -000	EA
0019	00004.000	0972684-0012	SCREW 6-32 X 1/2 THD SLOT HEX WASHER HD	EA
0022	00002.000	0972969-0005	SCREW #6-20 X 3/8 LG THD PL HEX WASHER	EA
0023	00006.000	0972684-0018	SCREW 8-32 X 3/8 THD FRM,SLOT HX WSR HD	EA
0024	00001.000	0972988-0045	SCREW 8-32 X .500 PAN HEAD CRES	EA
0025	00001.000	0411115-0084	NUT,PLAIN 8-32 UNC-2B HEX CRES QPL - MS35649-284	EA
0028	00001.000	0411104-0137	WASHER, LOCK-SPRING, HELICAL, #8 QPL - MS35338-137	EA
0029	00002.000	0411027-0807	WASHER,#8 FLAT,CRES,.188 X .375 X .049 QPL - MS15795-807	EA
0030	00001.000	0411100-0072	LOCKWASHER #8,INTERNAL TOOTH CRES QPL - MS35333-72	EA
0031	00001.000	2223079-0001	CABLE ASSEMBLY,GROUNDING ----------000	EA
0032	00001.000	2223080-0001	PLATE,BLANK,EXTERNAL FLOPPY 1678-3080-005	EA
0033	00002.000	0972988-0013	SCREW 4-40 X .250 PAN HEAD CRES	EA
0034	00002.000	0411104-0135	WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135	EA
0035	00002.000	0411027-0803	WASHER .125 X .250 X .022 FLAT CRES QPL - MS15795-803	EA
0037	00001.000	2220556-0001	SPEAKERS,8 OHM 2 WATT SEE TI- DRAWING	EA
0038	00001.000	0972373-0001	GUARD FAN RTN --476143	EA
0039	00004.000	0972802-0014	FASTENER,SPEED NUT,STL,6-32,.41 L 078553-C10132-632	EA
0041	00001.000	2223108-0001	CABLE ASSY,SPEAKER ----------000	EA
0042	00001.000	2223262-0001	CARD GUIDE LOWER ----------000	EA
0043	00003.000	2211909-0002	PCB SPACER,NYLON,.37"BODY SEE TI- DRAWING	EA
0044	00005.000	2220850-0001	GUIDE,NYLON,2.50' LONG,GROOVE MOUNTING SEE TI- DRAWING	EA

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223038-0002 G MAIN ENCLOSURE SUBASSY-BPO

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00001.000	2223024-0001	CHASSIS,TERMINAL 1678-3024-008	EA
0003	00001.000	2223037-0002	POWER SUPPLY ASSY,INTERNATIONAL 1669-2037-000	EA
0004	00001.000	2220563-0003	FAN,230VAC,50/60 HZ,9W,32CFM,3.12X1.5" SEE TI- DRAWING	EA
0007	00001.000	2223003-0001	MOTHERBOARD - PEGASUS 1254-3003-005	EA
0016	00003.000	2211907-0005	SPACER,PCB,.31"BODY,NYLON,HOLE/#6 SCREW SEE TI- DRAWING	EA
0017	00003.000	2220484-0001	SUPPORT,PC BOARD,SELF-MOUNT - - -000	EA
0018	00002.000	2220487-0001	SPEEDNUT,J-TYPE,WITH T-NUT - - -000	EA
0019	00004.000	0972684-0012	SCREW 6-32 X 1/2 THD SLOT HEX WASHER HD	EA
0023	00006.000	0972684-0018	SCREW 8-32 X 3/8 THD FRM,SLOT HX WSR HD	EA
0024	00001.000	0972988-0045	SCREW 8-32 X .500 PAN HEAD CRES	EA
0025	00001.000	0411115-0084	NUT,PLAIN 8-32 UNC-2B HEX CRES QPL - MS35649-284	EA
0028	00001.000	0411104-0137	WASHER, LOCK-SPRING, HELICAL, #8 QPL - MS35338-137	EA
0029	00002.000	0411027-0807	WASHER,#8 FLAT,CRES,.188 X .375 X .049 QPL - MS15795-807	EA
0030	00001.000	0411100-0072	LOCKWASHER #8,INTERNAL TOOTH CRES QPL - MS35333-72	EA
0031	00001.000	2223079-0001	CABLE ASSEMBLY,GROUNDING ----------000	EA
0032	00001.000	2223080-0001	PLATE,BLANK,EXTERNAL FLOPPY 1678-3080-005	EA
0033	00002.000	0972988-0013	SCREW 4-40 X .250 PAN HEAD CRES	EA
0034	00002.000	0411104-0135	WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135	EA
0035	00002.000	0411027-0803	WASHER .125 X .250 X .022 FLAT CRES QPL - MS15795-803	EA
0037	00001.000	2220556-0001	SPEAKERS,8 OHM 2 WATT SEE TI- DRAWING	EA
0038	00001.000	0972373-0001	GUARD FAN PTN --476143	EA
0039	00004.000	0972802-0014	FASTENER,SPEED NUT,STL,6-32,.41 L 078553-C10132-632	EA
0041	00001.000	2223108-0001	CABLE ASSY,SPEAKER ----------000	EA
0042	00001.000	2223262-0001	CARD GUIDE LOWER ----------000	EA
0043	00003.000	2211909-0002	PCB SPACER,NYLON,.37"BODY SEE TI- DRAWING	EA
0044	00005.000	2220850-0001	GUIDE,NYLON,2.50' LONG,GROOVE MOUNTING SEE TI- DRAWING	EA

LIST OF MATERIALS

11/24/82

PART NUMBER 2223038-0003 — REV G — DESCRIPTION: MAIN ENCLOSURE SUB ASSY-VDE

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2223024-0001	CHASSIS,TERMINAL 1678-3024-008	EA
0003	00001.000	2223037-0002	POWER SUPPLY ASSY,INTERNATIONAL 1669-2037-000	EA
0004	00001.000	2220563-0003	FAN,230VAC,50/60 HZ,9W,32CFM,3.12X1.5" SEE TI- DRAWING	EA
0007	00001.000	2223003-0001	MOTHERBOARD - PEGASUS 1254-3003-005	EA
0016	00003.000	2211907-0005	SPACER,PCB,.31"BODY,NYLON,HOLE/#6 SCREW SEE TI- DRAWING	EA
0017	00003.000	2220484-0001	SUPPORT,PC BOARD,SELF-MOUNT - - -000	EA
0018	00002.000	2220487-0001	SPEEDNUT,J-TYPE,WITH T-NUT - - -000	EA
0019	00004.000	0972684-0012	SCREW 6-32 X 1/2 THD SLOT HEX WASHER HD	EA
0023	00006.000	0972684-0018	SCREW 8-32 X 3/8 THD FRM,SLOT HX WSR HD	EA
0024	00001.000	0972988-0045	SCREW 8-32 X .500 PAN HEAD CRES	EA
0025	00001.000	0411115-0084	NUT,PLAIN 8-32 UNC-2B HEX CRES QPL - MS35649-284	EA
0028	00001.000	0411104-0137	WASHER, LOCK-SPRING, HELICAL, #8 QPL - MS35338-137	EA
0029	00002.000	0411027-0807	WASHER,#8 FLAT,CRES,.188 X .375 X .049 QPL - MS15795-807	EA
0030	00001.000	0411100-0072	LOCKWASHER #8,INTERNAL TOOTH CRES QPL - MS35333-72	EA
0031	00001.000	2223079-0001	CABLE ASSEMBLY,GROUNDING ----------000	EA
0032	00001.000	2223080-0001	PLATE,BLANK,EXTERNAL FLOPPY 1678-3080-005	EA
0033	00002.000	0972988-0013	SCREW 4-40 X .250 PAN HEAD CRES	EA
0034	00002.000	0411104-0135	WASHER, LOCK-SPRING, HELICAL, #4 QPL - MS35338-135	EA
0035	00002.000	0411027-0803	WASHER .125 X .250 X .022 FLAT CRES QPL - MS15795-803	EA
0037	00001.000	2220556-0001	SPEAKERS,8 OHM 2 WATT SEE TI- DRAWING	EA
0038	00001.000	0972373-0001	GUARD FAN RTN --476143	EA
0039	00004.000	0972802-0014	FASTENER,SPEED NUT,STL,6-32,.41 L 078553-C10132-632	EA
0041	00001.000	2223108-0001	CABLE ASSY,SPEAKER ----------000	EA
0042	00001.000	2223262-0001	CARD GUIDE LOWER ----------000	EA
0043	00003.000	2211909-0002	PCB SPACER,NYLON,.37"BODY SEE TI- DRAWING	EA
0044	00005.000	2220850-0001	GUIDE,NYLON,2.50" LONG,GROOVE MOUNTING SEE TI- DRAWING	EA

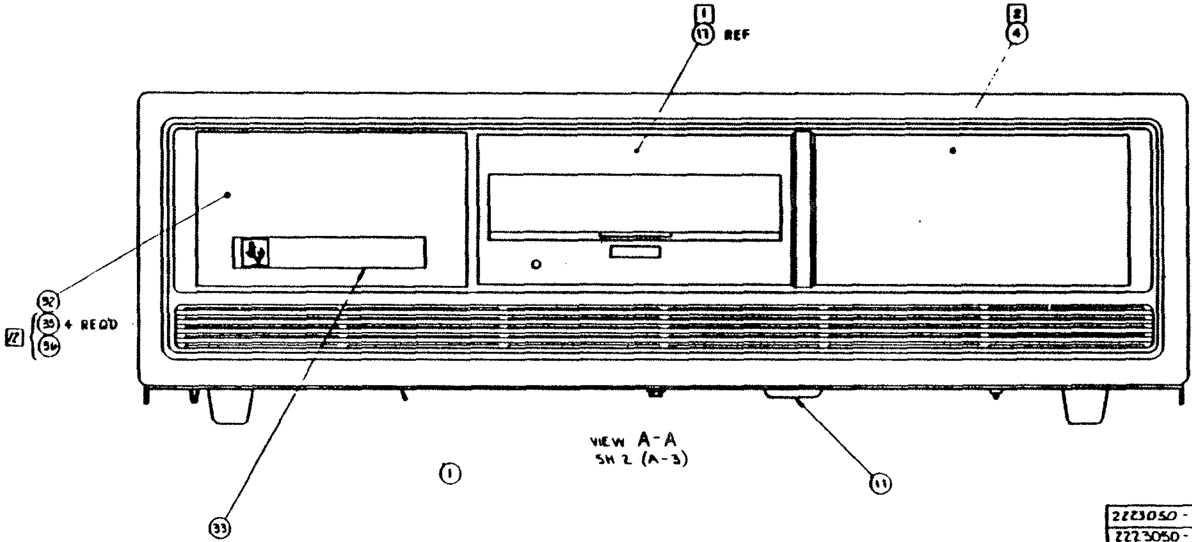
2223050 1

NOTES UNLESS OTHERWISE SPECIFIED

1. FACE PLATE OF ITEM 17 MUST BUTT AGAINST OPENING OF 'FRONT PANEL' BEFORE TIGHTENING ITEM 22
2. FACE OF 'INSERT PLATE' (ITEM 4) MUST BUTT AGAINST OPENING OF 'FRONT PANEL' BEFORE TIGHTENING ITEM 14
3. CAUTION STATIC SENSITIVE DEVICES ON THIS ASSEMBLY, PROPER GROUNDING REQUIRED
4. LOCATION OF LABELS (ITEMS 9, 51, 38 AND 39) IS NOT CRITICAL
5. POWER CORD, ITEM 6 OR 7 IS TO BE PACKED LOOSE WITH UNIT
6. ITEM 10 SELF DESTRUCT LABEL PLACED APPROXIMATELY IN THIS LOCATION
7. ~~ITEMS 42, 43, 44, 445 TO BE PACKED LOOSE WITH UNIT (DASH ONE ONLY)~~
8. ITEM 44/45 TO BE PACKED LOOSE WITH UNIT (DASH ONE AND DASH TWO)
9. SECURE ITEM 41, WITH CLIP PROVIDED, WHEN NOT IN USE
10. IF CONNECTORS P21 AND P22 ARE NOT USED SECURE WITH ITEM 29 AS SHOWN
11. SET MOTHERBOARD OPTION JUMPER PLUGS AS FOLLOWS: -0001, -0002 CONNECT 1 EACH TO E2, E4, E6 AND E20, -0003 CONNECT 1 EACH TO E4 AND E6, CONNECT E1 TO E2 AND E9 TO E20
12. TORQUE TO 0.5 ± 0.1 NM
13. TORQUE TO 0.7 ± 0.1 NM
14. TORQUE TO 1.1 ± 0.1 NM
15. TORQUE TO 0.9 ± 0.1 NM
16. REFER TO ITEM 50 FOR FLOPPY DRIVE CONFIGURATION INSTRUCTIONS WHICH MUST BE PERFORMED (-0001 AND -0003 ONLY)

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	(1) UPDATED LM	6/15/82	[illegible]
B	CN 501136 (D) [illegible] (1) LM-2 DELE IT 22 PN996759-14 QTY 3 (2) LM-18-2 ADD IT 29, ADD IT 46, DELE IT 40 PN2220250-1 QTY AR	[illegible]	M Bali
C	CN 502136 (C) Blue (1) LM UPDATE (2) CREATE -3 LM	[illegible]	M Bali
D	CN 502200 (B) LAMB (1) ADD NOTE 11 (2) SH 2 Z 28 ADD VIEW C	[illegible]	M Bali
E	CN 501609 (D) Blue (1) CHNG PER ENG SPEC	[illegible]	M Bali



PART NO.	DESCRIPTION
2223050-0003	SYSTEM ASSY, DOMESTIC - 320 K FLOPPY
2223050-0002	SYSTEM ASSY, DOMESTIC - BASIC
2223050-0001	SYSTEM ASSY, DOMESTIC - STANDARD

PARTS LIST

TEXAS INSTRUMENTS

SI-METRIC

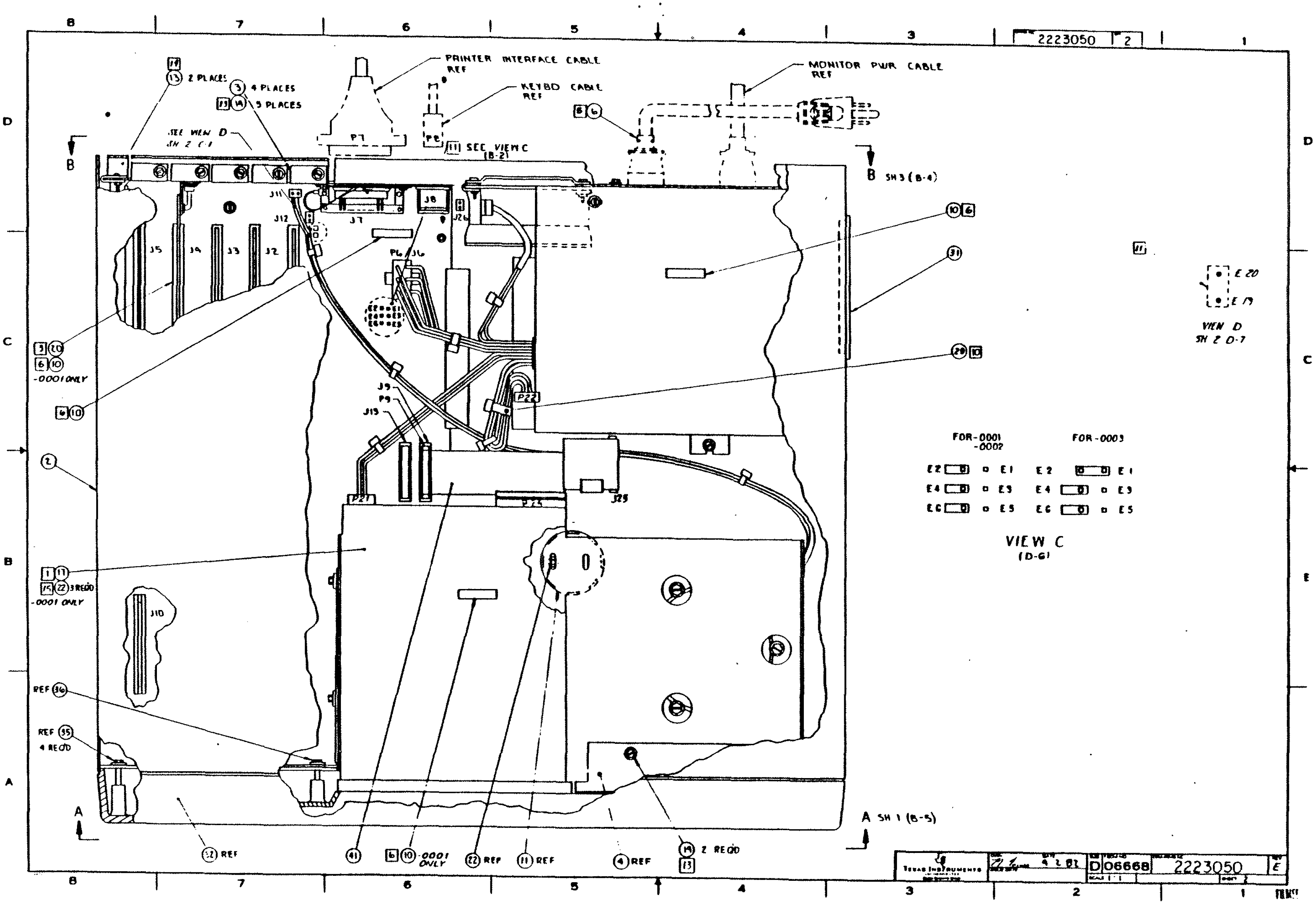
SYSTEM ASSY, DOMESTIC

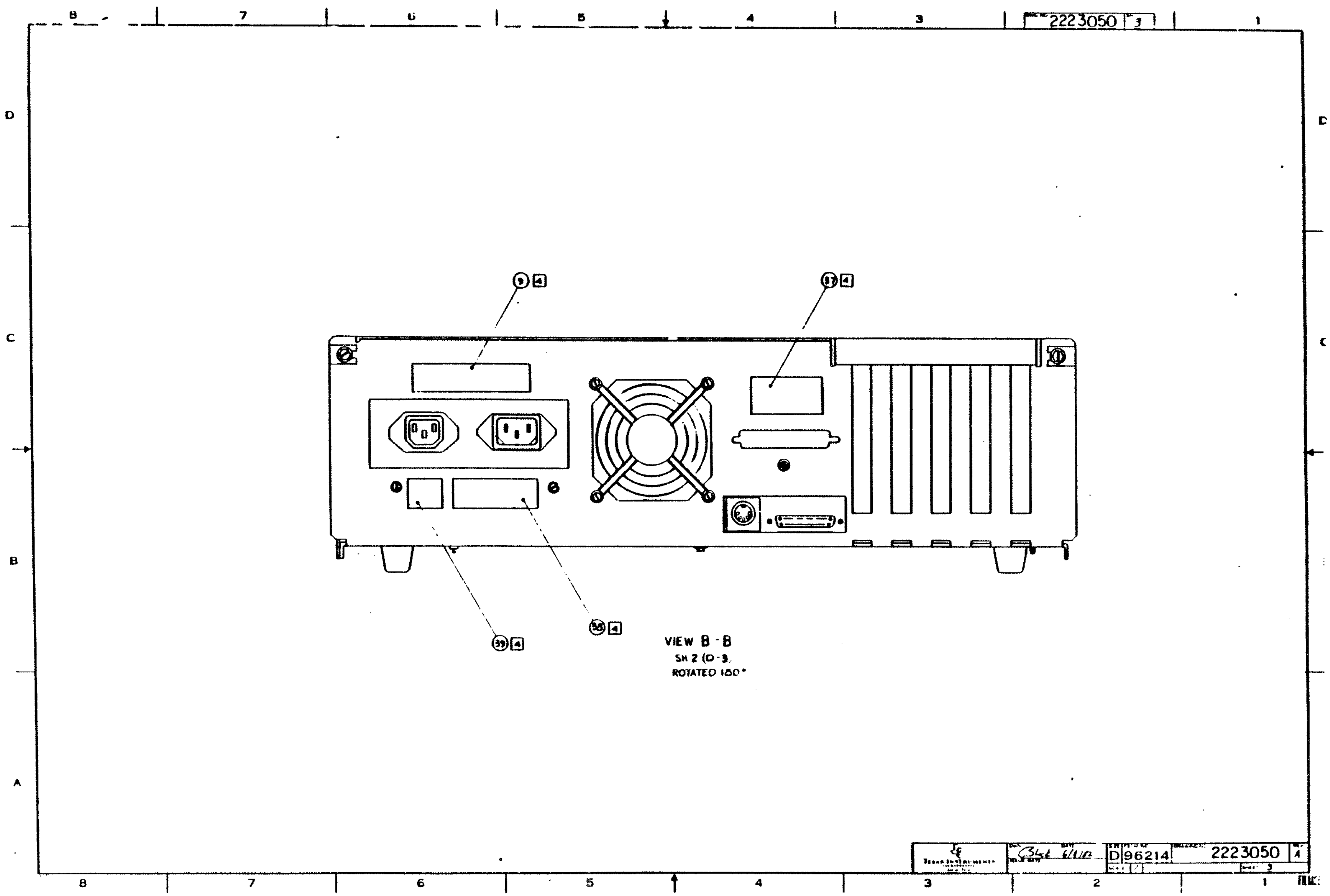
D 06668 2223050

NEXT ASSY 2223040 USED ON 8755

APPLICATION

300 CC LM


2223050
2
PRINTER INTERFACE CABLE REF
KEYBD CABLE REF
MONITOR PWR CABLE REF
2 PLACES
4 PLACES
5 PLACES
SEE VIEW D SH 2 C-1
SEE VIEW C (B-2)
B SH 3 (B-4)
P7
P8
J11
J12
J7
J8
J26
J5
J4
J3
J2
P6
J6
J9
P9
J15
P22
P21
P23
J25
J10
-0001 ONLY
3 REQD
REF
4 REQD
A SH 1 (B-5)
2 REQD
E 20
E 19
VIEW D SH 2 D-7
FOR-0001 -0002
FOR-0003
E2
E1
E4
E3
E6
E5
VIEW C (D-6)
TEXAS INSTRUMENTS
D 06668
2223050
E



2223050
VIEW B - B
SH 2 (D-3)
ROTATED 180°
D 96214
2223050
A

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2223050-0001	F	SYSTEM ASSY-STANDARD

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..................................	UM
0001	00001.000	2223038-0001	MAIN ENCLOSURE,SUBASSY 1669-1038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00004.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00001.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996289-0001	CORD SET,3-PIN PWR-DOMESTIC BLACK 080126-0-7889-008-GY	EA
0007	00000.000	0996289-0002	CORD SET,3-PIN PWR-DOMESTIC GRAY W/CLIP 080126-0-7919-008-GY	EA
0007A			*MAY BE USED AS AN 080126-0-7919-008-GY	
0007B			*ALTERNATE TO ITEM 6. 080126-0-7919-008-GY	
0009	00001.000	2223075-0001	LABEL,SERIAL-950 TERM,STANDARD DOM 1669-1075-000	EA
0010	AR	0976943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00007.000	0972684-0011	SCREW, THREAD FORMING, #6-32 1282-5256-000	EA
0017	00001.000	2220446-0001	DISK DRIVE ASSY,FLOPPY,5.25 INCH 1254- -000	EA
0020	00001.000	2223009-0001	ALPHA CRT CONTROLLER 1254-3009-005	EA
0022	00003.000	2210071-0009	SCREW, 6-32 X 3/8, HEX HEAD SEE TI- DRAWING	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4'D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0037	00001.000	2211184-0001	LABEL,.334H, FCC CLASS A EQUIPMENT SEE TI- DRAWING	EA
0038	00001.000	2269942-0001	LABEL,UL	EA
0039	00001.000	2269943-0001	LABEL,CSA	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA
0050	REF	2223279-0001	CONFIGURATION,FLOPPY DISK DRIVES	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..........................
2223050-0002	E	SYSTEM ASSY-BASIC

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0001	00001.000	2223038-0001	MAIN ENCLOSURE,SUBASSY 1669-1038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00005.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00002.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996289-0001	CORD SET,3-PIN PWR-DOMESTIC BLACK 080126-0-7889-008-GY	EA
0007	00000.000	0996289-0002	CORD SET,3-PIN PWR-DOMESTIC GRAY W/CLIP 080126-0-7919-008-GY	EA
0007A			*MAY BE USED AS AN 080126-0-7919-008-GY	
0007B			*ALTERNATE TO ITEM 6. 080126-0-7919-008-GY	
0009	00001.000	2223075-0002	LABEL,SERIAL-950 TERMINAL,BASIC DOMESTIC 1669-2075-000	EA
0010	AR	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00007.000	0972684-0011	SCREW, THREAD FORMING, #6-32 1282-5256-000	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4 D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0037	00001.000	2211184-0001	LABEL,.334H, FCC CLASS A EQUIPMENT SEE TI- DRAWING	EA
0038	00001.000	2269942-0001	LABEL,UL	EA
0039	00001.000	2269943-0001	LABEL,CSA	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223050-0003 F SYSTEMS ASSY STANDARD-320K

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00001.000	2223038-0001	MAIN ENCLOSURE,SUBASSY 1669-1038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00004.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00001.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996289-0001	CORD SET,3-PIN PWR-DOMESTIC BLACK 080126-0-7889-009-GY	EA
0007	00000.000	0996289-0002	CORD SET,3-PIN PWR-DOMESTIC GRAY W/CLIP 080126-0-7919-008-GY	EA
0007A			*MAY BE USED AS AN 080126-0-7919-008-GY	
0007B			*ALTERNATE TO ITEM 6. 080126-0-7919-008-GY	
0009	00001.000	2223075-0001	LABEL,SERIAL-950 TERM,STANDARD DDM 1669-1075-000	EA
0010	AR	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00007.000	0972684-0011	SCREW, THREAD FORMING, #6-32 1282-5256-000	EA
0017	00001.000	2220446-0002	DISK DRIVE ASSY,FLOPPY,5.25INCH-DUAL HD SEE TI- DRAWING	EA
0020	00001.000	2223009-0001	ALPHA CRT CONTROLLER 1254-3009-005	EA
0022	00003.000	2210071-0009	SCREW, 6-32 X 3/8, HEX HEAD SEE TI- DRAWING	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4 D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0037	00001.000	2211184-0001	LABEL,.334H, FCC CLASS A EQUIPMENT SEE TI- DRAWING	EA
0038	00001.000	2269942-0001	LABEL,UL	EA
0039	00001.000	2269943-0001	LABEL,CSA	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA
0050	REF	2223279-0001	CONFIGURATION,FLOPPY DISK DRIVES	EA

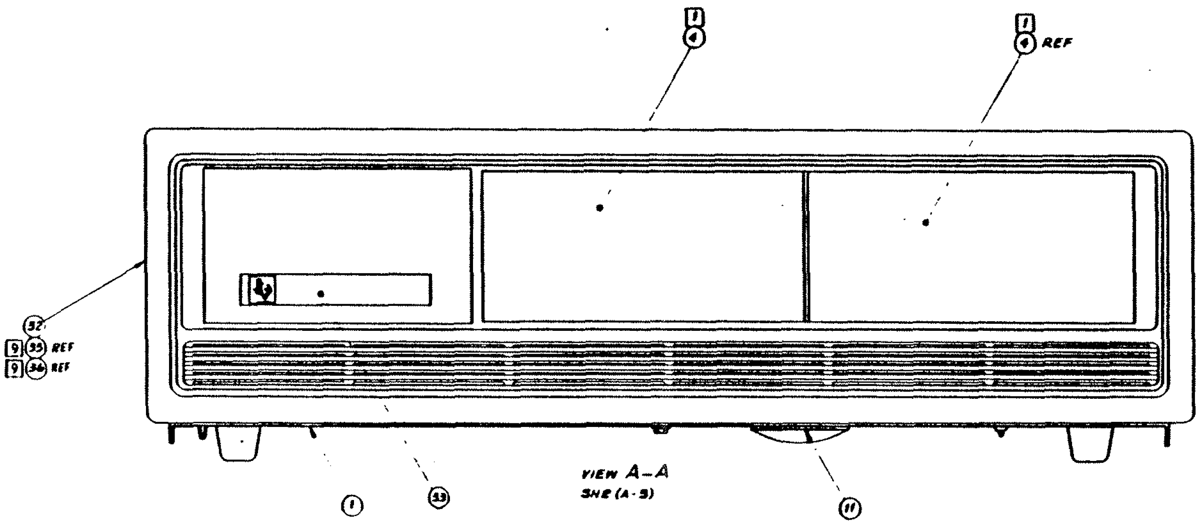
2223051 | 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	(1) UPDATED LM		
B	CN 501137 (D) (1) ALL LM ADD IT 29 & IT 46		
C	CN 497471 (D) LAMB (1) DELE IT 5 QTY 1 (2) ADD IT 48 (3) NOTE 6 WAS ... (ITEMS 5 & 46) ...		
D	CN 501608 (D) (1) CHANGE PER ENG REDESIGN		

NOTES UNLESS OTHERWISE SPECIFIED

1. FACE OF INSERT PLATE (ITEM 4) MUST BE BUTT AGAINST OPENING OF FRONT PANEL BEFORE TIGHTENING (ITEM 14)
2. IF CONNECTORS P21 AND P22 ARE NOT USED, SECURE WITH ITEM 29 AS SHOWN
3. LOCATION OF LABELS (ITEM 9 AND 46) IS IS NOT CRITICAL
4. POWER CORD (ITEM 6) IS TO BE PACKED LOOSE WITH UNIT
5. SELF DESTRUCT LABEL (ITEM 10) TO BE PLACED APPROXIMATELY THIS LOCATION
6. MANUAL (ITEMS 46 & 48) TO BE PACKED LOOSE WITH UNIT
7. CAUTION STATIC SENSITIVE DEVICE ON THIS ASSEMBLY, PROPER GROUNDING REQUIRED
8. SECURE ITEM 41 WITH CLIP PROVIDED, WHEN NOT IN USE
9. TORQUE TO 0.5 ± 0.1 NM
10. TORQUE TO 0.7 ± 0.1 NM
11. TORQUE TO 1.1 ± 0.1 NM
12. SET MOTHERBOARD OPTION JUMPER PLUGS AS FOLLOWS: CONNECT 1 EACH TO E2, E4 CONNECT E5 TO E6, AND E19 TO E20



PART NO.	DESCRIPTION
2223051-0003	SYSTEM ASSY, INTERNATIONAL - 115V
2223051-0002	SYSTEM ASSY, INTERNATIONAL - VDE
2223051-0001	SYSTEM ASSY, INTERNATIONAL - BPO

PARTS LIST

TEXAS INSTRUMENTS

SI-METRIC

SYSTEM ASSY, INTERNATIONAL

D 06668 2223051

SHEET 1 OF 5

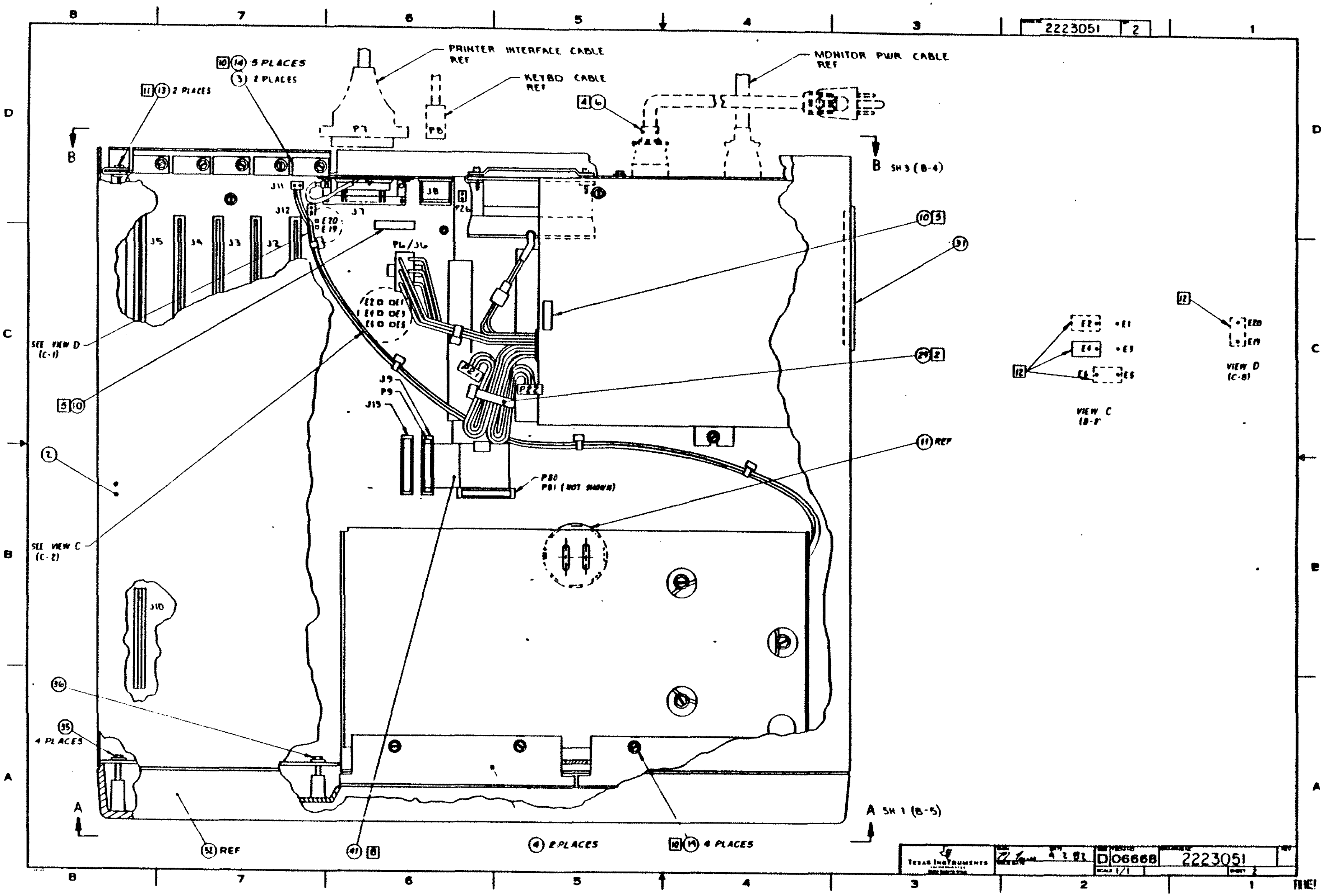
NEXT ASSY: 2223040 USED ON: 8755

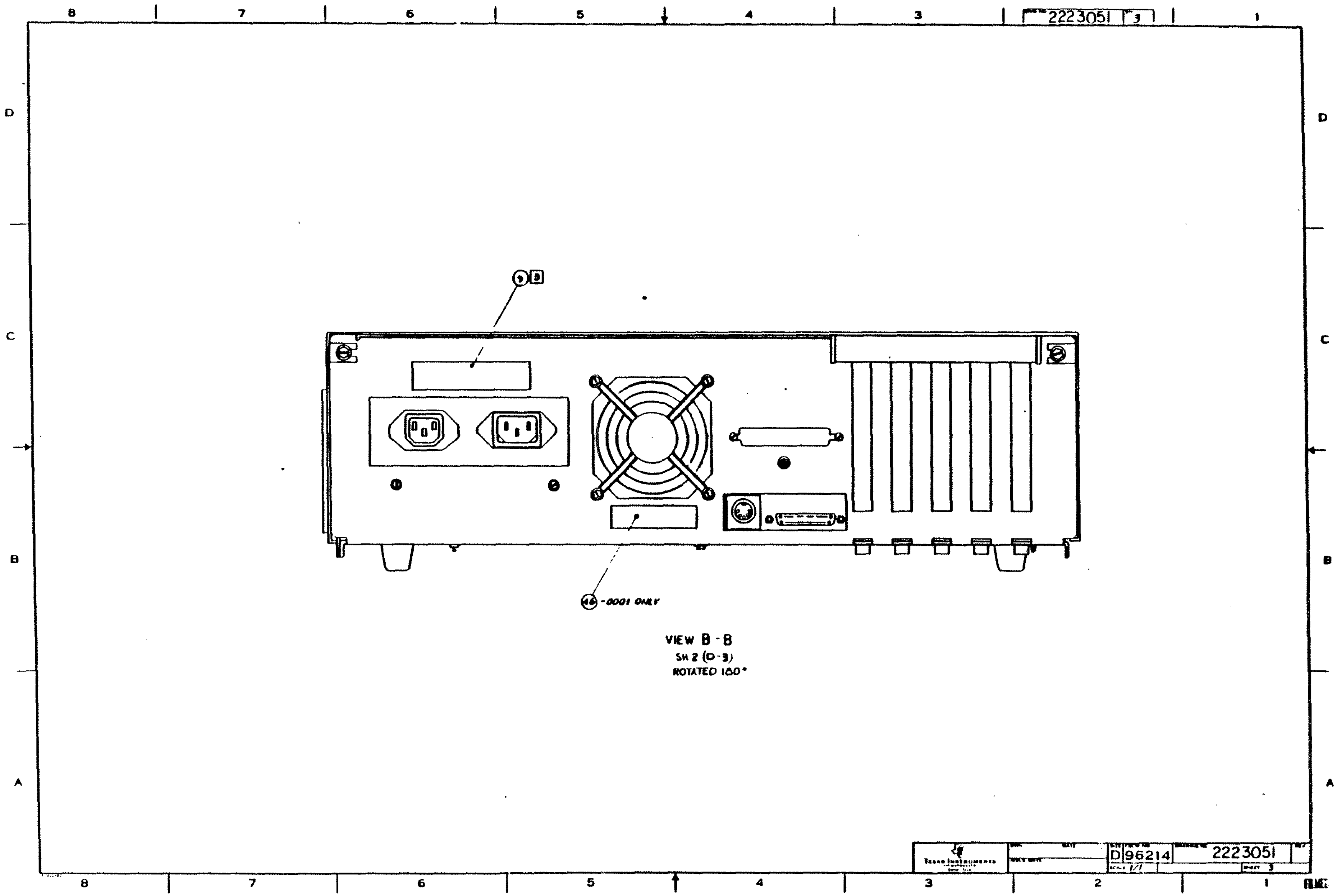
APPLICATION

PROCESS | CLASSIFICATION

REV STATUS OF SHEETS: D D D / 1 2 3

300 CC LM


2223051
PRINTER INTERFACE CABLE REF
KEYBD CABLE REF
MONITOR PWR CABLE REF
5 PLACES
2 PLACES
P7
P8
J11
J12
J7
J8
J5
J4
J3
J2
P6/J6
P26
E20
E19
J9
P9
J13
P80
P81 (NOT SHOWN)
P21
P22
J10
SEE VIEW D (C-1)
SEE VIEW C (C-2)
4 PLACES
REF
2 PLACES
4 PLACES
B SH 3 (B-4)
A SH 1 (B-5)
VIEW C (B-8)
VIEW D (C-8)
TEXAS INSTRUMENTS
D 06668
2223051


2223051
3
9
3
46 -0001 ONLY
VIEW B - B
SH 2 (D-3)
ROTATED 180°
TEXAS INSTRUMENTS
D
96214
1/1
2223051
3

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION..............................
2223051-0001 D SYSTEM ASSY-INT'L BPO

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2223038-0002	MAIN ENCLOSURE SUBASSY-BPO 1669-2038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00005.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00002.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996695-0001	CABLE,POWER W/O PLUG (INTL.) 080126-107-2-093	EA
0009	00001.000	2223075-0003	LABEL,SERIAL-950 TERM,BASIC BPO 1669-3075-000	EA
0010	AR	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00009.000	0996741-0006	6-20 X 3/8 SEMS SCREW TYPE B SEE TI- DRAWING	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4 D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0047	00001.000	2222574-0001	LABEL,CAUTION (BPO)	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION...........................
2223051-0002	D	SYSTEM,ASSY-INT'L VDE

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	2223038-0003	MAIN ENCLOSURE SUB ASSY-VDE 1669-3038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00005.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00002.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996290-0001	CORDSET,POWR-WEST EURO-RT ANGLE PLUG	EA
0009	00001.000	2223075-0004	LABEL,SERIAL-950 TERM,BASIC VDE 1669-4075-000	EA
0010	AR	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00009.000	0996741-0006	6-20 X 3/8 SEMS SCREW TYPE B SEE TI- DRAWING	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4 D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION...........................
2223051-0003	D	SYSTEM ASSY-INT'L 115V

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	2223038-0001	MAIN ENCLOSURE,SUBASSY 1669-1038-000	EA
0002	00001.000	2223029-0001	COVER,TERMINAL 1678-3029-006	EA
0003	00005.000	2223033-0001	PLATE OPTION BOARD 1678-3133-009	EA
0004	00002.000	2223034-0001	INSERT PLATE,FLOPPY 1678-3134-008	EA
0006	00001.000	0996289-0001	CORD SET,3-PIN PWR-DOMESTIC BLACK 080126-0-7889-008-GY	EA
0007	00000.000	0996289-0002	CORD SET,3-PIN PWR-DOMESTIC GRAY W/CLIP 080126-0-7919-008-GY	EA
0007A			*MAY BE USED AS AN 080126-0-7919-008-GY	
0007B			*ALTERNATE TO ITEM 6. 080126-0-7919-008-GY	
0009	00001.000	2223075-0005	LABEL,SERIAL-950 TERMINAL,BASIC 1669-5075-000	EA
0010	AR	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0011	00001.000	2211919-0002	PLUG,HOLE-1.563 DIA SEE TI- DRAWING	EA
0013	00002.000	0972988-0043	SCREW 8-32 X .375 PAN HEAD CRES	EA
0014	00009.000	0996741-0006	6-20 X 3/8 SEMS SCREW TYPE B SEE TI- DRAWING	EA
0025	REF	2223082-0001	INTERCONNECT DIAGRAM	EA
0029	00001.000	0972632-0001	STRAP,TIE DOWN,CABLE-NON-STD,0-1-1/4 D.	EA
0031	00001.000	2223076-0001	INSERT SWITCH OPENING 1255-3519-002	EA
0032	00001.000	2223020-0001	PANEL,FRONT 1255-3521-002	EA
0033	00001.000	2223090-0001	NAMEPLATE,PROFESSIONAL COMPUTER ----------000	EA
0035	00004.000	0972969-0009	SCREW,6-20 X 7/8 HEX WASHER HEAD SEE TI- DRAWING	EA
0036	00001.000	0972969-0008	SCREW,6-20 X 3/4 HEX WASHER HEAD	EA
0041	00001.000	2223097-0001	CABLE ASSY,MOTHERBOARD TO FLOPPY ----------000	EA
0046	00001.000	0999456-9701	MANUAL,INFORMATION REQUEST FORM 1225-9456-000	EA
0048	00001.000	2223203-0001	MANUAL-GETTING STARTED 1261-3203-000	EA

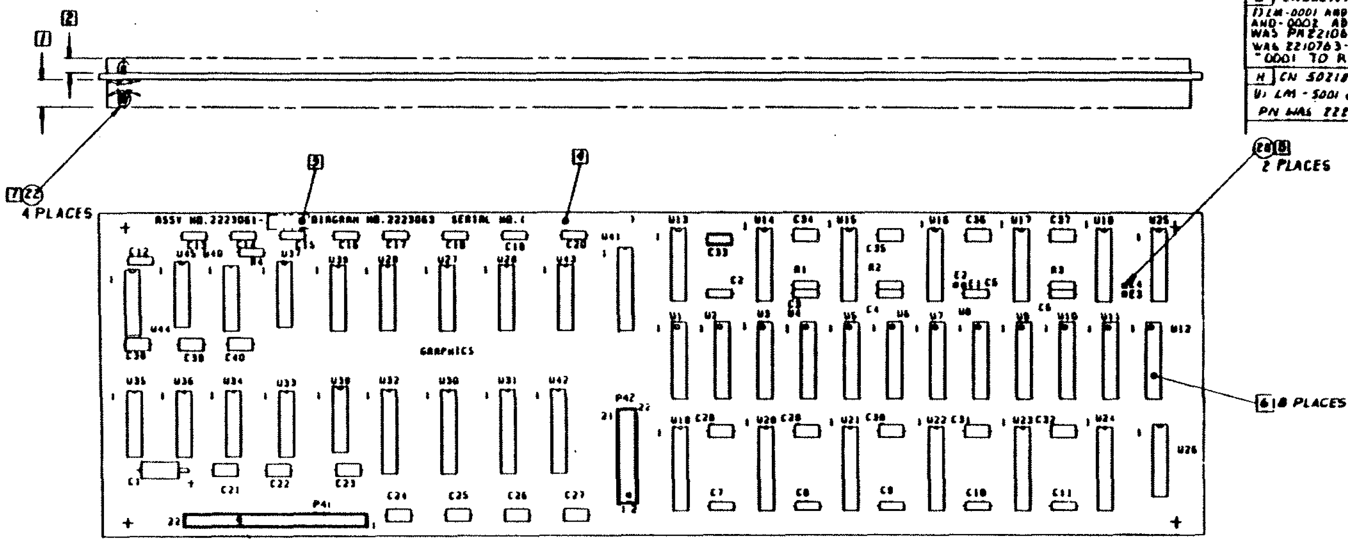
2223061

NOTES UNLESS OTHERWISE SPECIFIED

1. MAXIMUM COMPONENT HEIGHT ABOVE THE BOARD SHALL BE 5.6
2. MAXIMUM LEAD LENGTH BELOW BOARD SHALL BE 2.3
3. MARK APPROPRIATE DASH NUMBER AND REVISION LETTER IN SPACE INDICATED PER PROCESS 3
4. MARK SITE DATE CODE AND SERIAL NUMBER IN SPACE INDICATED PER ITEM 24 PARAGRAPH 4.0 AND PROCESS 3
5. CAUTION THIS ASSEMBLY AND CERTAIN COMPONENTS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE. OPERATOR AND EQUIPMENT GROUND AND PACKAGE IS REQUIRED. STATIC SENSITIVE COMPONENTS ARE: U1 THRU U45
6. COMPONENTS U5, U6, U7, U8, U9, U10, U11, U12 ARE USED ON -0002 ONLY
7. INSTALL ITEM 22 AFTER UNIT TEST
8. INSTALL ITEM 28 BETWEEN E2-E1 AND E4-E3 ON -0001 ASSEMBLY ONLY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	LM UPDATE	4-7-82	[illegible]
B	LM UPDATE	4-7-82	[illegible]
C	CN 502108 (D) Cluck (1) LM UPDATE	8-8-82	M B[illegible]
D	CN 500553 (D) RT[illegible] (1) LM-1A-2 DELE IT1 P/N 2223061 QTY 1 (2) LM-5001 & -5002 IT 18 WAS 418356	8-10-82	M B[illegible]
E	CN 497440 (C) [illegible] (1) LM-5001 & -5002 IT 3 WAS 2220517-2 (2) LM-5001 & -5002 ADD IT 26	8-31-82	M B[illegible]
F	CN 502187 (B) LAMB (1) UPDATE REV LEVEL	9-30-82	M B[illegible]
G	CN 502197 (D) S DAWS (1) LM-0001 AND -0002 IT 999 WAS IT 101 AND 102 (2) LM-0001 AND -0002 ADDED IT 27 AND 28 (3) LM 5001 AND 5002 IT 4 WAS PN 2210669-1, ITEM 6 WAS PN 2210658-1, IT 13 PN WAS 2210763-1 (4) ADDED NOTE 7 AND 8 (5) ADD PN 2223273-0001 TO REV LEVEL BLOCK	10-22-82	M B[illegible]
H	CN 502182 (B. Ole[illegible]) (1) LM-5001 & 5002 IT 8 PN WAS 2223265-1 (2) IT 13 PN WAS 2223264-1 (3) IT 4 PN WAS 2223268-1	11-4-82	M B[illegible]



—11.2 MAX PIN HEIGHT

—11.2 MAX PIN HEIGHT

PART NUMBER	DESCRIPTION
2223061-5002	GRAPHICS CRT CONTROLLER - 3 PLANE AUTO INSER
2223061-5001	GRAPHICS CRT CONTROLLER AUTO INSERTER
2223061-0002	GRAPHICS CRT CONTROLLER - 3 PLANE
2223061-0001	GRAPHICS CRT CONTROLLER

PARTS LIST

QTY	QTY	QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

SEQ NO	PROCESS	SPEC	NO	ADDITIONAL CLASSIFICATION	NOTES
3	MARK	902-01	01	HGT 1.5 CLR WHT (CAT 4)	3 4
2	SLDR	127-01	00	HAND SOLDER	
1	SLDR	124-02	00	WAVE SOLDER	

PROCESSES — FOR CORRELATION TO GOVT AND SPECIFICATIONS SEE TI DRAWING 72444

REVISION LEVEL BLOCK						
UNIT TEST	2223273-0001	G	G	G	G
ASSEMBLY	2223061-0001	E	F	G	H
PWB	2223062-0001	B	B	B	B
DIAGRAM	2223063-0001	A	A	A	A

REV STATUS OF SHEETS

APPLICATION: NEXT ASSY 2223040, USED ON 8755

DATE 5-3-82

TEXAS INSTRUMENTS — SI-METRIC

GRAPHICS CRT CONTROLLER

D 06668 2223061

SCALE NONE

320

LM/CC 1

4-43

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION
2223061-0001	H	GRAPHICS,CRT CONTROLLER

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0002	REF	2223063-0001	DIAGRAM,LOGIC,GRAPHICS CRT CONTROLLER	EA
0007	00001.000	2210653-0001	IC,LS138,3-TO-8 LINE DECODER V-LIST-LS138 BURN-IN	EA
0007A			U26 V-LIST-LS138 BURN-IN	
0021	00001.000	2210288-0022	HEADER,1-ROW,22 CONTACTS, .100" CENTERS SEE TI- DRAWING	EA
0021A			P41 SEE TI- DRAWING	
0022	00004.000	0996341-0003	SPACER,PC BOARD,ZYTEL,NATURAL COLOR	EA
0023	00001.000	2210057-0011	HEADER, STR. PIN, 22 POS 007791--87215-7	EA
0023A			P42 007791--87215-7	
0024	REF	0994396-9901	PROCEDURE,SITE & DATE CODE SERIALIZATION	EA
0027	REF	2223273-0001	SPECIFICATION,UNIT TEST-GRAPHICS CRT	EA
0028	AR	0411400-0024	WIRE, 24AWG ELECTRO TIN PLATED COPPER	FT
0999	00001.000	2223061-5001	GRAPHICS,CRT CONTROLLER-AUTO INSERT 1254-3061-002	EA
9999	00001.000	0239999-9999	COST, SHRINKAGE	EA

11/24/82

PART NUMBER	REV	DESCRIPTION
2223061-0002	H	GRAPHICS,CRT CONTROLLER 3 PLANE

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0002	REF	2223063-0001	DIAGRAM,LOGIC,GRAPHICS CRT CONTROLLER	EA
0007	00001.000	2210653-0001	IC,LS138,3-TO-8 LINE DECODER V-LIST-LS138 BURN-IN	EA
0007A			U26 V-LIST-LS138 BURN-IN	
0021	00001.000	2210288-0022	HEADER,1-ROW,22 CONTACTS, .100" CENTERS SEE TI- DRAWING	EA
0021A			P41 SEE TI- DRAWING	
0022	00004.000	0996341-0003	SPACER,PC BOARD,ZYTEL,NATURAL COLOR	EA
0023	00001.000	2210057-0011	HEADER, STR. PIN, 22 POS 007791--87215-7	EA
0023A			P42 007791--87215-7	
0024	REF	0994396-9901	PROCEDURE,SITE & DATE CODE SERIALIZATION	EA
0027	REF	2223273-0001	SPECIFICATION,UNIT TEST-GRAPHICS CRT	EA
0999	00001.000	2223061-5002	GRAPHICS,CRT CONTROLLER 3 PLANE-AUTO INS 1254-3063-004	EA
9999	00001.000	0239999-9999	COST, SHRINKAGE	EA

LIST OF MATERIALS

11/24/82

PART NUMBER 2223061-5001 — REV H — DESCRIPTION: GRAPHICS,CRT CONTROLLER-AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00001.000	2223062-0001	PWB,GRAPHICS CRT CONTROLLER	EA
			SEE TI- DRAWING	
0003	00004.000	2220517-0002	IC,16KX4BIT RAM,330NSEC READ CYCLE TIME	EA
			SEE TI- DRAWING	
0003A			U1,U2,U3,U4	
			SEE TI- DRAWING	
0004	00006.000	2210669-0001	IC,LS166,8-BIT PARALLEL/SERIAL INPUT	EA
			V-LIST-LS166 BURN-IN	
0004A			U13,U14,U15,U16,U17,U18	
			V-LIST-LS166 BURN-IN	
0005	00001.000	2223084-0001	GRAPHICS LOGIC ARRAY	EA
			1254- -000	
0005A			U41	
			1254- -000	
0006	00006.000	2210695-0001	IC,LS245,OCTAL BUS,XCIVER,3ST.OUTPUT	EA
			V-LIST-LS245 BURN-IN	
0006A			U19,U20,U21,U22,U23,U24	
			V-LIST-LS245 BURN-IN	
0007	00001.000	2210653-0001	IC,LS138,3-TO-8 LINE DECODER	EA
			V-LIST-LS138 BURN-IN	
0007A			U25	
			V-LIST-LS138 BURN-IN	
0008	00003.000	2210658-0001	IC,LS151,1-OF-8 DATA SELECTOR/MULTIPLEXE	EA
			V-LIST-LS151 BURN-IN	
0008A			U27,U28,U29	
			V-LIST-LS151 BURN-IN	
0009	00003.000	2210702-0001	IC,LS273,OCTAL,D-FLIP-FLOP W/COM CLOCK	EA
			V-LIST-LS273 BURN-IN	
0009A			U30,U31,U32	
			V-LIST-LS273 BURN-IN	
0010	00004.000	2210659-0001	IC,LS153,DUAL 4-LINE TO 1-L DATA SEL/MPX	EA
			V-LIST-LS153 BURN-IN	
0010A			U33,U34,U35,U36	
			V-LIST-LS153 BURN-IN	
0011	00002.000	2210727-0001	IC,LS393,DUAL,4-BIT BINARY COUNTER	EA
			V-LIST-LS393 BURN-IN	
0011A			U37,U38	
			V-LIST-LS393 BURN-IN	
0012	00001.000	2210720-0001	IC,LS373,OCTAL D-TYPE LATCHES	EA
			V-LIST-LS373 BURN-IN	
0012A			U42	
			V-LIST-LS373 BURN-IN	
0013	00001.000	2210763-0001	IC,S174,HEX,FLIP-FLOP,SINGLE RAIL OUTPUT	EA
			V-LIST-S174 BURN-IN	
0013A			U43	
			V-LIST-S174 BURN-IN	
0014	00002.000	2210667-0001	IC,LS163,SYNC 4-BIT BINARY CNT,SYNC CLR	EA
			V-LIST-LS163 BURN-IN	
0014A			U39,U40	
			V-LIST-LS163 BURN-IN	
0015	00001.000	2210735-0001	IC,S00,QUAD,2-INPUT NAND	EA
			V-LIST-S00 BURN-IN	
0015A			U44	
			V-LIST-S00 BURN-IN	
0016	00001.000	2210604-0001	IC,LS04,HEX INVERTERS	EA
			V-LIST-LS04 BURN-IN	
0016A			U45	
			V-LIST-LS04 BURN-IN	
0017	00004.000	0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0017A			R1,R2,R3,R4	
			ROH - R-25	
0018	00001.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT	EA
			QPL -M39003/1-2304	

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2223061-5001	H	GRAPHICS,CRT CONTROLLER-AUTO INSERT

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0018A			C1	
			QPL -M39003/1-2304	
0019	00019.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS	EA
			004222-MC105E103Z	
0019A			C2,C3,C4,C5,C6,C7,C8,C9,C10	
			004222-MC105E103Z	
0019B			C11,C12,C13,C14,C15,C16,C17	
			004222-MC105E103Z	
0019C			C18,C19,C20	
			004222-MC105E103Z	
0020	00020.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	
0020A			C21,C22,C23,C24,C25,C26,C27	
			COR CA-C03Z5U104Z050A	
0020B			C28,C29,C30,C31,C32,C33,C34	
			COR CA-C03Z5U104Z050A	
0020C			C35,C36,C37,C38,C39,C40	
			COR CA-C03Z5U104Z050A	
0025	00001.000	0972946-0027	RES FIX 27.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0025A			R5	
			ROH - R-25	
0026	00000.000	2220517-0001	IC,16K X 4-BIT,RAM,260NSEC READ CYCLE T	EA
			SEE TI- DRAWING	
0026A			*THIS ITEM MAY BE USED AS	
			SEE TI- DRAWING	
0026B			*AN ALTERNATE TO ITEM 3.	
			SEE TI- DRAWING	

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2223061-5002	H	GRAPHICS,CRT CONTROLLER 3 PLANE-AUTO INS

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION...........................	UM
0001	00001.000	2223062-0001	PWB,GRAPHICS CRT CONTROLLER	EA
			SEE TI- DRAWING	
0003	00012.000	2220517-0002	IC,16KX4BIT RAM,330NSEC READ CYCLE TIME	EA
			SEE TI- DRAWING	
0003A			U1,U2,U3,U4,U5,U6,U7,U8,U9,	
			SEE TI- DRAWING	
0003B			U10,U11,U12	
			SEE TI- DRAWING	
0004	00006.000	2210669-0001	IC,LS166,8-BIT PARALLEL/SERIAL INPUT	EA
			V-LIST-LS166 BURN-IN	
0004A			U13,U14,U15,U16,U17,U18	
			V-LIST-LS166 BURN-IN	
0005	00001.000	2223084-0001	GRAPHICS LOGIC ARRAY	EA
			1254- -000	
0005A			U41	
			1254- -000	
0006	00006.000	2210695-0001	IC,LS245,OCTAL BUS,XCIVER,3ST.OUTPUT	EA
			V-LIST-LS245 BURN-IN	
0006A			U19,U20,U21,U22,U23,U24	
			V-LIST-LS245 BURN-IN	
0007	00001.000	2210653-0001	IC,LS138,3-TO-8 LINE DECODER	EA
			V-LIST-LS138 BURN-IN	
0007A			U25	
			V-LIST-LS138 BURN-IN	
0008	00003.000	2210658-0001	IC,LS151,1-OF-8 DATA SELECTOR/MULTIPLEXE	EA
			V-LIST-LS151 BURN-IN	
0008A			U27,U28,U29	
			V-LIST-LS151 BURN-IN	

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION...........................
2223061-5002 H GRAPHICS,CRT CONTROLLER 3 PLANE-AUTO INS

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0009	00003.000	2210702-0001	IC,LS273,OCTAL,D-FLIP-FLOP W/COM CLOCK	EA
			V-LIST-LS273 BURN-IN	
0009A			U30,U31,U32	
			V-LIST-LS273 BURN-IN	
0010	00004.000	2210659-0001	IC,LS153,DUAL 4-LINE TO 1-L DATA SEL/MPX	EA
			V-LIST-LS153 BURN-IN	
0010A			U33,U34,U35,U36	
			V-LIST-LS153 BURN-IN	
0011	00002.000	2210727-0001	IC,LS393,DUAL,4-BIT BINARY COUNTER	EA
			V-LIST-LS393 BURN-IN	
0011A			U37,U38	
			V-LIST-LS393 BURN-IN	
0012	00001.000	2210720-0001	IC,LS373,OCTAL D-TYPE LATCHES	EA
			V-LIST-LS373 BURN-IN	
0012A			U42	
			V-LIST-LS373 BURN-IN	
0013	00001.000	2210763-0001	IC,S174,HEX,FLIP-FLOP,SINGLE RAIL OUTPUT	EA
			V-LIST-S174 BURN-IN	
0013A			U43	
			V-LIST-S174 BURN-IN	
0014	00002.000	2210667-0001	IC,LS163,SYNC 4-BIT BINARY CNT,SYNC CLR	EA
			V-LIST-LS163 BURN-IN	
0014A			U39,U40	
			V-LIST-LS163 BURN-IN	
0015	00001.000	2210735-0001	IC,S00,QUAD,2-INPUT NAND	EA
			V-LIST-S00 BURN-IN	
0015A			U44	
			V-LIST-S00 BURN-IN	
0016	00001.000	2210604-0001	IC,LS04,HEX INVERTERS	EA
			V-LIST-LS04 BURN-IN	
0016A			U45	
			V-LIST-LS04 BURN-IN	
0017	00004.000	0972946-0081	RES FIX 4.7K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0017A			R1,R2,R3,R4	
			ROH - R-25	
0018	00001.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT	EA
			QPL -M39003/1-2304	
0018A			C1	
			QPL -M39003/1-2304	
0019	00019.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS	EA
			004222-MC105E103Z	
0019A			C2,C3,C4,C5,C6,C7,C8,C9,C10	
			004222-MC105E103Z	
0019B			C11,C12,C13,C14,C15,C16,C17	
			004222-MC105E103Z	
0019C			C18,C19,C20	
			004222-MC105E103Z	
0020	00020.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	
0020A			C21,C22,C23,C24,C25,C26,C27	
			COR CA-C03Z5U104Z050A	
0020B			C28,C29,C30,C31,C32,C33,C34	
			COR CA-C03Z5U104Z050A	
0020C			C35,C36,C37,C38,C39,C40	
			COR CA-C03Z5U104Z050A	
0025	00001.000	0972946-0027	RES FIX 27.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0025A			R5	
			ROH - R-25.	
0026	00000.000	2220517-0001	IC,16K X 4-BIT,RAM,260NSEC READ CYCLE T	EA
			SEE TI- DRAWING	
0026A			*THIS ITEM MAY BE USED AS	
			SEE TI- DRAWING	
0026B			*AN ALTERNATE TO ITEM 3.	
			SEE TI- DRAWING	

2223082

NOTES UNLESS OTHERWISE SPECIFIED

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN 50646 (D) ...	10-27-82	M B...
	(1) CHNG PER ENG REDESIGN		

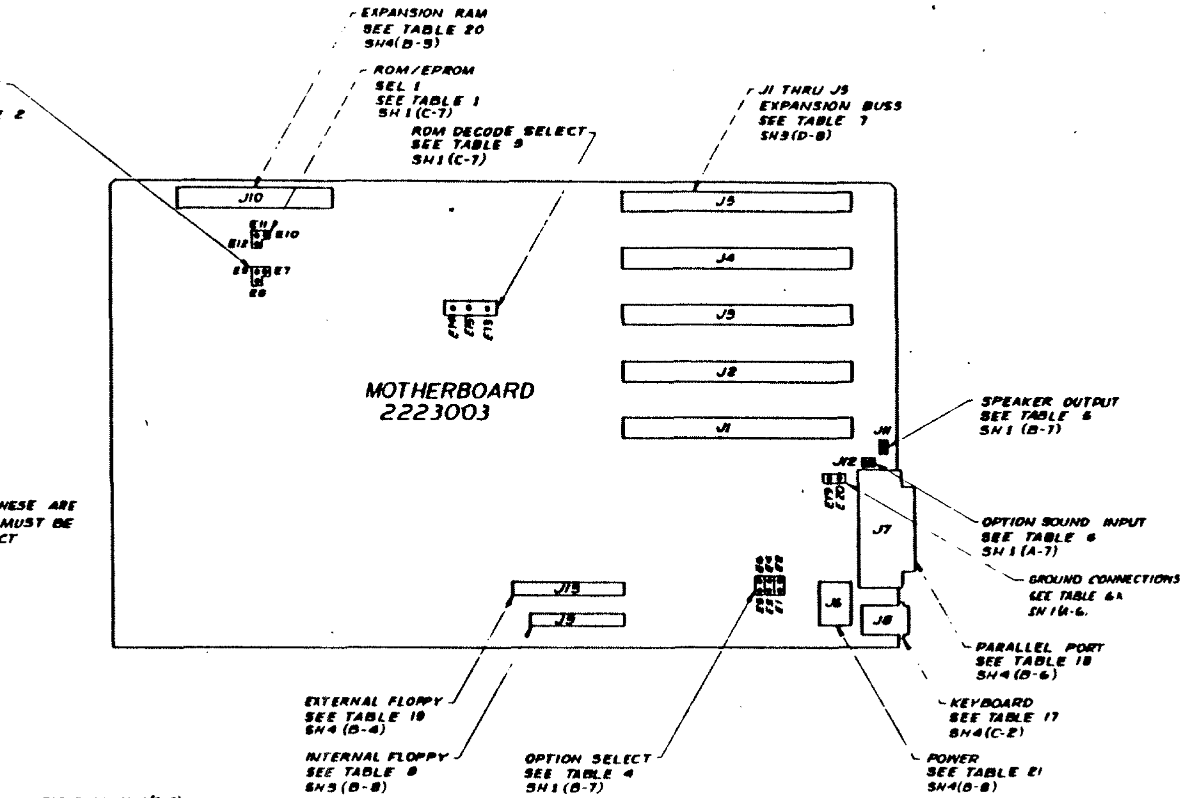


TABLE 1 SH 1 (D-5)

ROM/EPROM SEL 1	
JUMPER	OPTIONS
E11-E10	U63 = ROM
E11-E12	U63 = 4K EPROM

TABLE 2 SH1 (D-7)

ROM/EPROM SEL 2	
JUMPER	OPTIONS
E9-E7	U62=ROM
E8-E9	U62 = 4K EPROM

TABLE 3 SH1 (D-5)

ROM DECODE SELECT	
JUMPER	OPTIONS
E13-E14	4K ROMS DECODE
E13-E15	8K ROMS DECODE

NOTE: (E10-E11, E9-E8, & E13-E15) THESE ARE CONNECTED BY ETCH AND MUST BE CUT TO CHANGE THE SELECT

TABLE 4 SH1 (A-4)

OPTION SELECT	
JUMPER	OPTIONS
E1-E2	DOUBLE SIDED FLOPPIES
E3-E4	RESERVED
E5-E6	50 HZ

TABLE 5 SH1 (C-2)

SPEAKER OUTPUT (J11)	
PIN NO.	SIGNAL
1	SPEAKER
2	GROUND

TABLE 6 SH1 (B-2)

OPTION SOUND INPUT (J12)	
PIN NO.	SIGNAL
1	SOUND IN
2	GROUND

TABLE 6A SH 1 (B-3)

GROUND CONNECTIONS	
PIN NO.	SIGNAL
E19	LOGIC GROUND
E20	CHASSIS GROUND

PARTS LIST

TEXAS INSTRUMENTS

SI-METRIC

ELECTRICAL PIN CONFIGURATION

D 06668 2223082

SCALE NONE SHEET 1 OF 4

APPLICATION: 2223051 8755

REV STATUS OF SHEETS: REV A A A A; SH 1 2 3 4

PROCESS | CLASSIFICATION

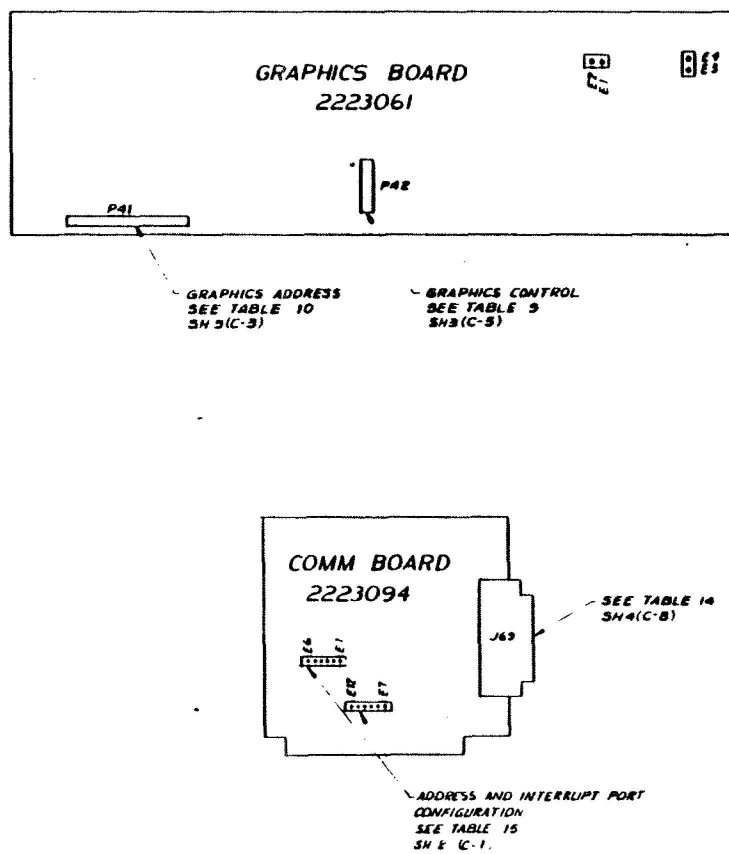


TABLE 15 SH 2 (A-4)

COMM BOARD PORT CONFIG			
PORT #	I/O ADDRESS	JUMPER OPTIONS	INTERRUPT LEVEL
1	ØE6 - ØE7	E1-E2, E7-E8	Ø
2	ØE8 - ØEF	E2-E3, E8-E9	1
3	ØFØ - ØF7	E4-E5, E10-E11	2
4	ØF8 - ØFF	E5-E6, E11-E12	4

TABLE 22 SH D-3 & D-4

BANK SELECT	
JUMPER	OPTION
E1-E2	BLANK GRAPHICS BANK 2
E3-E4	BLANK GRAPHICS BANK 3

2223082 2

TEXAS INSTRUMENTS | D 96214 | 2223082 | SCALE NONE | SHEET 2

2223082 3

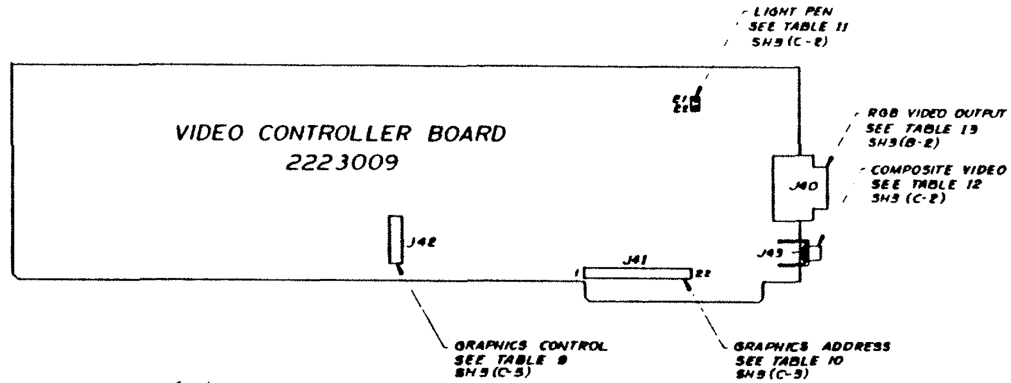


TABLE 7 SH1 (D-3)

EXPANSION BUSS CONNECTORS			
PIN NO.	SIGNAL	PIN NO	SIGNAL
1/A01	NMI-	32/B16	
2/B01	GND	33/A17	XA14
3/A02	XD7	34/B17	
4/B02	RESET	35/A18	XA13
5/A03	XD6	36/B18	
6/B03	+5V	37/A19	XA12
7/A04	XD5	38/B19	
8/B04	IR0	39/A20	XA11
9/A05	XD4	40/B20	CLOCK
10/B05		41/A21	XA10
11/A06	XD3	42/B21	IR6
12/B06		43/A22	XA9
13/A07	XD2	44/B22	IR5
14/B07	-12V	45/A23	XA8
15/A08	XD1	46/B23	IR4
16/B08	DMA-	47/A24	XA7
17/A09	XD0	48/B24	IR1
18/B09	+12V	49/A25	XA6
19/A10	WAIT-	50/B25	IR2
20/B10	GND	51/A26	XA5
21/A11	RFSH	52/B26	
22/B11	AMWC-	53/A27	XA4
23/A12	XA19	54/B27	
24/B12	MRDC-	55/A28	XA3
25/A13	XA18	56/B28	ALE
26/B13	AIOWC-	57/A29	XA2
27/A14	XA17	58/B29	+5V
28/B14	IORC-	59/A30	XA1
29/A15	XA16	60/B30	OSC
30/B15		61/A31	XA0
31/A16	XA15	62/B31	GND

TABLE 8 SH1 (A-5)

INTERNAL FLOPPY CONNECTOR (J9)			
PIN NO.	SIGNAL	FLOPPY 'A' PIN NO.	FLOPPY 'B' PIN NO.
1	GND	1	1
2		2	2
3	GND	3	3
4		4	4
5	GND	5	5
6		6	6
7	GND	7	7
8	INDEX-	8	8
9	GND	9	9
10	SEL1-	10	10
11	GND	11	11
12	SEL2-	12	12
13	GND	13	13
14		14	14
15	GND	15	15
16	MOT-	16	16
17	GND	17	17
18	DIRECT	18	18
19	GND	19	19
20	STEP-	20	20
21	GND	21	21
22	WDATA 1-	22	22
23	GND	23	23
24	WGATE -	24	24
25	GND	25	25
26	TRAK 0 -	26	26
27	GND	27	27
28	WPROT-	28	28
29	GND	29	29
30	RDATA -	30	30
31	GND	31	31
32	SIDI-	32	32
33	GND	33	33
34		34	34

TABLE 9 SH3(C-5), SH2(C-4)

GRAPHICS CONTROL (P42)			
PIN NO.	SIGNAL	P42 PIN NO.	SIGNAL
1	N.C.	2	N.C.
2	GR2-	1	GGNL-
3	GR1-	4	GRDL-
4	GR3-	3	GBLL-
5	XD7	6	D7
6	GRED-	5	GRED-
7	XD6	8	D6
8	GBLU-	7	GBLU-
9	XD5	10	D5
10	GGRN-	9	GGRN-
11	XD4	12	D4
12	DCLK	11	DCLK
13	XD3	14	D3
14	RD-	13	RD-
15	XD2	16	D2
16	WR-	15	WR-
17	XD1	18	D1
18	GSEL	17	GSEL-
19	XD0	20	D0
20	DDE	19	DE
21	GWAIT-	22	GWAIT-
22	RESET-	21	RST-

TABLE 10 SH3(C-2) SH2(C-3)

GRAPHICS ADDRESS (P41)			
PIN NO.	SIGNAL	P41 PIN NO.	SIGNAL
1	A0	1	A0
2	A1	2	A1
3	A2	3	A2
4	A3	4	A3
5	A4	5	A4
6	A5	6	A5
7	A6	7	A6
8	A7	8	A7
9	A8	9	A8
10	A9	10	A9
11	A10	11	A10
12	A11	12	A11
13	A12	13	A12
14	A13	14	A13
15	A14	15	A14
16	A15	16	A15
17	A16	17	A16
18	N.C.	18	N.C.
19	+5V	19	+5V
20	+5V	20	+5V
21	GND	21	GND
22	GND	22	GND

TABLE 11 SH3(D-1)

LIGHT PIN	
PIN NO.	SIGNAL
1	INPUT
2	GND

TABLE 12 SH3(D-1)

COMPOSITE VIDEO	
PIN	SIGNAL
BODY	GND
CENTER	OUTPUT

TABLE 13 SH3(D-1)

RGB VIDEO OUTPUT	
PIN NO.	SIGNAL
1	GND
2	GND
3	VRED
4	VGRN
5	VBLU
6	GND
7	N.C.
8	HDRIVE
9	VDRIVE

TEXAS INSTRUMENTS | D 96214 | 2223082 | SCALE NONE | SHEET 3

8 | 7 | 6 | 5 | 4 | 3 | 2223082 | 4 | 1

TABLE 14 SH2(B-4)

J69	
PIN NO.	SIGNAL
1	CHASSIS GND
2	TXD
3	RXD
4	RTS
5	CTS
6	DSR
7	SIGNAL GND
8	DCD
9	
10	
11	SCA/CH
12	SCF/CI
13	
14	
15	TXC
16	
17	RXC
18	
19	
20	DTR
21	
22	RI
23	SCA/CH
24	BAUDOUT/DA

~~TABLE 15 [illegible]~~

(COMMUNICATIONS BOARD) ADDRESS CONFIG *	
I/O ADDRESS	JUMPER OPTIONS
FF0X	E15-E18, E16-E19, E17-E20
FF2X	E3-E6, E15-E18, E16-E19
FF4X	E2-E5, E15-E18, E17-E20
FF6X	E2-E5, E3-E6, E15-E18
FF8X	E1-E4, E16-E19, E17-E20
FFAX	E1-E4, E16-E19, E3-E6
FFCX	E1-E4, E2-E5, E17-E20
FFEX	E1-E4, E2-E5, E3-E6

~~* THESE ARE THE ONLY ALLOWABLE JUMPER CONFIGURATIONS~~

~~TABLE 16 [illegible]~~

INTERRUPT LEVEL CONFIGURATIONS *	
LEVEL	JUMPER OPTIONS *
1	E7-E8
2	E9-E10
4	E11-E12
8	E13-E14

~~* ONLY ONE JUMPER ALLOWED~~

TABLE 17 SH 1 (B-2)

KEYBOARD (J8)			
PIN NO.	SIGNAL	KEYBOARD PWB CONN	COLOR
1	PWR (+12V)	E2	GRN
2	RCV DATA	E3	RED
3	XMIT DATA	E4	BLK
4	LOOPBACK DATA	E5	BLU
5	GND	E1	YEL

TABLE 18 SH1 (B-2)

PARALLEL PORT (J7)	
PIN NO.	SIGNAL
1	PTSTR-
2	PD1
3	PD2
4	PD3
5	PD4
6	PD5
7	PD6
8	PD7
9	PD8
10	PACK-
11	PBUSY
12	PAPOUT
13	PSELECT
14	PTAF-
15	PFAULT
16	PTINIT-
17	GND
18	↓
19	↓
20	↓
21	↓
22	↓
23	↓
24	↓
25	GND

TABLE 19 SH1 (B-3)

EXTERNAL FLOPPY CONNECTOR (J13)					
PIN NO.	SIGNAL	37 PIN D CONN	PIN NO.	SIGNAL	37 PIN D CONN
1	GND	20	21	GND	30
2		1	22	DIRECT2-	11
3	GND	21	23	GND	31
4		2	24	STEP2-	12
5	GND	22	25	GND	32
6		3	26	WDATA2-	13
7	GND	23	27	GND	33
8		4	28	WGATE2-	14
9	GND	24	29	GND	34
10		5	30	TRAK0-	15
11	GND	25	31	GND	35
12	INDEX-	6	32	WPORT-	16
13	GND	26	33	GND	36
14	MOT3-	7	34	RDATA-	17
15	GND	27	35	GND	37
16	SEL4-	8	36	SIDI-	18
17	GND	28	37	GND	
18	SEL3-	9	38		19
19	GND	29	39	GND	
20	MOT4-	10	40		

TABLE 20 SH1 (D-5)

EXPANSION RAM CONECTOR (J10)			
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1		23	
2		24	MA4
3		25	
4	MD7	26	P0
5	GND	27	
6	GND	28	MA6
7		29	
8	AMINC-	30	PE
9	+5V	31	CAS-
10	+5V	32	MD8
11		33	MD2
12	MA1	34	MD1
13		35	MD4
14	MA5	36	MD3
15		37	
16	MA7	38	MD5
17		39	
18	MA0	40	MD6
19		41	+5V
20	MA2	42	+5V
21		43	GND
22	MA3	44	GND

TABLE 21 SH1 (A-3)

POWER CONN (J6)	
PIN NO.	SIGNAL
1	+12V
2	+5V
3	GND
4	-12V
5	+5V
6	GND

TEXAS INSTRUMENTS | 6/2/81 | D 96214 | 2223082 | A | SCALE NONE | SHEET 4

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

NOTES UNLESS OTHERWISE SPECIFIED

[1] MAXIMUM COMPONENT HEIGHT ABOVE THE BOARD SHALL BE 19.0

[2] MAXIMUM LEAD LENGTH BELOW THE BOARD SHALL BE 2.3

[3] MARK APPROPRIATE ~~DASH NUMBER AND~~ REVISION LETTER IN SPACE INDICATED PER PROCESS 3

[4] MARK SITE DATE CODE AND SERIAL NUMBER IN SPACE INDICATED PER ITEM 25 PARAGRAPH 4.0 AND PROCESS 3

5. CAUTION THIS ASSEMBLY AND CERTAIN COMPONENTS ARE SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE. OPERATOR AND EQUIPMENT GROUND AND PACKAGE IS REQUIRED. STATIC SENSITIVE COMPONENT ARE: U1 THRU U11, Y1

[6] REMOVE 2 PANHEAD SCREWS FROM ITEM 21 PRIOR TO ASSY AND DISCARD

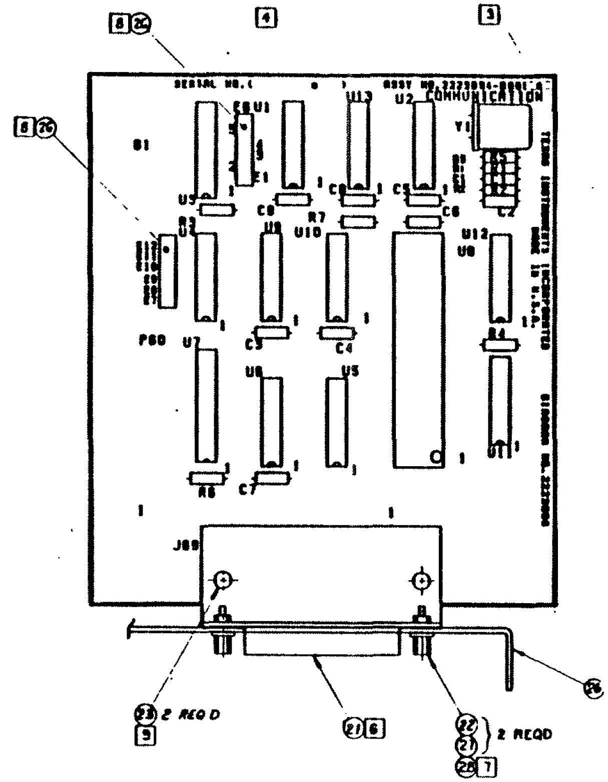
[7] APPLY ITEM 28 TO ITEM 22 AFTER ASSY

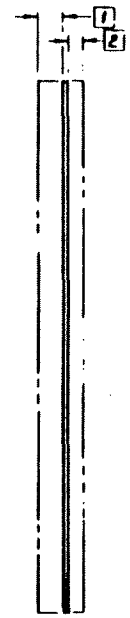
[8] INSTALL ITEM 26 (QTY 2) 1 EACH TO E7-E8 AND E1-E2

[9] INSTALL ITEM 23 FROM CONDUCTOR SIDE

2223094 E

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	LM UPDATE		
	FORMAL RELEASE		
B	CN 476726 (E) R. FLORES (1) LM UPDATE	6/25/82	M. BIEHL
C	CN 497454 (E) BLOCK (1) LM UPDATE	8/24/82	M. BIEHL
D	CN 502113 (D) LAMB (1) LM UPDATE (2) ADD NOTES 6 THRU 9 (3) ADD UNIT TEST TO REV LEVEL BLOCK	10-8-83	MB
E	CN 502400 (C) (1) LM UPDATE	11-4-83	MB





CONVERSION CHART	
mm	INCHES
0.25	.010
0.5	.02
1.5	.06
2.3	.09
19.0	.75

PART NO	DESCRIPTION
2223094-5001	COMMUNICATIONS CARD-AUTO INSERT
2223094-0001	COMMUNICATIONS CARD

QTY 3	QTY 2	QTY 1	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

SEQ NO	IDENT	P SPEC	NO	ADDITIONAL CLASSIFICATION	NOTES
3	MARK	902-01	01	HGT 1.6 CLR WHT (CAT 4)	3 4
2	SLDR	127-01	00	HAND SOLDER	
1	SLDR	124-02	00	WAVE SOLDER	

PROCESSES — FOR CORRELATION TO GOVT AND SPECIFICATIONS SEE TI DRAWING 1394?

REV. LEVEL BLOCK					
UNIT TEST	2223274-0001			D	E
ASSEMBLY	2223094-0001	B	C	D	E
PWB	2223093-0001	B	B	B	B
DIAGRAM	2223096-0001	A	A	B	B

REV STATUS OF SHEETS

NEXT ASSY	USED ON
2223040	8755

APPLICATION

MIKE BIEHL 5/25/82
GRAY McCORD
GRAY McCORD
RALPH CAPAN
SUSAN BRIDGEN
JIM MOON

TEXAS INSTRUMENTS

SI-METRIC

COMMUNICATIONS CARD

D 06668 2223094

SCALE NONE

320

LM

LIST OF MATERIALS

11/24/82

PART NUMBER 2223094-0001 REV F DESCRIPTION........................... COMMUNICATION CARD ASSEMBLY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0002	REF	2223096-0001	DIA,LOGIC,DETAILED,COMMUNICATIONS CARD	EA
0010	00001.000	2220519-0001	IC,USART,SERIAL COMMUNICATIONS CONT	EA
			1254- -000	
0010A			U8	
			1254- -000	
0019	00001.000	2210835-0003	CRYSTAL QUARTZ, 4.9152 MHZ, HC181U	EA
			SEE TI- DWG	
0019A			Y1	
			SEE TI- DWG	
0020	00002.000	2210288-0006	HEADER, 6-PINS .600 L,SNG ROW,STRT-POST	EA
			SEE TI- DRAWING	
0020A			E1-E6,E7-E12	
			SEE TI- DRAWING	
0021	00001.000	2220488-0003	CONNECTOR,RECEPTACLE,PCB,25-PINS	EA
			SEE TI- DRAWING	
0021A			J69	
			SEE TI- DRAWING	
0022	00002.000	0532348-0401	STUD, EXTENSION-CRES	EA
0023	00002.000	0972446-0013	RIVET,.116 DIA 5/16 LG DOME HD ALUM	EA
			- - -000	
0024	REF	0994396-9901	PROCEDURE,SITE & DATE CODE SERIALIZATION	EA
0025	00001.000	2223033-0002	PLATE,OPTION BOARD,WITH CUT OUT	EA
			1678-3223-007	
0026	00002.000	0972487-0001	JUMPER PLUG,CONNECTOR BLACK	EA
			5935-0900-000	
0027	00002.000	0411100-0070	LOCKWASHER #4 INTERNAL TOOTH CRES	EA
			OPL - MS35333-70	
0028	AR	0415804-0005	SEALING COMPOUND,ANAEROBIC-BLUE GRADE C	OT
0030	REF	2223274-0001	SPECIFICATION,UNIT TEST-COMMUNICATIONS	EA
0031	AR	0411435-0408	TAPE,INSULATION,ELECT.1/4 IN	RL
			MMM - 56-1/4	
0999	00001.000	2223094-5001	AUTO-INSERTED PARTS LIST FOR -0001	EA
			1254-3095-003	
9999	00001.000	0239999-9999	COST, SHRINKAGE	EA

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION..........................
2223094-5001 F AUTO-INSERTED PARTS LIST FOR -0001

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00001.000	2223095-0001	PWB COMMUNICATIONS CARD	EA
			1254- -000	
0003	00001.000	2210621-0001	IC,LS32,QUAD,2-INPUT OR	EA
			V-LIST-LS32 BURN-IN	
0003A			U1	
			V-LIST-LS32 BURN-IN	
0004	00001.000	2210608-0001	IC,LS10,TRIPLE,3-INPUT NAND	EA
			V-LIST-LS10 BURN-IN	
0004A			U2	
			V-LIST-LS10 BURN-IN	
0005	00001.000	2210654-0001	IC,LS139,DUAL 2-TO-4 LINE DECODER	EA
			V-LIST-LS139 BURN-IN	
0005A			U3	
			V-LIST-LS139 BURN-IN	
0006	00001.000	2210600-0001	IC,LS00,QUAD,2-INPUT NAND	EA
			V-LIST-LS00 BURN-IN	
0006A			U4	
			V-LIST-LS00 BURN-IN	
0007	00002.000	2210631-0001	IC,LS74,DUAL D FLIP-FLOP W/PSET & CLR	EA
			V-LIST-LS74 BURN-IN	
0007A			U5,U13	
			V-LIST-LS74 BURN-IN	
0008	00001.000	2210602-0001	IC,LS02,QUAD,2-INPUT NOR	EA
			V-LIST-LS02 BURN-IN	
0008A			U6	
			V-LIST-LS02 BURN-IN	
0009	00001.000	2210695-0001	IC,LS245,OCTAL BUS,XCIVER,3ST.OUTPUT	EA
			V-LIST-LS245 BURN-IN	
0009A			U7	
			V-LIST-LS245 BURN-IN	
0011	00002.000	2211189-0001	IC,SN75188NP3,BURN-IN,QUADRUPLE LINE DRI	EA
			SEE TI- DRAWING	
0011A			U9,U10	
			SEE TI- DRAWING	
0012	00002.000	2211349-0001	IC,SN75189AN3, QUAD LINE RECEIVERS	EA
			SEE TI- DRAWING	
0012A			U11,U12	
			SEE TI- DRAWING	
0014	00001.000	0972946-0085	RES FIX 6.8K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0014A			R3	
			ROH - R-25	
0015	00006.000	0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	EA
			ROH - R-25	
0015A			R1,R2,R4,R5,R6,R7	
			ROH - R-25	
0016	00001.000	2211247-0029	CAP,1000 PF,10%,50VDC,CERAMIC	EA
			SEE TI- DRAWING	
0016A			C1	
			SEE TI- DRAWING	
0017	00001.000	2211247-0010	CAP,12.0 PF, 5%,50VDC,CERAMIC	EA
			SEE TI- DRAWING	
0017A			C2	
			SEE TI- DRAWING	
0018	00007.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS	EA
			004222-MC105E103Z	
0018A			C3,C4,C5,C6,C7,C8,C9	
			004222-MC105E103Z	

2223106

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CN502107 (D)		M Ball
	(1) LM-1 DELE IT3 539130-3 QTY 25 (2) LM-1 DELE IT5 2210505-7 QTY 6.5 (3) LM-1 ADD IT 10 (4) GENERATE LM-5001		
B	CN503708 (D)	9-21-83	M Ball
	(1) GENERATE LM-2 & -5002 (2) UPDATE LM-1 & -5001 (3) ADD NOTE 6 (4) NOTE 4 WAS MK "PRL PRINT" PER PROCS I (5) NOTE 5 WAS MK P/N & REV LTR PER PROCS I (6) DELE PRCS I		

NOTES UNLESS OTHERWISE SPECIFIED

1. CABLE CLAMP SCREWS AND RETAINER SCREWS INCLUDED WITH ITEM 2
2. P2 DRAIN WIRE FOLDED UNDER CLAM SHELLS OF CABLE CLAMP ASSEMBLY.
3. P1 DRAIN WIRE TO BE TERMINATED TO CABLE CLAMP SCREW BY SOLDER LUG ITEM 7
4. MARK PER ITEM 9; LINE 4 TEXT: PARALLEL PRINTER
5. MARK PER ITEM 9; LINE 4 TEXT: P2
6. ITEM 11 TO BE WRAPPED AROUND CABLE AND SECURED UNDER CABLE CLAMP

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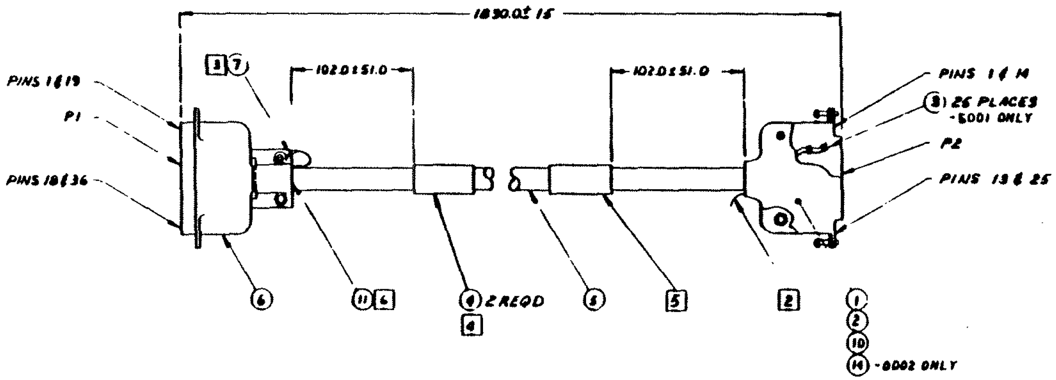


CONVERSION CHART	
mm	INCHES
0.25	0.010
0.5	0.02
3.18	0.125
102 ± 51.0	4.0 ± 2.0
1830 ± 15.0	72.0 ± 6.0

PART NO	DESCRIPTION
2223106-5002	CABLE ASSY PARALLEL, PRINTER, BULK/850
2223106-0002	CABLE ASSEMBLY, PARALLEL, PRINTER/850
2223106-5001	CABLE ASSY PARALLEL, PRINTER, BULK
2223106-0001	CABLE ASSEMBLY, PARALLEL, PRINTER

PARTS LIST

TEXAS INSTRUMENTS — SI-METRIC

CABLE ASSEMBLY, PARALLEL, PRINTER

NEXT ASSY 2223040 — USED ON 8752, 8755 — APPLICATION

D 06668 — 2223106

SCALE NONE

4 340

LM

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223106-0001	B	CABLE ASSEMBLY,PARALLEL,PRINTER

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2220401-0003	CONNECTOR,PLUG,25X#20 AWG,SPRING	EA
0002	00001.000	2220380-0008	CABLE CLAMP ASSY,.400 IN. DIA. CABLE ACC SEE TI- DRAWING	EA
0006	00001.000	0414127-0001	CONNECTOR,PLUG-36 CONTACTS	EA
0007	00001.000	2220955-0001	SOLDER LUG, #4 SCREW 1254- -000	EA
0008	00001.000	2223107-0001	WIRE LIST PT TO PT PRL PTR CABLE ASSY	EA
0009	REF	2265070-0001	SPEC, PRE-PRINTED CABLE MARKER	EA
0010	00001.000	2220797-0001	FERRULE,CABLE CLAMP,SPLIT RING ALUMINUM SEE TI- DRAWING	EA
0101	00001.000	2223106-5001	BULK CABLE ASSY,PARALLEL,PRINTER 1650- -000	EA

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223106-0002	B	CABLE ASSY,PARALLEL,PRINTER/850

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2220767-0002	CONNECTOR,PLUG,25 CONTACTS,2-ROW,22-26AG SEE TI- DRAWING	EA
0001A			P2 SEE TI- DRAWING	
0002	00001.000	2220380-0008	CABLE CLAMP ASSY,.400 IN. DIA. CABLE ACC SEE TI- DRAWING	EA
0006	00001.000	2220674-0001	CONNECTOR,RND CA TO PANEL,PLUG,STL SHELL SEE TI- DWG	EA
0006A			P1 SEE TI- DWG	
0008	REF	2223107-0001	WIRE LIST PT TO PT PRL PTR CABLE ASSY	EA
0009	REF	2265070-0001	SPEC, PRE-PRINTED CABLE MARKER	EA
0010	00001.000	2220797-0001	FERRULE,CABLE CLAMP,SPLIT RING ALUMINUM SEE TI- DRAWING	EA
0013	00000.000	0414127-0001	CONNECTOR,PLUG-36 CONTACTS	EA
0014	00001.000	2220827-0003	CONNECTOR,COVER,CAP,OR HOOD SEE TI- DRAWING	EA
0101	00001.000	2223106-5002	BULK CABLE ASSY PARALLEL 1620-8106-001	EA

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2223106-5001	B	BULK CABLE ASSY,PARALLEL,PRINTER

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0003	00025.000	0539430-0003	CONTACT,PIN 24-20AWG .068 INSUL DIA AMP -205202-2 ST	EA
0004	00002.000	2210317-0001	LABEL,BLANK,CABLE MARKER 085480-SLPF-19319-4	EA
0005	00006.500	2210505-0007	CABLE,SHIELDED,25 CONDUCTORS SEE TI- DRAWING	FT
0011	00000.130	0972361-0003	TAPE,FOAM,VINYL,SELF-ADH.25THK .50WIDE 012624-V548	RL

LIST OF MATERIALS

11/24/92

PART NUMBER	REV	DESCRIPTION..............................
2223106-5002	B	BULK CABLE ASSY PARALLEL

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0004	00002.000	2210317-0001	LABEL,BLANK,CABLE MARKER 085480-SLPF-19319-4	EA
0005	00007.000	2210505-0007	CABLE,SHIELDED,25 CONDUCTORS SEE TI- DRAWING	FT
0007	00001.000	2211389-0001	LUG,RING TONGUE,20-16AWG SEE TI- DRAWING	EA
0011	00000.130	0972361-0003	TAPE,FOAM,VINYL,SELF-ADH.25THK .50WIDE 012624-V548	RL

DWG NO 2223105 SH 1

APPLICATION	
NEXT ASSY	USED ON
2223046	8755

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

1.0 SCOPE:

THIS SPECIFICATION COVERS THE REQUIREMENTS FOR A MONITOR CABLE.

2.0 APPLICABLE DOCUMENTS:

WHERE THIS SPECIFICATION REFERS TO ANOTHER DOCUMENT, THAT DOCUMENT IS OF THE ISSUE IN EFFECT ON THE DATE OF INVITATION TO BID OR REQUEST FOR PROPOSAL. REFERENCED DOCUMENT APPLY TO THE EXTENT SPECIFIED HEREIN. THIS SPECIFICATION GOVERNS WHEN A REFERENCED DOCUMENT CONFLICTS.

CONVERSION CHART	
mm	INCHES
0.25	.010
0.5	.02
3.81	.150
1219.2	48.00

SPECIFICATION CONTROL DRAWING

REV STATUS OF SHEETS — SHEET 1 2 3 4

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLE ± 1°, 1 PLACE DECIMALS ± 0.5, 2 PLACE DECIMALS ± 0.25
- PARENTHETICAL INFO FOR REF ONLY

THIRD ANGLE PROJECTION

DWN DUNHAM DATE 5/12/82
CHK M. Bi... 6-10-82
ENGR
APVD-ENGR
QA
APVD-MFG
RLSE ... 6/11/82

TEXAS INSTRUMENTS INCORPORATED Digital Systems Group

SI-METRIC

INTERFACE CABLE, MONOCHROME MONITOR

SIZE A FSCM NO 06668 DRAWING NO 2223105

SCALE NONE SHEET 1 OF 4

100

3.0 REQIREMENTS:

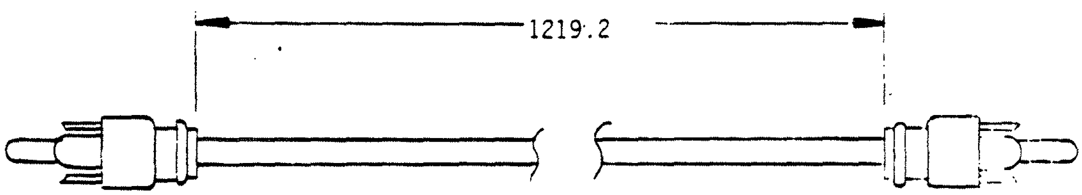
3.1 PHYSICAL: SEE FIGURE 1

3.1.1 CABLE MATERIAL:
ONE CONDUCTOR #27 AWG CONSISTING OF 7 STRANDS OF #56 AWG BARE COPPER WIRE OR 7 STRANDS OF #35 BARE COPPER COVERED STEEL WIRE. SHELD CONSISTS OF 4 ENDS OF #36 AWG TINNED COPPER SPIRAL WRAPPED OR BRAIDED COPPER WIRE. INTERNAL INSULATION OF POLYETHYLENE WITH OUTER JACKET AND CONNECTOR MOLDING TO BE LIGHT TAN IN COLOR MATCHING TI COLOR NUMBER 972939-2101. CABLE ASSEMBLY TO MEET THE REQUIREMENTS OF UL AND CSA.

3.1.2 MARKINGS:
PARTS OR WRAPPER SHALL BE MARKED WITH TEXAS INSTRUMENTS PART NUMBER .

3.1.3 IMPEDANCE:
CABLE IMPEDANCE SHALL BE 75 Ω NOMIMAL.

3.1.4 CONNECTORS:
BOTH ENDS OF THE SHIELDED CABLE SHALL BE TERMINATED EITHER WITH VICTOR PC-103 PHONO PLUGS OR BELDEN STYLE PHG761 SHORT STRAIGHT HANDLE PHONO PLUGS.



CABLE DIA. 3.81 NOM

FIGURE 1

4.0 QUALITY ASSURANCE PROVISIONS:

4.1 RESPONSIBILITY FOR INSPECTION:
UNLESS OTHERWISE SPECIFIED IN THE CONTRACT OR PURCHASE ORDER, THE SUPPLIER SHALL BE RESPONSIBLE FOR PERFORMING INSPECTIONS THAT ARE SUFFICIENT TO ASSURE THAT THE PARTS SUPPLIED MEET THE REQUIREMENTS SPECIFIED HEREIN.

5.0 PREPARATION FOR DELIVERY:

5.1 PACKAGING:
PACKING AND WRAPPING SHALL BE SUFFICIENT TO PROTECT AGAINST DAMAGE OR LOSS DURING SHIPMENT FROM THE SUPPLIER TO THE DESTINATION SPECIFIED IN THE PURCHASE ORDER.

5.2 MARKING:
THE SHIPPING CONTAINER SHALL BE MARKED WITH THE TI PART NUMBER (SEE PART NUMBER BLOCK) AND THE COUNT CONTAINED. ADDITIONAL MARKING ARE PERMITTED.

SUGGESTED SOURCE(S) OF SUPPLY:

1. BELDEN CORPORATION
   P.O. BOX 1980
   RICHMOND, INDIANA 47374

2. VICTOR ELECTRIC WIRE & CABLE CO.
   618 MAIN ST.
   WEST WARWICK,R.I. 02893

TEXAS INSTRUMENTS PART NUMBER	MANUFACTURER'S PART NUMBERS		
	SOURCE 1	SOURCE 2	SOURCE 3
2223105-0001	IF-4310	TBD	

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS DIVISION
HOUSTON TEXAS

A	2223105	REV	
	SHEET 4		

TI—4259-E

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION............................
2207985-0001	C	TEST PLUG, EIA, COMMUNICATIONS

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION............................	UM
0001	00001.000	0539903-0001	HOOD,CONN 25 PIN WITH RETAINERS AMP - 206478-3	EA
0002	00001.000	0539409-0005	CONNECTOR,PLUG 25 PINS AMP -205208-1	EA
0002A			P1	
0003	00012.000	0539430-0003	CONTACT,PIN 24-20AWG .068 INSUL DIA AMP -205202-2 ST	EA
0004	00001.750	2210012-1999	WIRE,ELECT,WHT,26 AWG,19 X 38,U/L 1429 090484-SEE TI DWG	FT

LIST OF MATERIALS

11/24/82

PART NUMBER REV DESCRIPTION..............................
2223099-0001 B PART NUMBER NOT AN ASSEMBLY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..........................	UM
0001	00009.000	2211118-0004	IC,64K-BIT DYNAMIC RAM,150NS TA/ROW TMS416-4-15NL	EA
0002	00001.000	2211752-0001	PLASTIC BAG, ANTI-STATIC SEE TI- DRAWING	EA
0003	AR	0970950-0003	URETHANE,SHEET SEE TI- DRAWING	EA
0004	00001.000	2223269-0001	CAUTION INSERT,RAM CHIP KIT	EA
0005	REF	0936660-0001	PEGASUS PACKAGING ASSY INDEX	EA

LIST OF MATERIALS

11/24/82

PART NUMBER	REV	DESCRIPTION..............................
2230528-0001	B	KEYBOARD,TILTING,LOW PROFILE

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION..............................	UM
0001	00001.000	2230529-0001	BASE,KEYBOARD 1255-7500-001	EA
0002	00001.000	2230536-0001	HOUSING,SHAFT,RIGHT 1255-7504-001	EA
0003	00001.000	2230534-0001	HOUSING,SHAFT,LEFT 1255-7503-001	EA
0004	00002.000	2230532-0001	SHAFT,CLUTCH SPRING 1255-7502-001	EA
0005	00001.000	2230546-0001	SPRING,CLUTCH,RIGHT	EA
0006	00001.000	2230546-0002	SPRING,CLUTCH,LEFT	EA
0007	00001.000	2230547-0002	SPRING,RETURN,RIGHT	EA
0008	00001.000	2230547-0001	SPRING,RETURN,LEFT	EA
0009	00001.000	2230540-0001	FOOT,TILT ADJUSTMENT 1255-7506-001	EA
0010	00001.000	2230527-0001	KEYBOARD,LOW PROFILE	EA
0011	00001.000	2230530-0001	COVER,KEYBOARD 1255-7501-001	EA.
0012	00002.000	2230538-0001	BUTTON,RELEASE 1255-7505-001	EA
0013	00002.000	2230554-0001	BRACKET,SPRING,BUTTON ----------000	EA
0014	00002.000	2230552-0001	CLIP,CLUTCH ----------000	EA
0015	00001.000	2230549-0001	CABLE ASSY,KEYBOARD	EA
0016	00001.000	2230553-0001	LABEL,SERIAL NO 1665-1553-000	EA
0017	00002.000	0972679-0029	SCREW	EA
0018	00012.000	0972679-0012	SCREW # 6-19 X 3/8 SLOTTED HEX	EA
0019	00002.000	0972679-0015	SCREW #6-19 X 3/4 THD SLOTTED HEX	EA
0020	00002.000	2230555-0007	RING,RETAINING	EA
0021	00001.000	0996943-0001	LABEL, SELF-DESTRUCT, .656 X .25 1652-1274-000	EA
0022	00002.000	2230556-0001	PAD,NONSKID,P/T	EA

Section 5

SCHEMATICS AND LOGIC DRAWINGS

This section contains schematic and logic drawings applicable to the Texas Instruments Professional Computer.

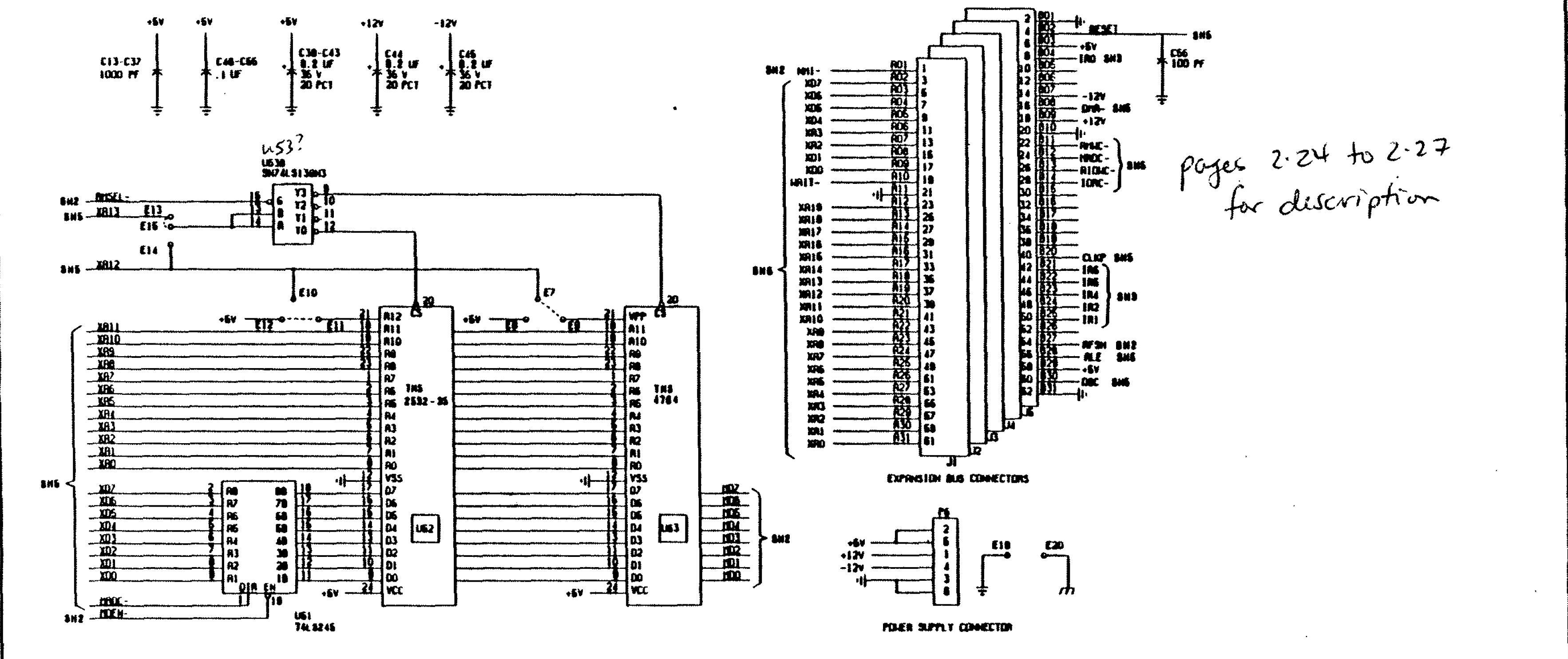
Drawings not available in time for printing:

Logic, Joystick	2223087*
Logic,Parallel Test Plug	2223278*

NOTES UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE .25 W, 5 PCT
2. CAPACITORS ARE 50 V, P80/M20 PCT
3. "NC" MEANS NOT CONNECTED

REV	DESCRIPTION	DATE	APPROVED
A	CN500540 (D) J Kavanaugh	9-13-82	



pages 2.24 to 2.27 for description

MOTHERBOARD ROMS & EXPANSION BUS

HIGHEST REFERENCE DESIGNATOR USED				
U67	C58	CR4	E20	J13
R48	Q2	Y1		

REFERENCE DESIGNATORS NOT USED				
E16				

TEXAS INSTRUMENTS

DIAGRAM, LOGIC, DETAILED-MOTHER BOARD

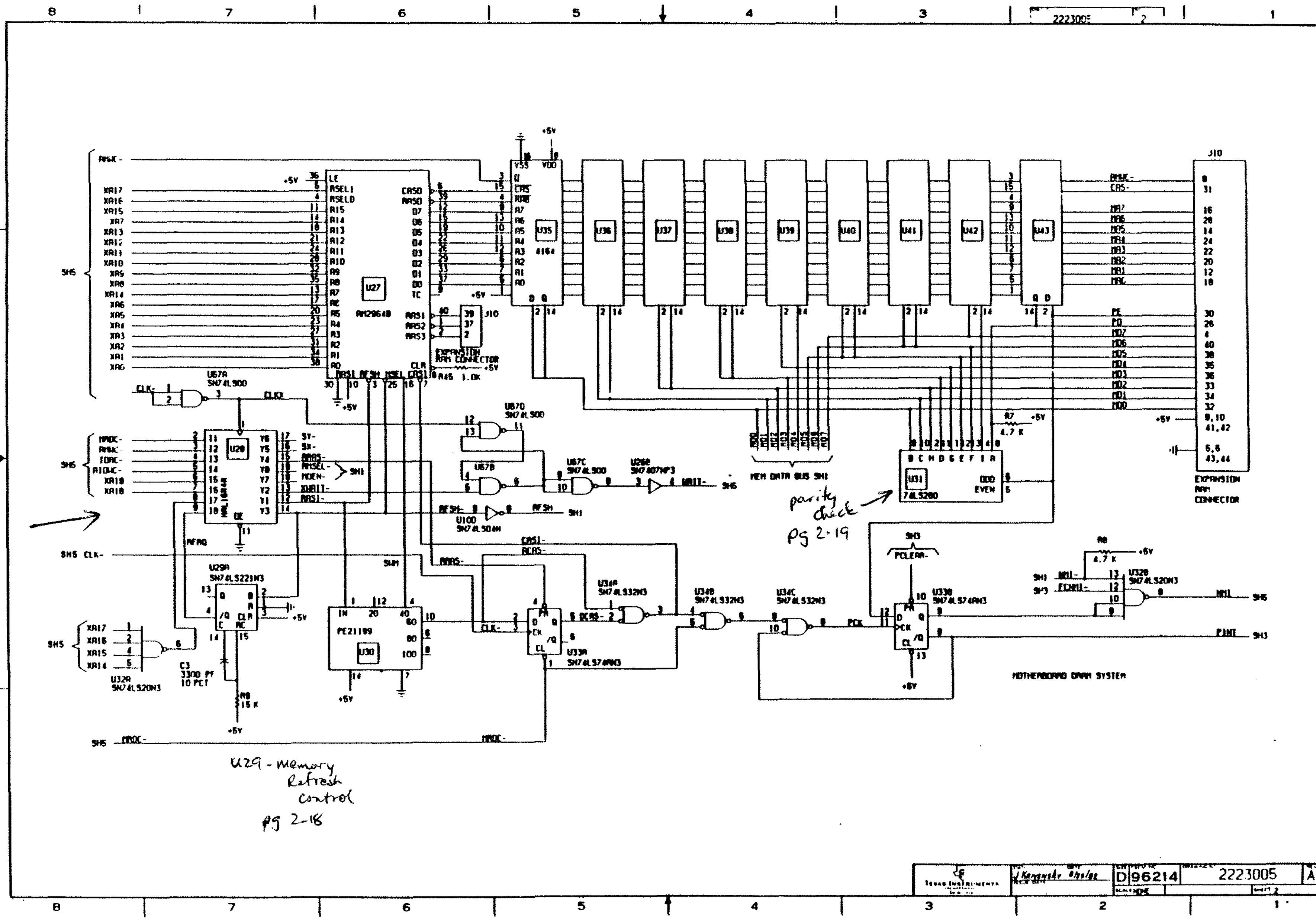
D 96214 2223005

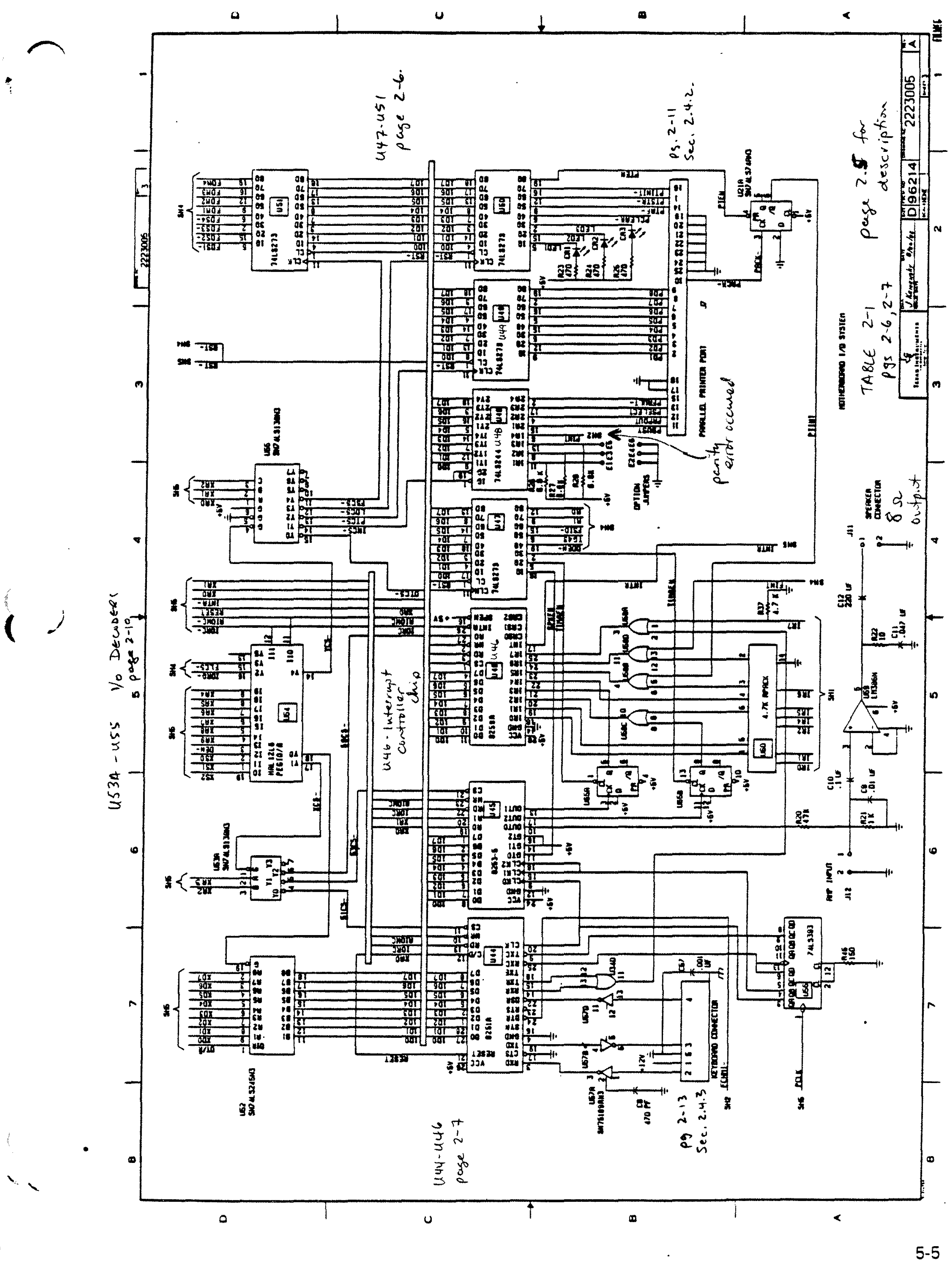
2223003 9766 NEXT ASSY USED ON APPLICATION

430

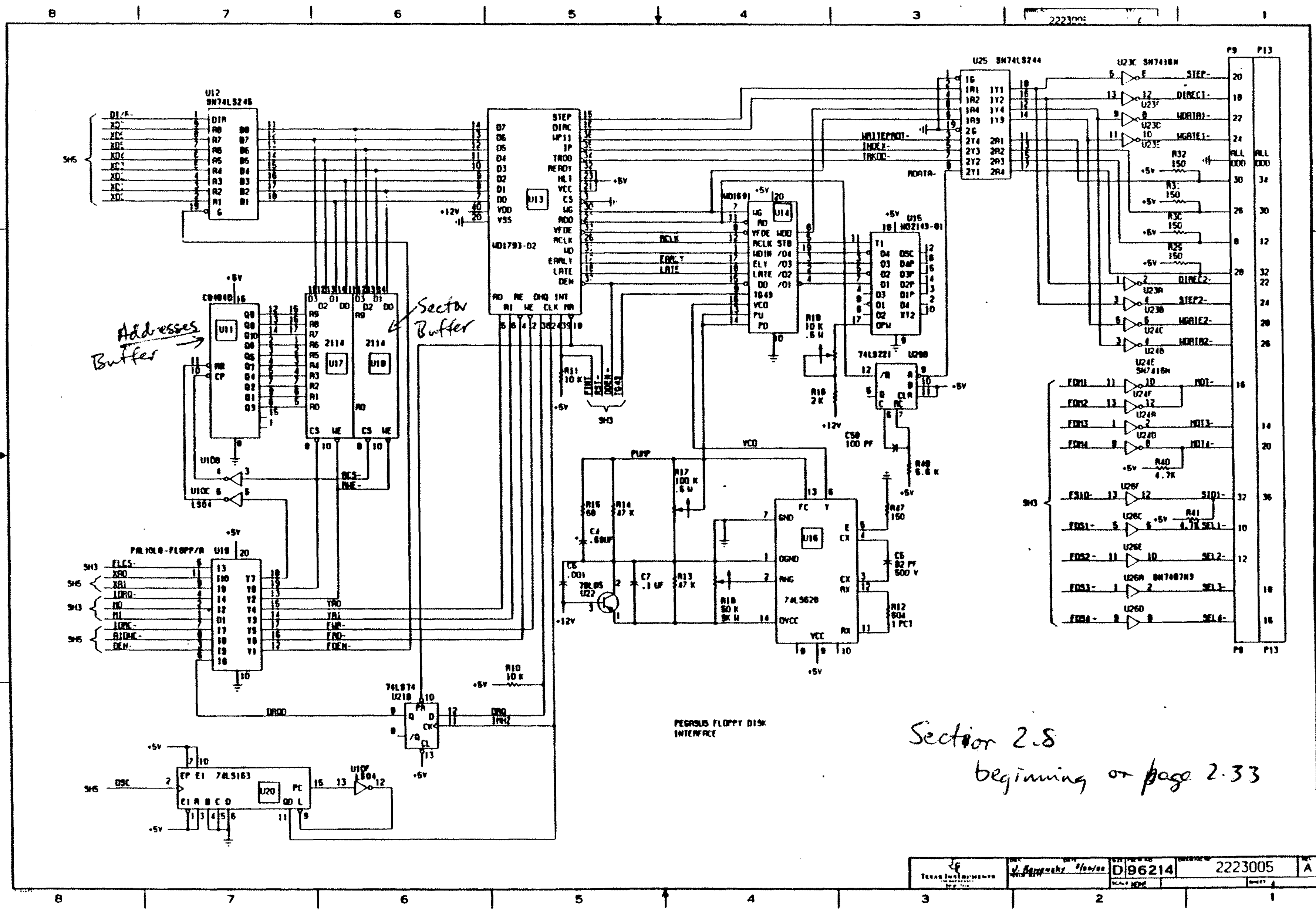
SHEET 1 OF 5

Memory Control State pg 2-21 Table 2-7

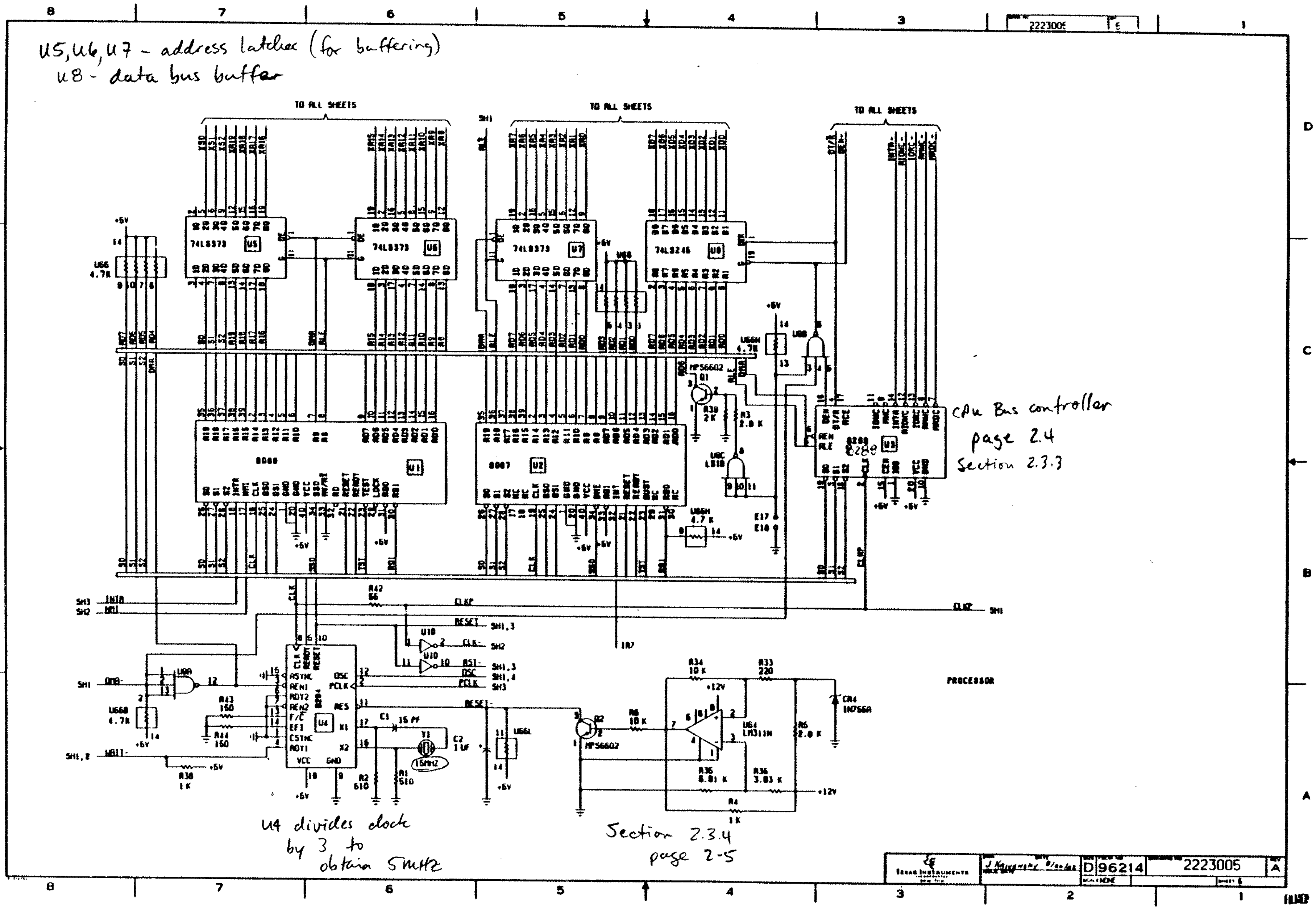


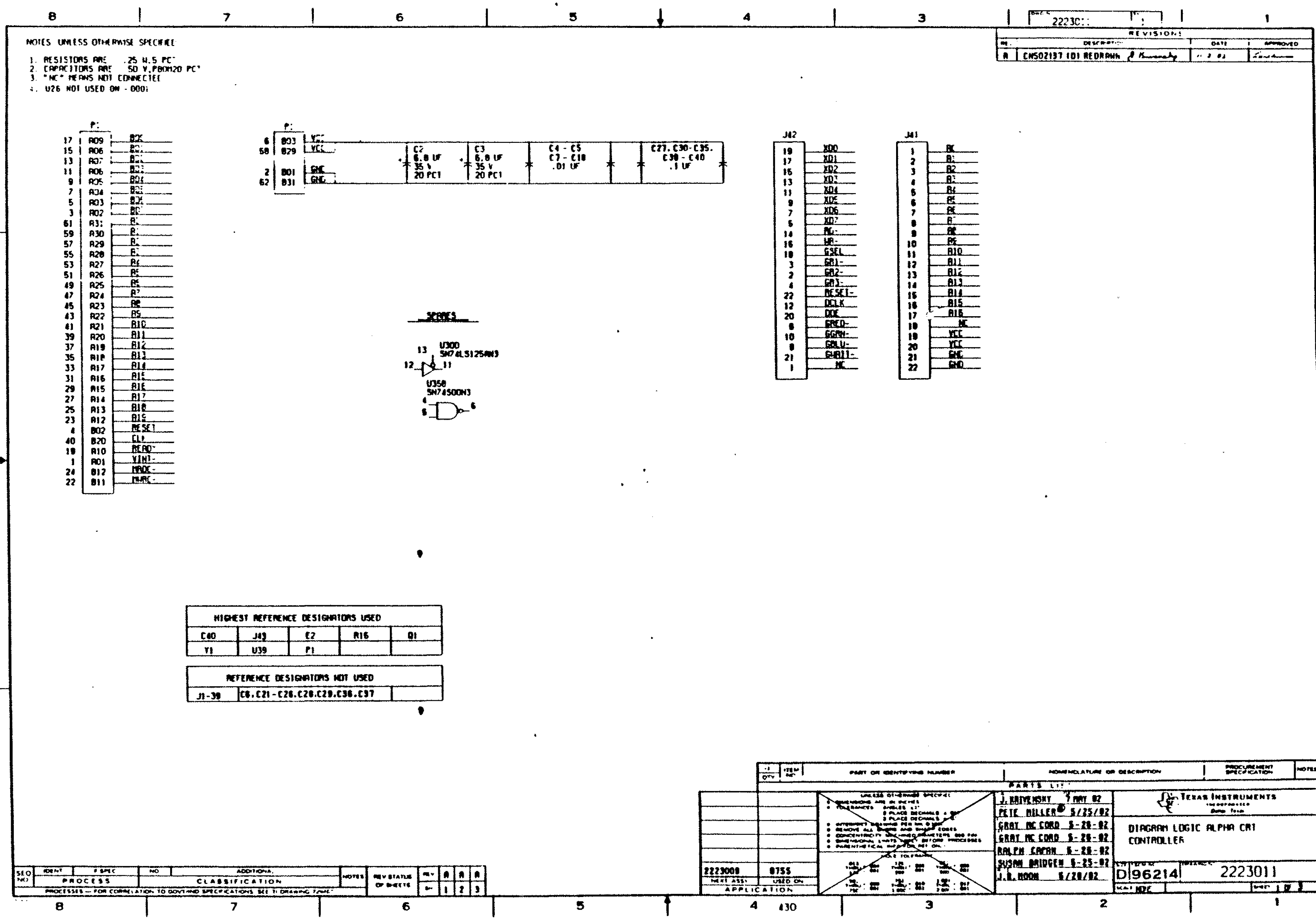


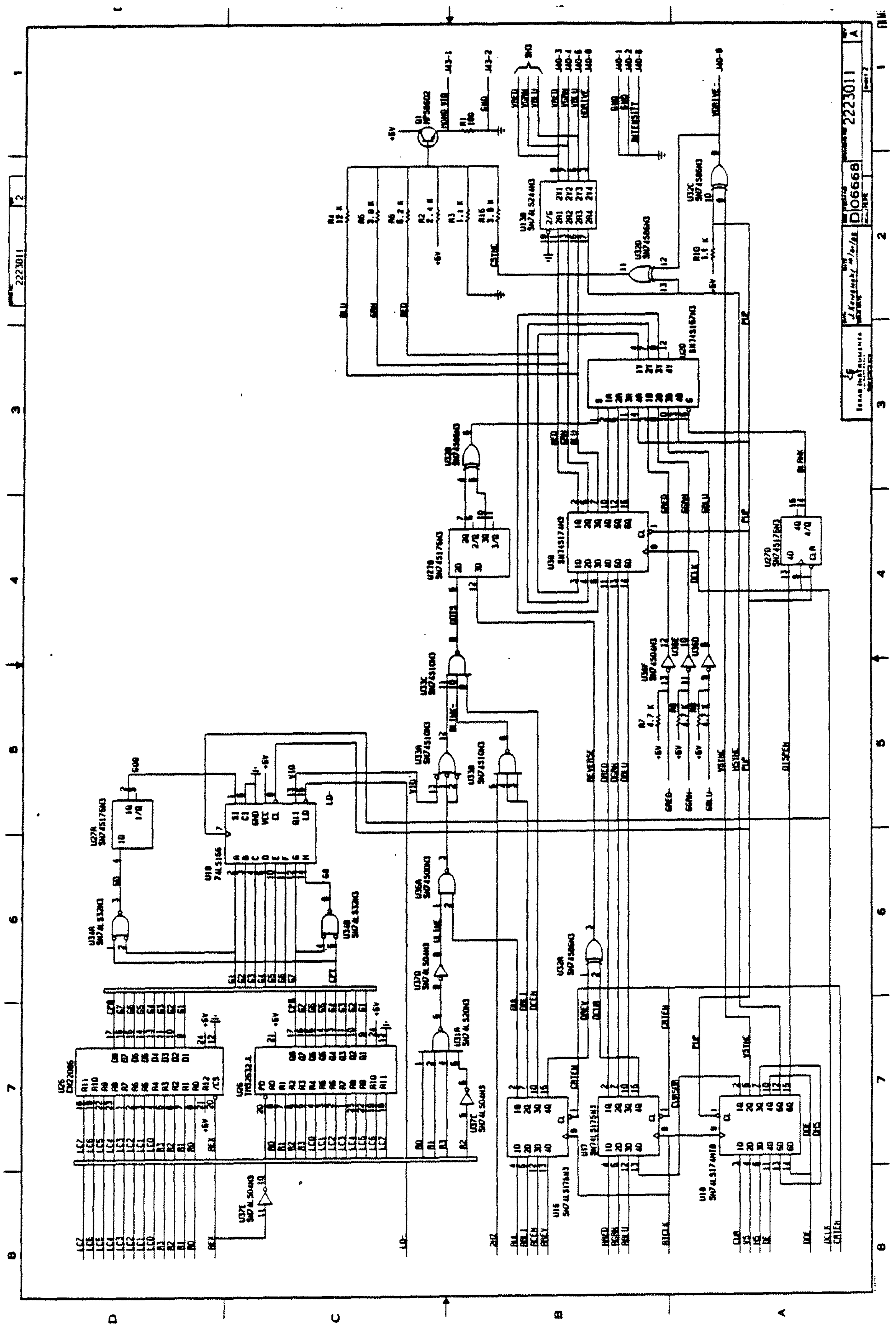
U53A - U55 I/O Decoders page 2-10
U47-U51 page 2-6
pg. 2-11 Sec. 2.4.2.
page 2.5 for description
TABLE 2-1 pgs 2-6, 2-7
U46 - Interrupt controller chip
parity error occurred
8 Ω output
U44-U46 page 2-7
pg 2-13 Sec. 2.4.3
MOTHERBOARD I/O SYSTEM
PARALLEL PRINTER PORT
OPTION JUMPERS
SPEAKER CONNECTOR
AMP INPUT
KEYBOARD CONNECTOR
2223005
D96214

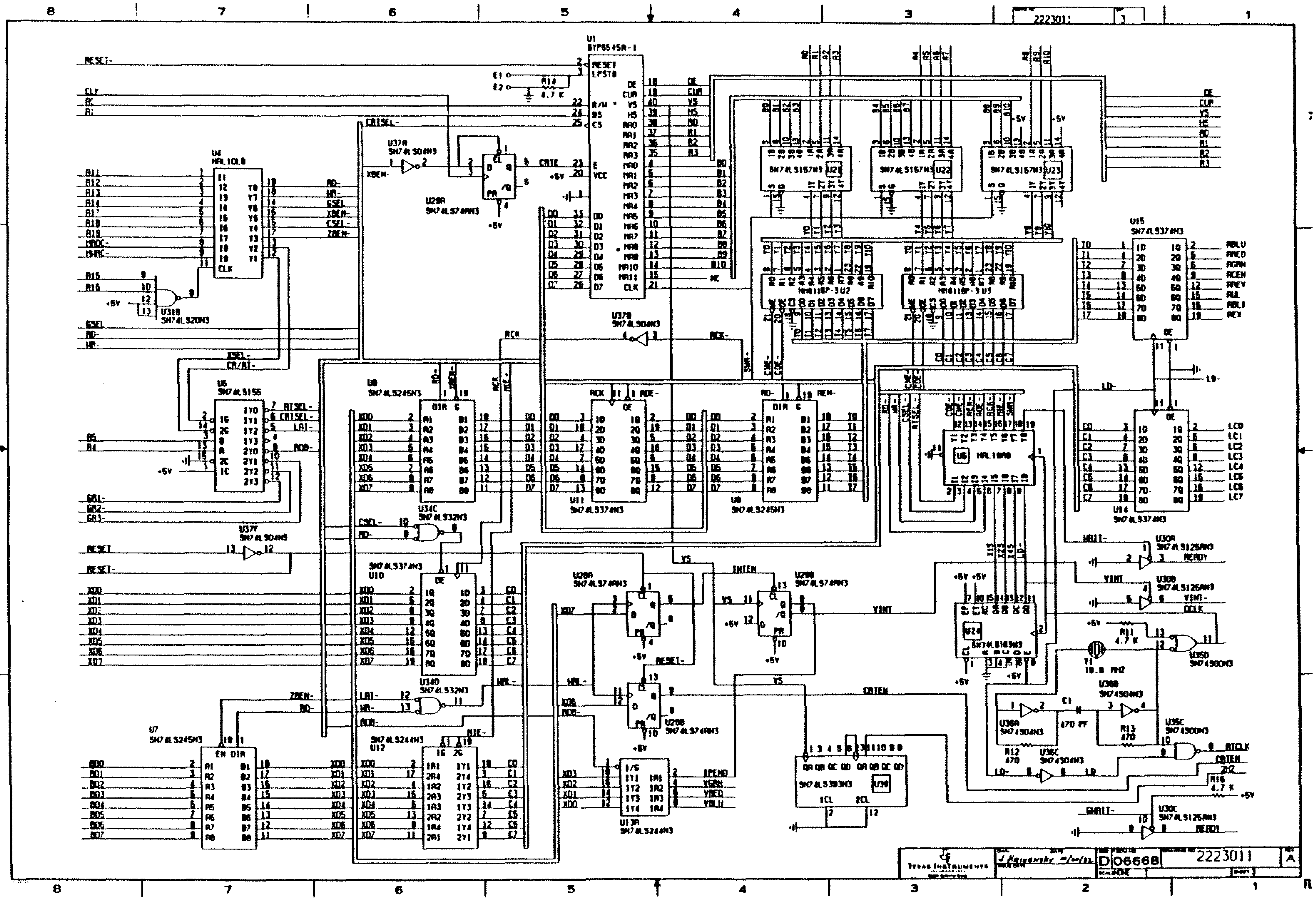


U12 SN74LS245
CD4040 U11
2114 U17
2114 U18
WD1793-02 U13
WD1691 U14
U15 WD2143-01
U25 SN74LS244
U23C SN7416N
74LS221 U29B
74LS620 U16
78L05 U22
PAL10L8-FLOPPY/A U19
74LS74 U21B
74LS163 U20
U26A SN7407N3
Addresses Buffer
Sector Buffer
PEGASUS FLOPPY DISK INTERFACE
Section 2.8
beginning on page 2.33
TEXAS INSTRUMENTS
D 96214
2223005
A


U5,U6,U7 - address latches (for buffering)
U8 - data bus buffer
TO ALL SHEETS
74LS373
74LS245
8088
8087
8288
CPU Bus controller
page 2.4
Section 2.3.3
8284
U4 divides clock by 3 to obtain 5MHZ
15MHZ
LM311N
MPS6602
Section 2.3.4
page 2-5
PROCESSOR
TEXAS INSTRUMENTS
D 96214
2223005
A

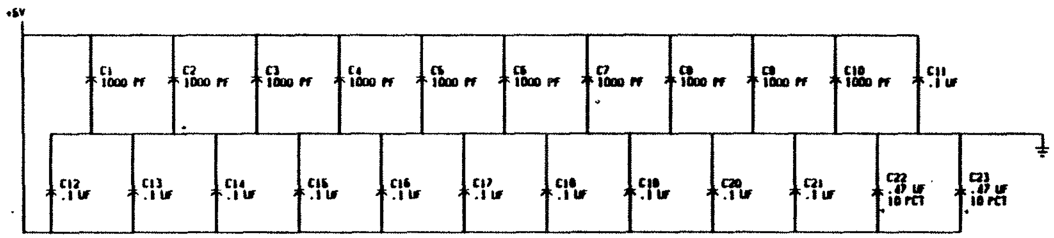

NOTES UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE .25 W,5 PCT
2. CAPACITORS ARE 50 V,P80M20 PCT
3. "NC" MEANS NOT CONNECTED
4. U26 NOT USED ON -0001
REVISIONS
A CN502137 (D) REDRAWN
SPARES
U300 SN74LS125AN3
U358 SN74S00N3
C2 6.8 UF 35 V 20 PCT
C3 6.8 UF 35 V 20 PCT
C4 - C5 C7 - C18 .01 UF
C27, C30-C35, C39 - C40 .1 UF
J42
J41
HIGHEST REFERENCE DESIGNATORS USED
C40 J43 E2 R16 Q1
Y1 U39 P1
REFERENCE DESIGNATORS NOT USED
J1-39 C6,C21-C26,C28,C29,C36,C37
J. KRIVENSKY 7 MAY 82
PETE MILLER 5/25/82
GARY MC CORD 5-26-82
GARY MC CORD 5-26-82
RALPH CAPAN 5-26-82
SUSAN BRIDGEN 5-25-82
J.R. MOON 5/28/82
TEXAS INSTRUMENTS
DIAGRAM LOGIC ALPHA CRT CONTROLLER
D 96214 2223011
2229000 0755
NEXT ASSY USED ON
APPLICATION
430


2223011
D06668
Texas Instruments


2223011
SYP6545A-1
HAL10L8
SN74LS155
SN74LS245N3
SN74LS374N3
SN74LS244N3
SN74LS167N3
MM6116P-3
SN74LS393N3
Texas Instruments
D 06668
2223011
A

NOTES UNLESS OTHERWISE SPECIFIED

1. CAPACITORS ARE ,60 V,P80M20 PCT



PARTS LIST

TEXAS INSTRUMENTS

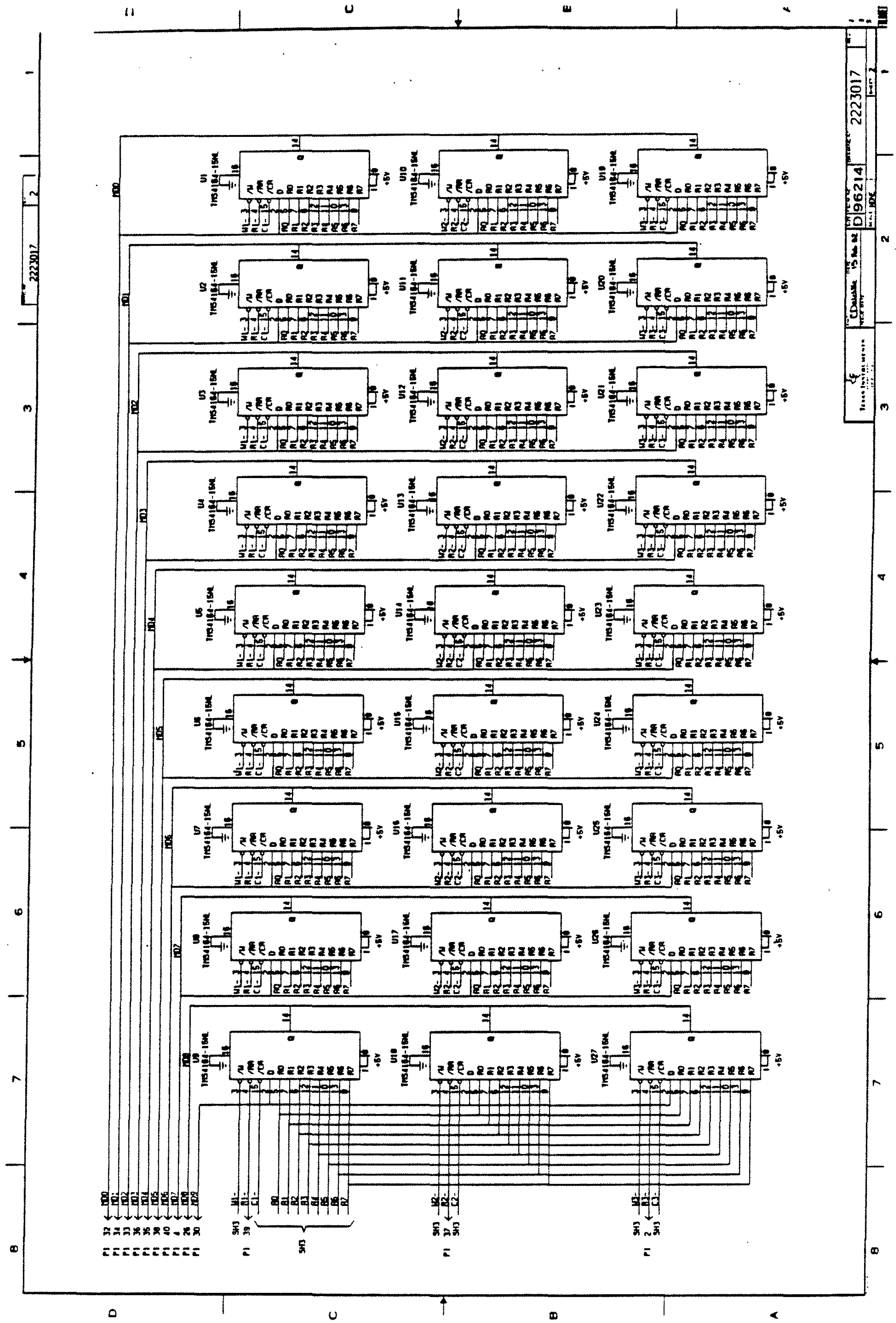
DIAGRAM, LOGIC, DETAILED-RAM EXPANSION

D 96214 2223017

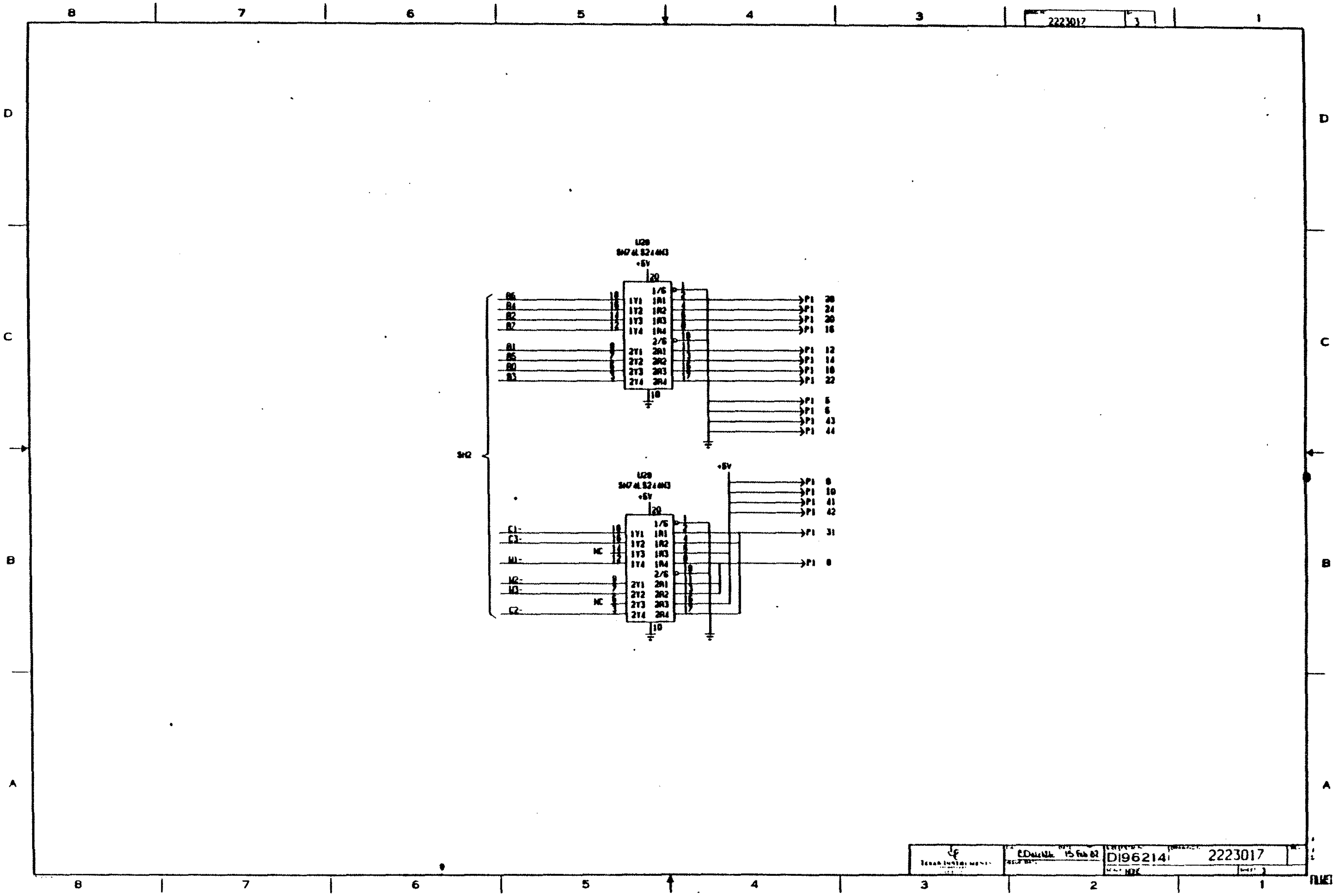
SCALE NONE SHEET 1 OF 3

2223016 NEXT ASSY | 0756 USED ON

APPLICATION



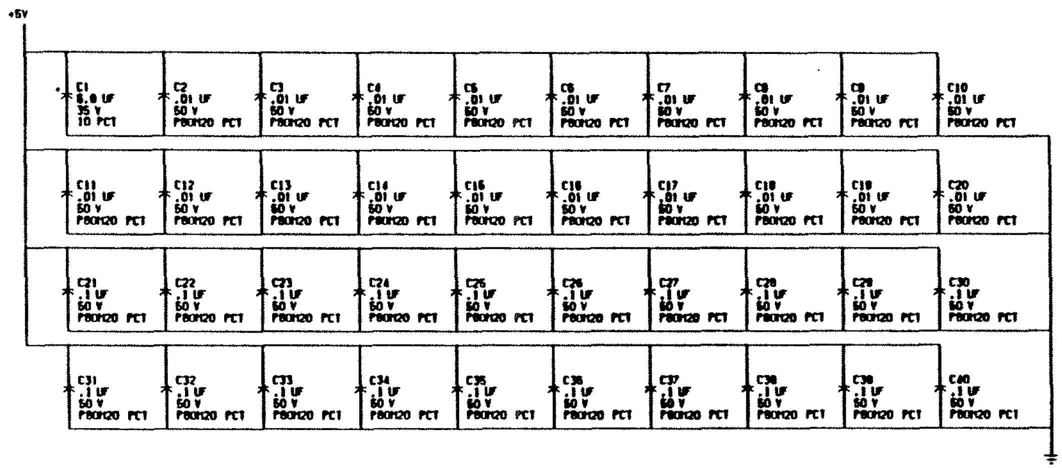
2223017
D96214


2223017
+5V
SH2
DI96214
2223017

NOTES UNLESS OTHERWISE SPECIFIED

[1] U5 THRU U12 USED ON -0002 ONLY

REV	DESCRIPTION	DATE	APPROVED
A	CN500643(D) CDalchke 21 Oct 82	11-8-82	



HIGHEST REFERENCE DESIGNATORS USED				
P2	U46	C40	R5	E4

REFERENCE DESIGNATORS NOT USED				

PARTS LIST

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

NEXT ASSY	USED ON
2223081	9795

APPLICATION

CDalchke 21 Oct 82
Rick Miller 5 May 82
Greg McCord 5 May 82
Greg McCord 5 May 82
Ralph Cason 5 May 82
Susan Bridges 5 May 82
Jim Moon 5 May 82

TEXAS INSTRUMENTS

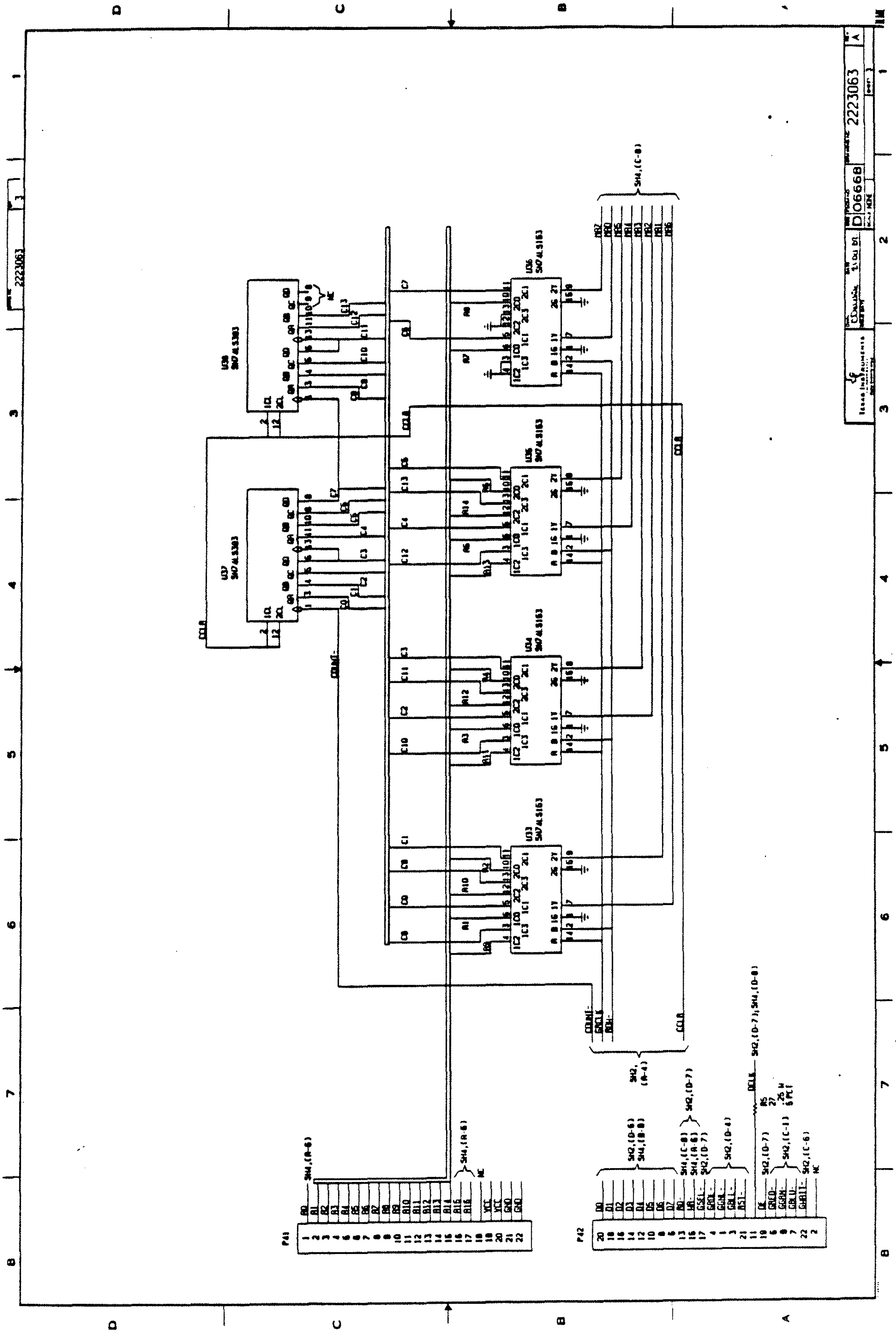
DIAGRAM, LOGIC
GRAPHICS

D196214 2223063

SHEET 1 OF 4

REV STATUS OF SHEETS: A A A A — 1 2 3 4

430 (H-MT)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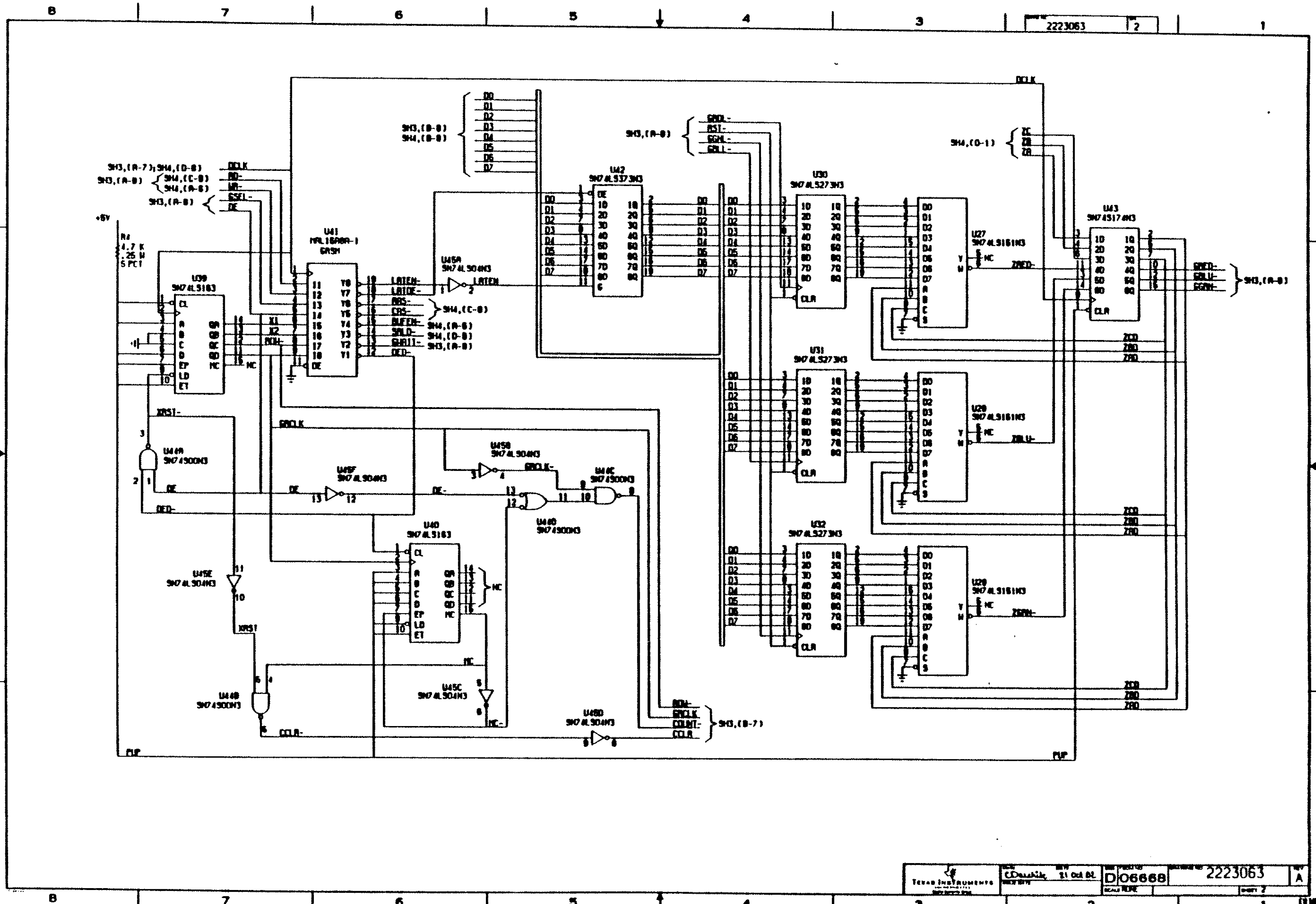
U36 SN74LS163
U37 SN74LS283
U38 SN74LS283
P41
P42
2223063
D06668


2223063
U41
MAL16R8A-1
U42
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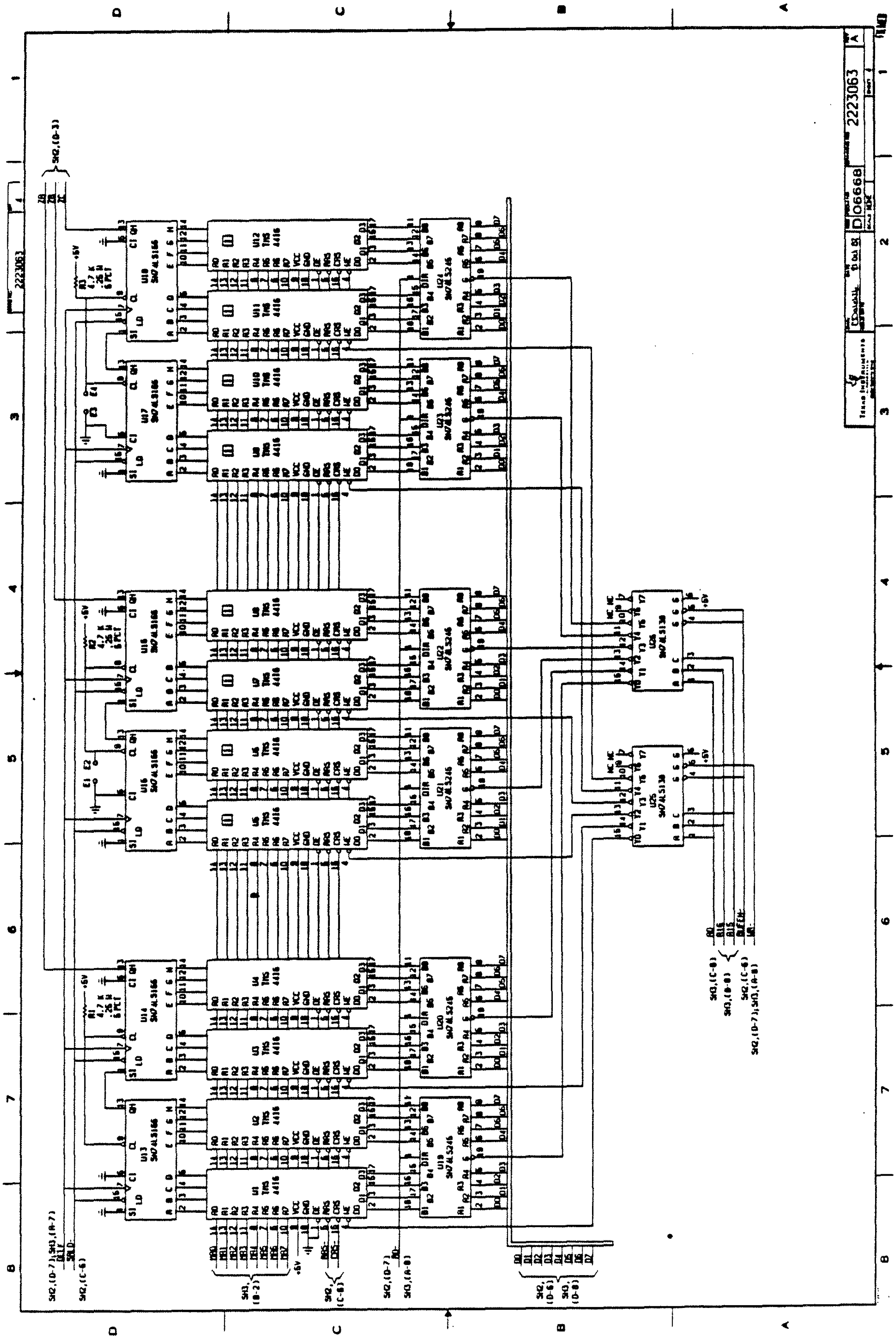
U30
SN74LS273N3
U31
SN74LS273N3
U32
SN74LS273N3
U27
SN74LS151N3
U43
SN74S174N3
U39
SN74LS163
U40
SN74LS163
U44A
SN74S00N3
U44B
SN74S00N3
U44C
SN74S00N3
U45A
SN74LS04N3
U45B
SN74LS04N3
U45C
SN74LS04N3
U45D
SN74LS04N3
U45E
SN74LS04N3
U45F
SN74LS04N3
DCLK
LATEN-
LATOE-
RAS-
CAS-
BUFEN-
SHLD-
SHIFT-
OED-
XRST-
XRST
GRCLK
CCLR-
COUNT-
REDL-
RST-
GGHL-
GBLL-
GRED-
GBLU-
GGRN-
+5V
4.7 K
.25 W
5 PCT
PUP
TEXAS INSTRUMENTS
D 06668
2223063
A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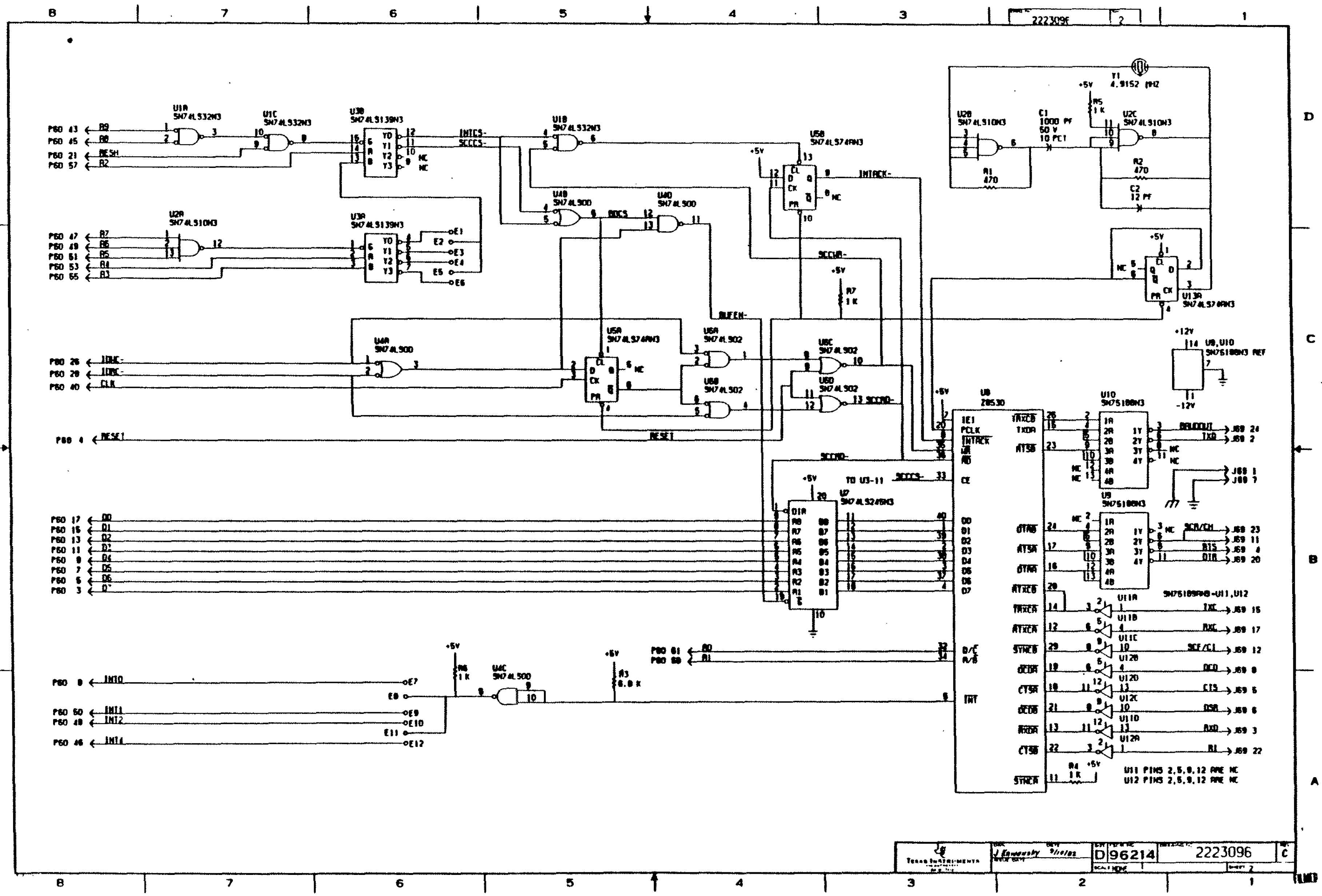
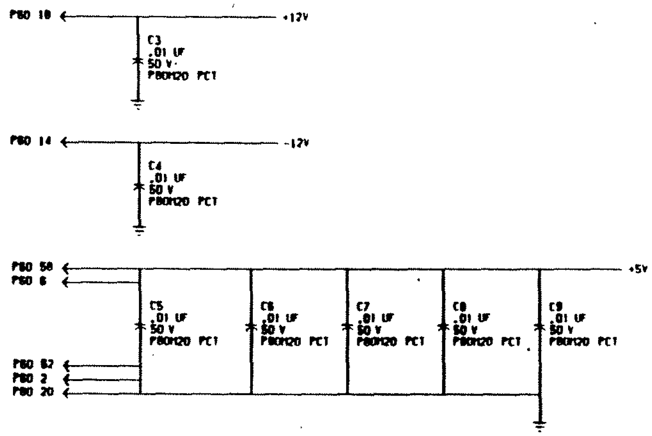
D06668
Texas Instruments
SN74LS166
TMS 4416
SN74LS245
SN74LS138


2223096 2
Y1 4.9152 MHZ
U1A SN74LS32N3
U1C SN74LS32N3
U3B SN74LS139N3
U1B SN74LS32N3
U5B SN74LS74AN3
U2B SN74LS10N3
C1 1000 PF 50 V 10 PCT
U2C SN74LS10N3
R1 470
R2 470
C2 12 PF
U2A SN74LS10N3
U3A SN74LS139N3
U4B SN74LS00
U4D SN74LS00
U13A SN74LS74AN3
U4A SN74LS00
U5A SN74LS74AN3
U6A SN74LS02
U6B SN74LS02
U6C SN74LS02
U6D SN74LS02
U9,U10 SN75188N3 REF
U8 Z8530
U10 SN75188N3
U9 SN75188N3
U7 SN74LS245N3
U4C SN74LS00
SN75189AN3-U11,U12
INTCS-
SCCCS-
INTACK-
SCCWR-
BUFEN-
SCCRD-
RESET
TO U3-11
U11 PINS 2,5,9,12 ARE NC
U12 PINS 2,5,9,12 ARE NC
TEXAS INSTRUMENTS
D 96214
2223096
C

NOTES UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS

REV	DESCRIPTION	DATE	APPROVED
A	CN476727 (E)		
B	CN500549 (D)		
C	CN501644 (E)		



HIGHEST REFERENCE DESIGNATORS USED				
C9	E12	U19	J69	R7
P80	T1			

REFERENCE DESIGNATORS NOT USED				
J1-88	P1-88			

PARTS LIST

J. KRIVENSKY 06 APR 82

TEXAS INSTRUMENTS

DIAGRAM, LOGIC, DETAILED-COMMUNICATION, SYNC/ASYNC

D 96214 2223096

2223094 0755

NEXT ASSY USED ON

APPLICATION

H-MT

SHEET 1 OF 2

2223096

GLOSSARY

abort -- To end a program and return control to the operating system, usually when a mistake or malfunction occurs.

acknowledge character (ACK) -- A transmission control character sent by a receiver as an affirmative response to a sender.

address -- A number that represents a register, a memory location, or some other data source or destination.

analog -- An object (or variable) that is represented by a physical quantity, such as a continuously varying voltage. The physical quantity that represents the variable behaves as some function of the variable. (Contrast with digital).

AND -- A binary function which is "on" if and only if all of its inputs are "on".

arithmetic and logic unit -- The part of a computer that does arithmetic, logic, and similar operations.

array -- An arrangement of elements (such as numbers) usually related in some fashion.

ASCII -- (American Standard Code for Information Interchange), an eight-level (7 bits + parity) code consisting of control and graphic characters.

asynchronous transmission-- Transmission in which information characters arrive at irregular intervals of time (usually bracketed by start elements and stop elements). (Contrast with synchronous transmission).

audio frequencies -- Frequencies which can be heard by the human ear (usually between 15 cycles and 20 000 cycles per second).

auto-call -- A feature that allows a terminal to initiate a call automatically over a switched (telephone) line.

backup copy -- A copy of a file that is kept for reference in case the original file is destroyed.

BASIC (Beginner's All-Purpose Symbolic Instruction Code) -- a higher-level language, similar in structure to FORTRAN but somewhat easier to learn because of a smaller command repetoire and simpler syntax. BASIC was invented at Dartmouth College in 1963 and is probably the most popular language for personal computers.

batch processing -- a technique of data processing in which jobs are collected and grouped before processing. Data thus are normally processed in a deferred mode.

baud, baud rate -- a measure of data transfer rate, equal to the number of discrete conditions or signal events per second. (See bits per second).

binary digit (bit) -- the smallest unit of information in the binary system of notation.

bit -- the abbreviation for binary digit. In the binary notation, a bit is either of the characters 0 or 1.

bit transfer rate __ the number of bits transferred per unit time, usually expressed in bits per second (bps).

bootstrap (to "boot") -- to get a system running from a coldstart in a manner like "pulling oneself off the ground by tugging on ones bootstraps".

branch -- in programming, to make a selection from among alternative choices of instructions.

break -- a long space on an asynchronous communications line that is intended to alert the receiving CPU. Minimum duration is one character time.

buffer -- a device or area of memory which is used to hold something temporarily. For example, the screen buffer contains graphic information to be displayed on the video screen.

buffering -- (Disk Control) Storing data between transfer operations. Data read from disk is buffered before transfer to system memory and data to be written is buffered after transfer from system memory.

byte -- a binary element string of 8 bits, usually operated upon as a unit.

carrier -- a continuous frequency capable of being modulated or impressed with a signal.

CCITT -- (Comite Consultatif Internationale de Telegraphie et Telephonie), an international consultative committee which sets communications standards. The CCITT V24 interface standard is similar to the EIA RS-232-C standard.

COBOL -- (COmmon Business-Oriented Language)- a programming language designed for business data applications

code -- a system of symbols (bits) for representing data (characters).

compile -- to translate a computer program expressed in a human-oriented language into a computer-oriented language.

control character -- (1) A charcter whose occurrence in a particular context controls the handling of data. (2) In the ASCII code, any of the 32 characters in the first two columns of the standard code table.

CPS -- characters per second.

CPU (Central Processing Unit) -- unit of a computer that includes circuits controlling the interpretation and execution of instructions.

crosstalk -- the undesired transfer of energy from one circuit to another.

cursor -- a movable spot of light on the screen of a display device, usually indicating where the next character will be entered.

cyclic redundancy check (CRC) -- a method of error detection which matches CRC characters generated by transmitting and receiving devices based on the content of the message at that location.
(Disk Control) - Comparison of the checksum derived from data as it was originally written into disk storage with the checksum derived from the same data as it is being read out of storage. The first checksum is appended to the data as it is written to the disk. After reading this data, the controller computes a new checksum from it and compares the two. If the checksums match, the data is correct. A checksum error may indicate a damaged area on the disk, data that has changed since it was written, or erroneous reading of correct data where a retry may work.

cylinder -- in a disk pack, the set of all tracks with the same nominal distance from the axis about which the disk pack rotates. These tracks can be accessed without repositioning the access mechanism.

data -- a general term for any type of information.

data communications -- the movement of computer-encoded information by means of communications transmission systems.

debug -- to find and delete mistakes in computer programs or in other software.

default value -- the value chosen automatically by the computer when no explicit choice is made by the user.

delimiter -- a character that separates and organizes elements of data.

diagnostic -- pertaining to the detection of a malfunction.

digital -- the representation of numerical quantities by means of discrete integer numbers. It is possible to express in digital form all information stored, transferred or processed by a dual-state condition; e.g., ON/OFF, OPEN/CLOSED, or TRUE/FALSE. (Contrast with analog).

direct memory access (DMA) -- direct data transfer between an I/O peripheral and memory, without computer intervention. (Disk Control) - The technique generally used to transfer blocks of data between a peripheral and random-access memory. It is called direct because the host does not handle the data during the transfer operation.

directory -- a logically organized data structure which holds pointers to access data sets by sequential number or name.

display -- a visual presentation of information.

double-precision -- using two computer words instead of one to represent a number.

downtime -- the time interval during which a computer is inoperable due to a fault.

EIA (Electronic Industries Association) -- The EIA Standard RS-232-C defines interconnection interfaces for terminals.

emulate -- to imitate one system with another such that the imitating system accepts the same data and achieves the same results as the imitated system.

EOF(end-of-file mark) -- a code which signifies that the last record of a file has been read.

equalization -- compensation for the loss of signal in a line.

FCC -- Federal Communications Commission -- a board of commissioners having the power to regulate all interstate and foreign electrical communication systems originating in the United States.

field -- an area in a record (see record) treated as a unit.

FIFO -- First-In First-Out memory buffer.

file -- a group of related records handled as a unit.

firmware -- memory chips with software programs already built in.

flag -- a character that signals the occurrence of some condition, such as the end of a word.

foreground processing -- high-priority processing, usually resulting from real-time entries, given precedence by means of interrupts, over lower priority "background" processing.

formatting: (Disk Control) The division of tracks into sectors to make it easier to retrieve and update data. In each sector, the block of data is preceded by an identifying header. Gaps are inserted between sectors and between the header and data blocks within each sector to allow time for control logic functions and speed fluctuations in the disk drive assembly.

FSK(frequency-shift keying) -- a means of transmitting data in which a "1" is represented as one frequency and a "0" as another frequency.

G -- giga; when referring to computer memory it represents 1 073 741 824. Otherwise it is 1,000,000,000.

global -- in programming, it is something that is defined in one section of a program and used in at least one other section.

graphics -- symbols normally produced by handwriting, drawing, or printing. Synonymous with graphic symbol.

graphic character -- a character, other than a control character, that is normally represented by a graphic.

half duplex channel -- a communications line capable of transmitting in both directions, but not at the same time.

hardware -- physical equipment, as opposed to a computer program or method of use, e.g., mechanical, electrical, magnetic, or electronic devices.

hertz -- a unit of frequency equal to one cycle per second. Abbreviated Hz.

hexadecimal -- pertaining to a selection, choice, or condition that has sixteen possible values or states. These values or states usually contain 10 digits and 6 letters A through F. Hexadecimal digits are equivalent to a power of 16.

host computer (Also just "host") -- the primary or controlling computer to which the terminal is connected by cable for communications.

identification characters -- characters sent by a station on a switched line to identify the station.

input/output (I/O) -- something that can be in an input or output process, either simultaneously or seperately.

instruction -- in a programming language, a meaningful expression that tells the computer to execute a specific task.

instruction set -- the set of the instruction of a computer or language.

integrated circuit -- a combination of interconnected circuit elements inseperably associated on or within a continuous substrate.

integrated modem -- a modem that is an integral part of the device with which it operates.

intelligent terminal -- a synonym for a terminal that is programmable and can do some processing operations.

interface -- interconnection between two pieces of equipment having different functions.

interpreter -- a computer program that interprets programming languages. Synonymous with interpretive program.

interrupt -- the temporary stopping of some phase of computer operation caused by an event external to the operation.

job -- a task submitted for a computer to do, it usually contains all necessary instructions, files, and data to complete the task.

joystick -- a stick that is hand-held by the user and usually is used to position something on the screen.

K -- an abbreviation for the prefix kilo, i.e., 1000 in decimal notation. In storage capacity, K frequently means two to the tenth power which is 1024 in decimal notation.

Kb -- Kilobyte.

KHz -- Kilohertz. a unit of frequency equal to 1000 hertz.

LED (Light Emitting Diode) -- a small solid-state device which emits light when a current is applied.

library -- a group of related files.

light pen -- in computer graphics, a pen-like device that can sense light. When it is held up to a CRT it can be used to identify display elements.

line, communications -- describes cables, telephone lines, etc., over which data is transmitted to, and received from, the terminal. Also referred to as the "line").

list -- to print or display data.

listing -- a printout, usually of a program.

load -- to enter data into memory or into registers.

machine language -- a language that is used as is by a machine.

magnetic disk -- a flat circular plate with a magnetizable surface layer on which data can be stored by magnetic recording. The disk may be rigid or flexible.

mass storage -- storage having a very large storage capacity.

message -- in data communications, an amount of information that contains a predefined beginning and end.

modem -- (contraction of modulator/demodulator). a device which modulates and demodulates signals transmitted over communicationbs facilities. The modulator is included for transmission and the demodulator for reception. A modem is used to permit digital signals to be sent over analog lines. Also called a data set.

modulation -- the process by which some characteristic of one wave is varied in accordance with another wave or signal. This technique is used in modems to make computer signals compatible with communications facilities.

mnemonic -- symbol or symbols used instead of terminology more difficult to remember. Usually a mnemonic has two or three letters.

multiplexing -- using a transmission line to carry several different signals at one time.

NAND -- a logic operator. The NAND of any two statements P and Q is false if and only if both P and Q are true.

nanosecond -- one-thousand-millionth of a second.

noise -- undesirable disturbances in a communications system. Noise can generate errors in transmission.

non-impact printers -- a printer in which printing is not the result of mechanical impacts; e.g. thermal printers.

object code -- output from a compiler or assembler which is itself executable machine code or is suitable for processing to produce executable machine code.

offline (local) -- describes the state when equipment or devices are not connected to the communications line.

online -- describes the state when equipment or devices are connected to the communications lines under control of a processor either directly or through a communication system. The physical connection can be accomplished by either multiwire cable or a communications line.

open -- to prepare a file for processing, e.g. editing.

operating system -- software that controls the execution of computer programs and that may provide scheduling, debugging, input and output control, accounting, storage assignment, data management, and related service. Sometimes called Supervisor, Executive, Monitor, Master Control Program depending on the computer manufacturer.

parallel transmission -- method of data transfer in which all bits of a character or byte are transmitted simultaneously either over separate communications lines or on different carrier frequencies on the same communication line.

parameter -- a variable that is given a constant value for a specific purpose or process.

parity check -- addition of non-information bits to data, making the number of ones in each grouping of bits either always odd for odd parity or always even for even parity. A transmission error can then be detected by checking each group of bits received for correct parity.

password -- a word or string of characters that is recognizable by automatic means and that permits a user access to protected storage, files, or input or output devices.

program -- a series of instructions written to solve a problem. Also, to design, write, and test computer programs.

protocol -- a formal set of conventions or rules governing the format, timing, and error control to facilitate message exchange between two communicating processes.

protected field -- a field into which the operator cannot enter data.

queue -- a line formed by items in a system waiting to be processed.

RAM -- random-access memory.

read -- to get data from a storage device.

record -- a collection of fields; the information relating to one area of activity in a data processing activity, e.g., all information on one inventory item. Sometimes called item.

relational character -- a character that expresses a relationship between two operands. Common relational operators are > (greater than), < (less than), and = (equal to).

retry -- (Disk Control) Repetition of search or read/write operations to recover from "soft" (correctable) errors.

ROM -- Read-only memory.

run -- to process a task, e.g. a program, through a computer.

scratch file -- a file where temporary calculations and work is done.

scrolling -- the continuous vertical or horizontal movement of data across the screen face.

search -- (Disk Control) Reading headers on the track passing under a read/write head so as to locate the desired sector. The controller compares each identification (ID) read from the track with the ID of the desired sector.

sector -- part of a track or band on a magnetic disk.

seek -- (Disk Control) Moving a set of read/write heads so that one of them is over the desired track.

serial transmission -- a method of transmission in which each bit of information is sent sequentially on a single channel rather than simultaneously as in parallel transmission.

simplex circuit -- synonym for one-way circuit.

slave station -- a data station that is under the control of a master station.

software -- a set of computer programs, procedures, rules and associated documentation concerned with the operation of network computers, e.g., compilers, monitors, editors, utility programs. (Compare. hardware).

space -- usually equivalent to a binary zero condition.

switched network -- a communications system where the physical path of the messages may be different with each use, such as the public telephone network.

synchronous transmission -- transmission in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized.

syntax -- the format, or rules, in which instructions must be presented to the data processing equipment.

terminal -- a device or computer which may be connected to a local or remote host system, and for which the host system provides computational and data access services.

text -- a sequence of characters forming part of a transmission which is sent from the data source to the data sink, and contains the information to be conveyed.

track -- that portion of a moving data medium which is accessible to a given reading head position.

trap -- a jump to a specific location caused by a hardware condition.

turnaround time -- in communications the time required for a device to switch from receiving to sending on a two-way alternate circuit. Time is required by line propogation effects, modem timing and computer reaction.

TWX -- teletypewriter exchange service.

video -- computer data shown or displayed on a cathode ray tube monitor or display.

write -- to record data on some storage device.

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