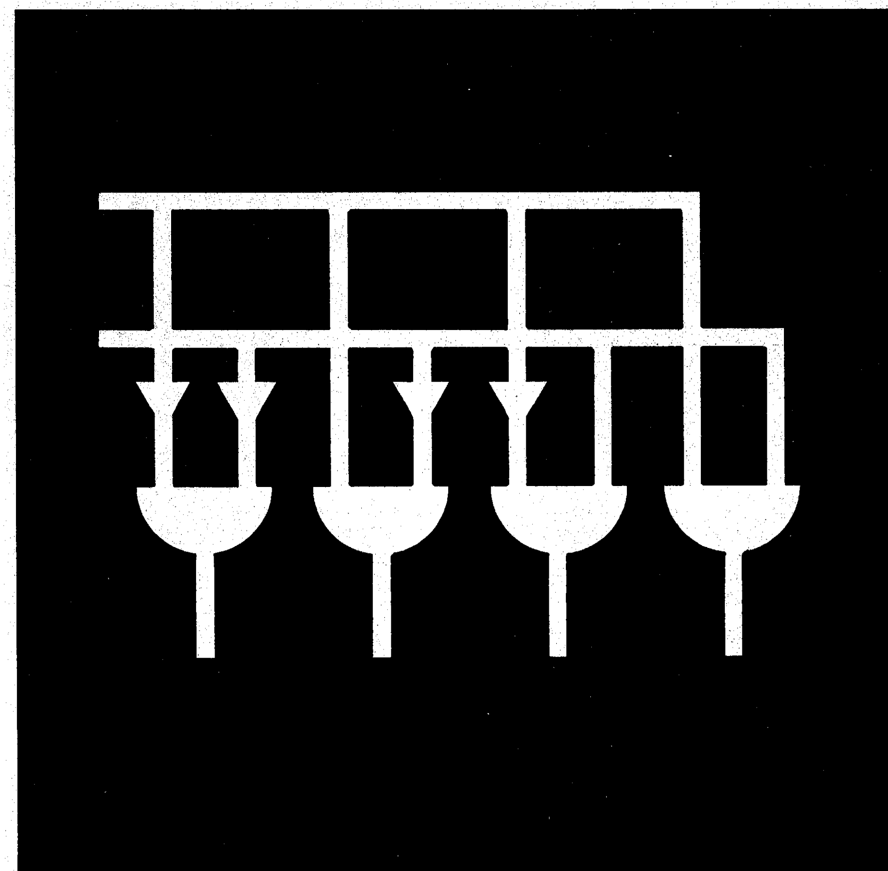
AN/UYK-1

A "STORED LOGIC" MULTIPLE PURPOSE COMPUTER



COMPUTER SIMULATION

APPLICATION STUDY

Thompson Ramo Wooldridge Inc.

TRW-130 (AN/UYK-1)

DATA PROCESSING SYSTEM

COMPUTER SIMULATION

APPLICATION STUDY

Thompson Ramo Wooldridge Inc.

RW *DIVISION*

8433 FALLBROOK AVENUE • CANOGA PARK, CALIFORNIA • DIAMOND 6-6000

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CONTENTS

1. INTRODUCTION

This Application Study serves to illustrate the use of a TRW-130 (AN/UYK-1) as a "host" machine in a computer simulation process. The Stored Logic properties of the TRW-130 enable it to perform computer simulation with greater efficiency than a conventional computer in the same price class because of the following factors:

1. The TRW-130 is more adept at performing multi-precision arithmetic.

2. The TRW-130 can perform "operand chaining", i.e., the accessing of successive pieces of an operand, more efficiently.

3. The TRW-130 can carry out its processing with a greater degree of "parallelism."

As a measure of the TRW-130's effectiveness as a simulator, we have used the <u>simulation ratio</u> S, defined as

$$S = \frac{\text{program running time on simulated computer}}{\text{program running time on TRW-130 under simulation}}$$

By this means we are able to evaluate the comparative effectiveness with which the TRW-130 simulates different computers.

For purposes of illustration, we have selected the Royal McBee LGP-30 and the Bendix G-15 as computers to be simulated on the TRW-130. Both of these computers have magnetic drum memories, so that the time they take to execute a program will depend on the extent to which the programmer has achieved "minimum latency" in his coding. The three main results of our analysis are:

1. For LGP-30 programs that have been randomly coded (i.e., in which no attempt has been made to obtain minimum latency), the simulation ratio (S) is about 24. This means that such programs will run 24 times as fast on the TRW-130 as on the LGP-30 itself.

2. For LGP-30 programs in which 50% of latency* has been removed through minimum latency coding, the simulation ratio (S) is about 12.

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*Our experience indicates that 50% is about all the latency that can be removed in practical situations from a drum computer program; hence the use of this figure here.

3. For G-15 programs, the corresponding figures are:

Random coding:	S = 14
50% latency removed:	S = 7

Thus, in the cases considered, the TRW-130 simulates programs faster than they would run on the machine they were written for. This clearly demonstrates the practicality of using the TRW-130 to simulate other computers.

In Section 2 of this note, a brief description is given of a TRW-130 program that simulates the LGP-30. In Section 3, a formula is developed for estimating the simulation ratio for any general-purpose computer being simulated on the TRW-130. Finally, in Section 4, this formula is applied to the LGP-30 and the G-15, to obtain the results quoted above.

2. SIMULATION OF THE LGP-30 ON THE TRW-130

The LGP-30 simulator consists of two sections:

1. a control section, and
2. an execution section.

The control section is entered once per simulated instruction. Its functions are to:

1. simulate the inter-instruction operations of the control flip-flop registers in the LGP-30;
2. identify the memory cells in the LGP-30 which will be affected by the instruction to be simulated next;
3. map addresses of these cells to their corresponding addresses in the TRW-130; and
4. branch to a routine which will directly simulate the next instruction.

The execution section of the simulator contains sixteen subsections. Each subsection performs a direct simulation of one particular LGP-30 instruction.

LGP-30 Simulated Memory Structure

The LGP-30 memory is structured in the TRW-130 as shown in Figure 1. Three TRW-130 words are used to hold one LGP-30 word.

TRW-130 Address	TRW-130 Word
K	LGP-30 Word 0: Bits 1 - 15
K + 1	: Bits 16 - 30
K + 2	: Bit 31
K + 3	LGP-30 Word 1: Bits 1 - 15
K + 4	: Bits 16 - 30
K + 5	: Bit 31
3C + K	LGP-30 Word C: Bits 1 - 15
3C + K + 1	: Bits 16 - 30
3C + K + 2	: Bit 31

Note: LGP-30 Bit 1 is most significant bit.

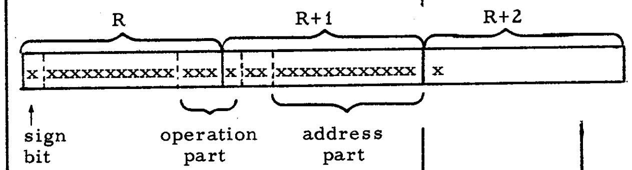
Figure 1. LGP-30 Simulated Memory Structure

Notation

General Notation

Symbol	Meaning
X	single-precision word
X, X+1	double-precision word
X, X+1, X+2	triple-precision word
$[X]_{m-n}$	bits m thru n of word X, where 1 = right-most bit
$\lvert X \rvert$	absolute value of X
$\longrightarrow$	replacement
x	multiplication
	logical product

Symbolic Notation

SYMBOL	MEANING	REMARKS	TYPE USAGE*	DATA JUSTIFICATION**
R, R+1, R+2	Simulated LGP-30 Instruction Being Executed			
A, A+1, A+2	Simulated LGP-30 Accumulator	32^{nd} bit is "spacer" bit	TS	32 bits, LJ
C	Simulated LGP-30 Counter Register	Contains LGP-30 location of next LGP-30 instruction to be executed.	TS	12 bits, RJ
OP	"Operation Part" of LGP-30 instruction being simulated	OP = $[R]_{1-3}, [R+1]_{15}$	TS	4 bits, RJ
AP	"Address Part" of LGP-30 instruction being simulated	AP = $[R+1]_{1-12}$	TS	12 bits, RJ
K	Memory Offset Constant	LGP-30 simulated cell C occupies TRW-130 locations 3C+K, 3C+K+1, 3C+K+2.	C	RJ
TC	Translated Counter Register	TC = 3C+K-1	TS	14 bits, RJ
TAP	"Translated Address Part" of LGP-30 instruction being simulated	TAP = 3AP+K	TS	14 bits, RJ
START	LGP-30 Program Start Address		IP	RJ
BP32	Breakpoint Switch 32		IP	RJ
BP16	Breakpoint Switch 16	0 = Breakpoint Switch UP	IP	RJ
BP8	Breakpoint Switch 8	1 = Breakpoint Switch DOWN	IP	RJ
BP4	Breakpoint Switch 4		IP	RJ
T	Table Offset Constant	T = TABLE	C	RJ
TABLE, TABLE +1,... TABLE +15	Multiple-Branch Table	This table contains 16 entries, each entry corresponding to an LGP-30 instruction; the i^{th} entry contains the address of the first logand of the routine which simulates the i^{th} LGP-30 instruction.	C	RJ

*Type Usage: TS = temporary storage; C = constant; IP = input parameter.

**Data Justification: LJ = left-justified; RJ = right-justified.

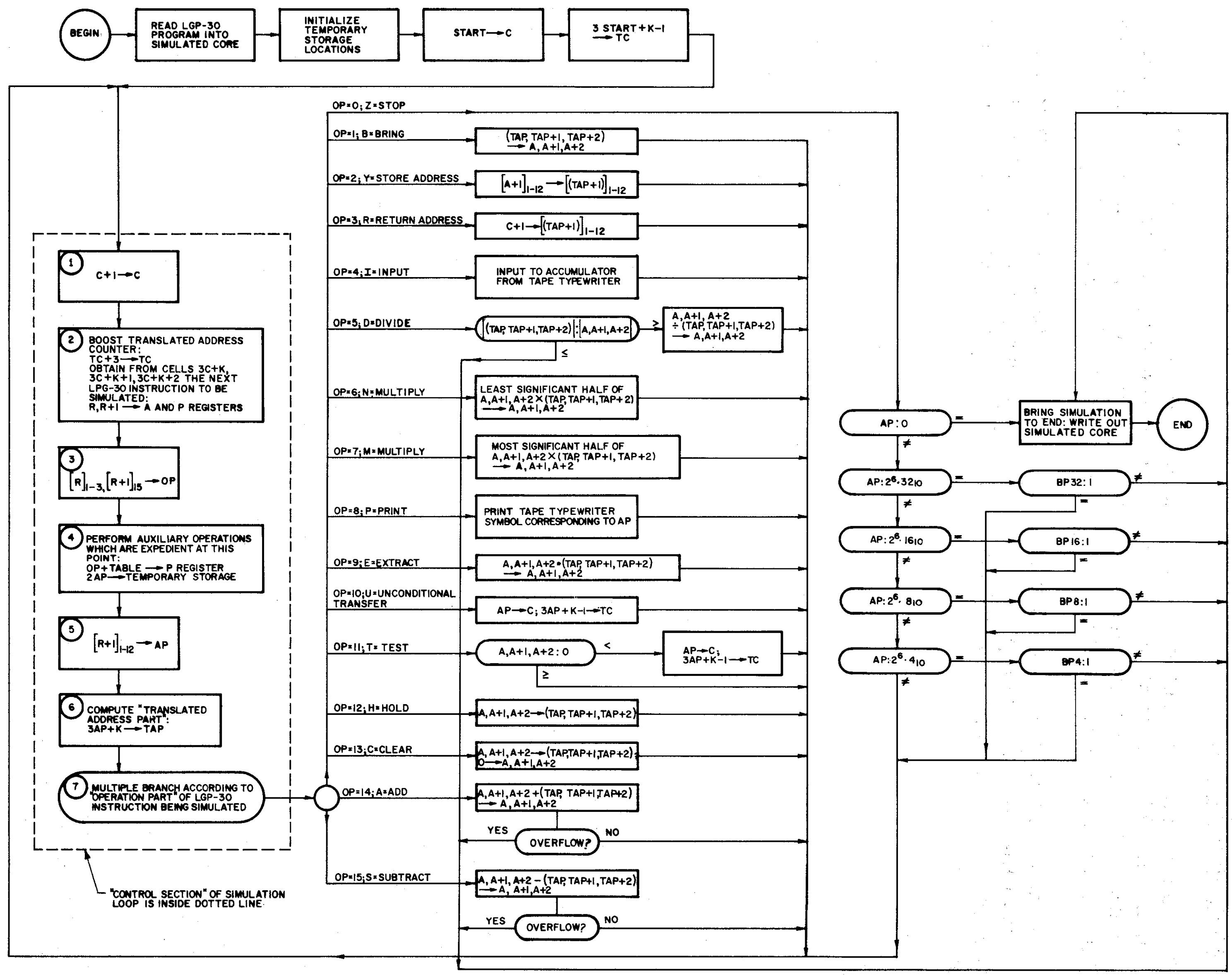


Figure 2. Flow Chart. Simulation of LPG-30 on TRW-130

Coding and Timing

The coding for the control section of the simulator is given in the Appendix. The control section requires a sequence of twenty-two words. Twenty of these contain logands; the other two contain imbedded constants. The processing time for the control section is 252 μs.

By writing TRW-130 subroutines corresponding to LGP-30 instructions, we find that the average processing time for the execution section is 120 μs. Therefore, the total simulation loop is processed in an average of 372 μs.

3. FORMULA FOR SPEED OF COMPUTER SIMULATION ON THE TRW-130

The speed with which a general purpose computer can be simulated on the TRW-130 can be expressed in terms of the various factors involved.

Let n = number of instructions available on simulated computer.

Let t_i = direct execution time (excluding latency) of i^{th} instruction on simulated computer, $i = 1, 2, \ldots, n$.

Let f_i = relative frequency of i^{th} instruction on simulated computer where

$$\sum_{i=1}^{n} f_i = 1$$

Note that f_i varies from program to program, and also from execution to execution of the same program.

Let ℓ = average latency time per instruction on simulated computer.

Note that ℓ is non-zero for drum computers and other types of serial-access computers; ℓ is zero for core computers.

Then, $t_i + \ell$ = average execution time for i^{th} instruction on simulated computer.

Let T_i = time to directly simulate on the TRW-130 the i^{th} instruction of simulated computer.

Now, define F as the overhead factor for a simulation program.

$$F = \frac{\text{processing time of control section}}{\text{average processing time of execution section}}$$

The factor we are interested in is S, where

$$S = \frac{\text{program running time on simulated computer itself}}{\text{program running time on the TRW-130 under simulation}}$$

We get:

$$S = \frac{\sum_{i=1}^{n} f_i(t_i + \ell)}{(F+1)\sum_{i=1}^{n} f_i T_i}$$

4. APPLICATION OF THE FORMULA FOR THE LGP-30 AND THE G-15

For the LGP-30, a reasonable estimate for the average instruction execution time (excluding latency) is

$$\sum_{i=1}^{n} f_i t_i = 300\mu s$$

The average latency time per instruction for random coding is one-half the drum revolution period:

$$\ell = 8,500\mu s$$

and with 50% latency removed,

$$\ell = 4,250\mu s$$

As indicated in Section 3, the average time to simulate an LGP-30 instruction on the TRW-130 is

$$\sum f_i T_i = 120\mu s,$$

while the overhead factor F is given by

$$F = \frac{252}{120} = 2.1$$

Thus, for randomly coded LGP-30 programs, the simulation ratio is

$$S = \frac{\sum_{i=1}^{n} f_i(t_i + \ell)}{(F+1)\sum_{i=1}^{n} f_i T_i} = \frac{300 + 8,500}{(2.1 + 1)(120)} = 24$$

With 50% latency removed, the simulation ratio is

$$S = \frac{300 + 4,250}{(2.1 + 1)(120)} = 12$$

For the Bendix G-15, the average instruction execution time (excluding latency) is estimated to be 650μs. In addition to a main drum memory with an average access time of 14.75ms, the G-15 has a fast memory with an average access time of 540μs. Thus, to estimate the latency in a G-15 program, it is necessary to make some assumptions about the distribution of data and instructions in these memories. If we assume that 80% of all accesses are directed to the main memory, and the remaining 20% to the fast memory, then the average latency time for a randomly coded program is

$$\ell = (.8)(14,750) + (.2)(540) = 11,908\mu s$$

With minimum latency coding, it is practical to remove approximately 50% of the latency from main memory access time (for simplicity, it is assumed this coding does not affect fast memory accesses), so that the latency time becomes

$$\ell = (.8)(.5)(14,750) + (.2)(540) = 6,008\mu s$$

In simulating the G-15 on the TRW-130, we expect the average time to simulate a G-15 instruction to be somewhat longer than in the case of the LGP-30, say on the order of 225μs. The simulation overhead factor will also be larger, say about 3, because of the more complicated G-15 instruction format. Thus, for randomly coded G-15 programs

$$S = \frac{650 + 11,908}{(3 + 1)(225)} = 14,$$

while for minimum latency coded programs,

$$S = \frac{650 + 6,008}{(3 + 1)(225)} = 7$$

APPENDIX

CODING OF CONTROL SECTION OF LGP-30 SIMULATOR ON THE TRW-130

A1

CARD COLOR			CORNER CUT	
RED	GREEN	MANILA	LEFT	RIGHT

LOGRAMMING SHEET

NOTE: Symbolic notation is "problem oriented"; it is not acceptable to assembler in this form.

RAMO-WOOLDRIDGE
A DIVISION OF *Thompson Ramo Wooldridge Inc.*

TO BE FILLED IN BY DISPATCHER:
SEQUENCE NO. ______
DATE: ______
TIME: ______

TO BE FILLED IN BY PROGRAMMER:
PROGRAMMER'S NAME ______
PROBLEM NO. ______
PRIORITY: ______
NO. OF CARDS ______

DATE ______ PAGE 1 OF 2
KEYPUNCHED BY ______ VERIFIED BY ______
DATE ______ DATE ______
TIME ______ TIME ______

	LOCATION 1–6	OPERATION 7–10	ADDRESS OPTION 11–12	CONT 13	SECONDARY FIELD 14–26	DUMP 27–28	L 30	E 37	A 44	P 51	M 58	D/T 65–71	µs 72–80
1	SIM	LA	DL		C		(C)	(SIM+1)	(C)	p	SIM+1	t	12
2		AS	DL		$ØNE		($ØNE)	(SIM+2)	"NEW" C	p	SIM+2	t	Block 1 12
3		SA	DL		C		(C)	(SIM+3)	(C)	p	SIM+3	t	12
4		NØ	IL		TC		R-1	(SIM+4)	(C)	3C+K	SIM+4	t	18
5		LA	DP		NØ		R	(SIM+5)	R	3C+K+1	SIM+5	t	Block 12
6		NØ	DP		NØ		R+1	(SIM+6)	R	3C+K+2	SIM+6	t	2 12
7		HP	DL		TC		3C+K+2	(SIM+7)	R	R+1	SIM+7	t	12
8		SØ	DM	D	L1		3C+K+2	(SIM+8)	X_{11},ØP	X_2,AP,0_1	SIM+8	t	15
9		CC	DM		XA		00017	(SIM+10)	ØP	X_2,AP,0_1	SIM+10	t	Block 12
10		ØCT			00017			E X T R A C T P A T T E R N					3
11		SA	DL		ØP		ØP	(SIM+11)	ØP	X_2,AP,0_1	SIM+11	t	12
12		AS	DL		T		TABLE	(SIM+12)	ØP+TABLE	X_2,AP,0_1	SIM+12	t	12
13		AP	DM	B	NØ		TABLE	(SIM+13)	X_2,AP,0_1	ØP+TABLE	SIM+13	t	12
14		CC	DM		XA		17777	(SIM+15)	2AP	ØP+TABLE	SIM+15	t	Block 12
15		ØCT			17777			E X T R A C T P A T T E R N					4
16		SA	DL		S1		2AP	(SIM+16)	2AP	ØP+TABLE	SIM+16	t	12
17		SØ	DM	S	R1		2AP	(SIM+17)	AP	ØP+TABLE	SIM+17	t	15
18		SA	DL		AP		AP	(SIM+18)	AP	ØP+TABLE	SIM+18	t	Block 5 12
19		AS	DL		S1		2AP	(SIM+19)	3AP	ØP+TABLE	SIM+19	t	Block 12
20		AS	DL		K		K	(SIM+20)	3AP+K	ØP+TABLE	SIM+20	t	6 12

FORM 2204 VELLUM

NOTE: X_m denotes m bits which are irrelevant; 0_m denotes m zero bits.

LOGRAMMING SHEET

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CARD COLOR			CORNER CUT	
RED	GREEN	MANILA	LEFT	RIGHT

TO BE FILLED IN BY DISPATCHER:	TO BE FILLED IN BY PROGRAMMER:	DATE	PAGE 2 OF 2
SEQUENCE NO.	PROGRAMMER'S NAME		
DATE:	PROBLEM NO.	KEYPUNCHED BY	VERIFIED BY
	PRIORITY:	DATE	DATE
TIME:	NO. OF CARDS	TIME	TIME

	LOCATION 1–6	OPERATION 7–10	ADDRESS OPTION 11–12	CONT 13	SECONDARY FIELD 14–26	DUMP 27–28	L 30	E 37	A 44	P 51	M 58	D/T 65–71	µs 72–80
21		SA	DL		TAP		3AP+K	(SIM+21)	3AP+K	ØP+TABLE	SIM+21	t	12
22		LP	DP		NØ		(ØP+TABLE)	(ØP+TABLE)	3AP+K	ØP+TABLE+1	(OP+TABLE)	t	Block 7 12
													252µs

FORM 2204 VELLUM