A. Operation of the Basic Circuits

BEAST

1. Flip-Flop

The basic flip-flop circuit used in the WISC is shown in drawing W-021S, L-03A. The circuit has two stable states: either the right hand triode is conducting and the left hand triode is not or vice-verse. If the right hand triode is conducting the potential at plate 2 (the C's output plate) is nominally 55 volts. Consequently, the potential at pin 6 is approximately -30 volts (the left hand tube is biased below cut-off) and the potential at pin 1, $+133 volts, is determined by the voltage divider formed by the 10K and 82K resistors. The potential at pin 5 would be $130 volts if it were not for the current into the positive grid. This grid current limits the positive grid excursion to about 1.5 volts.

The two output terminals of the device thus will be at $133 and 55 volts, or 55 and 133 volts respectively. By definition the #1 pin of a flip-flop circuit is defined as the "1's" output. Likewise, the #2 pin of the 6J6 flip-flop* is the "0's" output. Also by definition if the 1's output is at the $130 volt level the flip-flop is said to contain a 1. Conversely if the ones output is at $55 volts the flip-flop contains a 0. It should be noted that the 1 level, $133 volts, is affected very little by variation in the characteristics of the vacuum tube, while the 0 level is very dependent upon the characteristic of the tube.

The device will remain with the 1's output high (or 0's output high) until a negative going pulse occurs at the 0's input (or 1's input). When this occurs the flip-flop will assume the other stable state. The pulse that sets the flip-flop to the 0 state is often called the "reset pulse" or "reset" while the pulse which sets it to the 1 state is sometimes referred to as the "trigger pulse" or "trigger". Although the circuit responds more readily to negative going waveforms it can be triggered or reset by a positive going pulse of sufficient amplitude. However, in the WISC the pulse and coupling capacitors used are such that the circuit will respond only to the negative going portion of a pulse.

The flip-flop is intended only for those applications where the trigger and the reset do not occur simultaneously. If such a condition exists the circuit tends to change to the other state, that is, if the flip-flop contains a 1 and receives a trigger and a reset simultaneously it will prefer the reset or 0 state. This action is sometimes desired, but it can be obtained more reliably (especially if the pulses occur at high repetition rates) from the standard WISC counter circuit.

The logical block diagram of the flip-flop shows that by convention the upper input is the 1's input, while the upper output terminal is the 1's output. This convention is followed in logical drawings wherever possible and any exceptions should be noted.

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* In the case of 9 pin double triodes the #6 pin is the 0's output.

## 2. Counter

The counter circuit is basically the same as that of the flip-flop the only difference being in the manner in which the input pulses are coupled. In the counter circuit the two input capacitors are replaced with two diodes and one CR differentiating circuit. The diodes are sometimes called commutating diodes in that they alternately couple the input pulses from one grid to the other. An examination of the potentials across each diode for each of the stable states will indicate how this is accomplished.

Logically the counter is somewhat of a frustrated flip-flop: given an input pulse it always changes to the state it wasn't in. Consequently, it repeats itself every other time it receives an input pulse. Thus it counts by a factor of two and if a number of these counters are connected in series they count down by a factor of $2^n$ where n is the number of counters in series. The last stage of such a counter chain changes from the 1 state to the 0 state only once for each $2^n$ input pulses

## 3. Cathode Follower

The schematic and logical diagrams of this circuit are shown in drawing W-0243L-02A. As the name implies the cathode or output terminal of this device follows, or is approximately equal to, the input or grid potential. The small signal gain of this circuit approaches unity within the limitations of its frequency response. If the input potential at some instant is $V_1$, the output potential is $V_1 \mp \Delta V$ where $\Delta V$ is the absolute value of the grid to cathode bias. For instance, if the input terminal (say pin 2) is connected directly to the plate of a flip-flop or counter the output potential (at pin 3) will be approximately 133 ∓ 4 volts or 55 ∓ 10 volts depending upon which state the flip-flop assumes. It should be noticed that the bias at the 55 volt input level is larger than that at the 133 volt input lever. From this it can be seen that the large signal gain in this case is approximately $\frac{133-55}{137-65} = \frac{72}{78} = 0.923$.

For reasons which will become obvious when discussing the gate circuit it is desirable that the high level output be maintained at +133 volts. Since the input terminals of a cathode follower are directly connected to a flip-flop plate they are often shunted by a 220 or 270K resistor to reduce the 1's level at the input terminals by about 4 volts. Thus the output of the CF is 129∓4 = 133 volts when the flip-flop is in the 1 state.

The cathode follower circuit possesses two features which make its use desirable. First, it possesses a high input inpedance, and second it has a low output impedance. It is used whenever a signal derived from a flip-flop or counter must drive a number of other circuits or must be transmitted some distance. It acts as a buffer between the signal source and the load hence it is sometimes referred to as a buffer.

The above statement concerning input and output impedance must be qualified somewhat. Obviously the triode will not conduct if the grid is at a large negative potential. In such a case the output impedance is 22K ohms. Again as the grid is driven positive a point will eventually

be reached where the bias will become zero. For grid potentials greater than those producing zero bias grid current will be drawn and the device no longer has a high input impedance. When the circuit is used with square waves another complication arises. If the grid is driven from the 1 level to the 0 level instantaneously, the tube will be cut off. The cathode potential will fall only as fast as the shunt and stray capacitances will discharge through the load and the cathode resistor. As an example, assume that the effective cathode to ground resistance is 20K and that the stray and shunt capacitance amount to 100 micro-micro farads. The RC time constant under these conditions is $(.020 \times 10^{6}$ ohms) $(100 \times 10^{-12}$ farads) = 2 micro-seconds, which is greater than the RC time constant in the flip-flop plate circuit. Hence, for these conditions the cathode is not following the grid and the fall time of the output signal is not determined by the input signal but by the RC time constant in the output circuit. The cathode follower circut, then, has a low output impedance for positive going signals and may have a low output impedance for negative going signals.

Other triodes than the 12A47 may be used as cathode followers in the WISC and BEAST. The basic operation of the circuit remains the same, and the grid to cathode bias at the 1 & 0 level will be only slightly different.

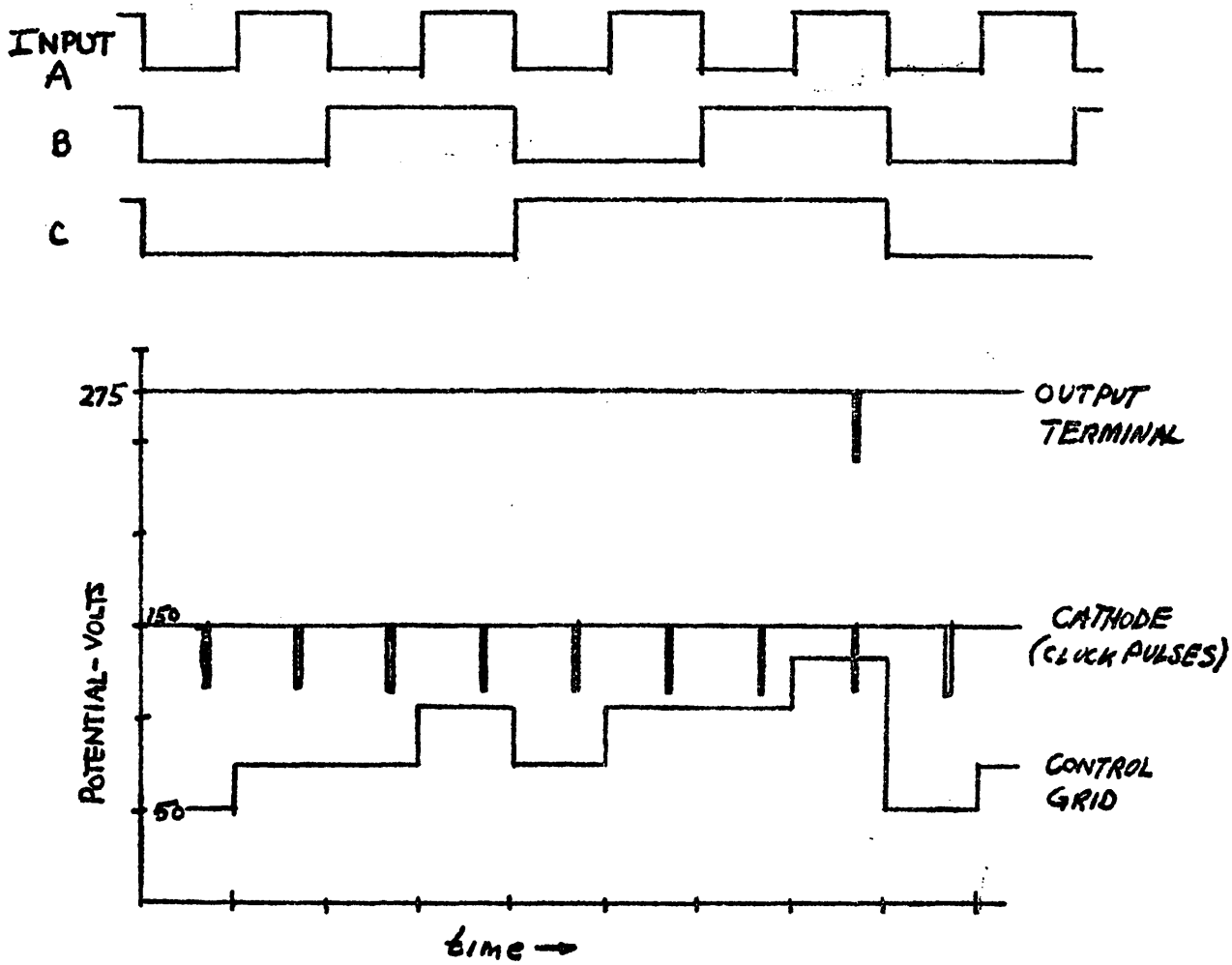
## 4. Negator

This circuit is alos shown in figure W-024SL-02A. The input to this circuit should be of the same form as the output of flip-flops and counters: i.e., either at +133 volts or at +55 volts. For these conditions the potential at the grid connection will be at +30 and -30 volts respectively, if the triode is not in the circuit. With the tube in the circuit the grid will be limited in its positive excursion to about +1 volt. The potential at the output terminals will be +55 volts if the input is +133 volts and 130 volts if the input is at 55 volts. Thus the circuit inverts or negates the input signal. The negator might be described as half a flip-flop, in fact a bi-stable circuit can be constructed from two negators by connecting the output of the first to the input of the second and vice-versa.

## 5. Pulsed Gates

The standard pulsed gate circuits used in the WISC are shown in figure W-023SL-04A. In all of these gates the cathodes are connected to a pulse generator which pulses the cathodes down from +150 volts to about +115 volts. The plate terminal is the output terminal and if a signal appears at this point it is a fair reproduction of the cathode pulse; i.e., the input and output pulses are about the same shape and magnitude. The pulse at the plate; however, is biased at +275 volts (the supply voltage). The grid, which controls the gate, is generally connected to three 100K resistors or their equivalent which are in turn connected to flip-flop plates or their equivalent. Thus there are $2^3$ or 8 possible conbinations of input conditions which can occur. However, there will only be four distinct potentials possible at the control grid itself.

In the following diagram the different time varying waveforms (A,B, and C) are connected to the three input control terminals.




A pulse will be present at the output only if all three control inputs are in the 1's state and the cathode is pulsed. It can be said that the gate passes the pulse and that the three inputs enable a pulse to be passed. Hence, the signals obtained from flip-flop or equivalent circuits are called "enables". The logical block diagram for this circuit indicates the three mixing resistors by the small circle about the point at which the three signals meet. The closed arrow indicates enables or d.c. signals while the open arrows denote pulse signals such as clock or gate pulses. It is possible to use these gate circuits in an OR combination by connecting the plate terminals in parallel. In this case there should be only one plate resistor for each such OR combination.

It is sometimes desirable that the output pulse from a gate be biased at +150 volts so that it can be connected to the cathode of another gate. This is accomplished by replacing the plate resistor by a 4:1 step down pulse transformer and connecting the correct secondary terminal to a +150 volt supply. It should be noted that the input of this type gate is connected directly to a cathode follower.

In some applications the pulse transformer used has a 1:1 ratio and is biased at -60 volts. In such applications the gate drives a beam power tube such as the 6CM6 or 6AQ5.

6. D.C. Gates

The basic d.c. gates used in the WISC are shown in drawing W-023SL-06A. The diodes used at the present time are type 1N38 manufactured by Radio Receptor Corporation and these seem to be quite reliable if reasonable precautions are taken in soldering them into the circuits. Since they are 100 volt diodes the input potentials to these diodes should be chosen so that this peak inverse voltage is not exceeded. In particular, it is not wise to connect one of the inputs to a diode gate to ground if the other inputs may reach +133 volts.

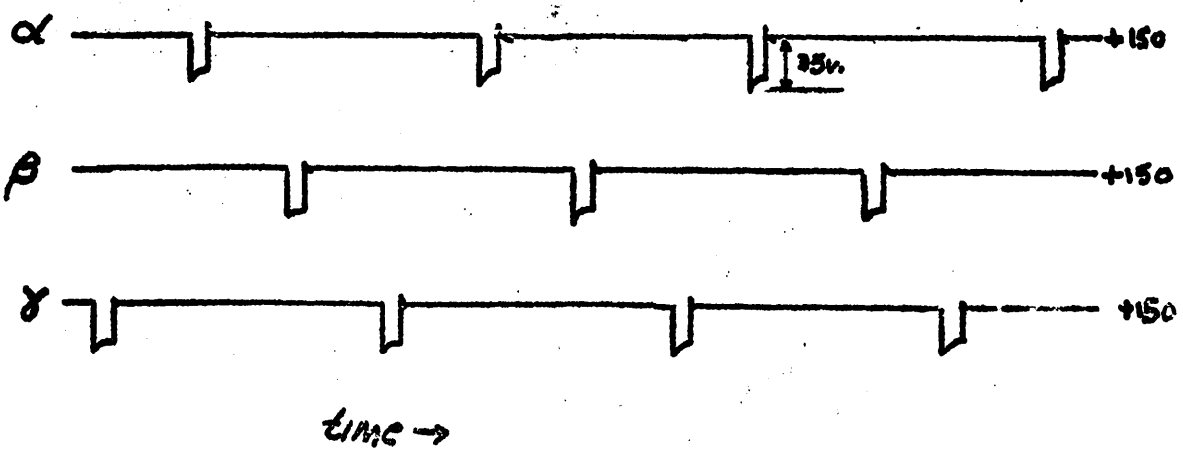
The 470K resistors chosen in the first two circuits represent a compromise between output rise or fall time and minimum loading of the circuits connected to the input terminals. Note the 150K resistor returned to +275 volts in the fourth circuit: An examination of the currents and potentials existing in this circuit will show the reason for this rather low resistance value.

Various combinations of all of these circuits may be used provided that appropriate buffering or isolation is used. In all of these circuits three inputs are shown; however, more than three may also be used safely.

B. The BEAST Circuit

1. The Clock Section

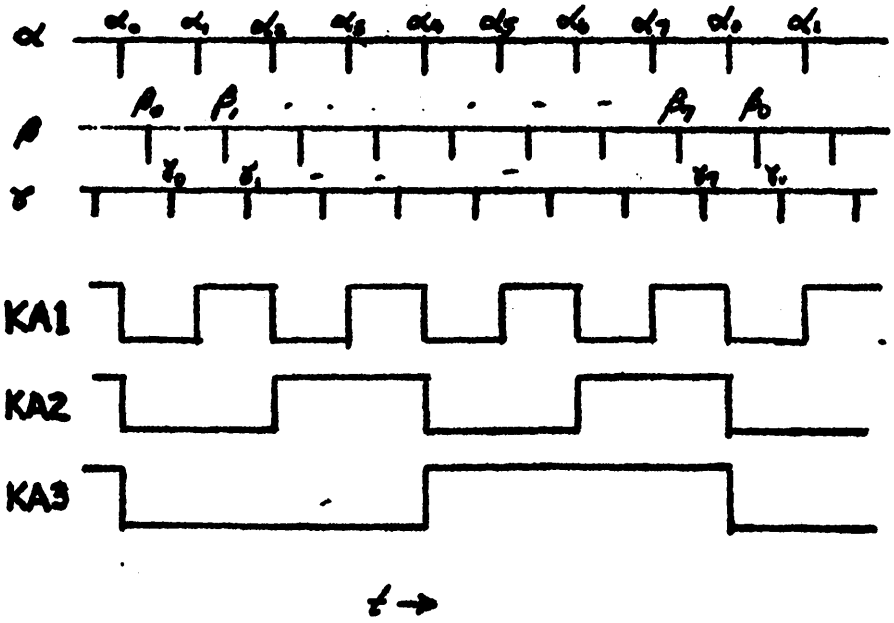
The clock or timing section of the BEAST generates the timing or synchronizing voltages used throughout the BEAST and available on the front panel. The one microsecond wide voltage waveforms used in the WISC and the BEAST are called pulses while the waveforms of longer duration or width are called enables. The frequency of the clock pulses generated in the BEAST is variable and can be set by means of the clock frequency switch to approximately 100KC, 10KC, or 1KC. The Manual setting of this switch can be used to generate one clock pulse at a time. As in the WISC there are three sets of families of these clock pulses designated as $\alpha$, $\beta$ and $\gamma$ and separated in time from each other by one third of their common period.



These clock pulses, nominally 35 volts in magnitude and biased at +150 volts, are available at the banana jacks on the front panel of the BEAST.

To simulate the major and minor cycle enables available in the WISC two five stage counters are used (counters A and B) Counter A, KA, receives clock pulses and therefore counts $2^5$ or 32 clock pulses before it repeats or zeroes itself. The ones output of the individual stages of counter A are available and are called KA1, KA2, - -, KA5. Counter B, KB, can be driven by clock pulses, KA5, or some other waveform selected by the operator. Hence it may repeat or zero itself once for each $2^5$ to $2^{10}$ clock pulses. The ones output of the individual stage of this counter, KB1, KB2, - -, KB5, are also available on the front panel.

The time at which all of the counters being used are in the zero state is called bit time zero (a bit time being defined as the time from $\alpha$ to $\alpha$ or $\beta$ to $\beta$.) Since these counters are run at $\alpha$ time the pulse which occurs at the time that the counters return to zero is defined as $\alpha_0$. As an example consider that counters KA1, KA2, and KA3 are being used for some purpose and that the repetition rate of counter KA3 is the smallest repetition rate being used. Then the length of a major cycle is 8 bit times. The timing and waveforms under this situation would be as follows:




If, however, KA5 were used there would be $2^5$ = 32 bit times per major cycle and the $\alpha$ pulses would be numbered $\alpha_0$ to $\alpha_{31}$.

## 2. Enable Generators $E_A$, $E_B$, $E_C$, $E_D$,

These circuits (Drawing W-002L-04A) are used to generate enables of variable repetition rates and widths. Actually each of these generators produces several enables: for instance, the $E_A$ generator produces $E_A$, $\bar{E}_A$, $E_{A1}$, $E_{A2}$, $E_{A3}$, and $E_{A4}$. Hence the term $E_A$ generator is somewhat misleading. A more proper term might be "the A enable generator" but for the sake of brevity the term $E_A$ generator indicates the circuitry which produces $E_A$ and its related family.

Each of the primary enables ($E_A$, $E_B$, $E_C$, and $E_D$) assumes the 1 state at the time that a selected KB counter goes to the zero state. For instance if the $E_A$ trigger selector switch set on the "KB3" position and the reset or width selector switch is set at "3" enable $E_A$ goes from the 0 state to the 1 state at the time that KB3 goes from the 1 state to the 0 state. $E_A$ then remaines in the 1 state for three bit times (see the example on page 9).

Since the counters run at $\alpha$ time $E_A$ is always a 1 from $\alpha_o$ to $\alpha_n$ where n is the width selected. $E_{A1}$, $E_{A2}$, $E_{A3}$, and $E_{A4}$ are each at the 1 level for 2/3 of a bit time such that they are sampleable at $\alpha_n$, $\beta_n$, $\gamma_n$, and $\alpha_{n+1}$ respectively.

A block diagram of the $E_A$ generator is shown on page 10. The foregoing comments and the diagrams pertaining to $E_A$ also are valid to $E_B$, $E_C$, and $E_D$ with the exception that the C and D enable generators only produce the first three enables (for example, $E_C$, $\bar{E}_C$, and $E_{C1}$).

## 3. Error Detecting Circuits

The error detecting circuits W-002L-02A are provided so that two enables may be compared to determine that they are identical (at least at the sampling time). For instance, the correct operation of counters A and B may be checked by connecting KA5 to the A coincidence input and KB5 to the B coincidence input and sampling at $\beta$ (or $\gamma$) time by connecting TIME AB to $\beta$ (or $\gamma$) pulses. If the two enables are not identical (both 1 or both 0) at $\beta$ (or $\gamma$) time, the enable Error AB will be generated and a neon light on panel J will be turned on.

A three position switch, also located on panel J, can be used to disable these circuits, reset the Error flip-flop, or allow the checking operation described above. This switch also controls the C and D error detecting circuits which are similar to the A and B circuits.

The signal Error AB is generated (if the switch is in the "CHECK" position) if $(A\bar{E}) + (B\bar{A}) = 1$ at the AB sampling time. Similarly Error DC is generated if $(C\bar{D}) + (\bar{C}D) = 1$ at the CD sampling time. If either of these two enables are present the ERROR enable is generated ($E_{AB} + E_{CD} = E$). This enable (ERROR) is used in the start-stop control circuits where it may cause the counters KA and KB to stop.

4. Run-Stop Control

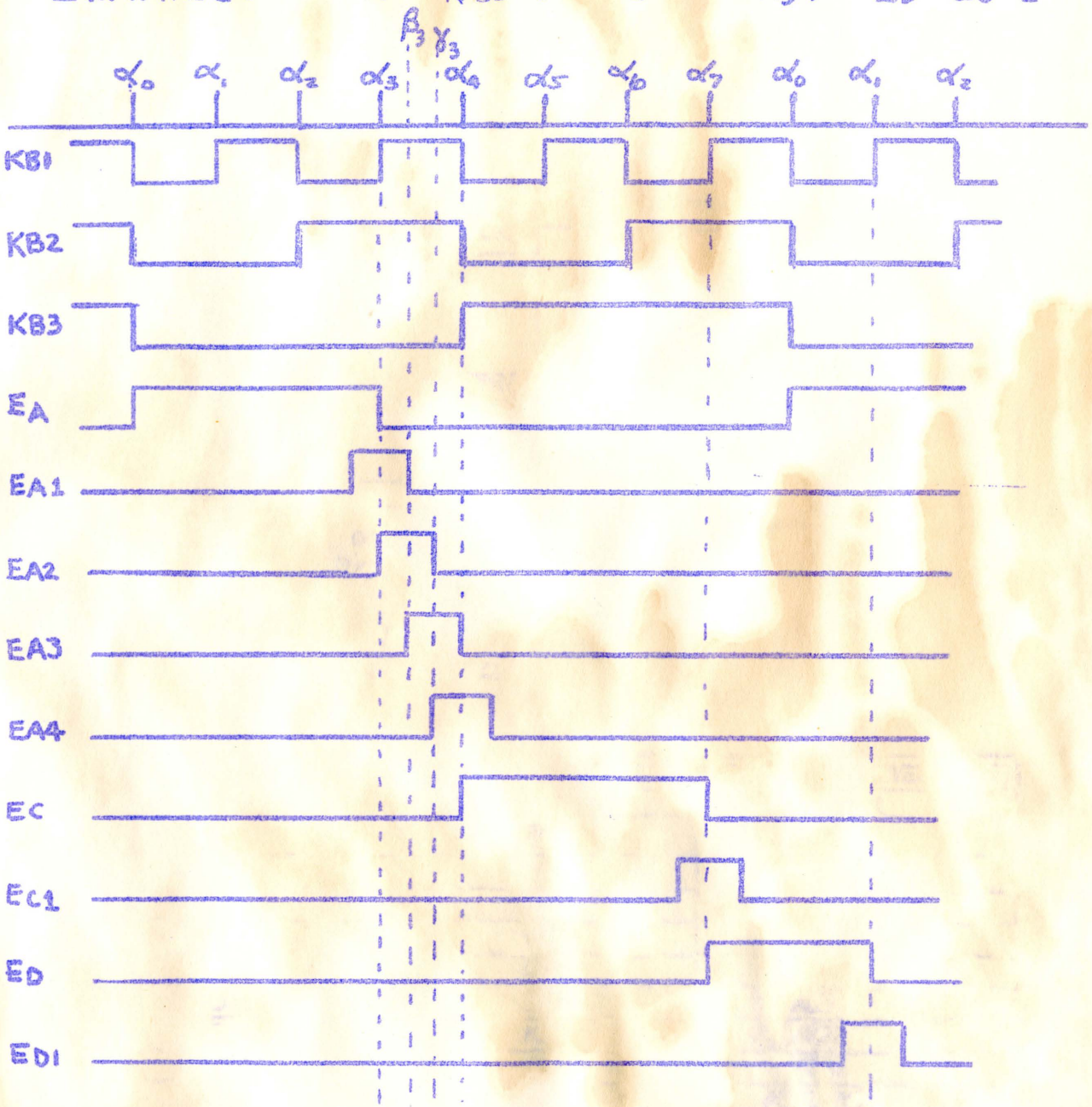
The run-stop control, drawing W-002-03A, has two functions: First, it controls or gates the RA pulses which run the A counter. The switch on panel J has three settings: Run, Internal, and External control. In the Run position counter A receives RA pulses continually while in the Internal position RA pulses are present only if R(RUN) is present. In the third or External position the counter is under the control of whatever enable is provided on the banana jack provided.

The enable R is produced by momentarily setting the lower switch to the "RESET" position. When this switch is momentarily set to "STOP" R will dissapear (become a 0), or if the enable E, error, should become a 1 while the switch is in the "RUN" position.

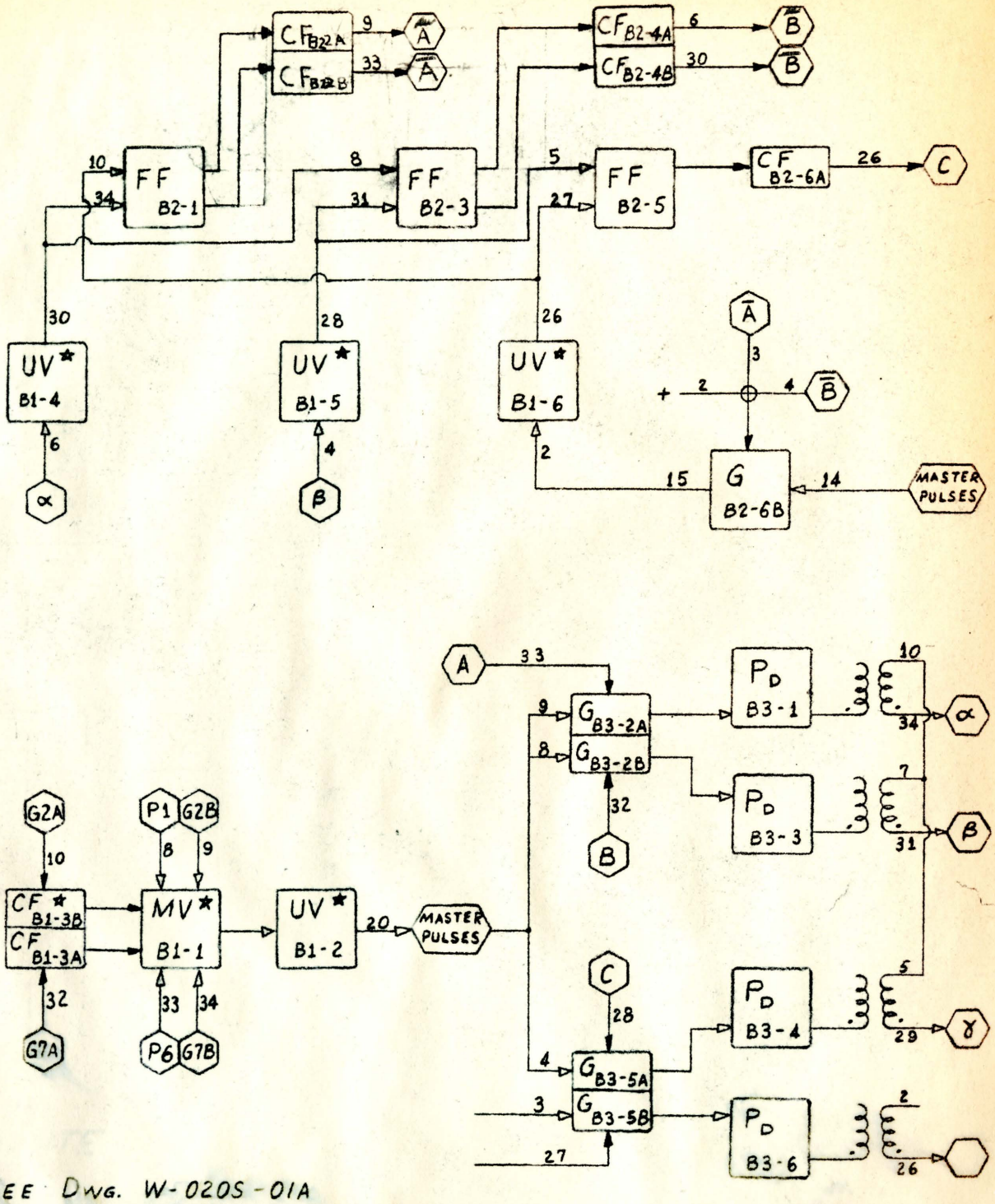
The second function of the run-stop control circuits is to synchronise counters A and B when they are run at the same frequency (see note on drawing W-002L-05A). If counters A and B are in synchronism KA5 and KB5 will be identical and the expression $(KB5 + \overline{KA5})$ should equal 1. In this case the pulses RB will be present continually. If, however, these two counters are not in synchronism $(KB5 + \overline{KA5}) \neq 1$ and counter B will receive fewer pulses (RB) than counter A until they do become synchronized.

# ENABLE GENERATORS

EXAMPLE: $E_A = KB3 \cdot 3$ $EC = E_{A3} \cdot 7$ $E_D = E_C \cdot 1$




2/21/58 AKS







★ SEE DWG. W-020S-01A
SPECIAL CIRCUITS

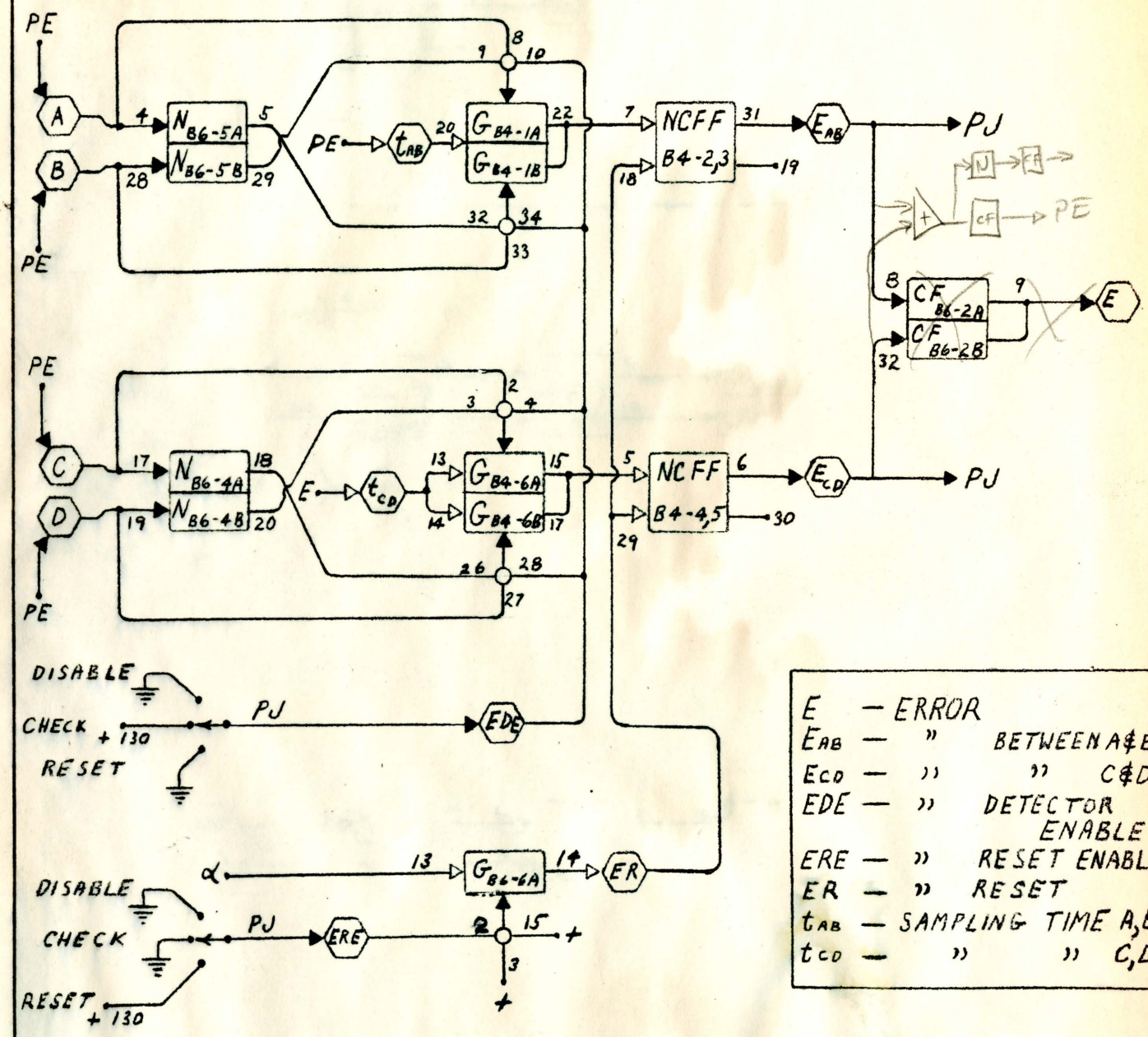
| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

Capacitors in _____
Resistors in _____ ½ W, 10%
} UNLESS OTHERWISE NOTED

UNIVERSITY of WISCONSIN
Elec. Eng. Dept.– Computer Research
CLOCK SECTION
- BEAST -

| Dr. RK | Eng. AKS | Date 4-25-57 |
|---|---|---|
| Dwg No. W-002L-01A | | |

# ERROR DETECTING CIRCUITS




E — ERROR
$E_{AB}$ — " BETWEEN A&B
$E_{CD}$ — " " C&D
EDE — " DETECTOR ENABLE
ERE — " RESET ENABLE
ER — " RESET
$t_{AB}$ — SAMPLING TIME A,B
$t_{CD}$ — " " C,D

ERROR DETECTING
SWITCH PANEL J

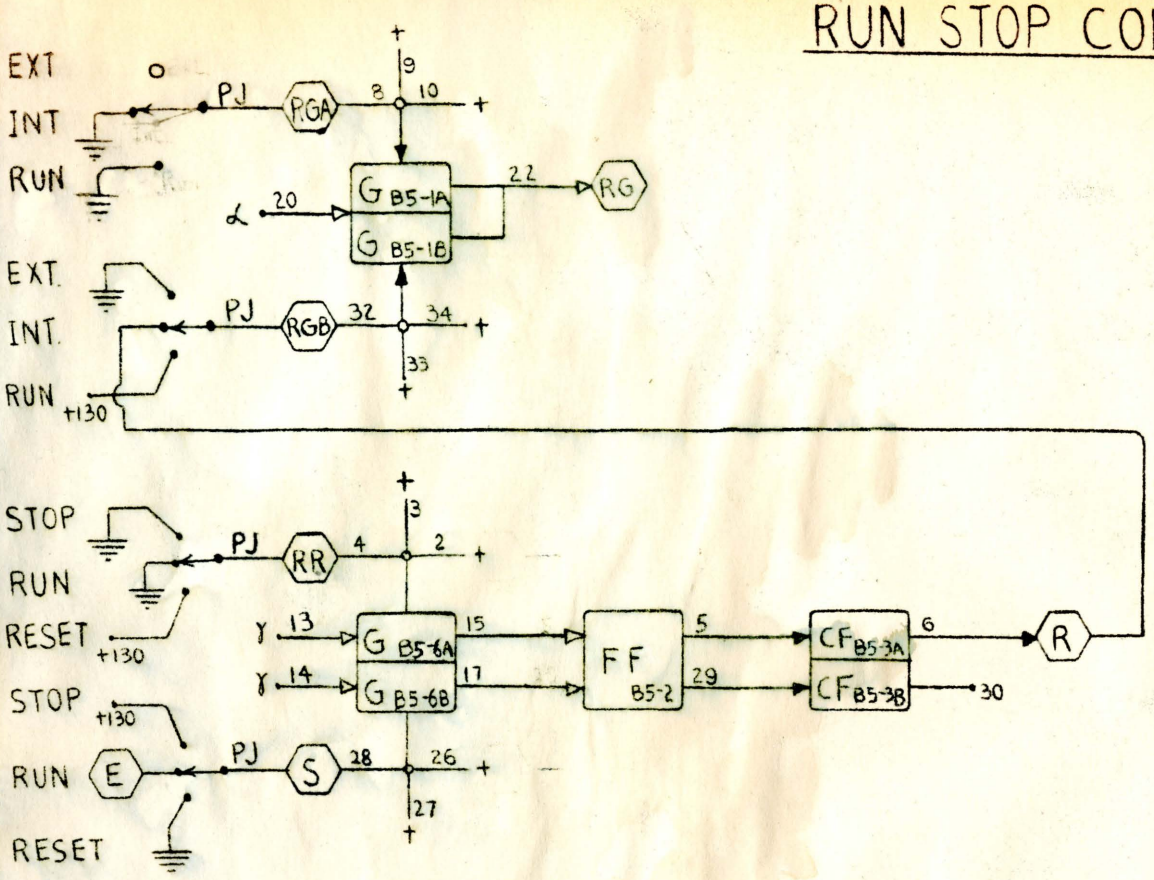
| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

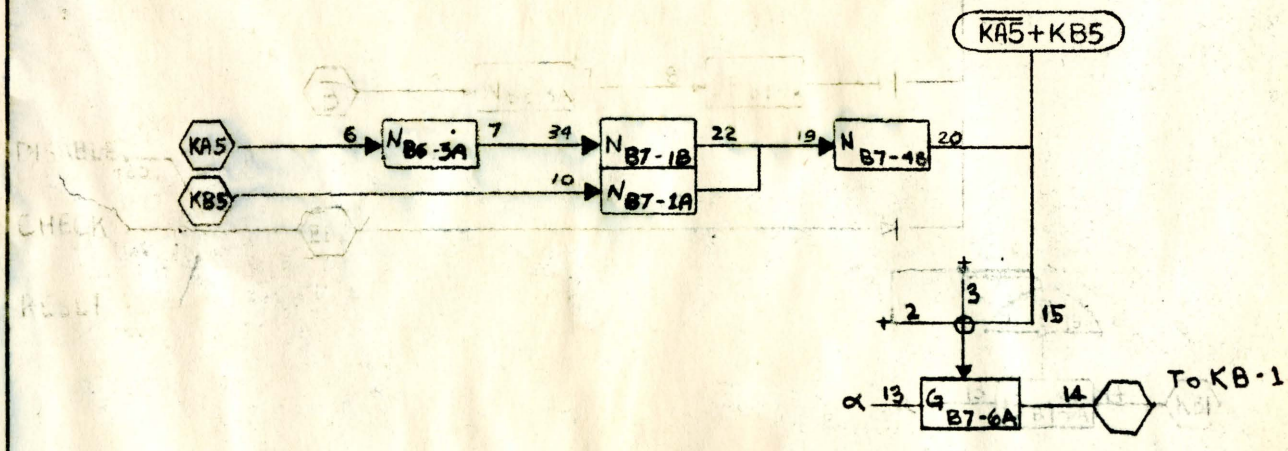
Capacitors in _____ } UNLESS OTHERWISE NOTED
Resistors in _____ ½ W, 10%

UNIVERSITY of WISCONSIN
Elec. Eng. Dept.— Computer Research
ERROR DETECTING CIRCUITS
— BEAST —

| Dr. N.P. | Eng. A.K.S. | Date 6 APR '57 |
|---|---|---|
| Dwg No. W-002L-02A | | |

# RUN STOP CONTROL




| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

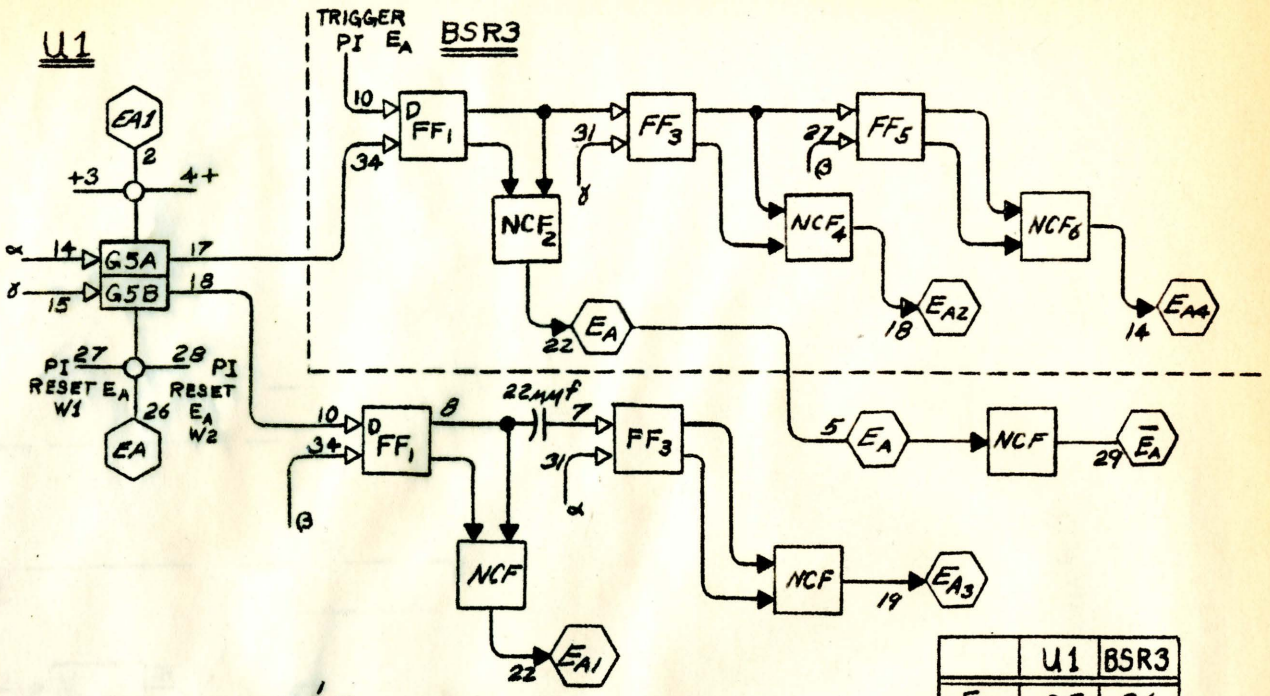
Capacitors in _____
Resistors in _____ ½ W, 10 %
} UNLESS OTHERWISE NOTED

**UNIVERSITY of WISCONSIN**
Elec. Eng. Dept.— Computer Research
RUN-STOP CONTROL - BEAST

| Dr. G H/AKS | Eng. A K S | Date 6/6/57 |
|---|---|---|

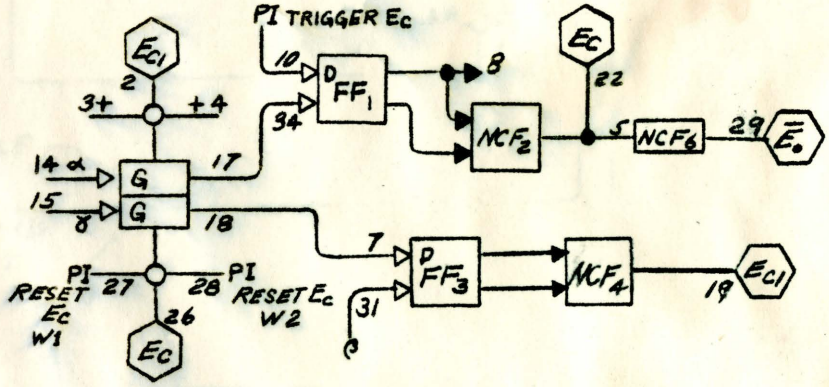
Dwg No. W-002 L - 03A

## $E_A$ & $E_B$




| | U1 | BSR3 |
|---|---|---|
| $E_A$ | C5 | C6 |
| $E_B$ | C3 | C4 |

## $E_C$ & $E_D$




| | U1 |
|---|---|
| $E_C$ | $C_2$ |
| $E_D$ | $C_1$ |

| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

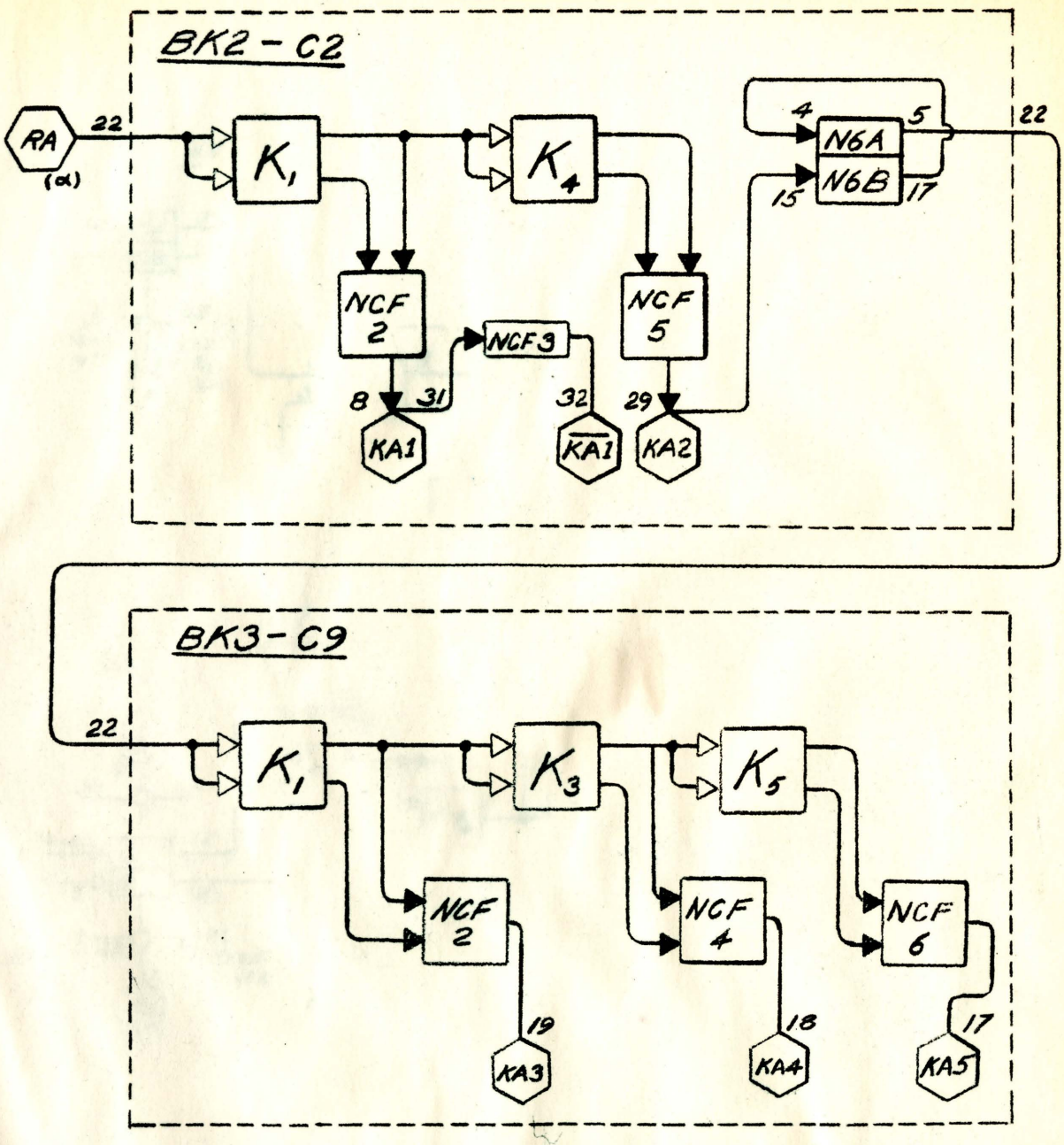
Capacitors in _____
Resistors in _____ ½ W, 10%
} UNLESS OTHERWISE NOTED

UNIVERSITY of WISCONSIN
Elec. Eng. Dept.– Computer Research
ENABLE GENERATING SECTIONS – A & B and C & D
~ BEAST ~

Dr. BCA | Eng. AAS | Date 6-28-71

Dwg No. W002L-04A

# COUNTER A




COUNTER B SAME EXCEPT BK2 IN C8, BK3 IN C7 AND INPUT TO BK2 COMES FROM PANEL J: EXT RB KA5 → B COUNTER SECTION

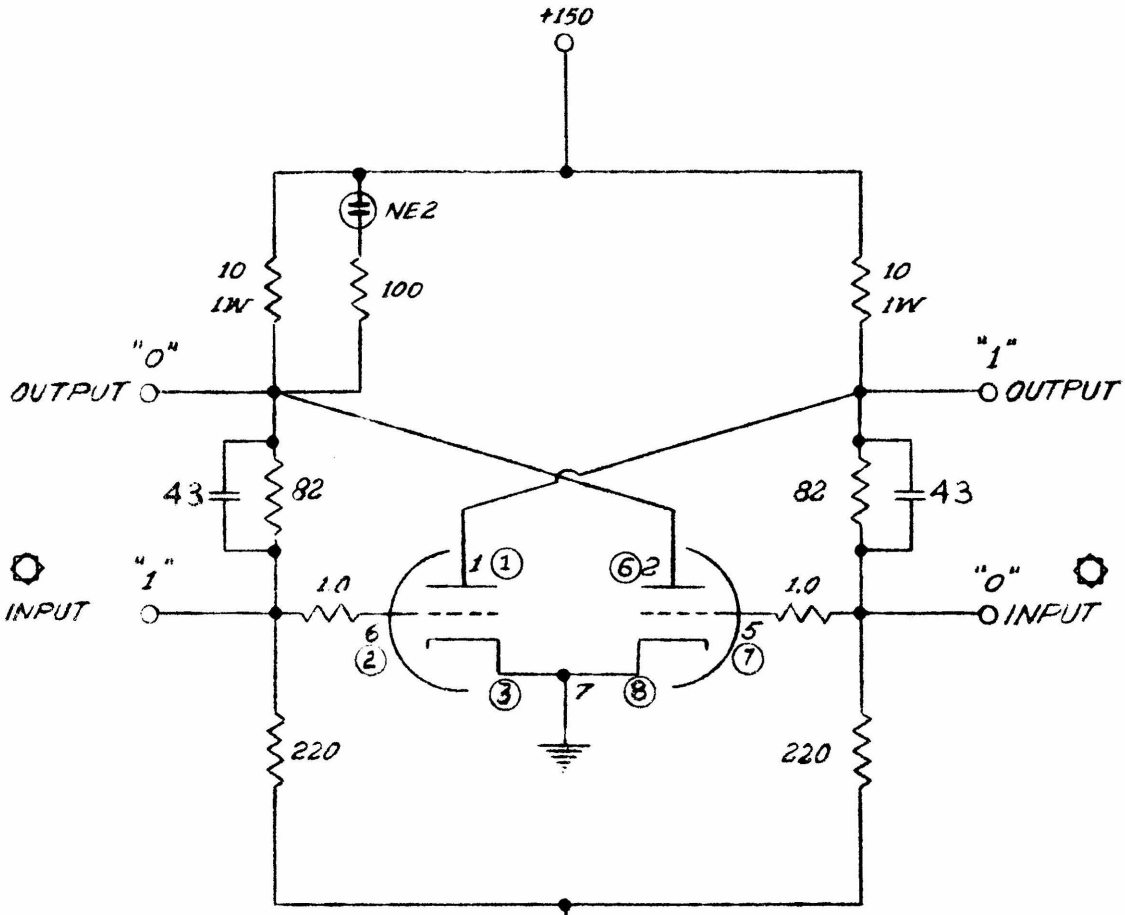
| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

Capacitors in _____
Resistors in _____ ½ W, 10%
} UNLESS OTHERWISE NOTED

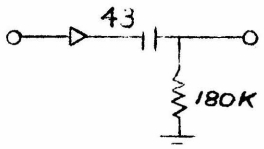
UNIVERSITY of WISCONSIN
Elec. Eng. Dept.– Computer Research
COUNTER SECTION
~ BEAST ~

Dr. BLH | Eng. AKS | Date 6-27-57

Dwg No. W002L-05A

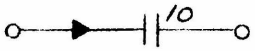



INPUT COUPLING



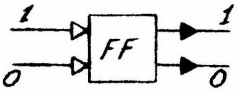

INPUT IF PULSES
(CLOCK OR GATE)

-250



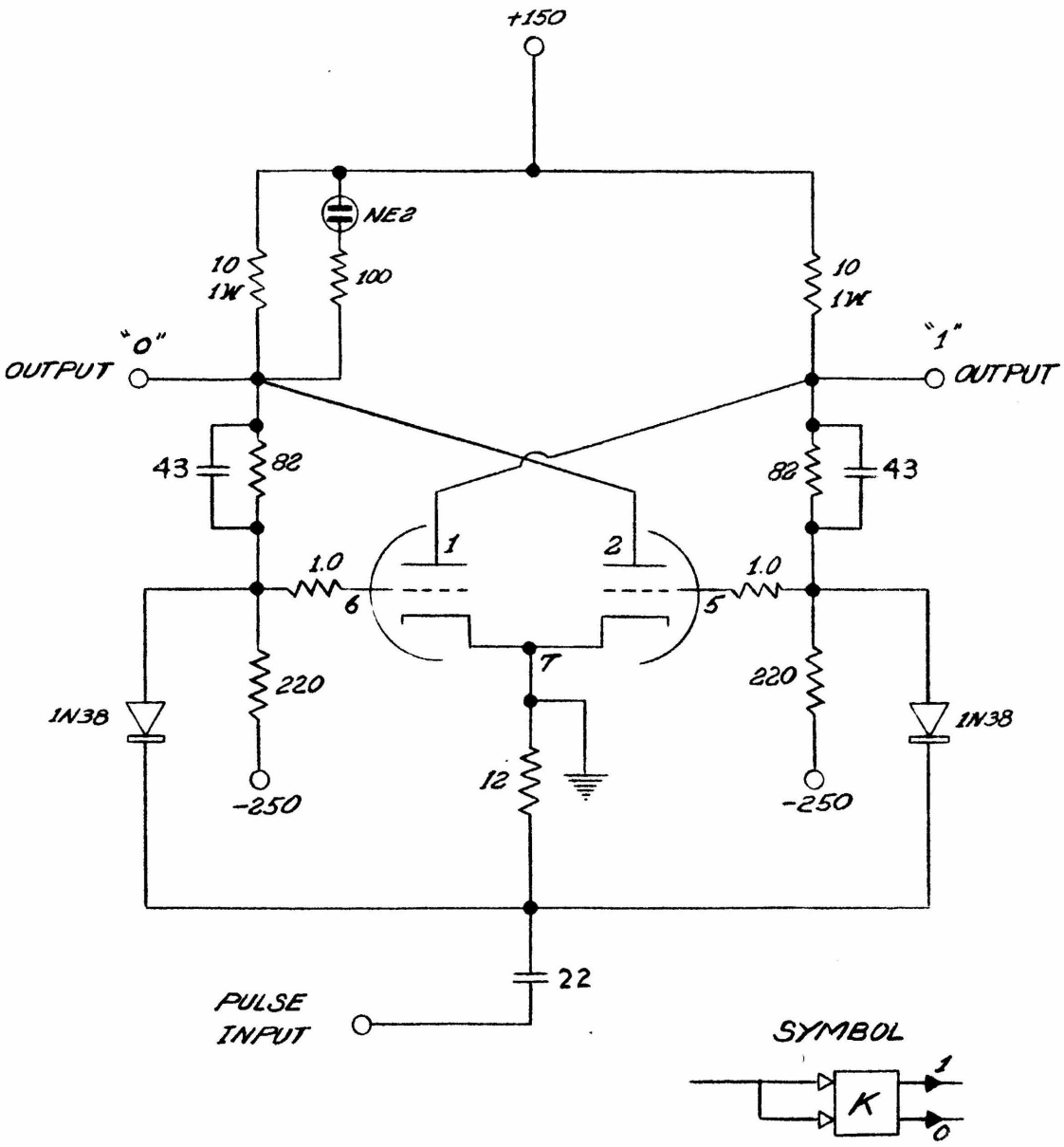

INPUT IF PREVIOUS
STAGE IS FF OR K

SYMBOL




CAPACITORS IN MMfd
RESISTORS IN KΩ ½ W, 10%
} UNLESS OTHERWISE NOTED

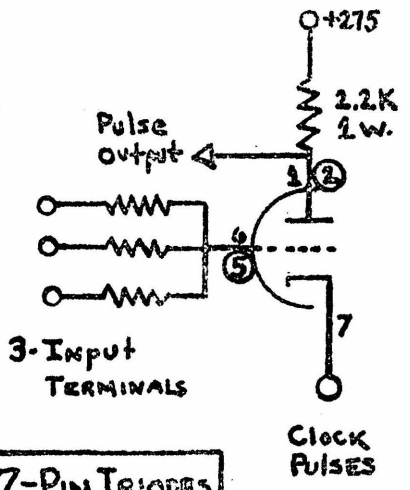
STANDARD WISC FLIP-FLOP
TYPE 5844, 5965, 6211
DRAWING No W-021S, L-03A
ISSUE NUMBER 2
DATE: 7-27-57



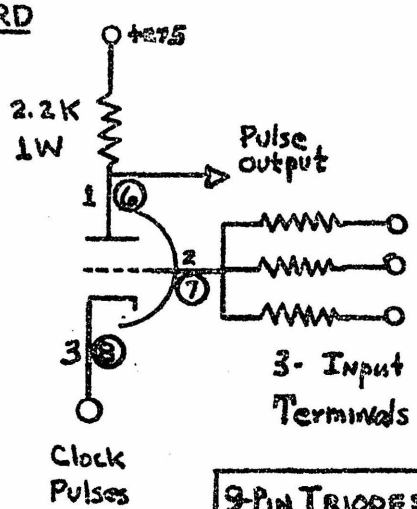

CAPACITORS IN MMfd
RESISTORS IN KΩ ½ W, 10%
} UNLESS OTHERWISE NOTED

STANDARD WISC COUNTER
TYPE 6J6 OR 5844
DRAWING No W-022S, L-01A
ISSUE NUMBER-2
DATE: 7-27-51

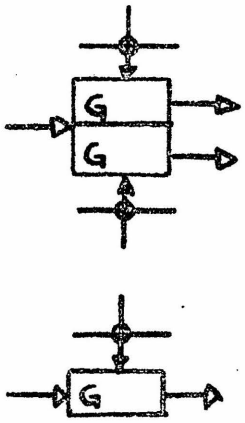
## STANDARD GATES



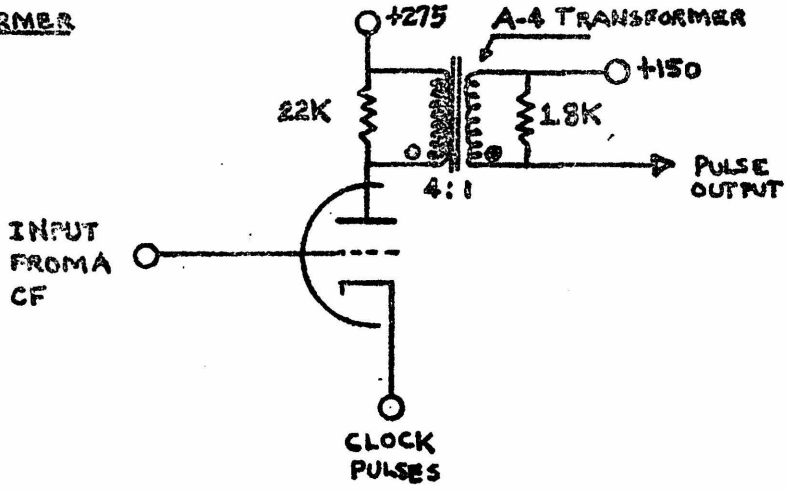

7-Pin Triodes

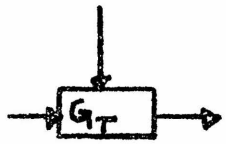



9-Pin Triodes

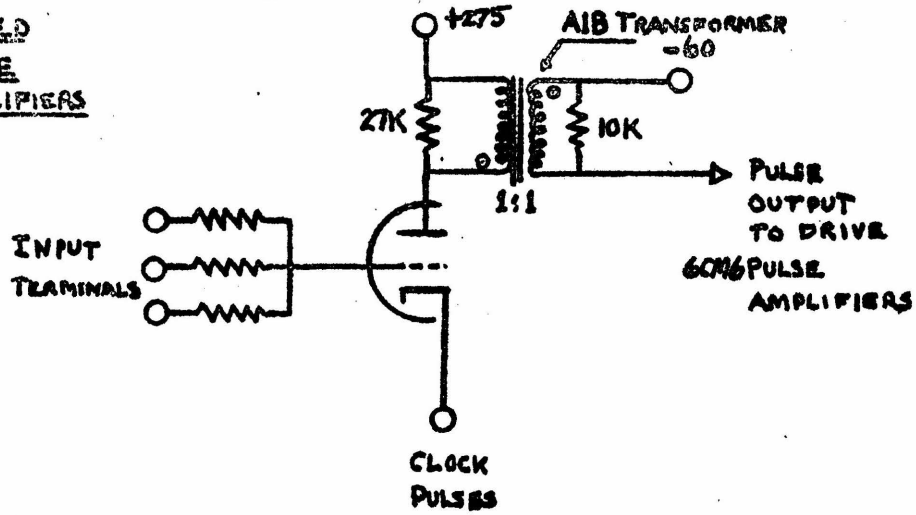


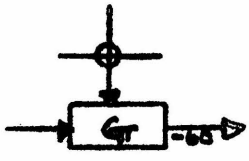

## TRANSFORMER COUPLED GATES




## GATED PULSE AMPLIFIERS



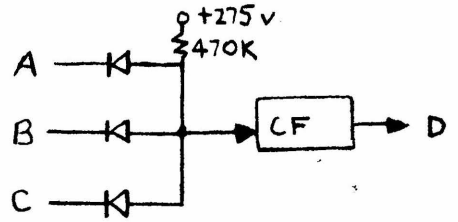
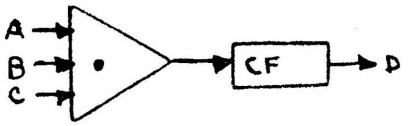
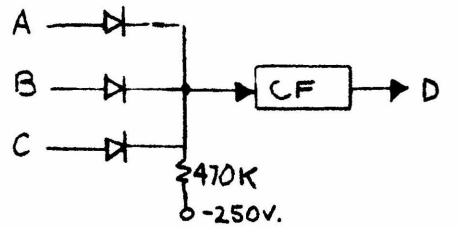
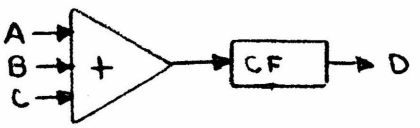
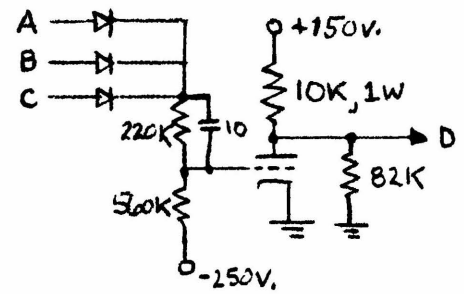
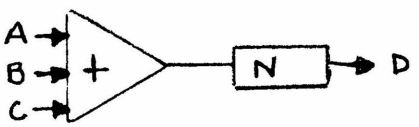
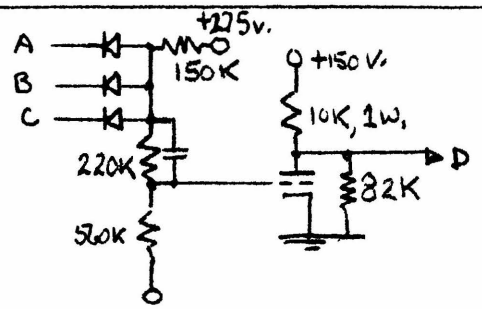
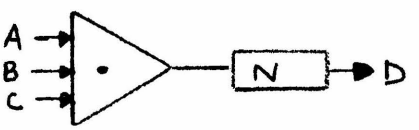

| Issue No | Revisions | By | Date |
|---|---|---|---|
| 2 | 7PN, 9PN, GT | AKS | 2/28/58 |

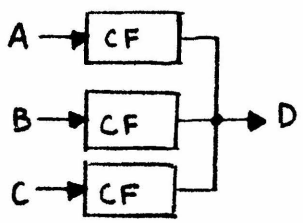
PULSE GATES - WISC

CAP. IN μμfd.
RESISTORS IN KΩ, ½W, 10%
ALL GRID RESISTORS ARE 100K, ½W

| DR. AKS | ENG. AKS | DATE 2/28/58 |
|---|---|---|

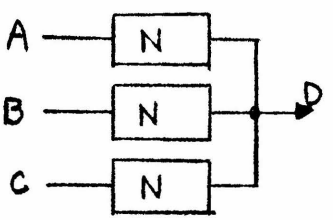
Dwg. No. W-0235L-04A

| CIRCUIT | SYMBOL | LOGICAL FUNCTION |
|---|---|---|
|   |   | $A \cdot B \cdot C = D$ |
|   |   | $A+B+C = D$ |
|   |   | $\overline{A+B+C} = D$<br>$\overline{A} \cdot \overline{B} \cdot \overline{C} = D$ |
|   |   | $\overline{A \cdot B \cdot C} = D$<br>$\overline{A}+\overline{B}+\overline{C} = D$ |




$D = A+B+C$

ONLY 1 CATHODE RESISTOR IS USED




$D = \overline{A+B+C}$
$= \overline{A} \cdot \overline{B} \cdot \overline{C}$

ONLY 1 PLATE RESISTOR IS USED

| Issue No. | Revisions | By | Date |
|---|---|---|---|
| | | | |

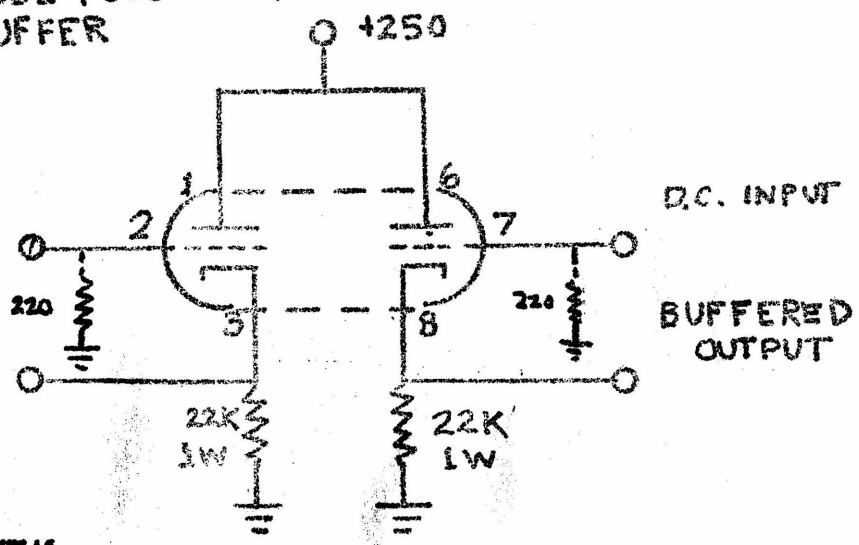
UNIVERSITY of WISCONSIN
Elec. Eng. Dept.– Computer Research
D.C. GATES

Capacitors in μμf
Resistors in KΩ ½ W, 10%
} UNLESS OTHERWISE NOTED

| Dr. AKS | Eng. AKS | Date 2/21/58 |
|---|---|---|

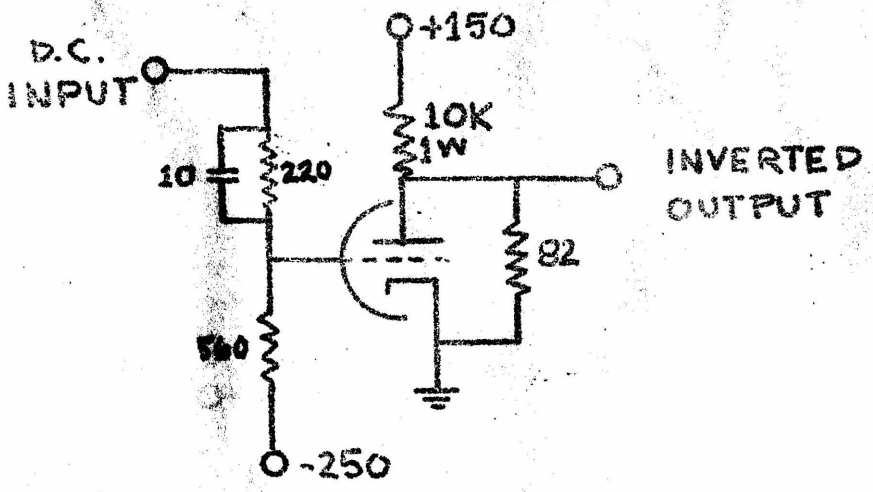
Dwg No. W-023S,L-06A

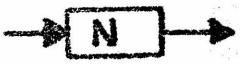
## CATHODE FOLLOWER OR BUFFER




IF INPUT IS FROM A FF 220 K RESISTOR SHOULD BE USED


## NEGATOR OR INVERTOR

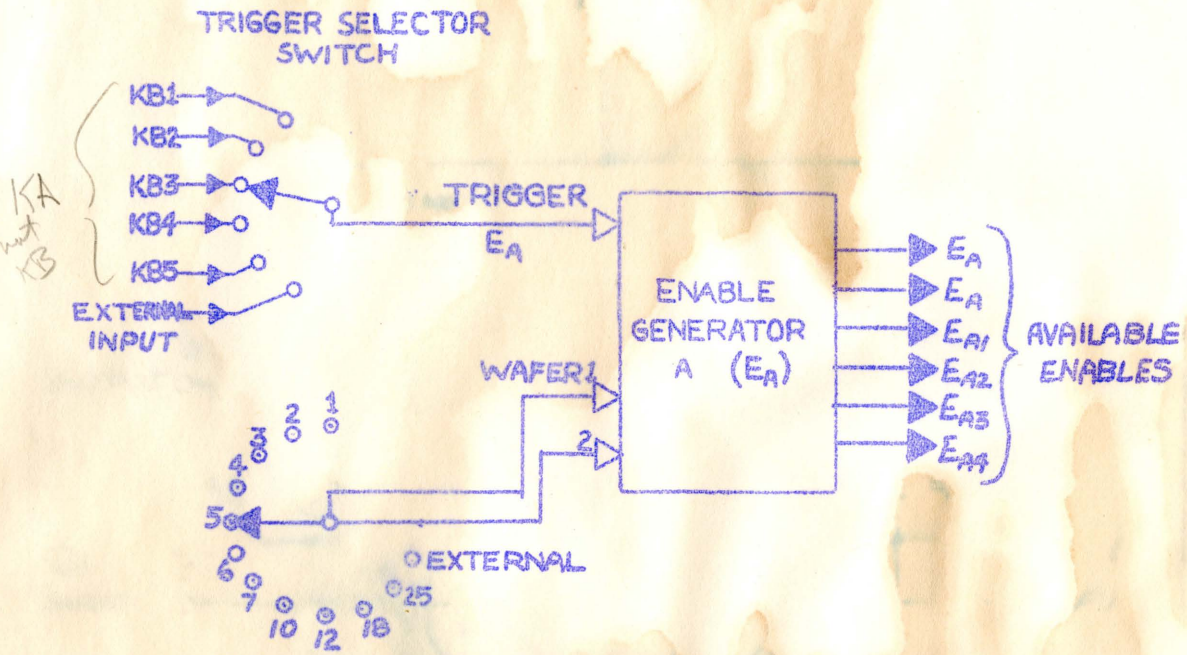



CAPACITORS IN $\mu\mu$fd. } UNLESS
RESISTORS IN K$\Omega$, ½W, 10% } NOTED

CATHODE FOLLOWER & NEGATOR - WISC

| DR. AKS | ENG. AKS | Date 6/26/56 |
|---|---|---|
| Dwg. No W-024S,L-02A | | |




| WIDTH SELECTOR SETTING | WIDTH SELECTOR SWITCH CONNECTIONS | |
|---|---|---|
| | WAFER 1 | WAFER 2 |
| 1 | KB1 | 1 |
| 2 | KB1 | 1 |
| 3 | KB2 | 1 |
| 4 | KB1 | KB2 |
| 5 | KB3 | 1 |
| 6 | KB3 | KB1 |
| 7 | KB3 | KB2 |
| 10 | KB4 | KB1 |
| 12 | KB4 | KB1 • KB2 |
| 18 | KB5 | KB1 |
| 25 | KB5 | KB4 |
| EXTERNAL | EXTERNAL | EXTERNAL |