III BASIC ENGINEERING DESIGN

A Underlying Philosophy of Design

The design of a large scale complex piece of electronic equipment such as a digital computer is an undertaking of no small proportion. As has been stated, almost innumerable possibilities exist in the field of circuit design when only the logical function a circuit is to perform is specified. It became apparent quite early in the design of the WISC that some type of "guideposts" should be established, insofar as circuit design was concerned. Such guideposts were not set forth as specifications nor were they intended to be so binding as to unduly restrict the freedom of choice in the design of circuits.

One of the first of these was the decision to build up the larger logical sections using only basic circuits (gates, flip-flops, etc.) and methods of coupling which had been tested for reliability as thoroughly as possible. This in itself is a far from new approach to such a problem, but can be easily overlooked under circumstances which exist where a major aspect of a problem is its educational value. Such a procedure functions also to greatly reduce the necessary "bread-boarding" which is such an inherent part of electronic circuit design.

A second such guide to design concerns the matter of reliability. One of the desirable aspects of the WISC was to be its small size and greatly reduced number of vacuum tubes. This is obviously a desirable feature in almost any such machine. However, this characteristic is, in many respects, incompatible with the unquestionable need for reliability in a computing machine. It was felt, therefore, that where any decision had to be made between these two features, the choice was to go on the side of reliability if the more reliable choice could be determined. This latter matter may seem superficial, but just such decisions have had to be made in cases where the "reliability factor" (as is usual) could not be measured in any sort of quantitative way, while the number of tubes involved was in the hundreds.

Another of the fundamental design requirements concerns the use of energy storing circuit components, primarily capacitors. To build a machine completely devoid of both inductors and capacitors, would solve a large number of problems before they had arisen. Unfortunately, this is not possible in the WISC*, at least without greatly increasing the size of the machine. The reason behind the desire to avoid energy storage components and their consequent resonances or time constants lies in the nature of the signals which exist in computers. The periodicity with which sequences of "ones" and "zeros" may occur in a calculation cannot be predicted. Because of this fact, capacitor and transformer coupling of any kind, if used, must be used with care. This precaution is taken in the WISC, in most cases by making any time constants well below 10 microseconds, and by making certain that any inductive elements are critically damped or operate in such a manner that they cannot be driven at resonant frequency by any possible type of signal which might be encountered.

Methods of coupling from a flip-flop or gate into another

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*A close approach to this is accomplished in the ILLIAC and ORDVAC machines.

flip-flop have been quite thoroughly examined. This coupling is directly into the grid circuit junction via small capacitors. It has been made the practice to avoid simultaneous pulsing of both grids, even though the "speed-up" capacitors can usually be relied upon in such a case to insure reversal of the state of the flip-flop. Coupling from one flip-flop to another is done also by capacitors (or diodes in the case of a counter). This has resulted in operation considered as satisfactory, although it is felt that transferring information via a gate is probably more reliable. This compromise has been made in view of the great simplicity of numerous circuits which is gained thereby.

Another detail of circuit operation which has been avoided in the logical planning is the controlling of a gate by a gate enabling voltage which is subject to change during the same "clock" pulse time that the gate is pulsed. To avoid this "pitfall" is a matter that requires a constant state of alertness. Its importance, however, cannot be overestimated. Such operation results in sub-standard gate output pulses. It also results frequently in operation which appears superficially satisfactory, but is in actuality causing a digit-time shift in the information timing or "losing" a digit at infrequent intervals.

A case in which this just-mentioned type of operation may prove reliable, although it still to be avoided if possible, is in the "suicide" type of circuit. If a flip-flop in a given state controls a gate in such a way that it opens the gate to passage of a pulse that will reverse the state of the flip-flop, so called suicide operation results. If the pulse does not pass, the flip-flop will remain in the state which permits it to pass. If it does pass, the flip-flop will be reversed in state. Such a paradox is seemingly resolved only by a sufficient portion of the pulse being passed to effect the desired change in state of the flip-flop.

B Gates & Switches

Those circuits which can be classed under the bread heading of "gates and switches" comprise one of the groups of basic sub-elements which are vital to digital information handling. The distinction between a "gate" and a "switch" is not a clear one, if there is, indeed, any distinction at all. If any differentiation is to be made, a "gate" might be defined as a circuit analogous to a single-pole single-throw switch, while a "switch" can be considered as a circuit which is analogous to a single- or multi-pole multi-throw switch.

For present purposes, only the capabilities and types of inputs and outputs of the gates and switches will be discussed. A good deal of research has gone into testing of various types of gates, and, although far from all the possibilities have been explored, several basic gates have been selected which, to date, have proven satisfactory for use in the design of final circuits for the WISC.* These fall into two major classes, namely pulsed gates and "d-c" gates.

The pulsed gates are primarily for the purpose of controlling the basic 1-microsecond clock pulses. The various types of these gates consist, for the most part, of a basic triode circuit.

*This subject is covered more thoroughly in a digital computer internal report by A. K. Scidmore, dated December 9, 1953.

This circuit is in the form of a cathode-pulsed gate with up to 3 inputs to the control grid. This gate is shown schematically in figure 3. A great deal of versatility as well as economy in number of tubes is obtained by having 3 inputs to a single grid. Input coupling is made directly from flip-flop (or equivalent circuit) plates through 100 kilohm resistors to the gate grid. The output consists of negative 30-volt 1-microsecond pulses, at a d-c voltage level of 250 volts positive. The output impedance, during pulsing, is approximately 1700 ohms. The gate is logically a 3-input "and" gate, although the complement information in the controlling "flip-flops" can be used which results in a 3-input "or" gate. Greater versatility can be obtained with this gate if two are cascaded with an impedance transformation from the first plate to the second cathode as shown in figure 4. This gives a six-input "and" or "or" gate, or by using various inputs, a large number of "and-or" possibilities. Up to three of these gates in cascade have been tested with no objectionable deterioration in the output pulse, but the maximum possible number has not been ascertained at this writing.

Where the inputs to several of these gates are mutually exclusive, an additional logical "or" can be achieved by using a common output resistor. This provides added flexibility in assembling logical "and-or" pyramids. Another common use of several gates with a common output resistor is to provide, in conjunction with flip-flops, assemblies which, under our previous definition, can be called switches. Examples of such switching circuits are shown in figure 5. Each possible combination of flip-flop settings connects a different input to the switch output.

The "d-c" class of gates is so called since the output is a function of the grid inputs only and does not convert the "d-c" input to a pulse or train of pulses at the output. The output may remain high or low for as short a time as 6 microseconds or for an indefinitely long period of time. Such a gate, to permit ease of logical pyramiding, must have an output which is essentially the same in voltage range as any one of its inputs. The logical function is achieved primarily by means of crystal diodes, and the "impedance match" by use of the tube sections. Several types of such gates are shown in figure 6.

CCCCCCC) Flip-Flops

Another basic circuit used to a great extent in digital computer circuits is the Eccles-Jordan "flip-flop" or bistable multivibrater circuit. This circuit because of the manner in which it operates is also frequently called a "toggle." The "flip-flop" can be and is used in a variety of different ways, depending on how it is connected into a circuit. Two devices of which it is a component, namely the binary counter and the shift register, are described in greater detail in the next section of this thesis. Other uses include information storage, pulse-to-static signal transformation, and gate and switching control. An example of this latter use is shown in figure 5 in the section discussing gates and switches. Much advantage is taken of these last three uses in the assembly of the order interpreter unit for the WISC.

Much has been written on the original Eccles-Jordan circuit and numerous modifications and variations of it. No effort will

be made here to do other than describe the characteristics of the circuit used in the WISC. This circuit is shown in schematic form in figure 7.

As the figure shows, cross-coupling "speed-up" capacitors are used. These capacitors, when used on a flip-flop circuit, have several effects. One of these, as has been implied, is to speed up the transition of the circuit from one stable state to the other. This is the primary reason that they are used in the WISC, since the flip-flop must be capable of controlling a gate or switch within 3 microseconds after receiving a trigger pulse. This length of time is, by comparison with those of many flip-flop applications in present computing machines, a relatively long time. However, since the basic clock pulse rate of the WISC permits it, a simple circuit is used with comparatively high grid circuit impedances and triodes rather than pentodes. While it achieves no small economy in number of tubes and power supply requirements, the use of triodes instead of pentodes increases the transition time.

Another function of these capacitors, which is not as obvious, is their action as a transient "memory". This effect more-or-less insures that when the circuit is pulsed either bilaterally, as in a counter, or on the conducting grid only, it will change to the opposite state. This is caused by the charge unbalance in these capacitors when a flip-flop is in the steady state condition, which is such that when triggered the circuit is driven to the opposite stat. This method of driving a flip-flop requires, at least when bi-laterally driven, that the trigger pulse be of short duration compared to the time constant of the charge and discharge path of the "speed-up" capacitors. If such capacitors are not used it becomes almost mandatory, to obtain reliable operation, that the flip-flop be unilaterally driven or else set to the desired condition with a pulse or control voltage of long duration compared to the transient time of the flip-flop circuit.

After delineating some of the advantages of cross-coupling capacitors on the flip-flop circuits used in the WISC, it would be well to mention some of the disadvantages. One of the difficulties caused by these capacitors is the addition of an RC time constant in the grid circuit. This time constant is, for the WISC flip-flop, the longest of any RC time constants present insofar as recovery time is concerned. Unless the transient capacitor discharge has become negligible by the time another initiating pulse occurs, a somewhat larger pulse will be required to reverse the state of the flip-flop. This can be seen in figure 8. Another of the results obtained by addition of these capacitors is a greater sensitivity of the flip-flop in its response to input pulses. This can be either good or bad depending on the point of view, since certainly it is desirable that the circuit respond when a pulse is applied but just as desirable that the circuit does not respond to extraneous pick-up or other such undesired signals. This latter problem is affected further by the size of the series grid resistors used. The larger these resistors, the less sensitive the flip-flop becomes.

These series grid resistors are primarily used, however,

for a different purpose which is suppression of parasitic oscillation within the flip-flop circuit. No detailed study has at this time been made with regard to parasitic oscillations, other than observation of effects which were most undesirable and could be explained only by the apparent presence of such oscillations. Series grid resistors removed these undesirable effects.

D Binary Counters

Two somewhat more complicated circuits which are sufficiently basic to merit special mention are the binary counter and the shift register. These both consist largely of flip-flop circuits with appropriate coupling. The first of these, the binary counter, will be discussed in this section of the thesis, shift registers being covered in the section immediately following.

The vacuum tube type of binary counter consists of a series chain of flip-flops so connected that a change of state from the arbitrarily designated "zero" condition to the opposite or "one" condition causes no change to the next or any other following stage, while a change in state from the "one" condition to the "zero" condition will cause the next following flip-flop stage to reverse its state regardless of whether it contains a "one" or a "zero". It is apparent, then, that whatever system is used, the input coupling to a stage must be bilateral or balanced, such that the input paths to the two grids are essentially the same and the necessary gating or screening of the input pulse so as to cause the flip-flop to reverse state is accomplished by means of potentials existing in the circuit which are caused by the driven flip-flop itself. Many methods have been used to accomplish this, ranging from direct capacitor coupling which relies on the various capacitor charge unbalances to achieve correct operation, to a dual register counter using 4 gates per stage.* The general rule of "more complex more reliable" seems to hold among these variations, and the circuit which it is hoped was an optimum choice for the WISC is shown in figure 9.

This circuit consists of an RC differentiating network coupled from the "ones" plate resistor of the preceding flip-flop to "ground". The differentiated output pulses connect to the cathodes of two germanium diodes. The anodes of these diodes connect directly to the grid circuit junction points of the flip-flops. The input to the first flip-flop stage consists of the same type of coupling except that the differentiating resistor is not necessary if the input consists of negative pulses, since no differentiating is needed. The input capacitor is usually required since, in general, it is necessary to remove the d-c voltage level of the input pulses. The back resistance of the diodes is adequate to maintain the i.;t d-e voltages at the correct level.

A re-examination of the requirements of a counter will show that when several consecutive stages including the first stage all contain a "one", receipt of another pulse at the input will cause all these stages, as well as the first stage which contains a "zero" to reverse their states. These changes cannot occur simultaneously, since the change of one stage must be sufficiently

*Ware, W. H., The Logical Principles of a New Kind of Binary Counter, Proceedings of the I.R.E. 10:1429-37, October 1953.

underway to have generated enough of an output pulse to initiate action in the following stage. This causes a "ripple" of operation down the counter chain that is, in actuality, the "carry". When the carry travels the entire length of a given counter chain (which may be of arbitrary length) the result is a definite delay between the receipt of the initiating pulse and the transition of the final stage in the counter chain. This delay, in the WISC counter circuit, is approximately 0.2 microseconds per stage.

Considering the matter of this delay from the viewpoint of logical design there are two aspects to be pointed out. First there is the disadvantage that if the final stage is to control a gate or switch pulsed with the set of digit pulses next following the set used to pulse the counter, the counter delay reduces the time available for the gate input to reach its steady state value. Secondly, and more on the advantage side, it permits an output or final flip-flop stage of a four- (or more) stage counter chain to control its own input, since a 1-microsecond input pulse is terminated by the time the output responds. This tpe of control might be used, for example, when it is desired to stop a counter on the all "zero" or reset position. Since this example would be a "suicide" type of circuit (by our previous definition) it would probably operate satisfactorily with a single counter stage. The advantage of the delay still exists for the greater-than-four case pointed out, however, since the control under these circumstances might also start or stop other operations pulsed at the same time as the counter.

E Shift Registers

The second type of cascaded flip-flop chain, the shift register, differs fundamentally from the counter in its operation. In this case, the flip-flops are so connected that, upon receipt of a control pulse or pulses, any given flip-flop assumes the state of the flip-flop preceding it. It is apparent, then, that each flip-flop must, in some manner, pass the information it contains to the flip-flop which follows it in the chain.

The shift register is highly useful and consequently a much used component of digital computers. Its types vary over quite a wide range. Some are unilateral and some bilateral, the latter to permit shifting either direction. Some are constructed of vacuum tOes whOe newer types are made of ferrite cores* or transistors*. Some are single register and others are dual register. Some are simultaneously pulsed and others sequentially pulsed.

Uses of shift registers, just as their types, are many and varied. They are used as storage devices or as delay units. They are used for shifting of information such as is required of the operands in some arithmetical manipulations. They are used for serial-to-parallel and parallel-to-serial information conversion.

The requirements of a shift register pose a somewhat greater problem in circuit design than a binary counter, at least so far as simplicity of design is concerned. The source of this difficulty lies in the fact that whereas a counter stage is never called upon to change its state unless the preceding stage changes, a shift register stage may be required to change state whether

*See references 4 and 5.

the preceding stage changes or not, and, in addition, either or both of these changes, if they occur, may be from a "one" to a "zero" state or vice-versa. This creates a problem inasmuch as no clear-cut output can be obtained from a stage, if it does not change state, by which the following stage can be set to the correct position. In a sequentially pulsed register, this problem causes no great difficulty since the stages can be sequentially set to the "zero" (or "one") position. This reduces the need of information from the preceding stage to the case in which it is a "one" (or "zero") only and this information is easily obtained when the preceding stage is later pulsed to the "zero" (or" "one") state. Such a register is, however, not usually desirable, since it requires a comparatively large amount of time to accomplish a shift of one place (although the shifting of more than one place can be going on at the same time) and because of the need for a rather elaborate source of sequential pulses and consequent excessive number of connections.

If simultaneous pulsing is used and all stages are set to the "zero" position at once, the information contained in the register is destroyed. Numerous ways have been devised to get around this difficulty. In almost all cases of simultaneously pulsed registers this is done by providing a "transient" storage of some sort. This storage can, in the simplest case, be a resistor-capacitor combination, or, in more complex circuits, delay line sections or an additional register. In all cases the principle is essentially the same. The register may be set to "zero" and all "ones" information is held in the "transient" storage sufficiently long to permit the stages to recover after which the "ones" information enters the stage following that which previously contained it. In the case of R-C or delay line storage, the time of storage is, of necessity, short. If an alternate register is used, the recovery time of the register can be arbitrarily long (disregarding other machine considerations) after which the information is pulsed back in a manner similar to that which it was pulsed in. Maximum versatility can be obtained if the information is "gated" back and forth between two registers, this being almost a necessity if bi-directional shifting is to be accomplished.

The shift registers decided on for use in the WISC are of two types. Both are uni-directional vacuum tube registers and use capacitor coupling between stages. One is a dual register with information pulsed to the temporary register with one set of digit pulses and pulsed back again with the next following set, leaving the information available for sampling with the third set of digit pulses. This type of register, while not absolutely necessary, simplifies the switching requirements where information may have to be "picked off" from any one of several stages while it is 32.ng shifted.

The other type of register, which is satisfactory for use as storage or for serial to parallel conversion, operates partly sequentially and partly simultaneously. Since a "three phase" pulse system is used in the WISC, three flip-flops can be pulsed sequentially during one digit time. Such a three-stage register only shifts two different bits of information, since upon

completion of the third pulse two stages contain the same information. Connecting a series of such registers and pulsing these all simultaneously results in a register of arbitrary length which can accomplish one shift per digit time with roughly a 25 per cent reduction in the number of flip-flop stages required. The "idle" stage in each group of three provides the "transient" storage required for simultaneous pulsing operation.

To permit cascade connection of shift register units, the output must be such that the phasing is correct to connect to the input of the same or other shift registers. This may require additional stages to obtain correct phasing, especially if a switch is used. In the case of the subdivision of registers used in the WISC this is indeed the case, although only 19 flip-flop stages are required for a register which handles 12 bits.

The "subdivision" of the shift registers mentioned in the preceding paragraph refers to the length of the registers, measured in number of digits, between input and output terminations. The units for the WISC are comprised almost entirely of 5 or 7 stages. These values are advantageous for several reasons. In an order, the addresses consist of 5 digits of "time" information (position on the drum periphery) and seven digits of track information. Since these two different types of information must be handled in different manners, it is advantageous to be able to switch them separately. A five- and a seven-stage register in cascade are then also terminated and it is possible to separately switch an entire address. Appropriate choices of 7 and 5 also will permit registers of 40 digits (significant digits of a number), 50 digits (word length), 55 digits (minor cycle), 10 digits (exponent and sign information), and 14 digits (order type and extract information).

A slight disadvantage of the WISC registers using the "sequential-simultaneous" pulsing is that two shift enabling control voltages are required to operate the registers. As has been pointed out, it is not advisable to attempt to control a gate with a control voltage which is changed at the same time as its cathode is pulsed. This necessitates the use of a gate enabling voltage to open the input gate to the register which enabling voltage occurs at a different time than the shift enabling voltage that starts and stops the pulses causing the shifting operation. There is more than one possible choice of this timing, but the one which is used on the WISC registers is a shift enable which starts and terminates two digit phases (6-2/3 microseconds) before the input gate or switch enable. The duration of these voltages, of course, is dependent on the switching operation being performed.

The requirement just mentioned will complicate to some extent the design of the order decoder and control unit, since all switching controls for the shift registers will have to be of this dual nature.

There are two logical requirements which must be borne in mind with regard to the "sequential simultaneous" shift registers. One of these, which is disadvantageous, is that information cannot be obtained in parallel from a register while it is shifting (unless suitable gating using two different sample pulses is used)

since the information is not static in all stages at once during any of three possible sample times. The other, which is advantageous, concerns input-output timing. The terminations are made in such a manner that the output of a register can be connected to its own input. When this is done directly, the first stage operates the same as all other stages and contains information for 2 of the 3 phase times of a complete digit time. If no effort is made to obtain information in parallel during shifting, it is only necessary that the first stage hold information for 1 phase time which permits the additional phase time to be used in some other way (i.e. in generating the sum digit in an adder) with there still being time to circulate the new number back into the register with the same duration shift enable voltage.

Figures 10 and 11 show, respectively, the wave shapes and the circuit diagram of a "sequential-simultaneous" shift register.

F Recirculators

A serial machine with a cyclic storage has a need for a temporary storage of some kind. There are several reasons for this need, perhaps the most obvious being the necessity for having the two operands at the same time to perform arithmetic. Since the operands, in general, are not available simultaneously from the standard memory, one or both of them must be stored temporarily in some manner until the second is available. This may be done in various ways such as with shift registers or, especially in a single address machine with one or more accumulators.

From the time of its original inception, this short memory requirement of the WISC has been planned for by the use of recirculators. These units, as used on the WISC, are partially electronic and partially mechanical, the latter part being actually an integral part of the drum. It consists, in essence, of a "dual" head mounted on a single track, the distance along the drum periphery between the two heads being something less than the desired storage time. This storage time is ordinarily either 55 digits or 44 digits, the first being a minor memory cycle and the second being a minor arithmetic cycle. "Something less than", as used above, refers to the fact that there is some delay in the "write in-read out" process which can be allowed for by decreasing the mechanical separation of the heads. It is also desirable in some cases, especially where the use of a recirculator in the arithmetic section is concerned, to be able to shift a number. By making the recirculation time shorter or longer than a word time by a whole number of digits, a shift of the digits occurs each time one minor cycle is completed. This shift is with respect to a number being recirculated with a period of exactly one word time. To be able to process either direction when shifting, it is necessary that a recirculator span be less than a word length by the maximum number of digit times it is desired to shift in one minor cycle in addition to the delay already mentioned.

With this reduced span, it is necessary to use additional shift register stages in a complete recirculator loop to make the total recirculation time equal to one word length, or, to shift either direction, one word length plus the number of digits per revolution it desired to be able to shift.

A complete recirculator loop, then, is made up of a writing head, a circumferential distance along the drum surface (the span), a reading head, an amplifier and reclocking gate, an appropriate number of shift register stages, one or more switch gates, and a writing amplifier which connects to the already mentioned writing head. This is shown diagramatically in figure 12.

No attempt will be made in this thesis to cover the subject of magnetic drum reading and writing, since space does not permit. A brief mention should be made, however, of the "reclocking" gate mentioned in the preceding paragraph. When a single signal is written on the drum, a "spreading" occurs which causes the output signal to be of longer duration than the original writing pulse. This, in itself, would cause no great trouble except for the fact that this "spreading" of the signal, at the repetition rate used, is limited by the presence of adjacent digits and as a result neither the leading nor the trailing edge of the output pulse will be fixed in time for all different combinations of adjacent "one" or "zero" signals. This requires that the output of the reading amplifier be reclocked to obtain output pulses or enabling voltages which are synchronized with one of the phases of digit pulses. It should be remarked that there are other reasons for this reclocking, and it is even more necessary in connection with standard memory reading than in recirculator reading. This reclocking is accomplished by using a reading amplifier output suitable for use as a gate enable, and using it as such.

The recirculators also make another desirable feature easy to obtain. As was pointed out in a previous section, more-or-le o unavoidable delays occur at various places in the course of information flow through the machiiiiine. If successive processing of a word or order is not to result in the information being shifted to a later and later position in time, these delays must be compensated for in some way. Since the input and output are essentially terminations, a delay in time causes no trouble. Wherever the information is in such a place that it can be in some way recirculated within the machine, it must be kept within certain limits insofar as time position is concerned. This latter type of circulation cannot proceed very far without the information passing through a recirculator, and this is where any delays which may have occurred can be compensated for. By taking information from an earlier stage of the shift register contained in the recirculator loop, the information is, in effect, shifted backwards in time by a number of digit times equal to the number of shift register stages*.

Logical requirements to be kept in mind in designing circuits in which a recirculator is used are relatively few. One such requirement is that the information be kept continually circulating as long as it is desired to preserve it. This type of storage is volatile and unless the information is kept circulating it will vanish. Another requirement, at least if shifting is to be possible, is that any shift registers in the loop be of the dual register type. A third requirement, in order to permit non-shift storage, is that* which of the pulses used to operate

*This obviously is not a case of negative time. What actually happens, of course, is that of the 55 digit times "wasted" each time the information recirculates only 55-n digit times are wasted on the final passage through the recirculator loop.

the shift register be at the same phase time as the pulses used to drive the writing amplifier. That is, the shift registers must be sampleable (or static) at the time a writing pulse is to be generated.

TO GEY 8TH HEXADECIMAL CHARACTER IN AN EXTRACT ORDER

NO. OF DIGITS TO EXTRACT

---STARTING AT BIT X
(FIRST DIGIT TO WRITE)

0-15	16-31	32-47	48-50	
0	1	2	3	0-15
4	5	6	7	16-31
8	9	A	B	32-47
C	D	E	F	48-50

10^{th} OR 9^{th}	CHARACTER	NUMBER OF DIGITS TO EXTRACT FIRST DIGIT TO WRITE		
0	0	16	32	48
1	1	17	33	49
2	2	18	34	50
3	3	19	35	
4	4	20	36	
5	5	21	37	
6	6	22	38	
7	7	23	39	
8	8	24	40	
9	9	25	41	
a	10	26	42	
b	11	27	43	
c	12	28	44	
d	13	29	45	
e	14	30	46	
f	15	31	47	