

## UNIVERSAL HIGH-SPEED DIGITAL COMPUTERS: A SMALL-SCALE EXPERIMENTAL MACHINE

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### SUMMARY

An experimental electronic computing machine has been constructed, using the serial binary-digital system of number representation. The principle of its operation is explained by means of an analogy; and its design and construction are described in detail. Although the machine is small in size, it has been designed with a view to expansion, and will then be intrinsically capable of performing any computation automatically.

### (1) INTRODUCTION

Science and engineering rely to an increasing extent on computation as a means of making the fullest possible use of existing knowledge; if normal methods of computation are employed, the solution of a problem may require months of uninteresting and, to a great extent, purely mechanical work by human computers. The mechanical nature of the work gave rise to the idea of automatic computing machines. There is nothing new in this idea, for the construction of an automatic computing machine was proposed by Charles Babbage<sup>1</sup> as long ago as 1864. Babbage's machine was to contain a "mill," where arithmetical operations were performed on data drawn from the "store." He realized that it is not sufficient to provide equipment which is merely capable of performing arithmetical operations on numbers fed to it by a human being; it is desirable that the machine should undertake the whole of a computation, consisting of a very large number of such operations, on a variety of different numbers. Furthermore, the amount of human intervention required should be confined to formulating, at the start, a plan for the computation and taking note, at the finish, of the answer.

The machine must, therefore, have automatic access to its operating instructions and to the numbers with which they are concerned, so that a storage system is essential. The store must hold a large quantity of information, in order to allow of lengthy computation without reference to the human operator, and it must preferably permit of rapid access to any portion of such information in order to work much faster than a human computer.

Babbage's machine would be too slow in operation for most present-day needs, and, with this in mind, machines using electronic techniques have been constructed,<sup>2,3,4</sup> such as the Eniac. In this machine, ten double-triode valves were used to store each decimal digit, so that, although the machine contained 18 000 valves, the storage capacity was far too small for any except the restricted types of computation for which it was designed.

Thus the need for universal high-speed automatic computing machines has stimulated work on inexpensive storage-systems of large capacity, which allow access to the stored numbers at high speed. Two practical systems are the mercury delay-line

Written contributions on papers published without being read at meetings are invited for consideration with a view to publication.

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store<sup>5, 6, 7</sup> and the cathode-ray tube store,<sup>8, 11</sup> both of which have been used as the basis of working machines.

The paper describes an experimental computing machine built, primarily, to investigate the engineering problems involved in the use of the cathode-ray-tube storage-system mentioned above, and to subject the system to the most searching tests possible. The machine has been built on a small scale as regards storage capacity and complexity of computing circuits, and it can deal only with quite trivial computations.\* None the less, it is considered worthy of description, first, because the engineering and mathematical principles involved are the basis on which more complex machines have been designed, and secondly, because it is felt that those principles will be more readily grasped by the general reader if described in terms of the small machine.

Although it is possible to solve extremely complex mathematical problems with the aid of an enlarged machine of the type being considered, it will now be shown that no mathematical skill is required of the machine; all that is required is slavish obedience to the instructions which have been given to it by a human agency.

### (2) COMPUTING WITHOUT MATHEMATICAL SKILL

#### (2.1) The Basic Principle

If any computation is to be performed without the necessity for thought, the steps in the computation must be systematic and inflexible. \* Fig. 1 contains the outline of a system which makes this possible. It is convenient in the first instance, to forget the electronic character of the machine and to assume that the computation is to be performed by a human being, but one whose capabilities are restricted to those listed under "Facilities." The blocks marked Instructions (I), Numbers (N), Accumulator (A), and Control (C) may be treated as sheets of paper, the A and C sheets being initially blank and the instructions sheet bearing a list of instructions on separate numbered lines (I<sub>1</sub> to I<sub>j</sub>). The numbers sheet also has numbered lines (N<sub>1</sub> to N<sub>k</sub>), some containing numbers to be used in the computation and some to be used as working space.

Referring to the "rules," an external stimulus is needed to change the state of the human being from "quiescent" to "active," and thereafter operations 1, 2 and 3 are performed over and over again until facility 7 changes the state back to quiescent.

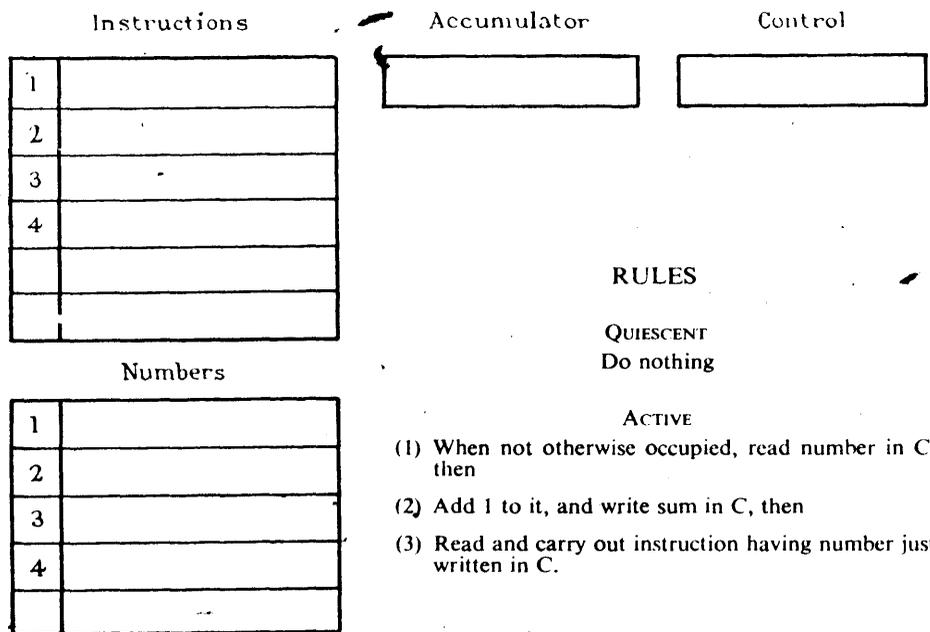
That a system of this kind can perform a calculation will be illustrated by an example.

#### (2.2) Example of a Simple Calculation

In the example chosen, it is required to determine the highest factor of an integer,  $x$ , the method being to divide  $x$  by integral trial factors which decrease successively by unity until one is found which gives zero remainder. The technique used for division is repeated subtraction of the divisor from the dividend. The necessary instructions (termed the programme) and numbers

\* The machine described in this paper was completed in June, 1948.

## WILLIAMS, KILBURN AND TOOTILL: UNIVERSAL HIGH-SPEED



## FACILITIES

- (1) A can be read, and written into any line in  $N_r N_r$ .
- (2)  $N_r$  can be read and written into C.
- (3)  $N_r$  can be read, and written into A.
- (4)  $N_r$  can be read, and added to what is in A, the sum being written in A.
- (5) As 4, but subtracted.
- (6) The number in A can be tested for sign, zero counting as positive; 1 is added to C if number is negative, no action being taken if number is positive.
- (7) The system can make itself quiescent.

N.B.—Reading does not erase the read quantity, but writing obliterates anything already present.

*Abbreviated form*  
 $a, N_r$   
 $N_r, C$   
 $n_r, A$   
 $a + n_r, A$   
 $a - n_r, A$   
 Test

Stop

Fig. 1.—Schematic illustrating the behaviour of the computer.

are tabulated in Fig. 2. Line  $N_1$  (numbers sheet, line 1) contains  $x$  and line  $N_2$  contains the initial trial factor,  $y_0$ , which may be  $(x - 1)$ .

When made active initially, the "human being" is "not otherwise occupied" and so, by rule 1, he reads the contents of C (denoted by  $c$ ), which are zero. Next, by rule 2, he adds 1 to this and writes the answer ( $c = 1$ ) in C, and finally, by rule 3, he performs the instruction so numbered,  $I_1$ . This results in the contents of  $N_1$  ( $= x$ ) being written in A, by facility 3. The contents of A at each step are shown in Fig. 2, and the line headed C symbolizes the behaviour of  $c$ . Rule 1 now applies again, so that  $c$  is again read ( $= 1$ ), 1 is added ( $c = 2$ ),  $I_2$  is performed (facility 5) and  $(x - y_0)$  appears in A. Rules 1 and 2 now put  $c$  equal to 3 and  $I_3$  is performed; this is a "test" (facility 6) to which the answer is "positive," since  $y_0$  is less than  $x$ . Hence, no action is taken, and, by the same process as before,  $I_4$  is next carried out (facility 2), resulting in a 1 being written in C. The next instruction is  $(1 + 1)$ , i.e.  $I_2$ , which leaves  $(x - y_0) - y_0 = (x - 2y_0)$  in A. If  $(x - 2y_0)$  is still positive, the next two instructions,  $I_3$  and  $I_4$ , will again recycle the process to  $I_2$ . This will continue until the contents of A (denoted by  $a$ ) become negative, say, after  $(r + 1)$  cycles, when they are  $x - (r + 1)y_0$ , just after performing  $I_2$  for the  $(r + 1)$ th time. The answer to the ensuing test,  $I_3$ , is "negative" for the first time, so that 1 is added to  $c$  and the next application of rule 2 yields 5 instead of 4. The next instruction to be obeyed is thus  $I_5$ ; the recycling instruction,  $I_4$ , has been omitted.

Instruction 5 adds  $y_0$  to  $a$ , giving  $a = (x - ry_0)$ . This

quantity cannot now be negative, since  $x - (r + 1)y_0$  was the first of these quantities to be negative. Instructions 6, 7, 8 and 9 check whether  $(x - ry_0)$  is zero or positive by

- (a) Placing 1 in line  $N_3$  for temporary storage, ( $I_6$ ).
- (b) Writing zero in A, ( $I_7$ ).
- (c) Subtracting  $(x - ry_0)$  from this, giving  $a - (x - ry_0)$ .
- (d) Testing the sign of this quantity ( $I_8$ ), which will be negative, except when it is zero, i.e. when  $y_0$  is a factor of  $x$ .

In general,  $y_0$  is not a factor of  $x$  and the negative result causes  $I_{10}$ , the "stop" instruction, to be omitted. The next instructions to be obeyed are 11, 12 and 13, which manufacture  $(y_0 - 1)$  and write it in  $N_2$  in place of  $y_0$ . Instruction 14 then writes 0 in C, and the whole process starts again with  $(y_0 - 1)$  as the new trial factor. It is clear that all the integers from  $y_0$  downwards will be tested, until, finally, one is found that is a factor, so that, after  $I_8$ , when  $a = 0$ , no action is taken by the subsequent test,  $I_9$ , and "stop" ( $I_{10}$ ) is reached for the first time. The highest factor of  $x$  will now be found in  $N_2$ ; it is the successful trial factor.

It has been demonstrated that a particular problem of arithmetic can be solved by slavish obedience to instructions in accordance with a simple basic rhythm. It is important to note the following points:

- (a) The necessary number of different types of instruction is small.
- (b) The number of instructions in the table of instructions is extremely small compared with the number of instructions

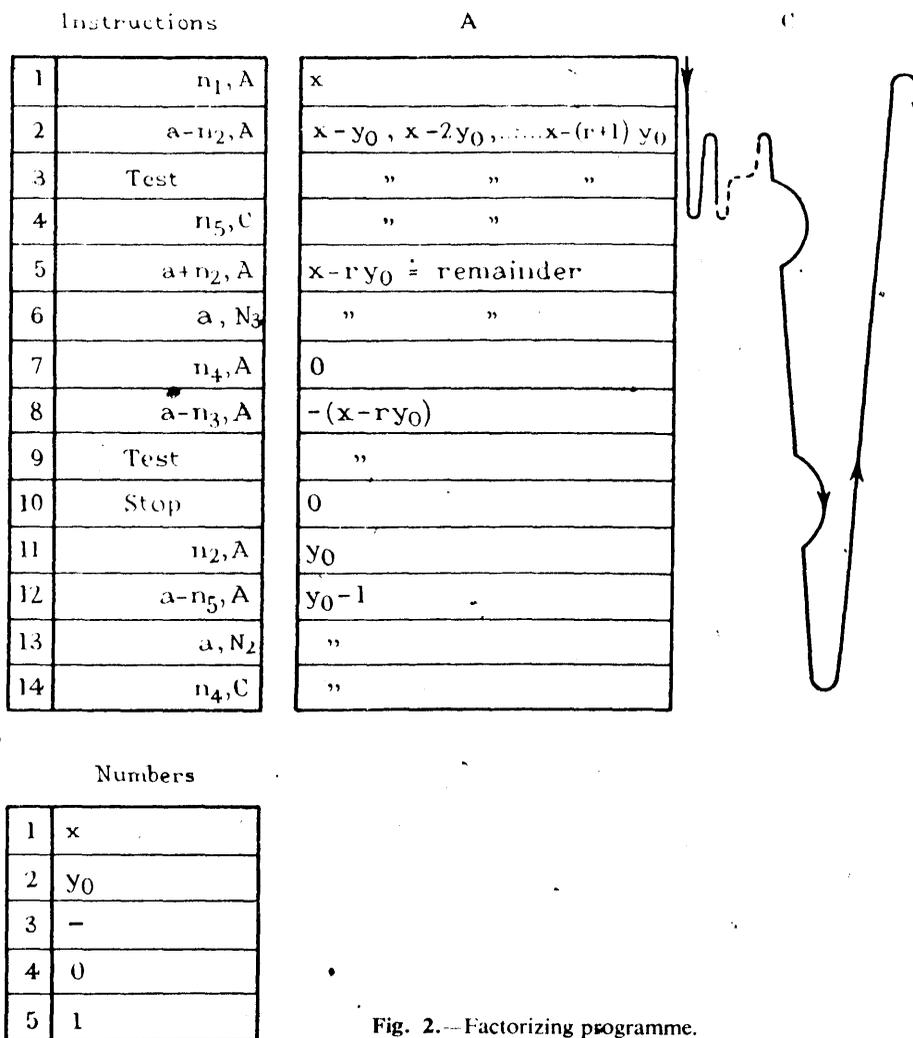


Fig. 2.—Factorizing programme.

obeyed in solving the problem, because of the recycling process provided by facility 2, which may set up a loop of instructions.

(c) The test facility supplies the necessary means of breaking out of these loops at the correct point in the computation.

(d) The facilities and the basic rhythm, whereby references to C alternate with carrying out the instructions, are the distinguishing features of the human being (or machine) performing the computation.

(e) The initial contents of I and N are the distinguishing features of the particular computation.

It will be seen that, if a different programme is supplied, the unthinking human being will proceed to perform a different computation without any alteration in the rhythm and facilities available for use. This is the reason for calling calculating systems of the above type "universal."

Furthermore, if the programme is left unchanged but different numbers are placed in lines  $N_1$  and  $N_2$ , the highest factor of the new contents of line  $N_1$  will be found. Each programme thus represents a "complex facility" analogous to those listed in Fig. 1, and can be made available by keeping it in an accessible "library."

The electronic equivalents of these operations are now described with particular reference to Fig. 1.

(3) THE ESSENTIALS OF THE MACHINE

(3.1) The Main Storage

The first step in constructing the machine is to replace the sheets of paper I, N, A and C, described in Section 2, by storage units. It is desirable to combine I and N into a single storage unit, called the Main Store (S) which will contain instructions, data and working space. This increases the flexibility of the machine, since instructions may be modified, by ordinary arithmetical processes under the control of other instructions, and thereafter used again as systematically different instructions. Another great advantage is that the total storage-capacity provided may be smaller, since large variations in the relative amount of storage space allotted to instructions and numbers may occur as between one problem and another.

There are therefore three distinct stores, S, A and C, within the machine, which are now described in the order mentioned. In describing S, a summary is given of the important external characteristics of the cathode-ray-tube storage-system on which the machine is based.<sup>8</sup>

The essential parts of the main storage are shown in Fig. 3. At the points in the gate circuit where numbers enter and leave the store—the "write" and "read" terminals, respectively—the

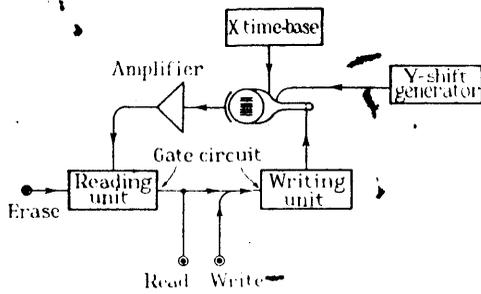


Fig. 3.—The main store, S.

data is represented in what is called "serial" or "dynamic" form by a train of 32 pulses, each pulse having either a standard amplitude or zero amplitude, representing a 32-digit number in the binary system of numbering. These pulse trains are related to the dash waveform, shown at (a) in Fig. 4, which consists of trains of 32 pulses alternating with gaps of 4 pulses' duration which serve to accommodate the flyback of the time-base and to separate numbers from their neighbours. The pulse instants of the dash waveform are numbered successively from 0 to 36.

The number itself is represented as at (b), where the dash pulses are used to define the digit positions of binary numbers. In any digit position, reproduction of a dash pulse represents "1," whereas failure to reproduce a dash pulse represents "0." Using these rules, the train (b) is interpreted as a binary number at (c).

For reasons associated with the computation processes, which will be explained later, it is essential that the first digit of any train shall represent the least significant digit of the number. There is thus, in Fig. 4, a conflict between the convention that

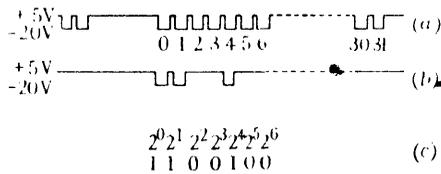


Fig. 4.—Representation of a number as a pulse train.  
 (a) Dash waveform.  
 (b) Pulse train representing a number.  
 (c) Binary number represented by (b) (19 in decimal notation).

time flows from left to right and the convention that the least significant digit of a number should appear on the right. Since this paper is concerned more with waveforms than with numbers, the waveform convention will be retained and the number convention rejected.

For ease of reference, each set of 32-dash pulses, together with the 4-digit space preceding it, is called a "beat." The time scale of the system allows 8.5 microsec (1 "digit period") for each digit, and, of these, 5 microsec are occupied by the digit pulse. A complete beat occupies 306 microsec, of which 34 microsec are blank.

The 32 digits of any number are stored as charge patterns on the cathode-ray-tube screen, on a line drawn out by the time-base, which flies back during the four blank periods ("black-out period") of each beat. The function of the Y-shift generator is to shift the line at right angles to its length to any one of 32 alternative positions, or "lines," corresponding with 32 different stored numbers. Successive beats are designated alternately "scan" and "action" beats, and are defined by a waveform called the "halver" waveform; during scan beats, the Y-shift generator

goes through the lines in ordered sequence, to regenerate the charge patterns on them before leakage has blurred them; during action beats, the Y-shift generator causes any chosen line to be swept, so that a number can be read out of it at the "read" terminal or written in via the "write" terminal; in either event the number has the form shown in Fig. 4(b).

During scan beats, the store regenerates the information it contains, because the number stored in the particular line that is being scanned appears at the "read" output-terminal of the gate-circuit expressed in the form shown in Fig. 4(b), and this "read" output-signal is used in the gate circuit for the purpose of immediately re-writing, and hence regenerating, the stored number.

When reading out of a line, the regeneration is not inhibited, so that the information is retained in the store; when writing in, the "read" output is caused to be zero, by inhibiting the first half of the gate-circuit by means of an "erase" waveform, and the new information supersedes the old.\*

Instructions are stored as two binary numbers. The first number selects the desired line or "address" in S by means of the Y-raster generator, whilst the second number selects one of the different types of operation listed under "Facilities" in Fig. 1. This latter number is called the "function number," and will consist of three binary digits, since there are less than eight functions.†

When considered as stored data, there is obviously no difference between a number and an instruction, since both are arrangements of 0's and 1's; the difference lies in the manner in which they are treated by the machine.

Now that the main-store has been considered, it is appropriate to discuss the computational section of the machine.

(3.2) The Accumulator

The Accumulator storage-tube (see Fig. 5) holds only one line, the X-scan being identical with that of the main store. The

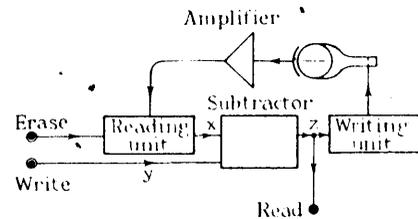


Fig. 5. The accumulator, A.

source of data on which computations are to be performed is, of course, the main store, and this data  $x$  in the figure is obtained from the "read" terminal of S, and applied to the "write" terminal of A.

In this small machine, the subtractor<sup>10</sup> indicated in the figure, is the only computing circuit associated with the accumulator, and the facilities available are ‡

(a)  $s_r$ , A. i.e. the negative of the number in line  $r$  is written in A. To achieve this, the erase waveform is used to eliminate any output from the reading unit, so that, as the store sweeps line  $S_r$  and the accumulator sweeps its single line, the digits from  $S_r$  are made available one by one at  $y$ , subtracted from 0, and the result recorded in the appropriate digit position in A.

(b)  $a - s_r$ , A. That is, the new number in A is to be the old one minus the content of line  $r$  of the store. This process is as

\* See Section 7.1.1.  
 † Instructions using Facilities 6 and 7 consist of a function number only.  
 ‡ Since N has been incorporated into S,  $N_r$  of Fig. 1 is now replaced by the more general  $S_r$ .

above, except that "erase" is not applied and the digits of the number in A become available at appropriate times, so that the digits arriving at y can be subtracted from them instead of from zero.

(c) a, S<sub>r</sub>. That is, the contents of A are to be written into the main store, line r. To do this, the "read" terminal of A is connected to the "write" input of the store which has been arranged to sweep line r. During this operation, nothing flows in at y.

It follows that facility 4 of Fig. 1 is not available; furthermore, facility 3 is replaced by facility (a) above.

These are disadvantages which cannot be overcome without additional apparatus, but which are easily circumvented by lengthening the programme. For example, if two numbers, x and y, stored in S<sub>1</sub> and S<sub>2</sub>, are to be added and their sum written in S<sub>3</sub>, the programme given in Table 1 can be employed.

Table 1

Instruction	Corresponding contents of A
s <sub>1</sub> , A	x
a, s <sub>2</sub> , A	x + y
a, S <sub>3</sub>	x + y
s <sub>3</sub> , A	x + y
a, S <sub>3</sub>	x + y

Thus, a subtractor can be used to perform additions.\* Since, in general, the converse is not true, a subtractor is preferred to an adder.

In the above discussion, it is implicit that, if the present contents of A are x and if y is applied to the "write" terminal, then z (x + y) appears in A. Thus, although z is being written in A, x must be delivered simultaneously by the reading circuit.\*

The representation of negative numbers which is used arises naturally: 32 digits are recorded for each number, digit r representing 2<sup>r</sup>, counting the initial digit as digit 0, so that digits representing powers of 2 higher than the 31st are not recorded. If a positive number, y, is subtracted from zero, the subtraction process will be cut short after digit 31 has been dealt with, so that the answer will appear as (2<sup>32</sup> - y).

If y = 2<sup>31</sup>, digit 31 of (2<sup>32</sup> - y) is 1. If the range of positive numbers represented is restricted to 0 ≤ y < (2<sup>31</sup> - 1), there is no ambiguity, and digit 31 becomes a sign-indicating digit; if it is 0, the number represented is positive, and, if it is 1, the representation is called the "complement" of the number and is interpreted as minus that number.

It is now necessary to organize the flow of data between S and A, and vice versa, as a result of instructions which are held in S and selected by Control.

(3.3) The Control

The Control storage-tube holds two lines (see Fig. 6), the X-scan being in synchronism with that of S and A and the two positions of the Y-shift being arranged to occur at appropriate times.

One line of C performs the function mentioned in Section 2.2, i.e. it contains a number, c, which is, in general, increased by unity after the previous instruction has been obeyed. Since, as described in Section 2, this number is used as an instruction to

\* See Section 7.1.2.

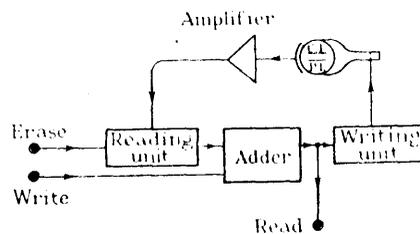


Fig. 6.—The control, C.

select the next instruction, it is called the "control instruction" and the line of C which holds it, is called the "C.I." line.

Having selected the next or "present instruction," it is found convenient to write it on the second or "P.I." line of C.\*

The present instruction is then obeyed. It is thus apparent that, in the automatic state, the operation of the machine may be divided into two similar stages. During stage 1, the contents of C.I. are used to select the present instruction from S and write it on the P.I. line; whilst during stage 2, the contents of P.I. are used to perform one of the elementary operations on an item of data. During both stages the "read" output of C (i.e. C.I. or P.I.) is the controlling factor. This output exerts its control over the machine via a unit called a "staticisor."

(3.4) The Staticisor

To each digit position of an instruction (C.I. or P.I.) is assigned a "staticisor unit" (see Section 7.2), and the assembly of such units is called "the staticisor." For ease of reference, the staticisor is split into two blocks, the "L staticisor" and the "F staticisor," which correspond with the address and function numbers of an instruction. The operation of the staticisor is such that it accepts the instruction in dynamic form from the "read" terminal of C and retains it in static form until it can be used.

The operation can, perhaps, best be understood in terms of the L staticisor. Here, the object is to choose some address, or line, of S. In Section 3.1 it was stated that during scan beats, the lines of S were scanned sequentially, and that, during the interleaved action-beats, chosen lines were scanned. In Fig. 7, the

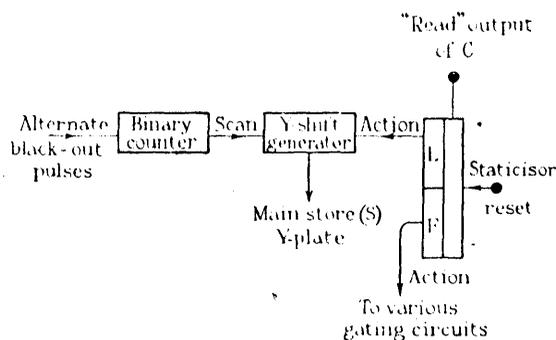


Fig. 7.—The staticisor

mechanism for the Y-scanning of S is shown schematically. During scan beats, control of the line of S which is scanned, is carried out by a binary counter (consisting of five stages), which is triggered every alternate blackout period,<sup>8</sup> whilst, during action beats, control is by the L staticisor. Throughout an action beat, the L staticisor must remain set to some chosen line-value obtained from the "read" terminal of C, but during scan beats, when control of the Y-shift generator has been switched to the

\* If the function number zero is made to correspond with the instruction s<sub>1</sub>, C, this occurs without special measures being needed. (See Section 4.3.)

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binary counter, it is permissible to change the setting of the L staticisor.

Similar remarks apply to the F staticisor, which, during an action beat, forces the machine into the configuration selected to permit or inhibit the flow of data along chosen channels.\*

One cycle of the operation of the staticisor may thus be summarized as follows:

(a) During a scan beat, accept the "read" output of C and retain it.

(b) During the following action beat, supply the information received during (a). At the end of this action beat, accept a re-trigger pulse and assume the zero configuration, in preparation for (a).

Supplied with the S, A and C systems and the staticisor, the machine now has the facilities of storing information, computing, orderly selection of the next instruction and a means of holding instructions in a form suitable for use when the opportunity arises (during action beats), and whilst waiting for this opportunity (during preceding scan beats).

To complete the essential framework of the machine it is necessary to cause it to carry out the rules of Fig. 1, by doing nothing when quiescent, and by executing an unvarying time-sequence, called the "rhythm," when active.

### (3.5) The Rhythm

The distinction between the quiescent and active states is made by generating a repetitive pulse, called a "pre-pulse," only when the machine is active. The "stop" instruction operates by inhibiting this pulse.†

When a pre-pulse is given, the standard rhythm occurs and persists until one "present" instruction has been obeyed. The time elapsing between pre-pulses is called a "bar." When the machine is active, a bar normally contains stages 1 and 2 of Section 3.3, during which C.I. and P.I., respectively, are obeyed. Since each of these instructions controls the machine via the staticisor, for which purpose a scan and an action beat are required, a bar contains four beats. The two scan beats are called S1 and S2, and the interleaved action-beats A1 and A2. The rhythm is indicated in Fig. 8(a). After the pre-pulse, Fig. 8(b), and during S1, unity, Fig. 8(c) (or two if a test instruction has revealed a negative content of A, it being convenient to add the "1" of facility 6 with the "1" of rule 2‡) is added to C.I., and the result is applied to the staticisor from the "read" terminal of C. During A1, as a result of C.I., the selected instruction is sent to the P.I. line of C, and at the end of A1, the staticisor is reset, Fig. 8(d). During S2, this present instruction is applied to the staticisor from the "read" terminal of C. During A2, some chosen line of S, and facility (Fig. 1) are called for by the staticisor, i.e. P.I. is obeyed. At the end of A2, the staticisor is again reset, the next pre-pulse is given and the cycle is repeated.

Key waveforms§ in the above rhythm are the "instruction-gate waveform," Fig. 8(e), which allows information to reach the staticisor from the "read" terminal of C only during the scan beats of a bar, the control Y-shift waveform, Fig. 8(f), which causes C.I. and P.I. to be scanned at the appropriate times and the action waveform, Fig. 8(g), which defines the action periods of a bar, A1 and A2.

In order to simplify testing the machine and correcting programmes, there are automatic and manual methods of generating the pre-pulse. The automatic operation of the machine has just been described. In manual operation, the length of the bar is determined by the human operator, who generates a pre-pulse by pressing a button.

When the button is pressed a single pre-pulse is generated at the

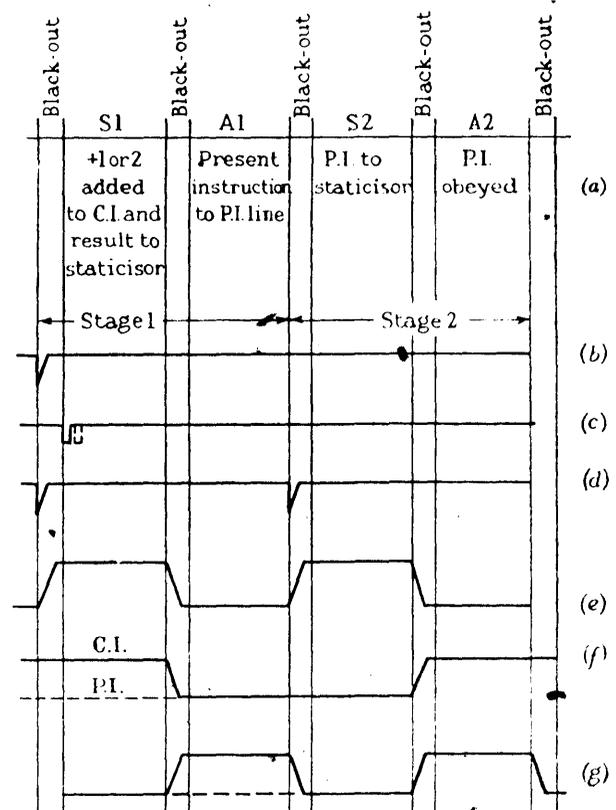


Fig. 8.—Rhythm waveforms.

- (a) The rhythm.  
 (b) Pre-pulse.  
 (c) +1 or +2 pulse.  
 (d) Staticisor reset pulse.  
 (e) Instruction-gate waveform.  
 (f) Control Y-shift waveform.  
 (g) Action waveform.

beginning of an S<sub>1</sub> beat, and this, in turn, initiates one cycle of the waveforms of Fig. 8; at the completion of this cycle the machine relapses into its quiescent state.

Every channel by which the information can flow between S, A, C and the staticisor is controlled either by the action waveform or by the instruction-gate waveform, and it is arranged that, in the quiescent state, all these channels are blocked but the information contained in S, A and C is regenerated. This quiescent state of the machine corresponds with the rule "do nothing" of Fig. 1.

The above general description of the machine is amplified by more detailed description in the following Sections.

## (4) THE CONSTRUCTION OF THE MACHINE

### (4.1) Requirements for Automatic Operation

Computations are built up from two types of transfer, namely from accumulator to store, termed an "inward transfer," and from store to accumulator or control, termed an "outward transfer." These are achieved (see Fig. 9) by means of connections from the A "read"-terminal to the S "write"-terminal via the Inward-Transfer Gate\* (I.T.G.), and from the S "read"-terminal to A and C "write"-terminals via the Outward-Transfer Gate\* (O.T.G.). The two transfer gates are necessary to prevent transfers occurring at the wrong times, such as during scan beats or during action beats when the instruction does not require them; they are therefore controlled by the F-staticisor and the "action" waveform.

\* See Section 4.3.  
 † See Section 7.5.

‡ See Section 7.3.  
 § See Section 7.4.

• See Section 7.7.

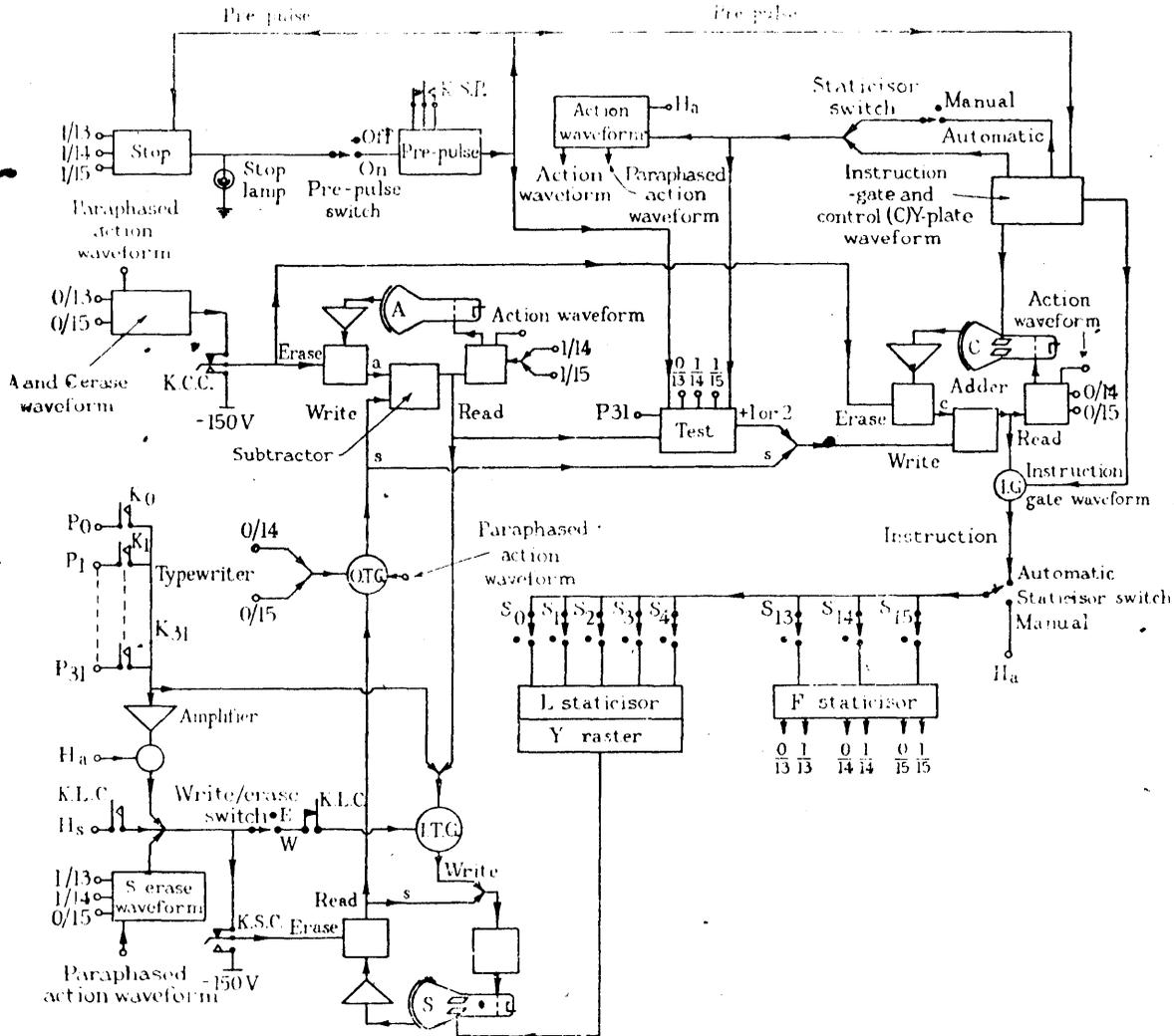


Fig. 9. Schematic of computer\*  
All switches are shown in the position for automatic operation.

The F-staticisor and "action" waveform also control the "erase"-waveform circuits,\* which are necessary whenever a writing operation is performed. The distinction between the facilities  $-s, A$  and  $(a-s), A$  is made by the erasing circuit, which can make  $a$  equal to zero. In a similar way, since writing from  $S$  to  $C$  is performed via the adder,<sup>10</sup> a new facility is introduced,  $(c+s), C$  by not erasing  $c$  during the writing process. This is merely an alternative means of altering the number in  $C$  for recycling (or other) purposes, but it offers advantages in many circumstances. In building up programmes, the relative position of an instruction may well be more important than its absolute position, so that relative alterations of the C.I., by adding positive or negative numbers, are often better than absolute changes. The writing operation is, however, always required during  $A1$  for the P.I.

The destination of information read from  $S$  is selected by the F-staticisor and "action" waveform, by blacking out either storage-tube  $A$  or  $C$ , whichever is not required.

In all instances, the F-staticisor affects the circuits which it controls via a "decoding valve,"† which responds only to certain

function-numbers; the decoding valve can deliver an output only during action beats of a bar, as determined by the "action" waveform.

The F-staticisor is controlled by digits 13, 14 and 15 for the following reason. The number of digits allotted to the address number must be sufficient to specify any line in the store. Although there are only 32 lines on the single storage-tube used in the small-scale machine, provision is made for using a store holding up to 8 192 numbers (262 144 digits), by allotting the first thirteen digits of the instruction number to the address number. If the present number of lines per storage tube (32) is not changed, the first five digits of the address number will specify the line (see Fig. 10) and the next eight digits will specify one storage-unit out of 256 units. The next digits are the function digits; in a more complicated machine, further function digits will be required to enable any one out of a large number of facilities to be specified.

In order to describe the operation of the other equipment represented in Fig. 9, the sequence of operations when an instruction is obeyed will be described in more detail.

When the pre-pulse switch is set to "off," defining the quiescent state of the machine, the pre-pulse circuit generates no pre-pulses so that the inward- and outward-transfer gates and the

\* See Section 7.7.  
† See Section 7.6. The decoding valve is replaced by diode coincidence-gates in the erasing circuits and the test circuit; this is for convenience and simplicity in the small-scale machine. The principle involved is the same.

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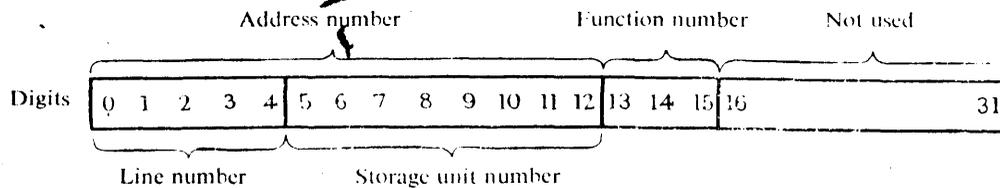


Fig. 10. Composition of an instruction.

instruction gate remain closed. This means that no new information can be written automatically into any of the three stores. The absence of pre-pulses also ensures that no erasing waveforms are generated. In this way, all the information in the stores is preserved, with the exception of the last contents of the P.I. line in the control, which are no longer required. A pre-pulse occurs as a result of depressing the "single pre-pulse" key, KSP, or of setting the pre-pulse switch to "on" when the "stop" flip-flop circuit is not operated. The pre-pulse occurs (see Fig. 8), and the "+1" or "+2" signal\* is emitted during a scan period, so that the outward-transfer gate is closed, and nothing except the "+1" or "+2" signal is applied to the "write" terminal of the control. The pre-pulse has also triggered the instruction-gate waveform circuit, so that the C.I. passes through the instruction gate and is applied to the staticisor if the staticisor switch is set to "automatic." During S1 therefore, the line staticisor is set to the line where the P.I. is located, and the function staticisor is set to 000. The S-erasing waveform circuit is not stimulated by the F-staticisor for this code, and remains quiescent during the following action-period, the P.I. appearing at the "read" terminal of S. The outward-transfer gate is open during this beat, and the P.I. passes to the "write" terminals of A and C. The decoding valve associated with A does not permit the cathode-ray-tube beam-current to be turned on for code 000, so that, although the complement of the P.I. appears at the output of the subtractor, it is not written in A. However, C is bright and the A-and-C-erase waveform circuit is operating, so the P.I. is written into C, on the P.I. line. The erasing waveform prevents the previous P.I. from being added in.

During S2, the P.I. emerges unchanged from C, since there is neither an input to the y terminal of the control adder from the outward-transfer gate which is closed during scan period nor a signal from the test circuit. The instruction gate is again opened, the L-staticisor is set to a data line and the F-staticisor is set to one of seven different codes. The mechanism of outward transfer has just been described with reference to the P.I.; for the inward transfer, A is brightened and the S-erase circuit operates to open the inward-transfer gate and inhibit the "read" output of S. It is not necessary, therefore, to close the outward-transfer gate to prevent an outward transfer.

The "test" and "stop" instructions do not involve any information from S, so they may be allowed to set the action-line, staticisor to any line, usually line 0. When the "test" instruction is obeyed, the function staticisor closes the outward-transfer gate during A2 and prepares a trigger circuit for the test flip-flop circuit during the last digit period of A2. At this instant, if the number stored in the accumulator is negative, its sign digit triggers the flip-flop circuit, which remains in the triggered condition during the S1 beat of the next bar and controls two gates, cutting off the usual "+1" signal and substituting a "+2" signal. The retriggering waveform must be generated by the next pre-pulse, since the flip-flop circuit must not be re-triggered during any intervening quiescent beats, such as may occur with manual operation. The action waveform trigger-pulses (see

Section 7.4) are suitable for this purpose; the first of these re-triggers the test flip-flop circuit at the end of S1, and the second has no effect.

When the "stop" instruction is obeyed, the F-staticisor triggers the "stop" flip-flop, but an outward transfer could still occur. It is desirable to prevent this, so the outward-transfer gate is again closed. Since automatic operation is under discussion, the pre-pulse switch is at "on," and the "stop" flip-flop circuit output is able to cut off the pre-pulses. Since the re-trigger pulse for the "stop" flip-flop circuit is the pre-pulse, a manual pre-pulse must be given before the machine may be restarted. When the "stop" flip-flop circuit operates, the "stop" lamp gives a visible signal.

Before a computation can be performed, the store must be loaded with the programme in binary-numerical code form, and with the data. The method used to do this was devised in order to use the minimum amount of equipment, and is consequently rather laborious. It suffices, however, to demonstrate the principles of the machine, and this is now described.

#### (4.2) Requirements for Manual Operation

The first step in loading the machine is to erase any old information, so the pre-pulse switch is set to "off" and the "store-clearing" key, KSC, operated, breaking the regenerative loop. All information is erased in about 20 millise (i.e. one raster regeneration-period), and the standard display of zeros is presented, whereupon the key is restored.

The staticisor switch is set to "manual." In this position, the halver waveform,  $H_n$ , which is at +5 volts during action periods and -60 volts during scan periods, simulates the number whose digits are all 1, during scan periods; any number may now be impressed on the staticisor by opening the appropriate switches S0 to S4 and S13 to S15,\* thus preventing the corresponding flip-flop circuits from triggering. In particular, any desired line of S may be selected, and it then remains selected during every action beat while the configuration of S0 to S4 is unchanged.

The "typewriter" is an array of 32 press-buttons, by means of which any single  $P_n$  pulse may be applied to the input of the inward-transfer gate. The typewriter output pulse also passes (during action beats only) to the circuit which is holding the inward-transfer gate closed, thus opening it at the correct instant to allow the digit to be written on the selected line. By this means, any number may be written, digit by digit, on a blank line. If it is desired to delete a digit, the "write/erase" switch is set to the "erase" position, so that the inward-transfer gate remains closed. The connection to the "erase" terminal of S now breaks the regenerative loop for one digit-period only. If it is desired to erase a whole line, the "line-clearing" key, KLC, is operated. This applies a negative erasing-voltage to S during action beats, so long as the key is held, so that none of the information on the action line is regenerated. If the KLC "break" contact, in series with the "write/erase" switch, were omitted, the erasing voltage could open the inward-transfer gate and allow the contents of the accumulator to be written on the selected line.

\* The "+1" and "+2" signals are pulses  $P_0$  and  $P_1$ , where  $P_n$  are repetitive waveforms which represent  $2^n$ , i.e. single dash pulses in the  $n$ th digit position.

\* They must be closed for automatic operation.

In order to start automatic computation, it is necessary to have the correct number on the C.I. line, so that the start is made at the right place in the programme. The simplest procedure is to draw up the programme so as to have the first instruction on line 1. If the "control-and-accumulator-clearing" key, KCC, is then operated and restored, zero is written on the C.I. line. The number fed to the staticisor during the S1 beat following the first pre-pulse is therefore 1, so that the first instruction is selected.

For the purpose of testing the machine, the switches S13, S14 and S15 are provided. Used in conjunction with S0-S4, these enable any instruction to be set up when the staticisor switch is in the manual position. The instruction can then be obeyed repetitively, with automatic pre-pulses, or just once, if KSP is used. Since the staticisor demands the required operation during every action period, it is necessary to modify the action waveform, as shown by the dotted line in Fig. 8(g), so as to make A2 the operative beat. If this were not done, the required operation would be performed twice for each pre-pulse, once during A1 and once during A2.

In order to complete the description of the machine, the design of the circuits used to interpret the instructions, will be described.

(4.3) The Allocation of Function Numbers

This machine performs seven different operations (during A2 beats), namely:

(0) The contents of any line in the store may be written in the C.I. line of control.

(1) The contents of any line in the store may be added to the contents of the C.I. line.

(2) The complement of the contents of any line in the store may be written in the accumulator.

(3) The contents of the accumulator may be written in any line in the store.

(4) The contents of any line in the store may be subtracted from the contents of the accumulator.

(6) The "test" may be performed.

(7) The "stop" circuit may be operated.

The distinction between operations 0 and 1, on the one hand, and 2 and 4, on the other, is made by cutting off the cathode-ray-tube beam current in one or other of the A and C stores, as described in Section 4.1. When either A or C has been selected in this way, the distinction between a writing operation (into which the existing contents of A or C do not enter) and a calculating operation, is made by the circuit which generates the erasing waveform. When a storage tube is not brightened, it is immaterial whether its erasing terminal is stimulated or not, and this makes it possible to common the erasing circuits of A and C [see Fig. 11(a)]. Operation 3 is the only one which demands that the inward-transfer gate be open and that the store-erasing-circuit should operate; hence, both these circuits may be controlled by the same waveform. Operations 6 and 7 require some means for preventing all transfers. Outward transfers can be prevented either by making the store-tube dark, or by closing the outward-transfer gate; inward transfers can occur only for operation 3. The alternative possibilities are summarized, for all operations, in Fig. 11(a). The "test" and "stop" circuits are not included in the Table, since it is obviously correct to make each circuit operate only for its own function number. It was decided to make the store

Circuit	Operation	0	1	2	3	4	6	7
		s. C	c + s. C	- s. A	a. S	a - s. A	Test	Stop
Store	C.R.T.	Bright	Bright	Bright	Bright	Bright	†	†
	Erase	No	No	No	Yes	No	*	*
Control	C.R.T.	Bright	Bright	Dark	—	Dark	—	—
	Erase	Yes	No	—	*	—	*	*
Accumulator	C.R.T.	Dark	Dark	Bright	Bright	Bright	Bright	—
	Erase	—	—	Yes	No	No	No	*
Transfer gates	Out	Open	Open	Open	—	Open	†	†
	In	—	—	Closed	Open	Closed	Closed	‡

(a)

— Immaterial.  
 \* Must not erase if tube bright, immaterial if tube dark.  
 † Either S data, or O.T.G. closed.  
 ‡ Closed if A and S bright, otherwise immaterial.

Circuit	Operation	0	1	2	3	4	6	7
		s. C	c + s. C	- s. A	a. S	a - s. S	Test	Stop
Control		Bright	Bright	Dark	Dark	Dark	Dark	Dark
Accumulator		Dark	Dark	Bright	Bright	Bright	Bright	Bright
A and C erase		Yes	No	Yes	No	No	No	No
O.T.G.		Open	Open	Open	Open	Open	Closed	Closed
I.T.G. open and S erase		No	No	No	Yes	No	No	No
Function number		000	100	010	110	001	011	111

(b)

Fig. 11.— The allocation of function numbers.

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cathode-ray tube bright for all functions; other decisions are summarized in Fig. 11(b). These remarks apply to A1 and A2 beats only; conditions during S1 and S2 beats, and during quiescent beats, were described in Section 3.5. Furthermore, during A1 beats, the operation is always controlled by the C.I., whose function number is zero.

A 3-digit function number could be allotted arbitrarily to each of these operations; seven decoding valves could be used, each to respond to one function-number. The outputs of these valves would then have to be combined by a buffer circuit, in order to operate, say, the A-and-C-erasing circuit for two different function numbers. A decoding valve can, however, be made to respond to 1, 2 or 4 function numbers by omitting connections from one or more of the sections of the function staticisor. For example, if the function numbers 000 and 010 are allotted to operations 0 and 2, then a decoding valve connected only to the 0 outputs of staticisor sections 13 and 15, will respond equally to both function numbers and can be used directly to control the A-and-C-erasing circuit. This technique of associating the decoding valve with one particular circuit instead of with one particular operation has been used because it eliminates the apparatus needed for the above-mentioned buffer circuits and makes a slight reduction in the number of decoding valves needed. It is thought that this will be true for larger computing machines with many more possible operations and function numbers, but, here, the disadvantage of the technique will become more obvious. Unless the number of operations which require a given circuit to work can be arranged to be a power of 2, function numbers will have to be wasted in order to make it up to a power of 2, by providing dummy operations. These may, however, already exist if the total number of operations that the machine can perform is not itself a power of 2.

Starting from the fact that the function number for operation 0 must be 000, the function numbers shown in the bottom row of Fig. 11(b) were allotted by trial and error.\* They result in the following requirements for the operation of circuits (during A1 and A2 only):

- (1) Control cathode-ray tube to be brightened when digits 14 and 15 are zero.
- (2) Accumulator to be darkened when digits 14 and 15 are zero.
- (3) A-and-C-erasing circuit to operate when digits 13 and 15 are zero.
- (4) Outward-transfer gate to close when digits 14 and 15 are unity.
- (5) S-erasing circuit to operate and inward transfer gate to open for 110.
- (6) "Test" flip-flop trigger circuit to be prepared for 011.
- (7) "Stop" circuit to operate for 111.

### (5) CONCLUSION

The computing machine which has been described has operated successfully using various programmes. Using a highest-common-factor programme, in 0.5 sec, it showed that 314 159 265 and 271 828 183 are co-prime. This example illustrates the speed with which the machine operates. It has also operated continuously for several hours, for testing purposes. For example, using the laborious highest-factor programme described (in modified form) in Section 2.2, it operated for 52 minutes to find the highest factor of  $2^{18}$ . During this time, about 130 000 numbers were tested, involving some 3.5 million operations. These examples, although mathematically trivial, show that it is feasible to construct a machine to undertake useful computation, using the techniques which have been described.

\* A more systematic approach is possible if the size of the task warrants it.

However, it is essential that quicker means be provided for loading the programmes and numbers into the store. In addition, more storage capacity and a greater diversity of computing circuits are needed, the latter to ease the labour of devising the programmes and to increase the speed of computation. These developments are in hand, and the authors hope to publish a description of them later.

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### (7) APPENDICES

#### (7.1) The Writing Process

##### (7.1.1) Writing in One Attempt.

The storage experiments described by Hartree,<sup>4</sup> proved that numbers consisting of 32 binary digits can be stored for an indefinitely long time, but the experimental method used for impressing the charge patterns on the fluorescent screen of the storage cathode-ray tube gave no indication of the time taken by this operation. When this storage system is used as part of a computing machine, the time taken to record numbers obtained as a result of the elementary operations of which the computation is made up will be a factor which determines the speed of operation of the whole machine. It is known that charge distributions can be maintained on the screen by continually re-writing the information, for this is the method used to regenerate the stored numbers. If, however, the charge distributions were initially created as the result of a cumulative process, then they can be converted to other distributions only by a similar cumulative process. It is implicit in the description given in Reference 8, that writing new information on a storage line is complete in one attempt, since it is stated that, every time a storage line on the face of the cathode-ray tube is scanned

and regenerated, each digit area is first reduced to a standard state of charge. If it were not in this standard state initially it is then restored to its previous state. During this process, the previous state of the digit area is "remembered" by a condenser in the gate circuit.

The completeness of single-attempt writing was investigated by writing, cyclically, two different numbers, in turn, into a storage line and allowing each to be regenerated for observation purposes for one sweep after it had been written. The amplifier output waveforms during this regeneration sweep, for the newly written dots and dashes, were found to be substantially the same as those for dots and dashes which were left unchanged throughout the cycle, which shows that writing is complete in one attempt.

#### (7.1.2) Amplifier Waveforms Obtained whilst Writing.

The characteristics of the amplifier waveform produced by the writing process are of practical importance. It has been found useful, in the design of computing circuits, to be able to read the number stored on a line at the same time as it is being superseded by a new number, e.g. with the subtractor described in Section 3.2. If the time base is a repetitive waveform, the amplifier output waveform depends on:

(a) The charge distribution existing before the line in question is scanned.

(b) The modulating waveform applied to the cathode-ray-tube grid during the scan.

The waveforms previously described<sup>8</sup> are the special cases which arise in the course of normal regeneration, when (b) is such as to leave (a) unchanged. The first part of the c.r.t.-grid waveform is the same, whether the digit being written is a dot or a dash, so that the amplifier output during this time depends only on the charge distribution, i.e. on the number being superseded. Since the gate circuit operates only on this first part, the "read" output it produces will be of this number.

The observed unbalance of the amplifier waveforms obtained whilst writing, is also to be expected on theoretical grounds. When a dot or a dash is regenerated normally, the charge left on the screen after the digit area has been scanned is exactly the same as it was before, so that the time integral of currents flowing to the pick-up plate, and hence of the amplifier output-waveform, is zero, i.e. the normal dot-and-dash waveforms are balanced about their starting level. When, however, a dot charge-distribution, Fig. 12(a), is converted into a dash charge-distribution,

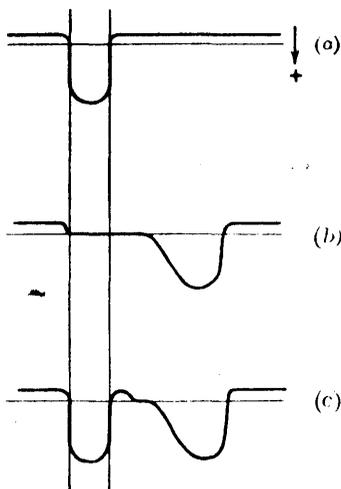


Fig. 12.—Possible digit charge-distributions.

- (a) Dot charge-distribution.  
 (b) Dash charge-distribution.  
 (c) Dot charge-distribution with residue of a former dash.

Fig. 12(b), there is an increase in the positive charge left on the screen, so that the associated amplifier-waveform is positive, on the average. When an attempt is made to convert the dash distribution back into a dot distribution, the distribution shown in Fig. 12(c) is left; the trail of the charge—characteristic of the dash distribution—is too far away from the first part of the digit area to be filled in appreciably, and therefore it remains. There has been a larger increase in positive charge this time, so the amplifier output-waveform will be even more unbalanced in the positive direction.

This novel form of dot distribution will be regenerated by the gate circuit, as if it were a normal dot. The negative pulse that this distribution will produce when the beam is turned on in its initial position will ensure that the beam is turned off again at the end of the dot period, before the beam moves, and that the positive trail of the charge will gradually leak away at the inherent storage-time rate, the distribution shown in Fig. 12(c) reverting to that shown in Fig. 12(a). If the dot is changed back into a dash before this leakage has occurred, there will be a net decrease in positive charge, of the same amount as the increase produced when a dash is converted into a dot, and, in this instance, the amplifier output-waveform will be unbalanced in the negative direction.

#### (7.1.3) Detailed Description of Waveforms.

It is necessary to describe the effect of a paused time-base on the normal amplifier-waveforms, before the writing waveforms can be described. It has been stated\* that a linear time-base can be used, and that, in this instance, the dots are really very short lines; if, however, a time base is used which pauses during the dot period, the dots are true dots. With a linear time-base, the "well" of the dot charge-distribution is filled in, very slightly, at the start of the dot, so that the negative pulse, appropriate to

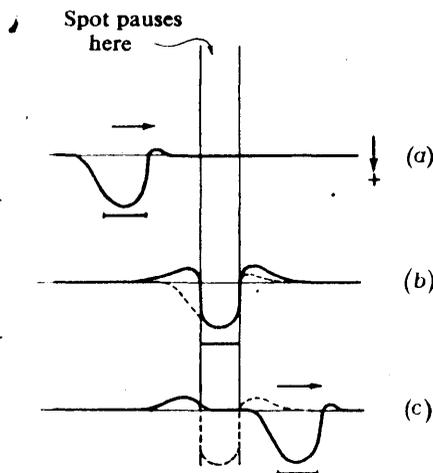


Fig. 13.—Charge distributions for constant beam-current.

- (a) Trail of charge due to spot in motion.  
 (b) Charge distribution after spot has been stationary.  
 (c) Charge distribution after spot has moved on.

a dot, is slightly reduced in amplitude. With a paused time-base this does not occur; typical output-waveforms with a paused time-base are shown in Fig. 14(a). Since the spot does not move during the dot period, the dot pulses are now due entirely to the electron-cloud effect, and are therefore sharply pointed. The dash waveform has an irregularity between the initial positive pulse and the anticipation pulse, which is caused by the time-base pause in the following way.

If no black-out modulation is applied to the cathode-ray-tube grid, the amplifier output waveform is as shown in Fig. 14(c).

\* Reference 8, Section 3.2.

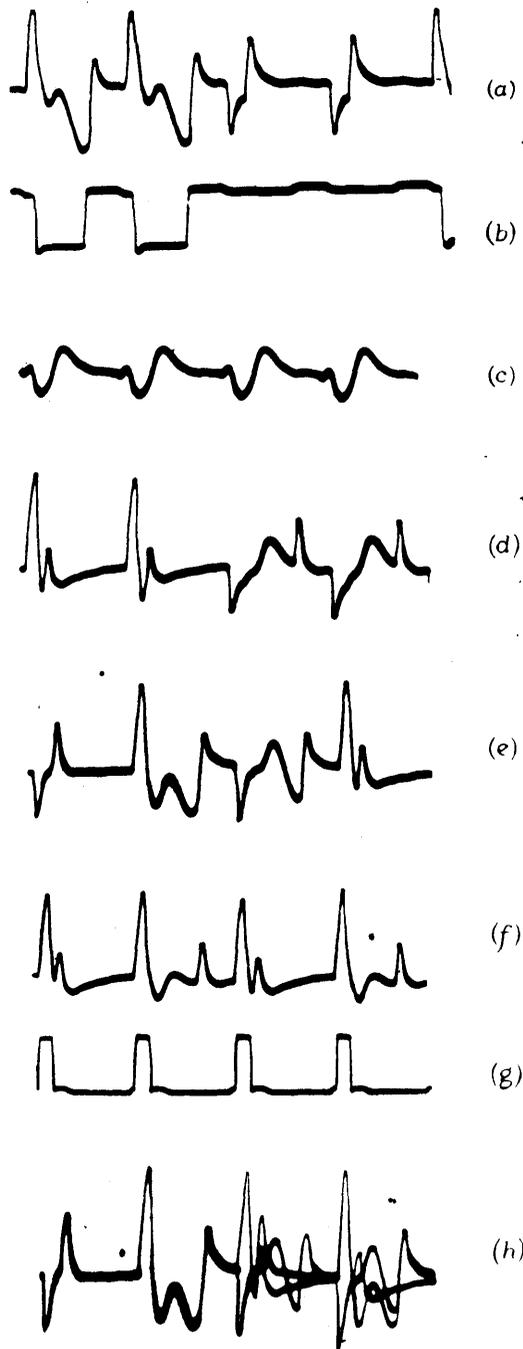


Fig. 14.—Amplifier waveforms.

- (a) Normal waveform using a paused time-base.  
 (b) "Read" waveform.  
 (c) Waveform due to time-base pause.  
 (d) Dot-on-dash and dash-on-dot waveforms.  
 (e) Normal dash-on-dot with dash residue, and dot-on-dash waveforms.  
 (f) Dot- and dash-on-furrow waveforms.  
 (g) Strobe.  
 (h) Superimposed waveforms.

The beam current here is constant throughout the scan and the waveform is due solely to the time-base pauses. When the spot is moving across the screen with constant velocity, the charge distribution is of the form of Fig. 13(a), the trail of charge shown being in motion with the spot. When the spot is stopped, the charge distribution is converted to a simple well-distribution of charge [Fig. 13(b)] by the destruction of the positive charge

which was behind the moving spot and by a slight building up of negative charge behind and before the stationary spot.\* These two effects add together to produce the negative pulse of Fig. 14(c). When the spot starts to move again, the opposite effect occurs, i.e. the positive trail of charge behind the spot is re-created and the negative charge in front of the spot is reduced; this gives rise to the positive pulse seen in the Figure. The small negative charge left behind just before the position where the pause occurred [Fig. 13(c)] accounts for the initial slight positive tendency of the waveform in Fig. 14(c) when the area in question is scanned again; the time integral of the positive portions of the pulse is equal to the time integral of the negative portion, since the area is left in the same state as it was originally.

The form taken by the dash waveform, shown in Fig. 14(a), follows from the foregoing. The initial positive pulse results only from digging a well, since the time base is stationary at first. It is therefore narrower than the pulse resulting from a linear time-base, which is due partially to creating a trail of charge behind the spot, in addition to digging the well. The negative overshoot which follows is due to the negative charge which piles up in front of the spot [Fig. 12(c)]. The positive motion, which follows the negative overshoot, starts when the spot begins to move and is due to the destruction of this charge, together with the creation of a trail of positive charge behind the spot as it moves away from its initial position. The waveform is completed by the anticipation pulse.

The precise shape of the amplifier output-waveform is, of course, dependent on many factors, which vary between different storage units. This is shown by comparing Figs. 14(a) and 14(e), which were obtained from two different storage-units using a common time-base, and, although the differences are marked, they are quite tolerable, since, in each, there is a marked difference between the pulses, positive and negative, which occur during the strobe period. The dot, dash, and digit periods appropriate to the paused time-base photographs are 1.6, 5.4 and 8.5 microsec, respectively. The amplitude and timing of the waveforms in Fig. 14 may be estimated by comparison with the strobe waveform Fig. 14(g), which is 24 volts in amplitude, and recurs at 8.5-microsec intervals.

There are three conversion processes to consider in the operation of writing:

(a) Writing a dash on a dot.

The amplifier waveform obtained whilst converting the dot charge-distribution of Fig. 12(a) to the dash charge-distribution of Fig. 12(b) is shown in positions 3 and 4 of Fig. 14(d). This waveform shows:

- (i) An initial negative pulse, due to the electron cloud forming when the beam current is turned on. This occurs whilst the spot is paused.
- (ii) A positive-going portion which starts when the spot begins to move. This is due to the creation of the trail of charge behind the spot.
- (iii) A final positive pulse, due to the collapse of the electron cloud, which occurs when the beam is turned off.

(b) Writing a dot on a dash.

The amplifier output-waveform obtained whilst converting the dash charge-distribution of Fig. 12(b) to the dot charge distribution of Fig. 12(c) is shown in positions 1 and 2 of Fig. 14(d). This waveform shows:

- (i) A net positive pulse, formed in the normal manner when the beam is turned on.

\* The portions of the screen on either side of the line scanned will remain throughout at a slightly negative equilibrium potential, which is maintained by a rain of stray electrons arriving at the screen and leaving by leakage paths.

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(ii) A negative overshoot, due to the negative charge which piles up in front of the spot.

(iii) A positive pulse, due to the collapse of the electron cloud when the beam is turned off.

(c) *Writing a dash on a dot with the residue of a previous dash.*

The amplifier output-waveform obtained whilst converting the dot charge-distribution of Fig. 12(c) to the dash charge-distribution of Fig. 12(b) is shown in position 3 of Fig. 14(e). This waveform shows:

(i) An initial negative pulse, due to the electron cloud forming when the beam current is turned on.

(ii) A positive-going portion, due to creating the trail of charge when the spot begins to move.

(iii) The negative-going anticipation pulse, due to the merging of this trail of charge with the well left since the area was last a dash and to the consequent net destruction of positive charge. This portion merges with (ii).

(iv) A positive pulse, due to the collapse of the electron cloud when the beam is turned off.

Any cyclic method of writing dashes on dots, which recurs often enough to give a good picture on the oscillograph, will yield this last waveform. The method used to produce the waveform of Fig. 14(d), was to allow the electron beam to scan the line of digit areas at constant beam-current. This gives a "furrow" which is at the same potential along its length, except for the minor irregularities such as the one shown in Fig. 13(c). Two dashes, followed by two dots, were written on this furrow, and then two dots followed by two dashes. The amplifier waveform during this second writing operation is that of Fig. 14(d), and, during the first operation, the individual waveforms are similar to those of Fig. 14(f). The dot-on-furrow waveform of positions 1 and 3 of Fig. 14(f) is similar to the dot-on-dash waveform of Fig. 14(d); the dash-on-furrow waveform of positions 2 and 4 is similar to the normal dash waveform, except that there is no anticipation pulse.

Finally, Fig. 14(h) shows the dot-on-dash and dash-on-dot-with-dash-residue waveforms superimposed. They are also superimposed on the normal dot-waveform in position 3 and on the normal dash waveform in position 4. This enables their amplitude and timing to be compared easily, and shows that the first part of the hybrid waveforms is the same as that of the normal waveform corresponding to the initial charge-distribution. The effect of the unbalance in the writing waveforms can also be clearly seen, in that the amplifier output-voltage does not return immediately to its datum level after the marked asymmetry of the dot-on-dash waveform. This is because the amplifier in use is an a.c.-coupled one.\* The recovery is not quite complete before the start of the following digit-period, and the effect is cumulative when, say, a whole line of dashes is converted to dots on the same sweep, which is the worst condition. With correct adjustments of brilliance, focus and amplifier gain, the depression of the base line in this instance can be made insufficient to prevent correct operation of the gate circuit by the last digit waveform in the line.

### (7.2) A Staticisor Unit

The circuit diagram of Fig. 15 shows one unit of the three which comprise the F-staticisor (see Fig. 9). The five units of the L-staticisor are similar, except that the four output cathode-followers, V3-V6, are omitted, the single output being taken from the suppressor grid of V2. The two diodes in the grid circuit of V1, form a coincidence gate which the negative pulse,  $P_n$ , opens only for the  $n$ th digit of the instruction; this appears at the terminal labelled "from  $S_n$ ". The potential of

\* Reference 8, Appendix I.

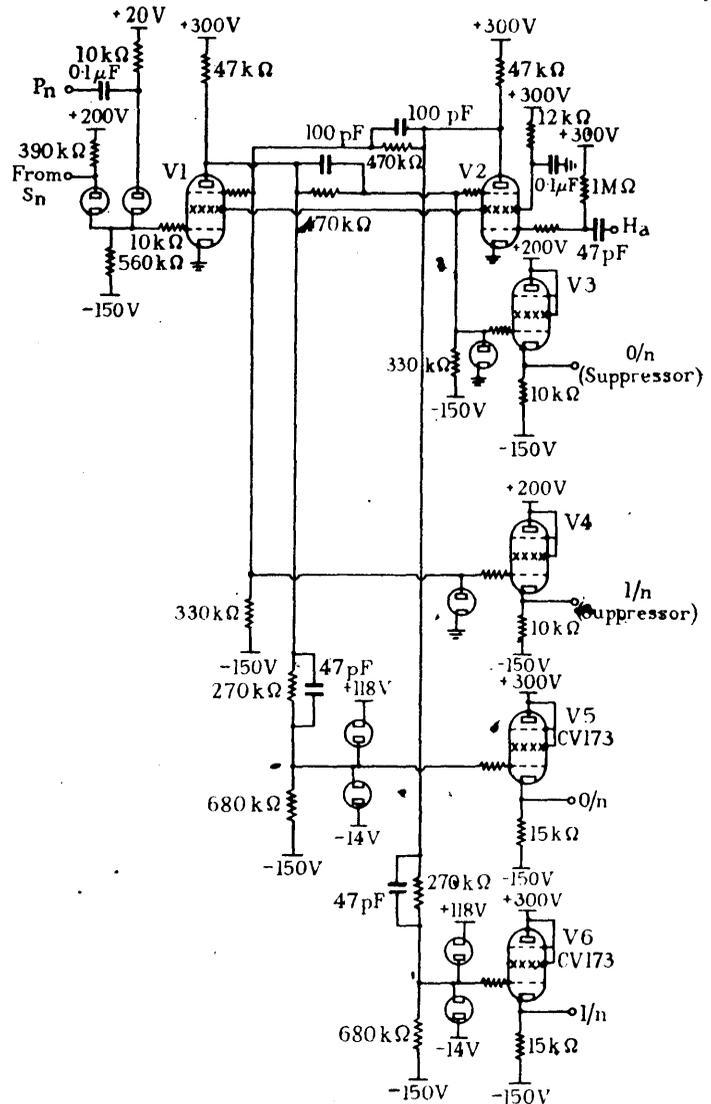


Fig. 15.—Staticisor section  $n$ .

The convention is used that all pentodes are CV1091 (EF50), and all diodes are CV1092 (EA50) when they are not marked otherwise, and all unmarked grid-stoppers are 470 ohms.

the cathodes can move negative, under the influence of the resistor connected to the negative supply, only when both diode anodes are negative. When either anode returns to its rest level of about +3 volts, V1 draws grid current.

V1 and V2 form a direct-connected flip-flop circuit and negative pulses, derived by differentiating the halver waveform,  $H_n$ , restore it to its rest condition (if it has been disturbed) at the end of every action beat. In this condition, anode current flows in V1, so that the flip-flop circuit is triggered when a negative pulse occurs at the diode cathodes. Triggering can occur only during scan beats, so that the flip-flop circuit maintains its state for the duration of one complete action beat. The 0/n (suppressor) output moves from -60 volts to zero if the staticisor unit is triggered, while the 1/n (suppressor) output moves from zero to -60 volts. The 0/n and 1/n outputs move positive and negative, respectively, between the levels -10 and +120 volts; their use is described in Section 7.6.

### (7.3) The Pre-Pulse and Stop Circuits

The functions of the pre-pulse circuit, which is shown on the right of Fig. 16, were stated in Section 3.5. In addition to

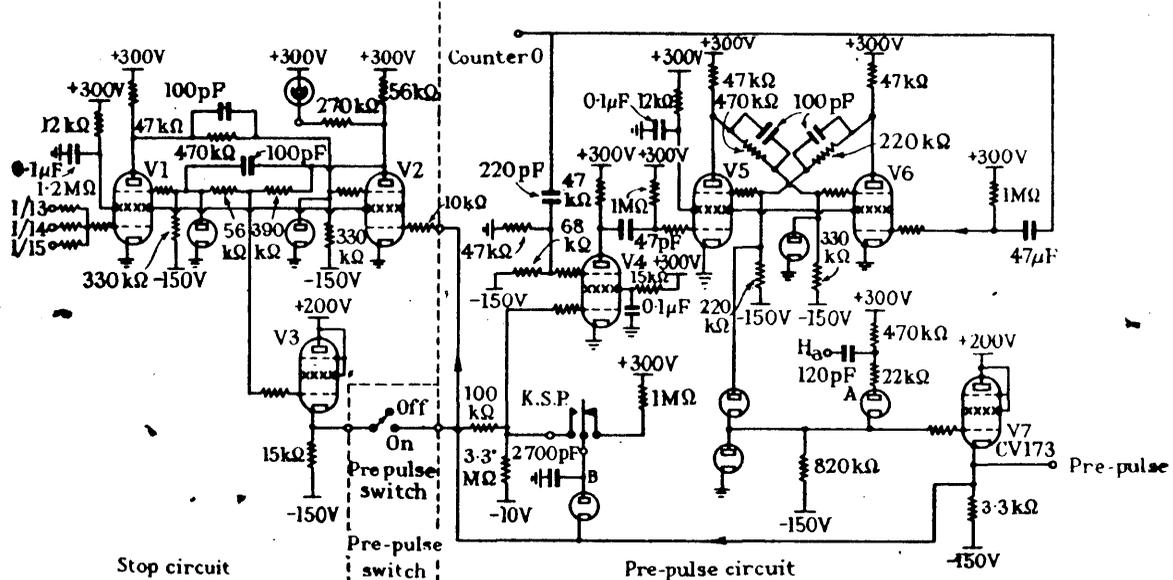


Fig. 16.—“Stop” and pre-pulse circuits.

generating no more than one pre-pulse for each operation of KSP, the circuit is required to minimize the possibility of generating a mutilated pre-pulse by pressing the key at an inappropriate instant. When KSP is released, the condenser connected to its moving contact is charged to a slightly positive potential defined by the cathode potential of V7. If the pre-pulse switch is “off,” the control grid of V4 is cut off. When KSP is operated, contact bounce may occur, such as is shown in Fig. 17(c), so that, while the make contacts are connected, the grid of V4 is raised to earth potential [Fig. 17(d)]. The suppressor grid of V4 is cut off except for a series of positive pulses, obtained by differentiating counter 0, which is a repetitive square wave of period twice the halver waveform. The anode of V4 thus remains at + 300 volts until the grid and suppressor together allow the valve to conduct; a negative pulse then occurs. If the grid is raised to earth potential during one of the positive suppressor-pulses, the negative pulse produced at the anode may be very small, like the first pulse shown in Fig. 17(e). The flip-flop circuit, V5 and V6, is similar to the staticisor one, and the suppressor-grid waveform of V5 controls a diode coincidence gate. A train of negative pulses is produced by differentiating  $H_a$  (see “waveform at A” in Fig. 17), each of which is a possible pre-pulse; however, when the flip-flop circuit is in its rest condition, they are prevented from reaching the pre-pulse output-terminal. The small-sized pulse at the anode of V4 attempts to trigger the flip-flop circuit; if it fails, the consequent disturbance of the suppressor-grid waveform of V5 occurs at a time when there is no possible pre-pulse at point A. Eventually, a pulse will be produced which will trigger the flip-flop circuit, and the suppressor-grid waveform of V5 will allow the next pulse at point A to become a pre-pulse. The pre-pulse charges the condenser connected to the moving contact of KSP to a negative potential (see “waveform at B”) so that the grid of V4 does not allow the valve to conduct again, irrespective of contact bounce which may still persist.

The negative edges of counter 0 define an instant suitable for re-triggering the flip-flop circuit (see “V6 grid”) before another pre-pulse can be generated. Thus, only one pre-pulse is generated for each operation of KSP, provided its action is truly a “break-before-make” one.

In the normal condition of the “stop” flip-flop circuit (V1 and V2), V1 is taking anode current. The potential of the cathode of V3 is then about + 30 volts, and, if the pre-pulse switch is

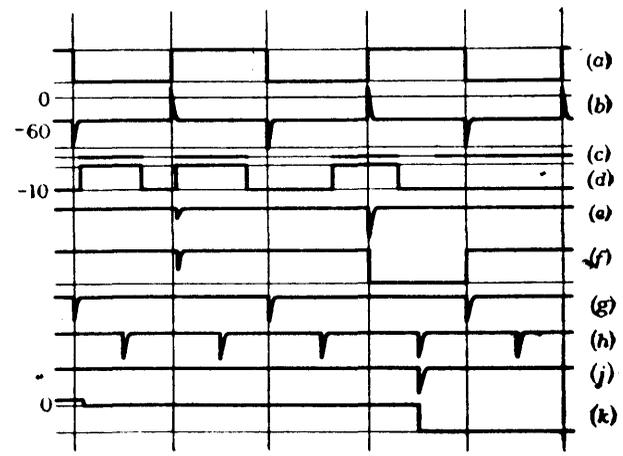


Fig. 17.—Waveforms in the pre-pulse circuit.

- (a) Counter 0.
- (b) V4 suppressor.
- (c) KSP operated.
- (d) V4 grid.
- (e) V4 anode.
- (f) V5 suppressor
- (g) V6 grid.
- (h) A.
- (i) Pre-pulse.
- (k) B.

“on,” V4 draws grid current. The pre-pulse flip-flop circuit is triggered by each positive-going edge of counter 0, and the suppressor-grid waveform of V5 is an inverted copy of counter 0, so that every other pulse appearing at A becomes a pre-pulse. The pre-pulses thus occur at the requisite four-beat intervals. The grid of V1 can never become negative until the “stop” code, 111, is set up on the F-staticisor (see Section 7.6). This may occur during an S2 beat, whereupon the “stop” flip-flop circuit is triggered and the potential on the cathode of V3 becomes about - 60 volts. Before the end of the S2 beat, the grid of V4 is cut off, so that the next positive pulse on the suppressor grid is prevented from having any effect. Thus, no further pre-pulses occur after the “stop” flip-flop circuit has been triggered by the “stop” instruction; hence, it must be re-triggered by external intervention. The neon pilot lamp in the anode circuit of V2 lights when the machine stops.

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(7.4) The Control Y-Plate, Instruction-Gate, and Action-Waveform Circuits

Fig. 18 represents the method used to generate these waveforms. The flip-flop circuits and diode coincidence-gate shown are similar to the ones described in Sections 7.2 and 7.3. The pre-pulse (see Fig. 19) triggers a flip-flop circuit on one grid; it is re-triggered on the other grid by  $H_s$  waveform, the zig-zag line

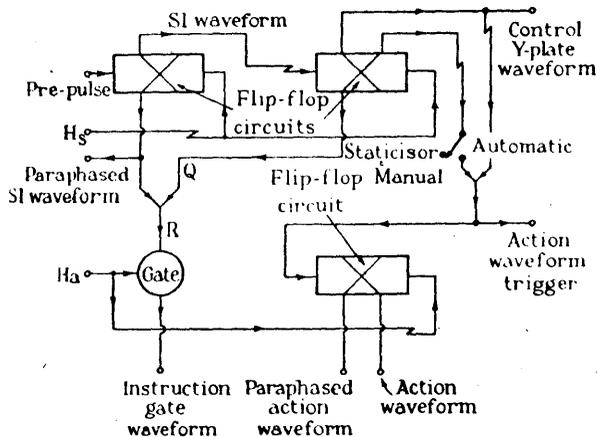


Fig. 18.—Schematic of control Y-plate, instruction-gate, and action-waveform circuits.

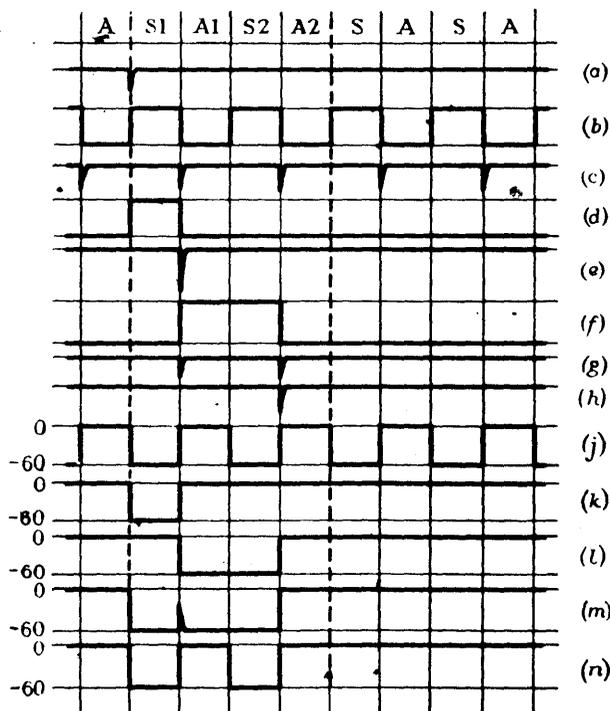


Fig. 19.—Waveforms in the circuits shown in Fig. 18.

- (a) Pre-pulse.
- (b)  $H_s$ .
- (c)  $H_s$  differentiated.
- (d) S1 waveform.
- (e) S1 differentiated waveform.
- (f) C Y-plate.
- (g) Action waveform trigger (auto).
- (h) Action waveform trigger (manual).
- (i)  $H_a$ .
- (j) Paraphased S1.
- (k) Q.
- (l) R.
- (m) R.
- (n) Instruction gate.

on the diagram representing differentiation;  $H_s$  is the paraphased version of the halver waveform  $H_a$ . The anode waveform of the left-hand valve is thus the "S1 waveform," shown in Fig. 19, while the suppressor-grid waveform is the "paraphased S1 waveform"; this is fed out to the "test" circuit (see Section 7.5). The second flip-flop circuit is triggered by a differentiated S1 waveform and re-triggered by a differentiated  $H_s$  waveform. Since each trigger pulse coincides with a re-trigger pulse, the trigger pulse must be made of longer duration, so that it can override the re-trigger pulse. The control Y-plate waveform (described in Section 3.3) appears at the left-hand anode; its amplitude and d.c. level are adjusted for the Y-plate of the cathode-ray tube, the deflection being asymmetrical.

The suppressor-grid waveform appearing at point Q (see Fig. 19), is mixed with the paraphased S1 waveform in a diode buffer-circuit. The two inputs to this circuit go to the cathodes of two diodes, the anodes being connected together, with a leak resistor to a positive supply-voltage. Thus, each input can pass through the circuit to the output without interaction between inputs, and the output waveform is the "waveform at R." This is fed to a diode coincidence-gate via a cathode-follower. The output of the gate can move negative only when both  $H_a$  and the waveform at R are negative, and thus the instruction-gate waveform is generated.

The control Y-plate waveform and its paraphased version are differentiated, the positive pips being removed. These differentiated waveforms are mixed in another diode buffer-circuit, after one of them has passed through a contact on the staticisor switch. This gives the waveform called "action-waveform trigger," which consists of two pulses for automatic operation and one for manual operation. It is used to trigger a further flip-flop circuit which is retriggered by differentiated  $H_s$  waveform. The suppressor-grid waveforms of this flip-flop circuit form the action and paraphased action waveforms which were illustrated in Fig. 8.

(7.5) The Test Circuit

The functions of the "test" circuit, which is shown schematically in Fig. 20, were described in Fig. 1. A coincidence gate, consisting of five diodes with commoned cathodes, generates the

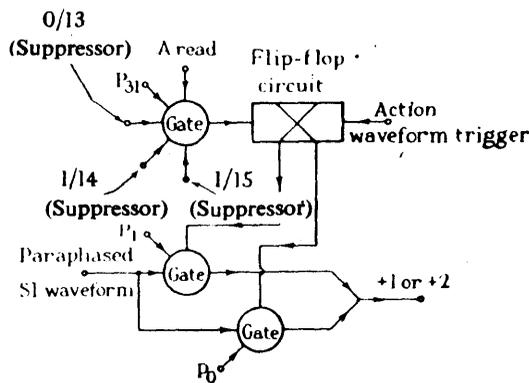


Fig. 20.—Schematic of the "test" circuit.

trigger pulse for the "test" flip-flop circuit. For all codes except the "test" one, 011, at least one of the three inputs from the F-staticisor is zero volts, which prevents any output. Only when the F-staticisor is set to 011 are all three of these inputs at -60 volts; when this occurs, the last digit of the "read" output of A is selected by P31 and triggers the flip-flop circuit if it is a 1. The suppressor-grid waveforms of this flip-flop circuit are fed to two further coincidence gates via cathode-followers.

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Each of these is inhibited, except during S1 beats, by the paraphased S1 waveform (see Fig. 19). The third input of one gate is the  $P_0$  pulse (representing the number 1) and that of the other gate the  $P_1$  pulse (representing the number 2). The outputs of these two gates are combined in a diode buffer-circuit to form the +1 or +2 signal. The action-waveform trigger pulses form a convenient means of re-triggering the "test" flip-flop circuit since the only restriction on the time of re-triggering is that it shall occur after the  $P_1$  pulse at the beginning of an S1 beat and before the P31 pulse at the end of the following A2 beat.

#### (7.6) The Decoding Valves

The possibility of operating a machine with several storage units was mentioned in Section 4.1. For example, for 256 storage units, eight further staticisor units, numbers 5 to 12, would be necessary, forming the E-staticisor (for electronic storage-unit selection). Each unit is similar to the unit of the F-staticisor described in Section 7.2, except that V3 and V4 are not required. An extra valve is necessary in each gate circuit, in addition to the four described in Appendix 9.2 of Ref. (1); in Fig. 21, V5 is

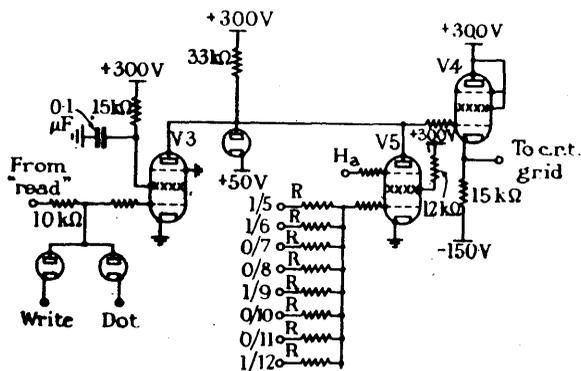


Fig. 21.—Gate circuit of storage tube number 147.

the extra valve, and the whole forms the writing unit of the gate circuit. During scan periods when the suppressor-grid of V5 is cut off, the anode current of V3 is cut off for long or short periods, producing the dot or dash waveform at the cathode-ray-tube grid output-terminal, as described in the above reference. During action periods, however, if the grid of V5 is at earth potential, the cathode-ray tube will be blacked out, irrespective of the anode current of V3. This will be so in the example chosen, for every configuration of the E-digits of an instruction except 11001001 (or 147 in decimal notation). In this case, all the grid-leak resistors, R, are connected to -10 volts, so that the control grid of V5 is cut off and the cathode-ray-tube screen is bright. With each of the other 255 cathode-ray tubes, at least one of the leaks is connected to +120 volts, overriding the other seven, causing V5 to draw grid current and blacking out the cathode-ray-tube trace. The value of R is not critical, except that all leak resistors must be approximately equal; a value of 2.5 megohms would give sufficiently fast operation. Since each of the staticisor cathode-followers, V5 and V6 of Fig. 15, has to

control 128 of these resistors, the total loading on one of them would be about 20 kilohms.

The same technique is used in the control gate-circuit, to arrange that control is brightened, during A1 and A2, only for F numbers ending in 00. In the accumulator gate-circuit, the d.c. level of the grid waveform of the decoding valve is adjusted, by means of a resistor to the negative voltage supply, so that the valve conducts only for F numbers ending in 00.

#### (7.7) The Transfer Gates and Erasing Waveform Circuits

The purpose of the transfer gates was described in Section 4.1. The circuit diagram of the outward-transfer gate is shown in Fig. 22. This double-cathode-follower type of coincidence gate

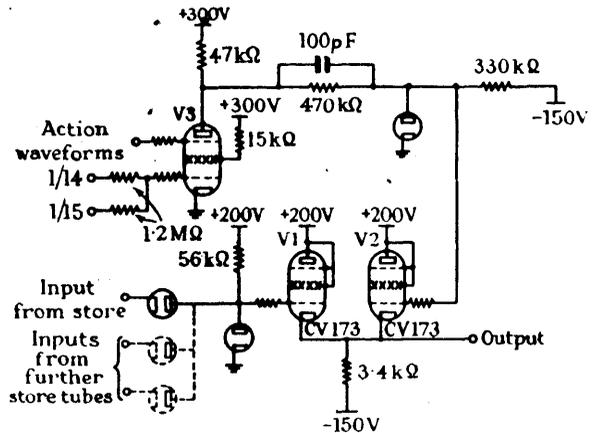


Fig. 22.—Outward-transfer gate.

is preferred to the diode type, because it gives fast operation without putting a heavy load on the input sources. Although there is only one cathode-ray tube in the store of the machine, a buffer circuit is provided to accept the "read" output of several storage tubes. This is passed on to the output terminal when the grid of V2 is negative; this occurs, in general, during A1 and A2. However, when the two F numbers which end in 11 occur, the grid of V3 is cut off and the gate remains closed. This is functionally the same as the arrangement shown in Fig. 9.

The inward-transfer gate is similar, except that V3 is omitted and the grid of V2 is connected to the store erasing-circuit as shown in Fig. 9. There are then two inputs to V1, from the accumulator and the typewriter.

The store erasing-waveform circuit consists of a 4-input diode coincidence-gate with a cathode-follower connected to its output. The paraphased action waveform prevents the output moving negative except during the A1 and A2 periods, when it moves to -60 volts only if all three of the suppressor voltages from the F-staticisor are at -60 volts, which occurs only for the F-number 110. The accumulator and control erasing-waveform circuit is similar, except that one connection to the F-staticisor is omitted, so that it responds to two F numbers, 000 and 010.