

*Univac*<sup>®</sup>

LARC

PROCESSOR

MAGNETIC DRUM  
SYNCHRONIZER SYSTEM

*Remington Rand Univac*<sup>®</sup>

DIVISION OF SPERRY RAND CORPORATION

UNIVAC ENGINEERING CENTER • PHILADELPHIA

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NOVEMBER 1961

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# SECTION 1

## INTRODUCTION

### 1-1. SCOPE OF THIS MANUAL

This manual describes the logic of the Univac<sup>®</sup>-Larc\* drum synchronizer system. The description is designed to apply to any Larc system, from the basic to the fully expanded. The drum-read and drum-write synchronizers chosen for discussion appear in every Larc system and are identical to all other drum-read or drum-write synchronizers unless a statement is made to the contrary.

The circuit illustrations throughout the manual, with the exception of figure 1-1, are in the form of simplified logic diagrams which include the numbers of the detailed engineering drawings they are intended to represent.

Only logical functions and operations are considered in this manual. Descriptions of the physical characteristics and circuitry operation of the components in the drum synchronizer system will be found in the Larc Circuitry and Larc Drum Storage manuals.

### 1-2. ORGANIZATION OF THIS MANUAL

The manual is divided into seven sections and two appendices.

The rest of this section presents a general outline of the drum synchronizer system and of how it is used in the Larc system. Section 2 provides only sufficient background information on the drum file and method of drum storage to enable the reader to understand the drum circuits in the processor better. The information is therefore necessarily incomplete.\*\*

Section 3 is a description of the logical circuits through which the processor program connects the drums to the synchronizers and controls the movement of the drum read-write head assemblies.

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\*\* For complete information, refer to the Larc Drum Storage manual and Section 5 of the Larc Processor Programming manual.

The logic of the synchronizers themselves is presented in the remaining sections. Sections 4 and 5 describe two areas of logic that are essentially identical in all drum synchronizers—namely, the circuits through which the program controls, and is informed of, synchronizer activities, and the circuits that allow the program to determine which recording areas on the drums pass under the read-write head assemblies.

Section 6 defines the logic common to all drum-write synchronizers only—that is, the circuits that control data transfers from memory to drum; Section 7 treats the logic common to drum-read synchronizers only—that is, circuits controlling data transfers from drum to memory.

Appendix A is a description of the special logic incorporated in drum-read synchronizer 1 and drum-write synchronizer 1 for the purpose of detecting drum bad spots and relocating sectors.

Appendix B summarizes the error insertion logic for drum synchronizers.

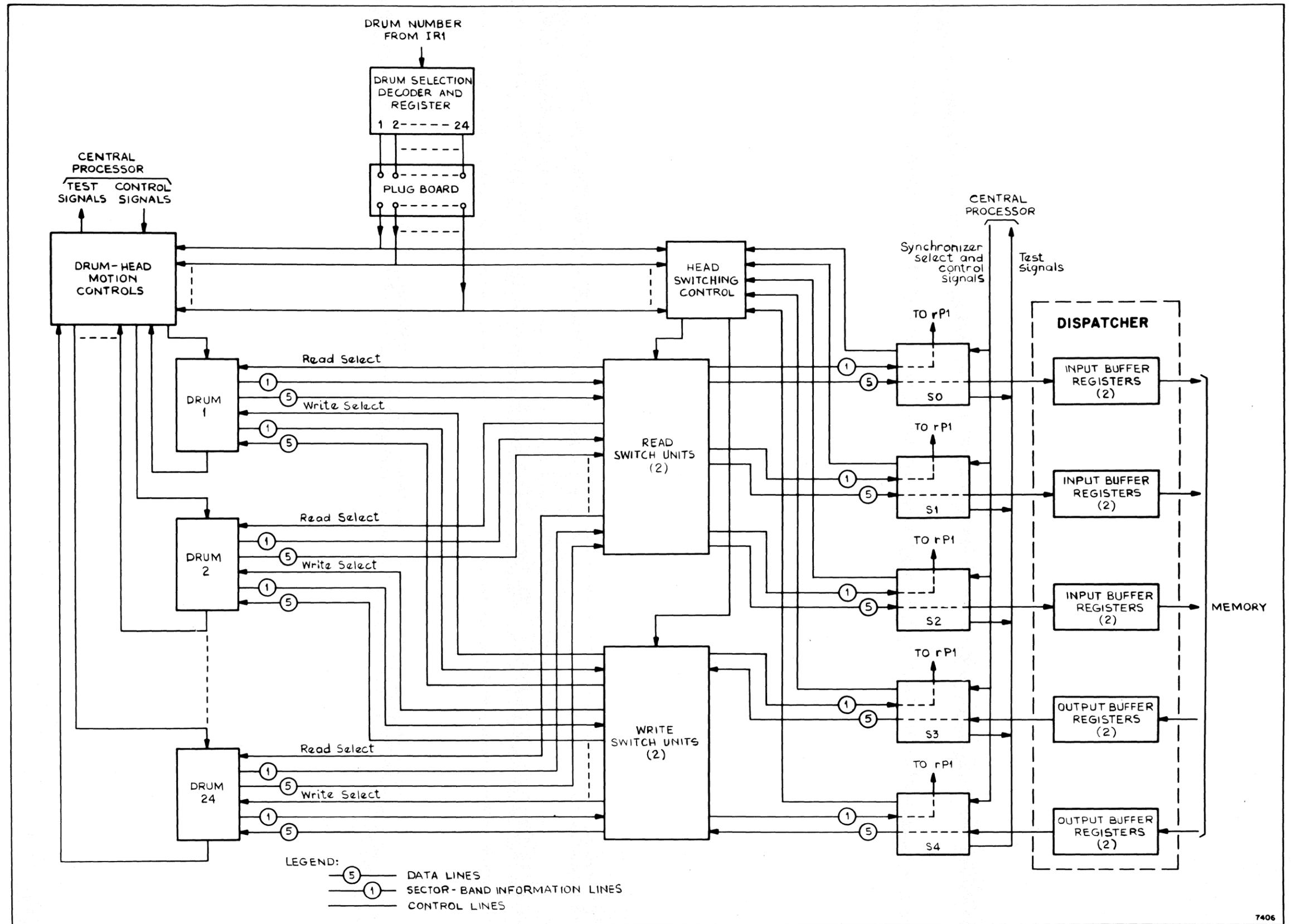
### **1-3. OUTLINE OF SYSTEM**

The basic Larc drum synchronizer system contains 12 drums, two drum-read synchronizers designated S1 and S2, and one drum-write synchronizer designated S3. The system can be expanded to a maximum of 24 drums, with an additional drum-read synchronizer designated S0 and an additional drum-write synchronizer designated S4. The general block diagram in figure 1-1 represents the fully expanded system.

Under program control, any drum-read synchronizer can transfer data recorded on any drum to the memory by way of the two input buffer registers in the dispatcher for the synchronizer; similarly, any drum-write synchronizer can transfer memory data from its two output buffer registers in the dispatcher to any drum. The data lines to any drum-read synchronizer are connected to the read bus of any drum by relays in the read-switch units; each set of 12 drums requires one read-switch unit. The data lines from any drum-write synchronizer are connected to the write bus of any drum through relays in the write-switch units, of which there is one for each set of 12 drums.

The synchronizer-to-drum connections made in the read- and write-switch units are controlled by the head-switching controls in response to program instructions specifying drum and synchronizer number. For every synchronizer-to-drum connection made, the read- or write-switch units provide a read- or write-select signal that switches the drum read-write head assembly to the drum-read bus or drum-write bus respectively.

An extra read line is included in both the read and write buses of every drum and in the buses between the read- and write-switch units and the synchronizers. This line always reads a special track on the drum (even when the read-write head assembly is switched to the write position), and provides any synchronizer connected to the drum with information as to which data location on the drum will next pass under the read-write head assembly. The synchronizer transfers this information to register P1 in the central processor, where the program can determine whether it represents a location to or from which the synchronizer must transfer information.



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Figure 1-1. Drum Synchronizer System

The program controls the movement of the drum read-write head assemblies through the drum-head motion controls in the central processor. Similarly, the program controls synchronizer activity through program and status controls in the synchronizers themselves.

Note from figure 1-1 that the drums in a system can be functionally interchanged by means of a plugboard—that is, the number assigned to each drum is controlled through a plugboard.

The system is designed so that all the drum-synchronizers included in the system can be simultaneously engaged in transferring data between the drums and the buffer registers.

The drum-head motion controls are independent of the synchronizers. The read-write head assembly of a drum can be positioned in parallel with the read-write head assembly of any other drum, or in parallel with a read or write operation being performed on any other drum. Because of this feature, two drums can be switched alternately to the same synchronizer to achieve a continuous data-transfer rate of 366,000 decimal digits per second, including latency and connection time. While the read-write head assembly of one drum is being positioned, the synchronizer can be switched to the other drum. When the read-write head assembly of the second drum has to be repositioned, the synchronizer is switched back to the first drum, and so on.



## **SECTION 2**

### **DRUM STORAGE**

#### **2-1. GENERAL**

The storage provided by the drums in the Larc system is auxiliary to the memory and is intermediate in speed, cost, and capacity between the memory and magnetic-tape storage. The drums serve as a repository for data which are not required immediately for a current series of computations, but will be or are likely to be required for problems currently being run or scheduled to be run next. Data stored on the drums might include input data and instructions for current and future problems, intermediate results for a current problem, and service routines.

#### **2-2. DRUM CHARACTERISTICS**

A magnetic drum consists of a rotating cylinder coated with a permanent magnetic material. Binary digits are stored on the surface of the drum as small magnetized areas; the nominal pulse-repetition rate for recording the digits is 500 kc. The drum is driven at a speed of 884 rpm to produce a pulse density of 450 binary bits per inch.

A single movable head assembly is used for both reading and recording the binary bits. Under the control of the processor program, this read-write head assembly moves over the surface of the drum in a direction parallel to the axis of the drum and in a systematic stepping fashion.

Recording is by phase modulation: if a binary 1 is being recorded, the writing current from the positive side of a drum-write amplifier is positive during the first half of the bit interval and negative during the second half; for a binary 0 it is negative during the first half and positive during the second half.

#### **2-3. ORGANIZATION OF DATA ON DRUM**

Data are recorded on the drum in 100 circumferential bands, numbered 00 through 99. Each band is divided into 25 sectors numbered 00 through 24 and separated by short "spaces between sectors". Each sector contains 100 Larc words of 12 decimal digits each; thus each band contains 2500 words and the capacity of a drum is 250,000 words or 3,000,000 decimal

digits. Reading or recording can start only at the beginning of a sector, and one sector is the smallest unit that can be read or recorded during any one reference to the drum.

A band is composed of six channels. The four information bits and the parity check bit of a Larc digit are recorded in parallel in five of the channels. Words and digits of a word are stored serially. Recorded bit-serially in the sixth channel at the beginning of each sector are a sentinel, the address of the following sector, and the band number (00-99); that is sector address  $n + 1$  is recorded at the beginning of sector  $n$ . During sector  $n$  the processor program must determine whether or not it will read or write in sector  $n + 1$ .

Access to a particular band is gained by moving the single six-channel head assembly back or forth along the length of the drum. The six individual read-write heads are spaced in the head assembly at twice the channel spacing on the drum, and the six channels of one band are always interspaced with the channels of another. Two bands are interlaced by recording one band of an interlaced pair with the head assembly in one position, and recording the other band of the pair with the head assembly shifted a distance equal to the channel spacing.

The 100 bands on a drum are arranged in this order:

00 99 01 98 02 97 . . . . . 47 52 48 51 49 50

Bands 00 and 99 are the first pair of interlaced bands, bands 01 and 98 are the next, and so on. See part a. of figure 2-1.\*

Bands on which recording is extensively imperfect are designated "bad bands" and are identifiable by the absence of information in channel 6.

## 2-4. HEAD MOVEMENT

The head assembly can be positioned over a band by either of two movements:

- (1) Stepping the head assembly shifts it from one band of an interlaced pair to the equivalent band of an adjacent pair. See part b. of figure 2-1.
- (2) Jogging the head assembly shifts it from one band of a pair to the other band of the same pair. See part b. of figure 2-1.

The forward or right direction is considered to be from the band 00 end of the drum; the backward or left direction is from the band 50 end of the drum. Thus the head assembly can be stepped forward from band 00 to 01,

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\*The sectors of interlaced bands are not necessarily aligned as shown in figure 2-1. Any sector of one band of an interlaced pair may be adjacent to any sector of the other band of the pair. For example, sector 03 of band 99 may be adjacent to sector 01 of band 00.

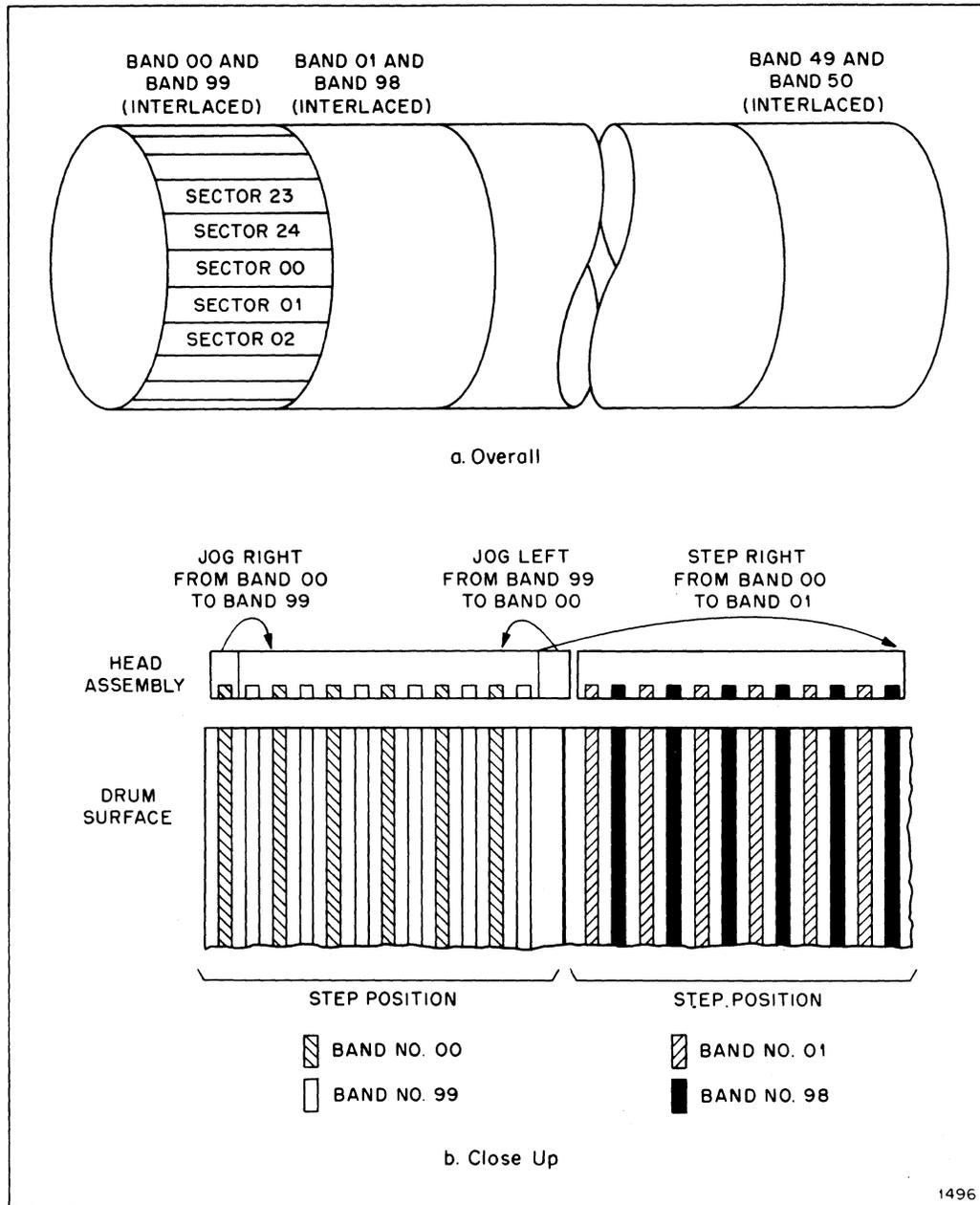


Figure 2-1. Divisions of Drum Surface

to 02, to 03, and so on to band 49; at band 49 it can be jogged right to band 50. The stepping mechanism can then be reversed and the head assembly stepped backward from band 50 to 51, to 52 and so on to 99; at band 99 it can be jogged left to band 00, the starting point. In this way, the head assembly has passed over all 100 bands and returned to the starting point without requiring the equivalent of tape rewind time.

Jogs right and jogs left are also known as jogs high and jogs low. Thus bands 00 through 49 are jog-low positions and bands 50 through 99 are jog-high positions.

## 2-5. ACCESS TIME

A step of the head assembly takes approximately 50 msec; a jog also takes approximately 50 msec. Reversal of the stepping direction takes 15 msec. A complete band of information (2500 words) can be transferred between the memory and a drum in about 82 msec, including 8 msec connection time and about 1.5 sectors of latency time. If only one specific sector on a band is desired, up to a full drum revolution of latency time (about 70 msec) may be required to gain access to the sector.

The alternate use of two drums with the same synchronizer (heading 1-3) eliminates the wasting of time in head assembly steps.

## SECTION 3

### DRUM CONTROL CIRCUITS

#### 3-1. GENERAL

The drum control circuits in the central processor divide into three sections:

- (1) Drum-select controls;
- (2) Drum-head motion controls; and
- (3) Drum-head switching controls.

Figure 3-1 is a simplified logic diagram of all three sections. A list of drum instructions appears in table 3-1.

#### 3-2. DRUM-SELECT CONTROLS

The number of a drum required for use by the processor program is specified by the contents of digit positions 6 and 7 of instruction register 1. Function signal 809, decoded from drum instructions 31, 32, and 52, gates these two digits in parallel from IRI to the tape and drum number register. The two-digit contents of the tape and drum number register,  $\overline{\text{PXID}}-\overline{\text{PXIOD}}$ , are applied to the drum-selection decoder which generates one signal for each drum selected,  $\overline{\text{PDTI}}-\overline{\text{PDT24}}$ . These 24 signals pass through a plugboard (figure 3-1) to produce drum-select signals  $\overline{\text{PD1}}-\overline{\text{PD24}}$  as long as the plugboard connections are made as in figure 3-1. However, with the plugboard connections any drum can be assigned to any drum number.

Drum selection for the master input-output tests performed by instruction 99 is performed in the following manner. For testing the drums as a group, function signal 899 is gated with test-selector signal PS0 or PS5 and applied to all plugboard inputs to force the generation of all 24 drum-select signals. For testing the drums in groups of six as a result of the 899 and PS5 test, function signal 899 is gated with certain test-selector signals to force generation of the select signals for specified drums as follows:

<u>Test-Selector Signal</u>	<u>Drums</u>
PS6	7 - 12
PS7	13 - 18
PS8	19 - 24

Table 3-1. Drum Instruction

Instruction	Code	Description	Function Signals
Test Action FF of Drum	31 xxxDD MMMM	Test action FF of drum DD. If set, $M \rightarrow C$ and reset FF. If reset, $(c) + 1 \rightarrow C$ .	831
Set Action FF of Drum	32 xxxDD xxxxx	Set action FF of drum DD.	832
Step Drum-Head Assembly	35 xxxxx MMMM	Test local/remote signal from drum. If drum is on local, head assembly does not step and $M \rightarrow C$ . If drum is on remote control, head-assembly step begins and $(c) + 1 \rightarrow C$ .	833 835
Set Step Direction Backward	36 xxxxx MMMM	If step direction of drum is already set backward, $(c) + 1 \rightarrow C$ . If step direction of drum is set forward, the step-direction relay starts to reverse and $M \rightarrow C$ .	836
Set Step Direction Forward	37 xxxxx MMMM	If step direction of drum is already set forward, $(c) + 1 \rightarrow C$ . If step direction of drum is set backward, step-direction relay starts to reverse and $M \rightarrow C$ .	837
Jog Drum Head to High Position	38 xxxxx MMMM	Test local/remote signal from drum. If drum is on local control, head assembly does not jog and $M \rightarrow C$ . If drum is on remote control, head assembly starts to jog to high position and $(c) + 1 \rightarrow C$ .	833 838
Jog Drum Head to Low Position	39 xxxxx MMMM	Test local/remote signal from drum. If drum is on local control, head assembly does not jog; $M \rightarrow C$ . If drum is on remote control, head assembly starts to jog to low position and $(C) + 1 \rightarrow C$ .	833 839

If none of these three groups contains a drum requiring attention, the drum or drums that called the program into the drum test routine from the 899 and PS5 test must be located in the group 1 through 6.

### 3-3. DRUM-HEAD MOTION CONTROLS

The drum-head motion controls allow the processor program to:

- (1) Set the direction of drum-head assembly stepping (instructions 36 and 37);
- (2) Step the head assembly (instruction 35);
- (3) Jog the head assembly (instructions 38 and 39);
- (4) Determine when any of the preceding operations has been completed.

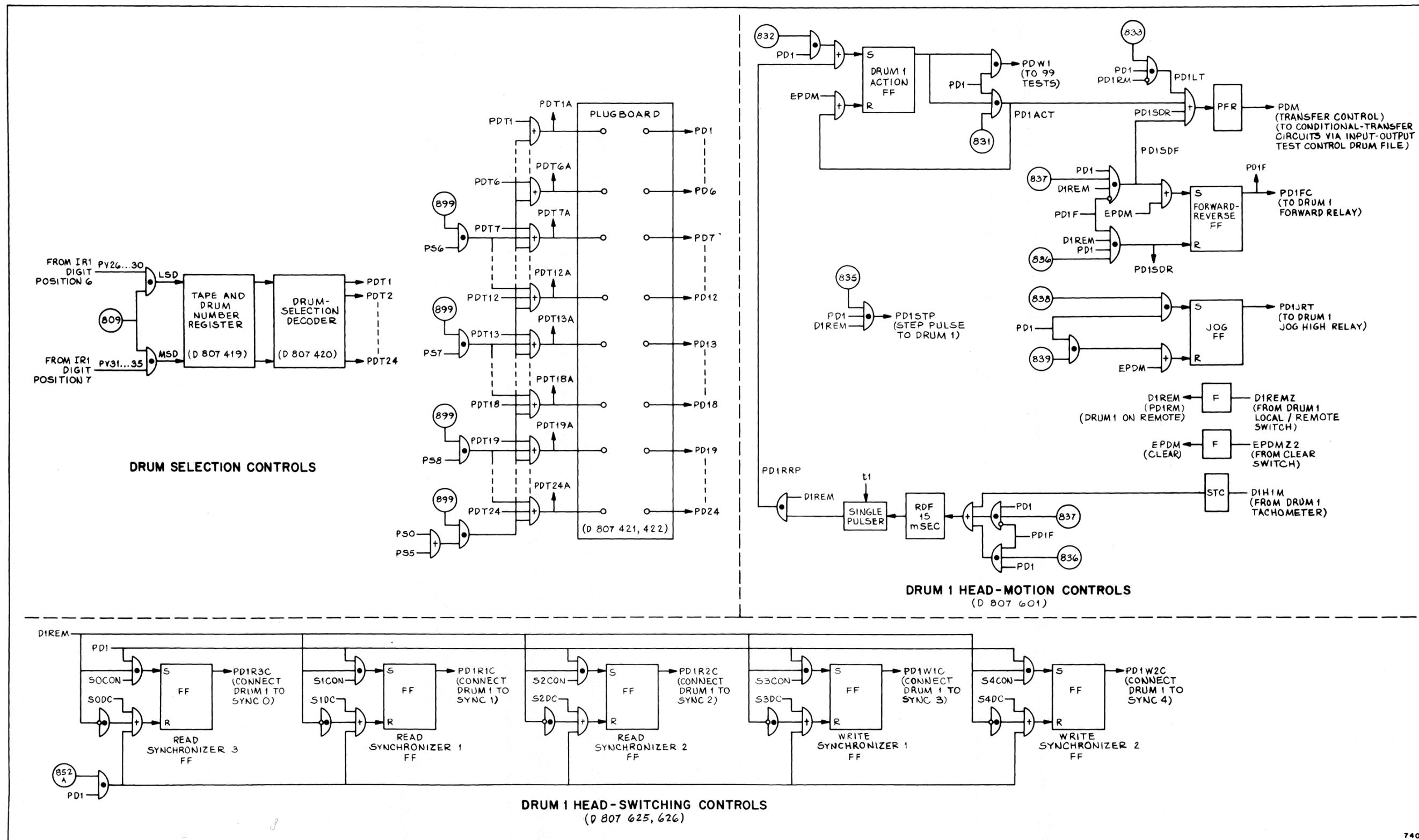


Figure 3-1. Drum Control Circuits

Each drum in the system has its own set of drum-head motion controls in the central processor. The controls for all drums are identical, and the circuit illustrated for drum 1 in figure 3-1 therefore represents the drum-head motion controls for any drum.

The controls consist basically of a forward-reverse FF, a step-pulse gate, a jog FF, and a drum-action FF.

#### 3-4. SETTING STEP DIRECTION

Instruction 37 sets the forward-reverse FF by means of function signal 837 as long as drum 1 is on remote control (DIREM low) and the flip-flop is not already set (PDI $\bar{F}$  high). In the set state the flip-flop generates signal  $\bar{Z13}/\overline{PDI\bar{F}C}$  high, which energizes the forward relay of the forward-reverse circuit in the drum. The conditions which set the flip-flop also produce signal  $\overline{PDI\bar{S}D\bar{F}}$  high, which causes a transfer of control out of the drum control routine. The forward-reverse FF is reset by function signal 836 (instruction 36) if the flip-flop is not already reset (PDI $\bar{F}$  high) and if the drum is on remote control (DIREM low). In the reset state the flip-flop generates signal  $\bar{Z13}/\overline{PDI\bar{F}C}$  low which deenergizes the forward relay of the forward-reverse circuit of the drum. The conditions which reset the flip-flop also produce signal  $\overline{PDI\bar{S}D\bar{R}}$  high, which causes a transfer of control out of the drum control routine.

#### 3-5. STEPPING

Function signal 835 from the 35 instruction is applied to a gate in the drum 1-head-motion controls. It opens to produce the step-pulse  $\bar{Z13}/\overline{PDI\bar{S}T\bar{P}}$  for the step-control circuit in the drum, provided drum 1 is on remote control (DI $\bar{R}E\bar{M}C$ ). If drum 1 is on local control (PDI $\bar{R}M$  low), another gate is opened by function signal 833 (produced by the same instruction) to generate signal  $\overline{PDI\bar{L}T}$  high which causes a transfer of control.

#### 3-6. JOGGING

The jog FF is set by function signal 838 (instruction 38) and reset by function signal 839 (instruction 39). In the set state the flip-flop generates signal  $\bar{Z13}/\overline{PDI\bar{J}R\bar{T}}$  high, which energizes the jog relay in the jog-control circuit of the drum to produce a jog high. The reset output of the flip-flop is  $\bar{Z13}/\overline{PDI\bar{J}R\bar{T}}$  low, which deenergizes the jog relay and produces a jog low. Function signal 833 is also generated by the jog-high and jog-low instructions to cause a transfer of control if drum 1 is on local control, exactly as described for the step instruction.

#### 3-7. COMPLETED ACTION

The completion of any jog, step, or change-step-direction instruction is indicated by the set state of the drum-action FF.

While a step or jog of the head assembly is in progress, a tachometer in the drum generates a 400 cps signal on the  $Z13/D1\bar{H}I\bar{M}$  line (figure 3-1) to indicate that the head is in motion. The signal sets the STC shown in

figure 3-1 every 2.5 msec, which prevents a 15-msec RDF from recovering. When the tachometer signal ends—that is, when the head assembly is in position—the RDF is allowed to recover for the full 15 msec and its output is then single-pulsed and timed to a late t1. This single pulse is gated with the drum-on-remote-control signal D1REMC to become signal  $\overline{\text{PD1RRP}}$  high, which sets the drum-action FF. The 15-msec delay after the head assembly has been positioned allows for the settling time of the assembly.

The time required to reverse the head-stepping mechanism in the drum is also approximately 15 msec. Therefore, when the stepping direction is to be reversed, the conditions which change the state of the forward-reverse FF (function signal 837 and  $\overline{\text{PD1F}}$  low, or function signal 836 and PD1F low) also trigger the 15-msec RDF to produce signal  $\overline{\text{PD1RPP}}$  high and set the drum action FF.

In addition to being set for a completed jog, step or change step direction instruction, the drum action FF can be set by instruction 32 with function signal 832. This is a programming convenience for forcing the program into the drum test routine. The output of the drum-action FF is sampled by two gates. One of them is alerted only by drum-select signal PD1 and it produces signal  $\overline{\text{PDW1}}$  high if the flip-flop is set; the output of the gate, together with the outputs of the corresponding gates in the control circuits for other drums, allow the 99 instruction to perform its tests of the drums as one group and in groups of six. The other gate is used specifically for testing the action FF of drum 1; it is alerted by drum-select signal PD1 and sampled by instruction 31 with function signal 831 to generate signal  $\overline{\text{PD1ACT}}$  high if the drum 1 action FF is set.  $\overline{\text{PD1ACT}}$  high causes a transfer of control and resets the flip-flop.

Clear signal  $\overline{\text{EPDMA/G}}$  high, derived from the drum CLEAR pushbutton on the processor control panel, resets the drum-action FF and the jog FF, and sets the forward-reverse FF.

### 3-8. DRUM-HEAD SWITCHING CONTROLS

The head-switching controls for each drum in a system are a group of flip-flops, each of which is set for the connection of its drum to a different synchronizer in the system. The head-switching controls for a given drum synchronizer system therefore contain as many flip-flops as there are drums times the number of synchronizers ( $d \times S = \text{FFs}$ )—from 36 flip-flops in the basic system to 120 in the fully expanded system. These flip-flops generate the signals that cause the relays in the read- and write-switch units to connect any synchronizer to any drum.

Figure 3-1 shows the head-switching control for drum 1 in a fully expanded system. As an example of drum-to-synchronizer connection, assume that a 52 instruction (connect-drum-synchronizer) is decoded and requires drum 1 to be connected to read synchronizer 2 (S2). Function signal 852A, produced at t1, is gated with drum-select signal PD1 to generate signal  $\overline{\text{PD1DC}}$  high. This signal resets all the flip-flops in the drum 1 head-switching control, thereby disconnecting drum 1 from all synchronizers. At the same time, function signal 852A is gated in read synchronizer 2 with synchronizer-select signal PS2 to produce signal  $\overline{\text{S2DC}}$  high, which resets the read-synchronizer 2 FF in the head-switching control of each drum, thereby disconnecting read synchronizer 2 from all drums.

Function signal 852B, produced at t4, is gated in read synchronizer 2 with synchronizer-select signal PS2 and read-synchronizer-2-available signal S2AV to generate signal S2CON. If drum 1 is on remote (processor) control, S2CON sets the read-synchronizer 2 FF in the drum 1 head-switching control. The set output of this flip-flop,  $\overline{Z13}/\overline{PDIR2C}$ , causes the read-switch unit to connect the read bus of drum 1 to the data lines of read synchronizer 2, and to switch the read-write head assembly of drum 1 to the read position.



## SECTION 4

### PROGRAM AND STATUS CONTROLS OF DRUM SYNCHRONIZERS

#### 4-1. GENERAL

The program and status controls are circuits within each drum synchronizer through which the processor program initiates synchronizer operations and monitors both the state of the synchronizers and the stage reached in synchronizer operations. The controls are essentially identical in all drum synchronizers; the program and status control chosen for description and illustrated in figure 4-1 is that of write synchronizer 1 (S3). The minor differences between this control and the controls of other synchronizers are pointed out both in the description and in figure 4-1.

Table 4-1 (page 4-5) is a list of the drum synchronizer instructions.

#### 4-2. SYNCHRONIZER AVAILABILITY

As long as its availability FF is set, drum-write synchronizer 1 is available for use by the processor program. It is set to 'available' by instruction 54 (function signal 854 and PS3) at the end of the last drum-write routine for which the synchronizer was used. The synchronizer clear signal ES3CL high also sets the availability  $\overline{FF}$ . As function signal 854 sets the flip-flop, it also produces signal  $\overline{S3TC}$  (high), which prevents further setting of the sector-change FF, so that the synchronizer is disconnected from the control loop of the program. In drum-write synchronizers only,  $\overline{S3TC}$  (high) and  $\overline{S4TC}$  (high) further generate signals  $\overline{S3DC}$  (high) and  $\overline{S4DC}$  (high), which are sent to the drum-read switching controls to disconnect the drum-write synchronizers from all drums.

Instruction 56 determines synchronizer availability by testing the output of the availability FF (S3AV) with function signal 856 and PS3. If the flip-flop is set, the resulting signal  $\overline{PZ3AV}$  high causes a transfer of control in preparation for connecting the synchronizer to the required drum. The connect instruction (52) resets the availability FF to 'unavailable' with function signal 852B and PS3.

### 4-3. SYNCHRONIZER CONNECTION

The function signals 852A and 852B generated by the connect instruction cause the connection of drum-write synchronizer 1 as follows:

- (1) 852A at  $t_1$  is gated with synchronizer-select signal PS3 to produce signal  $\overline{S3DC}$  high, which disconnects the synchronizer from any drum to which it had previously been connected. (This is the case for all drum synchronizers, whether read or write.) At the same time 852A is gated with the appropriate drum selector signal to disconnect the selected drum from all synchronizers.
- (2) At the same  $t_4$  that 852B applies a reset pulse to the availability FF, it gates with PS3 and the set output of the flip-flop (S3AV) to generate signal S3CON. Signal S3CON is transmitted to the drum-head switching controls to connect the synchronizer to the selected drum, and triggers an 8-msec RDF to allow for relay-switching time in the write-switch unit.

The output of the RDF ( $\overline{S3SSJ}$ ) is single-pulsed to become the connection-complete signal S3CP, which performs the following functions:

- (1) Resets the bad-band FF;
- (2) Sets the no-address FF;
- (3) Triggers the 10-msec RDF;
- (4) Causes the sector-band address-processing circuits to begin reading sector-band addresses from the band over which the head-assembly has been positioned.

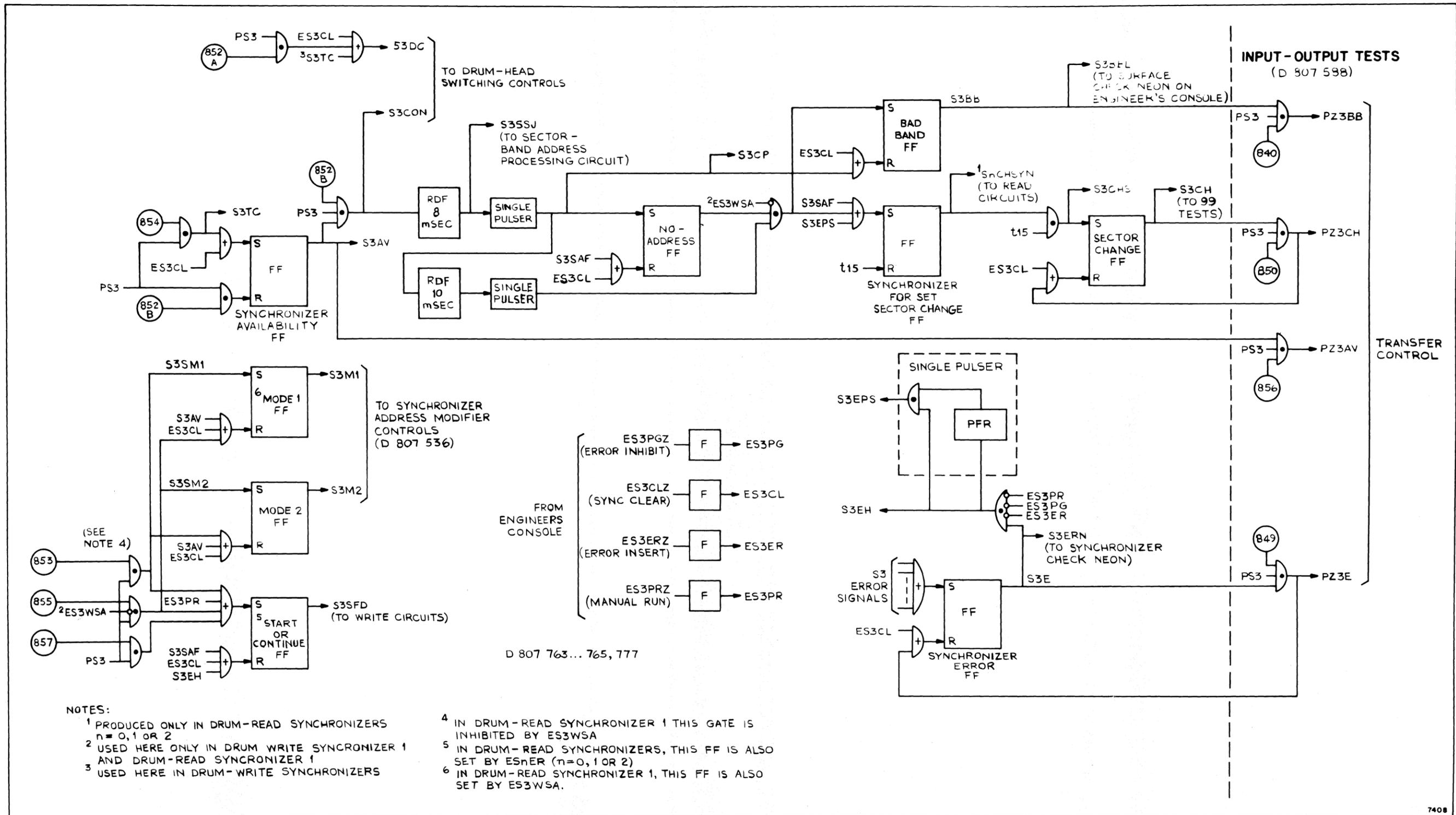
If, by the time the 10-msec RDF recovers, the no-address FF has not been reset by the sector-band address-register-full signal  $\overline{S3SAF}$  high from the sector-band address processing circuits, no sector addresses have been read and the band is considered bad. The set output of the no-address FF is therefore gated with the single-pulsed output of the 10-msec RDF to set the bad-band FF and the synchronizer-for-set-sector-change FF.

The gating of the set output of the no-address FF is inhibited by signal  $\overline{ES3WSA}$  high (from the write-sector-address mode switch on the engineer's console) when drum-write synchronizer 1 is being used for relocating sectors.\*

The set output of the synchronizer-for-set-sector-change FF sets the sector-change FF at  $t_{15}$  to call the program back into the drum control routine (instructions 99 and 50), where instruction 40 samples the output of the bad-band FF with PS3 and function signal 840. When tested, the set output of the bad-band FF (S3BB) generates signal  $\overline{PZ3BB}$  high, which causes a transfer of control to an error routine. Signal S3BB also generates signal Z13/S3BBL, which lights the SURFACE CHECK neon on the synchronizer panel of the engineer's console.

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\* Refer to Appendix A.



- NOTES:
- 1 PRODUCED ONLY IN DRUM-READ SYNCHRONIZERS  
n = 0, 1 OR 2
  - 2 USED HERE ONLY IN DRUM WRITE SYNCHRONIZER 1  
AND DRUM-READ SYNCHRONIZER 1
  - 3 USED HERE IN DRUM-WRITE SYNCHRONIZERS
  - 4 IN DRUM-READ SYNCHRONIZER 1 THIS GATE IS  
INHIBITED BY ES3WSA
  - 5 IN DRUM-READ SYNCHRONIZERS, THIS FF IS ALSO  
SET BY ES<sub>n</sub>ER (n=0, 1 OR 2)
  - 6 IN DRUM-READ SYNCHRONIZER 1, THIS FF IS ALSO  
SET BY ES3WSA.

Figure 4-1. Drum-Write Synchronizer 1 Program Control and Status Circuits

Table 4-1. Drum Synchronizer Instructions

Instruction	Code	Description	Function Signals
Availability Test	56xxSxx MMMMM	Test drum synchronizer S availability FF (S = 0,1,...4). If FF is set (synchronizer available), M → C. If FF is reset (synchronizer unavailable), (C) + 1 → C.	856
Connect Drum Synchronizer	52xxSDD MMMMM	Connect drum synchronizer S to drum DD and reset synchronizer S availability FF to unavailable. (S = 0,1,...4; DD = 01,02,...24). Test local/remote signal from drum DD. If drum is on local control, M → C. If drum is on remote control, (C) + 1 → C.	833 852A 852B
Master Input-Output Priority Test	99xxlxx MMMMM	If sector-change FF of any drum synchronizer is set, M → C.	899
Sector-Change Test	50xxSxx MMMMM	Test sector-change FF of drum synchronizer S (S = 0,1,...4). If FF is set, M → C and reset FF. If FF is reset, (C) + 1 → C.	850
Error Test	49xxSxx MMMMM	Test error FF of drum synchronizer S (S = 0,1,...4). If FF is set, M → C and reset FF. If FF is reset, (C) + 1 → C.	849
Bad-Band Test	40xxSxx MMMMM	Test bad-band FF of drum synchronizer S (S = 0,1,...4). If FF is set, M → C. If FF is reset, (C) + 1 → C.	840
Transfer Sector-Band Address	58xxSxx xxxxx	Transfer contents of sector-address register of drum synchronizer S (S = 0,1,...4) into register P1.	858
Start Synchronizer Mode 1	53xxSxx xxxxx	Set start-continue and mode 1 FFs of drum synchronizer S (S = 0,1,...4), and transfer starting address from register P1 to synchronizer S address register in dispatcher.	853 818
Start Synchronizer Mode 2	55xxSxx xxxxx	Set start-continue and mode 2 FFs of drum synchronizer S (S = 0,1,...4) and transfer starting-address from register P1 to synchronizer S address register in dispatcher.	855 818

Table 4-1. Drum Synchronizer Instructions (cont.)

Instruction	Code	Description	Function Signals
Continue	57xxSxx xxxxx	Set start-continue FF of drum synchronizer S (S = 0,1,...4). Mode 1 is same as previously ordered.	857
Set to Available	54xxSxx MMMM	Set availability FF of drum synchronizer S (S = 0,1,...4) to available. Test error FF of synchronizer S. If FF is set, M → C and reset FF. If FF is reset, (C) + 1 → C. If S = 3 or 4 (write-synchronizer), disconnect synchronizer from all drums.	854 849

#### 4-4. LOCATION OF REQUIRED BAND AND SECTOR

When the head-assembly is positioned over a good band, the no-address FF is reset by signal  $\overline{S3SAF}$  high before the 10-msec RDF recovers, and the bad-band FF remains reset.

Signal  $\overline{S3SAF}$  high, however, also sets the synchronizer-for-set-sector-change FF each time a new sector-band address is read from the drum. As the flip-flop is reset by timing signal t15, its set output is timed to t15 to become signal  $\overline{S3CHS}$  high, which sets the sector-change FF.\*

The set output of the sector-change FF ( $\overline{S3CH}$ ) calls the program into the drum control routine (through the 99 instruction) and is tested by instruction 50 with PS3 and function signal 850; the resulting signal ( $\overline{PZ3CH}$  high) resets the flip-flop and causes a transfer of control to the bad-band and error tests (40 and 49). If neither of these tests is successful, the sector-change FF is known to have been set by the reading of a new sector-band address, and instruction 58 can therefore be issued to determine whether the required sector is about to pass under the head assembly.

#### 4-5. START AND CONTINUE

When the program determines, as a result of the 58 and comparison instructions, that the sector following the one currently under the head assembly is the sector at which data transfers are to begin, it starts synchronizer operations through three flip-flops: the start-or-continue FF, the mode 1 FF, and the mode 2 FF.

The 53 instruction (function signal 853) sets the start-or-continue FF and generates signal  $\overline{S3SM1}$  high to set the mode 1 FF and reset the mode 2 FF. Instruction 55 (function signal 855) also sets the start-or-continue FF but generates signal  $\overline{S3SM2}$  high to set the mode 2 FF and reset the mode 1 FF. Instruction 53 is used for partial-band transfers, and instruction

\* In drum-read synchronizers the outputs of the synchronizer-for-set-sector change FFs are tapped off, untimed, to provide signals  $\overline{S0CHSYN}$ ,  $\overline{S1CHSYN}$ , and  $\overline{S2CHSYN}$  for use in the read circuits.

55 for full-band transfers. Both start instructions are the same except that in mode 2 the synchronizer automatically causes the synchronizer address modifier to subtract 2499 from the memory address from which the last word of sector 24 is transferred, so that the first word of sector 00 is transferred from the first of the memory addresses allocated to the band. The set outputs of the mode flip-flops ( $\overline{S3M1}$  high or  $\overline{S3M2}$  low) are sent to the synchronizer address controls to cause the address modifications appropriate to the mode of synchronizer operation.\* The set output of the start-or-continue FF ( $\overline{S3SFD}$  low) is sent to the write circuits to initiate writing.\*\*

The start instructions initiate synchronizer operations for data transfers to one sector only, since signal  $\overline{S3SAF}$  high resets the start-or-continue FF each time a new sector begins to pass under the head assembly. Thus, for transfers to more than one sector, synchronizer operations for each of the sectors after the first are started by the 57 (continue) instruction, which sets the start-or-continue FF (function signal 857). The 57 instruction neither changes the state of the mode flip-flops nor specifies a new starting address, so that all sectors are processed in the mode and memory-addressing sequence specified by the original start instruction.

Signal  $\overline{ES3CL}$  high from the CLEAR pushbutton on the synchronizer panel of the engineer's console resets all three flip-flops. Both mode flip-flops are also reset by signal  $\overline{S3AV}$  high—that is, when the synchronizer is set to available. In addition to being reset and set by signals already mentioned, the start-or-continue FF is reset by synchronizer error signal  $\overline{S3EH}$  high (heading 4-6) and set by

- (1) Manual run signal  $\overline{ES3PR}$  high from the engineer's console;
- (2) Error insert signals  $\overline{ESOER}$ ,  $\overline{ES1ER}$ , and  $\overline{ES2ER}$  high from the engineer's console, in drum-read synchronizers only.

Note that, when drum-write synchronizer 1 is being used to relocate sectors, signal  $\overline{ES3WSA}$  high from the write-sector-address mode switch on the engineer's console sets the drum-write synchronizer 1 mode 1 FF and prevents the 55 instruction from setting the start-or-continue FF of the same synchronizer.

#### 4-6. SYNCHRONIZER ERRORS

Checking circuits throughout the synchronizer detect various synchronizer error conditions and generate error signals that set the synchronizer error FF as well as the appropriate error diagnostic FFs in the central processor. These signals are listed and described in table 4-2. Since error detection in drum-write synchronizers and drum-read synchronizers is not identical, the error signals produced in drum-read synchronizer 1 ( $S1$ ) are separately listed and described in table 4-3. In both tables the number of the error diagnostic FF set when each error signal is generated is also listed. The number indicates the number and selector digit of

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\* Refer to Section V of the Larc Dispatcher manual.

\*\* In drum-read synchronizers the output of the flip-flop is sent to the read circuits but has no signal designation.

Table 4-2. Drum-Write Synchronizer 1 Error Signals

Error Signal	Name of Signal	Diagnostic FF Set	Condition Generating Error
S3SE1	Start error	47-6	A start instruction is given while the synchronizer is already writing.
S3SE2	Start error	46-9	A start instruction is issued too late to begin writing on sector whose address was last read into sector-address register.
S3CE	Continue error	47-5	No writing is in progress when continue instruction is issued.
S3FLE	Overflow error	46-4	Dispatcher fails to grant word-transfer request in time to maintain flow of information to drum.
S3C2E1	Initial word-count error	47-3	Word-counter does not read 1 when first word of sector is to be written.
S3C2E2	Word-count parity error	47-3	Word count contains even total of 1-bits.
S3TRIME	Trim-current error	46-8	Trim current is on when synchronizer is not being used, or off when synchronizer is writing.
S3PE	Output information parity error	46-6	Output information digit contains even total of 1-bits.
S3TED	Timing error	47-8	Cycling-unit timing error occurs while synchronizer is writing.
S3ADE	Sector-band address parity error	47-1	Sector-address or band-number digit contains even total of 1-bits.
S3MSE*	Memory-select error	46-2	(1) Memory-address digit contains even total of 1-bits, or (2) an improper address is used.
S3E1*	HSB-parity error	46-1	There is even total of 1-bits in digit of word transferred into drum write synchronizer 1 output buffer register.

\* Generated in the central processor.

the instruction that tests the error diagnostic FF. For example, diagnostic FF 47-6 is tested by a 47 instruction with a selector digit of 6.

The synchronizer error FF itself is tested by instruction 49 (function signal 849). If the flip-flop is set, instruction 49 generates signal PZ3E high to reset the flip-flop and cause a transfer of control to an error routine. The set output of the synchronizer error FF (S3E) is further used

- (1) To generate signal Z13/S3ERN, which lights the synchronizer CHECK neon on the engineer's console;
- (2) To generate error signal S3EH low, S3EH high for distribution within the synchronizer. This error signal is inhibited, however, if the ERROR INSERT (signal ES3ER high), ERROR INHIBIT (signal ES3PG high), or MANUAL RUN (signal ES3PR high) push-button is pressed.

Table 4-3. Drum Read Synchronizer Error Signals

Error Signal	Signal Name	Diagnostic FF Set	Condition Generating Error
SISE	Start error	47-6	Start instruction is given when synchronizer is already reading or when it is too late to begin reading from required starting sector.
SICE	Continue error	47-5	No reading is in progress when continue instruction is issued.
SIFLE	Overflow error	46-4	Dispatcher fails to grant word-transfer request in time to maintain flow of information from drum.
SIPE	Input information parity error	46-5	Input information digit contains even total of 1-bits.
SIPCE	Information parity checker error	47-2	Malfunction exists in input information parity checker.
SISLE1	Sector-length error	47-3	End-of-sector sentinel is detected before word counter indicates end of sector.
SISLE2	Sector-length error	47-4	Word counter indicates end of sector before end-of-sector sentinel is detected.
SIOSK	Overskew error	47-8	Head assembly skew exceeds capacity of one or more channel information registers.
SIAD E	Sector-band address parity error	47-1	Sector-address or band-number digit contains even total of 1-bits.
SIMSE*	Memory-select error	46-2	(1) Memory-address digit contains even total of 1-bits, or (2) an improper address is used.
SIE1*	HSB-parity error	46-1	There is even total of 1-bits in digit of word transferred from drum-read synchronizer 1 input buffer register.

\* Generated in the central processor.

$\overline{S3EH}$  high is single-pulsed to provide the 0.5- $\mu$ sec error signal  $\overline{S3EPS}$  high, also for distribution within the synchronizer.

In the program and status control, signal  $\overline{S3EH}$  high resets the start-or-continue FF, and signal  $\overline{S3EPS}$  high sets the sector-change FF through the synchronizer-for-set-sector-change FF. The set state of this latter flip-flop calls the program into the drum control routine through the 99 and 50 instructions, and the 49 instruction is then the first test made.



## SECTION 5

### SECTOR-BAND ADDRESS CIRCUITS OF DRUM SYNCHRONIZERS

#### 5-1. GENERAL

The sector-band address circuits of the drum synchronizers allow the program to determine which bands and sectors on a drum pass under the head assembly. Basically the circuits provide temporary storage for the band number and sector address which are read serially from channel 6 at the beginning of each sector before being transferred in parallel to register P1 in the central processor.

The sector-band address circuits of all drum synchronizers are almost identical. The circuit illustrated in figure 5-1 and described in this section is that of drum-write synchronizer 1; it is chosen to represent the sector-band address circuit of any drum synchronizer. The differences between the sector-band address circuit described and the circuits in other drum synchronizers are noted both in figure 5-1 and in the text.

The circuit is divided for discussion purposes into the three sections shown in figure 5-1:

- (1) Input and self-sprocketing circuit;
- (2) Synchronization circuit;
- (3) Sector-address and band-number register and controls.

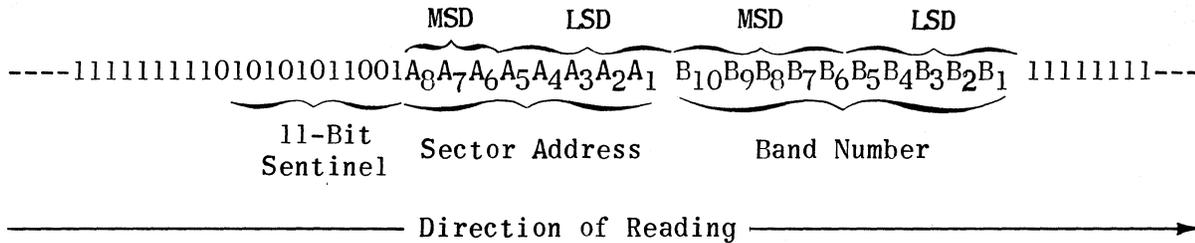
Note that the alphabetic designations given to certain gates and flip-flops in figure 5-1 are purely for discussion purposes.

#### 5-2. SECTOR ADDRESSES AND BAND NUMBERS

The data recorded in channel 6 at the beginning of each sector consist of an 11-bit sentinel, the address of the following sector, and the band number. The sector address is a 2-digit number (00-24), the LSD is a Larc 5-bit digit (four information bits plus check bit), and the MSD, since it has a maximum count of 2, contains only two information bits plus check bit. The band number is a Larc code 2-digit number (00-99); thus



the sector address and band number contain a total of 18 bits. The sequence of these bits and the sentinel is as follows:



### 5-3. INPUT AND SELF-SPROCKETING CIRCUIT

The information from the sector-address channel on the drum (DSAR3A/DSAR3B) enters the synchronizer through the special drum-read amplifier. The output from the amplifier is a sinewave the zero crossings of which correspond to peak voltages picked up from the drum. The + and - outputs are 180 degrees out of phase. The output from either side of the amplifier triggers a corresponding Schmitt-trigger A-type circuit. The Schmitt circuit is chosen to provide a negative pulse of fixed duration, starting from a positive-going zero crossing at its input.

The outputs from the ST-A circuits are negative-going 0.3- $\mu$ sec pulses which open gates A and B. Depending on whether the input signal represents a 1 or a 0, gate A or B opens to produce a corresponding 1 ( $\overline{S3ADIS}$  high) or 0 ( $\overline{S3ADOS}$  high) information signal which is fed to both the self-sprocketing and the synchronization circuits. For the self-sprocketing operation, gates A and B are controlled by the output of FF A. During the 8-msec connection time, signal  $\overline{S3SSJ}$  high from the program and status controls keeps FF A set to inhibit both gates A and B. The connection-complete signal  $\overline{S3CPD}$  high then resets the flip-flop so that the gates are alerted to pass the first information pulses from the drum.

The outputs of gates A and B are connected to a long-delay element (LD). After a delay of approximately 0.33  $\mu$ sec, a positive output from terminal C of the LD unit sets FF A. After a delay of approximately 1.35  $\mu$ sec, an output from terminal D resets the flip-flop. While the flip-flop is set, gates A and B are inhibited. The timing of the inhibit pulse is such that it covers the possible times of any "auxiliary" zero crossings—that is, zero crossings that result from recording two or more consecutive like bits. The first relevant bit to enter the synchronizer is the 0-bit that precedes the 11-bit sentinel. Occurring at a significant zero crossing, the 0-bit adjusts the inhibiting action of FF-A to the times of non-significant zero crossings so that the self-sprocketing circuits will correctly read the sentinel, sector address and band number bits.

### 5-4. SYNCHRONIZATION CIRCUIT

The sector-address synchronization circuit consists of two asynchronous flip-flops (FFB and FFC) and two single-pulsers (1 and 2). The purpose of the circuit is to synchronize each sequential sentinel, sector-address, and

band-number bit to the pulseformer clock pulses at the earliest time possible. The circuit is designed to meet the most stringent timing requirements that can be expected with the arrival of two consecutive asynchronous binary 1's and 0's from the drum.

Input information pulses  $\overline{S3AD1S}$  and  $\overline{S3AD0S}$  set FFB and FFC, respectively. For the worst case assume that two input pulses correspond to consecutive binary 1's occurring at the minimum pulse repetition period of 1.6  $\mu$ sec. After FF B is set by the first pulse, a synchronized pulse must be generated from the output of single-pulsers 1 and fed back to reset the flip-flop before the arrival of the next pulse. The criterion for establishing this requirement is that the minimum pulse width (W) received from the input circuits be specified as this:

$$W \geq 2 \Delta S + 45 \text{ m}\mu\text{sec}$$

where  $\Delta S$  is the maximum delay of an S-type circuit.

## 5-5. SECTOR-BAND ADDRESS REGISTER AND CONTROLS

The sector-band address register is an 18-bit shift register composed of 18 flip-flops. The sentinel, sector-address, and band-number bits from the single-pulsers of the synchronization circuit enter the least significant bit position of the register (FF1) and are shifted right, one place at a time. Input to the register is controlled by the gate-sector-address FF and the sector-address-register-available FF. The gate-sector-address-full FF and associated logic provides the synchronizer and the program with control signals that indicate when the register contains a legitimate sector address and band number.

## 5-6. READING FIRST SECTOR ADDRESS AFTER CONNECTION

The gate-sector-address FF is initially set by connection-complete signal  $\overline{S3CPD}$  high to generate signal  $S3GADS$ , which alerts gates C, D, and E. Output signal  $S3SNX$  from single-pulsers 1, representing a 1-bit, opens all three gates to produce information signal  $S3SN$  low and sprocket signals  $\overline{S3SAS}$  high,  $S3SAS$  low.  $\overline{S3SAS}$  breaks the recirculation paths of all flip-flops in the register while  $S3SAS$  shifts the contents of the register one place to the right and  $S3SN$  sets FF1 to introduce the 1-bit. An output from single-pulsers 2, representing a 0-bit, opens gates D and E only, so that the signals produced are  $S3SN$  high,  $\overline{S3SAS}$  high, and  $S3SAS$  low. The latter two signals act as previously described while  $S3SN$  high resets FF1 of the register to introduce the 0-bit.

When the first 10 bits of the sentinel have been shifted into the first 10 flip-flops of the register and the remaining 1-bit is present at the output of single-pulsers 1 ( $S3SNX$ ), the first-sentinel-detecting gate opens to produce signals  $\overline{S3ADFS}$  and  $\overline{S3ADFSX}$ , both high.  $\overline{S3ADFS}$  clears every flip-flop in the register except FF1, and resets the gate-sector-address-full FF (initially set by  $\overline{S3CPD}$  high\*). The reset output of the gate-sector-address-full FF ( $S3GSAF$ ) alerts gate F. Signal  $\overline{S3ADFSX}$  blocks gate E so

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\*The flip-flop is also set by (1) synchronizer-clear signal  $\overline{ES3CL}$ , (2) synchronizer-error signal  $\overline{S3EH}$  (in drum-write synchronizer 1 only), and (3) the output of gate G, which detects illegitimate sector addresses (heading 5-8).

that the signals produced by the remaining 1-bit (S3SNX) of the sentinel are S3SN low,  $\overline{S3SAS}$  high, and S3SAS high—a combination which results in the storing of the 1-bit in FF 1 of the register.\*

The successive bits of the sector address and band number enter the synchronizer and are shifted along the register. By the time the remaining 1-bit of the sentinel occupies the 18th flip-flop of the register, only the last bit of the band number remains to enter the register. The set output of the 18th flip-flop (S3A8) provides a second alerting signal for gate F, which opens as soon as the sprocket signal S3SAS is generated for the last bit of the band number. In drum-write synchronizer 1 only, gate F is inhibited by the write-sector-address mode signal  $\overline{ES3WSA}$ . The output of gate F ( $\overline{S3GADSR}$  high) does the following:

- (1) It sets the gate-sector-address-full FF;
- (2) It resets the gate-sector-address FF to prevent the transfer of further information from channel 6;\*\*
- (3) It sets FF-D.

The set output of FF-D (S3SAFC) therefore indicates that the register now contains a complete sector address and band number; S3SAFC is gated with timing signal t2 to generate register-full control signal S3SAF.

S3SAF, S1SAF, and S2SAF in drum-read synchronizers are not timed; in drum-read synchronizer 1, during sector-address writing, the effect of S1SAFC is blocked by  $\overline{ES3WSA}$ , and S1SAF is generated by signal  $\overline{S3DRP}$ , which is produced in the drum-write synchronizer 1 write circuits. Further, in drum-read synchronizers, FF-D is replaced by a pulseformer.

S3SAF performs the following functions:

- (1) It resets FF-D;
- (2) It prepares the write circuits for operation;
- (3) It sets the sector-address-register-available FF;
- (4) It causes the sector-change FF to be set, thereby alerting the program to the fact that the sector address and band number may now be transferred to register P1.

When the program issues the 58 instruction, function signal 858 generates signal S3SAR, which gates the sector-band address register contents to register P1.

## 5-7. READING SECTOR ADDRESSES OTHER THAN FIRST

The process of transferring the bits of the sentinel, sector address, and band number from the synchronization circuit through the sector-band

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\* Note that  $\overline{S3ADFS}$  is also generated initially by S3CP in order to clear the register.

\*\* Other resetting signals to the flip-flop are (1) synchronizer-clear signal  $\overline{ES3CL}$ , (2) synchronizer-error signal  $\overline{S3EH}$ , (3) signal  $\overline{S3TC}$ , produced by the 54 instruction, and (4) write-sector-address mode signal  $\overline{ES3WSA}$  (in drum-write synchronizer 1 only).

address register to register P1 is the same for any sector read, except that after connection, for sectors other than the first, the connection-complete signal  $\overline{S3CPD}$  high is not present to set the gate-sector-address and gate-sector-address-full FFs.

Signal  $\overline{S3GADSR}$  (as already pointed out) resets the gate-sector-address FF to block gates C, D, and E as soon as a sector address and band number have been read into the sector-band address register. In drum-read synchronizers the signals that set the flip-flop again for each succeeding sector are S0SAF, S1SAR, and S2SAR; that is, gates C, D and E are alerted again as soon as the contents of the sector-band address register are transferred to register P1.

In drum-write synchronizers, however, the gate-sector-address FF cannot be set again to alert gates C, D, and E until 30  $\mu$ sec after a synchronizer has finished writing a sector. The 30- $\mu$ sec delay is the time required to "unblock" the read amplifiers for channel 6 after the removal of write current from the other five channels. Thus the gate-sector-address FF on figure 5-1 is set for each succeeding sector after the first by signal  $\overline{S3GADSS}$  high, which is derived as follows:

- (1) When the sector-band address register becomes full, signal  $\overline{S3SAF}$  high sets the sector-address-register-available FF to "unavailable." \*
- (2) As it transfers the sector-band address to register P1, S3SAR also resets the flip-flop back to "available" and triggers a 30- $\mu$ sec RDF, provided that signal  $\overline{S3WCB}$  from the write circuits is low to indicate that no writing is in progress.
- (3) The output of the RDF is single-pulsed to become signal  $\overline{S3GADSS}$  high, which sets the gate-sector-address FF.
- (4) If writing is in progress ( $\overline{S3WCB}$  high) at the time S3SAR is generated, the RDF is triggered by the reset output of the sector-address-register-available FF (S3ARA) as soon as signal S3WCR from the write circuits indicates that writing is about to end.

#### 5-8. ILLEGITIMATE SECTOR ADDRESSES

Misrecording in channel 6 could produce a false sentinel which would allow the sector-band address register to be filled with the 1-bits recorded between each sector-band address and the next. Thus the band number and sector address in the register would be 88 28—an illegitimate sector address. Gate G on figure 5-1 therefore detects the last bit of the false sentinel shifted to FF 18 (S3A8) and a sector address greater than 24 (S3A6-S3A3). The output of gate G sets the gate-sector-address-full FF to prevent the generation of register-full control signal S3SAF.

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\* The flip-flop is also set by (1) synchronizer-clear signal  $\overline{ES3CL}$ , (2) signal  $\overline{S3TC}$ , produced by the 54 instruction, and (3) write-sector-address mode signal  $\overline{ES3WSA}$ .

\*\* The flip-flop is also reset by the manual run signal  $\overline{ES3PR}$ .

For sectors other than the first one which is read after connection, a series of 1-bits is read into the register ahead of the sentinel. Thus, as the first sentinel signal  $\overline{S3ADFS}$  applies a reset pulse to the gate-sector-address-full FF, it also inhibits gate G to prevent the reset pulse from being overridden.

## 5-9. SECTOR-BAND ADDRESS PARITY CHECK

The sector address and band number bits are checked for odd parity by the sector-band-parity-check FF. The flip-flop is initially reset by the first sentinel signal  $\overline{S3ADFS}$  high. Thereafter, every 1-bit in the sector address and band number transferred into the register changes the state of the flip-flop. If each of the four digits of the sector-band address contains an odd total of 1-bits (as it should), the flip-flop changes state an even number of times during the 18-bit transfer and ends up reset. Should the flip-flop be in the set state when the register-full signal  $S3SAF$  is produced, error signal  $\overline{S3ADE}$  high is generated to set the synchronizer error FF and error diagnostic FF 47-1.

## SECTION 6

### WRITE CIRCUITS

#### 6-1. GENERAL

The write circuits of both drum-write synchronizers in the expanded system are essentially identical, except for additional logic included in drum-write synchronizer 1 for the writing of sector addresses. The write circuit described in this section and illustrated in figure 6-1 is that of drum-write synchronizer 1.

The circuit consists of a set of control flip-flops, word and digit counters, and a write-waveform generator for each of the five information channels (A, B, C, D, and E) of a band.

The write operation is basically a process of transferring each digit to be recorded—all five bits in parallel—from an output buffer register to the five write-waveform generators; through its associated drum-write amplifier each generator produces a waveform that crosses the zero axis, in the appropriate direction and at the significant time, to cause a 1- or 0-bit to be recorded on the drum.

Any sector that passes under the head assembly between the time the synchronizer is connected and the time a write operation begins is known as a nonwriting sector. During such a sector, a buffer-clear cycle and word- and digit-counter stepping are performed, but no information is transferred to the write-waveform generators.

Since the address of the sector at which the program requires a write operation to begin is recorded at the beginning of the preceding sector, the program issues the start instruction during a nonwriting sector. The start instruction, stored by the start-or-continue FF remains ineffective until the following sector moves under the head assembly. Thus, in mode 2 there is only one nonwriting sector—the first sector to pass under the head assembly after connection. In mode 1 there are as many nonwriting sectors as are necessary to reach the starting sector.

During each writing sector the program determines whether to issue the continue instruction for writing on the following sector. The continue instruction is therefore also stored by the start-or-continue FF.

Prior to recording memory information in a sector, the synchronizer records in each information channel a starting sequence of alternate 1- and 0-bits ending in a sentinel of two consecutive 1-bits. The memory information immediately follows the sentinel. The time taken to record the starting sequence and sentinel is approximately 54  $\mu$ sec.

When the 100th word of memory information has been recorded in a sector, the synchronizer records a 1-bit in channels A, B, C, and E and a 0-bit in channel D. This 10111 bit combination is the end-of-sector sentinel.

## 6-2. WRITE-WAVEFORM GENERATORS

In the phase-modulation method of recording, the direction of the current waveform as it crosses the zero axis at a particular phase of each cycle determines whether a 1 or a 0 is recorded. The convention used in the Larc system is based on the polarity of the waveform at the output of the write-waveform generators: a 1 is written for a positive-going zero crossing, and a 0 for a negative-going zero crossing.

Figure 6-1 shows the write-waveform generator for channel X\*. The generator consists of (1) a pulseformer-type flip-flop connected as a binary counter and (2) an associated drum-write amplifier. The flip-flop changes state every 2  $\mu$ sec under control of timing signal t04 from the central processor, so that with no input information the generator oscillates at a fixed frequency of 250 kc. The outputs of the flip-flop are connected to the drum-write amplifier through control gates that are inhibited by write control signal S3WC high when no writing is in progress. When the synchronizer is writing, however, the flip-flop output is gated to the amplifier to produce waveforms (signals S3WDX\*, S3WDX\*) that are transmitted over the write bus to the read-write head in the connected drum. Amplifier output is 180 degrees out of phase with the output of the flip-flop.\*\* The control gates are inhibited also by S3EH (high) when a synchronizer error occurs and by synchronizer-clear signal ES3CL (high).

Significant zero crossings occur at the output of the write-waveform generator at late t4—early t5, and late t0—early t1. During a write operation, information pulses (S3LBn<sup>†</sup>) from the buffer register arrive at the write-waveform generator flip-flop at t26 together with resetting signal S3WWGR (high). If S3LBn is high to represent a 1-bit, it overrides S3WWGR to set the flip-flop (if it is not already set), so that at the following t04 the zero crossing at the amplifier output is positive-going to write a 1. If S3LBn is low to represent a 0-bit, signal S3WWGR resets the flip-flop (if it is not already reset), so that at the following t04 the zero crossing at the amplifier output is negative-going to write a 0. Thus the information pulses arriving at t26 double the number of possible zero crossings and provide a basic writing frequency of 500 kc.

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\* X = A, B, C, D, or E.

\*\* For full description of write-waveform generators, refer to Section I of the Larc Circuitry manual.

† If X = A, n = 1.  
If X = B, n = 2.  
If X = C, n = 3.  
If X = D, n = 4.  
If X = E, n = 5.

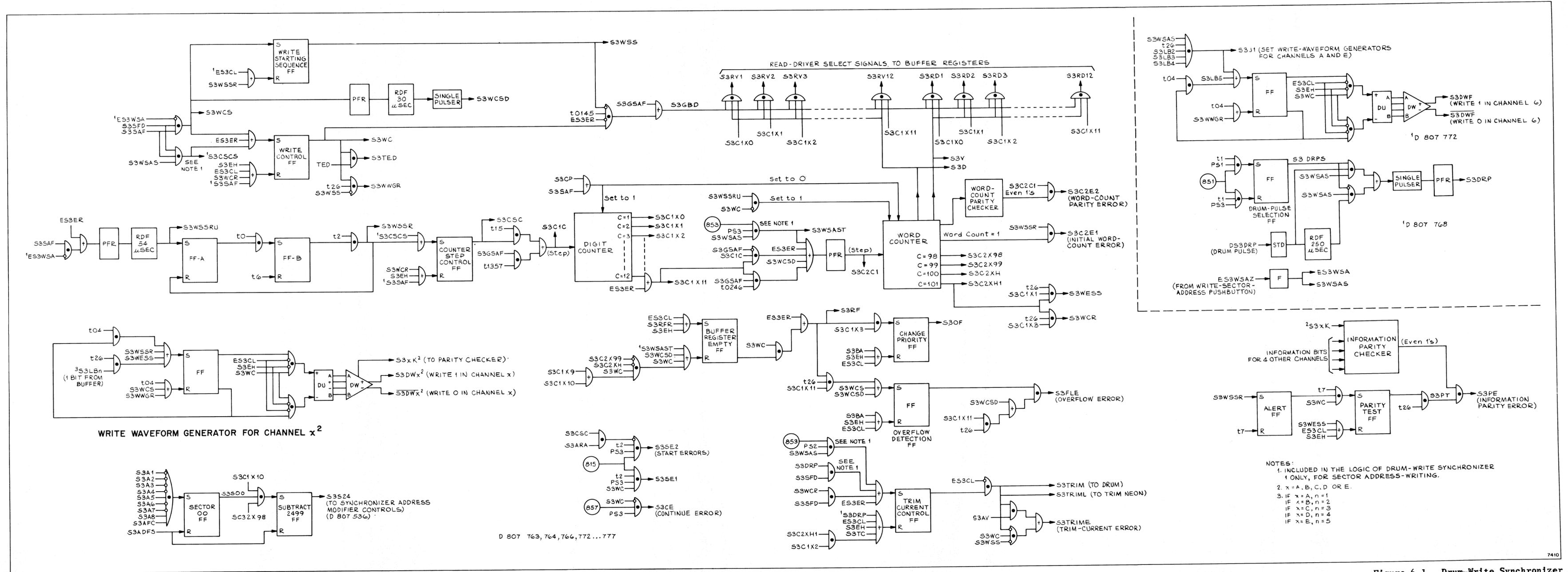


Figure 6-1. Drum-Write Synchronizer 1 Write Circuits

The waveforms that write the starting sequence and sentinel at the beginning of each sector are produced through the write-waveform generators in the following manner (figure 6-2). As soon as the sector-band address register is filled, signal  $S3SAF$  produces signal  $\overline{S3WCS}$  (high), which resets the generator flip-flop at  $t_2$  (if it is not already reset), so that the starting sequence will begin at the following  $t_4$  with a 0-bit. At  $t_3$ , write control signal  $S3WC$  goes low for the rest of the sector to open the generator control gates. During the following 54  $\mu\text{sec}$  the generator flip-flop changes state every 2  $\mu\text{sec}$  at  $t_4$  so that the starting sequence of alternate 1's and 0's is recorded. At the first  $t_2$  after the 54- $\mu\text{sec}$  delay, which ends with the recording of a 1, signal  $\overline{S3WSSR}$  (high) sets the flip-flop so that at the following  $t_4$  a second 1 is recorded, thereby providing the sentinel of two consecutive 1-bits. Immediately after the sentinel the information pulses from the buffer register set and reset the flip-flop as already described.

At the end of each sector, end-of-sector signal  $\overline{S3WESS}$  (high) is generated at  $t_{26}$  to set the generator flip-flops of channels A, B, C, and E, and reset the generator flip-flop for channel D. Thus, at the following  $t_{04}$ , the end-of-sector sentinel 1 0 1 1 1 is written.

### 6-3. DIGIT COUNTER

The digit counter performs two main functions for the synchronizer:

- (1) It keeps track of the number of digits that have been transferred from a buffer register\* at any given time;
- (2) It controls buffer-register readout by producing the sequential buffer-read signals  $S3RV1$ — $S3RV12$  and  $S3RD1$ — $S3RD12$ .

The digit counter consists of four flip-flops and a set of decoding gates. The outputs of the flip-flops ( $S3C10$ ,  $\overline{S3C10}$  through  $S3C13$ ,  $\overline{S3C13}$ ) are fed back in such a way that successive applications of a step signal ( $S3CIC$ ) cause the flip-flops to act as a counter which produces a maximum of 12 counts in the code shown in table 6-1.

During normal buffer readout the digit-counter step signal ( $S3CIC$ ) is derived from the set output of the counter step control FF ( $S3CSC$  low) at  $t_{15}$ . The flip-flop is set by signal  $\overline{S3WSSR}$  (high) when the starting sequence and sentinel have been recorded, and is not reset until signal  $\overline{S3WCR}$  (high) occurs at the end of the sector. The flip-flop is also reset by  $\overline{S3EH}$  (high) whenever a synchronizer error occurs. (In drum-write synchronizer 1 only, an additional resetting signal is the sector-band-address-register-full signal  $\overline{S3SAF}$  (high) and an additional setting signal is  $S3CSCS$  (high); both are used in the writing of sector addresses.)

During a buffer-clear cycle, step signal  $S3CIC$  is derived from the gate-sector-address-full signal  $S3GSAF$  at  $t_{1357}$ .

The decoding gates decode the outputs of the digit counter flip-flops to produce one output signal for each of the 12 counts,  $S3CIX0$ — $S3CIX11$ .

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\* Each drum synchronizer has two buffer registers (odd and even).

Table 6-1. Digit Counter Code

FF4	FF3	FF2	FF1	Decimal Count
0	0	0	0	0
0	0	0	1	1
0	0	1	1	2
0	1	1	1	3
0	1	1	0	4
0	1	0	0	5
1	1	0	0	6
1	1	1	0	7
1	1	1	1	8
1	0	1	1	9
1	0	0	1	10
1	0	0	0	11

In addition to being distributed to other parts of the write circuits for control purposes, the digit-counter output signals are applied to the two groups of buffer-read-driver gates that produce the core-select signals for the synchronizer's two output buffer registers. Both groups of gates are alerted by control signal S3GBD when buffer readout is required. If the even buffer register contains the word to be written, word-counter output signal S3D alerts the 12 gates through which signals S3C1X0—S3C1X11 generate buffer-read signals S3RV1—S3RV12, respectively. When the odd buffer register contains the word to be written, word-counter output signal S3V alerts the 12 gates through which S3C1X0—S3C1X11 generate buffer-read signals S3RD1—S3RD12, respectively.

The digit counter is initially cleared to S3C1X0 by the connection-complete signal S3CPD (high). At the beginning of each sector after connection, the counter counts at least twice from 0 through 11 while the sector-band address register is being filled, thereby clearing both buffer registers of any residual information and ensuring that only new information from the memory will be written on the drum. As soon as the sector-band address register is filled, signal S3SAF (high) clears the counter to S1C1X0 so that the first digit word of the sector is transferred from the proper cores in the buffer register.

Each time a word of a sector is written—that is, each time the digit counter reaches S3C1X11—the next step signal sets the counter back to S3C1X0 to read out the first digit of the next word. The reversion from S3C1X11 to S3C1X0 also produces the word-counter step signal S3C2C1.

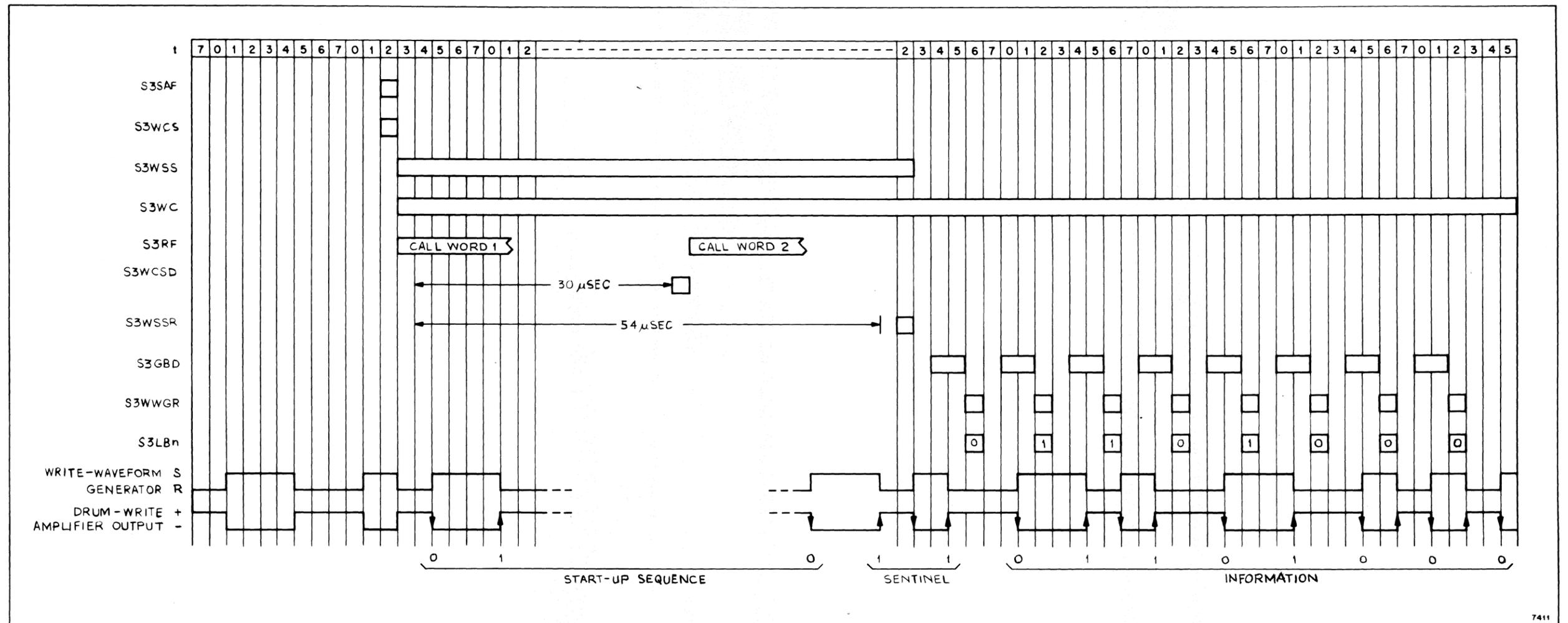


Figure 6-2. Timing for Starting Sector-Write Operation

## 6-4. WORD COUNTER

The word counter is composed of eight flip-flops. Seven of them are connected as a seven-stage counter that operates on the code shown in table 6-2; the eighth flip-flop provides the correct parity check bit for each count. The counter is stepped up by one count each time the digit counter passes its highest count—that is, each time a word has been transferred from one of the synchronizer's output buffer registers. Thus the word counter keeps track of the number of words transferred and thereby indicates when a sector transfer of 100 words is complete.

Table 6-2. Word Counter Code

(Check Bit) FF8	FF7	FF6	FF5	FF4	FF3	FF2	FF1	Decimal Count
1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
1	0	0	0	0	0	1	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	1	0	0	4
1	0	0	0	0	1	0	1	5
0	0	0	0	0	1	1	1	6
1	0	0	0	0	1	1	0	7
1	0	0	0	1	1	0	0	8
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	95
0	1	1	1	0	0	0	0	96
1	1	1	1	0	0	0	1	97
0	1	1	1	0	0	1	1	98
1	1	1	1	0	0	1	0	99
1	1	1	1	0	1	0	0	100
0	1	1	1	0	1	0	1	101

The word-counter step signal ( $S3C2C1$ ) is produced through a pulse-former in the following ways:

- (1) A buffer-clear cycle precedes each sector and is performed while signal  $S3GSAF$  indicates that the sector-band address register is receiving the sector address and band number. During this cycle, word-counter step signal  $S3C2C1$  is derived from the highest count of the digit counter ( $S3C1Y11$ ) and timed to  $t1357$ .
- (2) While a sector is being written or while the nonwriting sector is passing under the head assembly, step signal  $S3C2C1$  is produced at  $t26$  when the digit count is 12 ( $S3C1X11$ ) and a digit-counter step occurs ( $S3CIC$ ).
- (3) At the beginning of each sector, signal  $\overline{S3SAF}$  (high) clears the word counter to 0\*. The counter is then jammed to 1 in preparation for the nonwriting sector by signal  $S3WSSRU$ , which produces signal  $S3C2S1$  (high) to set FF1 and reset FF8 of the counter. In preparation for each succeeding sector, signal  $S3WCSD$  (high) generates step signal  $S3C2C1$  to step the counter from 0 to 1, and the set signal  $S3WC$  (high) from the write control FF prevents  $S3WSSRU$  from generating  $S3C2S1$  (high).
- (4)  $\overline{S3WSAST}$  (high), the remaining signal that generates the word-counter step signal, is derived as indicated on figure 6-1 for use in the writing of sector addresses.

$S3C2C1$  directly steps only the two lowest-order flip-flops in the counter (FF2 and FF1). When FF2 and FF1 contain the combination 1 0 ( $S3C21 \cdot S3C20$ ), respectively—that is, after every fourth step—the next  $S3C2C1$  signal generates a second step signal ( $S3C2C2$ ) which steps FF4 and FF3. Similarly, when FF4 and FF3 contain the combination 1 0 ( $S3C23 \cdot S3C22$ ), respectively—that is, after every 16th step—signal  $S3C2C2$  generates a third step signal,  $S3C2C3$ , which steps FF6 and FF5. When the counter reads 63 ( $S3C25 \cdot S3C24$ ), signal  $S3C2C3$  sets FF7 for the rest of the counting sequence. FF8 changes state under control of  $S3C2C1$  to provide the necessary check bit ( $S3C27$  or  $\overline{S3C27}$ ) for each count.

A set of gates decodes the outputs of the word-counter flip-flops for counts of 98, 99, 100, and 101, to produce control signals  $S3C2X98$  ( $S3C2Y98$ ),  $S3C2X99$ ,  $S3C2XH$ , and  $S3C2XH1$ , respectively. By the time the counter reads 101, the 100th word of a sector has been transferred.

Notice from table 6-2 that the two lowest-order flip-flops alternately contain a like bit combination ( $S3C20 \cdot S3C21$  and  $\overline{S3C20} \cdot \overline{S3C21}$ ) and an unlike bit combination ( $S3C20 \cdot \overline{S3C21}$  and  $\overline{S3C20} \cdot S3C21$ ). The outputs of these flip-flops therefore provide an indication of the next buffer register (odd or even) from which a word is to be transferred. Each like bit combination generates even-count signal  $S3V$ , and each unlike bit combination generates odd-count signal  $S3D$ . As shown in figure 6-1, signals  $S3V$  and  $S3D$  alert the read-driver gates of the odd and the even buffer register,

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\* As soon as connection is complete, signal  $\overline{S3CPD}$  (high) also clears the word counter to 0 in preparation for the first buffer-clear cycle.

respectively. This apparent inconsistency results from the fact that the word transferred from the memory to an output buffer register always leads by 1 the word-counter reading.

Signals S3V and S3D are transmitted also to the address- and buffer-register controls in the dispatcher to specify the buffer register (even and odd respectively) to which the next word from the memory is to be transferred.

When the word counter indicates by control signal S3C2XH1 that the 100th word has been written and the digit counter reaches a count of 2 (S3C1X1), signal S3WESS (high) is generated at t26 to cause the end-of-sector sentinel to be written. At a t26 4  $\mu$ sec later, when the digit counter has stepped to 4 (S3C1X3), control signal S3WCR (high) is generated to end the write operation for the sector.\*

#### 6-5. MEMORY ACCESS CONTROL

The synchronizer requests the transfer of a word from the memory to one of its output buffer registers by transmitting signal S3RF (low) to the priority circuits in the dispatcher. As shown in figure 6-1, S3RF (low) is produced in the synchronizer either by error-insert signal  $\overline{\text{ES3ER}}$  (high) or, during the writing of a sector (S3WC low), by the reset condition of the buffer-register-empty FF. When a requested transfer has been started, the priority circuits transmit signal  $\overline{\text{S3RFR}}$  (high) to set the flip-flop, thereby cancelling the request.

Signal  $\overline{\text{S3WCS}}$  (high), produced at the beginning of the starting sequence of each writing sector, resets the buffer-register-empty FF to request the transfer of the first word of a sector.  $\overline{\text{S3WCS}}$  also triggers a 30- $\mu$ sec RDF, the output of which is single-pulsed to become  $\overline{\text{S3WCSD}}$  (high).  $\overline{\text{S3WCSD}}$  resets the flip-flop again to request the transfer of the second word. The flip-flop is reset to request each succeeding word transfer of a sector whenever the 10th (S3C1X9) or 11th (S3C1X10) digit of the word being written is transferred to the write-waveform generators.

Since the first two word transfers of a sector are requested during the starting sequence that is, before actual writing begins—the request for each succeeding word is made during the processing of the word that precedes it by 2. Thus the requests for the 99th and 100th words are made during the writing of the 97th and 98th words respectively. Word count signals S3C2X99 and S3C2XH therefore prevent the buffer-register-empty FF from being reset during the 99th and 100th words.

The imminence of overflow on the synchronizer is indicated if the transfer request for word n is still not granted (S3RF low) by the time the fourth digit (S3C1X3) of word n - 1 is transferred to the write-waveform generators. These conditions set the change-priority FF to

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\* Digit count S3C1X3 is used to indicate the end of a sector rather than S3C1X0, since the write current must remain on for several microseconds after the writing of the last word as a safety measure to remove the "end-of-write" current transient from the last information digit. Also, 2  $\mu$ sec are needed to write the end-of-sector sentinel.

generate overflow signal  $\overline{S30F}$  (high).  $\overline{S30F}$  then causes the priority circuits to assign to the synchronizer's word-transfer request higher priority than that assigned to any other synchronizer.

In both modes of synchronizer operation, word transfers are made from sequential memory locations. Thus mode control signals  $S3M1$  and  $S3M2$  from the program and status controls (figure 4-1) cause the synchronizer address modifier in the dispatcher to add 1 to each memory address from which a word is transferred.

For a mode 2 operation, however, the synchronizer must also cause the address modifier to subtract 2499 from the address of the last word of the 24th sector of a band. For this purpose the write circuits include a sector-00 FF and a subtract-2499 FF. Both flip-flops are reset initially at the beginning of each sector by the sentinel-detected signal  $\overline{S3SADFS}$  (high). The sector-00 FF remains reset until the sector-band address register contains 00. Since the sector address precedes by one sector the sector to which it refers, a register content of 00 indicates that sector 24 is currently under the head assembly.

The set output of the sector-00 FF ( $S3S00$  (low)) alerts the setting gate to the subtract-2499 FF. When the digit and word counters indicate by signals  $S3C1X10$  and  $S3C2X98$ , respectively, that the request for the 100th word is being made, the subtract-2499 FF is set to generate signal  $S3S24$  (low).  $S3S24$  is sent to the synchronizer address-modifier controls to cause 2499 to be subtracted from the address of the 100th word so that the first word of sector 00 will be transferred from the first memory location allotted to the band.

The sector-00 and subtract-2499 FFs are duplicated for checking purposes.

## 6-6. OVER-ALL OPERATION

The remaining elements of the write circuit, other than the various error detectors, are best described within the context of the over-all operation of the circuit. The over-all operation can be divided into three distinct sequences:

- (1) The buffer-clear cycle;
- (2) The nonwriting sectors;
- (3) The writing sectors.

### 6-7. BUFFER-CLEAR CYCLE

A buffer-clear cycle occurs at the beginning of each sector (writing and nonwriting) as soon as the sentinel-detected signal  $\overline{S3ADFS}$  (high) resets the gate-sector-address-full FF in the sector-band address processing circuits to generate signals  $S3GSAF$  (low),  $\overline{S3GSAF}$  (high). These signals effect the buffer clear cycle as follows:

- (1)  $\overline{S3GSAF}$  generates signal  $S3GBD$  (low) to alert both sets of buffer-read-driver gates throughout the cycle.

- (2) S3GSAF generates digit-counter step signal S3C1C every microsecond at t1357. The sequential digit-counter output signals S3C1X0—S3C1X11 read out any residual digits in whichever buffer register is indicated by the current odd-even count of the word counter (S3V or S3D). Any digit read out is lost.
- (3) When the digit count is 12 (S3C1X11), S3GSAF produces word-counter step signal S3C2C1 at t1357. The word count is therefore increased by 1 and the alternate odd-even count signal (S3D or S3V) allows the next sequence of digit counter outputs to read out any residual digits from the other buffer register. These digits are also lost.

Since signals S3GSAF (low) and  $\overline{S3GSAF}$  (high) are present for 36  $\mu$ sec, the synchronizer has more than enough time to perform its 24- $\mu$ sec buffer-clear cycle and start on another.

#### 6-8. NONWRITING SECTOR

As explained under heading 6-1, every sector between synchronizer connection and the start of a write operation is a nonwriting sector during which word and digit counting occur but no information is written.

A nonwriting sector starts whenever the sector-band address register is filled with a sector address and band number (as indicated by S3SAF low,  $\overline{S3SAF}$  high), but the start-or-continue FF is reset ( $\overline{S3SFD}$  high). Under these conditions the sequence of operations is as follows.

- (1)  $\overline{S3SAF}$  does the following:
  - (a) Clears the word counter to 0;
  - (b) Clears the digit counter to 1 (S3C1X0); and S3SAF triggers the 54- $\mu$ sec starting-sequence RDF.
- (2) The output pulse from RDF (S3WSSRU (low))
  - (a) Sets the word counter to 1;
  - (b) Sets FF-A (figure 6-1).
- (3) The output of FF-A sets FF-B at t0. The output of FF-B is timed to t2 to become signals S3WSSR (low),  $\overline{S3WSSR}$  (high).
- (4)  $\overline{S3WSSR}$  does the following:
  - (a) Resets FF-A (FF-B is reset by timing signal t6);
  - (b) Sets the counter-step-control FF.
- (5) The output of the counter-step-control FF (S3CSC low) generates the digit-counter step signal S3C1C every 2  $\mu$ sec at t15.
- (6) Every time the digit counter reaches 12 (S3C1X11), step signal S3C1C produces the word-counter step signal S3C2C1 at t37.

- (7) When the word counter reaches 101 (S3C2XH1) and the digit count is 3 (S3C1X2), a reset pulse is applied to the trim-current-control FF.
- (8) At the next digit count (S3C1X3), signals S3WCR (low),  $\overline{\text{S3WCR}}$  (high) are produced at t26.
- (9)  $\overline{\text{S3WCR}}$  resets the counter-step-control FF; S3WCR sets the trim-current-control FF if the following sector is the starting sector, as indicated by the set state of the start-or-continue FF, S3SFD (low).
- (10) The set output of the trim-current-control FF is passed through a low-speed driver to provide trim current signal  $\overline{\text{S3TRIM}}$  (high), which results in the energizing of the trim heads in the drum in order to erase the old information on the margin of each channel. The set state of the flip-flop further provides signal  $\overline{\text{S3TRIML}}$  (high), which extinguishes the TRIM neon on the engineer's console. The TRIM neon is therefore lighted when the trim current is off and not lighted when the trim current is on.

#### 6-9. WRITING SECTOR

A writing sector starts whenever (1) the sector-band address register contains a legitimate sector address and band number and (2) a start or continue instruction was issued during the preceding sector. The writing sector divides into three parts:

- (1) Writing the starting sequence;
- (2) Writing the memory information;
- (3) Ending the sector.

6-10. STARTING SEQUENCE. The order of operations for writing the starting sequence (figure 6-2) follows in list form.

- (1)  $\overline{\text{S3SAF}}$  (high) does the following:
  - (a) Clears the word counter to 0;
  - (b) Sets the digit counter to 1 (S3C1X0);
  - (c) Resets the counter-step-control FF to prevent digit- and word-counter stepping during the starting sequence.

S3SAF (low) does the following:

- (a) Triggers the 54- $\mu$ sec starting-sequence RDF;
- (b) Gates with the set output (S3FSD low) of the start-or-continue FF to generate signal  $\overline{\text{S3WCS}}$  (high).

- (2)  $\overline{S3WCS}$  does the following:
- (a) Sets the write-control FF to produce signals  $S3WC$  (low),  $\overline{S3WC}$  (high). ( $S3WC$  opens the write-waveform generator control gates to allow writing of the starting sequence.)
  - (b) Resets the write-waveform generator flip-flop at  $t_2$  so that the starting sequence begins with a 0-bit;
  - (c) Sets the write-starting-sequence FF to produce signal  $\overline{S3WSS}$  (high). ( $\overline{S3WSS}$  prevents the generation of signal  $S3GBD$  (low), so that the buffer-read-driver gates are blocked during the starting sequence; it also prevents the generation of signal  $\overline{S3WWGR}$  (high), the recurring ( $t_{26}$ ) reset pulse to the write-waveform generator.)
  - (d) Resets the buffer-register-empty FF to generate signal  $S3RF$  (low), which requests the first word transfer for the sector. Since the word counter reads 0, this word will be transferred into the even buffer register;
  - (e) Triggers a 30- $\mu$ sec RDF.
- (3) The output of the 30- $\mu$ sec RDF is single-pulsed to provide signal  $\overline{S3WCSD}$  (high).  $\overline{S3WCSD}$  does the following:
- (a) Generates word-counter step signal  $S3C2C1$  to step the word count to 1.
  - (b) Resets the buffer-register-empty FF to request the second word transfer of the sector. Since the word counter now reads 1, this word will be transferred into the odd buffer register.
- (4) The output of the 54- $\mu$ sec starting sequence RDF ( $S3WSSRU$  low) is passed through two flip-flops (described under heading 6-8) to become signals  $S3WSSR$  (low),  $\overline{S3WSSR}$  (high) at  $t_2$ .  $\overline{S3WSSR}$  does the following:
- (a) Resets the write-starting-sequence FF. Signal  $\overline{S3WSS}$  then goes low to allow generation of  $S3GBD$  (low) at  $t_{0145}$  and  $\overline{S3WWGR}$  (high) at  $t_{26}$  for the rest of the sector;
  - (b) Sets the write-waveform generator so that the starting sequence ends in the sentinel of two consecutive 1-bits;
  - (c) Sets the counter-step-control FF to allow digit- and word-counter stepping for the rest of the sector.

Thus, by the end of the starting sequence the write circuits are prepared to begin writing memory information immediately—that is,

- (1) The write-control FF is set;
- (2) The write-starting-sequence FF is reset;

- (3) The counter-step-control FF is set;
- (4) The trim-current-control FF is set;
- (5) The digit count is 1 (S3C1X0);
- (6) The word count is 1;
- (7) Word 1 of the sector is in the even buffer register;
- (8) Word 2 is in—or on the way to—the odd buffer register.

6-11. INFORMATION WRITING. The information-writing sequence begins 0.5  $\mu$ sec after the write-starting-sequence FF has been reset. The set output of the write-control FF (S3WC low) gates with timing signal t0145 to generate the 1- $\mu$ sec signal S3GBD (low) at regular 1- $\mu$ sec intervals. S3GBD allows and times buffer readout so that information pulses reach the write-waveform generators at 2- $\mu$ sec intervals at t26.

The digit counter steps repetitively from 1 to 12 to read out the digits of the words transferred into the buffer registers. Each time the digit counter reaches 12 (S3C1X11), the word counter is stepped to switch readout from one buffer register to the other, and keeps track of the number of words written. Each time the digit counter reaches 9 or 10, the next word transfer is requested.

Each bit of a digit read out to the write-waveform generators is accompanied by the signal  $\overline{\text{S3WWGR}}$  (high) at t26, so that each write-waveform generator is set or reset as required to write the information bit (heading 6-2).

6-12. END OF SECTOR. A word count of S3C2XH1 indicates that the 100th word has been written and starts the end of sector sequence as follows. S3C2XH1 does the following:

- (1) Gates with digit count 2 signal S3C1X1 to produce signal  $\overline{\text{S3WESS}}$  (high) at t26.  $\overline{\text{S3WESS}}$  causes the end-of-sector sentinel to be written (heading 6-2).
- (2) Gates with digit count 3 signal S3C1X2 to reset the trim-current-control FF.
- (3) Gates with digit count 4 signal S3C1X3 to generate signals S3WCR (low),  $\overline{\text{S3WCR}}$  (high) at t26.
  - (a)  $\overline{\text{S3WCR}}$  (i) resets the write-control FF; (ii) resets the counter-step-control FF.
  - (b) S3WCR sets the trim-current-control FF if the start-or-continue FF has been set (S3FSD low) by a continue instruction during the sector just ended.

### 6-13. SYNCHRONIZER ERROR

When a synchronizer error occurs, error signal  $\overline{S3EH}$  (high) has the following effect on the write circuits. It resets (a) the write-control FF, (b) the counter-step-control FF, (c) the change-priority FF, and (d) the trim-current-control FF, and sets the buffer-register-empty FF.

### 6-14. SYNCHRONIZER CLEAR

The synchronizer-clear signal  $\overline{ES3CL}$  (high) resets (a) the write-control FF, (b) the write-starting-sequence FF, (c) the change-priority FF, and (d) the trim-current-control FF, and sets the buffer-register-empty FF.

The synchronizer-clear signal is also used in conjunction with the error-insert signal  $\overline{ES3ER}$  (high) to test certain of the error-detection circuits in the synchronizer by creating error conditions. If error signals are not generated (and synchronizer CHECK neon is not lighted) by the affected error-detection circuits, the circuits themselves are at fault. The combined effect of the synchronizer-clear and error-insert signals is summarized in Appendix B.

### 6-15. ADDITIONAL LOGIC

As is evident from figure 6-1, most of the logic in the write circuits of drum-write synchronizer 1 is affected by the additional logic provided for the writing of sector-addresses. This logic is described within its proper context in Appendix A.

### 6-16. ERROR DETECTION

Included in the write circuits in figure 6-1 are various error-detecting circuits. These circuits, described under headings 6-17 through 6-24, generate most of the error signals that set the synchronizer error FF and appropriate error diagnostic FFs as listed in table 4-2.

6-17. START-ERROR CHECKER. The start-error checker consists of two gates. One gate generates start-error signal  $\overline{S3SE1}$  (high) at  $t_2$  if a start instruction is issued (function signal 815) and the set output of the write-control FF ( $S3WC$  low) indicates that the synchronizer has already started. The other gate produces start-error signal  $\overline{S3SE2}$  (high) at  $t_2$  if a start instruction (function signal 815) is issued too late to start writing on the sector of which the address was the last transferred to register P1. It is too late

- (1) If the reset state of the counter-step-control FF ( $S3CSC$  high) indicates that the nonwriting sector has been completed—that is, the 101-word count has been reached and signal  $\overline{S3WCR}$  (high) has been generated to reset the counter-step-control FF, or
- (2) If the set state of the sector-address-register-available FF ( $S3ARA$  high) indicates that the next sector address has already been read into the synchronizer.

6-18. CONTINUE-ERROR CHECKER. The continue-error checker is a gate that generates continue-error signal  $\overline{S3CE}$  (high) if a continue instruction is issued (function signal 857) after the write-control FF has been reset ( $\overline{S3WC}$  low) by signal  $\overline{S3WCR}$  (high).

6-19. OVERFLOW CHECKER. The overflow checker consists of an overflow-detection FF, which is set every time the synchronizer makes a word-transfer request and reset by signal  $\overline{S3BA}$  (high) from the dispatcher when the word is transferred. The flip-flop is set for (1) the first word-transfer request of a sector by signal  $\overline{S3WCS}$  (high), (2) the second word-transfer request by signal  $\overline{S3WCSD}$  (high), and (3) succeeding requests by the transfer-request signal  $\overline{S3RF}$  (low) at t26 and a digit count of 12 ( $\overline{S3C1X11}$ ). Overflow error signal  $\overline{S3FLE}$  (high) is generated under this condition: the flip-flop is not reset by  $\overline{S3BA}$  for the completion of the first word transfer by the time signal  $\overline{S3WCSD}$  is produced to set it again for the second word. Similarly,  $\overline{S3FLE}$  is generated at t26 if the flip-flop is not reset for the completion of each succeeding word transfer by the time ( $\overline{S3C1X11}$ ) the next transfer request is made.

6-20. INITIAL WORD-COUNT CHECKER. During the starting sequence the word-counter is stepped from 0 to 1 by signal  $\overline{S3WCSD}$ . If at the end of the starting sequence indicated by  $\overline{S3WSSR}$  (low) the word count is other than 1, error signal  $\overline{S3C2E1}$  (high) is generated.

6-21. WORD-COUNT PARITY CHECKER. The word-count parity checker is a set of gates that decodes the outputs of the eight word-counter flip-flops to determine whether they represent an odd or even total of 1-bits. The contents of the flip-flops are detected in three groups: FF1, FF2, FF3; FF4, FF5, FF6; and FF7, FF8; as shown in table 6-3. The signals resulting from this detection are then gated to provide error signal  $\overline{S3C2E2}$  (high) at the next word-counter step signal  $\overline{S3C2C1}$  if the word-count contains an even total of 1-bits (table 6-4).

6-22. TRIM-CURRENT ERROR CHECKER. The trim-current error checker consists of two gates which detect either of the following conditions to generate trim-current error signal  $\overline{S3TRIME}$  (high):

- (1) The trim-current-control FF is set ( $\overline{S3TRIM}$  high) while the synchronizer is set to available ( $\overline{S3AV}$  low).
- (2) The trim-current-control FF is still reset ( $\overline{S3TRIM}$  low), even though a starting sequence is ended ( $\overline{S3WSS}$  low), and writing is in progress ( $\overline{S3WC}$  low).

6-23. INFORMATION PARITY CHECKER. Each output information digit is checked for parity as it is transferred from the drum-write amplifiers to the drum. The five output bits for channels A through E are tapped off from the five drum-write amplifiers as signals  $\overline{S3W(A-E)K}$ ,  $\overline{S3W(A-E)K}$  and transferred to the information parity checker. The checker is a set of gates which decodes the digit for an even total of 1-bits and produces error signal  $\overline{S3PE}$  (high) as long as the checker-control signal  $\overline{S3PT}$  (low) is present to indicate that the parity check is relevant.

Signal  $\overline{S3PT}$  (low) is produced as follows: when the writing of the starting sequence ends, signal  $\overline{S3WSSR}$  (high) sets an alert FF at t2. At

Table 6-3. Word-Count Parity Decoding

Word-Counter FFs	Number of 1-Bits	Signals Produced
1, 2, 3	Odd	$\overline{S3C20M} - \overline{S3C20Q}$ (all low)
	Even	S3C20R (low)
4, 5, 6	Odd	$\overline{S3C23M} - \overline{S3C23Q}$ (all low)
	Even	S3C23R (low)
7, 8	Odd	$\overline{S3C26M}, \overline{S3C26N}$ (both low)
	Even	S3C26R (low)

Table 6-4. Conditions Producing Error-Signal  $\overline{S3C2E2}$  (High)

Word-Counter FFs	Totals of 1-Bits			
	a.	b.	c.	d.
1, 2, 3	Even	Odd	Even	Odd
4, 5, 6	Even	Odd	Odd	Even
7, 8	Even	Even	Odd	Odd

the following t7 the set output of the flip-flop is gated with the write-control signal S3WC (low) to set the parity-test FF, and the alert FF is reset.

The set output of the parity-test FF generates checker-control signal S3PT (low) at every t26. At the end of the sector, signal  $\overline{S3WESS}$  (high) resets the flip-flop. Thus S3PT is generated at the appropriate intervals throughout the memory-information writing part of the sector only. The parity-test FF is also reset by synchronizer-error signal  $\overline{S3EH}$  (high) or synchronizer-clear signal  $\overline{ES3CL}$  (high).

6-24. TIMING ERROR CHECKER. This checker is a gate which opens to generate timing-error signal  $\overline{S3TED}$  (high) if a cycling unit timing error occurs (TED low) while a write operation is in progress on the synchronizer (S3WC low).



## SECTION 7

### READ CIRCUITS

#### 7-1. GENERAL

The read circuits of all drum-read synchronizers are basically identical; this section describes and illustrates (figure 7-1) the read circuit of drum-read synchronizer 1 (S1), which differs from the read circuits of the other drum-read synchronizers (S2 and S0) only in that it contains extra logic for the sector-address writing facility. This extra logic is described within its proper context in Appendix A.

The principal functions of the read circuits are these:

- (1) To transfer information words, one digit at a time, from the drum to the synchronizer's input buffer registers;
- (2) To correct any misalignment of the bits of each digit read from the drum. Such misalignment is caused by skewing of the head assembly;
- (3) To initiate the transfer to memory of each word read into an input buffer register.

For the purposes of description, the read circuit is broken down into the following functional divisions:

- (1) Input circuits;
- (2) Skew-correction circuit;
- (3) Buffer-control circuit;
- (4) Error-detection circuits.

#### 7-2. INPUT CIRCUITS

The five bits read from the five channels of a band by the head assembly are transferred into the synchronizer read circuits through five drum-read amplifiers. Figure 7-1 shows the drum-read amplifier and input

path for channel x\*; the input signals from the drum are therefore DxR1A, DxR1B.

The input circuits perform these functions:

- (1) Causing each bit read to act as its own sprocket;
- (2) Synchronizing each bit and its sprocket signal to the internal timing of the processor; and
- (3) Realigning the bits of each digit before the digit is transferred to an input buffer register.

### 7-3. SELF-SPROCKETING

The output from the drum-read amplifier is a sinewave of which the zero crossings correspond to peak voltages picked up from the drum. The + and - outputs are 180 degrees out of phase. A positive-going zero crossing from the + side indicates a 1-bit and triggers the Schmitt-trigger A-type circuit (designated STA-1 on figure 7-1) to produce a negative 0.2- $\mu$ sec signal at the input to gate A. Similarly, a positive-going zero crossing from the - side of the amplifier indicates a 0-bit and triggers STA-2 to generate a negative 0.2- $\mu$ sec pulse at the input to gate B.

The operation of gates A and B is controlled by a long-delay element and FF-A, which together ensure that the gates open only for STA outputs produced by significant zero crossings. At synchronizer connection, signal  $\overline{SICPD}$  (high) resets FF-A. The reset condition of the flip-flop allows gates A and B to generate the 0.2- $\mu$ sec signals  $\overline{SIXIS}$  (high) for 1-bits and  $\overline{SIXOS}$  (high) for 0-bits, respectively.  $\overline{SIXIS}$  and  $\overline{SIXOS}$  are applied to the long-delay element; if either of them is high—that is, if either a 1 or a 0 is read in—the long-delay element generates a high signal at point C after 0.33  $\mu$ sec to set FF-A. After 1.35  $\mu$ sec a high signal is produced at point D to reset FF-A again. During the time FF-A is set, both gates A and B are inhibited. The timing of the inhibit signal is such that it covers the possible times of any nonsignificant zero crossings—that is, zero crossings that result from the recording of two or more consecutive like bits.

### 7-4. SYNCHRONIZATION

The outputs of the self-sprocketing circuit ( $\overline{SIXIS}$  (high) and  $\overline{SIXOS}$  (high)) are synchronized to the internal timing of the processor through FF-B, FF-C, and their associated single-pulsers. The 0.2- $\mu$ sec signal  $\overline{SIXIS}$  sets asynchronous FF-B. The set output of FF-B is single-pulsed through a double-pulseformer arrangement (as shown in figure 7-1) to produce the synchronized 0.5- $\mu$ sec 1-bit signals  $SIXISS$  (low),  $\overline{SIXISS}$  (high). The output of the single pulser resets FF-B.

Similarly, the 0.2- $\mu$ sec signal  $\overline{SIXOS}$  sets asynchronous FF-C. The set output of FF-C is single-pulsed to generate the synchronized 0.5- $\mu$ sec 0-bit signal  $\overline{SIXOSS}$  (high), and the output of the single-pulser resets FF-C.

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\* x = A, B, C, D and E.



## 7-5. INPUT CONTROL

When a start or continue instruction is issued during a sector, the set output of the start-or-continue FF generates signal  $\overline{S1RCS}$  (high) as soon as the sector address and band number at the beginning of the next sector fill the sector-band address register (S1SAF low).  $\overline{S1RCS}$  sets the read-control FF to generate read control signals S1RC (low),  $\overline{S1RC}$  (high), and also triggers a 29- $\mu$ sec RDF.

The single-pulsed output of the 29- $\mu$ sec RDF ( $\overline{S1FSS}$  high) sets the gate-information FF to produce the information-gating control signals S1GSL (low), S1RT1 (high), and  $\overline{S1RT1}$  (low).  $\overline{S1RT1}$  alerts the first-sentinel detector to begin the search for the two consecutive 1-bits recorded at the end of the starting sequence in each channel. The 29- $\mu$ sec delay before alerting the detector ensures that the search for the sentinel does not begin prior to the reading of the starting sequence of alternate 1's and 0's.

The detector consists of two flip-flops, the first of which, FF-D, is set by an input 1-bit,  $\overline{S1X1SS}$  (high), and reset by an input 0-bit,  $\overline{S1X0SS}$  (high); the second flip-flop, FF-E, is set by an input 1-bit only if FF-D is set—that is, only if two consecutive 1-bits are read. The set output of FF-E, S1XSD (low), therefore indicates that the sentinel has been read and the next information read is to be transferred to an input buffer register. Signal S1XSD allows FF-F to be set by each 1-bit read ( $\overline{S1X1SS}$ ) and allows FF-G to be set by any bit read ( $\overline{S1X1SS}$  or  $\overline{S1X0SS}$ ).

Control signal S1GSL gates the outputs of FF-F and FF-G at t0246 to produce the synchronized information signal S1SN (low for 1, high for 0) and synchronized sprocket signals S1XSL (low),  $\overline{S1XSL}$  (high), respectively. Both FF-F and FF-G are reset by timing signal t1357.

## 7-6. SKEW CORRECTION

If the bits of a digit are misaligned because of skewing of the head assembly during reading or recording, some bits of the digit will be read into the synchronizer before the others. The skew-correction circuit in the synchronizer realigns the bits of each digit, where necessary, before the digit is gated into an input buffer register.

The skew-correction circuit (figure 7-2) is a set of five information-bit shift registers (one for each channel) and five associated sprocket counters. Each bit read from a channel is transferred into the register for the channel under control of the associated sprocket counter. Each time all five registers contain at least one bit, the registers are shifted simultaneously one place, so that a complete and aligned digit is shifted out of the registers for transmission to a buffer register.

The information-bit registers are composed of a number of flip-flops which varies with the channel and is a function of the maximum permissible amount of skew. The registers for channels A and E each have a 5-bit capacity (five flip-flops), those for channels B and D a 4-bit capacity each (four flip-flops), and the register for channel C a 3-bit capacity (three flip-flops). The sprocket counter for each channel is a group of flip-flops of which the outputs are fed back in such a way that the flip-flops act as a

counter each time the synchronized sprocket signal indicates that a bit has been read from the channel. The maximum count produced by each sprocket counter is, again, a function of the maximum permissible skew; the counters for channels A and E (four flip-flops each) count to 6, those for channels B and D (three flip-flops each) count to 5, and the counter for channel C (three flip-flops) counts to 4.

Table 7-1 shows the code on which the sprocket counters operate. Note that the FF4 column is relevant only to the counters for channels A and E.

Table 7-1. Sprocket Counter Code

FF set = 1.  
FF reset = 0.

Count	FF4	FF3	FF2	FF1
1	0	0	0	1
2	0	0	1	0
3	0	0	0	0
4	0	1	1	0
5	0	1	0	0
6	1	1	1	0

The following description of the operation of the skew-correction circuits is made with reference to figures 7-2 and 7-3.

Prior to the beginning of a sector-read operation, signal  $\overline{S1RT1}$  from the input control is high to keep all five sprocket counters set to 1—that is, it sets FF1 in each counter and resets the remaining flip-flops. The set outputs of the FF1s,  $\overline{S1AS1}$ — $\overline{S1ES1}$  (high), inhibit gate A.

A sprocket count of 1 alerts the input gate to FF1 of its corresponding information-bit register so that the first bit to be read from a channel is stored in FF1 of the register for the channel. Simultaneously, the sprocket signal generated by each bit read steps the sprocket counter to 2 so that the input gate to register FF2 is alerted to receive the next bit. As this bit is stored in FF2, the sprocket counter is stepped to 3 to alert the input gate to register FF3, and so on.

Because of the system of self-sprocketing, the storing of each bit read from a channel in the information register of the channel occurs in parallel with—but independently of—the same process in the other four channels. In this way, with maximum permissible skew (figure 7-3) the bits read in simultaneously from the two outside channels can belong to digits as many as four digit positions apart on the sector. However, as soon as the sprocket counter for each channel reads 2 or greater, the five FF1s of the registers are known to contain the five bits of one digit. A reading of 2 or greater in each counter is indicated when FF1 in each counter is reset (table 7-1). The reset outputs of the FF1s of the five sprocket counters,  $\overline{S1AS1}$ — $\overline{S1ES1}$  (all low) open gate A to generate signals  $\overline{S1SR}$  (low),  $\overline{S1SR}$  (high), which shift the contents of each register one place to the right; a realigned digit is shifted out of the registers and pulseformed

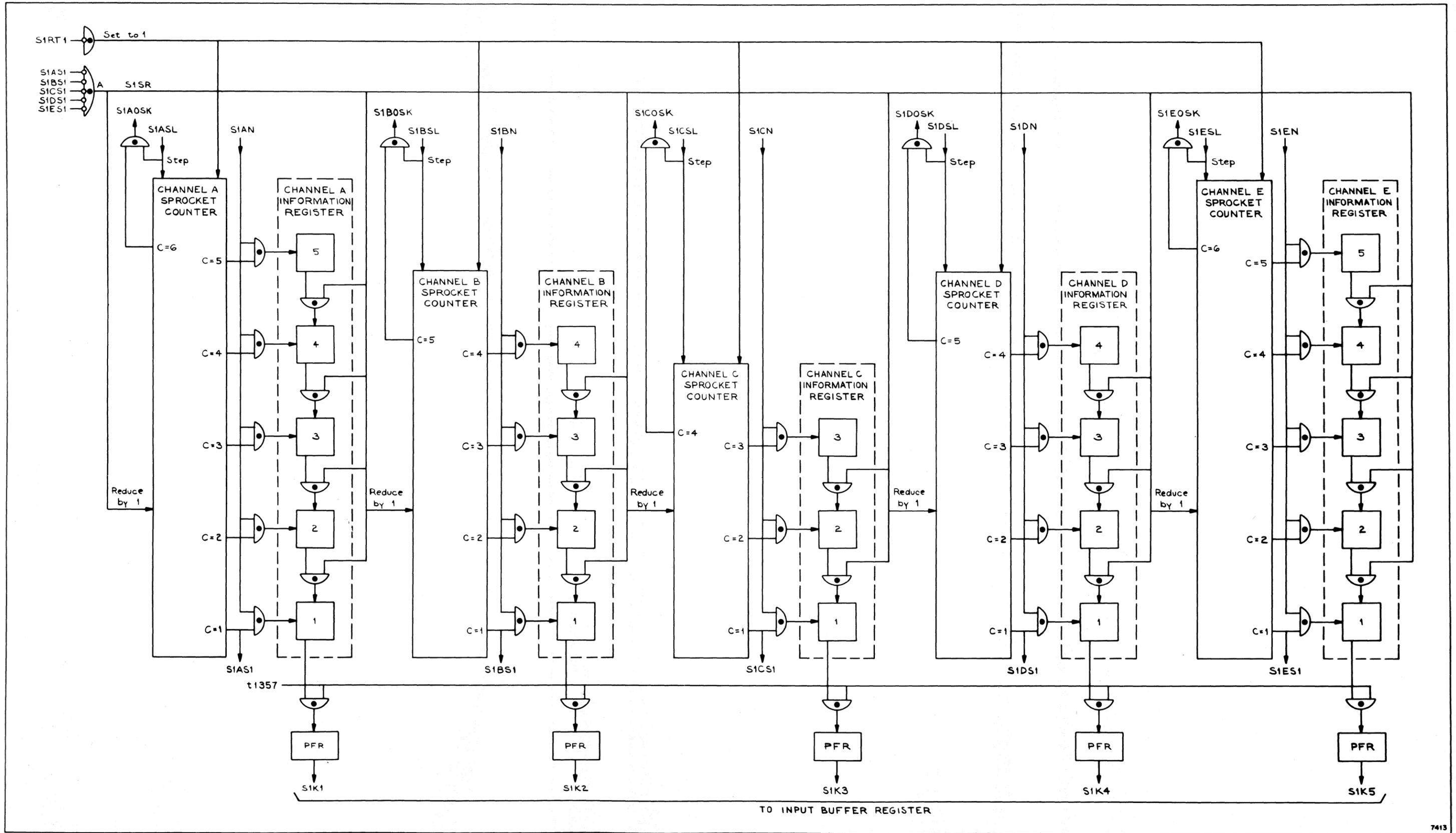


Figure 7-2. Skew Correction Circuits

for transmission to an input buffer register as signals S1K1—S1K5. At the same time, signals S1SR and  $\overline{S1SR}$  reduce each sprocket counter reading by 1 so that at least one counter reverts to 1 and therefore at least one of the signals  $\overline{S1AS1}$ — $\overline{S1ES1}$  goes high to block gate A until the next time the FFs of the five registers contain a digit.

7-7. OVERSKEW. Note from figure 7-3 that, with maximum permissible skew, a realigned digit is shifted by S1SR (low),  $\overline{S1SR}$  (high) to the input buffer register as soon as one of the sprocket counters reaches its highest count. If, however, the amount of skew exceeds the capacity of the information registers, one of the sprocket counters will already have reached its highest count before S1SR,  $\overline{S1SR}$  can be generated to effect the digit transfer. Thus, in each channel an overskew-error signal is generated when a sprocket signal occurs while the sprocket counter is set at its maximum count.

The five overskew-error signals  $\overline{S1AOSK}$ — $\overline{S1EOSK}$  (high) are buffed to set the synchronizer-error FF and error-diagnostic FF 47-8. Each of the overskew-error signals also sets an overskew FF for its appropriate channel. The set output of the overskew FF lights one of the five SKEW MONITOR neons on the engineer's console to indicate the channel in which overskew has been detected.

Various combinations of the five neons also light if malfunctions occur in the input paths from the channels.

7-8. SKEW MONITORING. Patch panels in the output circuits of the sprocket counters for channels A and E allow monitoring of amounts of skew. Connections can be made through the patch panel for channel A, for example, to detect any desired sprocket count. When that count is reached and a sprocket pulse occurs, signal  $\overline{S1AOST}$  (high) is generated to set the overskew in channel 1 FF, thereby lighting SKEW MONITOR neon 1. Signal  $\overline{S1EOST}$  (high) is similarly derived for channel E and sets the overskew-in-channel-5 FF to light SKEW MONITOR neon 5. Since  $\overline{S1AOST}$  and  $\overline{S1EOST}$  do not necessarily indicate an error, they do not set the synchronizer error FF or error-diagnostic FF 47-8.

#### 7-9. SECTOR END

The same conditions that generate S1SR (low),  $\overline{S1SR}$  (high) also generate signals S1C1C1 (low) and S1C1C2 (low). When S1C1C2 occurs and the FFs of the five information registers contain the end-of-sector sentinel ( $S1EN1 \cdot \overline{S1DN1} \cdot S1CN1 \cdot S1BN1 \cdot S1AN1$ ), the end-sentinel detector gate opens to produce the end-of-sector control signals S1T00 (low),  $\overline{S1T00}$  (high), S1ESS (low), and  $\overline{S1ESS}$  (high) for distribution in the read circuits.

In the input circuits  $\overline{S1ESS}$  (high) resets the gate-information FF to prevent further reading from that sector and to set all sprocket counters back to 1 in preparation for the next sector.

The read-control FF remains set until the end of a complete drum-read operation (sector-band address register full and start-or-continue FF reset). Both the read-control and gate-information FFs are reset by the synchronizer-error signal  $\overline{S1EH}$  (high) and the synchronizer-clear signal  $\overline{ES1CL}$  (high).

Note that the error-insert signal produces end-of-sector control signals  $S1ESS$  (low),  $\overline{S1ESS}$  (high) only.

## 7-10. BUFFER-CONTROL CIRCUIT

The buffer-control circuit is composed of a digit counter, a word counter, four flip-flops, and a set of gates, all of which enable the circuit to perform the following functions:

- (1) Transfer the digits of a word read from the drum into the correct digit positions of the input buffer registers;
- (2) Count the words read from a sector and ensure that they are transferred alternately into the odd and the even input buffer register;
- (3) Request the dispatcher to transfer to memory each word that fills a buffer register;
- (4) Cause the dispatcher to make the necessary modification to the memory-addressing sequence when the synchronizer has read the 24th sector of a band in mode 2.

## 7-11. BUFFER WRITE-DRIVER SELECT GATES

Each aligned input digit shifted out of the skew-correction circuit for transmission to a buffer register is accompanied by a write-driver select signal that causes the digit to be written into the correct digit position of the correct buffer register.\* The select signals are derived through a set of 24 buffer write-driver select gates, 12 of which generate the odd buffer register write-driver select signals  $S1DW1$ — $S1DW12$ , and 12 the even buffer register write-driver select signals  $S1WV1$ — $S1WV12$ .

Throughout a sector-read operation all 24 gates are alerted by signal  $S1GBD$  (low), the set output of the gate-buffer-driver FF. This flip-flop is set at the beginning of a sector by signal  $\overline{S1FSS}$  (high) as the search for the first sentinel is about to start, and reset at the end of the sector when signals  $S1C2Z99$  and  $S1C2C$  indicate that the 100th word has been transferred into a buffer register.

During the sector-read operation, signals  $S1D$  and  $S1V$  from the word counter alternately alert the even buffer register write-driver select gates and the odd buffer register write-driver select gates, respectively, so that the 12 sequential digit-counter outputs for each word,  $S1C1X0$ — $S1C1X11$ , can alternately generate select signals  $S1WV1$ — $S1WV12$  and  $S1WD1$ — $S1WD12$  respectively.

The gate-buffer-driver FF is also reset by synchronizer-error signal  $S1EH$  (high), synchronizer-clear signal  $ES1CL$  (high), and error-insert signal  $ES1ER$  (high).

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\* Note that the write-driver select gates may cause the same register digit position to be selected several times while a digit is being aligned in the skew-correction circuit. Thus, in the case of the skew illustrated in figure 7-3, the first bit of information from channel A would be written into the buffer five times before the first bit from channel E was written once.

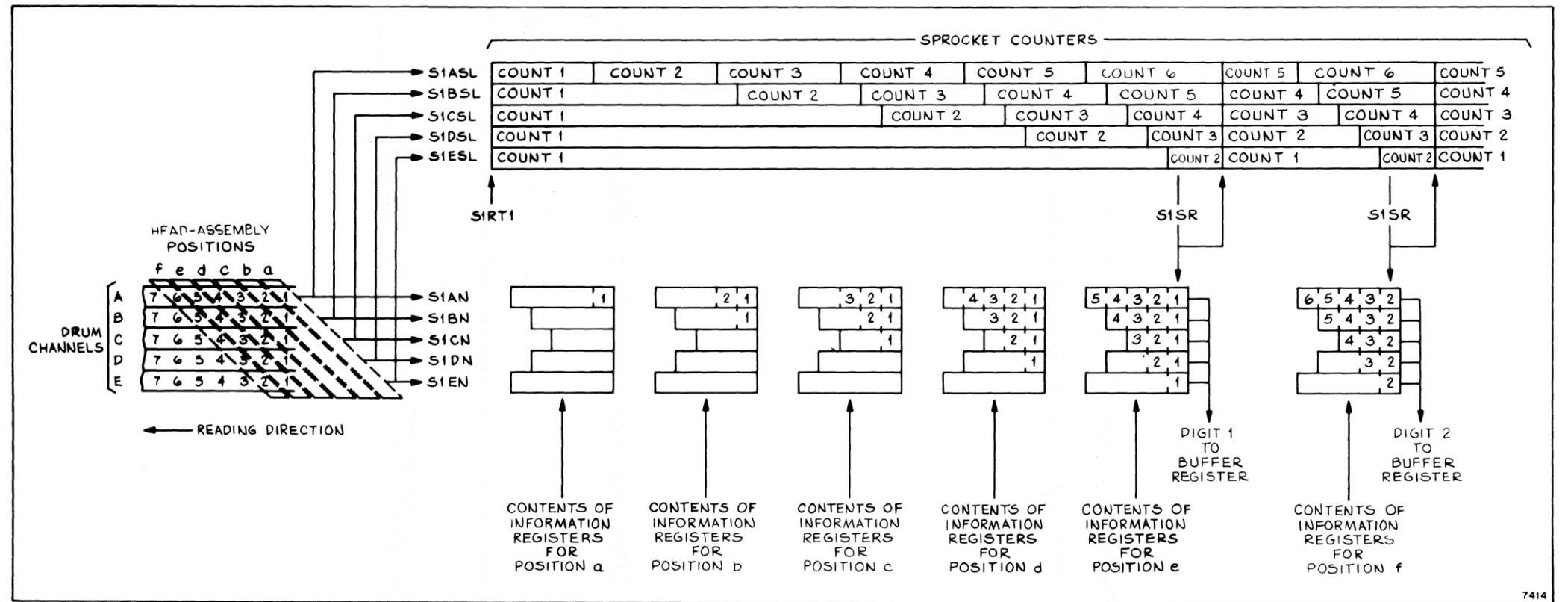


Figure 7-3. Skew Correction

## 7-12. DIGIT COUNTER

The design of the digit counter in the read circuit is identical to that of the digit counter in the write circuit (heading 6-3).

At the beginning of a sector, sector-band address-register-full signal  $\overline{S1SAF}$  (high) clears the digit counter to 1 ( $S1C1X0$ ) in preparation for the first digit read. Each time an aligned digit is shifted out of the skew-correction circuit, signals  $S1SR$  (low) and  $S1C1C2$  (low) step the counter up by one count. When the maximum count of 12 is reached, the next step signal sets the counter back to 1. In this way the counter steps repetitively from 1 through 12 as the digits of successive words are read, and generates the sequential output signals  $S1C1X0$ — $S1C1X11$  that operate the buffer write-driver select gates.

## 7-13. WORD COUNTER

The word counter is a seven-stage binary counter similar in configuration to that described for the write circuit (heading 6-4), except that it has no eighth (check-bit) flip-flop. The counter operates in straight binary code, counting up to decimal 100 in order to keep account of the number of words read from each sector.

At the beginning of a sector, signal  $\overline{S1SAF}$  (high) clears the counter to 0. Thereafter the counter is stepped up by one count by signal  $S1C2C$  (low) each time the digit counter is stepped from 12 ( $S1C1X11$ ) to 1 ( $S1C1X0$ )—that is, each time a complete word has been read and transferred into a buffer register.

The lowest-order flip-flop of the counter is alternately set and reset with each count; its output signals ( $S1V$  (low) for odd counts and  $S1D$  (low) for even counts) therefore provide a means of switching buffer write-in between the odd and the even buffer registers as described under heading 7-11. Signals  $S1V$  and  $S1D$  are also sent to the address- and buffer-register controls in the dispatcher as an indication of whether the next word must be transferred to memory from the even buffer register or the odd buffer register, respectively.

A counter reading of 99, denoting that the 99th word has been read, produces output signals  $S1C2X99$  and  $S1C2Y99$  to alert the subtract-2499 FFs. Signal  $S1C2X99$  also is pulseformed to become signal  $S1C2Z99$ . When the 100th word has been read and signal  $S1C2C$  is generated to step the counter to 100,  $S1C2Z99$  resets the gate-buffer-drivers FF. With a counter reading of 100, denoting that a complete sector has been read, counter output signal  $S1C2XH$  is generated to alert the sector-length error checker.

## 7-14. MEMORY ACCESS

Each time only one digit of a word remains to be written into a buffer register, digit-count signal  $S1C1X11$  resets the buffer-register-full FF to generate signal  $S1RF$  (low).  $S1RF$  is sent to the priority circuits in the dispatcher to request the transfer of the word from the buffer register to the memory. When memory access is gained for the transfer, the dispatcher returns signal  $\overline{S1RFR}$  (high) to set the buffer-register-full FF and cancel

the request. The flip-flop is also set by the synchronizer-error signal  $\overline{S1EH}$  (high) and synchronizer-clear signal  $\overline{ES1CL}$  (high).

In both modes of synchronizer operation, word transfers are made to sequential memory locations. Thus, mode-control signals  $S1M1$  and  $S1M2$  from the program and status controls (figure 4-1) cause the synchronizer address modifier in the dispatcher to add 1 to each memory address to which a word is transferred.

For mode 2 operation, however, the synchronizer must also cause the address modifier to subtract 2499 from the address of the last word of sector 24. For this purpose the read circuit includes a sector-00 FF and a subtract-2499 FF. Both flip-flops are reset at the beginning of a sector by signal  $\overline{S1ADFS}$  (high). The sector-00 FF remains reset until the sector-band address register contains sector address 00, indicating that sector 24 is currently under the head assembly.

The set output of the sector-00 FF,  $S1S00$  (low), alerts the setting gate to the subtract-2499 FF. When the digit and word counters indicate by signals  $S1C1X11$  and  $S1C2X99$  that the last digit of the 100th word is about to be read into a buffer register, the subtract-2499 FF is set to generate signal  $S1S24$  (low).  $S1S24$  causes the address modifier controls to subtract 2499 from the address to which the 100th word is transferred, so that the first word of sector 00 will be transferred to the first memory location allotted to the band.

The sector-00 and subtract-2499 FFs are duplicated for checking purposes.

## 7-15. ERROR-DETECTION CIRCUITS

Included in the read circuits in figure 7-1 are various error-detecting circuits. These circuits, described under headings 7-16 through 7-21, generate most of the error signals that set the synchronizer-error FF and appropriate error-diagnostic FFs as listed in table 4-3.

### 7-16. START-ERROR CHECKER

The start-error checker is a gate which generates start-error signal  $\overline{S1SE}$  (high) at  $t_3$ , if a start instruction is issued (function signal 815) (1) while the synchronizer is already reading ( $\overline{S1RC}$  high) or (2) too late to begin reading the sector whose address was last read into the sector-band address register. It is too late if the next sector-band address has already been read ( $\overline{S1SAF}$  high) to set the synchronizer-for-set-sector-change FF ( $\overline{S1CHSYN}$  high) and the sector-change FF ( $\overline{S1CHD}$  high).

### 7-17. CONTINUE-ERROR CHECKER

The continue-error checking gate generates continue-error signal  $\overline{S1CE}$  (high) if a continue instruction is issued (function signal 857) and the synchronizer is not already reading ( $\overline{S1RC}$  low).

#### 7-18. INFORMATION-PARITY CHECKER

Each input information digit is checked for parity 0.5 msec before it is transferred to an input buffer register. The outputs of the FFs of the five information registers,  $S1AN1-S1EN1$ ,  $\overline{S1AN1}-\overline{S1EN1}$ , are applied to the information parity checker which is operative when signals  $S1C1C1$  and  $S1C1C2$  are low; they indicate that the five FFs contain an aligned input digit. The checker is a set of gates which decodes the digit for an even total of 1-bits to produce information parity error signal  $\overline{S1PE}$  (high). When the digit checked is the end-of-sector sentinel 10111, signal  $\overline{S1ESS}$  (high) blocks the generation of  $\overline{S1PE}$ .

#### 7-19. INFORMATION-PARITY-CHECKER CHECK

The output of the information parity checker is also gated with end-of-sector signal  $\overline{S1ESS}$  (low) to generate error signal  $\overline{S1PCE}$  (high) if the checker fails to detect an even total of 1-bits in the end-of-sector sentinel.

#### 7-20. SECTOR-LENGTH ERROR CHECKER

The sector-length error checker consists of two gates. One gate opens to generate sector-length error signal  $\overline{S1SLE1}$  (high) if the digit indicated by  $S1C1C2$  to be contained in the FFs of the information registers is the end-of-sector sentinel ( $\overline{S1T100}$  low) and the word counter still has not reached 100 ( $S1C2XHD$  high). The second gate generates sector-length error signal  $\overline{S1SLE2}$  (high) if the digit indicated by  $S1C1C2$  to be contained in the FFs of the information registers is not the end-of-sector sentinel ( $\overline{S1T100}$  low) and the word counter reads 100 ( $S1C2XHD$  low).

Note that this circuit effectively checks the operation of the word counter which, in drum-read synchronizers, undergoes no count-parity check.

#### 7-21. OVERFLOW-ERROR CHECKER

The overflow-detection FF is set when signal  $S1RF$  goes low to request the transfer to memory of the word in one buffer register and the digit counter is set back to 1 ( $S1C1X0$ ) to begin write-in to the other buffer register. It is reset when signal  $\overline{S1BA}$  (high) from the dispatcher indicates that the requested word transfer is complete. If a requested word transfer from one buffer register does not take place by the time the other buffer register is full, word-counter step signal  $\overline{S1C2C}$  (high) gates with the set output of the overflow-detection FF to generate overflow-error signal  $\overline{S1FLE}$  (high).

If the 100th word-transfer request of a sector does not take place before the sector address sentinel of the next sector is detected, the overflow-error signal is produced by gating the set output of the flip-flop with the sentinel-detected signal  $\overline{S1ADFS}$ .

Further resetting signals to the flip-flop are the synchronizer-error signal  $\overline{S1EH}$  (high) and the synchronizer-clear signal  $\overline{S1ICL}$  (high).



## APPENDIX A

### SECTOR-ADDRESS WRITING

#### A-1. GENERAL

The method of organizing information on a drum with each information band accompanied by an associated sector-band address channel has two important advantages:

- (1) The positioning of the individual sectors on a band can be varied in order to relegate any bad-spot areas from the actual recording region to spaces between sectors.
- (2) A bad band can be made identifiable by the omission of address information from its sector-band address channel.

The finding of bad spots and the writing of sector-band addresses are achieved by the special sector-band addressing routine through drum-read synchronizer 1 and drum-write synchronizer 1 when the WRITE SECTOR ADDRESSES pushbutton on the engineer's console is pressed. Prior to the running of the special routine, the selected drum must be manually prepared as described in Section 3 of the Larc Maintenance manual, Analysis and Isolation of Faults.

In order to accommodate the sector-band addressing routine, certain modifications and additions are made to the logic of the two synchronizers, as mentioned throughout this manual and noted on figures 4-1, 5-1, 6-1, and 7-1. Moreover, the significance of certain drum-synchronizer instructions is changed during the routine. (Refer to table A-1.) The rest of this appendix provides (1) a very general description of the sector-band addressing routine as related to its use of the two synchronizers and (2) a detailed description of the synchronizer logic involved.

#### A-2. SECTOR-BAND ADDRESSING ROUTINE

For the purpose of description, the sector-band addressing routine divides into three parts:

- (1) Determining the speed of the drum;
- (2) Finding any bad-spot areas on a band;
- (3) Writing sector-band addresses on the band.

Table A-1. Special Drum Synchronizer Instructions

Instruction	Code	Description	Function Signal
Sector change test	50xxSxxMMMM (S = 1,3)	M → C if synchronizer S has detected a drum pulse.	850
Select undelayed drum pulses	51xx1xxxxxxxx	Set drum-pulse-selection FF to select undelayed drum pulses.	851
Select delayed drum pulses	51xx3xxxxxxxx	Reset drum-pulse-selection FF to select delayed drum pulses.	851
Connect	52xxSDDxxxx (S = 1,3; DD = 01-24)	Connect synchronizer S to drum DD and set synchronizer S to unavailable.	852
Start synchronizer in mode 1	53xxSxxxxxxxx (S = 1,3)	Start synchronizer S and process one band, using starting address rPl. For S = 1, this instruction immediately starts the search for the first sentinel in all information channels. For S=3, the instruction starts a write operation when the first drum pulse occurs. Also for S = 3, the instruction transfers the word whose address is in rPl into an output buffer register.	853
Start timing read	55xx1xxxxxxxx	Using the starting address in rPl, write decimal 4s to the memory, one every 2 μsec, between two consecutive drum pulses.	855
Turn on trim current	51xx2xxxxxxxx	Set trim-current-control FF. Flip-flop resets at first drum pulse that does not start a write operation.	851
Transfer sector-band address	58xx1xxxxxxxx	Transfer sector-band address from sector-band address register to rPl. After transfer, synchronizer starts searching for next sector-band address.	858
Start buffer-clear	51xx5xxxxxxxx	Reset S3 gate-sector-address-full FF to start buffer-clear cycle.	851
Stop buffer-clear	51xx6xxxxxxxx	Set S3 gate-sector-address-full FF to halt buffer-clear cycle.	851

A-3. TIMING DRUM SPEED. A drum produces a drum pulse each time it revolves once. Therefore, by causing the read synchronizer to transfer a digit (decimal 4) every 2 μsec between two consecutive drum pulses, the program can determine the speed of a drum revolution.

A-4. BAD-SPOT DETECTION. When the drum speed is found to fall within a certain range, bad-spot detection proceeds as follows:

- (1) Starting five word positions on a band after the drum pulse, the program uses the write synchronizer to record in the next three

word positions a sequence of alternate 1-bits and 0-bits in each of the five information channels, ending in a sentinel of two consecutive 1-bits. For the remainder of the band—that is, until the next drum pulse occurs—the synchronizer records the test pattern of three 1-bits alternating with three 0-bits in each channel.

- (2) The read synchronizer then is connected to start searching for the sentinel of two consecutive 1-bits in each channel. When the sentinel is detected, the synchronizer transfers the test pattern to the memory for comparison. A bad spot is indicated as soon as the comparison operation discovers a difference between the pattern read back and the one known to have been written. The program considers a bad-spot area to extend from two words before the word in which a discrepancy occurs to four words after it—a total of seven words.
- (3) Starting from the drum pulse, the write synchronizer records the sequence of alternate 1-bits and 0-bits in each channel, terminating the sequence in the 1-1 sentinel at the end of the last detected bad-spot area. For the rest of the band—that is, until the next drum pulse—the synchronizer writes the test pattern in each channel.\*
- (4) After the fourth word of the last detected bad-spot area, the program starts the read synchronizer searching for the 1-1 sentinel. The synchronizer proceeds as in step (2).
- (5) The procedure outlined in steps (3) and (4) is repeated as many times as are necessary to check the whole band.
- (6) In order to check the eight-word area immediately following the drum pulse (step (1)), steps (3) and (4) are repeated with the drum pulse delayed 250  $\mu$ sec.

A-5. WRITING SECTOR-BAND ADDRESSES. When the program has thus determined the locations of any bad spots on a band, and the bad spots are few enough for the band to be considered good, the write synchronizer is connected to write the sector-band addresses in channel 6 so that the bad spots fall between sectors. If the band is considered bad, channel 6 is filled with 1-bits.

A-6. CHECKING SECTOR-BAND ADDRESSES. Since bad-spot detection does not check channel 6, the program uses the read-synchronizer to transfer the sector-band addresses into register P1 of the central processor for comparison with the address information known to have been written.

## A-7. DRUM-READ SYNCHRONIZER 1

The special logic included in drum-read synchronizer 1 is best described in the sequence in which it is used within each of the operations

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\* Note that the previously recorded starting sequence and test pattern are automatically erased five word positions in advance of the head assembly for each new write operation.

required of the synchronizer by the sector-band addressing routine. (Refer to figures 4-1, 5-1, and 7-1.)

Signals  $\overline{ES3WSA}$  (high), S3WSAS (low), derived from the WRITE SECTOR ADDRESSES pushbutton, perform the following control functions for the read synchronizer throughout the routine:

- (1) Block the output of the no-address FF;
- (2) Prevent instruction 55 from setting the start-or-continue FF and the mode 2 FF;
- (3) Prevent instruction 53 from setting the start-or-continue FF and the mode 1 FF;
- (4) Set the mode 1 FF;
- (5) Prevent the reset output of the gate-sector-address-full FF from producing signals S1SAF (low),  $\overline{S1SAF}$  (high);
- (6) Allow the drum pulse to produce S1SAF (low),  $\overline{S1SAF}$  (high);
- (7) Block the end-of-sector sentinel detector;
- (8) Reset word-counter FF2.

The drum pulse, which is required for read synchronizer operation, is derived through a special circuit in drum-write synchronizer 1 (figure 6-1). Received over the drum pulse bus, drum pulse DS3DRP is immediately single-pulsed, if the drum-pulse-selection FF is set (signal S3DRPS low), to provide signals S3DRP (low),  $\overline{S3DRP}$  (high). If the flip-flop is reset (signal S3DRPS low), the drum pulse is delayed 250  $\mu$ sec before being single-pulsed, for reasons explained under heading A-4. The drum-pulse-selection FF is set by instruction 51 with a selector digit of 1, and reset by same instruction with a selector digit of 3.

#### A-8. DRUM TIMING

Synchronizer operation for drum timing is as follows:

- (1) Instruction 55 (function signal 855) with a selector digit of 1 (PS1) sets FF-H (figure 7-1).
- (2) The next drum pulse to occur
  - (a) Produces S1SAF (low),  $\overline{S1SAF}$  (high), which
    - (i) Cause the sector-change FF to be set;
    - (ii) Clear the digit counter to 1;
    - (iii) Clear the word counter to 0.

- (b) Sets the buffer-register-full FF;
  - (c) Resets the gate-information FF;
  - (d) Generates signal  $\overline{S1STIME}$  (high), which
    - (i) Sets the read-fours FF;
    - (ii) Resets FF-H;
    - (iii) Sets the gate-buffer-drivers FF.
- (3) The set output of the read-fours FF,  $S1R4FF$  (low),  $\overline{S1R4FF}$  (high),
- (a) Sets FF1 in the channel C information register to set up memory code decimal 4 (00100) in the FF1s of the information registers.
  - (b) Generates signals  $S1SR$  (low),  $\overline{S1SR}$  (high),  $S1C1C1$  (low), and  $S1C1C2$  (low) every  $t15$ .  $S1SR$  (low) and  $S1C1C2$  step the digit counter as  $S1SR$  (low) and  $\overline{S1SR}$  (high) shift decimal 4 from the information registers to be pulseformed and transmitted to a buffer register; the digit and word counts produce the relevant buffer-write-driver select signals; thus every  $2 \mu\text{sec}$  a decimal 4 is transferred into a buffer register;
  - (c) Trigger a  $20\text{-}\mu\text{sec}$  RDF to generate signal  $\overline{S1C2CS}$  (high), which
    - (i) Resets the buffer-register-full FF to request the transfer to memory of the first word of decimal 4s; for each succeeding word-transfer request, the buffer-register-full FF is reset as the digit count reverts from 12 to 1.
    - (ii) Generates word-counter step signal  $S1C2C$  to step the word count to 1; each succeeding word-counter step is produced as the digit count reverts from 12 to 1, but since signal  $\overline{ES3WSA}$  (high) keeps word-counter FF2 reset, the word count can only alternate between 0 and 1; these counts are sufficient to switch digit write-in and word readout between the two input buffer registers by means of signals  $S1D$  and  $S1V$ , respectively.
- (4) The next drum pulse to occur (that is, after one revolution)
- (a) Resets the read-fours FF;
  - (b) Sets the buffer-register-full FF;
  - (c) Resets the gate-buffer-drivers FF;
  - (d) Generates  $S1SAF$  (low),  $\overline{S1SAF}$  (high), which

- (i) Cause the sector-change FF to be set;
- (ii) Clear the word counter to 0;
- (iii) Clear the digit counter to 1.

#### A-9. READING TEST PATTERN

Synchronizer operation for reading the test pattern is as follows:

- (1) Instruction 53 (function signal 853) with a selector digit of 1 (PS1) generates signal  $\overline{S1FSSX}$  (high), which
  - (a) Sets the gate-buffer-drivers FF;
  - (b) Sets the gate-information FF.
- (2) The synchronizer now operates in the normal manner, searching for the 1-1 sentinel in each channel and then reading the information that follows the sentinel—in this case the test pattern. However, the read-control FF and the start-or-continue FF remain reset throughout the operation, and the word counter simply alternates between counts of 0 and 1 (heading A-8).
- (3) The first drum pulse to occur
  - (a) Resets the gate-information FF;
  - (b) Resets the gate-buffer-drivers FF;
  - (c) Sets the buffer-register-full FF;
  - (d) Clears the word counter to 0;
  - (e) Clears the digit counter to 1;
  - (f) Sets the sector-change FF.

#### A-10. READING SECTOR-BAND ADDRESSES

- (1) Instruction 51 (function signal 851) with a selector digit of 1 (PS1) sets the drum-pulse-selection FF at t1 to detect the undelayed drum pulse.
- (2) Instruction 52 (function signal 852B) with a selector digit of 1 (PS1) connects the synchronizer and generates connection-complete signal  $\overline{S1CPD}$  (high) after 8 msec.  $\overline{S1CPD}$  sets the gate-sector-address FF and the gate-sector-address-full FF. The reading of sector-band addresses into the sector-band address register is performed in the normal manner (headings 5-6 and 5-7).

However, since  $\overline{ES3WSA}$  (high) prevents SIGSAF (low) from producing  $\overline{S1SAF}$  (high) to set the sector-change FF each time the sector-band address register is filled, the synchronizer does not inform the program when each address is read. Instead, starting from a drum pulse, the program determines (from its information on where the addresses were written) the times at which it must issue the 58 instruction in order to transfer each sector band address to register P1.

## A-11. DRUM-WRITE SYNCHRONIZER 1

The special logic in drum-write synchronizer 1 is treated in the same way as that of drum-read synchronizer 1. (Refer to figures 4-1, 5-1, and 6-1.)

Signals  $\overline{ES3WSA}$  (high) and S3WSAS (low) perform the following control functions for the write synchronizer throughout the routine:

- (1) Block the output of the no-address FF;
- (2) Prevent instruction 55 from setting the start-or-continue FF and the mode 2 FF;
- (3) Reset the gate-sector-address FF;
- (4) Prevent the reset output of the gate-sector-address-full FF from producing signals S3SAF (low),  $\overline{S3SAF}$  (high);
- (5) Allow the drum pulse to produce S3SAF (low),  $\overline{S3SAF}$  (high);
- (6) Prevent S3SAF from triggering the 54- $\mu$ sec RDF;
- (7) Block the normal setting gate to the write-control FF;
- (8) Prevent the generation of word-counter step signals S3C2C2 and S3C2C3.

## A-12. WRITING TEST PATTERN

- (1) At the same time that the read synchronizer is being used to time drum speed, the write synchronizer can be connected by instruction 52\* and the trim current can be started by instruction 51 (function signal 851) with a selector digit of 2 (PS2), which sets the trim-current-control FF. The flip-flop is reset as soon as a drum pulse occurs while the start-or-continue FF is reset.
- (2) Prior to the writing of the test pattern, a buffer-clear cycle is performed by instruction 51. Function signal 851 with selector

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\* Note that connecting the write synchronizer automatically breaks the connection between the read synchronizer and the drum, but connection to the drum pulse bus is not affected by these instructions.

digit signal PS5 resets the gate-sector-address-full FF to produce signals S3GSAF (low),  $\overline{\text{S3GSAF}}$  (high), which effect buffer clearing in the normal manner (heading 6-7). After a minimum of 24  $\mu\text{sec}$ —the time required to clear both buffer registers—function signal 851 with selector digit signal PS6 generates signal  $\overline{\text{S3C2R}}$  (high) at t1.  $\overline{\text{S3C2R}}$  sets the gate-sector-address-full FF and clears the word counter back to 0.

- (3) Instruction 53 (function signal 853) with a selector digit of 3 (PS3)
  - (a) Sets the start-or-continue FF;
  - (b) Sets the mode 1 FF;
  - (c) Generates signal  $\overline{\text{S3WSAST}}$  (high), which
    - (i) Steps the word counter to 1;
    - (ii) Resets the buffer-register-empty FF to request the transfer of the first word.
- (4) A second 53 instruction with a selector digit of 3
  - (a) Resets the buffer-register-empty FF again to request the transfer of the second word;
  - (b) Steps the word counter back to 0. Since  $\overline{\text{ES3WSA}}$  (high) prevents the generation of the step signals for word-counter FFs 2 through 7, the word count can only alternate between 0 and 1; these counts are sufficient to switch word write-in and digit readout between the two output buffer registers by means of signals S3V and S3D, respectively.
- (5) The next drum pulse to occur
  - (a) Gates with S3SFD to set the trim-current-control FF;
  - (b) Generates signal S3SAF, which gates with S3SFD to produce  $\overline{\text{S3CSCS}}$  (high), which
    - (i) Sets the write-control FF;
    - (ii) Sets the counter-step-control FF.
- (6) Writing now goes ahead in the normal manner with S3GBD (low) produced at every t0145,  $\overline{\text{S3WWGR}}$  (high) at every t26, digit-counter step signal S3C1C at every t15, and word-counter step signal S3C2C1 each time the digit count reverts from 12 to 1; each digit-10 or digit-11 count resets the buffer-register-empty FF to request the next word transfer.
- (7) The next drum pulse to occur indicates that a complete band has been written and
  - (a) Resets the trim-current-control FF;

- (b) Generates S3SAF (low),  $\overline{\text{S3SAF}}$  (high), which
- (i) Cause the sector-change FF to be set;
  - (ii) Reset the write-control FF;
  - (iii) Reset the counter-step-control FF;
  - (iv) Clear the word counter to 0;
  - (v) Clear the digit counter to 1.

The sequence of alternate 1-bits and 0-bits and the 1-1 sentinel that precedes the test pattern is written by transferring words containing digits of 00000 and 01110 (i) in alternate positions, with the last such word ending in two consecutive digits of 01110. The digit 00000 causes the write waveform generators to record a 0-bit in each channel; the digit 01110 is decoded to produce signal  $\overline{\text{S3J1}}$  (high), which sets the write waveform generators for channels A and E so that a 1-bit is recorded in each channel.

For the test pattern, the sequence of three 1-bits alternating with three 0-bits is written in channels 2, 3, and 4 by words of 333555444666 and in channels 1, 4, and 5 by words of 999222555+++.

#### A-13. SECTOR-BAND ADDRESS WRITING

For the writing of sector-band addresses, synchronizer operations are as described under heading A-12. The writing of the serial bits of the starting sequence, sentinel, sector address, and band number is accomplished by applying the fifth bit of each digit to the write waveform generator for channel 6. The words transferred are composed of (1) digits of decimal 0 (00010 in memory code), which therefore write 0-bits in channel 6, and (2) digits of decimal 1 (10011 in memory code) which therefore record 1-bits in channel 6.

## APPENDIX B

### ERROR-INSERT LOGIC

Pressing of the ERROR INSERT pushbutton for a given synchronizer on the engineer's console generates the error-insert signal that checks the operation of certain of the synchronizer's error-detection circuits.

Prior to the error insertion the synchronizer must be cleared and disconnected from any drum. The error-insert signal then creates error conditions in the synchronizer. If the affected error-detection circuits fail to produce error signals (and therefore the neon indicators are not lighted), the associated error paths to the diagnostic flip-flops are not functioning properly.

Tables B-1 and B-2 show the effect of error-insertion on the error-detection circuits of drum-write synchronizer 1 and drum-read synchronizer 1 respectively.

Table B-1. Drum-Write Synchronizer 1 Error Insert Logic

Error Circuit Checked	Error Conditions Set Up By ES3CL (High) and ES3ER (High)	Error Signal Produced
Trim-current error checker	ES3CL sets the availability FF to available (S3AV low), and ES3ER sets the trim-current-control FF (S3TRIM high)	$\overline{S3TRIME}$
Overflow-error checker	ES3ER produces digit-count signal S3C1X11 and word-transfer request signal S3RF, which set the overflow-detection FF at t26. At the following t26, S3C1X11 gates with the set output of the flip-flop.	$\overline{S3FLE}$
Sector-band address parity checker	ES3ER sets the sector-band address-parity-check FF and produces S3SAF (low) every t2. S3SAF gates with the set output of the flip-flop.	$\overline{S3ADE}$
Information parity checker	ES3ER sets the write-control FF to produce S3WC (low), and triggers the 54- $\mu$ sec RDF to produce S3WSSR (high) at t2. These signals set the information-parity-check FF to produce S3PT (low) at t26. ES3ER also prevents the generation of S3GBD (low) and S3WC produces S3WWGR every t26 so that the output of the write-waveform generators is 00000.	$\overline{S3PE}$

Table B-1. Drum-Write Synchronizer 1 Error-Insert Logic (cont.)

Error Circuit Checked	Error Conditions Set Up By ES3CL (High) and ES3ER (High)	Error Signal Produced
Initial word-count checker	ES3ER prevents word-counter FF2 from setting and generates word-counter step signal S32C1, so that the word counter remains at 0000001 (count 1). ES3ER also triggers the 54- $\mu$ sec RDF to produce S3WSSR.	S3C2E1
Word-counter parity checker	The word count remains set to 1. (Refer to preceding.) S3C2C1 and S3SAF change the state of the word-counter check-bit FF every pulse time to produce a word-count parity error every other pulse time.	S3C2E2

Table B-2. Drum-Read Synchronizer 1 Error-Insert Logic

Error Circuit Checked	Error Conditions Set Up By ES1CL (High) and ES1ER (High)	Error Signal Produced
Sector-band address parity checker	ES1ER sets the sector-band address-parity FF and produces signal S1SAF (low).	S1ADE
Information-parity-checker check	ES1ER produces end-of-sector signal S1ESS (low) and forces the information-parity checker output to indicate an odd total of 1-bits.	S1PCE
Overskew-error checker	ES1ER sets the start-or-continue FF and produces S1SAF (low) so that signal S1RCS (high) is generated to trigger the 29- $\mu$ sec RDF. The output of the RDF (S1FSSX high) sets the gate-information FF to produce signal S1GSL (low). ES1ER sets FF-G to generate the sprocket-counter step signals S1ASL-S1ESL every t0246. Since ES1ER also blocks the generation of shift-right signals S1SR (low), S1SR (high), the sprocket counters for all channels exceed their maximum counts.	S1OSK
Information-parity checker	With the sprocket counters being stepped as described above and with no input information, the information registers are filled with 0-bits, and the digit transferred from the FFs of the registers to the information-parity checker is 00000. As soon as the sprocket counters have been stepped once, signal S1C1C2 is generated to alert the information-parity checker.	S1PE
Sector-length error checker	ES1ER produces word-count 100 signal. S1C2XHD and S1C1C2 are generated as described above. Signal S1T100 remains low.	S1SLE2