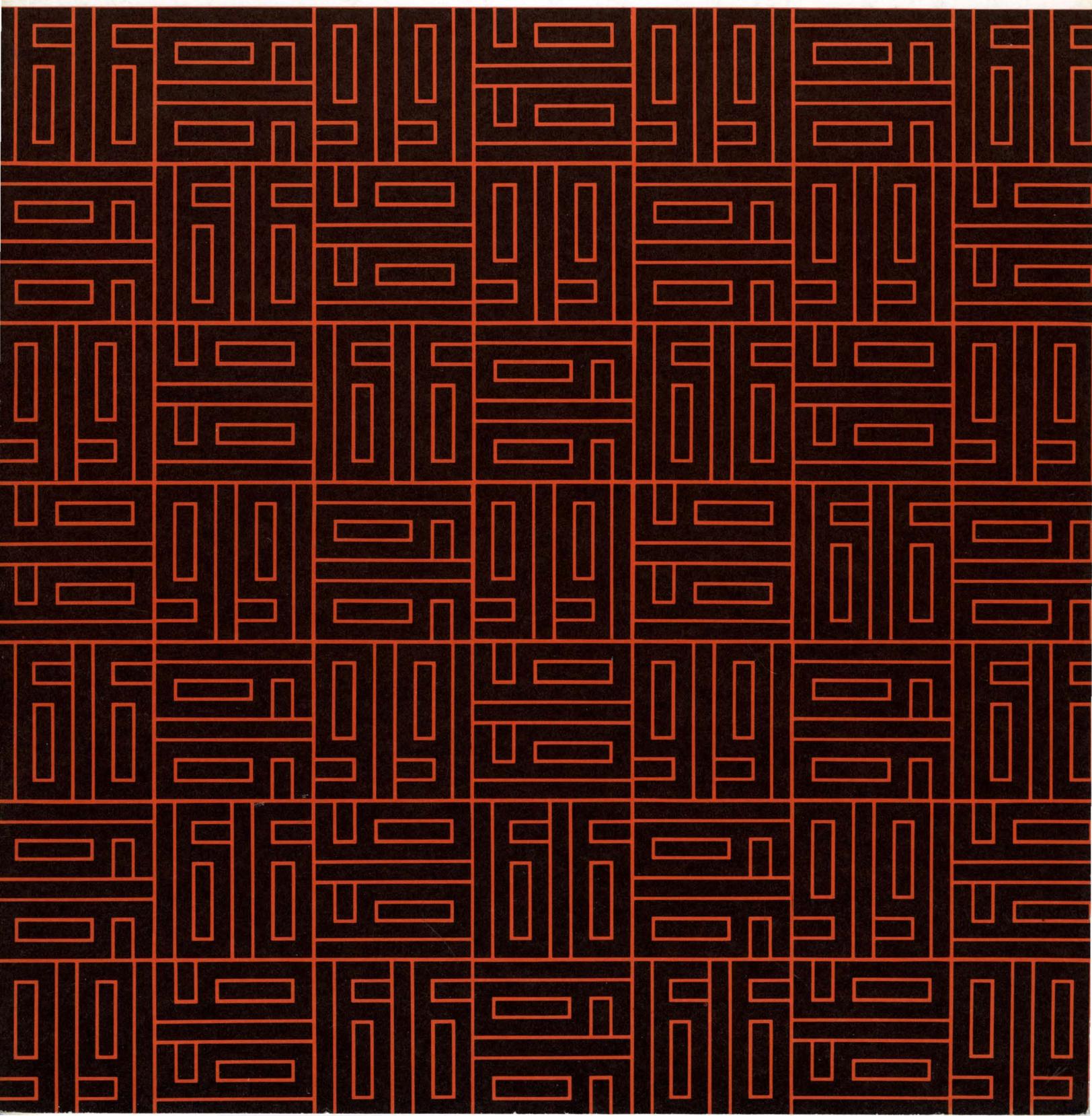


general description UNIVAC 1616



SPECIFICATIONS

SUMMARY

Characteristics

General-purpose, 16-bit digital computer
 Real-time capability
 Physically and functionally modular and expandable
 MSI (medium scale integration) elements
 Integral cooling blowers and power supplies

Environment

Industrial
 Militarized – MIL-E-16400 (Ship-Shore)

CENTRAL PROCESSOR

Standard Features

Two's complement arithmetic
 8-bit byte, 16-bit and 32-bit operands
 16 high-speed general purpose registers
 Program status register
 Single bus functional interface
 Direct addressing capability to 65K words or 131K bytes
 4 Level interrupt processing (hardware serviced)
 16-bit and 32-bit instructions – in any mix
 Basic instructions – 4 formats
 Add 750 nanoseconds
 Multiply 4.15 microseconds
 Divide 4.15 microseconds
 Indexing via general registers
 Load and store multiple registers
 Processor – peripheral channel
 Up to 16 input/output devices (multiplexed)

Optional Features

Up to 4 sets of 16 general registers
 Real-time clock and breakpoint registers (with related instructions)
 Status register No. 2
 Instructions
 Square Root
 Reverse register
 Scale factor shift
 Count ones
 Set, clear and test bit
 Memory protection via lock and key (lockout)
 Processor – memory parity checking
 Memory interface with separate address, read data and write data lines
 NDRO memory (192 words)
 Built in Confidence test and initial load program
 Up to 4 processor-peripheral channels
 Processor-peripheral channel parity checking
 Up to 4 separate input/output controllers (16 channels each)

MAIN STORAGE

Standard Features

Expandable – 4K to 65K words in 4K increments
 16-bit words
 Independently accessible memory banks
 Read/restore cycle time – 750 nanoseconds is optimal
 Asynchronous timing – request and acknowledge signals

Optional Features

Optional memory types – core, plated wire, film, etc.
 Parity
 Priority multiplexer – multi-port option

INPUT-OUTPUT CONTROLLER (1 to 4 OPTIONAL)

Asynchronous operation
 Processor initiated program chain
 10 instructions, format same as for CP
 IC buffer control memory (64 words)
 4 input and output channel groups (1 to 4 groups)
 Parallel 16-bit channel interface
 8 bit byte, 16-bit word or 32-bit dual-channel transfer
 Interface voltage levels - 4 channel groups
 -3.0 volt, 3.5 volt or -15.0 volts
 Power supplied by Central Processor (100 watts maximum)
 Data parity checking – optional

WORD TRANSFER RATES (Thousand words per second)						
INTERFACE & VOLTAGE (TYPE)	Number of Channels					
	1	2-4	5-8	9-12	13-16	
-15V _i (NTDS) IN	41.6	41.6	83.3	124.4	166.6	
OUT	41.6	41.6	83.3	124.4	166.6	
+ 3.5 (A NEW) and - 3.0 (NTDS) IN	190.	250.	500.	750.*	1,000.*	
OUT	190.	250.	500.	750.*	1,000.*	
- 3.0 (1108) IN	667.	1,300.*	70.*	1,300.*	1,300.*	
OUT	667.	1,300.*	700.*	1,300.*	1,300.*	

*Maximum total is 1,300K words per second

I/O Channel operation priority
 First level by channel
 Second level by function

POWER SUPPLY

CP and IOC

115V, 1 phase, 47 Hz to 500 Hz input
 Regulated dc output to CP and IOC

Memory

115V ± 10V, 1 phase, 60 Hz ± 2 Hz input
 Regulated dc outputs to memory

Optional Features

Power loss protection
 Power fault interrupt to CP
 Automatic master clear
 Automatic restart

With all the other small-scale computers on the market today, why should you choose the

UNIVAC® 1616 COMPUTER?

Because of . . .

THE FAMILY APPROACH! Start small! The 1616 gives you just exactly the computing ability you need. Then, the 1616 can grow — up to a good-sized system able to keep up with your needs. It's all there: hardware and software — flexible, modular, ready to grow. Ultimately it can give way to a larger UNIVAC system of the same lean breed.

APPLICATIONS TAILORING! The 1616 is adaptive — you can decide on those special capabilities you need, and have them added to your machine. With its modular design, many special needs can be easily met in the 1616 simply by adding printed-circuit cards and programming routines. Speak up and get the ideal computer for your job! Univac stands ready to help tailor a system for you.

LOWER OWNERSHIP COSTS! Price / performance? Since memory is the key price item in small computers, use the memory most effectively and you get better performance at lower prices. We've compared the 1616 with its five chief competitors. We ran six programs of varying kinds and sizes. The result? The 1616 has the lowest memory utilization and the lowest average execution time!

MODULAR ARCHITECTURE! Not only can you set up a processor for specific operations, but you can build the whole system to suit your needs. If you want floating-point, read-only memories, or other standard packages, plug 'em in. If more memory is needed, add 4096-word increments. If specialized or expanded input/output needs arise, satisfy them by adding I/O control modules and peripheral devices. Finally, if you outgrow one 1616, move another alongside the first — get a multiple system controlled by an executive program. With each jump in hardware growth, there can be a corresponding expansion in software. Each level does its own job competently, and can also absorb the duties of the lesser levels.

CURRENT TECHNOLOGY! Printed-circuit cards use medium-scale integration to combine the flexibility of discrete-component design and the economy, compactness, and reliability of large-scale integration. This reduces cost, physical volume, and power requirements. Some circuit speeds can be doubled!

RELIABILITY REPUTATION! We've learned a lot over the years about what it takes to build reliable computers: high-quality components, the most effective manufacturing techniques, implementing the best design. Your 1616 automatically has all this built-in reliability available at its regular price.

CONSTRUCTION AND MAINTAINABILITY! Easy-build and quick-fix — that's the story of the 1616. All logic circuitry is on plug-in cards for easy insertion and removal; memory modules plug in and out as needed. Modular arrangement, growth changes, and maintenance thus become very simple. Diagnostic programs permit testing without unplugging; test points permit analysis and evaluation.

PROVEN SOFTWARE SUPPORT! We've got it made! Software support that is. No matter what application or configuration, your 1616 can be supplied with software modules to match. Tailored to interact, they're all part of the big picture. No matter how your system grows, the software keeps pace. You can't lose.



Read on for more specific information 

APPLICATIONS

A UNIVAC 1616 Computer can answer the needs of your application. Functionally, the basic computer has the capability to process all problems that are normally assigned to general-purpose computers. However, optional features that enhance the computing speed, input/output, computing capacity, programming convenience or some other requirement of your application may be added in modular form. Your current and near future applications define a starting point – an initial configuration. You can start with a system that is used for remote inquiry and local batch processing, or you can select a system that will handle a combination of data collection and distribution tasks, inquiry or transaction processing, message switching, business and scientific processing.

Sixteen fast, integrated circuit, general-purpose registers that may be used as accumulators, index registers, address registers or temporary operand storage, and an instruction set tailored to their manipulation provide for extremely rapid processing of parameters or data by decreasing the number of required main memory references. The contents of any number of registers can be changed by one simple instruction. This saves program space and 50 percent of the time to execute the load and store process.

Functionally, the 1616 architecture is organized around a common data bus. Transfers and manipulation of data are accomplished through the common bus. The various functional elements accept bit configurations from the bus, interpret or manipulate them, and when appropriate, return bit-configured information to the bus for acceptance by another functional element. This architectural technique allows great flexibility in tailoring a system to meet the requirements of specific applications (see Figure 1).

For **Air Traffic Control**, fast and repetitive calculations must convert radar data and flight facts into visual displays. UNIVAC 1616 Computer programming flexibility, I/O capability, and speed enable it to maintain a dynamic display of air traffic activities within an airport control area.

The UNIVAC Militarized 1616 Computer can effectively reduce **Shipboard Command and Control** system burden by absorbing specific data reduction and related overhead tasks. It reduces large volumes of raw data and arranges them for direct integration into the total system. Direct memory access for I/O transfers permits uninterrupted processing.

The UNIVAC 1616 Computer easily handles **Radar, Sonar and Beacon Signal Processing** tasks with its fast central processor, programmable real-time clock, and high-speed, hardware-initiated interrupt structure. A very fast, programmable input/output section transfers data in real-time.

In shipboard **Control Systems** such as air traffic, radar, ECM and navigation, data are received from many sources. Here again the 1616 excels; data channels can be increased as required. The fast general register set and the associated single and double precision instructions enable fast, complex computation.

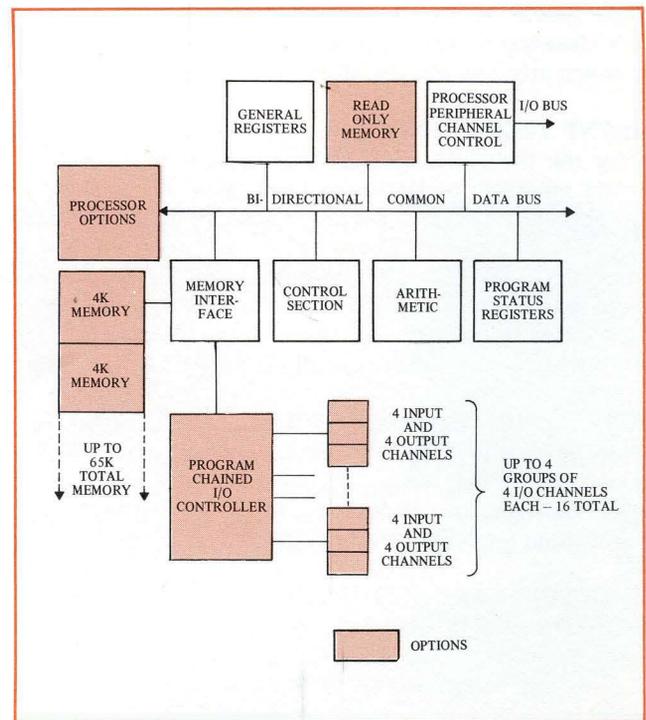


Figure 1. Functional Diagram

SYSTEM CONFIGURATIONS

Basic Configuration

The basic functional computer consists of a central processor, a memory module of at least 4096 words, and one processor/peripheral channel. The memory module can be expanded in 4096-word increments. Each such module operates as an asynchronous functional unit. Memory expansion to 65K words is implemented by adding modular units, all of which are directly addressable by the computer control section. The basic processor/peripheral input/output can be increased to four channels. The optional functional enhancements to the processor can be added as required.

IOC Configuration

Applications that require direct memory access (DMA) for input/output transfers, a large capacity I/O capability, or special purpose channels will include the programmable input/output controller that can accommodate 4, 8, 12, or 16 independent and asynchronous input/output parallel channels. To incorporate this functional module, a shared memory interface is included to allow the IOC to

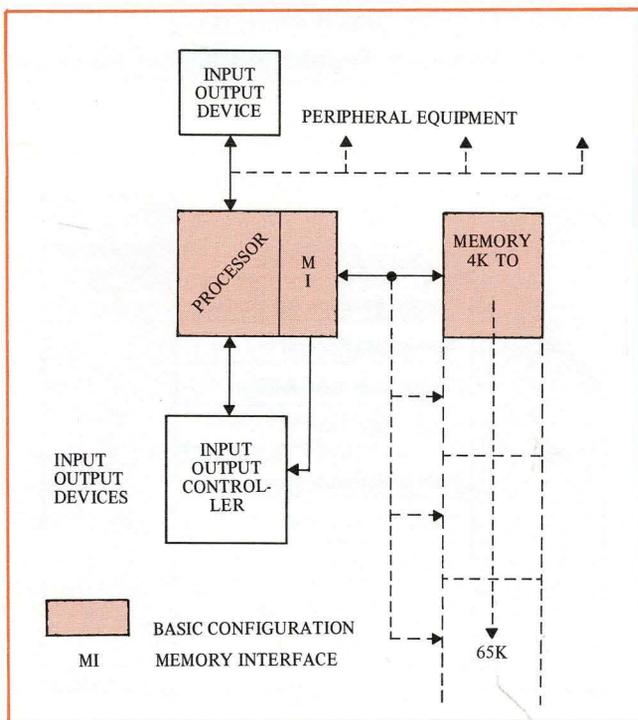


Figure 2. Basic and IOC Configuration

steal memory cycles from the processor. Input/output activity is given priority over the processor in addressing memory.

Multi-Port Memory Access Configuration

A large capacity processing configuration is offered as an initial choice or as a growing step from a basic configuration. This configuration capitalizes on the memory overlap feature. The processor and input/output controllers are independent users of the memory modules. One can work with one or more available memory banks while the other works with a different module. This feature is accomplished by including a priority multiplexer module with each memory bank. Up to 4 input/output controllers may be connected to the processor. In case of simultaneous requests to one memory module, the priority multiplexer honors the user of the higher priority port first. An analysis of this feature shows that there can be as many memory references during one time cycle as there are users (i.e., processors and input/output controllers). Thus, the overall throughput in such a configuration is increased considerably.

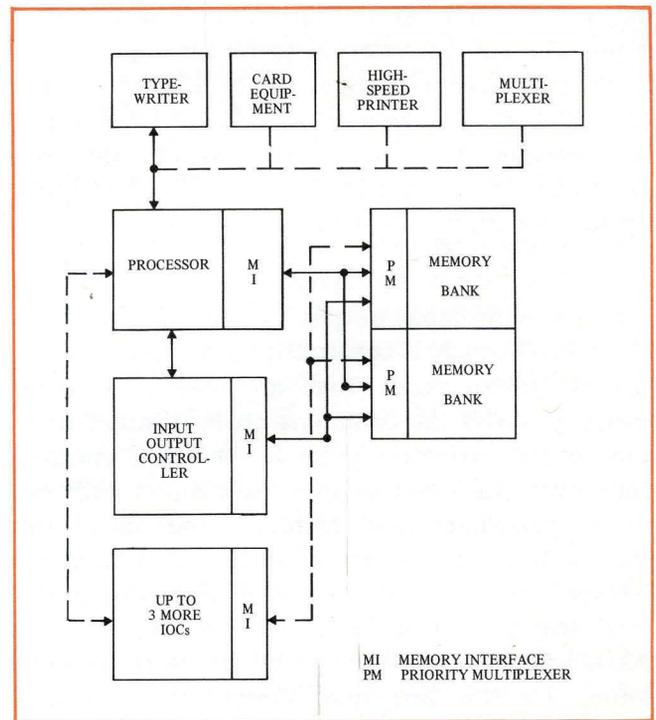


Figure 3. Multi-Port Memory Configuration

INPUT/OUTPUT

Input/output features of the UNIVAC 1616 Computer provide characteristics and interfaces that can be implemented readily for a wide variety of peripheral devices.

Processor Controlled Input/Output

One eight-bit processor controlled input/output channel that operates on a byte-by-byte interrupt basis is provided with the basic 1616 configuration. These channels are compatible with most Univac standard peripheral channels. (See Figure 4 for interface definition.) Up to 16 peripherals can be addressed by the channel. Parity checking and expansion to four processor-controlled channels can be provided as options.

Input/Output Controller (IOC)

A programmable input/output controller can be added to a basic 1616 configuration as an option when the application requires a high input/output transfer capacity, direct memory access or compatibility with UNIVAC militarized peripheral equipment. The IOC provides up to four groups of four input and output channel (4, 8, 12, or 16 I/O channels). Each channel is capable of transferring data, peripheral commands, or interrupt codes over an 8- or 16-bit parallel interface. Dual channel operation permits 32-bit parallel transfers.

Activity with input/output devices connected to the IOC channels is controlled by a chain of commands (instructions) that are stored in main memory. After the command chain is initiated by the central processor program, the IOC controls the peripheral devices, provides a direct path between peripherals and memory, and allows the central processor to continue its other tasks. A 64-word memory of monolithic elements in the IOC stores control words during I/O activity. Asynchronous timing of word transfers is determined by the peripheral device on a request-acknowledge mode of communication. (See Figure 5 for interface definition.)

Termination of active buffers (input/output transfers) may be monitored by the IOC if requested by the command chain. A *monitored buffer termination* interrupts the processor unless that class interrupt is locked out.

Interrupt information transfers from peripheral devices to the central processor are stored at assigned memory locations where they are available to the interrupt processing routine when the IOC interrupts the processor.

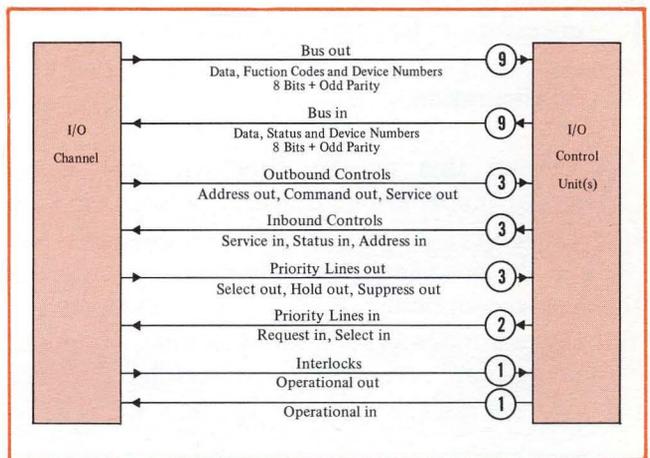


Figure 4. Processor/Peripheral Channel Interface

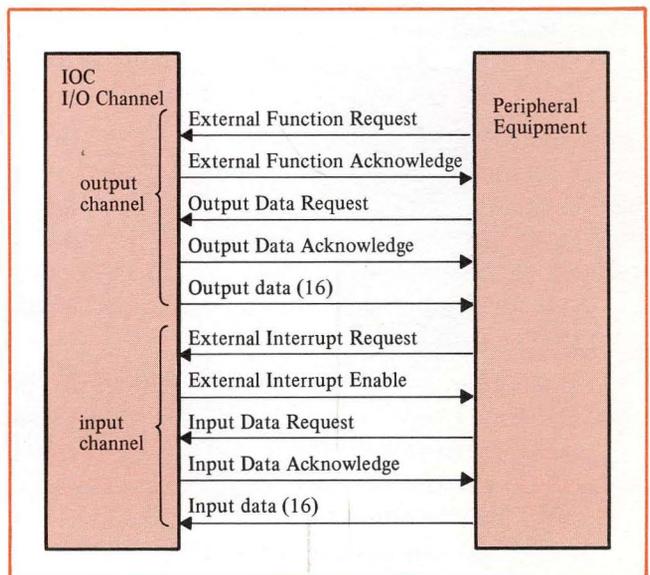


Figure 5. IOC Channel Interface

INTERRUPT PROCESSING

The UNIVAC 1616 furnishes a rapid and efficient method of service and control to interrupt structured operations. All interrupting conditions are arranged in four major priority classes with minor levels of priority within each class as shown in Table 1.

TABLE 1. INTERRUPT PRIORITY

Class	Priority Within Class	Interrupt	Binary Interrupt Code Generated
Class I, Hardware Errors	1	Power Fault	000
	2	CP Memory Resume Error	001
	3	CP Parity Error*	010
Class II, Software Interrupts	1	CP Instruction Fault	000
	2	Privileged Instruction Error	001
	3	Memory Lock and Key Error*	010
	4	RTC Overflow	011
	5	Executive Call	100
Class III, IOC Interrupts	1	External Interrupt	000
	2	Chain 0	001
	3	IOC Hardware Errors*	010
	4	I/O Data Parity Error*	011
Class IV, Proc./Periph. Interrupts	1	Service In Request	001
	2	Status In Request	000

*Optional

Each class has priority of service over any class with a higher number and each interrupt within a class has priority of service over any interrupt in that class with a higher number. When an interrupt is honored, all others are locked out until the active processing status information is stored and new status information for the interrupt processing routine is activated. Lockouts are then set or released as programmed. High priority interrupts can be suspended and nested within lower priority interrupt processing. A low priority interrupt occurring when its class is locked out will be serviced after the lockout is released.

Each interrupt that occurs generates a unique code that is used to modify the address stored in the load program address register location, assigned to

that interrupt class, before being transferred to the program address register. The interrupt processing circuitry is designed to store the computer and program status information in a specific memory location when an interrupt is honored. It immediately resets the program address and status registers with status information required for the service routine associated with the interrupting source and transfers control to that specific routine. Upon completion of the interrupt servicing routine, the process is reversed, and the suspended program continues from the point of interruption.

A Status Register No. 1 keeps a running account of the central processor status as tasks are performed. If this performance is interrupted, the current status is saved until the interrupt routine is completed. At this time, the status information is returned, and the interrupted task is re-entered to continue its job.

Power Protection and Recovery

An optional power transient protect feature provides voltage sensing circuits in the power supply that interrupts the computer when primary power is turned off, or when a severe power transient causes the voltage to fall below a critical level. This Class I, Priority I "Power Fault" interrupt provides an entry to a routine that saves the operating parameters (normally the registers in use) and terminates in a conditional "power-out-of-tolerance" closed loop. If power returns to normal at this point, the loop provides an entry to a parameter restoring routine, and an orderly restart of the interrupted program is begun at the point of interruption. However, if power goes below the operational level, a master-clear signal clears the computer. When power is re-applied and the "Auto Start" is selected, the processor enters an automatic recovery routine which restores the required registers and enters normal operation. This capability provides for sustaining operations under severe power fluctuations and for automatic restart and recovery following power failures.

INSTRUCTIONS

Ultra Efficient Instruction Set

Instructions defining operations for the UNIVAC 1616 computer are designed to maximize circuit effectiveness in performing high-speed computer functions. Its large set of flexible and comprehensive, single and double-word instructions places the 1616 far beyond the mini-computer capability; it is truly a medium-scale processor. Programs constructed with a high ratio of one word instructions to two word instructions *greatly increase* the 1616 *computing speed* and also *occupy less memory space*. Among the instructions in the total repertoire are many that *speed up* the capability of application programs and also provide greater flexibility for programmers.

Figure 6 defines the two 16-bit single word formats and the two 32-bit, two-word formats. Single-word formats can be used when operands are manipulated in high-speed general registers. Double-word formats are used for operations requiring memory references, indexing type operations and those that provide programmers with the convenience of listing constants in-line with instructions.

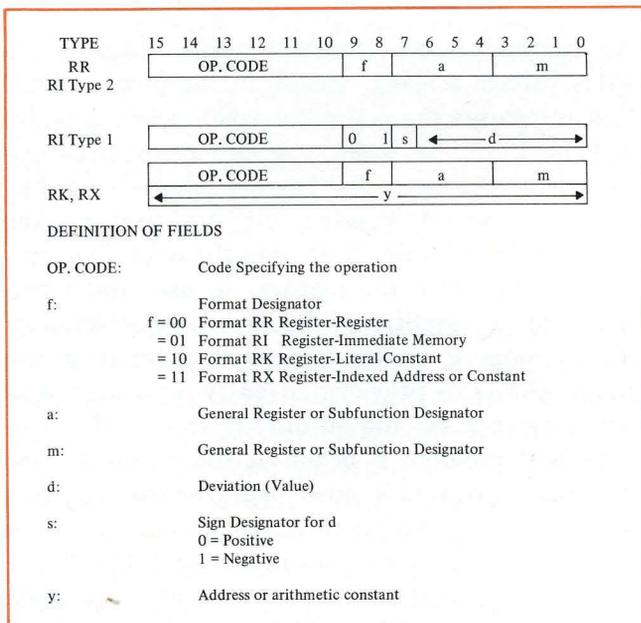


Figure 6. Instruction Word Formats

Table 2 lists the instructions in the 1616 repertoire and the execution time for each instruction.

The **Biased Fetch** instruction allows the central processor to check on the performance of tasks it assigns to an input/output controller.

Local Jump instructions are storage space and time savers in all systems designed around the natural "looping" method of programming. These saving benefits are apparent in both the program generation and job processing phases.

The **Jump and Link** instructions are standard features of the computer and fill the requirement for linking to re-entrant routines. Because these routines cannot be changed internally, linking is done externally, either through general registers or main memory.

An optional **Reverse Register** instruction is useful in reversing a stream of data that is received from a communication system and must be transmitted to another system in reverse order.

The optional **Scale Factor Shift** instruction provides a left shift function which positions the word for greatest significance and counts the number of digit positions shifted. It is used effectively in floating point arithmetic routines that convert fixed point numbers to floating point format.

A **Square Root** instruction is an option that is useful in scientific applications.

Set Bit, Clear Bit and Test Bit are optional instructions that provide a fine grain, computer word examination and change capability that are useful in real-time communications. Interacting tasks that communicate by flags and status words benefit highly from this flexible bit handling feature.

The following **Control Instruction** options are requirements when the Real-Time Clock or the Status Register No. 2 optional features are incorporated in the system.

- Load and Store Status Register No. 2
- Load and Store RTC
- Enable/Disable RTC.

TABLE 2. REPERTOIRE OF INSTRUCTIONS

INSTRUCTION	Execution Time in Memory Cycles				
	FORMAT				FOOTNOTE REFERENCE
	RR	RI	RK	RX	
BL Byte Load	-	-	-	3	
L Load	1	2	2	3	
LD Load Double	-	3	-	4	
LSQR Load Status Word	1	-	-	-	1
LPR Load P-Register	1	-	-	-	
LM Load Multiple	-	-	-	2	2
LP Load Program Status Word	-	3	-	4	
*LCR Load RTC	-	-	-	-	
*LSTR Load Status Register 2	1	-	-	-	
SSQR Store Status Word	1	-	-	-	1
BS Byte Store	-	-	-	3	
S Store	-	2	-	3	
SD Store Double	-	3	-	4	
SM Store Multiple	-	-	-	2	2
SZ Store Zeros	-	2	-	3	
*SCR Store RTC	1	-	-	-	
*SSTR Store Status Register 2	1	-	-	-	
RR Round Register	1	-	-	-	
IR Increase Register	1	-	-	-	
DR Decrease Register	1	-	-	-	
SU Subtract	1	2	2	3	
A Add	1	2	2	3	
P Make Positive	1	-	-	-	
N Make Negative	1	-	-	-	
TC Two's Complement	1	-	-	-	
TCD Two's Complement Double	1	-	-	-	
OC One's Complement	1	-	-	-	
C Compare	1	2	2	3	
AD Add Double	1	3	-	4	
SUD Subtract Double	1	3	-	4	1
CD Compare Double	1	3	-	4	
M Multiply	1	2	2	3	3
D Divide	1	2	2	3	
*SQR Square Root	1	-	-	-	4
*RVR Reverse Register	1	-	-	-	
*CNT Count Ones	1	-	-	-	
*SFR Scale Factor Shift	1	-	-	-	
XOR Exclusive OR	1	2	2	3	
MS Masked Substitute	1	2	2	3	
CM Masked Compare	1	2	2	3	
AND AND	1	2	2	3	
OR Inclusive OR	1	2	2	3	
LRS Logical Right Shift	1	-	2	-	4
ARS Algebraic Right Shift	1	-	2	-	
LRD Logical Right Double Shift	1	-	2	-	
ARD Algebraic Right Double Shift	1	-	2	-	
ALS Algebraic Left Shift	1	-	2	-	
ALD Algebraic Left Double Shift	1	-	2	-	
CLS Circular Left Shift	1	-	2	-	

INSTRUCTION	Execution Time in Memory Cycles					
	FORMAT				FOOTNOTE REFERENCE	
	RR	RI	RK	RX		
J Jump	1	-	2	3	5	
JS Jump and Stop	1	-	2	3		
JLR Jump, Link Register	1	-	2	3		
JE Jump Equal	1	-	2	3		
JNE Jump Not Equal	1	-	2	3		
JLS Jump Less	1	-	2	3		
JGE Jump Greater or Equal	1	-	2	3		
JO Jump Overflow	1	-	2	3		
JC Jump Carry	1	-	2	3		
JPT Jump Power out of Tolerance	1	-	2	3		
JKS Jump key set and Stop	1	-	2	3		
JB Jump Bootstrap	1	-	2	3		
XJ Index Jump	1	-	2	3		
JZ Jump Zero	1	-	2	3		
JNZ Jump Not Zero	1	-	2	3		
JP Jump Positive	1	-	2	3		
JN Jump Negative	1	-	2	3		
LJE Local Jump Equal	-	1	-	-	6	
LJNE Local Jump Not Equal	-	1	-	-		
LJLS Local Jump Less	-	1	-	-		
LJGE Local Jump Greater or Equal	-	1	-	-		
LJ Local Jump	-	1	-	-		
JLM Jump, Link Memory	-	-	2	3		
LJLM Local Jump Link Memory	-	2	-	-		
ER Executive Return	1	-	-	-		1
IOC Input/Output Command	1	-	-	-		7
BF Biased Fetch	-	2	-	3		
REX Execute Remote	-	-	2	-		
PCK Processor Command Out	-	-	2	3		
PTK Processor Transfer	-	-	2	3		
PTC Processor Transfer or Command	-	-	2	3		
SB Set Bit	1	-	-	-		
CB Clear Bit	1	-	-	-		
TB Test Bit	1	-	-	-		
*ECR Enable RTC	1	-	-	-		
*DCR Disable RTC	1	-	-	-		
INPUT-OUTPUT CONTROLLER						
AC Activity Control	1	-	-	-		
CC Channel Control	1	-	-	-		
ICK Initiate Chain	-	-	2	-		
RC Read Control Memory	-	-	-	3		
WC Write Control Memory	-	-	-	3		
IO Initiate Input/Output	-	-	-	4		
LCM Load Control Memory	-	-	2	3		
SCM Store Control Memory	-	-	-	3		
HC Halt Chain	1	-	-	-		
IP Interrupt Processor	1	-	-	-		
ZF Zero Flag	-	-	-	3		
SF Set Flag	-	-	-	3		

1 RR Format add 850 nanoseconds
 2 Plus number of registers
 3 RR and RK formats add 3.4 microseconds; RI and RX formats add 2.55 microseconds
 4 Plus 680 nanoseconds and 170 nanoseconds times number of positions shifted
 5 RR format, add 410 nanoseconds; RI, RK and RX formats, add 340 nanoseconds
 6 Plus 170 nanoseconds
 7 Plus execution time of remote instruction
 * Optional Instructions

SUPPORT SOFTWARE

Univac is prepared to support your software requirements no matter what application or 1616 system configuration is defined. Software as well as hardware follows the modular concept in compatibility, capability, and design. Software selection is in accordance with hardware capability and capacity. Three levels of support software are offered to aid programmers in preparing programs for the 1616; they are subsequently discussed. Assembly language syntax is standardized throughout.

The Level 0 support software provides the capability to prepare programs in advance of actual 1616 system delivery. It includes a General Purpose Assembler (GPA) for 1616 program generation and program listings; a 1616 Simulator (SIMPAC 16) that runs on the UNIVAC 1108/1106 Computer complex under EXEC 8 (executive); and a utility package operating directly on the 1616 for loading, executing, and debugging object programs produced by the assembler.

The 1106/1108 GPA and SIMPAC 16 are operable from a remote terminal device. Level 0 enables users to take full advantage of services provided by the EXEC 8 Operating System for economical program generation and initial debugging.

The Level 1 support software package operates directly on the 1616 computer under operator control from an on-line typewriter or other suitable communication device. The package includes:

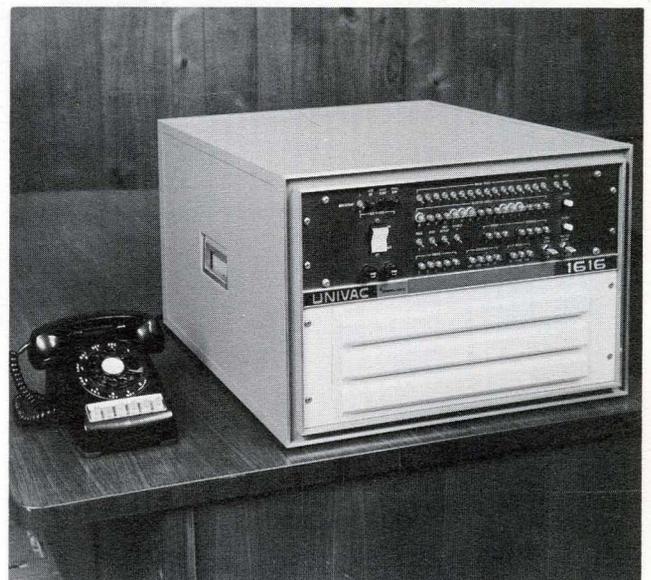
- A basic assembler that accepts the same symbolic language (ULTRA/16-0) as the Level 0 GPA and produces machine code programs and assembled listings.
- A source language text editor for correcting and updating symbolic programs easily.
- An object program loader that loads and links together separately assembled, relocatable outputs produced by the assembler.
- Debugging aids that provide such features as snap dumps, memory inspect and change, memory dumps, absolute code load, etc.
- Input/output handlers for devices used by the support software for user programs.

The Level 2 support software package is a very capable, versatile, and comprehensive collection of programs that run on a 1616 system.

The complete package will include the following modules:

- Compiler
- Macro Assembler
- Text Editor
- Librarian
- Linking Loader
- Debugging Aids
- Equipment Conversion Routines
- System Monitor

The Level 2 support software package operates on a higher level hardware configuration. It is offered on systems that include an 8192-word memory, a typewriter console, perforated paper tape equipment and a bulk storage peripheral device such as a small disk or drum device or two magnetic tape transports. High-speed printers and card equipment used with this minimum system enhance the program generation capability.



OPTIONS

Functional enhancements are available as additions to the basic configuration. Additional arithmetic capability, instructions, input/output and memory interfaces and other expansions may be provided to meet the requirements of your application. Some of the options are merely plugged into existing prewired slots while others are added by selecting a proper interconnecting wiring harness or a proper back panel wiring arrangement.

One set of 16 **General Registers** is a standard feature of the central processor. If, however, an application requires a high rate of task changes (i.e., switching from one program to another), up to three additional sets can be provided as options, thereby allowing certain program sections sole use of a set.

An automatic or semi-automatic **Power Failure Protection** optional feature protects the contents of memory and the internal registers when power to the computer falls below an operable level.

Optional **Memory Interfaces** are available in the computer to match the requirements of an optional memory system (e.g., core, plated wire, modular, future technological advances). Computers that must operate in a military environment can be supplied only by using memory systems that meet military specifications.

A **Multi-Port Memory Interface** permits sharing a memory module (bank) by more than one bus system. Overall processing efficiency and speed can be increased by overlapping operations that involve different memory modules in the system. For example, the IOC can transfer data to one module during the same period that the central processor is processing data in another.

A **Memory Parity** option provides automatic checking of data and instruction transfers to and from memory on an eight-bit byte basis.

An optional **Breakpoint Register** provides a convenient debugging aid. For example, the operator can monitor a specified instruction location or operand location when it is addressed by a running program.

One to four optional **Input/Output Controllers (IOC)** may be attached to a central processor when applications require:

- Large capacity input/output capability (An IOC can transfer data at memory speeds on an 8, 16, or 32-bit interface)
- Direct access to memory for input/output devices
- Independent input/output control
- Different channel interfaces or operating modes.

The IOC option also permits integrating a 1616 computer into a system that has an input/output equipment complex established.

Where applications require a **Direct Memory Access** for external devices, a separate **Priority Multiplexer** section can be supplied as an option. This unit provides multiport, asynchronous access to memory modules. Users (central processor or input/output controllers) are then connected to the memory module on different access ports and communicate with the module in a request-acknowledge mode via the priority circuitry. In case of conflicts the input/output is given priority – thereby maintaining the direct memory access. When the users address different memory modules, both modules operate concurrently. This overlapped operation doubles memory utilization and increases the overall processing capability accordingly.

An optional **Status Register No. 2** provides for capturing additional status information when the system is expanded to include more comprehensive interrupt handling capability and memory lockout protection. Unassigned fields may be used for future functional options.

The **Real-Time Clock** is an optional feature that provides a timing device that may be enabled on time increments suitable for a specific task or disabled as desired. At the expiration of time specified to the enabled clock the program is interrupted and control transfers to another routine.

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