

**USER'S GUIDE  
DIGITAL OUTPUT MODULE  
for use with  
Varian 620 or V73 Series Computers**

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## 1. INTRODUCTION

### 1.1 GENERAL

The Digital Output Module (DOM) and Digital Output Expansion Module (DOME) are hardware options that interface Varian 620 and V73 series computers with external devices which require digital data as their inputs.

A DOM includes four functional features:

- Digital Output Registers, which transfer digital data from the computer to an external device.
- Gated Inputs, which gate digital data from an external device into the computer.
- External Control (EXC) Interface Logic, which allows a computer program to control external devices via logic-signal EXC output lines.
- Sense (SEN) Interface Logic, which allows a computer program to test the status of external devices by sampling logic levels present on Sense input lines.

A DOME, which includes digital output registers and gated inputs, is used to expand the DOM's capability. Up to three DOMEs can be connected to each DOM. As many as 32 DOM and DOME modules can be attached to a single computer to provide the following I/O capability:

64 Digital Output Registers -	Each module (DOM or DOME) contains two 16-bit registers.
32 Gated 16-bit Inputs -	Each module (DOM or DOME) contains 16 gated inputs.

- |                               |  |
|-------------------------------|--|
| 64 External Control Outputs - | Each DOM contains eight External Control output lines. |
| 64 Sense Inputs -             | Each DOM contains eight Sense input lines.             |

Simple installation procedures allow the DOM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DOM for post-installation checkout of its operational status. In addition the module is fully supported by standard Varian software and input/output options.

## 1.2 FUNCTIONAL DESCRIPTION

All elements needed to perform the four basic DOM functions are packaged on a single plug-in printed circuit board. Figure 1-1 illustrates the functional elements included in a DOM module. A DOME contains only those elements shown in the shaded portion of Figure 1-1.

### Device Address

The computer program must select a DOM by its device address before any DOM operation can be performed. There are eight device addresses reserved for DOMs ( $50_8$  to  $57_8$ ). As many as four modules can be located at a single device address; one of the four, known as the master DOM, contains the device address decode logic. The other three are DOMEs which function as slaves to the DOM but provide the same basic capability.

### DOM Select

An individual register or gated input must be selected by the computer program, using an Extended EXC (EXC2) instruction. There are eight select lines located at each device address; each line is enabled by the corresponding EXC2 instruction.

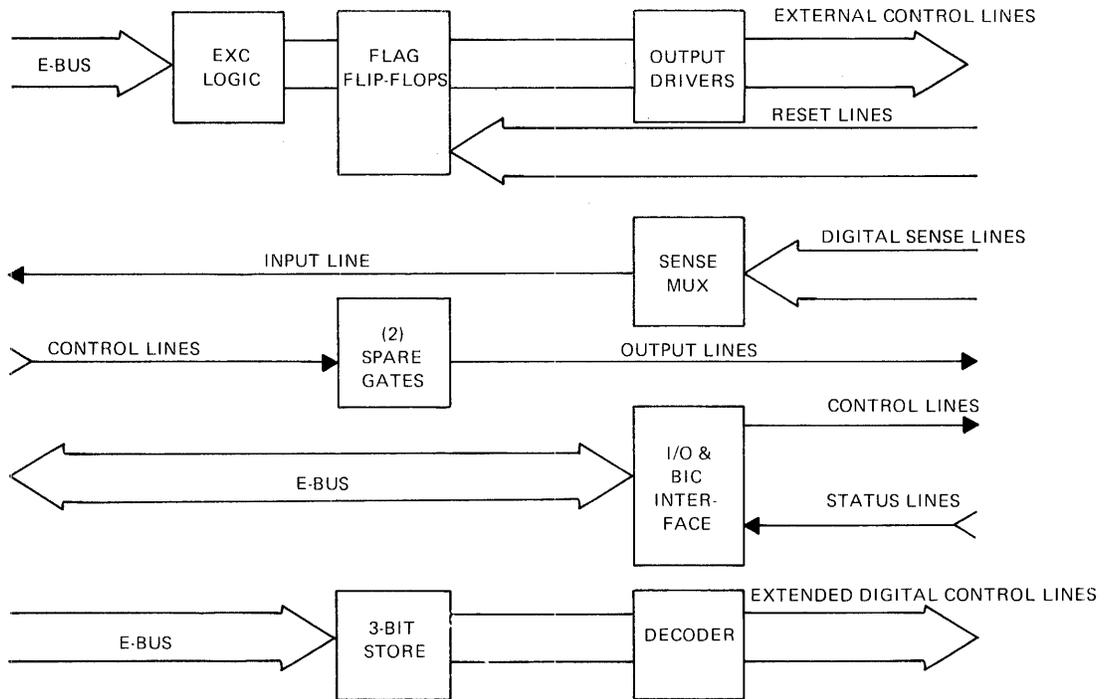
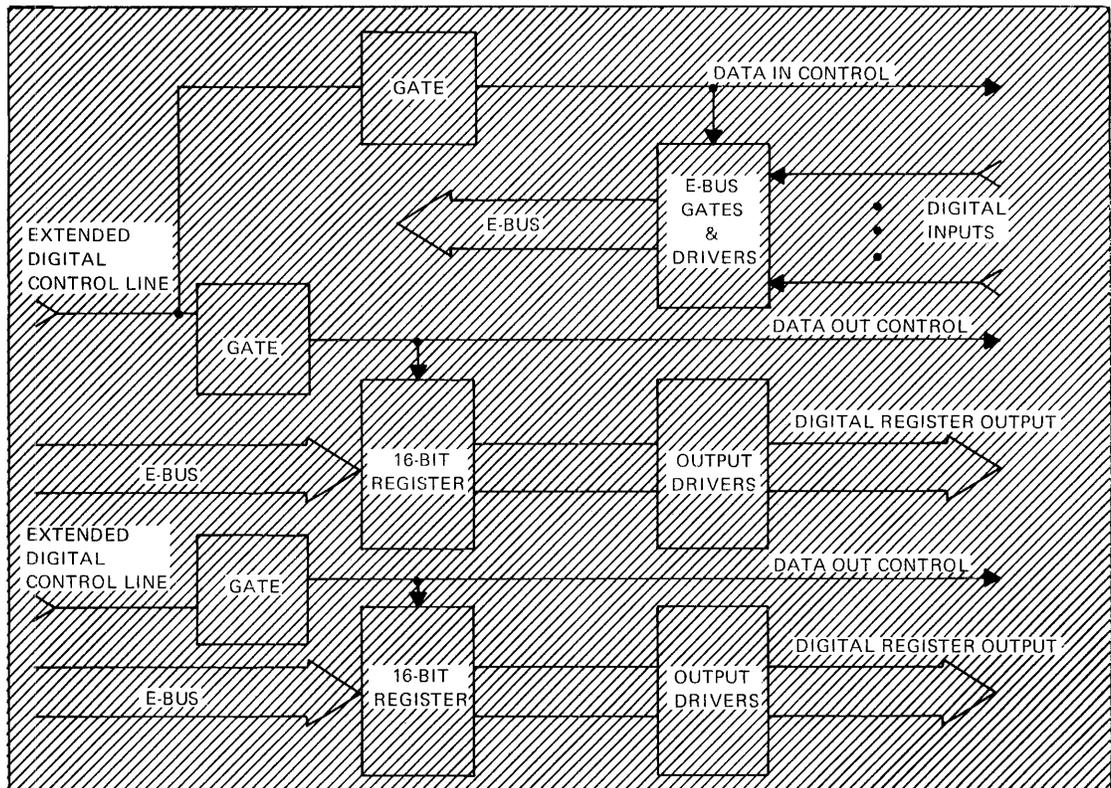


Figure 1-1. Digital Output Module Block Diagram

The master DOM contains the Select logic. Once selected, a register or gated input remains selected until a different register or gated input at the same address is selected, until SYSTEM CLEAR occurs, or until power is interrupted.

Data transfers may be performed under program control or via direct memory access (DMA); interface logic to the required Buffer Interlace Controller (BIC) is provided for the DMA transfer.

#### External Control (EXC) Interface

External Control signals, which are generated by the computer to control operations in external devices, are distributed to the external devices via eight EXC output lines. The DOM's EXC interface logic selects one of the eight output lines according to the contents of the function code received from the computer. The master DOM contains all EXC interface logic for that device address.

#### Sense Interface

The Sense multiplexer on the Digital Output Module selects one of eight sense input lines from external devices and gates the logic level present on that line to the computer. The master DOM contains all Sense interface logic for that device address.

## 2. PROGRAMMING

### 2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DOM and presents instructions for using the DOM software test package for module checkout. This section also describes the usage of two special driver programs which are supplied with the DOM. More detailed programming information may be found in the 620 series or V73 system handbooks.

A program directs DOM operation in four ways:

- Transfers data to digital output registers.
- Reads gated inputs.
- Distributes signals to External Control lines.
- Checks Sense input lines.

Note that data transfers may also be performed using the Buffer Interlace Controller (BIC) hardware option.

### 2.2 DATA TRANSFER UNDER PROGRAM CONTROL

The essential programming instructions for transferring data to a DOM output register are shown in Table 2-1. The instructions are given in the form of a block of code from a typical program.

A digital output register is selected for a data transfer operation by means of an EXC2 instruction. For example, an instruction with the format EXC2 XYY selects register number X at device address YY. Table 2-2 shows the standard register

and gated input number assignments for a DOM device address. After a register is selected, data is transferred to it by means of an OAR, OBR, or OME instruction.

Table 2-1. Instructions To Output Data Under Program Control

<u>Program Step</u>	<u>Function</u>
ONE LDA J	Load value of variable J into the computer A register. (LDB may be used instead of LDA.)
TWO EXC2 XYY	Select module's register or gated input number X (0 to 7) at device address YY (50 to 57).
THRE OAR OYY	Output data from A register to module at address YY (50 to 57). (OBR would be used if LDB had been used. OME could also be used to output data.)
(Time Delay Code)	
(Code to Generate Next Output Number)	
JMP ONE	

Table 2-2. Digital Register and Gated Input Number Assignments

Module	Register Number	Input Number
DOM (master)	0, 1	0
DOME (first slave)	2, 3	2
DOME (second slave)	4, 5	4
DOME (third slave)	6, 7	6

When an output register is selected at a particular device address, it remains selected until another EXC2 instruction selects a different register at the same device address. For example, assume the following sequence of coding:

EXC2	153	Select Second Register on First Module at Device Address 53.
⋮		
EXC2	253	Select First Register on Second Module at Device Address 53. This changes the selection specified by the previous EXC2 since both registers are located at the same device address.
⋮		
EXC2	252	Select First Register on Second Module at Device Address 52. This has no effect on the previous EXC2 instructions since the registers are located at different device addresses.

Thus, it is possible to select one register or gated input at each DOM device address. The following example illustrates the selection and usage of registers and inputs at four different device addresses.

EXC2	050	Select First Register on First Module at Device Address 50.
EXC2	351	Select Second Register on Second Module at Device Address 51.
EXC2	453	Select First Register on Third Module at Device Address 53.
EXC2	452	Select Gated Input on Third Module at Device Address 52.
LDA	V1	Load Variable V1 into Computer Register A.
LDB	V2	Load Variable V2 into Computer Register B.
OAR	050	Output V1 to Selected Register at Device Address 50.
OBR	051	Output V2 to Selected Register at Device Address 51.
LDA	V3	Load Variable V3 into Computer Register A.

OAR	053	Output Variable V3 to Selected register at Device Address 53.
CIB	052	Read Selected Input at Device Address 52 into Computer Register B.

### 2.3 DATA TRANSFER WITH BUFFER INTERLACE CONTROLLER

The Buffer Interlace Controller (BIC) is a hardware option which allows the user to transfer a block of data to or from a peripheral device using only one set of instructions. The user loads the first and last memory address location for a data block into special registers in the BIC; the BIC then transfers the specified data block to (or from) the peripheral device.

Once a program initiates the BIC data transfer, the BIC operates in parallel to the computer program, stealing cycles to access data from memory via direct memory access. Thus, the program can proceed independently with other processing.

Typically, the program instructions for initializing a BIC are coded as a separate subroutine. The applications program then calls this subroutine when BIC usage is required. Table 2-3 illustrates the coding of a BIC initialization subroutine and demonstrates the usage of the subroutine within an applications program.

The sequence of operations is as follows:

BIC Subroutine -

1. Sense that BIC is not busy, using a standard SEN 020 instruction. The BIC cannot be initialized while it is busy. If busy, loop until BIC completes its operation.
2. Initialize the BIC, using a standard EXC 021 instruction.
3. Store data block's initial and final addresses in the appropriate BIC address registers.
4. Enable the BIC, causing data transfer.

Table 2-3. Instructions To Output Data Under BIC Control

<u>Program Step</u>			<u>Function</u>
BIC Subroutine -			
BICS	ENTR	0	
WAIT	SEN	020, GO	Go when BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
GO	EXC	021	Initialize BIC.
	OME	020, FIRST	Set start address of memory block.
	OME	021, LAST	Set end address of memory block.
	EXC	020	Enable BIC.
	RETU*	BICS	
Applications Program -			
	EXC2	0650	Select channel.
WAIT	SEN	MNN, READY	Loop if device not ready.
	JMP	WAIT	
READY	CALL	BICS	Set up BIC.
	EXC	050	Connect BIC to DOM.
TWO	NOP		
	NOP		
	SEN	020, TWO	Check BIC not busy; return to TWO if busy.
	SEN	021, TEN	Check for abnormal stop.

Applications Program -

1. Select the DOM or DOME output channel by using the appropriate EXC2 instruction.
2. Wait until the peripheral device is ready to receive data. Sense line M at device address NN (50 to 57) is used to declare the device's status. Loop if the device is busy.
3. Call BIC subroutine.

4. Connect BIC to DOM, using an EXC instruction. An EXC 0YY instruction, where YY is the DOM device address, is used to output data. An EXC 1YY instruction is used to read gated input data.
5. The sample program in Table 2-3 suspends computation while the BIC is busy by looping around the statements,
 

```

TWO   NOP
      NOP
      SEN 020, TWO
      
```

 until data transfer has been completed.
6. Check for an abnormal stop; if yes, branch to suitable diagnosis or correction code.

Note that the BIC initial and final register addresses may be any pair of octal numbers in the range 20 through 27. Ordinarily, in systems employing more than one BIC, addresses 20 and 21 are assigned to the first BIC's registers; 22 and 23, 24 and 25, and 26 and 27 are assigned to the second, third, and fourth pairs of registers, respectively.

#### 2.4 GATED INPUTS

DOM gated inputs are selected in the same manner as digital output registers, using EXC2 instructions. For example, the instruction EXC2 XYY selects gated input number X (0, 2, 4, or 6) at device address YY (50 to 57). Table 2-2 shows the gated input number assignments for each DOM device address. Once selected, the gated input at a particular device address remains selected until another EXC2 instruction selects a different register or gated input at the same device address.

After an input is selected, it is read by means of an INA, INB, IME, CIA, or CIB instruction.

## 2.5 EXTERNAL CONTROL

External Control signals may be generated by a computer program to provide a variety of logic controls for external devices.

The user has eight External Control lines available at each DOM. The instruction that causes an External Control Signal is:

EXC      XYY

where X (0 to 7) defines one of eight External Control lines at DOM device address YY (50 to 57).

The signals are also made available to the backplane connectors so that they may be used to control certain portions of DOM logic when required by the use of an option such as the BIC. This use of EXC signals will depend on specific applications of the DOM.

A program can set, but cannot reset, an External Control signal; reset is a function of external hardware. As determined by external interconnections, one External Control signal can reset another, other external electronic components can control reset, or the External Control signal can reset itself (pulse operation). Several methods for resetting External Control output signals are discussed in this section. These methods illustrate how the program can use the EXC command to trigger sequences of operations that have been predetermined by system hardware interconnection. The wiring configurations for these methods are illustrated in Figures 2-1 through 2-6. In all cases, some external wiring is required; the external modifications for each method are shown to the right of the vertical dashed line in each figure. Section 3.2 discusses the circuit logic for these reset types.

### Command Sequence Reset

By connecting the EXC-N output of one latch to the REX-M of another latch, selecting the first will reset the second. This requires that the function codes in a series

of EXC commands always follow the sequence prescribed by the latch interconnections. Figure 2-1 illustrates one configuration. In this example, the command sequence would progress from EXC-0 to EXC-7.

For example, in the following sequence of instructions used with this configuration, one External Control line resets one other line.

EXC	050	EXC 750 is automatically reset, EXC 050 is set.
EXC	150	EXC 050 is automatically reset, EXC 150 is set.
EXC	250	EXC 150 is automatically reset, EXC 250 is set.

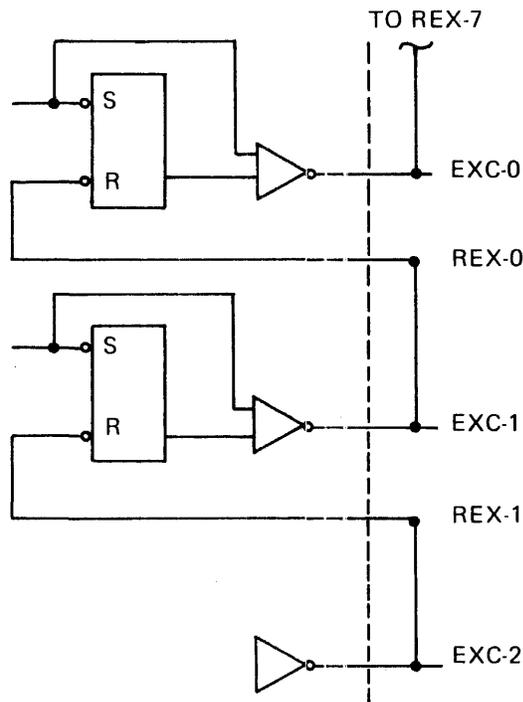


Figure 2-1. Command Sequence Reset Wiring

### Special Assignment Reset

One latch can be assigned as the reset latch. An EXC command selecting that latch will then reset all other EXC latches. Figure 2-2 illustrates this configuration. The following sequence of program instructions used with this configuration functions as follows:

EXC	050	Set EXC 050.
EXC	150	Set EXC 150.
EXC	250	Set EXC 250.
EXC	750	EXC 050, EXC 150, and EXC 250 are automatically reset.

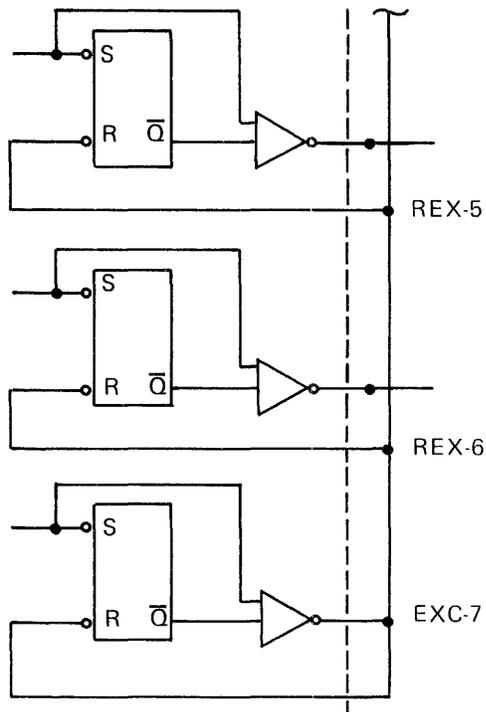


Figure 2-2. Special Assignment Reset Wiring

### Fixed Delay Reset

An EXC latch can reset itself, following a suitable delay provided by an RC, transmission line, or other delay circuit. Figure 2-3 illustrates a typical latch circuit

with an RC delay. An example of an instruction which can be used with such a configuration is as follows:

EXC 050 EXC is set for  $nn \mu\text{sec}$  then resets itself. ( $nn$  is determined by delay hardware added to the EXC output.)

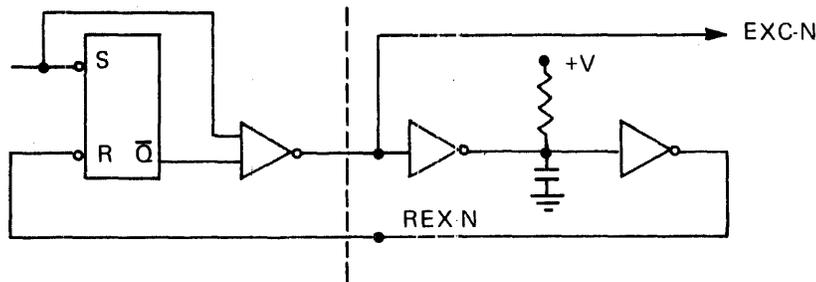


Figure 2-3. Fixed Delay Reset Wiring

Reset Returned By Receiving Device

The reset signal can be returned by the receiving device as shown in Figure 2-4. In this case, the pulse width is determined by the cable length. This insures that the pulse width is great enough for proper reception, regardless of cable capacitance.

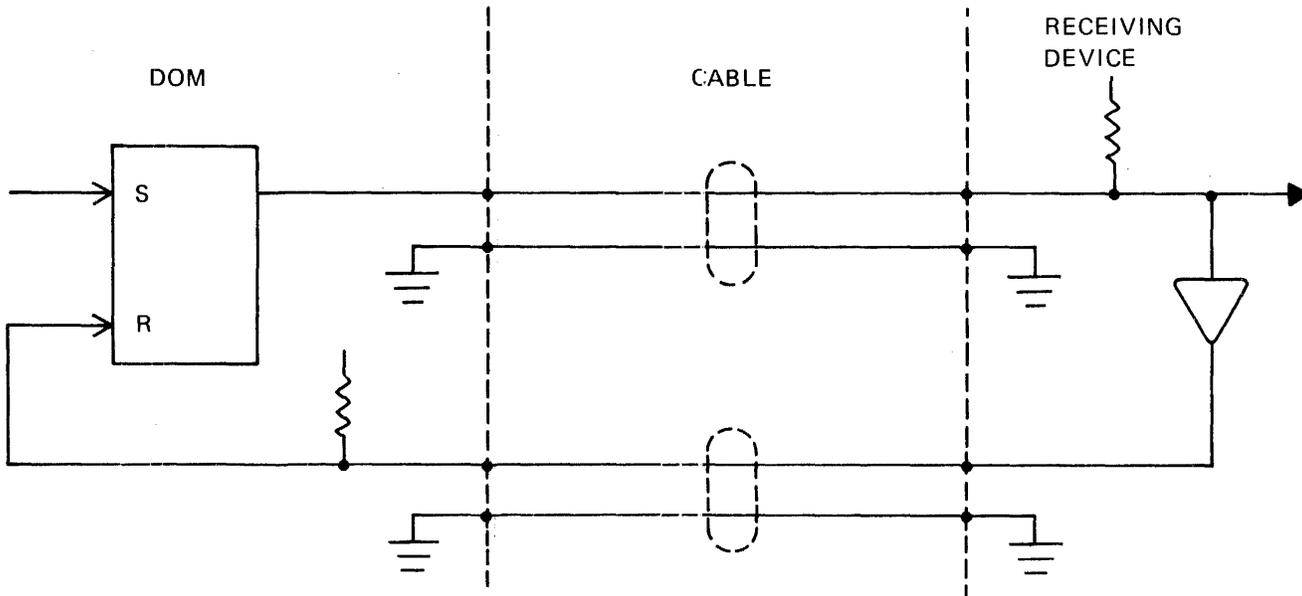


Figure 2-4. Reset Returned By Receiving Device

### Automatic Reset

Connecting a REX-N output to ground will cause the EXC-N output to reset as soon as the EXC input to the latch goes false. In the 620/L computer, this produces a 200 nanosecond pulse. (The pulse duration will differ for other computers.)

Figure 2-5 illustrates such a configuration. In this configuration, an EXC is set, and then reset after 200 nanoseconds. This is accomplished by making the EXC latch output follow the latch input, which is a 200 nanosecond pulse. Normally, the input pulse causes the EXC to be set "on", but the input pulse in no way influences resetting the EXC to "off".

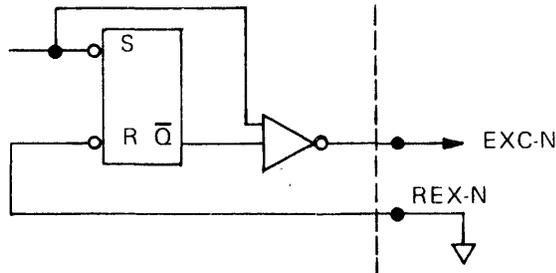


Figure 2-5. Automatic Reset Wiring

### External Logic Reset

In this case, the flip-flop is set by the program and reset by the external device. This is especially useful in passing data or control commands; the program sets the EXC flag to indicate that data is ready, and the external device resets it to acknowledge that it has received the data or that it is ready to accept additional data. The EXC output is connected to a Sense input as well as to the external device, so the program can determine that the acknowledgement has been received. (See Figure 2-6.) The same scheme can, of course, be used for receipt of data by the computer.

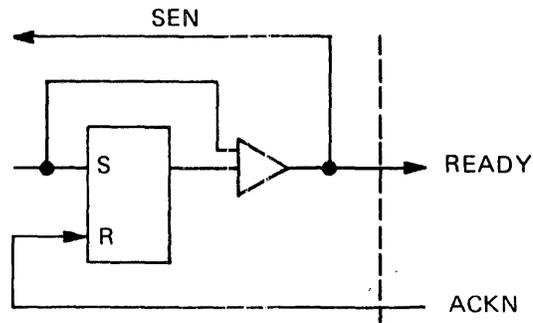


Figure 2-6. External Logic Reset Wiring

### External Control Usage With BIC

Table 2-4 illustrates a program using External Control Line 150 to connect the BIC to the Digital Output Module at device address 050. As discussed in Section 3.1, the execution of EXC 150 also establishes the direction of data flow into memory.

## 2.6 SENSE LINES

Sense lines allow the program to sense a signal from an external device, and branch depending on whether the Sense line is true or false.

There are eight external sense lines associated with each DOM device address. The command which selects a sense line is:

SEN     XYY

X (0 to 7) defines a specific line at device address YY (50 to 57).

Table 2-4 illustrates three uses of the SEN statement. Statement TWO inhibits data transfer via the BIC until Sense line 4 at device address 50 is sensed "false". The other two SEN statements are BIC system commands. (See 620 series or V73 system handbooks.)

Table 2-4. Use of External Sense Logic

	<u>Program Step</u>		<u>Function</u>
WAIT	SEN	020, ONE	Sense BIC not busy.
	NOP		
	NOP		
	JMP	WAIT	
ONE	EXC	021	Initialize BIC.
	OAR	020	Set start address in BIC register.
	OBR	021	Set end address in BIC register.
	EXC	020	Enable BIC
NOP	NOP		
	NOP		
TWO	SEN	450, NOP	Start data transfer when Sense line 4 at device address 50 is "false". Branch back if "true".
FIVE	EXC	150	Connect BIC to DOM.
	SEN	021, TEN	Check for abnormal stop.

## 2.7 DOM SOFTWARE DRIVERS

Two driver programs are supplied to provide convenient access to Digital Output Modules without detailed knowledge of hardware. These drivers may be used by themselves or embedded in an operating system.

The drivers and their functions are:

PDOM - Provides programmed data transfers, either input or output.

DDOM - Provides direct memory transfers, either input or output.

Note that these drivers assume the following device address assignments:

<u>Address (Octal)</u>	<u>Device</u>
050	DOM
020-021	BIC, No. 1
022-023	BIC, No. 2
024-025	BIC, No. 3
026-027	BIC, No. 4

If other device addresses are required, a reassembly of the drivers must be performed.

#### Programmed Data Transfer (PDOM)

The programmed data transfer driver (PDOM) provides programmed data transfers to or from a selected DOM. A variable number of 16-bit words are transferred each time the driver is called.

PDOM is called with the following assembly language sequence:

```
CALL PDOM, DOMNR, I/O SELECT, NUM, STRT ADDR, ERROR EXIT
```

All entries in the calling sequence are either direct addresses or indirect addresses which point to the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

DOMNR - An integer value which specifies the DOM register or input to be selected. The range of DOMNR must be between 1 and 64, inclusive;

otherwise control passes to ERROR EXIT. The DOMNR arguments correspond to the actual device address codes as follows:

<u>DOMNR</u>	<u>Device Address</u>
1	050
2	150
3	250
•	•
•	•
•	•
9	051
•	•
•	•
•	•
64	757

I/O SELECT - A pointer to the location of an I/O select code. The select code must be a one (1) which specifies input, or a zero (0) which specifies output. Note that the DOM hardware provides 32 input channels and 64 output channels. The DOMNR argument must be an odd number (1, 3, 5, 7, etc.) when calling for input. A conflict between the DOMNR and I/O SELECT arguments causes the driver to pass control to ERROR EXIT.

NUM - An integer value which specifies the total number of 16-bit words to be transferred to or from the selected DOM. If NUM is zero or less control passes to ERROR EXIT.

STRT ADDR - A pointer to the location containing the first word address of the input or output buffer.

ERROR EXIT - The actual start address of the user's error routine. Control is transferred to ERROR EXIT when illegal input arguments are detected.

Appendix C contains a sample program which illustrates the use of PDOM.

### Direct Memory Data Transfer

Two programs, DDOM and SDOM, are provided to utilize the BIC to transfer data directly from memory to a selected DOM without programmed intervention. DDOM and SDOM offer two advantages over PDOM:

- Data transfer rates are not limited by software overhead.
- The applications program is freed to work on other processes while the BIC supervises and controls the data transfer.

Unlike other peripherals, DOMs do not have built-in logic to determine when the next data item should be transferred to them. Therefore, external hardware must be provided to indicate when data from memory is to be transferred to the DOM. This is accomplished by providing a Data Ready line at P1-73 on the computer backplane. The data transfer timing is completely under the control of this line, which is also available on J1-9.

In addition to this external signal, two of the eight External Control outputs on the DOM control module must be dedicated. One jumper connects P1-79 to P1-74, and another jumper connects P1-80 to P1-75. The DDOM driver uses the following External Control lines for this function:

<u>DOMNR</u>	<u>EXC Used For BIC Connect</u>	
	<u>Output From Memory</u>	<u>Input to Memory</u>
1-8	EXC 050	EXC 150
9-16	EXC 051	EXC 151
17-24	EXC 052	EXC 152
25-32	EXC 053	EXC 153
33-40	EXC 054	EXC 154
41-48	EXC 055	EXC 155
49-56	EXC 056	EXC 156
57-64	EXC 057	EXC 157

DTO-X and DTI-X must be wired in daisy chain fashion from each master DOM to its slave DOMEs. P1-102 is wired to P1-102 of each DOME, and P1-63 is wired to P1-63 of each DOME. J1-5 and J1-8 also must be grounded so that the flip-flops associated with EXC 0XX and EXC 1XX are automatically reset.

Direct memory data transfer to a DOM is accomplished by a two-step process. First, DDOM is called to initiate the transfer and return control immediately. Then, SDOM is called at the user's convenience to determine when the transfer is complete.

### DDOM Driver

The DDOM driver is called with the following assembly language sequence:

```
CALL DDOM, BICNR, DOMNR, I/O SELECT, STRT ADDR, ERROR EXIT
```

All entries in the calling sequence are either direct addresses or indirect addresses of the actual arguments. Multiple levels of indirect addresses are permitted. The arguments are defined as follows:

BICNR - An integer value which specifies the BIC to be used for data transfer. The range of BICNR is from 1 to 4 corresponding to BIC device addresses 20-21<sub>8</sub> through 26-27<sub>8</sub>. A value outside the legal range causes control to pass to ERROR EXIT.

DOMNR - An integer value which specifies the DOM register or input to be selected. The range of DOMNR must be between 1 and 64, inclusive; otherwise control passes to ERROR EXIT. (See PDOM driver for a description of DOMNR and actual device address relationship.)

I/O SELECT - A pointer to the location of an I/O select code. The select code must be a one (1) which specifies input, or a zero (0) which specifies output. Note that the DOM hardware provides 32 input channels and 64 output channels. The DOMNR argument must be an odd number when calling for input. A conflict between the DOMNR and I/O SELECT causes the driver to pass control to ERROR EXIT.

NUM - An integer value which specifies the total number of 16-bit words to be transferred to or from the selected DOM. If NUM is zero or less, control passes to ERROR EXIT.

STRT ADDR - A pointer to the location containing the first word address of the input or output buffer.

ERROR EXIT - The actual start address of the user's error routine. Control is transferred to ERROR EXIT when illegal input arguments are detected.

Appendix C shows a sample program which illustrates the use of DDOM.

### SDOM Routine

The SDOM routine checks the status of a previously initiated direct memory data transfer. SDOM is called with the following assembly language sequence:

```
CALL SDOM, STATUS
```

The single entry in the calling sequence can be either a direct address or an indirect address which points to the actual argument. The argument is defined as follows:

STATUS - This argument receives a value of 0, 1, or 2 to indicate the status of the transfer operation:

<u>Value</u>	<u>Meaning</u>
0	Operation not complete
1	Operation complete; no errors
2	Operation aborted

## 2.8 TEST PROGRAMS

A set of test programs is provided for DOM checkout. The set consists of three programs which may be selected through the Maintain II Test Executive. The programs, numbered 0 through 3, are as follows:

<u>Test No.</u>	<u>Description</u>
0	Returns control to the Test Executive Program.
1	Tests External Control and Sense lines.
2	Tests registers and gated inputs.
3	Tests BIC interface.

These programs may be selected in any order and may be run as often as desired. This allows registers and inputs with different device codes to be tested.

The minimum computer configuration on which the tests may be run is a 620 or V73 series computer with 4 K of memory, a teletype terminal, and a DOM card. In addition, a DOM test shoe (Part No. 03-950401) is required for running the tests.

### Supervisor Program

A simple supervisor or test program selector is provided as part of the test package to allow the user to select individual tests and return control to the Test Executive Program. The Test Executive Program is a standard Varian software option which must be loaded and run prior to the initiation of the DOM test package. Instructions for operating this program are given in the Test Program Manual (Publication No. 98A 9908-960). The DOM test package is loaded through the Test Executive.

When the Test Executive Program is running, the "L" command may be used to load the test package and transfer control to its supervisor. If the test package is already loaded, the "G500" command may be used to transfer control to the supervisor.

When the supervisor is activated, it responds by issuing a carriage return/line feed and by starting to print a series of prompting messages. The user must enter a valid response to each message as it is printed. An invalid response causes the message to be repeated. The first message is:

```
DIGITAL OUTPUT TEST SUPERVISOR
ENTER DEVICE ADDRESS?
```

The user must enter the DOM device address, which is an octal number between 050 and 057, followed by a period. The supervisor will then print:

ENTER BIC DEVICE ADDRESS?

The user must enter any of the following assigned octal numbers: 020, 022, 024, or 026 followed by a period.

The DOM and BIC device addresses entered at this time will be used throughout the three tests, where applicable. To change device address selections, the supervisor must be reactivated from the Test Executive Program or run from location 500. After the device addresses have been entered, the supervisor will print:

ENTER TEST NO. ?

The user should enter any number between 0 and 3 followed by a period. The supervisor will then transfer control to the selected test program, which will identify itself and perform its specified functions.

Test 1 should be used for each master DOM to test the EXC and Sense logic.

Test 2 should be used for each digital output register in the system.

Test 3 should be used to check the BIC interface to the DOM and should be exercised on each digital output register that will be driven under BIC control.

#### Sense Switches

During all DOM tests, the sense switches may be used to control the mode of operation. The normal mode is followed when all switches are OFF; one or more switches may be set to control operation as follows:

SS1	Sense switch 1 suppresses teletype printouts of test results and error messages. This function is useful to speed up the
-----	--

continuous execution of a test so that an oscilloscope may be used to monitor signals.

SS2 Sense switch 2 causes a test to repeat indefinitely without user intervention.

SS3 Sense switch 3 terminates execution of a test and returns control to the supervisor. If sense switch 3 is set when the supervisor requests a new test number, the following message will be printed:

RESET SENSE SWITCH 3

A new test may be selected after SS3 is reset.

### Test 1 - External Control and Sense Test

This test uses a special test shoe which must be plugged into J1 and J2 of the DOM card. The test checks all EXC and Sense lines on a given device address. The test shoe is designed to connect each EXC output to a SENSE input and to reset another EXC according to the following table.

<u>EXC output</u>	<u>Sense Line</u>	<u>EXC reset</u>
00XX	03XX	06XX
02XX	07XX	00XX
04XX	05XX	02XX
01XX	06XX	04XX
03XX	04XX	01XX
05XX	02XX	03XX
07XX	00XX	05XX
06XX	01XX	07XX

Therefore, at each step in the table only one of the Sense lines should be true at a time. All Sense lines are polled after each step and errors are reported if detected and if sense switch 1 is reset.

When the test program is activated, it will print:

### EXTERNAL CONTROL AND SENSE TEST

If no errors occur during the execution of the test, the program returns control to the supervisor after printing the following message:

TEST PASSED

If errors occur during the test, one or more of the following messages will be printed:

EXC 00XX OR SEN 03XX ERROR  
EXC 02XX OR SEN 07XX ERROR  
EXC 04XX OR SEN 05XX ERROR  
EXC 01XX OR SEN 06XX ERROR  
EXC 03XX OR SEN 04XX ERROR  
EXC 05XX OR SEN 02XX ERROR  
EXC 07XX OR SEN 00XX ERROR  
EXC 06XX OR SEN 01XX ERROR

If the first error occurs, the problem may be in the address decoder logic on the master DOM.

### Test 2 - Register and Gated Input Test

Each DOM card has two output registers and one 16-bit gated input channel. For purposes of these tests the registers and inputs at a particular device address are numbered as shown in Table 2-2.

The DOM test shoe is used to connect digital output registers to the gated inputs. The even-numbered output register is assigned to J2-1 through 16 for bits 0 to 15, respectively; the odd-numbered output register is assigned to J2-17 through 32 for bits 0 to 15, respectively; a single set of input gates is assigned to J1-29 through J1-44 for bits 0 to 15, respectively on each card. The test shoe feeds the even-

numbered output register directly back into the input gates with a wired-OR condition with the odd-numbered output register. The odd-numbered output registers are fed back in a scrambled form.

The program outputs a series of 16-bit numbers to the selected output register and reads them back in through the input gates and unscrambles them if the odd-numbered register is selected. All 65,536 different 16-bit numbers are output. The values are checked to see if the inputs match the original outputs.

When the test program is activated, it will print:

```
REGISTER TEST
ENTER OUTPUT REGISTER NO
```

The user should enter the appropriate number between 0 and 7 followed by a period. The test program compares the inputs to the outputs and prints any readings which do not match. If the input and output readings match, the program prints:

```
TEST PASSED
```

This test runs for about 15 seconds for even-numbered registers and about 22 seconds for odd-numbered registers. The odd-numbered register tests run longer because the input must be unscrambled before it can be compared to the output. This is not required on the even-numbered register tests.

### BIC Interface Test

This test uses the even-numbered output register and input gates on each DOM under BIC control to test the BIC interface. The output register is tied directly back into the input gates by the test shoe.

EXC 0 is used to provide the trap-out request by wiring P1-74 to P1-79. EXC 1 is used to provide the trap-in request by wiring P1-75 to P1-80. Note that these connections should be made even if the BIC is not used.

When the test program is activated, it prints:

```
BIC INTERFACE TEST
ENTER OUTPUT REGISTER NO
```

The user must enter one of the following values: 0, 2, 4, or 6 followed by a period.

During the test, trap-in and trap-out requests are given alternately until 20 words have been passed out and then back into 40 sequential memory locations. They are checked to see that each pair of words matches; if not, both input and output are listed in octal. If all 20 pairs match, the program prints:

```
TEST PASSED
```

The 20 words passed during the test are as follows:

- All odd bits set (0125252<sub>8</sub>)
- All even bits set (052525<sub>8</sub>)
- Each single bit set (0100000<sub>8</sub>)  
                          (0040000<sub>8</sub>)  
                          ⋮  
                          (001<sub>8</sub>)
- All bits reset (0<sub>8</sub>)
- All bits set (0177777<sub>8</sub>)

### 3. I/O INTERFACE THEORY OF OPERATION

The Digital Output Modules coordinate four types of communication between the computer and peripheral devices: digital data out, digital data in, External Control signals out, and Sense signals in. The DOM logic responsible for providing these four interfaces is discussed in this section.

All communication between the DOM and the computer is conducted on the computer I/O bus. In the following discussion, mnemonics used to identify E-bus signals include the suffix "I". Signals transferred between the DOM and the BIC are carried on the B-bus; mnemonics for these signals include the suffix "B". Refer to a Varian 620 series or V73 system handbook and Buffer Interlace Controller Manual for details regarding communication conducted via the computer I/O bus.

The following discussions are keyed by letter designations to schematics and logic diagrams presented in Appendix D.

#### 3.1 DATA TRANSFER

##### Program-Controlled Data Transfer

A data transfer operation occurs in two stages. First, the individual register or gated input is selected; then a data word is sent to the selected register.

##### DOM Selection Stage

The selection stage begins when the computer enters the desired device address and function code on E-bus lines EB00-I through EB05-I and EB06-I through EB08-I. A NAND gate on the addressed master DOM decodes the device address and generates a Device Select signal. This is combined with the control line pulse FRYX-I (Function Ready). The resulting signal Function Select combines with a true level on EB15-I to clock the contents of the function code into the EXC2 storage register.

The EXC2 Decode Logic selects one of eight output lines, EXC2-0 through EXC2-7, according to the contents of the function code. Each EXC2 line is connected via a wire wrap jumper in the backplane to the clock input gate of a different register or gated input. An active EXC2 line enables one of three inputs to the clock input gate in preparation for the data transfer stage of the operation.

### Data Transfer Stage

The device address is again placed on the E-bus. A true level on EB14-I identifies the operation as a data transfer out and, together with Function-Select, sets the data transfer out (DTOS) latch. Output of the DTOS latch enables the second input to the clock input gate.

After the control pulse FRYX-I goes false, the computer removes the device address from the E-bus and places a data word on lines EB00-I through EB14-I, with a sign bit on EB15-I. This is followed by the control pulse DRYX-I. DRYX-I enables the clock input gate of the selected register or gated input, DRYX-I also resets the DTOS latch.

After DRYX-I goes false, the only true input to the clock input gate of the register is provided by the selected EXC2 line. This input remains true until a different EXC2 line at that device address is selected. Until that time, subsequent data transfer operations for that device address will be routed to the same register or gated input, without requiring another EXC2 instruction.

### BIC-Controlled Data Transfer

When a data transfer is under BIC control, a different set of DOM logic is involved.

### DOM Selection Stage

The DOM selection stage is the same for a BIC-controlled data transfer as for a program-controlled data transfer; the data transfer stage, however, is not.

## Data Transfer Stage

The BIC can be used to control the transfer of data to or from the computer memory under the control of the TROX-B signal.

The DOM provides a flip-flop to allow the computer to determine the direction of data flow. EXC-0 is normally wired to the X-OUT terminal and EXC-1 is normally wired to the X-IN terminal. REX-0 and REX-1 are grounded so that their corresponding EXCs operate as pulses.

EXC-0 is then executed when the BIC is to transfer data out of memory and EXC-1 is executed when the BIC is to transfer data into memory.

XRDY is an input signal to the signal to the Digital Output Module which is used to control the rate at which the BIC transfers data. XRDY presents two logic loads and has a 1 K ohm resistor to +5 Vdc. A low true pulse received by XRDY initiates a BIC data transfer operation after the BIC is connected. The XRDY pulse should be less than 2 microseconds and greater than 50 nanoseconds in duration.

### 3.2 EXTERNAL CONTROL DECODE

Every master DOM makes available eight EXC outputs. An output goes true when its flip-flop is set by the EXC decode logic. A function code, provided by the computer as a result of an EXC program instruction, specifies which EXC output flip-flop is set.

EXC output flip-flops are not reset by program instructions alone; they may be reset through a variety of hardware or hardware/software techniques. Some examples of methods for resetting EXC output flip-flops are discussed in Section 2.5.

The EXC output driver is capable of switching signals at levels up to +30 volts, with current sinking of up to 250 mA.

### 3.3 SENSE DECODE

Every master DOM is capable of sampling, one at a time, up to eight Sense input lines and forwarding the logic level present on the selected line to the computer. A function code, provided by the computer as a result of a SEN program instruction, specifies which Sense input is to be sampled.

Sense input signals are considered logically true when they are at 0 Vdc and logically false at +4 Vdc. When sampled, a true input will cause a jump condition in the program. The DOM provides a 5.6 K pullup resistor to +5 volts on each Sense input. It is therefore not necessary to drive the Sense inputs high. The Sense inputs are normally connected to external logic (0 to +5 volts) or switch closures to ground.

#### NOTE

Sensed signals should not be allowed to go negative with respect to DOM logic ground and should not be allowed to go more positive than the DOM +5 volts.

### 3.4 LOGIC DESIGN

The basic design of the data output logic is represented in the block diagram of Figure 3-1. Each output register consists of four data output logic devices, each of which contains four TTL/DTL bistable 4-bit latches per device.

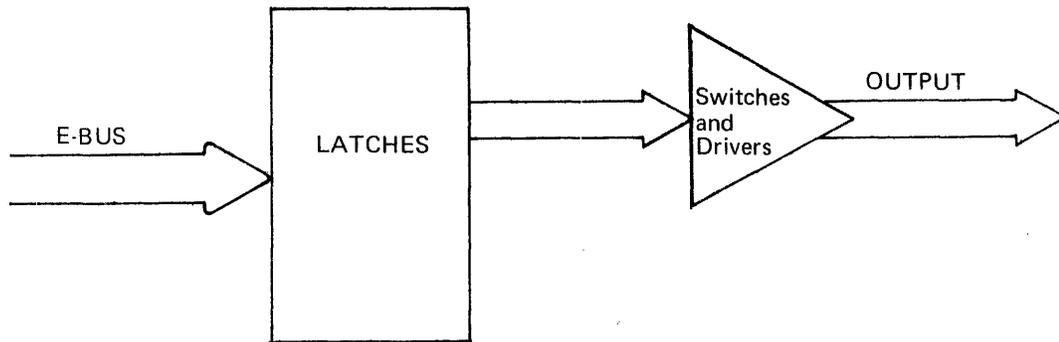


Figure 3-1. Digital Output Logic

Latches

Information present at a data (D) input (see Figure 3-2) is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

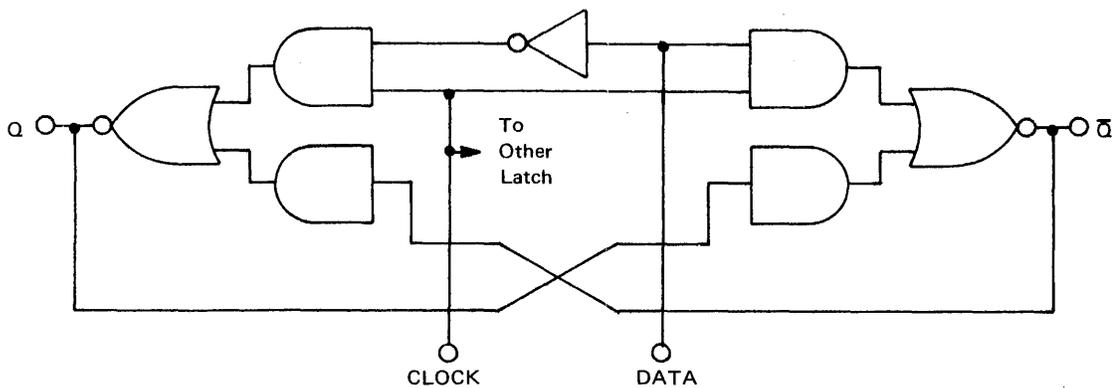


Figure 3-2. Latch - Functional Diagram

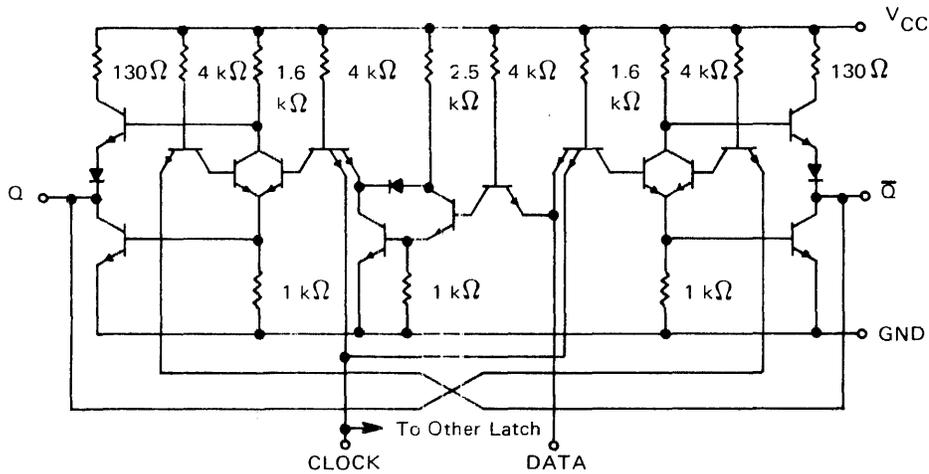


Figure 3-3. Latch - Schematic Diagram

### Drivers

The dual peripheral drivers used in the DOM incorporate the following features:

- 300 - mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

Typical applications of the drivers include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. The drivers offer improved freedom from latch-up and diode-clamped inputs for simplified system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. A schematic diagram of a single driver is shown in Figure 3-4.

Note that although the above specifications and comments apply to the output driver used in the DOM, some caution must be exercised in driver usage. Within the DOM

there is no isolation of the driver grounds from the logic ground of the computer; it is, therefore, recommended that the DOM outputs not be used to switch high-current loads or other loads likely to couple noise into the computer's ground system.

If the DOM is used drive logic, it is recommended that pull-up resistors to +5V be included at the receiving end of the line; the value of the resistor should be 5.6 Kohms (optionally 1 K ohm) maximum, or equal to the characteristic impedance of the line. In this application, total load current should be limited 100 mA.

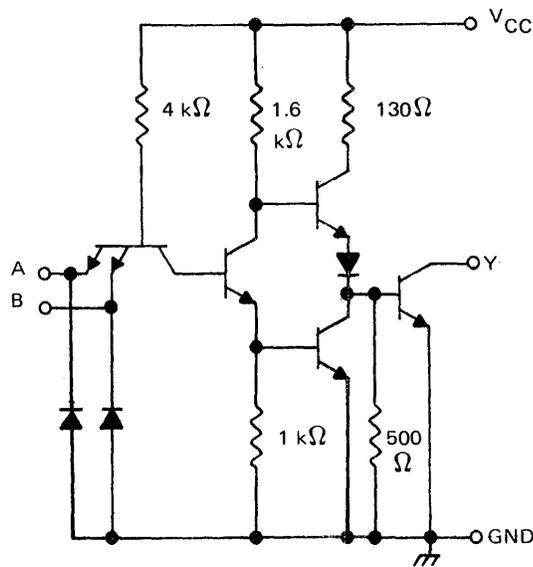


Figure 3-4. Driver - Schematic Diagram



## 4. INSTALLATION

### 4.1 PREREQUISITES

Each DOM or DOME requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by DOMs; their location in the frame is determined solely by considerations of convenience in backplane wiring.

### 4.2 INSTALLATION AND INTERCONNECTION

A DOM is installed vertically with its component side to the left in 620/i and 620/L computers, and horizontally with its component side up in the 620/f computer. Figure 4-1 illustrates a typical installation.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

Connection to the computer I/O-bus and the BIC option B-bus is provided through backplane wiring. All pin assignments for the I/O-bus and B-bus are listed in Appendix A.

For each DOM, connections to external instruments include two output registers and one 16-bit gated input and may include up to eight External Control outputs and up to eight Sense inputs. Pin assignments for these connections are also listed in Appendix A. Recommended connector types for J1 and J2 are identified in the summary of key specifications in Appendix B.

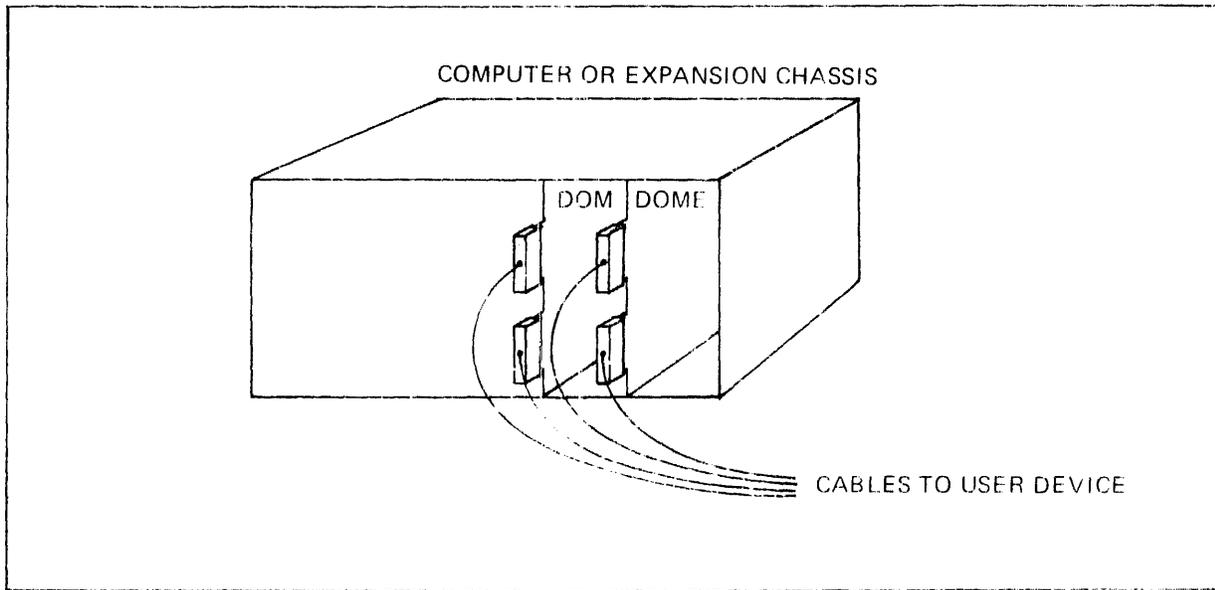


Figure 4-1. Typical Module Installation

Device Address Wiring

Table 4-1 lists the jumper connections required to wire a device address for a master DOM. Note that P1-76 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if multiple master DOM modules have the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Table 4-1. Device Address Wiring

Address	Wirewrap Jumpers		
050	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-65
051	P1-72 to P1-71	P1-69 to P1-68	P1-66 to P1-64
052	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-65
053	P1-72 to P1-71	P1-69 to P1-67	P1-66 to P1-64
054	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-65
055	P1-72 to P1-70	P1-69 to P1-68	P1-66 to P1-64
056	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-65
057	P1-72 to P1-70	P1-69 to P1-67	P1-66 to P1-64

## EXC2 Output Wiring

Table 4-2 lists the jumper connections required to wire the eight EXC2 outputs to select individual registers on the DOM and DOMEs.

Table 4-2. Register Select Connections

SIGNAL	CONNECTION		REGISTER NUMBER
	FROM	TO	
XEXC-0	DOM #1 P1-110	DOM #1 P1-77	1
XEXC-1	DOM #1 P1-112	DOM #1 P1-78	2
XEXC-2	DOM #1 P1-114	DOME #2 P1-77	3
XEXC-3	DOM #1 P1-103	DOME #2 P1-78	4
XEXC-4	DOM #1 P1-104	DOME #3 P1-77	5
XEXC-5	DOM #1 P1-105	DOME #3 P1-78	6
XEXC-6	DOM #1 P1-106	DOME #4 P1-77	7
XEXC-7	DOM #1 P1-108	DOME #4 P1-78	8
DTI-X	DOM #1 P1-63	DOME #2 P1-63	INPUT 2
DTI-X	DOME #2 P1-63	DOME #3 P1-63	INPUT 3
DTI-X	DOME #3 P1-63	DOME #4 P1-63	INPUT 4
DTO-X	DOME #1 P1-102	DOME #2 P1-102	3 & 4
DTO-X	DOME #2 P1-102	DOME #3 P1-102	5 & 6
DTO-X	DOME #3 P1-102	DOME #4 P1-102	7 & 8

## External Control Reset Wiring

Provision must be made for resetting External Control outputs. Basic information on techniques for resetting the outputs is presented in Section 2.5. One possible configuration is illustrated in Table 4-3.

Table 4-3. External Control Reset Wiring

Signals	DOM	DOM
EXC1/REX0	J1-6	J1-5
EXC3/REX2	J1-12	J1-11
EXC5/REX4	J1-18	J1-17
EXC7/REX6	J1-24	J1-23

## XRDY And X-IN/X-OUT Wiring

DOMs used in conjunction with the BIC option require an externally-supplied signal, XRDY, which synchronizes the data transfer with external device operation. EXC0

and EXC1 are connected to X-OUT and X-IN respectively to select the DOM for connection to the BIC and to establish the direction of data transfer. Further discussion of these requirements can be found in Section 3.1 of this manual.

A wiring configuration for BIC operation under internal program control is shown in Table 4-4. This configuration is used when operating the DOM Test Program as described in Section 2.8 of this manual.

For BIC operation under external control (externally supplied timing for BIC-connected operations), the external pulse is provided through J1-19. The pulse is low true and less than 1.8 microseconds for the 620/L computer.

Table 4-4. DOM Wiring for Program-Controlled BIC Operation

BIC Connections	P1-74 to P1-79 to P1-89 P1-75 to P1-80 to P1-87 ----- P1-85 to P1-73
--------------------	---

Note that if the BIC is not used, P1-79 and P1-80 should be grounded or, alternatively, P1-79 should be connected to P1-74, and P1-80 should be connected to P1-75.

### 4.3 INSTALLATION EXAMPLE

A typical DOM could be installed with the following wiring:

#### Device Address 050

P1-71 wired to P1-72  
P1-68 wired to P1-69  
P1-65 wired to P1-66

#### Register Select Connections

P1-110 wired to P1-77  
P1-112 wired to P1-78

#### BIC Control

P1-74 wired to P1-79  
P1-75 wired to P1-80

Note: If BIC is not used P1-79 and P1-80 should be grounded.

#### EXC Reset (These connections will be inside J1 connector hood.)

J1-5 to J1-4  
J1-8 to J1-7

## APPENDIX A: DOM PIN ASSIGNMENTS

### BACKPLANE WIRING

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1-1	Digital ground	
2	EB00	One bit of Device Address or data word
3	Digital ground	
4	EB01	One bit of Device Address or data word
5	Digital ground	
6	EB02	One bit of Device Address or data word
7	Digital ground	
8	EB03	One bit of Device Address or data word
9	Digital ground	
10	EB04	One bit of Device Address or data word
11	EB05	One bit of Device Address or data word
12	EB06	One bit of EXC, EXC2 or SEN code or data word
13	EB07	One bit of EXC, EXC2 or SEN code or data word
14	EB08	One bit of EXC, EXC2 or SEN code or data word
15	EB09	One bit of data word
16	EB10	One bit of data word
17	EB11	EXC tag line or one bit of data word
18	EB12	Sense tag line or one bit of data word
19	EB13	One bit of data word
20	EB14	Data tag line or one bit of data word
21	EB15	EXC2 tag line or one bit of data word
22	Digital ground	
23	Not used	
24	Digital ground	
25	Not used	
26	Digital ground	
27	FRYX	Function Ready
28	Digital ground	
29	DRYX	Data Ready
30	Digital ground	
31	SERX	Sense Response
32	Digital ground	
33	Not used	
34	Digital ground	
35	Not used	

BACKPLANE WIRING (Continued)

<u>Pin</u> <u>No.</u>	<u>Name</u>	<u>Function</u>
P1-36	Digital ground	
37	Not used	
38	Digital ground	
39	Not used	
40	Digital ground	
41	Not used	
42	Not used	
43	SYRT	Resets system logic
44	IUAX	Interrupt acknowledge from computer
45	Not used	
46	Not used	
47	Not used	
48	Digital ground	
49	TRQX	Transfer Request from DOM to BIC
50	TROX	Identifies direction of BIC-controlled data transfer
51	Digital ground	
52	Not used	
53	Digital ground	
54	CDCX	Notifies BIC that DOM is connected
55	Digital ground	
56	DCEX	Connect signal from BIC
57	Digital ground	
58	TAKX	Transfer Request acknowledge from BIC
59	Digital ground	
60	DESX	Disconnect from BIC
61	Not used	
62	Not used	
63	DTI-X	Jumper connection for DTI-X to DOMEs
64	EB00+	Jumper connection for wiring Device Address
65	EB00-	Jumper connection for wiring Device Address
66	EB0I	Jumper connection for wiring Device Address
67	EB01+	Jumper connection for wiring Device Address
68	EB01-	Jumper connection for wiring Device Address
69	EB1I	Jumper connection for wiring Device Address
70	EB02+	Jumper connection for wiring Device Address
71	EB02-	Jumper connection for wiring Device Address
72	EB2I	Jumper connection for wiring Device Address

BACKPLANE WIRING (Continued)

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1-73	Device Ready	Externally-supplied timing for BIC-connected operations
74	Not used	
75	Not used	
76	Enable	Not used
77	EXC2-N	Jumper connection for EXC2 signal assigned to Register 1
78	EXC2-M	Jumper connection for EXC2 signal assigned to Register 2
79	EPO-N	DOM Select signal for BIC-connected operations
80	Not used	
81	Not used	
82	Not used	
83	Not used	
84	Not used	
85	DTOS	Data transfer request to computer
86	EXC7	Jumper connection for internal use of EXC7
87	EXC5	Jumper connection for internal use of EXC5
88	Not used	
89	Not used	
90	EXC6	Jumper connection for internal use of EXC6
91	EXC2	Jumper connection for internal use of EXC2
92	Not used	
93	EXC3	Jumper connection for internal use of EXC3
94	EXC4	Jumper connection for internal use of EXC4
95	Not used	
96	Not used	
97	Not used	
98	EXC1	Jumper connection for internal use of EXC1
99	Not used	
100	Digital ground	
101	EXC0	Jumper connection for internal use of EXC0
102	DTO-X	Jumper connection for DTO-X signal to DOMEs
103	EXC2-3	Jumper connection for register Select line 3
104	EXC2-4	Jumper connection for register Select line 4
105	EXC2-5	Jumper connection for register Select line 5
106	EXC2-6	Jumper connection for register Select line 6
107	Not used	

## BACKPLANE WIRING (Continued)

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1-108	EXC2-7	Jumper connection for register Select line 7
109	Not used	
110	EXC2-0	Jumper connection for register Select line 0
111	Not used	
112	EXC2-1	Jumper connection for register Select line 1
113	Not used	
114	EXC2-2	Jumper connection for register Select line 2
115	Not used	
116	Not used	
117	Not used	
118	+5 Vdc	
119	Not used	
120	Not used	
121	+5 Vdc	
122	Digital ground	

## TERMINAL EDGE CONNECTOR WIRING

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
J1-1	DTIN	Data Transfer In
2	+5 Vdc	
3	EXC0	Output connection for EXC0
4	Digital ground	
5	REX0	Jumper connection for EXC0 reset
6	EXC1	Output connection for EXC1
7	Digital ground	
8	REX1	Jumper connection for EXC1 reset
9	EXC2	Output connection for EXC2
10	Digital ground	
11	REX2	Jumper connection for EXC2 reset
12	EXC3	Output connection for EXC3
13	Digital ground	
14	REX3	Jumper connection for EXC3 reset
15	EXC4	Output connection for EXC4
16	Digital ground	
17	REX4	Jumper connection for EXC4 reset
18	EXC5	Output connection for EXC5
19	Device Ready	External connection for BIC operation
20	REX5	Jumper connection for EXC5 reset
21	EXC6	Output connection for EXC6
22	Digital ground	
23	REX6	Jumper connection for EXC6 reset

## TERMINAL EDGE CONNECTOR WIRING (Continued)

<u>Pin</u>	<u>Name</u>	<u>Function</u>
J1-24	EXC7	Output connection for EXC7
25	REX7	Jumper connection for EXC7 reset
26	Sense 0	Input connection for Sense 0 line
27	Sense 1	Input connection for Sense 1 line
28	Sense 2	Input connection for Sense 2 line
29	DIN 00	Input word, bit 0, LSB
30	DIN 01	Input word, bit 1
31	DIN 02	Input word, bit 2
32	DIN 03	Input word, bit 3
33	DIN 04	Input word, bit 4
34	DIN 05	Input word, bit 5
35	DIN 06	Input word, bit 6
36	DIN 07	Input word, bit 7
37	DIN 08	Input word, bit 8
38	DIN 09	Input word, bit 9
39	DIN 10	Input word, bit 10
40	DIN 11	Input word, bit 11
41	DIN 12	Input word, bit 12
42	DIN 13	Input word, bit 13
43	DIN 14	Input word, bit 14
44	DIN 15	Input word, bit 15, MSB
J2-1	DOA 00	Register 1 output word, bit 0, LSB
2	DOA 01	Register 1 output word, bit 1
3	DOA 02	Register 1 output word, bit 2
4	DOA 03	Register 1 output word, bit 3
5	DOA 04	Register 1 output word, bit 4
6	DOA 05	Register 1 output word, bit 5
7	DOA 06	Register 1 output word, bit 6
8	DOA 07	Register 1 output word, bit 7
9	DOA 08	Register 1 output word, bit 8
10	DOA 09	Register 1 output word, bit 9
11	DOA 10	Register 1 output word, bit 10
12	DOA 11	Register 1 output word, bit 11
13	DOA 12	Register 1 output word, bit 12
14	DOA 13	Register 1 output word, bit 13
15	DOA 14	Register 1 output word, bit 14
16	DOA 15	Register 1 output word, bit 15, MSB
17	DOB 00	Register 2 output word, bit 0, LSB
18	DOB 01	Register 2 output word, bit 1

TERMINAL EDGE CONNECTOR WIRING (Continued)

<u>Pin</u> <u>No.</u>	<u>Name</u>	<u>Function</u>
J2-19	DOB 02	Register 2 output word, bit 2
20	DOB 03	Register 2 output word, bit 3
21	DOB 04	Register 2 output word, bit 4
22	DOB 05	Register 2 output word, bit 5
23	DOB 06	Register 2 output word, bit 6
24	DOB 07	Register 2 output word, bit 7
25	DOB 08	Register 2 output word, bit 8
26	DOB 09	Register 2 output word, bit 9
27	DOB 10	Register 2 output word, bit 10
28	DOB 11	Register 2 output word, bit 11
29	DOB 12	Register 2 output word, bit 12
30	DOB 13	Register 2 output word, bit 13
31	DOB 14	Register 2 output word, bit 14
32	DOB 15	Register 2 output word, bit 15, MSB
33	Sense 3	Input connection for Sense 3 line
34	Sense 4	Input connection for Sense 4 line
35	Sense 5	Input connection for Sense 5 line
36	Sense 6	Input connection for Sense 6 line
37	Sense 7	Input connection for Sense 7 line
38	DTOA	Data Transfer Out, Register 1
39	Digital ground	
40	Digital ground	
41	+5 Vdc	
42	Digital ground	
43	Digital ground	
44	DTOB	Data Transfer Out, Register 2

## APPENDIX B: SPECIFICATIONS

### DIGITAL OUTPUT

Number	Two 16-bit registers.
Type	Open collector transistor with 5.6 K ohms (1 K ohms, optional) to +5 Vdc. Sinks current when true. Capable of sinking 300 mA. Load pulses (DTOA and DTOB) are externally available; these pulses are 200 nanoseconds in duration, low true.
Available Fanout	30 logic loads.
Maximum Load Capacitance	100 pF.

### DIGITAL INPUT

Number	16 lines gated.
Type	One logic load with 5.6 K ohms (1 K ohm, optional) to +5 Vdc. Low true. Enable Gate (DTIN) is externally available. This signal is 1.9 microseconds in duration, low true.
DTIN Available Fanout	16 logic loads.
DTIN Maximum Load Capacitance	1000 pF. This signal is true when input data is gated onto the computer E-bus.

### DIGITAL CONTROL OUTPUTS

Number	Eight.
Type	TI SN7545IP Dual Peripheral Driver; sinks current when true. Each output will sink 300 mA and standsoff +30 V. Each EXC sets an R-S type flip-flop, which results in a dc logic low true output. Each flip-flop has an

## DIGITAL CONTROL OUTPUTS (Continued)

Type externally available reset input, 1 logic load, with 5.6 K ohms (1 K ohms, optional) to +5 Vdc. Reset input may be grounded for pulse operation or may be connected to an EXC for computer control of reset.

## DIGITAL SENSE INPUTS

Number Eight.

Type TTL logic levels. Ground true, open circuit inputs are held to +5V supply through 5.6 K ohm resistors (1 K ohm, optional).

## SPARE GATES

Number Two.

Type NOR gates are provided to accommodate special additional logic requirements.

POWER +5 Vdc  $\pm$  1%, 1A.

## TEMPERATURE RANGE

Operating -10 °C to 50 °C

Storage -55 °C to 85 °C

## PHYSICAL CHARACTERISTICS

Dimensions One printed circuit board 7-3/4 x 12 x 1/2 inches.

Connectors One 122-terminal card edge connector.  
Two 44-terminal card edge connectors.

APPENDIX C: DRIVER PROGRAM EXAMPLES

PAGE 1 DASG 05/07/73

		1 *	TEST DOM = PROGRAM CONTROL INPUT AND OUTPUT	
001000		2	ORG 01000	
	004012	3 PDOM	EQU 04012	
		4 *		
		5 *		
		6 *		
001000	002000	7 PDR0	CALL PDOM,DOMNR,OUT,NUM,OBUF,ERROR	
001001	004012			
001002	001030			R
001003	001031			R
001004	001033			R
001005	001200			R
001006	001025			R
001007	002000	8	CALL PDOM,DOMNR,IN,NUM,IBUF,ERROR	
001010	004012			
001011	001030			R
001012	001032			R
001013	001033			R
001014	001034			R
001015	001025			R
001016	001100	9	JSS1 **4	
001017	001022			R
001020	001000	10	JMP PDR0	
001021	001000			R
001022	000001	11	HLT 01	
001023	001000	12	JMP PDR0	
001024	001000			R
001025	000077	13 ERROR	HLT 077	
001026	001000	14	JMP PDR0	
001027	001000			R
001030	000011	15 DOMNR	DATA 9	DOM SELECT CODE
001031	000000	16 OUT	DATA 0	
001032	000001	17 IN	DATA 1	
001033	000001	18 NUM	DATA 1	NUMBER OF WORDS
001034		19 IBUF	BSS 100	INPUT BUFFER
001200		20 OBUF	BSS 100	OUTPUT BUFFER
	000000	21	END	

		1 *	TEST DOM - DIRECT ACCESS CONTROL (BIC) MODE	
		2 *		
002000		3	ORG	02000
	004144	4	DDOM	EQU 04144
	004367	5	SDOM	FQU 04367
002000	002000	6	DDRD	CALL DDOM,BICNR,DOMNR,OUT,NUM,IBUF,ERROR
002001	004144			
002002	002036	R		
002003	002037	R		
002004	002040	R		
002005	002042	R		
002006	002207	R		
002007	002033	R		
002010	002000	7	CALL	BICW GO WAIT BIC COMPLETE
002011	002353	R		
002012	002000	8	CALL	DDOM,BICNR,DOMNR,IN,NUM,IBUF,ERROR
002013	004144			
002014	002036	R		
002015	002037	R		
002016	002041	R		
002017	002042	R		
002020	002043	R		
002021	002033	R		
002022	002000	9	CALL	BICW
002023	002353	R		
002024	001100	10	JSS1	#+4
002025	002030	R		
002026	001000	11	JMP	DDRD
002027	002000	R		
002030	000003	12	HLT	3 HALT AFTER INPUT = OUTPUT
002031	001000	13	JMP	DDRD
002032	002000	R		
002033	000001	14	ERROR	HLT 1
002034	001000	15	JMP	DDRD
002035	002000	R		
002036	000001	16	BICNR	DATA 1
002037	000011	17	DOMNR	DATA 9 #051 SELECT
002040	000000	18	OUT	DATA 0
002041	000001	19	IN	DATA 1
002042	000001	20	NUM	DATA 1 NUMBER OF WORDS TRANSFERED
002043		21	IBUF	BSS 100 INPUT BUFFER
002207		22	OBUF	BSS 100 OUTPUT BUFFER
		23 *		

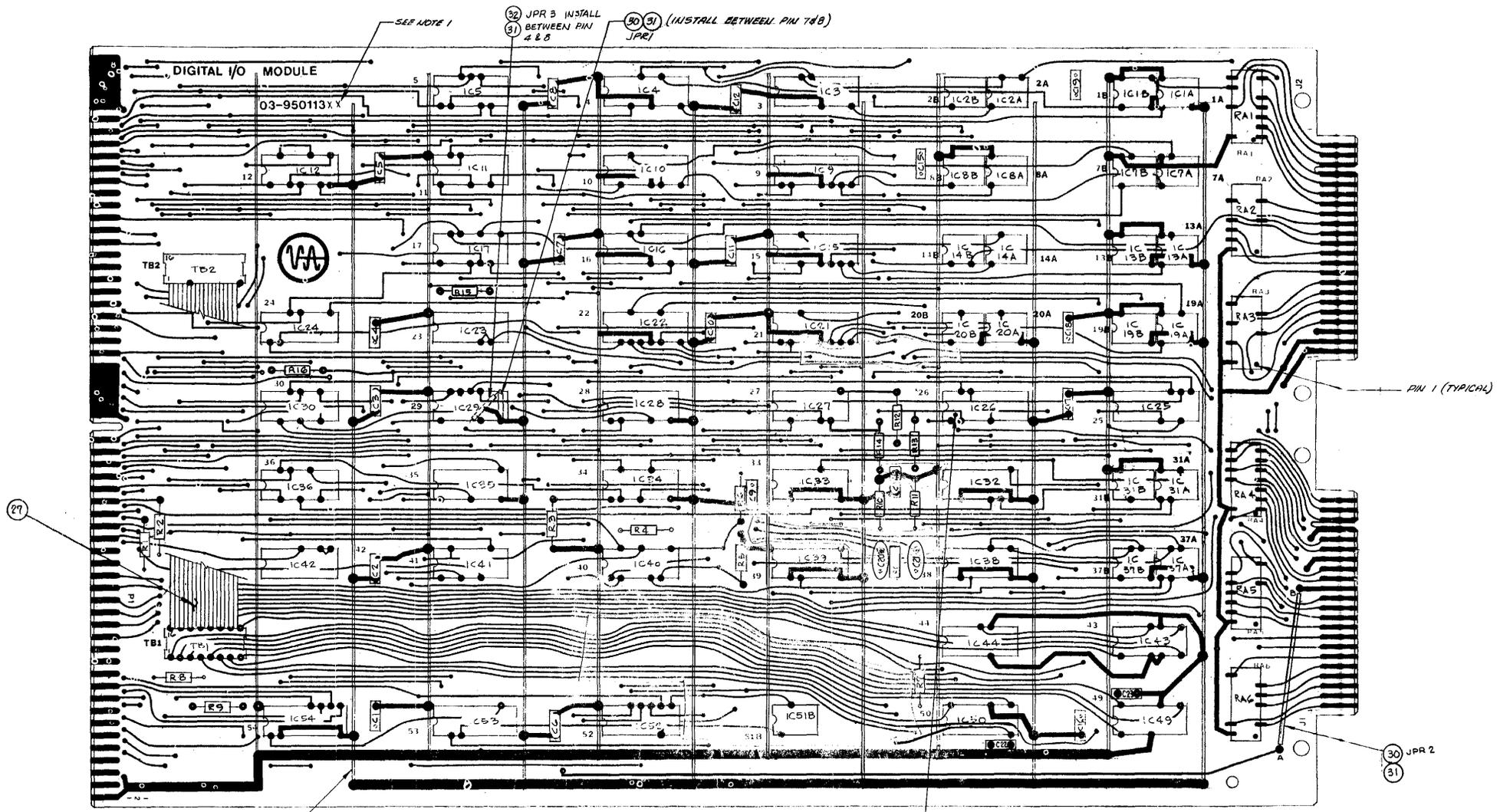
		24 *	BICW	BIC WAIT SUBROUTINE
		25 *		
002353	000000	26 BICW	ENTR	0
002354	002000	27	CALL	SDOM,BICS GO WAIT BIC COMPLETE
002355	004367			
002356	002376 R			
002357	012376	28	LDA	BICS
002360	001010	29	JAZ	BICW+1 BIC STILL BUSY
002361	002354 R			
002362	004341	30	LSRA	1
002363	001010	31	JAZ	**4
002364	002367 R			
002365	001000	32	JMP	ERROR BIC ABNORMAL STOP
002366	002033 R			
002367	001200	33	JSS2	**4
002370	002373 R			
002371	001000	34	JMP*	BICW
002372	102353 R			
002373	000002	35	HLT	2 CONDITIONAL HALT
002374	001000	36	JMP	DDRO RESTART
002375	002000 R			
002376	000000	37 BICS	DATA	0
	000000	38	END	



APPENDIX D: SCHEMATICS, ASSEMBLIES, AND PARTS LISTS

Digital I/O Module

03-950111



SEE NOTE 1

32 JPR 3 INSTALL BETWEEN PIN 4 & 8

30 31 (INSTALL BETWEEN PIN 7 & 8) JPR 1

PIN 1 (TYPICAL)

27

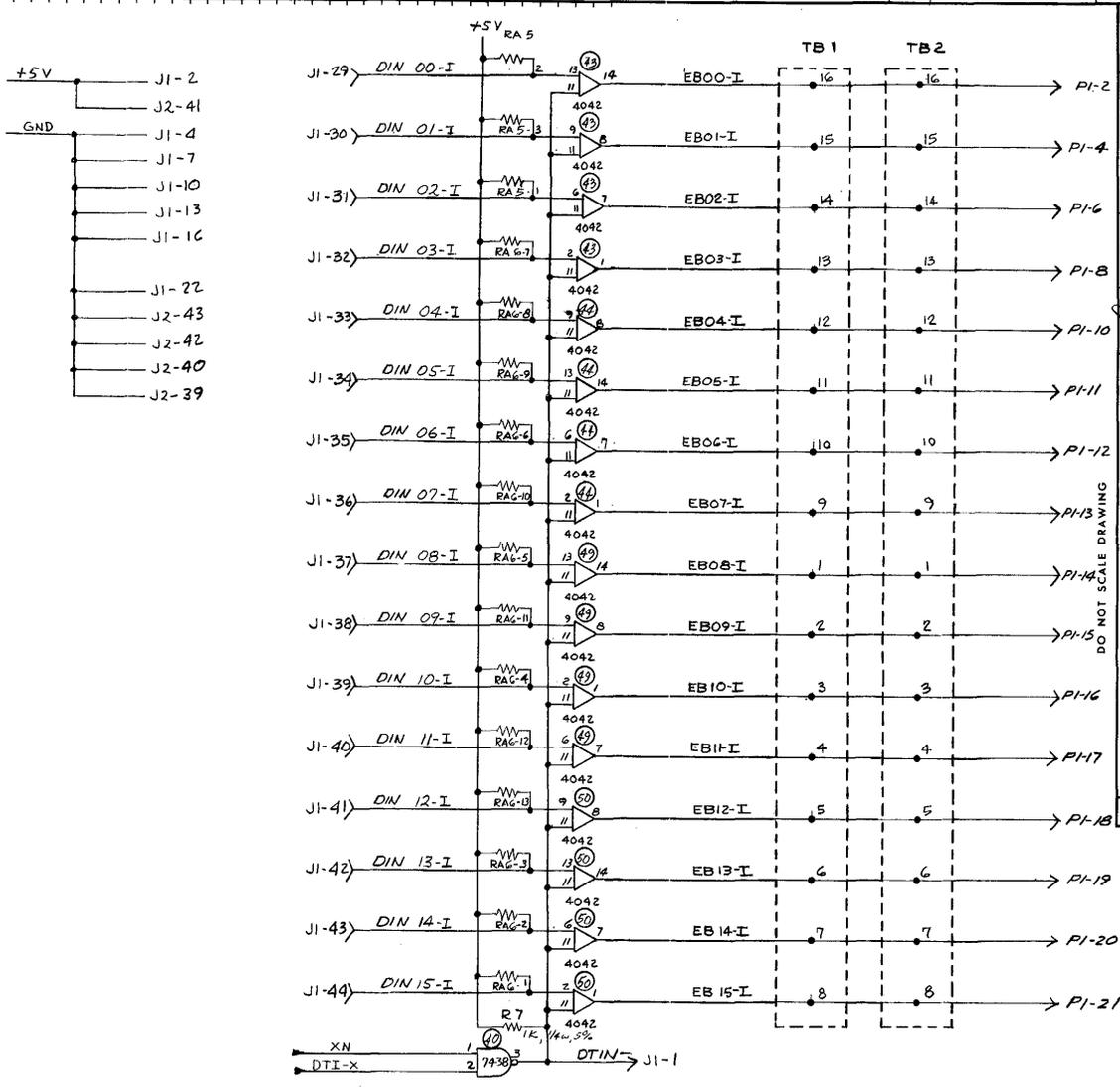
30 JPR 2  
31

FOE-03 ONLY, POSITION PIN 1 OF ITEM 5, RESISTOR ARRAY, AT PIN 1 OF ELEMENT SLOT



Digital I/O Module Assembly, 03-950113

<u>Schematic Reference</u>	<u>Description</u>	<u>Varian Part No.</u>
RA1-RA6, RA4-RA6 RA1-RA3, 5, 6, & IC26	Resistor, Array, 5.6K	03-998011
IC1A, IB, 2A, 2B, 7A, 8A, 8B, 13A, 13B, 14A, 14B, 19A, 19B, 20A, 20B, 31A, 31B, 37A, 37B, 51B	IC Element 75451	62-600260
IC3, 4, 9, 10, 15, 16, 21, 22, 53	IC Element 7475N	62-600351
IC30, 40, 27, 28	IC Element 7438	62-600294
IC25	IC Element 74151	62-600270
IC26, IC54	IC Element 9301	62-600400
IC29, 32, 33, 35, 38, 39	IC Element 7474	62-600365
IC11, 23, 34, 36, 41, 42	IC Element 7402	62-600356
IC24	IC Element 7430	62-600359
IC5, 12, 17	IC Element 7404	62-600013
IC52	IC Element 7400	62-600355
IC43, 44, 49, 50	IC Element 4042	62-600316



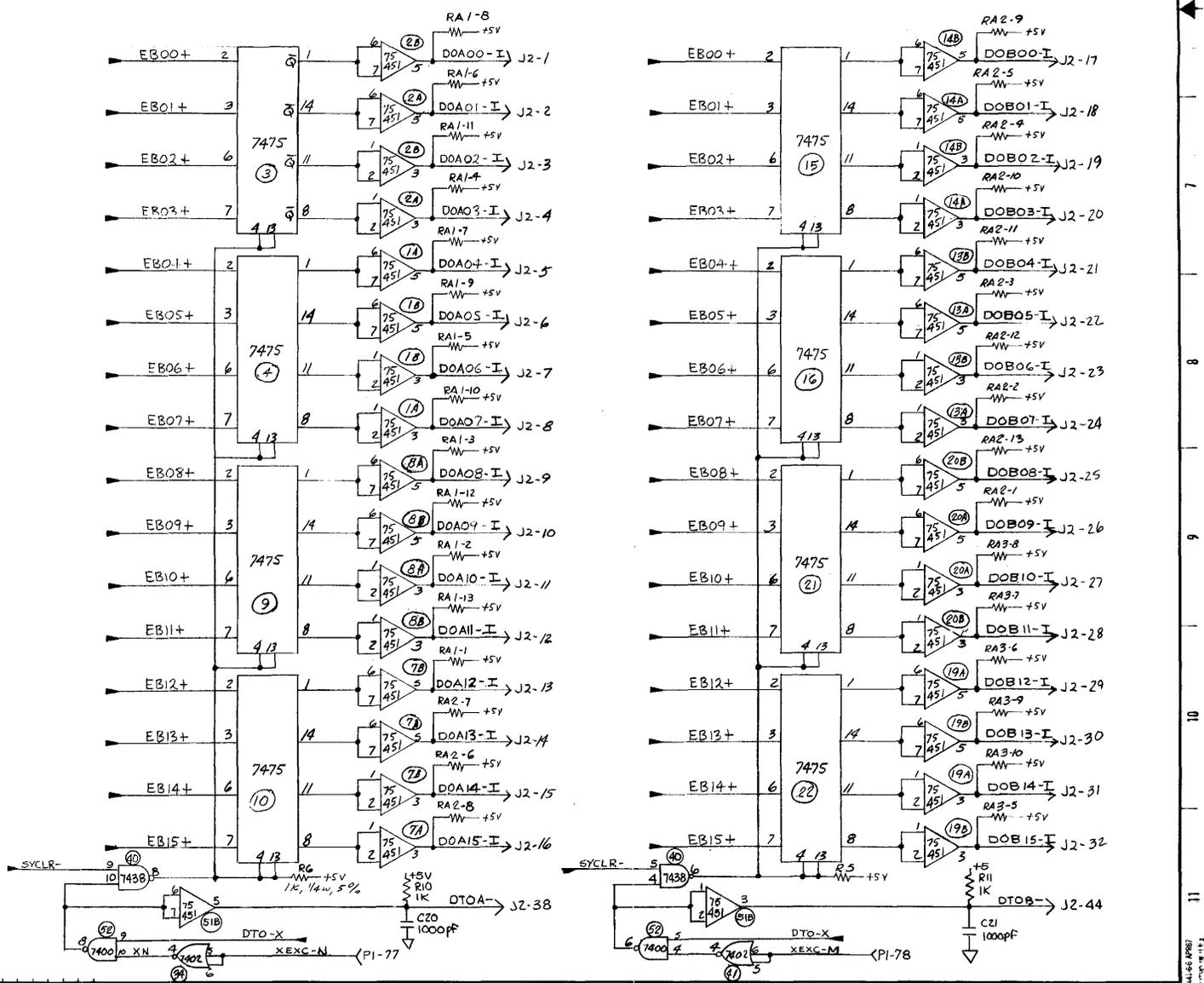
DATE	APPROVED	DATE	CLASS
2/14/71	[Signature]	6-15-71	A
2/14/71	[Signature]	6-15-71	A

DIGITAL I/O

DO NOT SCALE DRAWING

SEE SHEET 1

NO.	DESCRIPTION	DATE
1	SMT 2 of 2	



DESCRIPTION OF MATERIAL

PART NUMBER

NO.

D 03-950111

1

2

4

5

7

8

9

10

11

WEST ASSEMBLY

44-66 (P85)

FORM 125A