

USER'S GUIDE
DIGITAL INPUT MODULE
for use with
Varian 620 or V73 Series Computers

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1. INTRODUCTION

1.1 GENERAL

The Digital Input Module (DIM) is a hardware option which provides digital inputs to Varian 620 and V73 series computers. The module can be configured in either a mixed analog and digital system or a digital-only system.

The DIM is not a freestanding module; it requires various control functions from other modules. In a digital-only system, the DIM is supplied with abridged versions of the Varian Analog-to-Digital Converter (ADC) and Multiplexer (MUX) modules, which provide the necessary control logic. In a mixed analog and digital system, the DIM utilizes the control functions of standard ADC and MUX modules. An existing analog input system can be easily expanded, therefore, to accommodate both analog and digital inputs.

For details regarding the control functions supplied by the ADC and MUX modules, refer to the ADCM User's Guide (Publication No. 03-996 806) and High-Level Multiplexer User's Guide (Publication No. 03-996 807).

Each DIM provides four 16-bit digital input registers. Expansion to as many as 256 input registers is possible, since up to 64 DIMs can utilize a single pair of control cards.

Simple installation procedures allow the DIM to be installed either at the factory or on-site at the user's facility. A comprehensive software test package is provided with the DIM for post-installation checkout of its operational status. In addition, the module is fully supported by standard Varian software and input/output options.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 illustrates the functional elements included in a complete digital input system. These elements are packaged on three plug-in printed circuit boards. Those elements contained on the ADC control card are shown in the dotted portion of the figure; the elements contained on the MUX control card are shown in the diagonally striped portion of the figure; the unshaded area of the figure represents the elements contained on a DIM card.

Device Address

Each DIM requires two device addresses, which are set when the module is installed. The device addresses are used by the computer to select a particular DIM for operation. The addresses are actually assigned to the ADC and MUX cards which control the DIM and through which the DIM is accessed. Typically, the ADC is assigned device address 60 octal, and the MUX is assigned address 61 octal. The MUX contains the device address decode logic.

Channel Selection

DIM channels can be selected in either sequential or random mode via the MUX control card. The mode of channel selection is specified by the computer program using a standard assembly language instruction. In sequential mode, the channel address decode logic on the MUX control card automatically increments from channel address 1 to the final address prescribed by the program. In random mode, the DIM channel address is specified by the program. This mode permits the selection of DIM channels in any sequence.

End-Of-Scan Sense

The program can determine when a sequential channel selection operation is complete by issuing a Sense instruction that selects the End-of-Scan Sense input line

on the MUX control card. This line is logically true when the channel address decode logic selects the final channel address in a sequential operation.

Data Transfer

An internally-generated strobe signal automatically transfers data from the external source to a DIM storage register at 20-microsecond intervals. Optionally, the DIM can be wired to accept an external strobe from the data source.

Data transfers from DIM storage registers to the computer can be performed under program control or under control of the optional Buffer Interlace Controller (BIC). When operating under program control, data transfers are initiated by the computer and are executed under input instruction control. When operating with a BIC, data transfers are initiated by the computer and executed without input instruction control. The BIC permits automatic, high or low speed, block data transfers from the DIM to computer memory without disturbing the sequence of the main program.

Programmable Timer

A programmable timer is contained on the ADC control card. The timer provides a train of pulses in which the interval between pulses is determined by a data word that is loaded into the timer by the computer program. An internal crystal-controlled oscillator provides the time base used by the timer; there is also a provision for an external signal to be used as the time base. With the standard internal oscillator, the timer pulse can be varied between 1 microsecond and 65 milliseconds with a resolution of 1 microsecond. The programmable timer can be especially useful in setting the rate of sampling of input channels.

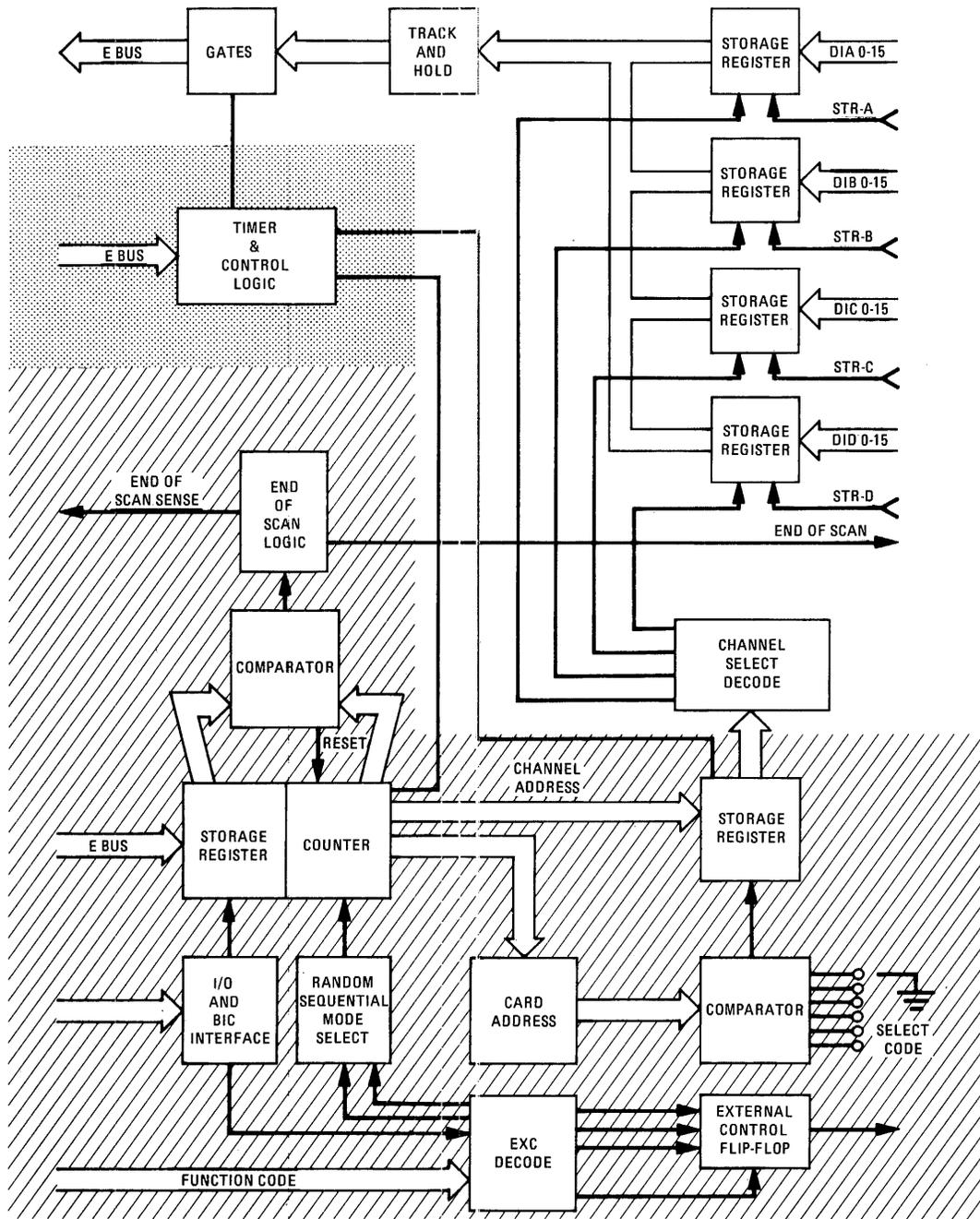


Figure 1-1. Digital Input System Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the DIM and presents instructions for using the software test package for module checkout. More detailed programming information may be found in the 620 series and V73 system handbooks.

A program is able to direct DIM operation in the following ways:

- Sets mode of channel selection.
- Outputs channel select codes.
- Tests for end-of-scan in sequential mode.
- Transfers data from digital input registers.
- Sets interval for programmable timer.
- Enables operation under BIC control.

Note that these programmed features deal primarily with the ADC and MUX modules which provide control functions for the DIM. Further information regarding these programmed functions is given in the User's Guides for the ADC and MUX modules. Also the ADC driver programs, which are described in the ADC User's Guide, may be used with the DIM.

Table 2-1 provides a summary of the basic assembly language instruction set used with the DIM.

Table 2-1. DIM Assembly Language Instruction Set

Instruction	Description
EXC 00YY	Connects MUX control module to BIC.
EXC 01YY	Selects Random Scan Mode.
EXC 02YY	Selects Sequential Scan Mode.
SEN 00YY	Senses End of Sequential Scan.
OAR 0YY	Outputs channel select code from the A register.
OBR 0YY	Outputs channel select code from the B register.
OME 0YY	Outputs channel select code from memory.
EXC 00XX	Connects ADC control module to BIC.
EXC 01XX	Starts data input under program control.
EXC 02XX	Enables DIM for start from external pulse or timer pulse.
EXC 03XX	Disables external pulses when starting the DIM under program control.
SEN 00XX	Senses DIM Data Ready.
SEN 01XX	Senses timer interval pulse.
SEN 02XX	Utility sense input. Can be used to sense external start.
OAR 0XX	Outputs timer interval word from register A.
OBR 0XX	Outputs timer interval word from register B.
OME 0XX	Outputs timer interval word from memory.
CIA 0XX	Clears A register and inputs DIM data to A.
CIB 0XX	Clears B register and inputs DIM data to B.
INA 0XX	Inputs DIM data to A register.
INB 0XX	Inputs DIM data to B register.
IME 0XX	Inputs DIM data to memory.
<p>Note: YY is the device address for the MUX control module. XX is the device address for the ADC control module.</p>	

2.2 CHANNEL SELECTION MODE

A program specifies the mode of channel selection with an EXC instruction. Sequential channel selection is specified with an EXC 02YY instruction, where YY is the device address of the MUX control card. Random channel selection is specified with an EXC 01YY instruction.

2.3 CHANNEL SELECT CODE TRANSFER

A program specifies the DIM input channel which is to be selected by means of an eight-bit channel select code. (Channels are numbered from 1 to 256.) This code may be transferred from the computer's A or B register or from memory to the MUX control card by means of a standard data-transfer-out operation. Transfer of the channel select code is accomplished with one of the following instructions:

OAR	0YY	Load device YY from A register
OBR	0YY	Load device YY from B register
OME	0YY	Load device YY from memory

where YY is the device address of the MUX control card.

In sequential mode, only the channel select code for the final channel address is sent to the MUX; all select codes from channel address 1 to the final address are generated automatically once the sequence has begun.

In random mode, each selection of a channel requires a separate data-transfer-out of the appropriate channel select code. The data transfer operation may be under program control or BIC control.

2.4 END-OF-SCAN SENSE

The program can test the status of a sequential channel selection to determine if the final channel has been selected (end-of-scan). It does this by executing SEN 0YY,

where YY is the device address of the MUX control card. A true level on the computer's sense input line, SERX-I, indicates that the DIM has completed its scan. If the computer does not intervene, the DIM will return to channel 1 and continue its scanning sequence.

2.5 BIC ENABLE

The BIC option can be used either to output a block of random channel addresses from memory to the DIM or to input a block of sequential or single-channel readings from the DIM to memory. If it is desirable to perform both of these operations under BIC control, two BICs are required.

The MUX control card is used to output random channel addresses via the BIC. In this case, the program enables the MUX to operate under BIC control by an EXC 0YY instruction, where YY is the MUX control card's device address. This sets the MUX to random mode and establishes the connection to the BIC so that random channel addresses may be passed to the MUX from memory via the BIC.

The ADC control card is used with the BIC to input a block of DIM readings from sequential channels. In this case, an EXC 0XX instruction is used to connect the DIM to the BIC; XX is the device address of the ADC control card.

2.6 TIMER INTERVAL PROGRAMMING

The timer on the ADC control card may be programmed to provide a single pulse after a predefined delay or a train of pulses at a predefined frequency. This is accomplished by outputting the desired pulse interval value to the timer register.

The defined value for the pulse interval is transmitted from the computer to the timer register as a 16-bit number (less than or equal to 65535_{10}). The timer decrements this number at the rate of one count per microsecond and issues an output pulse when the count reaches zero. In continuous mode, the timer auto-

matically reloads to the value in the buffer register and begins a new cycle. In single cycle mode, the next cycle must be initiated by an external signal. The timer mode is prewired to user specifications, but may be changed after installation.

The pulse interval may be loaded into the timer buffer register either directly from memory or via the computer's input/output registers. One of three statements is used to load the timer buffer register:

OAR	0XX	Output value from A Register to buffer register
OBR	0XX	Output value from B Register to buffer register
OME	0XX	Output value from memory to buffer register

where XX is the ADC control card's device address.

The status of the timer can be sensed by issuing a SEN 01XX instruction. A true sense response on Sense line 1 indicates that the timer has decremented to zero; a false level indicates that it has not. The timer continues operation whether or not the sense line is sampled. The line is automatically reset to false as soon as it has been sensed true.

2.7 DATA TRANSFER

Data is transferred from the DIM input registers to the computer using any of the standard input instructions INA, INB, CIA, CIB, or IME. Data is read from ADC device address (0XX). Note that in a combined analog and digital system, all data is received from the ADC device address.

2.8 PROGRAMMING EXAMPLES

The following examples illustrate typical sequences of program instructions which may be used to direct DIM operation. The examples assume device address 60 octal

for the ADC control card and device address 61 octal for the MUX control card.

Example 1 - Random Selection Under Program Control

In this example, a set of random channel numbers is used to select DIM channels. The channel numbers are transferred from an array in memory, and the resulting input values from the selected channels are stored in another array in memory. Note that a Sense instruction is used to check for data ready before reading each input channel. This is necessary since the hardware requires approximately 20 microseconds to advance to a new random channel, and this delay is not provided by the program code.

	LDB	INPT	Load First Word Address of Input Data Array.
	LDX	CHAN	Load First Word Address Channel Number Array.
	EXC	0360	Lock Out External Start on DIM.
	EXC	0161	Select Random Mode.
	CIA	060	Clear Data Ready Flag.
RAN1	LDA	0,1	Load First Channel Number.
	OAR	061	Output Channel Number to DIM.
	EXC	0160	Request Input.
LOOP	SEN	060,READ	Check if Data Ready.
	NOP		
	JMP	LOOP	Not Ready.
READ	CIA	060	Read Input Data.
	STA	0,2	Store Data in Array.
	IBR		} Check If All Values Have Been Read.
	IXR		
	TXA		
	SUB	WRDS	
	SUB	CHAN	

	JAN	RAN1	
	HLT		
CHAN	DATA	<u>xxx</u>	First Word Address of Channel Number Array.
INPT	DATA	<u>xxx</u>	First Word Address of Input Data Array.
WRDS	DATA	<u>xxx</u>	Number of Data Words.

Example 2 - Sequential Selection Under Program Control

In this example, DIM input channels are selected sequentially from channel 1 to the channel number specified by the program. The input values are stored in an array in memory, and the scan is terminated when the desired number of values have been read.

	LDX	INPT	Load First Word Address of Input Array.
	EXC	0360	Lock Out External Starts.
	EXC	0261	Select Sequential Mode.
	CIA	060	Clear Data Ready Flag.
	LDA	LAST	Load Last Channel Number.
	OAR	061	Output Last Channel Number.
SEQ1	EXC	0160	Request Input from Channel.
LOOP	SEN	060, READ	Check if Data Ready.
	NOP		
	JMP	LOOP	Not Ready.
READ	CIA	060	Read Input Data.
	STA	0, 1	Store Data in Array.
	IXR		} Check If All Values Have Been Read.
	TXA		
	SUB	WRDS	
	SUB	INPT	
	JAN	SEQ1	

	HLT		
INPT	DATA	<u>xxx</u>	First Word Address Of Input Data Array.
WRDS	DATA	<u>xxx</u>	Number of Data Words.
LAST	DATA	<u>xxx</u>	Last Channel Number.

2.9 DIM TEST PROGRAMS

A set of test programs is provided for checkout of the DIM and its ADC and MUX control cards. Four of these programs, which test the ADC and MUX control cards, are described in the ADC User's Guide. These test programs are numbered 1, 2, 3, and 6. An additional test program, number 7, is designed specifically for DIM checkout. Test 7 is described in this manual.

Program loading and selection procedures, as well as sense switch conventions, are described in the ADC User's Guide.

Test 7 -- Digital Input Test

This test is designed to check out one DIM card in both random and sequential modes. The test requires the installation of a special test shoe, which can be purchased from Varian (Part No. 03-950329). The test shoe provides a known 16-bit word as input to two of the DIM registers, while the other two registers not currently on the test shoe will be unaffected and will read the last strobed-in value. A three-position toggle switch on test shoe gives the ones complement of the output to each of the two registers as shown in Table 2-2.

Table 2-2. DIM Test Shoe Output

Channel Number	J1			J2		
	Switch Setting			Switch Setting		
	A	Off	B	A	Off	B
1 + 4n	N/A	N/A	N/A	0114631	N/A	0063146
2 + 4n	N/A	N/A	N/A	0063146	N/A	0114631
3 + 4n	0114631	0	0063146	N/A	0	N/A
4 + 4n	0063146	0	0114631	N/A	0	N/A

Where, n = integer 0 to 63

The test exercises each column in the table in both sequential and random modes.

After the test is selected, the program prints:

```
DIM TEST
ENTER CHANNEL NO?
```

In response to this message, the user should enter the first channel number of the DIM card being tested. The channel number must be the value $(1 + 4n)$ where n is an integer from 0 to 63; otherwise, the program will request the number again.

After the channel has been selected, the test program issues a series of requests to place the test shoe on J1 and J2 and to set the test shoe switch to position A or B. After complying with each request, the user types a period to initiate the test.

Note that it is important to set the test shoe toggle switch to OFF prior to removing the test shoe from J1 or J2. This causes the associated registers to be cleared.

The program checks the sequential mode of operation by reading all channels sequentially, beginning with channel number 1. The program first checks all channels

except the block of four for which the test has been requested to insure that neither test pattern is present on any channel. If either of these readings is found, the program prints the channel number and reading.

The program then checks the block of four channels requested by the user. Each is read and the input data is checked according the appropriate column of Table 2-2. If any error is detected, all four channel numbers and readings are printed.

After the sequential test, the program checks the random mode of operation. In this check, the four channels of interest are read and compared against the appropriate column of the table. If any error is detected, all four channel numbers and readings are printed.

If no errors are found in either the sequential or random check, "OK" is printed, and the test is repeated for the next column in the table. All four A/B columns of the table are tested in sequence and then control is returned to the test selection statement.

If sense switch 2 is set, the test will loop on the same column after a period is entered following the test shoe connection request.

3. THEORY OF OPERATION

3.1 GENERAL SYSTEM DESCRIPTION

The Digital Input Module operates in close conjunction with the ADC module. From the computer's standpoint, multiplexer channels are selected and 16-bit data words are acquired with no distinction as to whether a given channel contains analog or digital raw data.

If the DIM determines that one of its own channels is selected when a data input sequence begins at the ADC device address, it prevents the ADC from gating data to the E-bus and substitutes its own 16-bit data word to the E-bus. Therefore, if CDS is true (H) at device 29 pin 4, when ENABLE goes true (L → H) it clocks flip-flop 29 pin 5 (L) which forces ENABLE false (L) at P1 pin 83. ENABLE must be true (H) for ADC data to be gated to the E-bus. A zero level (L) at pin 11 of devices 6, 12, 18, and 24 gates the 16-bit data word of the selected DIM channel to the E-bus.

The CARD SELECT logic designed to compare the 6-bit code composed of signals C, D, E, F, G, and H (defined as "variable") with the 6-bit code composed of signals CL-C, CL-D, CL-E, CL-F, CL-G, and CL-H (defined as "fixed").

CARD SELECT is true (1) if either A or B is true and the variable code is the same as the fixed code, or (2) if both A and B are false and the variable code is one count greater than the fixed code.

When the Multiplexer module is operated in sequential mode, the "variable" channel address code changes each time the ADC BUSY signal goes true. In analog systems the signal information of the previous channel is retained for the ADC by the sample and hold circuit. Similarly, the DIM holds the A, B, and CARD SELECT signals with device 4 (see schematic 03-950354).

The DIM also contains a storage register (devices 5, 11, 17, and 23) which holds the 16-bit data word steady and uncharged while the data is gated to the computer E-bus. For example, if CP1 should occur just prior to DTIS, the TRACK signal would remain true and the computer would receive the 16-bits entered by that CP1 (L→H) transition. If CP1 should occur during DTIS, the TRACK signal would have already been clocked false by the leading edge of DTIS and the computer would receive the 16-bits entered by the last CP1 that occurred just prior to DTIS.

3.2 INPUT MODULE DESCRIPTION

Each DIM register is composed of four identical input devices. This basic input device (see Figure 3-1) provides four D-type flip-flops which operate synchronously from a common clock.

A three-state output facilitates usage of the device in a bus-organized system. The outputs can be wired directly to outputs of other devices without encountering the problems normally met with "collector-ORing" TTL circuits. This is accomplished by gating the normally low impedance logical "1" or logical "0" output into a high impedance state.

The high impedance state occurs on all outputs of all devices except the four outputs of the device selected. The result is that the selected device has a normal TTL low impedance output providing good capacitive drive capability and waveform integrity, especially during the transition from a logical "0" to logical "1". The other outputs are all in the "third-state" and take only a small amount of leakage current from the driving outputs.

The following logic levels control the device:

- Clocking occurs on the positive-going transistion.
- Clearing is enabled by taking the input to a logical "1" level.
- Outputs are placed in the "third-state" if either of the two Output Disable inputs is taken to a logical "1" level.

- If either of the two Data Input Disable inputs is a logical "1" level, the flip-flops will remain in their previous state when clocked.

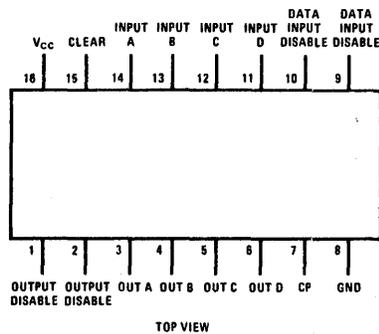
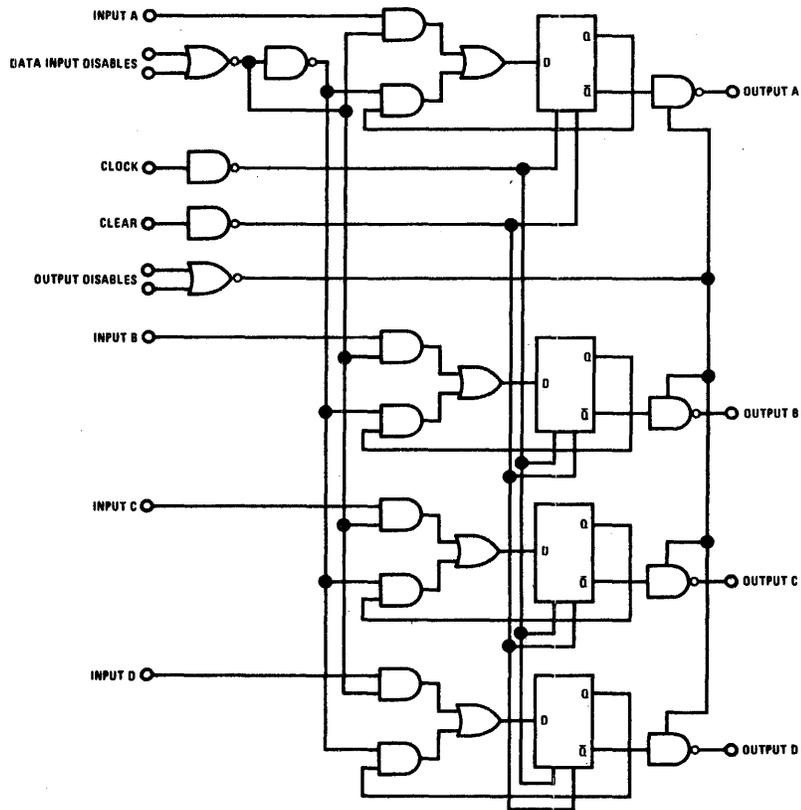


Figure 3-1. Input Device Functional Diagram

4. INSTALLATION

4.1 PREREQUISITES

Each DIM requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. The ADC and MUX control cards each require an additional card slot. No special slots are reserved for these cards, and their location in the frame is determined solely by considerations of convenience in backplane wiring.

For additional information on installation of the ADC and MUX cards, refer to the User's Guides for those modules.

4.2 INSTALLATION AND INTERCONNECTION

A DIM is installed vertically with its component side to the left in 620/i and 620/L computers, and horizontally with its component side up in the 620/f computer. The card is installed with the double pin edge pointing toward the installer.

Figure 4-1 illustrates a typical digital input installation, including a DIM with ADC and MUX control cards. Note that in a mixed analog and digital system, an analog power supply would also be required.

Connection to the computer I/O bus and the BIC option B-bus is provided through backplane wiring. Pin assignments for the I/O bus and B-bus are listed in the appendices of the ADC and MUX User's Guides.

Device Address Wiring

In a standard configuration, the DIM's ADC control card is assigned device address 60_8 and the MUX control card is assigned device address 61_8 . The jumper connections

for wiring these addresses are listed in Table 4-1.

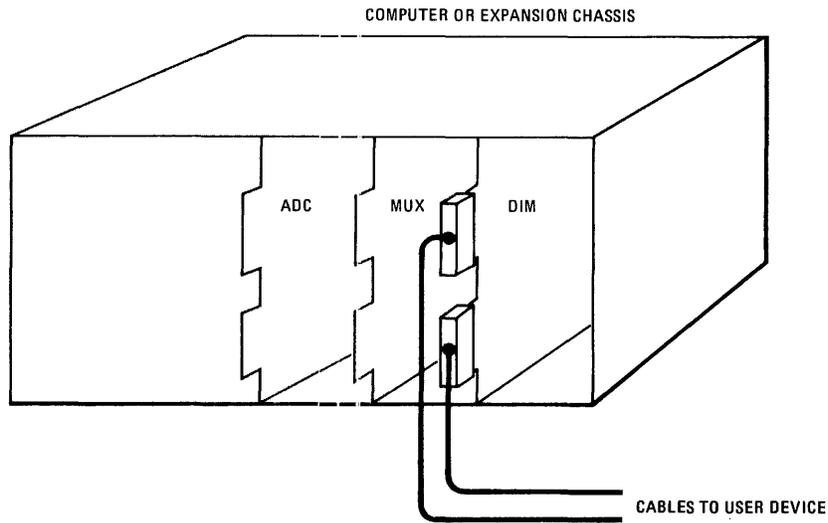


Figure 4-1. Typical Module Installation

Table 4-1. ADC And MUX Device Address Wiring

Signal Name	ADC to ADC		MUX to MUX	
EB-0	P1-65	P1-66		
EB-1	P1-68	P1-69		
EB-2	P1-71	P1-72		
EB-0			P1-64	P1-66
EB-1			P1-68	P1-69
EB-2			P1-71	P1-72
EB-3			P1-74	P1-75
EB-4			P1-76	P1-78

Card/Channel Selection Wiring

Tables 4-2 through 4-4 list the jumper connections required for preparing the MUX control card and DIM modules for card and channel selection.

Table 4-2 lists the daisy chain wirewrap connections for attaching multiple DIM cards to the MUX control card.

Table 4-2. Daisy Chain Wirewrap Connections for MUX And DIM Modules

Signal	MUX	to	DIM1	to	. . .	to	DIMn
Blanking	P1-42		P1-42		P1-42		P1-42
Chan Sel-A	P1-86		P1-86		P1-86		P1-86
Chan Sel-B	P1-85		P1-85		P1-85		P1-85
Chan Sel-C	P1-84		P1-84		P1-84		P1-84
Chan Sel-D	P1-102		P1-102		P1-102		P1-102
Card Sel-E	P1-104		P1-104		P1-104		P1-104
Card Sel-F	P1-105		P1-105		P1-105		P1-105
Card Sel-G	P1-90		P1-90		P1-90		P1-90
Card Sel-H*	P1-92		P1-92		P1-92		P1-92
*Card Sel-H must be inverted to operate modules with channel addresses above 128.							
Signal	(Any slot below chan 129)	to	(Any slot above chan 128)	to	(Any slot above chan 128)		
Card Sel-H	P1-92		P1-83		P1-83		
H-Inverted			P1-94 to P1-92		P1-94 to P1-92		

Table 4-3 lists the connections required for the ADC, MUX, and first DIM card to provide operation of channels 1 through 4.

Table 4-3. Jumper Connections for Channel Group 1-4

Signal	From ADC	To MUX	To DIM
ENABLE	P1-83		P1-83
DTIS	P1-89		P1-89
BUSY	P1-75	P1-101	P1-101
A		P1-86	P1-86
B		P1-85	P1-85
C		P1-84	P1-84
D		P1-102	P1-102
E		P1-104	P1-104
F		P1-105	P1-105
G		P1-90	P1-90
H		P1-92	P1-92
CL-F			P1-93
CL-E			P1-94
CL-D			P1-95
CL-C			P1-91
CL-H			P1-78
CL-G			P1-77

Table 4-4 lists the internal connections for wiring each DIM channel address group.

Table 4-4. Wirewrap Jumpers for DIM Channel Address Groups

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
5-8	x	x	x	x	x	
9-12	x	x	x	x		x
13-16	x	x	x	x		
17-20	x	x	x		x	x
21-24	x	x	x		x	
25-28	x	x	x			x
29-32	x	x	x			
33-36	x	x		x	x	x
37-40	x	x		x	x	
41-44	x	x		x		x
45-48	x	x		x		
49-52	x	x			x	x
53-56	x	x			x	
57-60	x	x				x
61-64	x	x				
65-68	x		x	x	x	x
69-72	x		x	x	x	
73-76	x		x	x		x
77-80	x		x	x		
81-84	x		x		x	x
85-88	x		x		x	
89-92	x		x			x
93-96	x		x			
97-100	x			x	x	x
101-104	x			x	x	
105-108	x			x		x
109-112	x			x		

X indicates ground connection

Table 4-4. (Continued)

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
113-116	x				x	x
117-120	x				x	
121-124	x					x
125-128	x					
129-132		x	x	x	x	x
133-136		x	x	x	x	
137-140		x	x	x		x
141-144		x	x	x		
145-148		x	x		x	x
149-152		x	x		x	
153-156		x	x			x
157-160		x	x			
161-164		x		x	x	x
165-168		x		x	x	
169-172		x		x		x
173-176		x		x		
177-180		x			x	x
181-184		x			x	
185-188		x				x
189-192		x				
193-196			x	x	x	x
197-200			x	x	x	
201-204			x	x		x
205-208			x	x		
209-212			x		x	x
213-216			x		x	

X indicates ground connection.

Table 4-4. (Continued)

Channel Group	P1-78 CL-H	P1-77 CL-G	P1-93 CL-F	P1-94 CL-E	P1-95 CL-D	P1-91 CL-C
217-220			x			x
221-224			x			
225-228				x	x	x
229-232				x	x	
233-236				x		x
237-240				x		
241-244					x	x
245-248					x	
249-252						x
253-256						

X indicates ground connection.

APPENDIX A: DIM PIN ASSIGNMENTS

Backplane Wiring

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1- 1	Digital Ground	
2	EB00-I	
3	Digital Ground	
4	EB01-I	
5	Digital Ground	
6	EB02-I	
7	Digital Ground	
8	EB03-I	
9	Digital Ground	
10	EB04-I	
11	EB05-I	
12	EB06-I	
13	EB07-I	
14	EB08-I	
15	EB09-I	
16	EB10-I	
17	EB11-I	
18	EB12-I	
19	EB13-I	
20	EB14-I	
21	EB15-I	
22	Digital Ground	
23	Not used	
24	Digital Ground	
25	Not used	
26	Digital Ground	
27	Not used	
28	Digital Ground	
29	Not used	
30	Digital Ground	
31	Not used	
32	Digital Ground	
33	Not used	
34	Digital Ground	
35	Not used	
36	Digital Ground	

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1-37	Not used	
38	Digital Ground	
39	Not used	
40	Digital Ground	
41	Not used	
42	Not used	
43	Not used	
44	Not used	
45	Not used	
46	Not used	
47	Not used	
48	Digital Ground	
49	Not used	
50	Not used	
51	Digital Ground	
52	Not used	
53	Digital Ground	
54	Not used	
55	Digital Ground	
56	Not used	
57	Digital Ground	
58	Not used	
59	Digital Ground	
60	Not used	
61	Not used	
62	Not used	
63	Not used	
64	Not used	
65	Not used	
66	Not used	
67	Not used	
68	Not used	
69	Not used	
70	Not used	
71	Not used	
72	Not used	
73	Not used	
74	Not used	
75	Not used	
76	Not used	
77	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1-78	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
79	Not used	
80	Not used	
81	Not used	
82	Not used	
83	Not used	
84	C	Jumper connection for wiring channel select code
85	B	Jumper connection for wiring channel select code
86	A	Jumper connection for wiring channel select code
87	Not used	
88	Not used	
89	Not used	
90	G	Jumper connection for wiring channel select code
91	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
92	H	Jumper connection for wiring channel select code
93	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
94	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
95	Ground Connect	Channel selection for group (N+1) through (N+4) (see Table 4-4)
96	Not used	
97	Not used	
98	Not used	
99	Not used	
100	Digital Ground	
101	Busy	Busy input from ADC Control Card
102	D	Jumper connection for wiring channel select code
103	Not used	
104	E	Jumper connection for wiring channel select code
105	F	Jumper connection for wiring channel select code
106	Not used	
107	Not used	
108	Not used	
109	Not used	
110	Not used	
111	Not used	
112	Not used	
113	Not used	
114	Not used	
115	Not used	

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
P1 -116	Not used	
117	Not used	
118	+5 V	
119	Not used	
120	Not used	
121	+5 V	
122	Digital Ground	

Terminal Edge Connector Wiring

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
J1-1	DIC-00	Input word Channel N+1, bit 1
2	DIC-01	Input word Channel N+1, bit 2
3	DIC-02	Input word Channel N+1, bit 3
4	DIC-03	Input word Channel N+1, bit 4
5	DIC-04	Input word Channel N+1, bit 5
6	DIC-05	Input word Channel N+1, bit 6
7	DIC-06	Input word Channel N+1, bit 7
8	DIC-07	Input word channel N+1, bit 8
9	DIC-08	Input word Channel N+1, bit 9
10	DIC-09	Input word Channel N+1, bit 10
11	DIC-10	Input word Channel N+1, bit 11
12	DIC-11	Input word Channel N+1, bit 12
13	DIC-12	Input word Channel N+1, bit 13
14	DIC-13	Input word Channel N+1, bit 14
15	DIC-14	Input word Channel N+1, bit 15
16	DIC-15	Input word Channel N+1, bit 16
17	DID-00	Input word Channel N+2, bit 1
18	DID-01	Input word Channel N+2, bit 2
19	DID-02	Input word Channel N+2, bit 3
20	DID-03	Input word Channel N+2, bit 4
21	DID-04	Input word Channel N+2, bit 5
22	DID-05	Input word Channel N+2, bit 6
23	DID-06	Input word Channel N+2, bit 7
24	DID-07	Input word Channel N+2, bit 8
25	DID-08	Input word Channel N+2, bit 9
26	DID-09	Input word Channel N+2, bit 10
27	DID-10	Input word Channel N+2, bit 11
28	DID-11	Input word Channel N+2, bit 12
29	DID-12	Input word Channel N+2, bit 13

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
J 1-30	DID-13	Input word Channel N+2, bit 14
31	DID-14	Input word Channel N+2, bit 15
32	DID-15	Input word Channel N+2, bit 16
33	Digital Ground	
34	Digital Ground	
35	Digital Ground	
36	Digital Ground	
37	Digital Ground	
38	STR-C	External strobe for Channel N+1 (or Ground Connect)
39	Digital Ground	
40	Digital Ground	
41	Digital Ground	
42	Digital Ground	
43	Digital Ground	
44	STR-D	External strobe for Channel N+2 (or Ground Connect)
J 2-1	DIA-00	Input word Channel N+3, bit 1
2	DIA-01	Input word Channel N+3, bit 2
3	DIA-02	Input word Channel N+3, bit 3
4	DIA-03	Input word Channel N+3, bit 4
5	DIA-04	Input word Channel N+3, bit 5
6	DIA-05	Input word Channel N+3, bit 6
7	DIA-06	Input word Channel N+3, bit 7
8	DIA-07	Input word Channel N+3, bit 8
9	DIA-08	Input word Channel N+3, bit 9
10	DIA-09	Input word Channel N+3, bit 10
11	DIA-10	Input word Channel N+3, bit 11
12	DIA-11	Input word Channel N+3, bit 12
13	DIA-12	Input word Channel N+3, bit 13
14	DIA-13	Input word Channel N+3, bit 14
15	DIA-14	Input word Channel N+3, bit 15
16	DIA-15	Input word Channel N+3, bit 16
17	DIB-00	Input word Channel N+4, bit 1
18	DIB-01	Input word Channel N+4, bit 2
19	DIB-02	Input word Channel N+4, bit 3
20	DIB-03	Input word Channel N+4, bit 4
21	DIB-04	Input word Channel N+4, bit 5
22	DIB-05	Input word Channel N+4, bit 6
23	DIB-06	Input word Channel N+4, bit 7
24	DIB-07	Input word Channel N+4, bit 8
25	DIB-08	Input word Channel N+4, bit 9
26	DIB-09	Input word Channel N+4, bit 10

<u>Pin No.</u>	<u>Name</u>	<u>Function</u>
J2-27	DIB-10	Input word Channel N+4, bit 11
28	DIB-11	Input word Channel N+4, bit 12
29	DIB-12	Input word Channel N+4, bit 13
30	DIB-13	Input word Channel N+4, bit 14
31	DIB-14	Input word Channel N+4, bit 15
32	DIB-15	Input word Channel N+4, bit 16
33	Digital Ground	
34	Digital Ground	
35	Digital Ground	
36	Digital Ground	
37	Digital Ground	
38	STR-A	External strobe for Channel N+3 (or Ground Connect)
39	Digital Ground	
40	Digital Ground	
41	Digital Ground	
42	Digital Ground	
43	Digital Ground	
44	STR-B	External strobe for Channel N+4 (or Ground Connect)

APPENDIX B: SPECIFICATIONS

DIGITAL INPUTS

Number	Four 16-bit registers.
Type	Low true; 1 TTL logic load plus 5.6 K ohms to +5 Vdc. Logic "1" Input = 0.0 to +0.8 Volts. Logic "0" Input = +2.0 to +5.0 Volts. Input Data Setup Time ≥ 0 nsec before (H \rightarrow L) strobe. Input Data Hold Time ≥ 100 nsec after (H \rightarrow L) strobe.

STROBE INPUTS

Number	Four
Type	One logic load plus 5.6 K ohms to +5 Vdc. Data is clocked into one input storage register on the high to low transition of its strobe signal. Data remains fixed as long as the strobe signal is high. If the strobe remains low for more than 20 microseconds, new data is automatically clocked into the storage register at 20 microsecond intervals.

TEMPERATURE RANGE

Specification	0 $^{\circ}$	to	50 $^{\circ}$ C
Operating	-10 $^{\circ}$	to	70 $^{\circ}$ C
Storage	-55 $^{\circ}$	to	85 $^{\circ}$ C

PHYSICAL CHARACTERISTICS

Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches.
Connectors	Two 44-terminal card edge connectors. One 122-terminal card edge connector.

APPENDIX C: SCHEMATICS, ASSEMBLIES, PARTS LIST

Digital Input Module

03-950354

DIGITAL INPUT MODULE, 950356

<u>Schematic Reference</u>	<u>Description</u>	<u>Varian Part No.</u>
IC2, 4, 7, 8, 13, 14, 19, 20, 31, 32, 37, 38, 43, 44, 49, 50	IC Element 8551	62-600 317
IC6, 12, 18, 24	IC Element 4042	62-600 316
IC9, 33, 36	IC Element 7402	62-600 356
IC10A, 10B, 16A, 16B, 25A, 25B	IC Element 75451	62-600 260
IC3	IC Element 9301	62-600 400
IC29	IC Element 7474	62-600 365
IC 5, 11, 17, 23	IC Element 7475	62-600 343
IC21, 27, 28	IC Element 936	62-600 309
IC15, 22, 35	IC Element 946	62-600 303
IC47, 48	IC Element 8200	62-600 347
IC42	IC Element 7486	62-600 366
IC41	IC Element 7483	62-600 373
IC46	IC Element 930	62-600 308
C1-C18	Capacitor, Ceramic - .01 μ f	41-228 004
C19-C22	Capacitor, Mica - 180 pf	41-159 568
RA1-RA6, RA30, 34	Resistor Array - 5.6 K	03-998 011

