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CHK	WHD	12/2/71
DSGN		
ENGR	<i>[Signature]</i>	11/22/71
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APPD	<i>[Signature]</i>	1/6/72



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TITLE  
 ENGINEERING DESCRIPTION  
 620-82  
 UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER  
 (UASC)

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## INDEX

	<u>PAGE</u>
<u>SECTION I - DESCRIPTION</u>	
1.1 Introduction	5
1.2 Functional Description	5
1.3 Logic Mnemonics List	12
 <u>SECTION II - INTERFACE AND CONNECTIONS</u>	
2.1 RS232 Option	14
2.2 Current Mode Option	14
2.3 Relay Option	15
2.4 DTL/TTL	15
2.5 Device Address and PIM Drivers	19
 <u>SECTION III - PROGRAMMING UASC</u>	
3.1 Instruction Set	20
3.2 Explanation of Instruction Set	21
3.3 Word/Character Format	22
 <u>SECTION IV - APPLICATION DATA</u>	
4.1 General Data	23
4.2 Cable Length Versus Rate of Operation	24
4.3 Version Selection	24
4.4 Assembly of Cable	26
4.5 Examples: Usage of RS232	29
4.6 Usage of Current Mode Model	32
4.7 Usage of Relay Version	35
 <u>SECTION V - TESTING</u>	
5.0 General	38
5.1 Test Routine	38
5.2 Test Connector	38



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CODE  
IDENT NO.  
**21101**

98A0767

C

SH 2 OF 53

REV

INDEX

SECTION VI - THEORY OF OPERATION

PAGE

6.0	General	40
6.1	Control Logic	40
6.2	Transmitter/Receiver Operation	42
6.3	Timing	46



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CODE  
IDENT NO.  
**21101**

98A0767

SH 2A OF 53 REV C

## INDEX

		<u>PAGE</u>
 <u>ILLUSTRATIONS</u>		
Figure 1.1	Functional Block Diagram	7
Figure 1.2	Baud Rate Selection Chart	6
Figure 1.3	Format Selection Chart	9
Figure 1.4	Asynchronous Format Examples	10
Figure 2.1	PIN Assignment Chart (Input/Output)	16
Figure 2.2	Device Address and PIM Connections	18
Figure 4.1	General Specification Chart	23
Figure 4.2	Cable Length Versus Baud Rate	24
Figure 6.1	Transmit Sequence Flow Chart	47
Figure 6.2	Receive Sequence Flow Chart	48
Figure 6.3	Transmitter - Block Diagram	49
Figure 6.4	Receiver - Block Diagram	50
Figure 6.5	Transmitter - Timing Diagram	51
Figure 6.6	Receiver - Timing Diagram	52
Figure 6.7	Oscillator/Counter - Timing Diagram	53



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CODE  
IDENT NO.  
**21101**

98A0767

SH 3 OF 53 REV C

# ENGINEERING DATA FORM

OPTION ----- Universal Asynchronous Serial Controller  
 MODEL ----- 620-82 (Formerly E2184)  
 NO. OF LOGIC CARDS REQ'D. ----- 1  
 NO. OF CARD SLOTS REQ'D. ----- 1  
 LOCATION OF SLOTS (NUMBERING) ----- Any I/O slot  
 CONNECTORS REQ'D. (EXCLUDING I/O) ----- 2- 44 pin burndy (supplied)  
 KEYING ----- NA  
 ST'D. DEVICE ADDRESS ----- 02 thru 07 (01 if for TTY) (Can be 00 thru 77)  
 WIRELIST NUMBER ----- PC board  
 MANUAL PUBLICATIONS NUMBER ----- 98A0767  
 PERIPHERAL EQUIPT. REQ'D ----- NA  
 MFG'R. ----- NA  
 MODEL ----- NA  
 GEN'L. SPECS ----- NA

**NOTES:**

RS232 version requires 100ma of +12V and -12V dc

Reference Documents:

Top Assembly	01A1259
Controller	<del>41D0567</del> 44D0677
Test Specification	98A0768
Test Prog. SPS	89A0228
Logic Diagrams	<del>91C0352</del> 91C0445
Test Routine	32A0107-010



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SHT 4 OF 53

## SECTION 1 DESCRIPTION

### 1.1 Introduction

The UASC (Universal Asynchronous Serial Controller) is a versatile character buffered serial controller which can operate in both half or full duplex modes. Four interfaces are available to the user: RS232, Current loop, relay and DTL/TTL. The DTL/TTL interface is always on the controller where as the RS232 or Current Mode or Relay interfaces are selected at time of purchase. The controller is not a data set controller but intended for use on direct connect interfaces.

The controller is capable of operating with one start bit and one or two stop bits, 5,6,7, or 8 bits of data, parity or no parity bit, and odd or even parity. Several operating frequencies from 9600 baud down to 45 baud are possible. All options and operating modes will be set up for the user by VDM, if all requirements are supplied at time of purchase. If the user does not specify the set up for the UASC, the RS232 version will be set up for 1200 baud with no parity, 8 bits of data and one stop bit. Also, the Current Mode version will be set up for 1200 baud with no parity, 8 bits of data and one stop bit. In addition, the relay version will be set up for 110 baud with no parity, 8 bits of data and two stop bits. Transmit and receive rates will always be equal. The user can easily modify the controller to his data transmission format by placing jumpers on the board as described in section 1.2.2.

### 1.2 Functional Description

Reference Block Diagram (Figure 1.1).

#### 1.2.1 Timing

Transmit and Receive clocking to the LSI transmitter/receiver circuit is derived from a 4.608 meg Hz crystal oscillator. A clock rate is derived by setting up the appropriate count in the 12 bit counter. The clock is set up to provide a clock rate 16 times the transmit/receive rate. See Figure 1.2.



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CODE  
IDENT NO.  
**21101**

98A0767

SH 5 OF 53 REV C

**FIGURE 1.2 - BAUD RATE SELECTION CHART**

Baud Rate	Div. By	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12
9600	15		X	X	X								
4800	30	X		X	X	X							
2400	60	X	X		X	X	X						
2000	72	X	X	X				X					
1800	80	X	X	X	X			X					
1200	120	X	X	X		X	X	X					
600	240	X	X	X	X		X	X	X				
300	480	X	X	X	X	X		X	X	X			
150	960	X	X	X	X	X	X		X	X	X		
110	1309			X	X	X				X		X	
75	1920	X	X	X	X	X	X	X		X	X	X	
45	3200	X	X	X	X	X	X	X				X	X

Note that jumper values are selected at one less than the desired divisor value. Other baud rates can be derived by the following formulas:

$$D = \left( \frac{CR}{2} \div 16 \right) \div BR - 1$$

or

$$(144,00) \div BR - 1$$

- D = Divisor
- CR = Clock or Oscillator Rate
- BR = Baud Rate desired

Note: Remainder should not exceed 1% of BR.

Jumpers E1 through E12 are placed on the controller (above the large chip) per the above chart.



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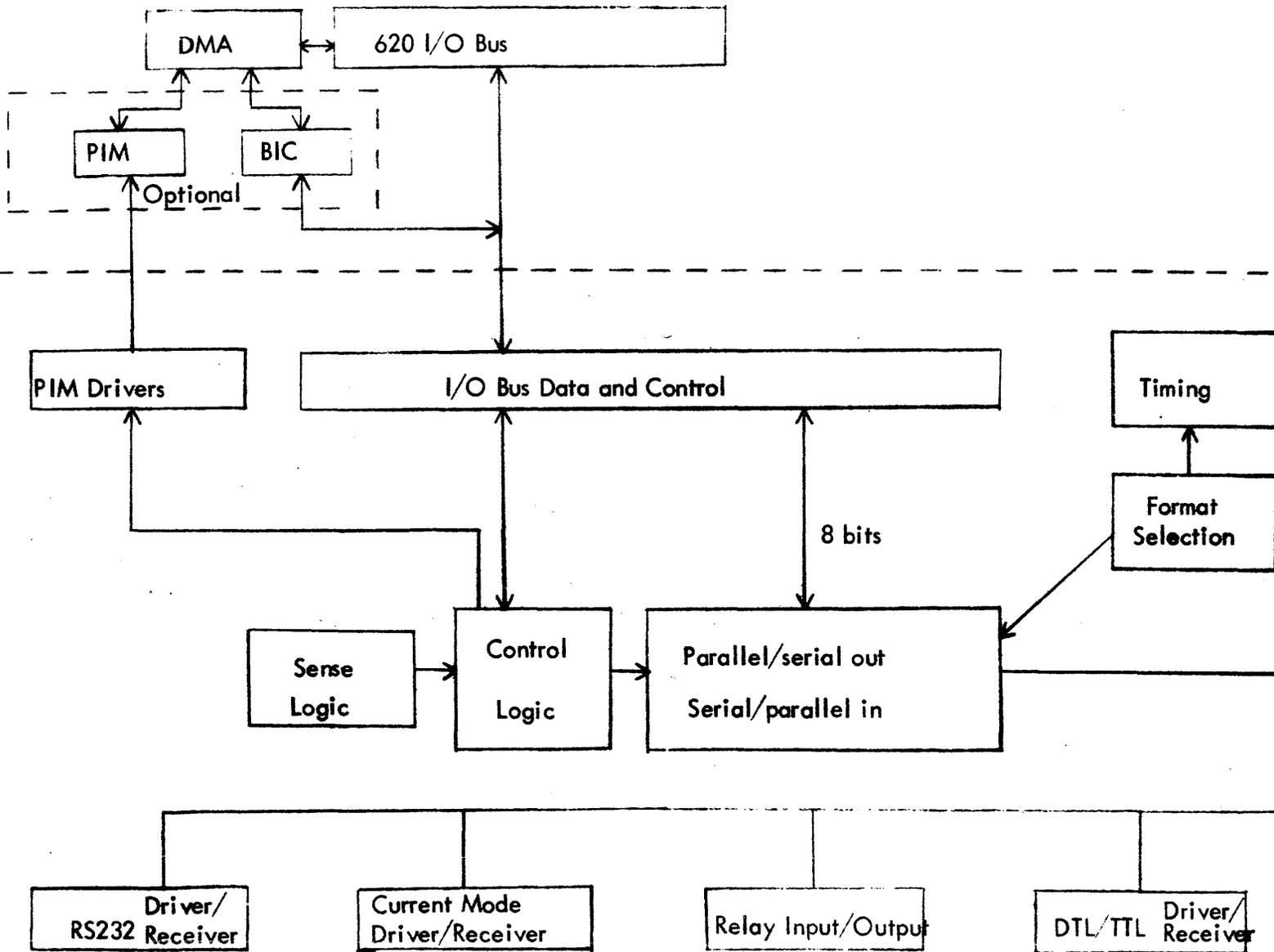
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**21101**

98A0767

C

SH 6 OF 53 REV

FIGURE 1.1 - FUNCTIONAL BLOCK DIAGRAM



Choice of four user interface circuits.

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### 1.2.2 Format Selection

Format selection is accomplished prior to initial operation or hookup to the serial device to be controlled. Choice of combinations of five jumpers will provide the following variations: One or two stop bits, 5-6-7 or 8 data bits, odd parity, even parity or no parity. (See Figure 1.3 and 1.4.)

### 1.2.3 620 I/O Bus

The I/O interface is an 8 bit interface to the 620 16 bit I/O. The most significant 8 bits are not used in the 16 bit data word. DMA data transfer in or out of the 620 is possible in conjunction with the BIC option. It should be noted that although this controller has full duplex capability, the BIC can only be connected to the transmit functions or to the receive function (not both at the same time).

### 1.2.4 Transmit Section

Data is transferred from the 620 I/O to the 8 bit parallel buffer register in the LSI circuit. The 8 bits are then transferred into the serial shift register and shifted out serially with the least significant bit (bit 0) shifted out first. A zero or "space" bit is inserted at the beginning of each serial word. This "Start Bit" precedes the 5,6,7, or 8 data bits and the parity bit (if selected) and the "Stop Bit"(s). The stop bit(s) is a "1" or "mark" bit.

### 1.2.5 Receive

Data is received into the serial shift register with Start Bit first followed by 5,6,7, or 8 data bits (least significant bit first), a parity bit (if selected), and 1 or 2 Stop Bits. When the complete character is shifted into the serial register, it is transferred into the parallel buffer register. Immediately after loading the parallel register, the Input Ready Sense line is made "true". Inputting the character will set Input Ready "false". Both Transmit and Receive functions are character buffered and operate independently. The format of the data being received must be the same as that selected for proper operation.

### 1.2.6 Control Logic

The Control Logic provides direction control for data transfer to and from the I/O bus, BIC connect control, Initialize control, and control of an external line (option enable/disable).



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IDENT NO.  
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98A0767

SH **8** OF **53** REV **C**

FIGURE 1.3

FORMAT SELECTION CHART

Jumpers Added

E13	Parity Bit Enabled
E14	One Stop Bit
E15 and 16	Five Data Bits per character
E15	Six Data Bits per character
E16	Seven Data Bits per character
E17	Odd Parity Bit

Result

Jumpers Omitted

E13	Parity Bit Disabled
E14	Two Stop Bits
E15 and 16	Eight Data Bits per character
E17	Even Parity Bit

Result

Typical ASCII devices use one start bit, 7 data bits and one parity or 8 data bits, with one or two stop bits.



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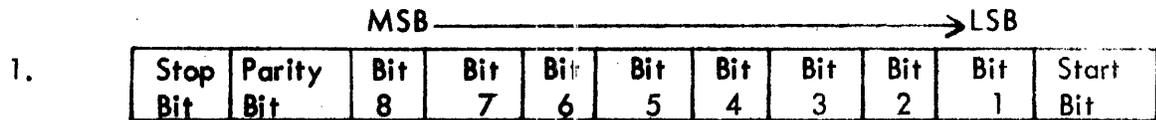
98A0767

C

SH 9 OF 53 REV

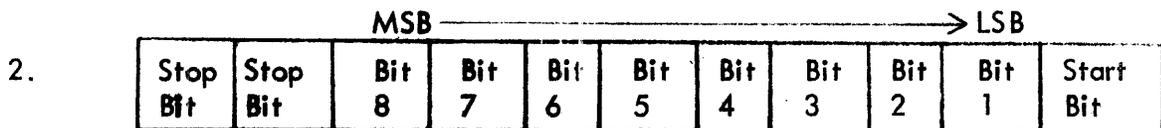
FIGURE 1.4

ASYNCHRONOUS FORMAT EXAMPLES



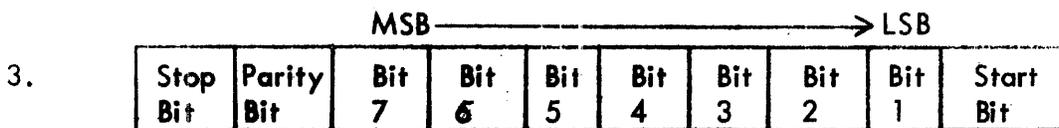
- a) 8 Data Bits Selected
- b) Parity Bit Selected
- c) One Stop Bit Selected

This is a good format for CPU to CPU.

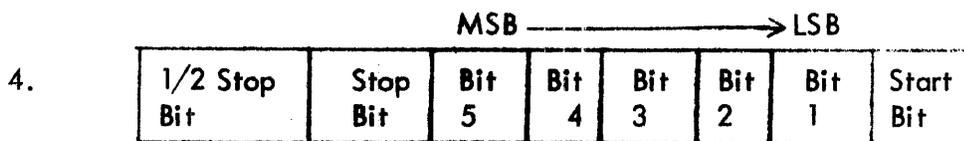


- a) 8 Data Bits Selected
- b) Parity Bit not Selected
- c) Two Stop Bits Selected

Typical for VDM teletype ASR 33 and 35.



- a) 7 Data Bits Selected
- b) Parity Bit Selected
- c) One Stop Bit Selected



- a) 5 Data Bits Selected
- b) Parity Not Selected
- c) Two Stop Bits Selected

Typical Baudot code.



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CODE IDENT NO.  
**21101**

98A0767

C

SH 10 OF 53

REV

### 1.2.7 Sense Logic

The Sense Logic provides status information to the operating program. Status of Input and Output data registers, three error indications, and an external input line can be monitored.

### 1.2.8 PIM Drivers

Three PIM Drivers are made available. One line indicates Input Ready. A second line indicates Output Ready. A third indicates either an Input Overflow Error or a Frame Error (**Break**). An Overflow Error indicates a second character was transferred to the parallel buffer register before the first character was Input. A Frame Error indicates that the first stop bit received was not a "1" bit. The program can detect that a "Break" character was received by verifying that the character received with the Frame Error indication was also an "All Zero" character. Typically, a "Line Break" is more than one consecutive character time. The UASC can receive but cannot transmit a "Line Break".

### 1.2.9 RS232 Driver/Receivers

The RS232 version fulfills the electrical characteristic requirements of EIA-RS232 B and C. Transmit data, receive data, a control line out and a status line in are implemented with RS232 drivers and receivers.

### 1.2.10 Current Mode Driver/Receiver

Transmit Data and Receive Data lines only are implemented with this interface. This current loop is capable of operation from 20MA to 60MA at voltages not to exceed 120V across the Transmit Driver. The current loop provides isolation greater than 10 meg ohms at 500Vdc. Detailed specifications are in section 2.2

### 1.2.11 Relay Input/Output

The relay input/output section is mechanized mainly for use as a Teletype Interface. A 2.2K - 2 Watt resistor in the Transmit or output circuit and a 2.7K - 2 Watt resistor in the Receive or input circuit are provided as dropping resistors to facilitate connection to the teletype provided line battery source on models 33 and 35. The line battery is a Teletype Option.

The resistors can be bypassed to provide a 20Ma - 12Vdc input/output circuit. Etched pads are made available for this purpose.



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CODE  
IDENT. NO.  
**21101**

98A0767

SH 11 OF 53 REV C

The relays are a "Reed" type relay which will function correctly from 0 to 300 baud (150 operations per second max).

### 1.2.12 DTL/TTL Driver/Receiver

The Transmit/Receive Data Lines, as well as the option driver line and option status line, are made available to the user for direct connect to DTL/TTL interfaces. These lines should not exceed 20 feet in cable length. The three previously described interfaces are routed through the DTL/TTL Receivers via the input connectors (J1 and J2).

### 1.3 Logic Mnemonics List

BRYX	BIC Data Ready
BTIA	Byte Transfer In
BTOA	Byte Transfer Out
CLK 16	Clock, 16 times data rate
CDCX	BIC Controlled Device Connect
CODX	Function Decode - CODO thru COD7
DAXX	Device Address
DRYX	Data Ready, I/O
DTIX	Data Transfer In
DTOX	Data Transfer Out
E/B Int	Framing Error or Overrun Error
EBXX	620 I/O Data Lines - EB00 thru EB15
EPE	Even Parity Select
FE	Framing Error on line break
FNCODX	Function Code EXC 0 thru EXC7
FRYX	Function Ready I/O
FUNCA	Function order any EXC command
INIT	Initialize
OE	Overrun Error
OPIN	Option Status Line
OPON	Optional Control Line Command Storage
ØSC	4.608 Mhz Oscillator Output
ØSC 1	2.304 Mhz Clock Rate
PE	Parity Error
PI	Parity Enable Line
RCRDY	Receive Data Buffer Ready
RCRINT	Receive Data Ready Interrupt
RD	Receive Data DTL/TTL Input
RD I	Receive Data Current Loop Input



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IDENT NO.  
**21101**

98A0767

SH 12 OF 53 REV

Logic Mnemonics List

RD2      Receive Data RS232 Input  
RD3      Receive Data Relay Input  
RSFF+    Clock Counter Reset Flip Flop  
RRX      Received Data - 8 bits parallel 9 thru 7  
SBS      Stop Bit Select  
SD        Send Data (Transmit)  
SERX     Sense Response  
TXRDY    Transmit Data Buffer Ready  
TXRINT   Transmit Ready Interrupt  
WLS1     Data Bits per Word Select  
WLS2     Data Bits per Word Select



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IDENT NO.  
**21101**

98A0767

C

SH 13 OF 53 REY

## SECTION II INTERFACE AND CONNECTIONS

### 2.1 RS232 Option

Conforms to EIA RS232 B and C as applicable.

2.1.2 Logic 0 = +4 to +24V

Logic 1 = 0V to -24V

### 2.2 Current Mode Option

#### 2.2.1 Driver Specification (Note 1)

Collector Emitter Voltage	$V_{CEO}$	150Vdc Max
Collector Current - Continuous	$I_C$	500 MAdc Max
Total Dissipation @25°C	$P_d$	1 Watt Max

#### 2.2.2 Receiver Specification (Note 1)

Input Forward Voltage Drop	$V_F$	1.5Vdc Max
Input Forward Continuous Current	$I_F$	60MA Max

#### 2.2.3 Isolation

Common Mode Protection	500V dc
Common Mode Resistance	10 Meg Ohms

2.2.4 Logic 0 = No loop current

Logic 1 = Loop current (20 ma min)

NOTE 1: Current limiting resistors (2.0K - 2W) are mounted in the input and output circuits. Values of these resistors may require change or shorted out. Current ratings above must not be exceeded.



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CODE  
IDENT NO.  
**21101**

98A0767

SH 14 OF 53 REV C

## 2.3 Relay Option

### 2.3.1 Input (Note 2)

Relay Input Coil Rating                      12.5Vdc max.

Relay Input Coil Resistance                  1250 ohms

### 2.3.2 Output (Note 2)

Reed Relay Contact Closure - Form A

### 2.3.3 Isolation

Common mode resistance                  10Meg Ohm @400Vdc

2.3.4      Logic 0 = No current  
              Logic 1 = Current (10 ma min)

Note 2: Current limiting resistors of 2.7K in the input side and 2.0K in the output side may be changed or shorted out. Caution must be used not to exceed 100 Ma through input relay coil.

## 2.4 DTL/TTL (not available when used with RS232)

### 2.4.1 Input

Both inputs present a 10Ma load at +5Vdc to the user.

### 2.4.2 Output

Both drivers are capable of sinking 50Ma at +5Vdc.

2.4.3      Logic 0 =  $\geq +2.4$  Vdc

              Logic 1 =  $0 \pm .5$  Vdc



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CODE  
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98A0767

SH 15 OF 53 REV **C**

FIGURE 2.1

PIN ASSIGNMENT CHART	
<u>RS 232</u>	
FUNCTION	PIN LOCATION
Serial Data Transmit	J2-36
Return	J2-35
Serial Data Receive	J2-42
Return	J2-41
Data In (Jumper)	J2-44 to J2-28
Optional Use Control Line	J2-34
Return	J2-33
Optional Use Status Line	J2-40
Return	J2-39

* CURRENT MODE VERSION	
FUNCTION	PIN LOCATION
Serial Data Transmit +	J2-4
Serial Data Transmit -	J2-10
Serial Data Receive +	J2-24
Serial Data Receive -	J2-18
Data In (Jumper)	J2-26 to J2-28

\* CAUTION: Excessive reverse current may damage the current mode interface.



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SH 16 OF 53

C

FIGURE 2.1 (Cont'd)

RELAY VERSION	
FUNCTION	PIN LOCATION
Serial Data Transmit +	J1-26
Serial Data Transmit -	J1-20
Serial Data Receive +	J1-36
Serial Data Receive -	J1-38
Data In (Jumper)	J1-40 to J1-2

* DTL/TTL CONNECTION	
FUNCTION	PIN LOCATION
Serial Data Transmit	J2-2
Return	J2-1
Serial Data Receive	J2-28
Return	J2-27
Optional Use Control Line	J2-22
Return	J2-21
Optional Use Status Line	J2-38
Return	

\* Note: The above Driver/Receiver cannot be used when the RS232 Driver/Receivers are in place.



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C

SH 17 OF 53 REV

**FIGURE 2.2**

DEVICE ADDRESS SELECTION							
TENS DIGIT				UNITS DIGIT			
D.A.	JUMPERS			D.A.	JUMPERS		
0X	76 to 83	77 to 85	78 to 87	X0	66 to 65	69 to 68	72 to 71
1X	76 to 82	77 to 85	78 to 87	X1	66 to 64	69 to 68	72 to 71
2X	76 to 83	77 to 84	78 to 87	X2	66 to 65	69 to 67	72 to 71
3X	76 to 82	77 to 84	78 to 87	X3	66 to 64	69 to 67	72 to 71
4X	76 to 83	77 to 85	78 to 86	X4	66 to 65	69 to 68	72 to 70
5X	76 to 82	77 to 85	78 to 86	X5	66 to 64	69 to 68	72 to 70
6X	76 to 83	77 to 84	78 to 86	X6	66 to 65	69 to 67	72 to 70
7X	76 to 82	77 to 84	78 to 86	X7	66 to 64	69 to 67	72 to 70

All pins on this page are on the I/O Back Panel.

INTERRUPT (PIM LINES)		
FUNCTION	PIN	Suggested Order of Priority
Transmit Data Reg. Ready	89	#2
Return	90	
Receive Data Reg. Ready	91	#1
Return	94	
Error or Break Interrupt	93	#3
Return	94	



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98A0767

SH 18 OF 53

C

## 2.5 Device Address and PIM Drivers

The DA for the UASC is wired on I/O back panel. The entire address, both octal digits, must be properly wired for the selected address. DA02 is the first standard address. Add 6 jumpers for the address selected per Figure 2.2.

The PIM drivers are implemented as pulse drivers and can be tied together as an "or" function or can be used on a one for one basis. The program must sense all three functions per interrupt if all are tied together to one PIM input. Reference Figure 2.2 for pin connections.



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CODE  
IDENT NO.  
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98A0767

SH 19 OF 53

C

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SECTION III  
PROGRAMMING - UASC

3.1 Instruction Set

Execute Instructions

EXC 0	1000XX	Connect BIC (output)
EXC 1	1001XX	Connect BIC (output)
EXC 2	1002XX	Connect BIC (input)
EXC 3	1003XX	Not used
EXC 4	1004XX	Initialize Controller
EXC 5	1005XX	Connect BIC (input)
EXC 6	1006XX	Enable (option)
EXC 7	1007XX	Disable (option)

Sense Instructions

SEN 0	1010XX	Frame Error or Break
SEN 1	1011XX	Output Ready
SEN 2	1012XX	Input Ready
SEN 3	1013XX	Not used
SEN 4	1014XX	Input Parity Error
SEN 5	1015XX	Not used
SEN 6	1016XX	Sense (option)
SEN 7	1017XX	Input overflow error

Data Transfer Instructions

OAR	1031XX	XFER "A" reg to controller
OBR	1032XX	XFER "B" reg to controller
OME	1030XX	XFER Memory to controller
INA	1021XX	XFER Data to "A" reg
INB	1022XX	XFER Data to "B" reg
IME	1020XX	XFER Data to Memory
CIA	1025XX	XFER Data to cleared "A" reg
CIB	1026XX	XFER Data to cleared "B" reg.

Standard Device Address is as follows:

1st Unit	=	02
2nd Unit	=	03
3rd Unit	=	04
4th Unit	=	05
5th Unit	=	06
6th Unit	=	07

DA01 may be used if UASC is used on the first teletype in a system.



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CODE  
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98A0767

SH 20 OF 53

## 3.2 Explanation of Instruction Set

### 3.2.1 EXC Instructions

EXC 0 and EXC 1 are both (either one) used to connect the BIC to output control of the UASC.

EXC 2 and EXC 5 are both (either one) used to connect the BIC to control input of the UASC. The multiple BIC connect instructions are implemented for compatibility of the UASC, Teletype Controller, Paper Tape Controller, etc., instruction sets. The EXC 6 and EXC 7 Instructions are used to turn on optional control line on and off. EXC 4 is used to reset all functions on the UASC.

### 3.2.2 Sense Instructions

SEN 0, Frame Error or Break, is used to detect that a character received did not have "mark" or "1" stop bits. The program can check the received character to verify that the data was all "zeros". If the data was all zeros and a Frame Error was sensed, a "Line Break" was received. If the data was not all zeros, the error was probably a "hit" on the line or noise.

SEN 1 and SEN 2 indicate the status of the Transmit and Receive buffer registers. SEN 4 indicates, when true, that a parity error has been detected on a character received.

SEN 6 indicates the status of an optional status line. SEN 7 indicates that another character was received before the prior character was removed from the input register.

### 3.2.2 Data Transfer Instructions

These instructions are self explanatory. See 3.1.

### 3.2.3 Interrupts

The interrupt functions are implemented on an individual system basis. SEN 1 and SEN 2 are implemented with individual drivers. SEN 0 and SEN 7 are "ORed" together on the same driver. All may be "ORed" together if desired.



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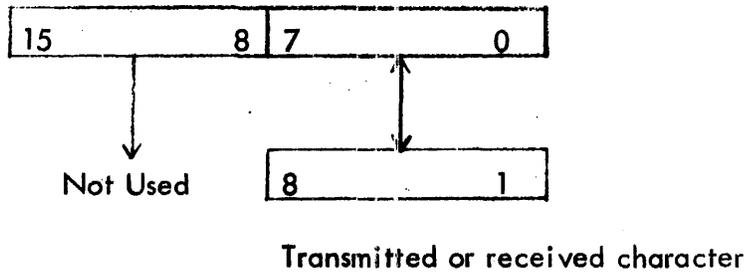
98A0767

SH 21 OF 53

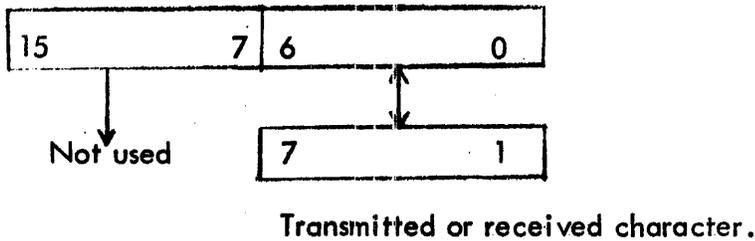
### 3.3 Word/Character Format (UASC to CPU)

Only data is transferred. Parity, if selected, is not transferred as part of data to or from the CPU.

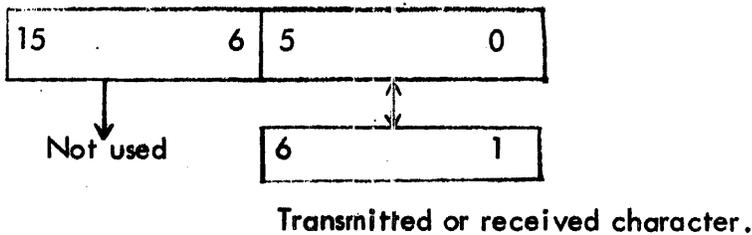
#### 3.3.1 16 Bit Word - 8 Bit Character



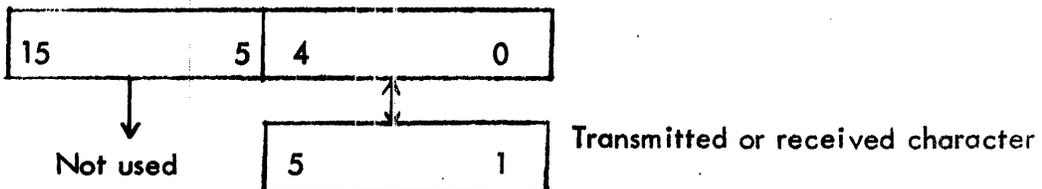
#### 3.3.2 16 Bit Word - 7 Bit Character



#### 3.3.3 16 Bit Word - 6 Bit Character



#### 3.3.4 16 Bit Word - 5 Bit Character



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98A0767

C

SH 22 OF 53

SECTION IV  
APPLICATION DATA

4.1 General Data

As previously mentioned in Section I, the controller is available in several versions. The general purpose nature of the controller logic and the three available interface types makes it adaptable for use in many applications where a serial bit/non-modem type interface is required. It is suggested that the user read and study this entire section prior to attempting operation.

The chart below gives the general characteristics of each model along with the cable length/rate restrictions.

FIGURE 4.1

Model	Serial Rate, BPS (bits per second)	Character Size	Stop Bit	Cable and Distance	Miscellaneous
RS232	45 to 9600 bps depending upon cable length (See Fig. 4.2)	5,6,7, or 8 level (bits). Parity bit (if any) is added to the data bits.	One or Two	Standard length=20ft., optionally up to 100ft.	
Current Mode	Same as RS232	Same as RS232	Same as RS232	Standard length=20ft. optionally up to more than one mile	User must provide "line battery" for loop current.
Relay	45 to 330 bps. Typically would be 75 or 110 bps. Relays will not operate reliably at higher than 300 bps.	Same as RS232	Same as RS232	Same as current mode	Same as current mode.



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98A0767

SH 23 OF 53

C

#### 4.2 Cable Length Versus Rate of Operation

As noted in Figure IV, the RS232 model cable length is restricted to 100'. The RS232 interface is not isolated and operates in a voltage mode as set forth in RS232 B and C. Therefore, the maximum cable distance must be observed. RS232 is typically restricted to 50 feet of cable distance, but usually operates well up to 100 feet. The other models operate on a current loop (isolated interface) basis and cables can be much longer. Table below gives some general guidelines. Cables should be twisted pair using 24 gauge (or larger) wire. Note that maximum operating rate of the relay version is 330 bps so Figure 4.2 applies primarily to the Current Mode version.

FIGURE 4.2

Cable Length	Rate in BPS
Distance up to 1,000 feet	10,000 bps maximum
Distance up to 2,000 feet	4,800 bps maximum
Distance up to 3,500 feet	1,800 bps maximum
Distance up to 5,000 feet	900 bps maximum
Distance up to 10,000 feet	300 bps maximum

#### 4.3 Version Selection

The three versions of the controller will cover a wide field of applications. The version of controller to be used depends primarily on the peripheral device interface. For example, a full-duplex terminal with an RS 232 I.F. (capable of operating with a 103 or 202 modem), but located within 100' of the computer, can usually be driven via the RS 232 version controller by adding a few jumpers at the peripherals (modem) connector. Typically, the modem control leads are jumpered "on" simulating the presence of the modem. "On" can be maintained by tying +12Vdc thru the 1K source to the control lead pins.

In the case where a user needs an isolated interface, he would use the current mode or relay version of the controller.

The data below will assist users in configuring workable systems. Several application cabling examples are shown for each version of the controller following the general discussion of cabling, full/half duplex, 20/60 ma and line battery implementation.



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SH 24 OF 53

C

#### 4.3.1 Full-Half Duplex Discussion

All models can operate in a true (simultaneous send and receive) full duplex manner or in a send only, receive only, send or receive - half - duplex manner.

If the controller is cabled up in a full duplex (4 wire) manner, it will not see a reflected (echoed) input of what it is sending. If, however, the controller is cabled up in a half-duplex manner (only one pair of wires used), the outputted data on the send circuit will be reflected (echoed) back into the controller's receive section as input. The CPU software must ignore this "echoed" input during output of a message in this case. See cabling examples and discussion of signal routing.

#### 4.3.2 20/60 MA Current Mode Operation

The Current Mode interface is limited at 20 to 60 MA operation. Two 2K-2 Watt dropping resistors are provided for use with a fixed voltage current source such as a model 33 or 35 teletype. Etched pads are provided for jumpering out the 2K resistors if a variable voltage current source (line battery) is available. The current loop interface provides DC isolation up to 500Vdc. If the user supplies the line battery, this isolation will be maintained. If loop current is derived from the 12V source on the controller board, isolation at the controller end is lost.

#### 4.3.3 Relay Current Loop Operation

The relay current loop is limited to 20 to 60 MA operation as well as the discrete current loop. 2K-2 Watt dropping resistors are provided for use with fixed voltage current sources (line battery), such as a model 33 or 35 teletype. Normal relay isolation is obtained with this interface when line battery is supplied by user.

#### 4.3.4 One and a Half Stop Bits

Although the user has the ability to select only one or two stop bits, he can operate with a 1-1/2 stop bit format. This is done by simply selecting two stop bits. For a Transmit function, the end result is that the maximum transfer rate is lowered by 1/2 bit time per character. For Received data, the controller ignores the second stop bit completely. Thus, the 1/2 bit time can be handled nicely and without noticeable speed reduction.



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SH 25 OF 53 FEB

#### 4.3.5 Line Battery Requirements

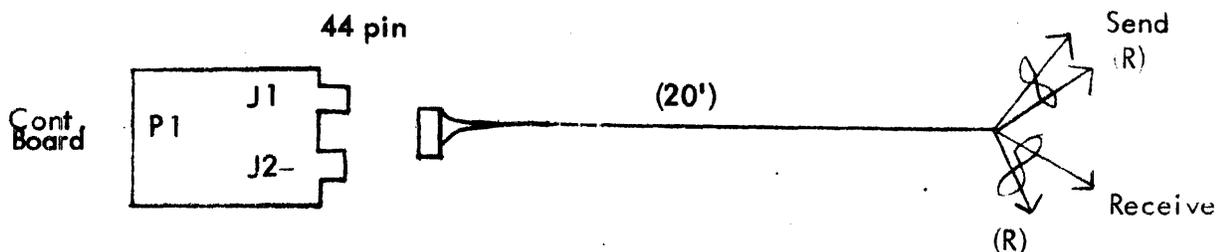
VDM may provide a controller only or a peripheral device along with the controller. If both the controller and VDM peripheral device is provided, VDM will supply "line battery". If VDM provides the controller only, the user (or peripheral supplier) will normally supply "line battery".

##### 4.3.5.1 What is "Line Battery"?

This is normally a power source (supply) capable of providing enough current for "loop" operation. In the case of a 20ma, full duplex loop application, a power supply capable of supplying 20ma to both loops is required. Voltage for proper operation of the VDM current loop (or relays) can be from 12V to 100V at 60ma maximum. Besides the power supply itself, a means of adjusting (and/or regulating) the amount of current is required. A trimpot or fixed resistor network (per loop supplied) is adequate. One "battery" supply can supply many current loops; Typically, a one amp, 24Vdc supply could handle 20 (20ma-full duplex) controller-peripheral device hookups. VDM suggests usage of a barrier strip approach for a multiple relay type loop installation. See next pages. Use of an isolated "separate" power supply is the preferable method of implementing line battery.

#### 4.4 Assembly of Cable (to peripheral device)

VDM provides a 20' open-ended cable kit with each controller. This cable kit includes a 44 pin Burndy type edge-on connector and hood, extra pins, and two twisted pairs in a jacket. The user makes up his cable to fit the application. See the examples for each type of controller. The cable routes from the top or bottom edge connector labeled J1-J2 on the controller, to the peripheral device. (Reference: figure 2.1) The two pairs provided in the 20' cable kit are needed for "send" signals and "receive" signals. The twisted pairs are connected to the 44 pin connector as shown on the following pages. Wires required for operation with the (option) control and status lines are not included.



Users must determine the proper pin numbers at the peripheral device if the peripheral is not supplied by VDM.



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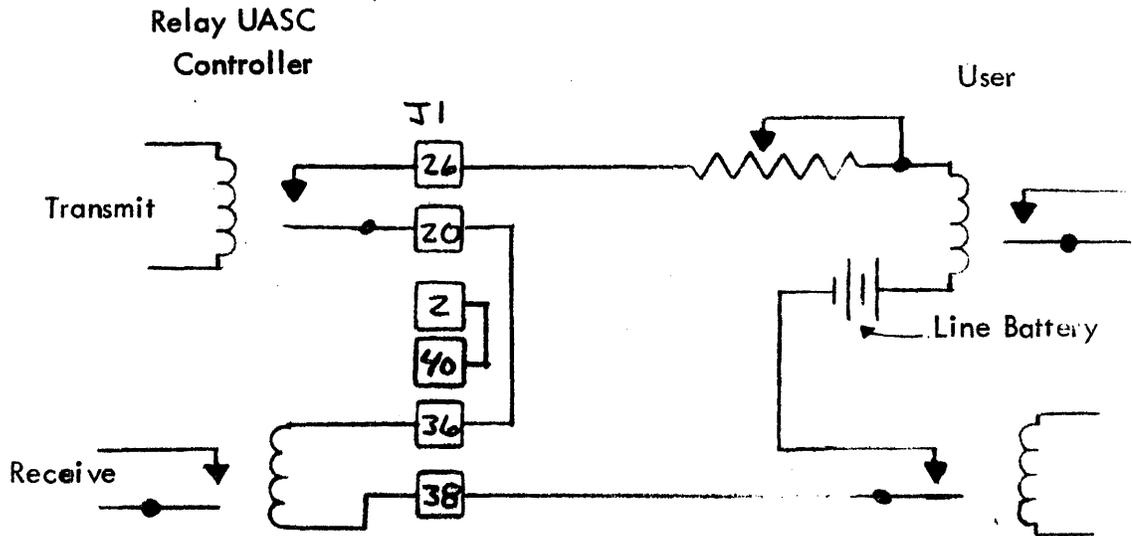
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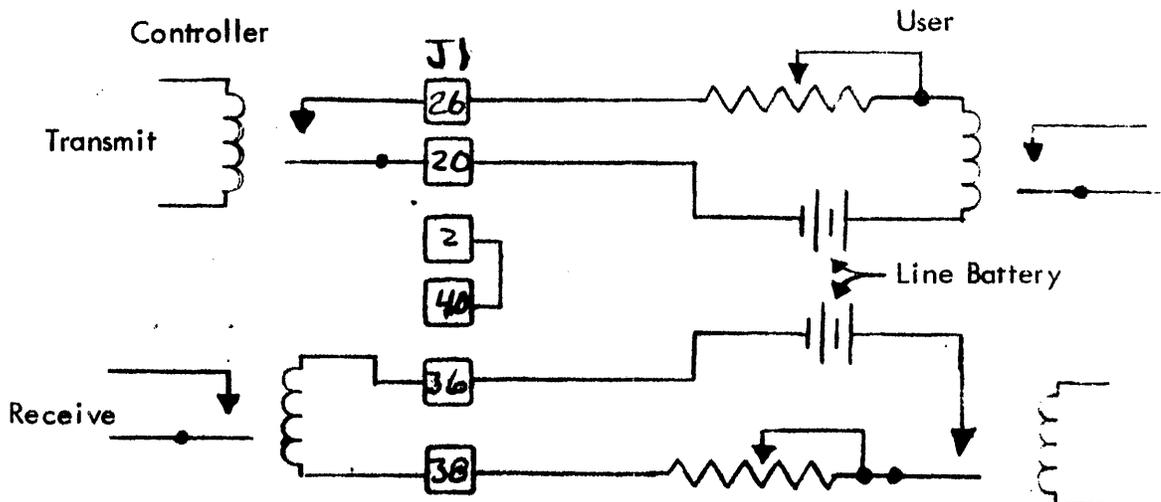
SH 26 OF 53 REV

4.4.1 Line Battery Hookup

4.4.1.1 Line Battery/Device Hookup - Half/Duplex



4.4.1.2 Line Battery/Device Hookup - Full Duplex



Note: Line Battery can be from one source if separate current limiting resistors are used.



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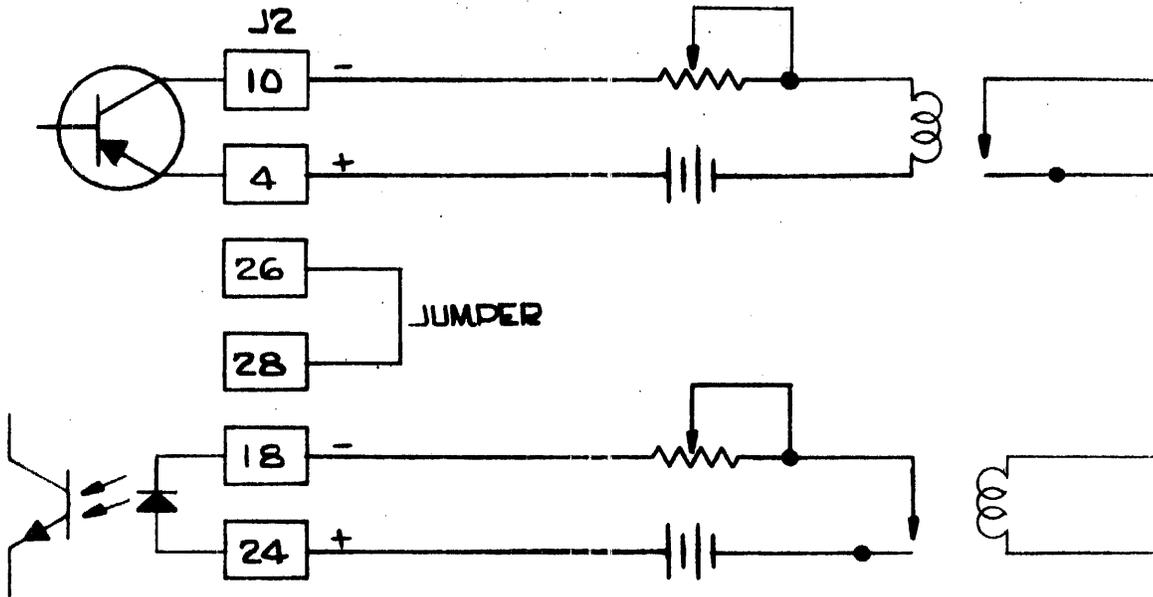
SH 27 OF 53 REV

### 4.4.1.3 Line Battery/Device Hookup - Full Duplex

Current Mode UASC

CONTROLLER

USER



Note: As in 4.4.1.2, line battery can be one source if separate current limiting resistors are used.



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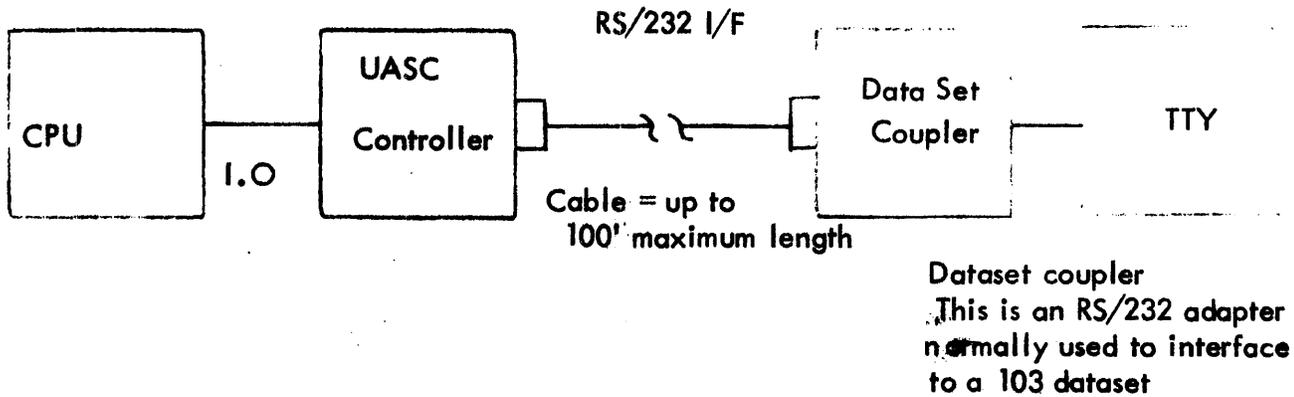
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SH 28 OF 53

4.5 Examples: Usage of RS232

4.5.1 Example #1 - Data Set Coupler

ASR-33 Teletype equipped with a dataset coupler.  
 Hardware controller to 110bps, 2 stop bits, no parity, 8 bits. Hook-up cable as shown.



Signal Routing

UASC

Dataset Coupler

<u>Pin</u>	<u>Signal</u>	<u>Signal</u>
J2-36	SD	RD
J2-35	(R)	(R)
J2-42	RD	SD
J2-41	(R)	(R)
J2-44	← Jumper	
J2-28		
J2-30	+V	CO-CTS-DSR Tie to +V for "on" condition



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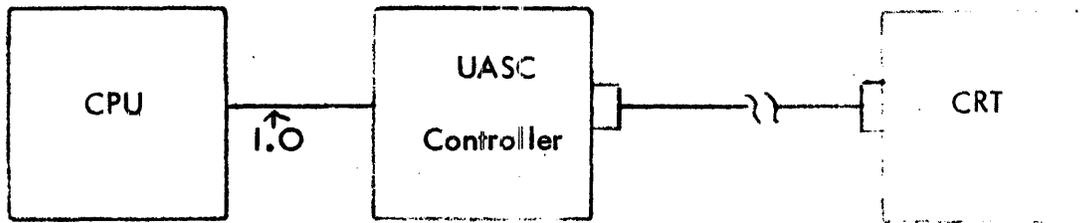
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SH 29 OF 53

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4.5.2 Example #2 - CRT Hookup

CRT with RS232 I/F (202 Modem). Hardwire controller to rate desired: Probably, 1200, 2400, or 4800 bps, 8 bits, 1 stop bit, parity.



Cabling

<u>UASC</u>		<u>CRT</u>
<u>Pin</u>	<u>Signal</u>	<u>Signal</u>

J2-36	SD	RD
J2-35	(R)	(R)
J2-42	RD	SD
J2-41	(R)	(R)

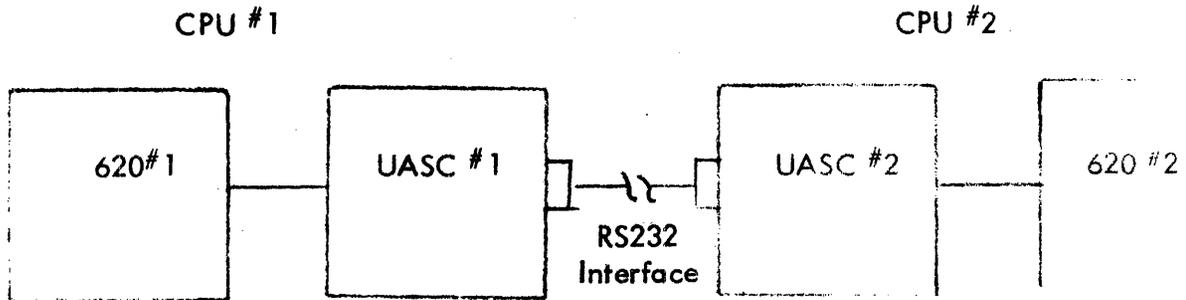
J2-30	CTS	} Tie to +V. For "on" condition
	CO	
	DSR	



4.5.3

Example #3 - 620 CPU to 620 CPU

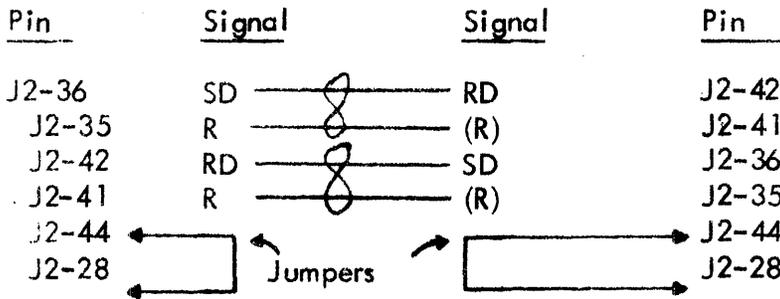
Hardwire the controller to 2400, 4800, or 9600 bpi. Set character size to 8 bits plus odd or even parity, one stop bit. Hook up the cable as shown.



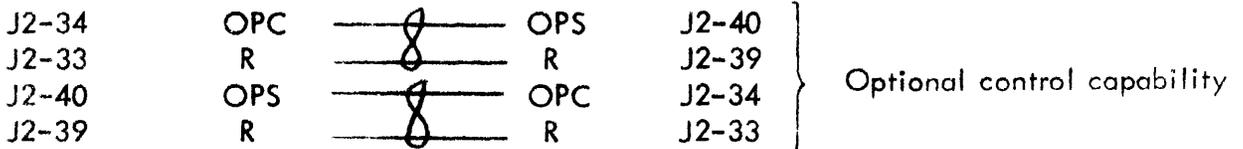
Cabling

#1 Controller

#2 Controller



There are no control leads to "tie on" in this case.



This hookup provides an additional control and status line.



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SH 31 OF 53 REV

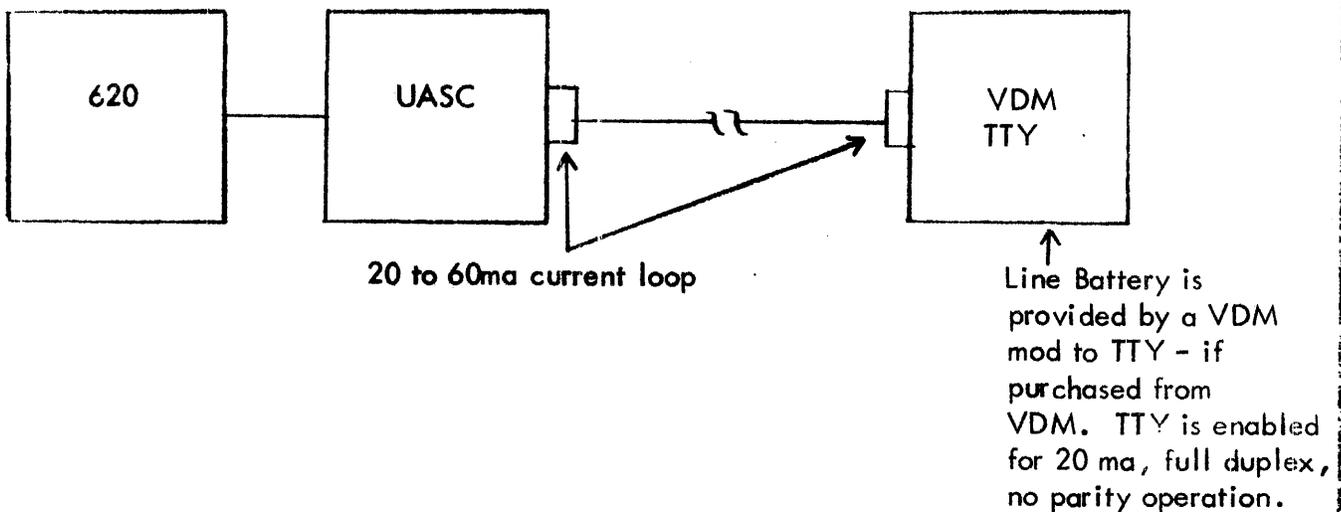
## 4.6 Usage of Current Mode Model

Unit has a solid state discrete current loop interface. It can typically be used to handle devices employing a current interface such as teletypes and/or terminals equipped with a 20/60ma current loop. Either half or full duplex operation is possible. This model has a major advantage over the RS232 interface in that the maximum cable length may be much longer. (See Figure 4.1). It has a major advantage over the relay interface in that the rate can be much higher than with electro-mechanical relays. See controller characteristics table and line battery discussion.

### 4.6.1 Example #1 - Interface to TTY

VDM modified KSR-ASR 33, 35 teletypes. Prepare the controller for 110 bps, 8 bits, no parity, 2 stop bits. Cable as shown.

Cable may be up to 10,000 feet long.



Cable Signals Note: 2.0K current limiting resistors must be in place for this hookup.

UASC		ASR 33 TTY		KSR/ASR 35	
Pin	Signal	Signal	Pin	Terminal Board	
J2-10	SD	RD	P2-8	Terminal 7	
J2-4	(R)				
J2-18	RD	SD	P2-6	Terminal 5	
J2-24	(R)	(R)	P2-9	Terminal 4	
J2-38	Jumper				



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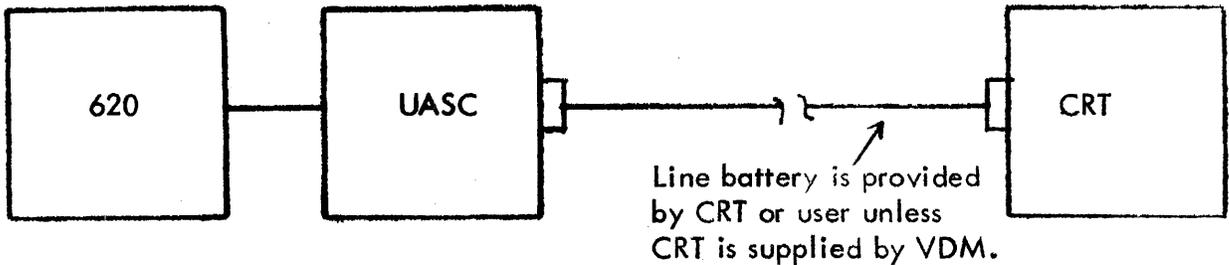
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SH 32 OF 53

REV

#### 4.6.2 Example #2 - CRT Hookup

CRT equipped with "current loop". Hardwire the controller to: bps = 1200, 2400, or 4800 bps, 8 data bits, 7 data plus parity, one stop bit. Hook-up cable as shown. See rate/distance table for maximum length of cable.

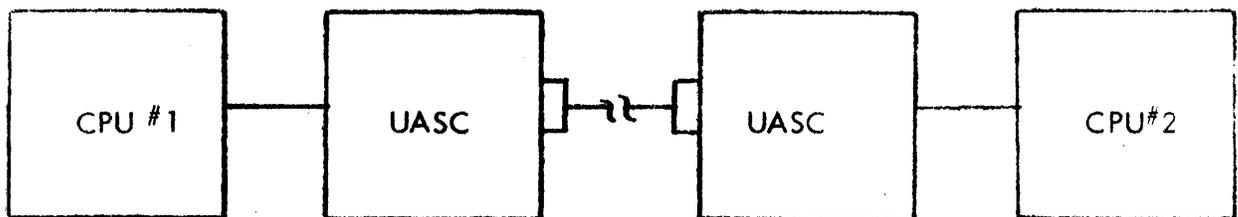


<u>Cable</u>		<u>CRT</u>
<u>Pin</u>	<u>Signal</u>	<u>Signal</u>
J2-4	SD	RD
J2-10	R	R
J2-24	RD	SD
J2-18	R	R
J2-26		
J2-28		

← Jumper  
Example #3 620 CPU to 620 CPU

Note: Current limiting resistors (R9 and R12) may require modification of value. 20ma min - 60 ma. max for logic "1".

Hardwire controller to: bps = 1200, 2400, 4800, or 9600 bps. Set to 8 bits plus odd or even parity, 1 stop bit. Hook up cable as shown. See rate/distance table for max. length of cable.



Cable hookup on next page.



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IDENT NO.  
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98A0767

C

SH 33 OF 53

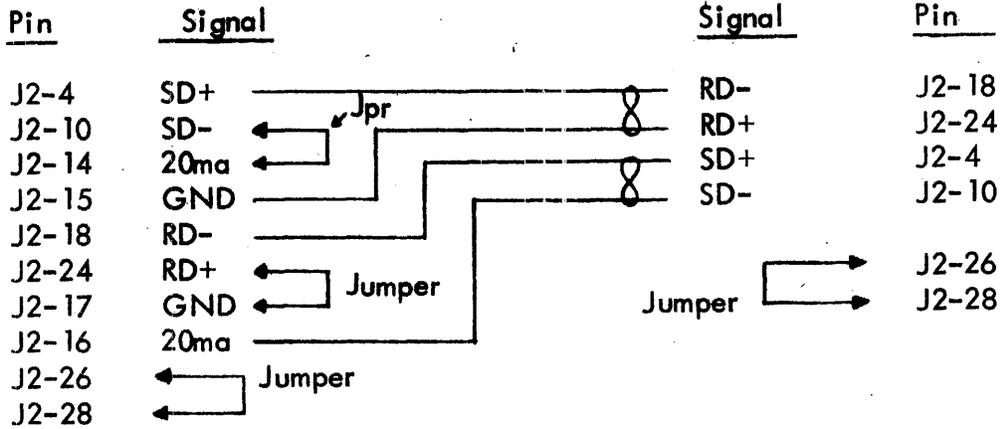
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4.6.3 (Cont'd)

Cable

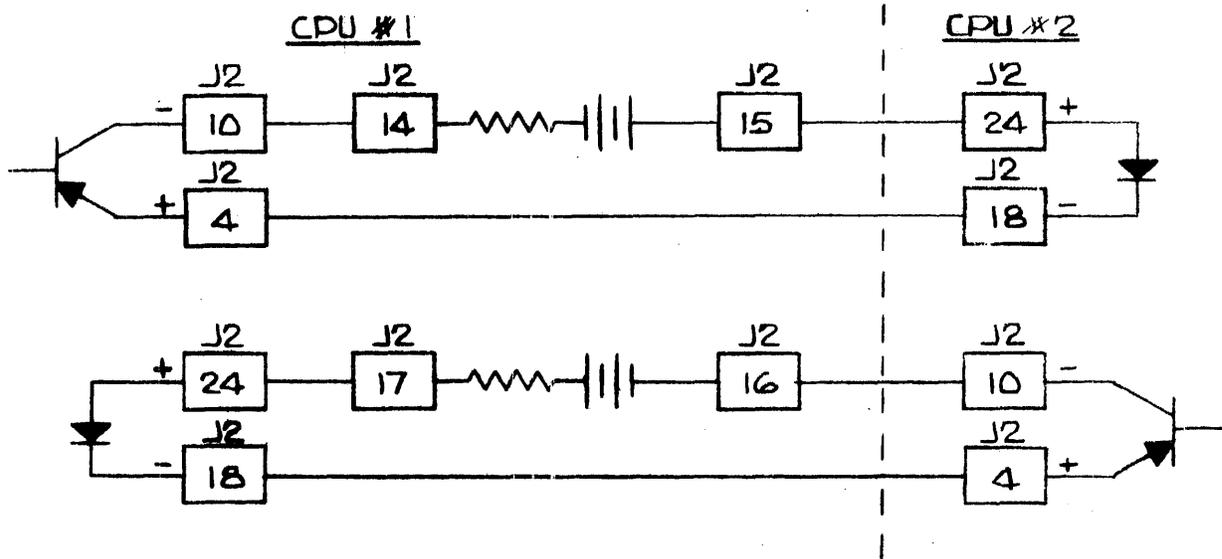
UASC#1 (Master)

UASC#2 (Slave)



Note: Current limiting resistors R9 and R12 on both ends are shorted out for this application.

620-620 Current Mode Interface Schematic



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98A0767

SH 34 of 53

#### 4.7 Usage of Relay Version

This model is equipped with a set of electromechanical (reed) relays and is designed for usage with teletype-telegraph (current loop) type equipment. It can handle 5 or 8 level applications such as (5 level) models 28, 32 (8 level) models 33 and 35 teletypes and 83B type polling (5 level) equipment. The relay interface can be hooked up to handle full or half-duplex "loops" as required. In the case of half-duplex operation, the CPU must ignore the "received" input while it is sending. The "received" input (while sending) is an "echo" only.

##### 4.7.1 Full Duplex - Cable Routing - Schematic

See 4.4.1.2



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**21101**

98A0767

SH 35 OF 53

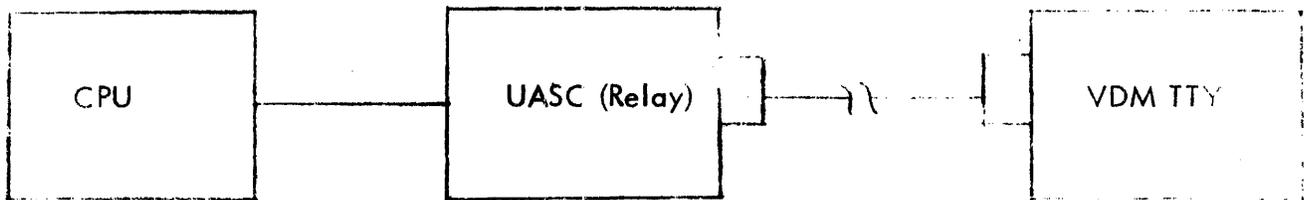
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### 4.7.3 Examples - Usage of Relay UASC

#### Example #1 - ASR/KSR 33 and ASR/KSR 35

VDM provided 33/35 Teletype = same hook-up as 4.6.1.

#### Cable Routing



#### Cable Routing

##### UASC

Pin	Signal	Signal	ASR 33	ASR 35
J1-26	SD	RD	P2-8	TB-7
J1-20	R			
J1-36	RD	SD	P2-6	TB-5
J1-38	R	R	P2-9	TB-4
J1-2				
J1-40				

Note: The 2.0K and 2.7K resistors (R13 and R14) must be in place when the UASC is interfaced to the TTYs as noted above.



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IDENT NO.  
**21101**

98A0767

SH 36 OF 53

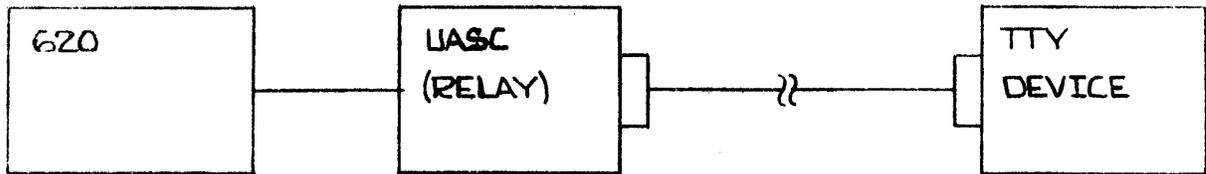
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#### 4.7.4 Example #2 - 5 Level TTY

620 CPU to user provided model 28 or 32 teletype or 83B unit.

Hardwire the controller to:

75 bps, 5 bit data, no parity, 2 stop bits, probably 60ma. Route cable and line battery as shown. See cable distance chart.



#### Signal Cable

See general cabling and previous page. Route cable for full or half duplex operation as required.

Half duplex - one pair cable used (ref: 4.4.1.1)

Full duplex - two pair cable used (ref: 4.4.1.2)



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98A0767

SH 37 OF 53

## SECTION V TESTING

### 5.0 General

The three interfaces, RS232, Current Mode, and Relay can be tested in a back-to-back configuration. Included in the UASC package is a test connector kit which can easily be assembled for the version purchased. The relay version can be tested when used with a TTY with standard VDM TTY test routines. VDM tests controllers prior to delivery using Test Specification 98A0768 as a guide.

### 5.1 Test Routine

The test routine requires that the UASC is installed in a 620 CPU slot with a properly wired test connector. Procedure for using this test routine is described in SPS 89A0228. This SPS also includes a description of the Test Routine.

### 5.2 Test Connector

The test connector is supplied in kit form. The test connector is assembled and used as further described.

#### 5.2.1 Assembly of Test Connector

##### 5.2.1.1 Model A - RS232C Test Connector

Install jumpers between the following pins:

36 to 42  
44 to 28  
34 to 40

Install test connector on J2.

##### 5.2.1.2 Model B - Current Mode Test Connector

Install jumpers between the following pins:

10 to 14  
4 to 18  
24 to 23  
26 to 28  
22 to 38

R9 and R12 must be temporarily jumpered (shorted)

Install test connector on J2.



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98A0767

SH 38 OF 53

C  
REV

5.2.1.3 Model C - Relay I/O Test

The relay version of the UASC can most easily be tested with a VDM modified ASR 33 teletype. The cable is wired per 4.7.3. Standard teletype test routines will verify operation.



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IDENT NO.  
**21101**

98A0767

**C**

SH 39 OF 53

REV

## SECTION VI THEORY OF OPERATION

### 6.0 General

Sections 1 thru 5 should be reviewed prior to using this Theory of Operation section. This section is written in a sequence that begins with the logic on page 1 and follows through to page 6 of 91C0445.

### 6.1 Control Logic

#### 6.1.1 Page 1

Contains power distribution, D.C. line filtering, and E-Bus connections. DAXX+, the Device Address, is made up of a 7 input "AND" function which is selectable at P1 on the back panel. Reference 2.5 and Fig. 2.2.

#### 6.1.2 Page 2

Contains the balance of the E-Bus connections which are further defined in the 620 interface manuals. CODO+ thru COD7+ are decoded at octal to 8 line decoder IC2. CODO+ thru COD7-- are used for both Sense and Command Instructions (Reference 3.1). EXC Commands are made up of FRYX (Function Ready), EB11+, DAXX (Device Address), and the appropriate COD(X) functions. WBBC is a nand gate latch which is set (EXC 0 or EXC 1) when transferring data out under BIC control. The latch is reset (EXC 2 or EXC 5) when transferring data in under BIC control. INIT (Initialize) is implemented on a "one shot" to assure that the LSI chip has a 2 usec reset pulse. INIT is pulsed by either a "SYSTEM RESET" from the control panel or an initialize command, EXC 4. OPON flip flop is set by EXC 6 and reset by EXC 7. OPON is storage for a control line that can be used for various different peripheral devices, an optional control.

#### 6.1.3 Page 3

Generally contains data control, interrupt drivers, and BIC control logic. The following terms are BIC oriented and are further defined in the BIC manual TAKK (Trap Acknowledge), DCEX (Device Connect Enable), CDCX (Controlled Device Connected), TROX (Trap Out), BCDX (BIC Disconnect), and TRQX (Trap Request). DTOX (Data Transfer Out) and DTIX (Data Transfer In) are used to steer data onto the E-Bus during data transfer commands such as an OAR or CIA instruction (Ref. 3.1).

The three interrupt drivers, TXRINT, RCRINT, and E/BINT are implemented as pulse drivers. Pulses are generated at the leading edge of the associated sense response term. For example, TXRDY- (Transmit Ready) initiates TXRINT.



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98A0767

C

SH 40 OF 53 REV

(PIM Driver Pulse) at the leading edge of TXRDY+. The interrupt drivers are pulsed to permit hardware "OR'ing" of all three drivers to one PIM input.

#### 6.1.4 Page 4

Contains the Sense response logic, the E-Bus drivers, and amplified outputs from the LSI chip. The Sense logic consists of the decoded control function bits (EB06, EB07, and EB08) which are decoded to CODO thru COD7 on page 2 of 91C0445. CODO is gated with FEB+ to obtain the first term in the Sense structure. CODO thru COD7 is used to implement SEN 0 thru SEN 7 respectively (Ref. 3.1).

#### 6.1.5 Page 5

Consists of the LSI Transmitter/Receiver chip and the four types of interface to the user. The LSI chip is covered in Section 6.2. Only one of the three optional interfaces will be found on a given board. The interface circuit specifications are found in Section II.

The RS232 interface is driven via IC21 for both TXDAT2 (Transmit Data) and OPCON2 (Option Control). RECDAT2 (Receive Data) and OPTION (Option Status Line) are received via IC 28. Both IC 21 and IC 28 are RS232 B & C compatible.

The Current Mode interface does not utilize the Option Control and Option Status lines. TXDAT1 (Transmit Data) is DC isolated via transformer coupling from signal ground. OSC1 running at a 2.3 MHZ rate transfers the output data (SD+) to the secondary of T1 via IC7. The pulsed data seen on the primary of T1 is effectively rectified by CR1. The voltage divider R7 and R8 properly bias the output driver Q1 which reconstructs the SD+ signal. Input data is also DC isolated from signal ground via an LED/Transistor, IC14.

The Relay interface is mechanized to permit utilization of 3 or 4 wire connections. Transmit Data is sent via K1 by means of a contact closure. Receive Data is received via K2. Normal D.C. isolation from signal ground is obtained with the relay interface.

The DTL/TTL interface is present on all three of the previously described interfaces. In fact, the other three interfaces utilize the DTL/TTL interface. The Receive Data is routed to RD at J1 or J2 and thru IC12. As an example the RS232 Receive Data line RD2 at J2-44 must be routed back thru the DTL/TTL receiver RD at J2-28. The optional control and Status lines OPCON1 and OPTION at J2-22 and J2-38 respectively are also always present on the three versions of the UASC. The DTL/TTL Transmit Data driver (TD at J2-2) is also always present on the three versions.



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IDENT NO.  
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98A0767

41 53

## 6.1.6 Page 6

Is covered in Section 6.3 .

## 6.2 Transmitter/Receiver Operation

### 6.2.1 Transmitter Operation

(Ref. Fig. 6.1, 6.3, and 6.5)

Power is applied, external reset is enabled and a clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TXRDY+, TRE+, and SD+ to logic "1" (Line is marking).

Once data strobe BTOA- is pulsed the TXRDY+ signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SD+ and TRE+ going to a logic "0", and TXRDY+ will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering.

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, TRE+ will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TXRDY+ is a logic "0" as was previously discussed.

It should be noted that the TRE+ line is not used. It can be used for timing reference when trouble shooting, however.

### 6.2.2 Receiver Operation

(Ref. Figs. 6.2, 6.4, and 6.6)

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available RCRDY+ to a logic "0".

Data reception starts when serial input signal changed from Marking (logic "1") to spacing (logic "0") which initiated a start bit. The start bit is valid if after transition from logic "1" to logic "0", the RD line continues to be at logic "0", when center



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CODE  
IDENT NO.  
**21101**

98A0767

SH 42 OF 53

sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DR) signal to determine if data has been read out. If the DR+ signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DR signal is at a logic "0" the receiver will assume that data has been read out. After DR goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

### 6.2.3 Description of Pin Functions

<u>Pin No.</u>	<u>Name</u>	<u>Symbol</u>	<u>Function</u>
1	V <sub>cc</sub> Power Supply	V <sub>cc</sub>	+5V Supply
2	V <sub>gg</sub> Power Supply	V <sub>gg</sub>	-12V Supply
3	Ground	GRD	Ground
4	Received Data Enable	RDE	A logic "0" on the receiver enable line places the received data onto the output lines. (Grounded)
5-12	Received Data Bits	RR7-RRO	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RRO.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity.



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CODE  
IDENT NO.  
**21101**

98A0767

SH 43 OF 53

C

<u>Pin No.</u>	<u>Name</u>	<u>Symbol</u>	<u>Function</u>
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run Error	OE	This line goes to a logic "1" if the previously received character is not read (DR line not reset) before the present character is transferred to the receiver holding register.
16	Status Enable	SE	A logic "0" on this line places the status bits onto the output lines. (Grounded)
17	Receiver Clock	CLK16	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data	BTIA-	A logic "0" will reset the DR line. Data remains available until replaced with new data.
19	Receive Data Ready	DR	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	RD	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	INIT	Resets all registers except RR7 - RRO registers. Sets SD, TRE, and THRE to a logic "1".
22	Transmitter Buffer Empty	THRE	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	BTOA-	A strobe on this line will enter the data bits into the data bits holding register.
24	End of Character	TRE	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. (Not used).



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CODE  
IDENT NO.  
**21101**

98A0767

SH 44 OF 53

C

<u>Pin No.</u>	<u>Name</u>	<u>Symbol</u>	<u>Function</u>															
25	Serial Output	SD	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.															
26-33	Data Bits Out	EB00-07	There are up to 8 data bits used.															
34	Control Level	CRL	A logic "1" on this lead will enter the control bits (PI, SBS, WLS1, WLS2, EPE) into the control bits holding register. This line is hard wired to a logic "1" level.															
35	No Parity	PI	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".															
36	Number of Stop Bits	SBS	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop and a logic "1" will insert 2 stop bits.															
37-38	Number of Bits/Character	WLS2 WLS1	These two leads will be internally decoded to select either 5, 6, 7, or 8 data bits/character. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>WLS1</th> <th>WLS2</th> <th>Bits/Character</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>5</td> </tr> <tr> <td>1</td> <td>0</td> <td>6</td> </tr> <tr> <td>0</td> <td>1</td> <td>7</td> </tr> <tr> <td>1</td> <td>1</td> <td>8</td> </tr> </tbody> </table>	WLS1	WLS2	Bits/Character	0	0	5	1	0	6	0	1	7	1	1	8
WLS1	WLS2	Bits/Character																
0	0	5																
1	0	6																
0	1	7																
1	1	8																
39	Odd/Even Parity	EPE	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.															
40	Transmitter Clock Line	CLK16	This is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.															



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CODE  
IDENT NO.  
**21101**

98A0767

SH 45 OF 53

C

### 6.3.1 Timing

Page 6 contains the crystal oscillator and the presetable counter for dividing the clock frequency to 16 times the data or baud rate. OSC1 (IC33) divides the oscillator output (4.608MHZ) by two. OSC+ and OSC1+ are gated together to create a 2.304 MHZ input to the 12 bit presetable ripple counter (IC13, IC20, and IC27). The down going edge of the carry line at pin 12 of IC27 causes the reset flip flop RSFF to set. The alternate clock pulse (OSC- and OSC) is gated into the preset line (pin 1 of IC12, IC20, and IC27) to preset the counter. The preset pulse rate is governed by the jumper combination as shown in Table II, Sheet 6 of 91C0445. The leading edge of the next count pulse resets the reset or preset flip flop, RSFF. (Ref. Fig. 6.7).



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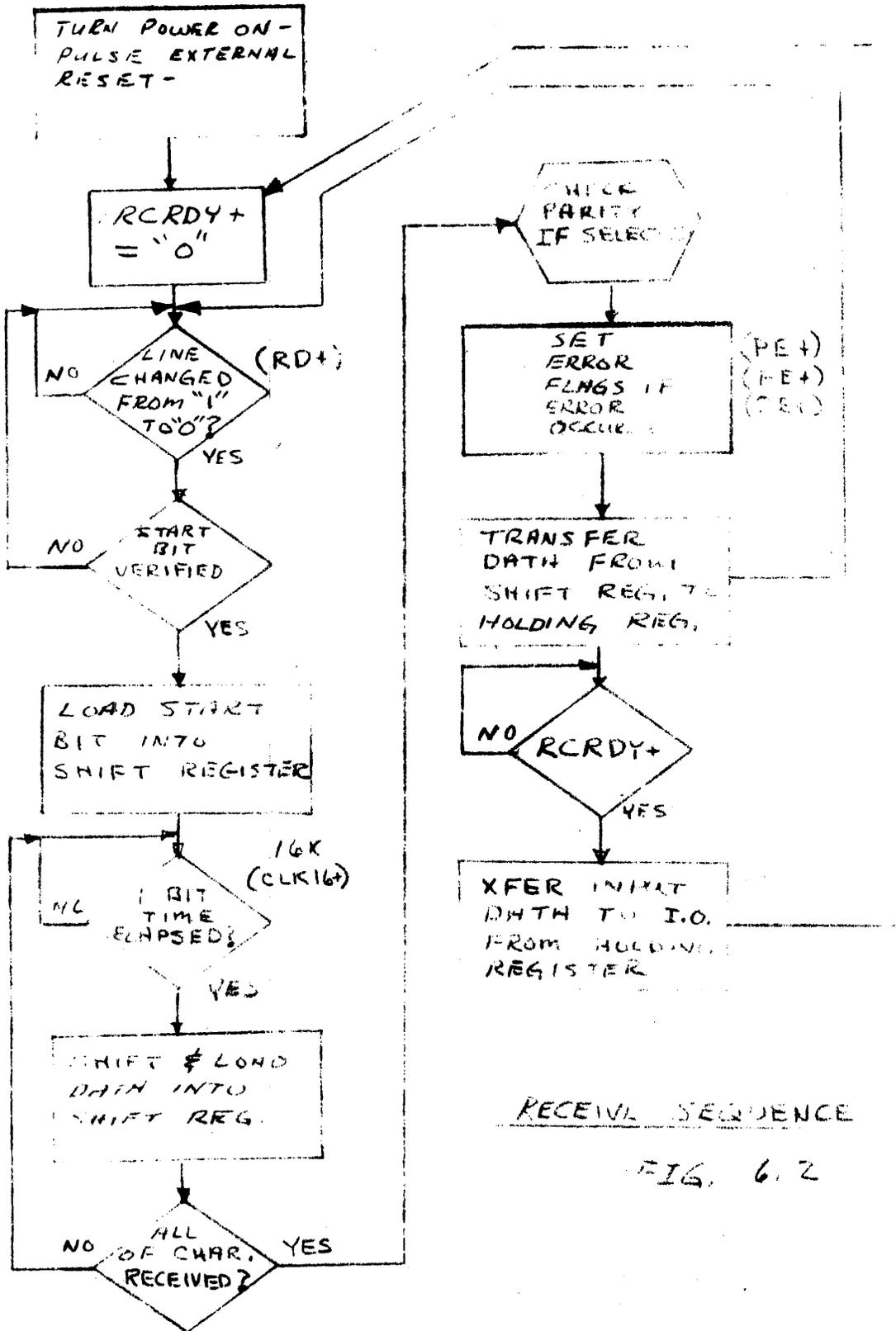
CODE  
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**21101**

98A0767

S14 46 of 53

C





RECEIVE SEQUENCE

FIG. 6.2



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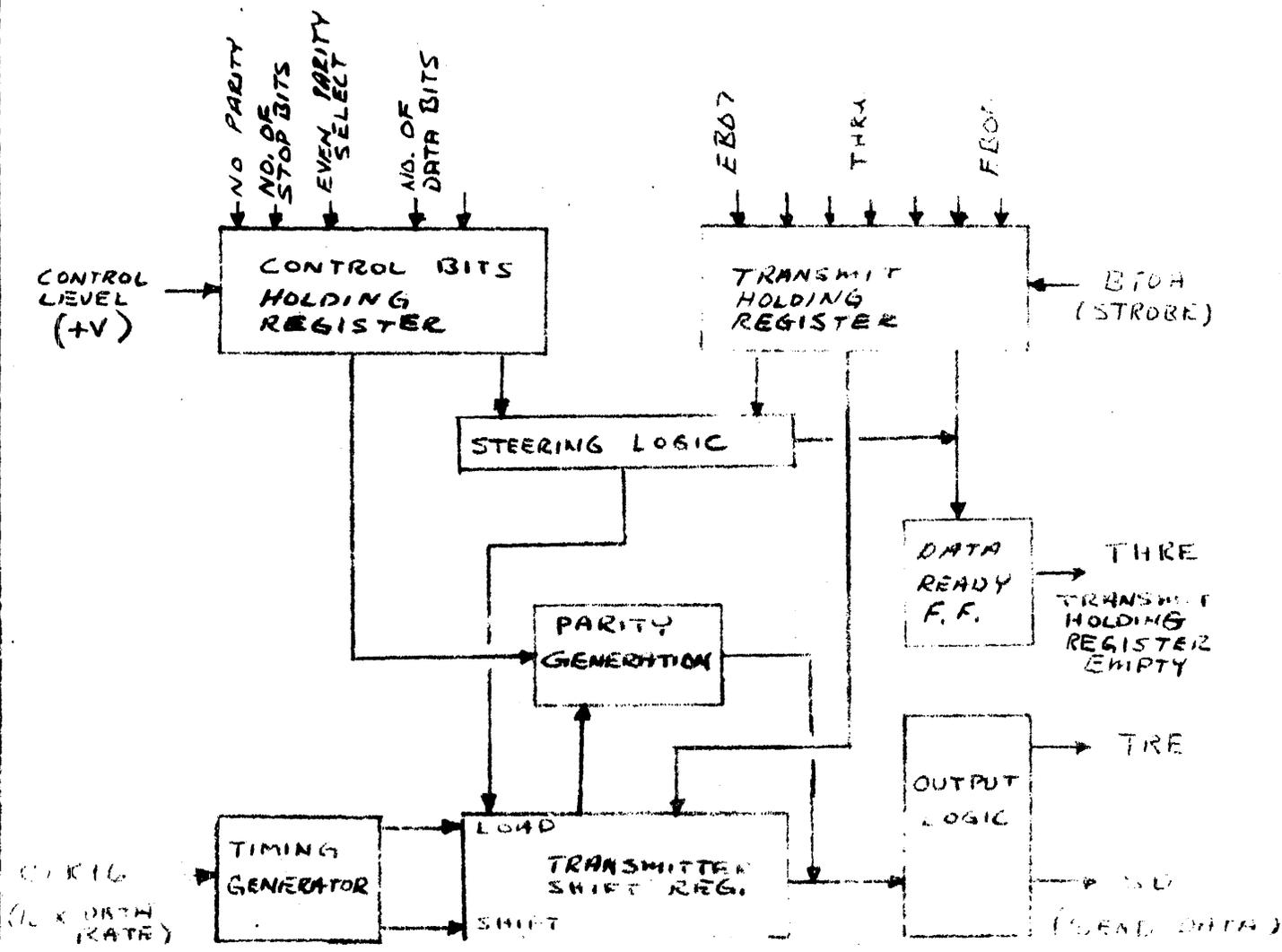
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**21101**

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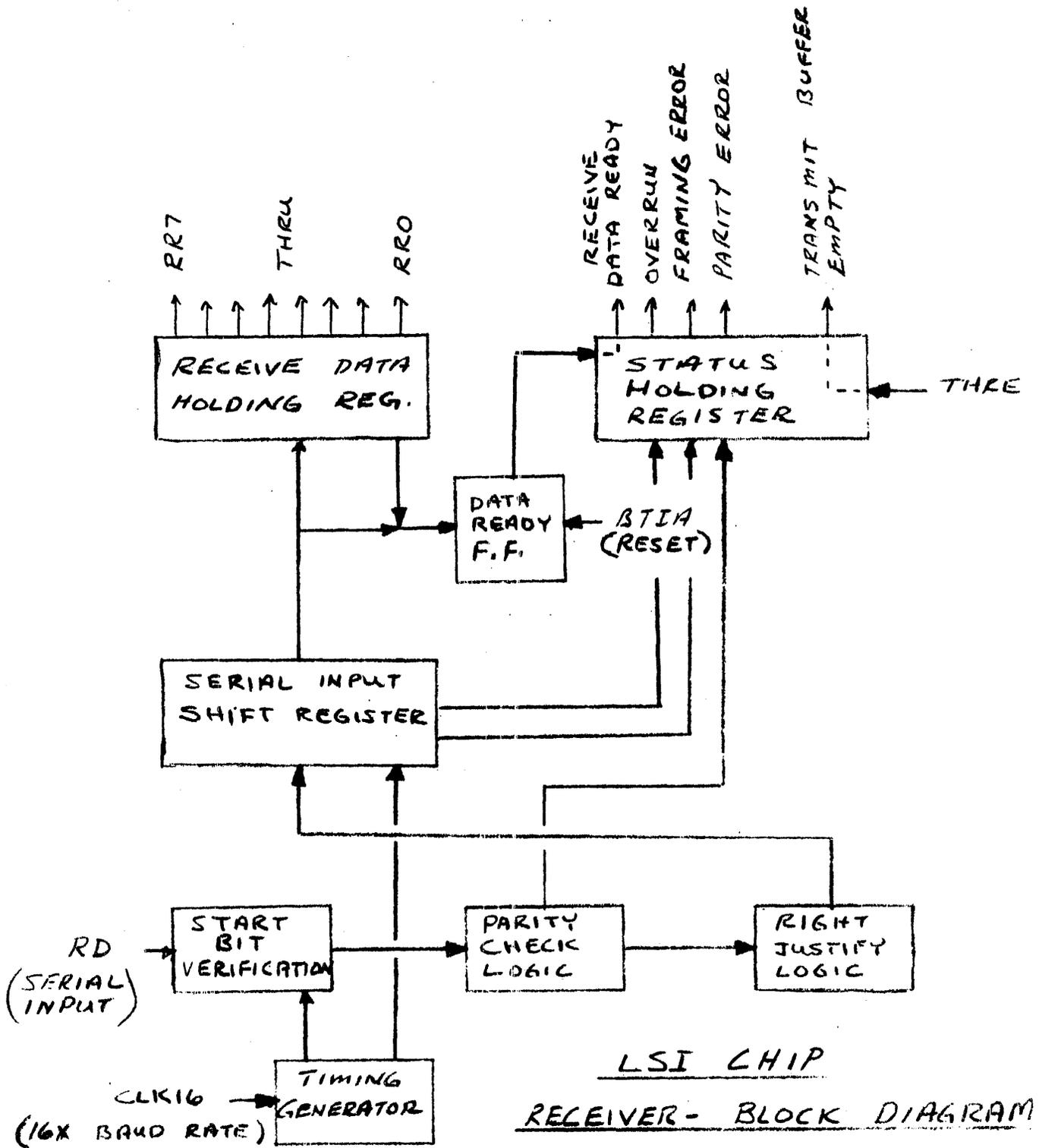
SH 48 OF 53

REV



LSI CHIP  
TRANSMITTER - BLOCK DIAGRAM

FIG. 6.3



LSI CHIP  
RECEIVER - BLOCK DIAGRAM  
 FIG 6.4



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CODE IDENT NO.  
**21101**

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C

SH 50 OF 53

REV

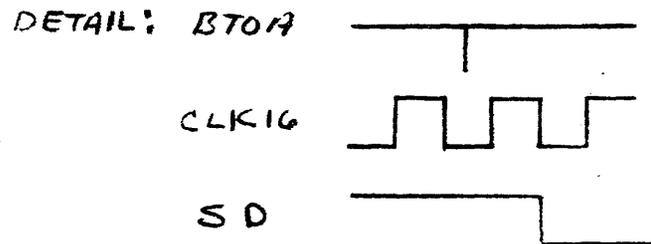
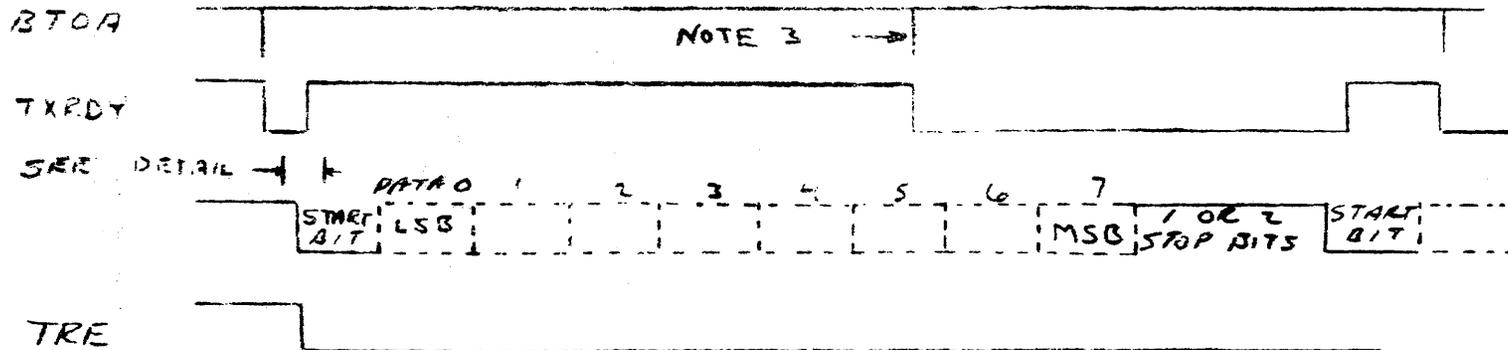


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21101

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NOTE:

Transmitter initially assumed inactive at start of diagram. Shown for 8 level code and parity and two stops.

1. Bit time = 16 clock cycles.
2. If transmitter is inactive the start pulse will appear on line within 1 clock cycle of time data strobe occurs. See detail.
3. Since transmitter is double buffered another data strobe can occur anywhere during transmission of character 1.

LSI CHIP TRANSMITTER TIMING

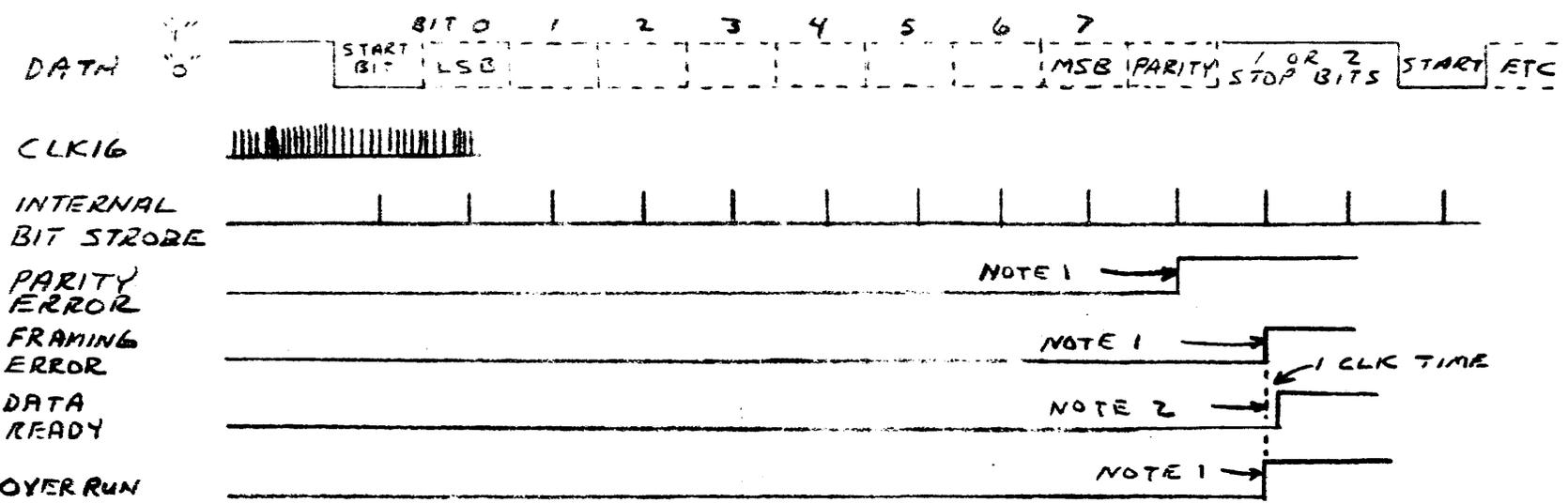
FIG 6.5



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CODE IDENT NO  
21101

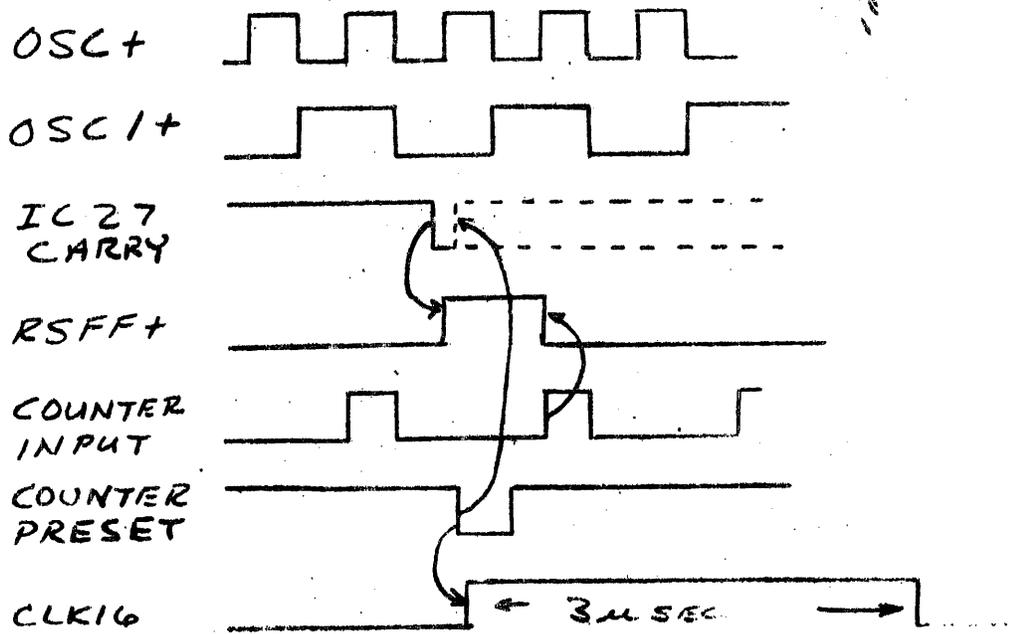
98A0761  
SH 52 OF 53



NOTES:

1. This is the time when the error conditions are detected, if error occurs.
2. Data available is set only when the received data, PE, FE, or has been transferred to the holding registers. (See receiver block diagram).
3. All information is good in holding register until data available tries to set for next character.
4. Above shown for 8 level code parity and two stop for no parity, stop bits follow data.
5. For all level code the data in the holding register is RIGHT JUSTIFIED; that is, LSB always appears in RRO (pin 12).

LSI CHIP RECEIVER TIMING  
FIG 6.6



OSCILLATOR/ COUNTER TIMING.

FIG 6.7



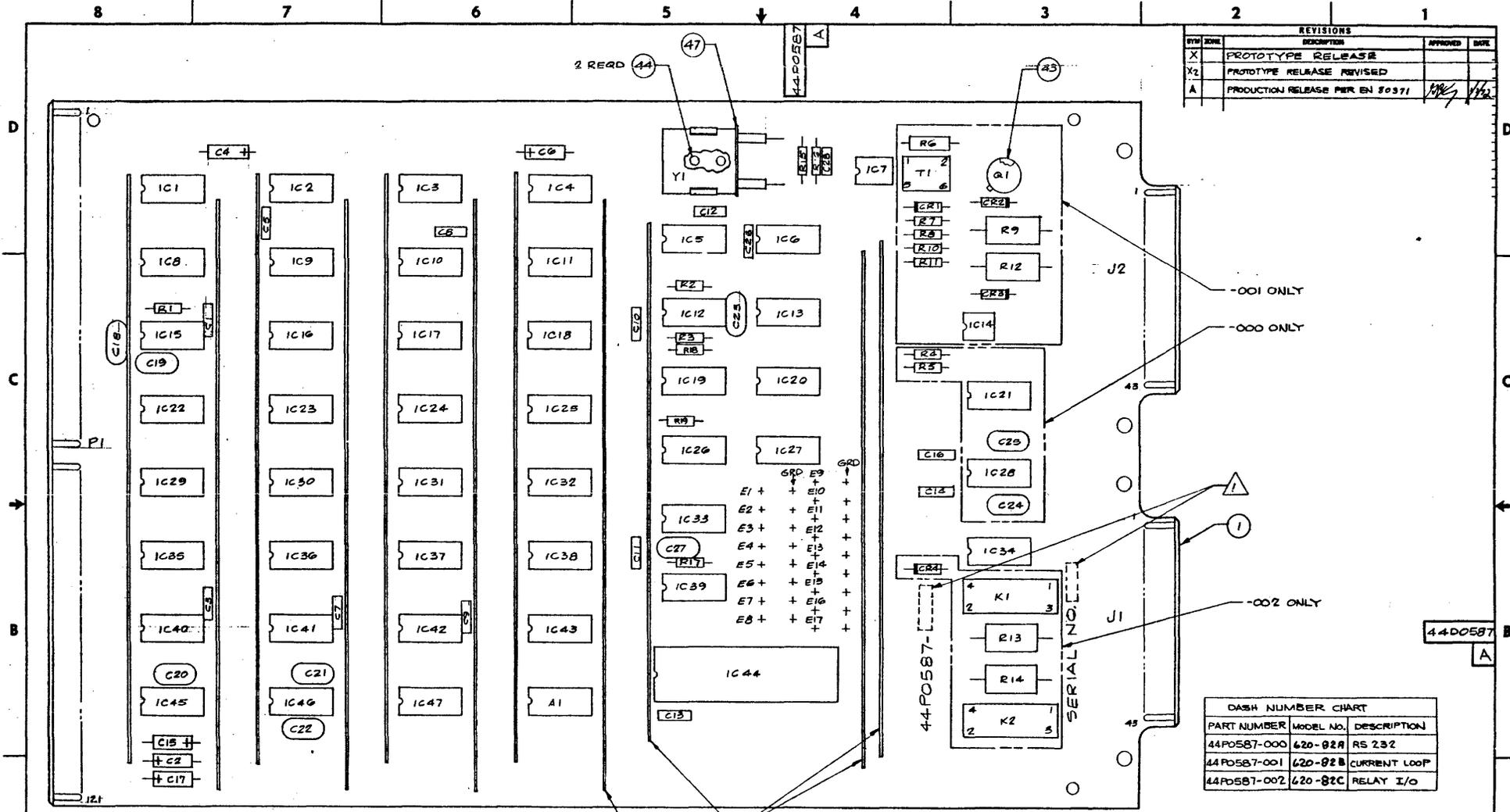
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CODE  
IDENT NO.  
21101

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SH 53 OF 53 REV



REVISIONS			
REV	DATE	DESCRIPTION	APPROVED
X		PROTOTYPE RELEASE	
X2		PROTOTYPE RELEASE REVISED	
A		PRODUCTION RELEASE PER EN 50371	

-001 ONLY

-000 ONLY

-002 ONLY

44-PO587

DASH NUMBER CHART		
PART NUMBER	MODEL NO.	DESCRIPTION
44-PO587-000	620-82A	RS 232
44-PO587-001	620-82B	CURRENT LOOP
44-PO587-002	620-82C	RELAY I/O

FOR PARTS LIST SEE 44-PO587

MARK REVISION LETTER AND VERSION OF PARTS LIST TO WHICH PART WAS MANUFACTURED AND SERIAL NO. USING .12 HIGH PERMANENT CHARACTERS APPROX. WHERE SHOWN.  
NOTE: UNLESS OTHERWISE SPECIFIED

- REFERENCE DRAWINGS
- 4000501 - P.C. BOARD
  - 9100352 - LOGIC DIAGRAM
  - 9700691 - ARTWORK
  - 9700692 - SILKSCREEN
  - 9700693 - SOLDER MASK

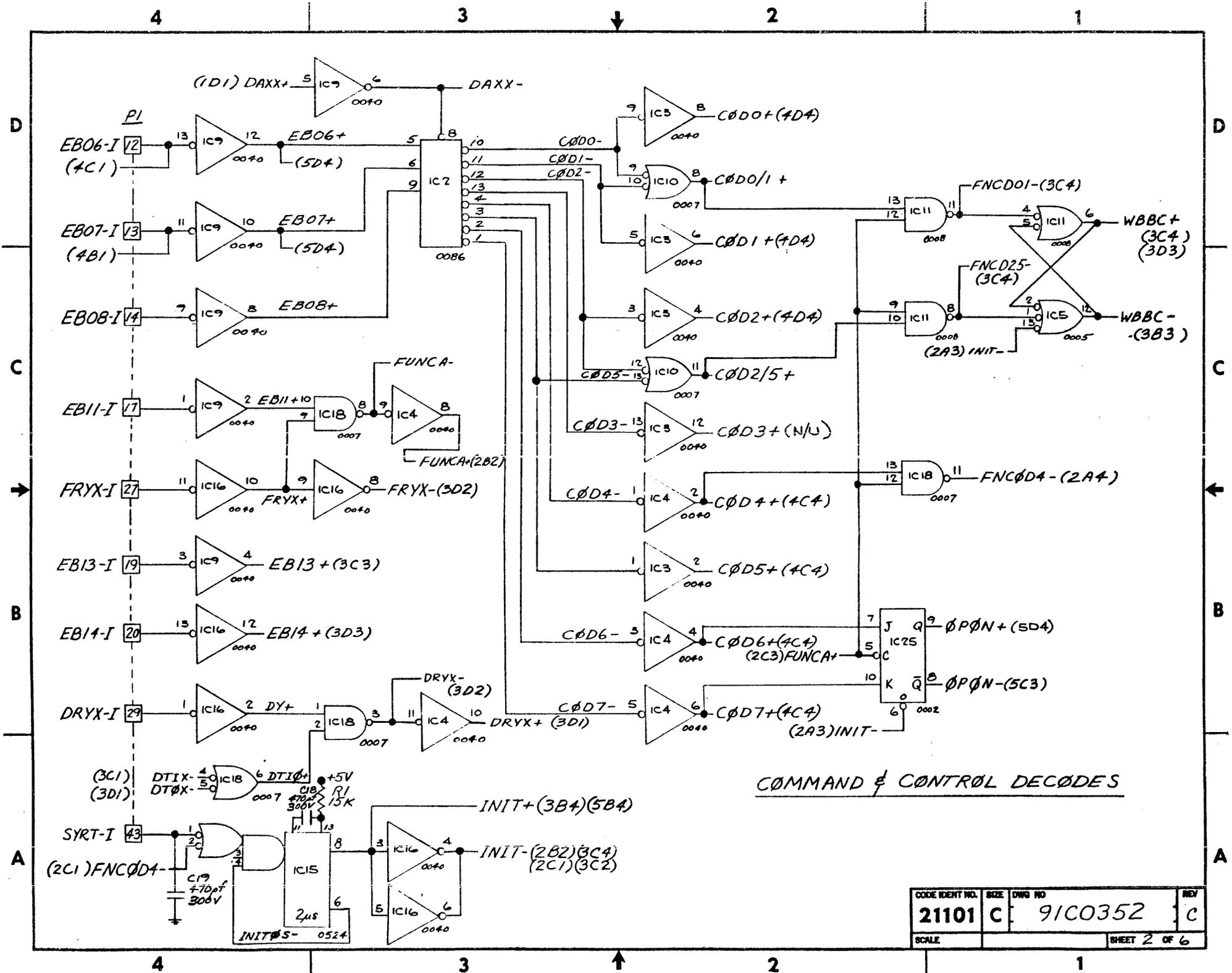
MODEL NO. 620-82A, 01C  
SERIAL NO. 01A1259  
DATE: 1/25/71

DIMENSIONS ARE IN INCHES AND AFTER FINISHING  
TOLERANCES UNLESS OTHERWISE SPECIFIED  
X ± .1  
XX ± .05  
XXX ± .02  
XXX ± .01  
XXX ± .005  
XXX ± .0025  
XXX ± .0015  
XXX ± .001  
XXX ± .0005  
XXX ± .00025  
XXX ± .00015  
XXX ± .0001

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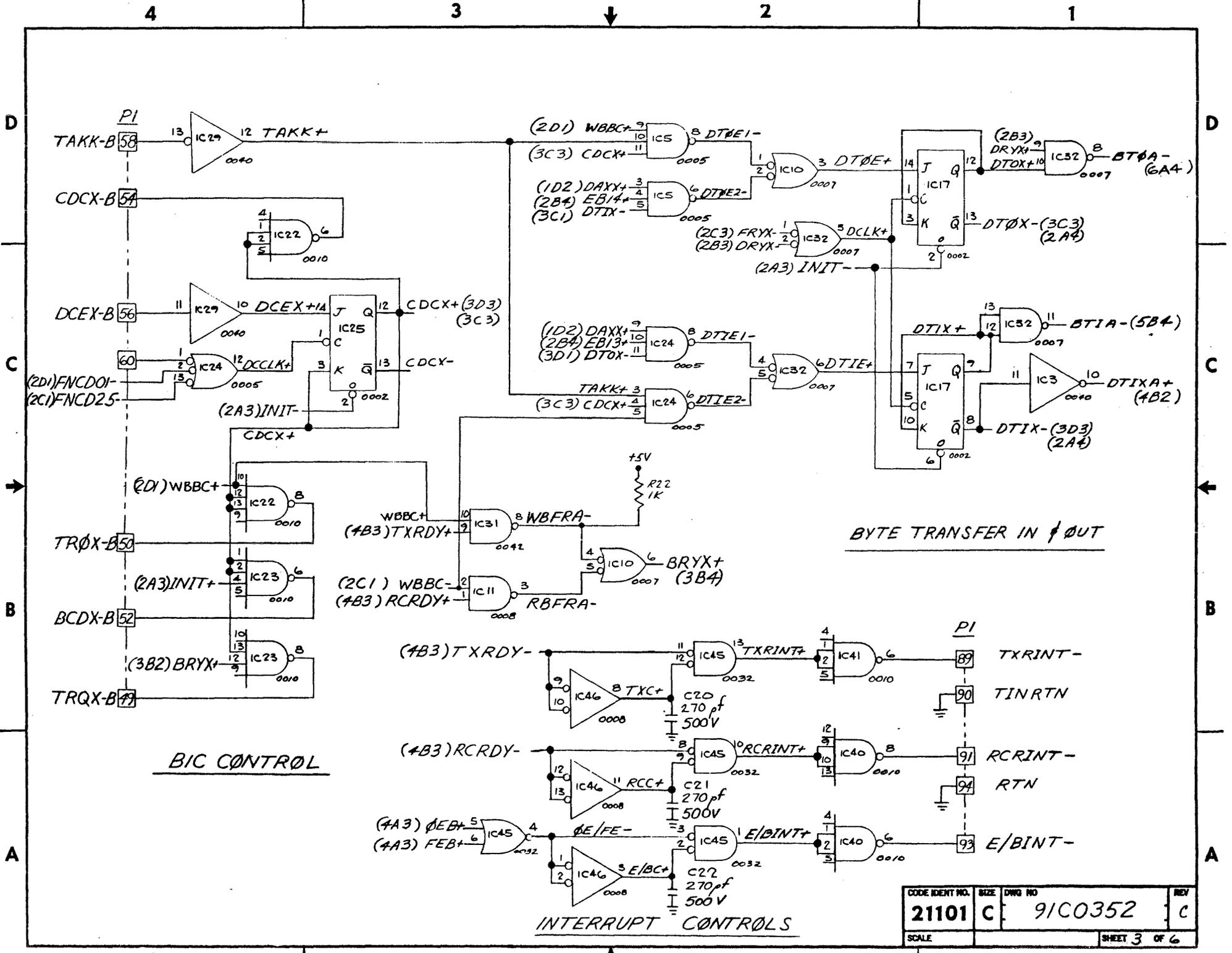
	TITLE <b>UNIV SER CONT ASSY</b> DM335
CODE IDENT NO. <b>21101</b>	DATE NO. <b>D 44-PO587</b>
SCALE 2/1	SHEET 1 OF 1





COMMAND & CONTROL DECODES

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0352	C
SCALE			SHEET 2 OF 6

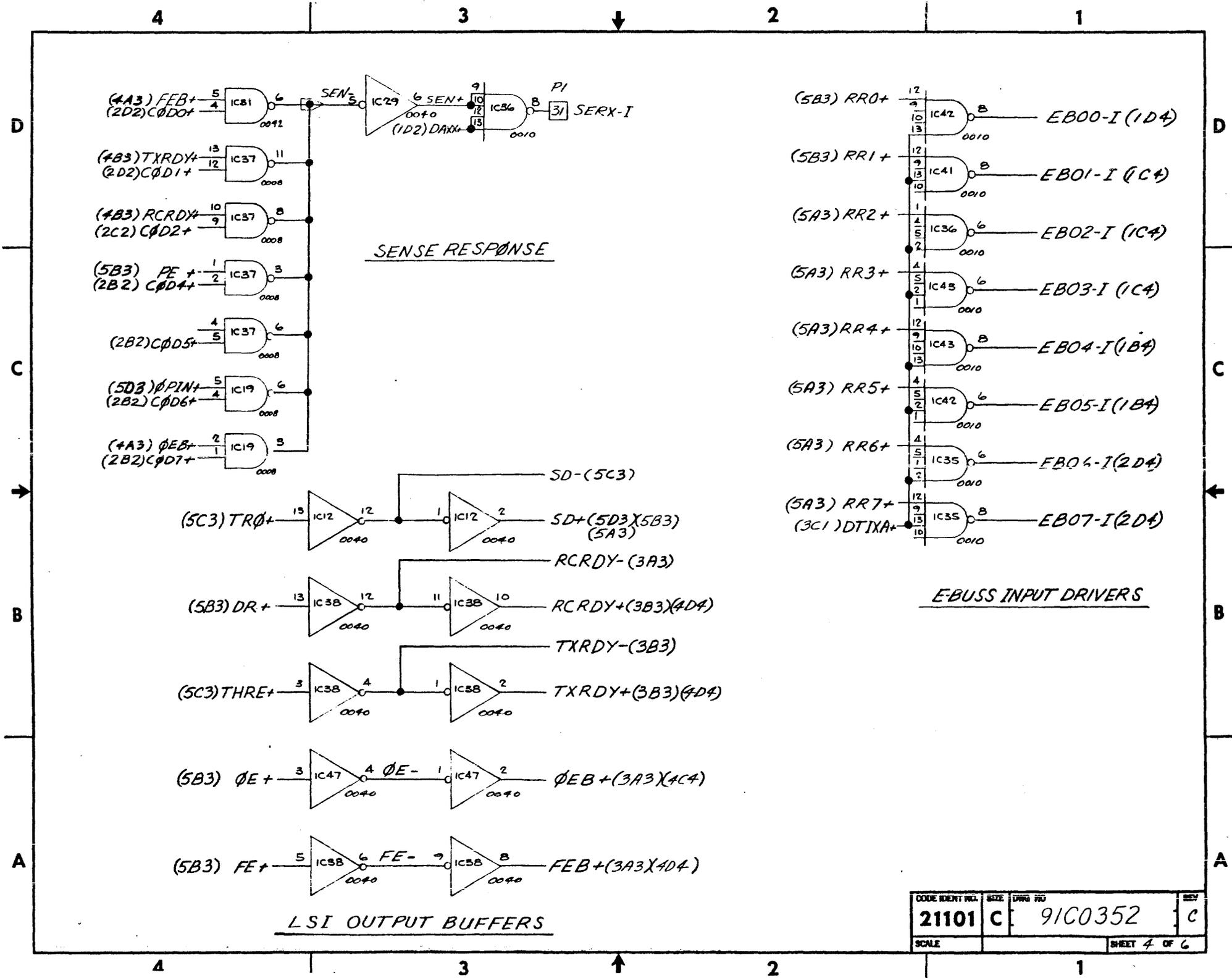


BYTE TRANSFER IN / OUT

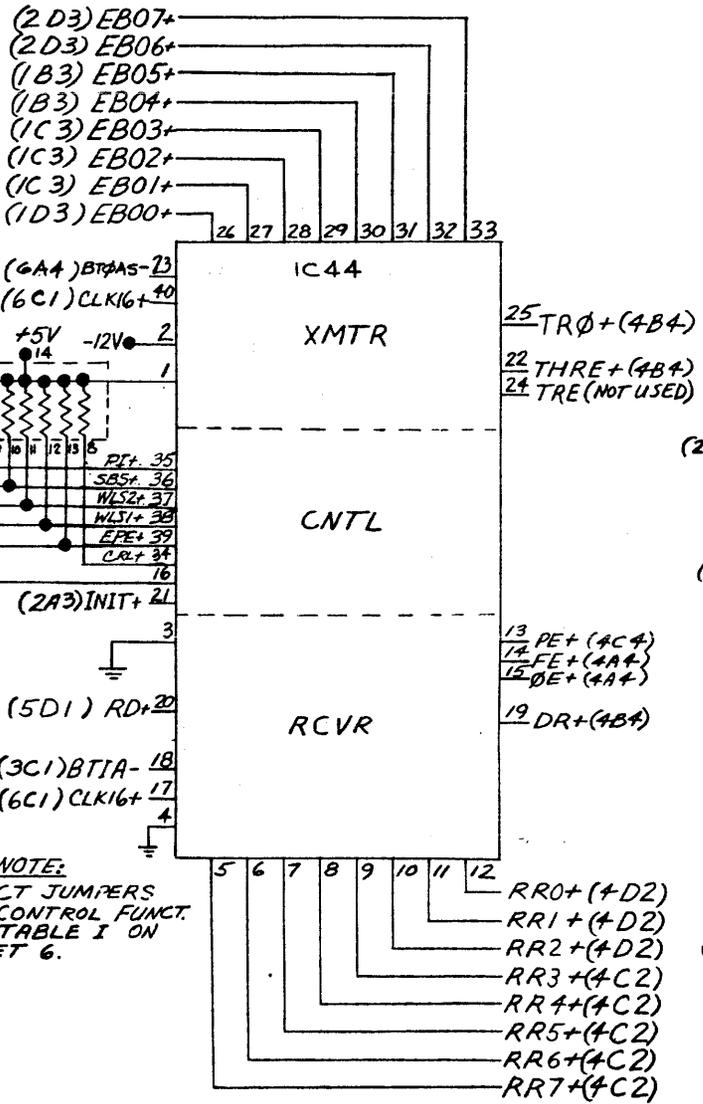
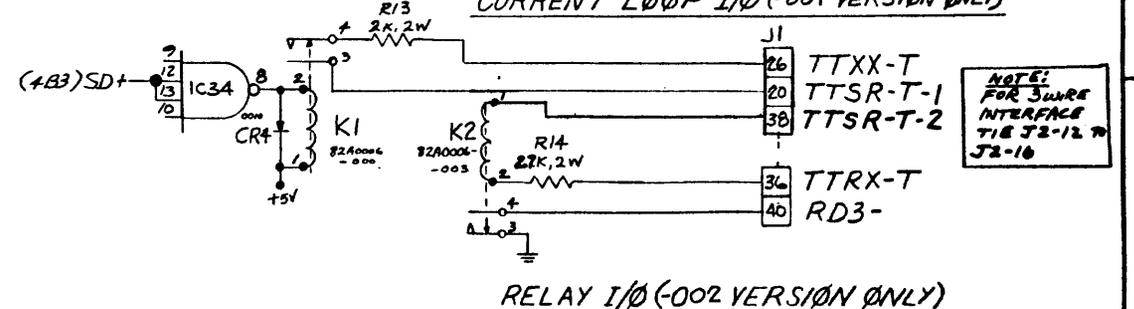
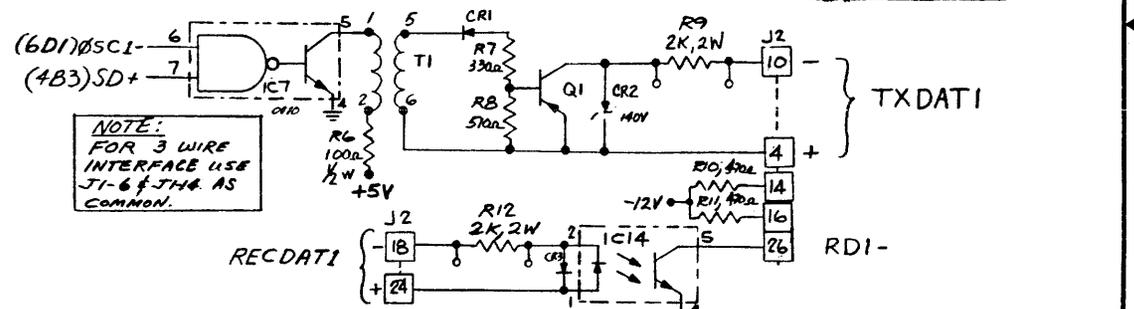
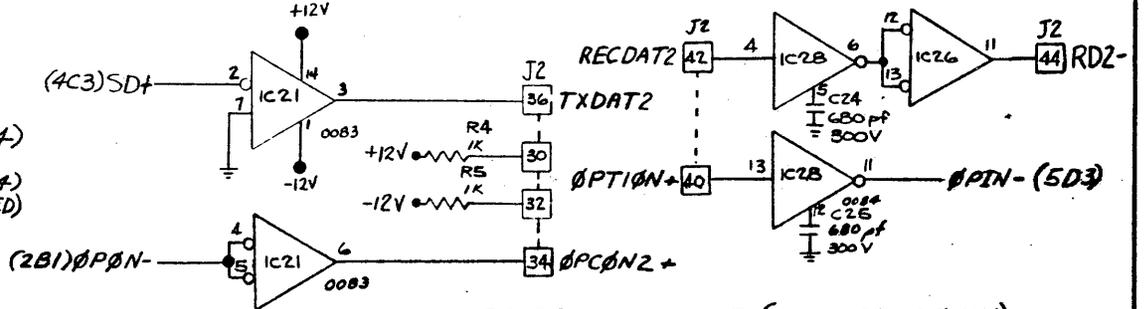
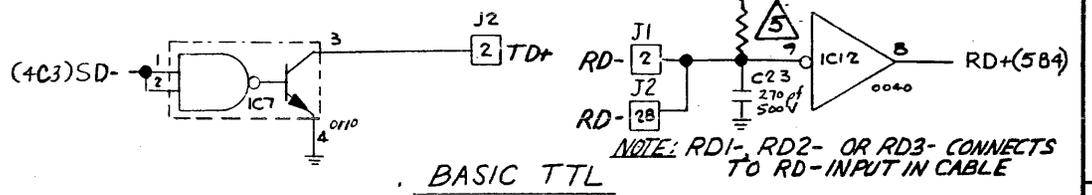
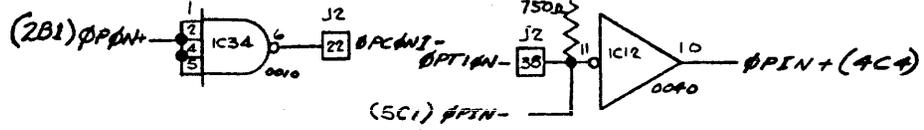
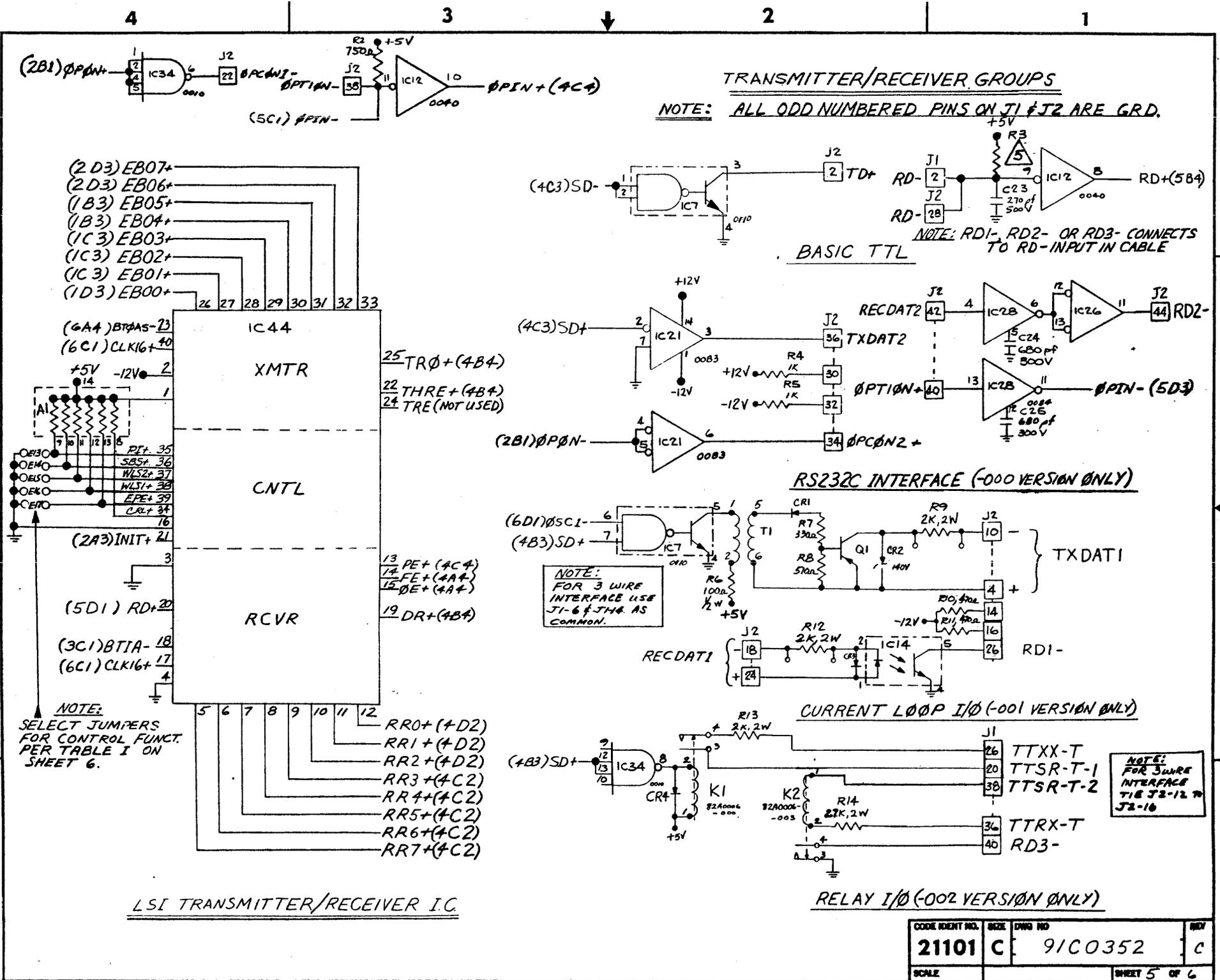
BIC CONTROL

INTERRUPT CONTROLS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0352	C
SCALE	SHEET 3 OF 6		

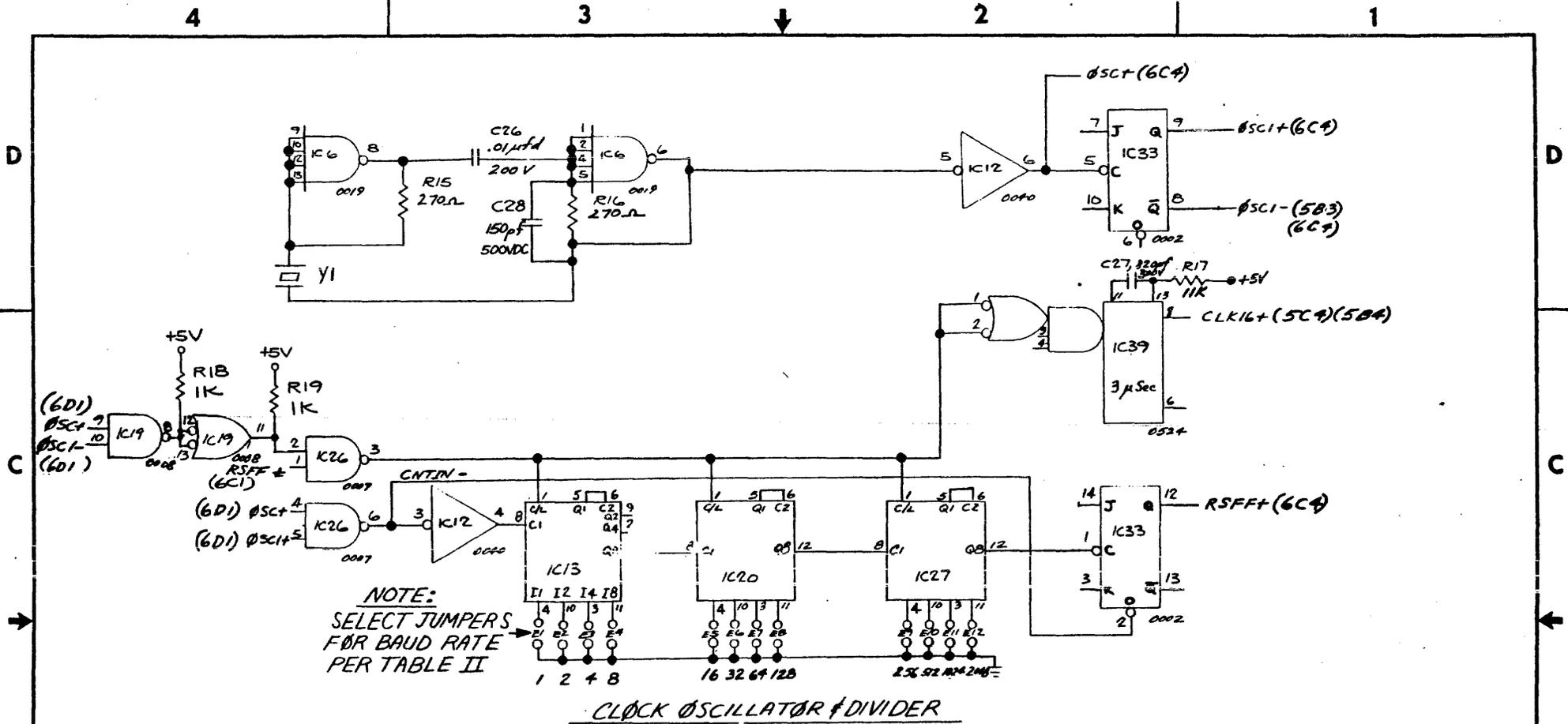


CODE IDENT NO.	SIZE	DATE	REV
21101	C	91C0352	C
SCALE		SHEET 4 OF 6	



**NOTE:**  
SELECT JUMPERS FOR CONTROL FUNCT. PER TABLE I ON SHEET 6.

CODE IDENT NO.	SIZE	DWG NO.	REV.
21101	C	91C0352	C
SCALE	SHEET 5 OF 6		



**NOTE:**  
 SELECT JUMPERS  
 FOR BAUD RATE  
 PER TABLE II

**CLOCK OSCILLATOR & DIVIDER**

**TABLE I**

JUMPER	IN	OUT
E13	PARITY	NO PARITY
E14	1 STOP BIT	2 STOP BITS
E17	ODD PARITY	EVEN PARITY
E15 } E16 }	5 DATA BITS	8 DATA BITS
E15	6 DATA BITS (IF E16 OUT)	
E16	7 DATA BITS (IF E15 OUT)	

REFER TO CONTROL FUNCTIONS  
 @ 5C4 FOR INSTALLATION

**TABLE II**

BAUD RATE	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12
9600		X	X	X								
4800	X		X	X	X							
2400	X	X		X	X	X						
2000	X	X	X				X					
1800	X	X	X	X			X					
1200	X	X	X	X	X	X						
600	X	X	X	X	X	X	X	X				
300	X	X	X	X	X	X	X	X	X			
150	X	X	X	X	X	X		X	X	X		
110			X	X	X				X	X	X	
75	X	X	X	X	X	X	X		X	X	X	
45	X	X	X	X	X	X	X			X	X	X

INSTALL JUMPERS MARKED "X" FOR  
 BAUD RATE DESIRED

