WANG

3202

ARCHIVING CARTRIDGE TAPE DRIVE

Models:

2229
6529
2529V

Customer Engineering
Product Maintenance Manual

729-1184-A

PREFACE

This document is the Standard (STD) Maintenance Manual for the Wang Archiving Cartridge Tape Drive. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the Archiving Cartridge Tape Drive. It will be updated on a regular schedule.

Second Edition (October, 1983)

This edition of the Archiving Cartridge Tape Drive STD manual obsoletes document no. 729-1184. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Service Notices (PSN's) or subsequent editions.

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CHAPTER 1

INTRODUCTION

1.1 SCOPE & PURPOSE

This manual contains information necessary to unpack, install and maintain the Wang Archiving Cartridge Tape Drive (ACTD). Included is a functional block level theory of operation, installation instructions, maintenance information, schematic diagrams and troubleshooting information. With the aid of this manual the Wang Customer Engineer will be able to make all necessary cable connections, perform initial turn-on and system checkout, make necessary adjustments, analyze failures and troubleshoot faults down to the major component and board level and remove and replace major components.

1.2 APPLICABLE DOCUMENTS

The following documents contain additional information which would be helpful to those who install or use this product:

Title	Wang Part No.
Model 2229 Cartridge Tape Drive User Manual	700-7716
Model 6529 Cartridge Tape Drive User Manual	700-8071
VS Utilities Reference Manual	800-1303UT-02
Model 2529V User Summary Card	800-6212

The address for ordering the above documents follows:

Wang Laboratories, Inc.
Supplies Division
c/o Order Entry Dept., M/S 5511
51 Middlesex St.
No. Chelmsford, MA 01863

1.3 GENERAL DESCRIPTION

The Archiving Cartridge Tape Drive is a peripheral device that utilizes a 1/4 inch magnetic tape cartridge to store data. It is designed primarily as a slave processor to provide reliable backup for Wang systems having fixed disk drives. There are three stand-alone models available: Model 2229 for use with the 2200 system, Model 6529 for OIS systems and Model 2529V for VS systems.

The tape interface is made to the Kennedy Model 6455 quarter inch cartridge tape system. Models 6529 and 2529V contain their own data link logic for interface to a master, a central processing unit (CPU), memory, tape DMA controller, and interface electronics to the Kennedy tape drive. All this logic is located on a single board that is contained within the tape unit. Model 2229 uses a mother/daughter board arrangement located in the 2200 CPU for interface with the 2200 system in place of the logic board used in the other models.

1.4 SPECIFICATIONS

Tape	
Width	0.25 in. (0.64 cm)
Length	450 ft (137.16 m)
Recording	
Recording Density	6400 bpi
Physical Tracks	4
Formatted Capacity	Up to 15 mb with 450 ft tape
Record Format	Single Track, serial
Tape Transport	
Tape Speed (Normal)	30 ips
Tape Speed (Rewind)	70 ips
Read Operation	Serial/Serpentine (see Figure 1-1)
Write Operation	Serial/Serpentine
Start/Stop Time	
Read/Write Operations	25 ms
Rewind/Search Operations	75 ms
Start/Stop Displacement	
Read/Write Operations	0.38 in. (0.97 cm)
Rewind/Search Operations	3.38 in. (8.59 cm)
Tape Head	
Recording Head	Serpentine Read after Write Selective Erase
Data Transfer Rate (drive to controller)	192,000 bits per second 24,000 bytes per second
Dimensions	
Height	6.69 in. (16.99 cm)
Width	15.38 in. (37.07 cm)
Depth	17.81 in. (45.24 cm)
Weight	28.5 lbs (12.96 kg)
Cables	
Model 2229	10 ft (3.05 m) parallel cable from Tape Drive to CPU
Models 2529V, 6529	25 ft (7.6 m) dual coaxial cable from Tape Drive to CPU (optional lengths up to 2000 ft (609.6 m)
Fuses	2 amp. @ 115V 1 amp. @ 230V

SPECIFICATIONS (continued)

Operating Environment	
Temperature	50°F to 90°F (20° C to 32° C)
Relative Humidity	35% to 65% noncondensing (recommended) 20% to 80% noncondensing (allowable)
Power Requirements	115Vac (98V to 128V allowable), 50/60 Hz 1.4 amp. to 2 amp. @ 115V 220Vac (196V to 256V allowable), 50/60 Hz 0.7 amp. to 1 amp. @ 220V
Controls	Power On/Off On-Line
Indicators	Power On On-Line Fault Tape Loaded

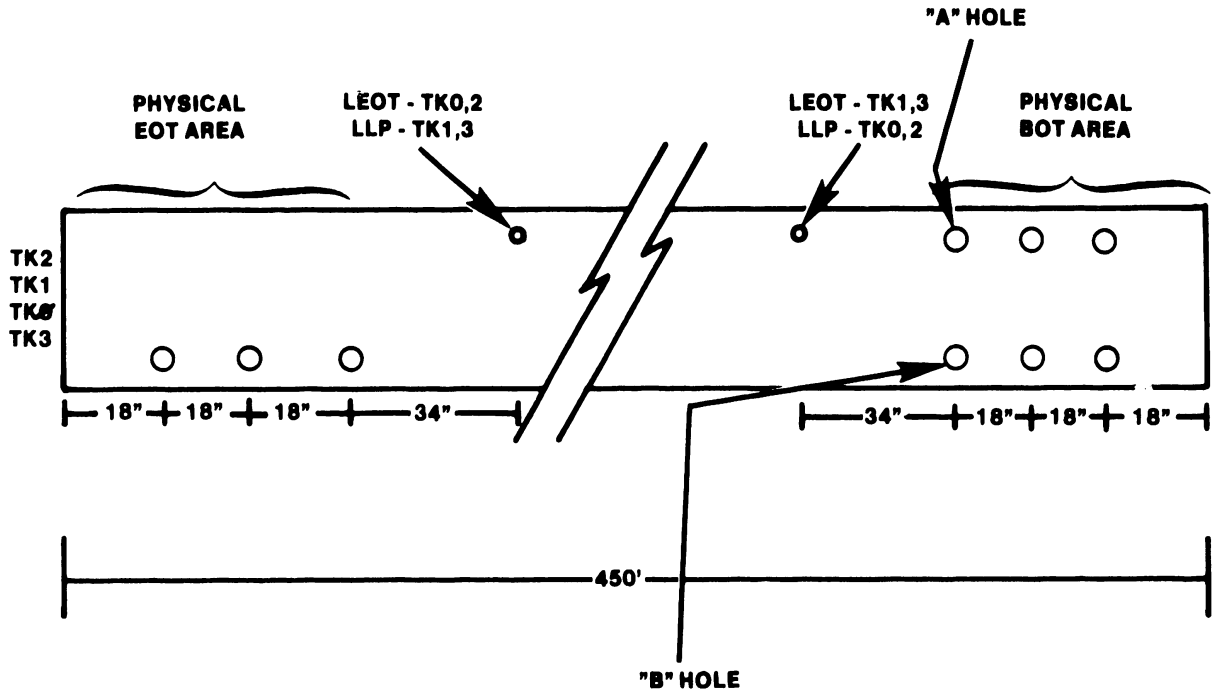


Figure 1-1 EOT/BOT Areas on Serial Serpentine Recorded Tape

CHAPTER 2

THEORY OF OPERATION

CHAPTER 2

THEORY OF OPERATION

2.1 INTRODUCTION

This chapter provides a functional description of the circuitry on the OIS/VS Interface board (210-8262A) used with Models 6529/2529V, the Mother board (210-8260) and Daughter board (210-8259) used with Model 2229 and the Regulator board (210-7770) used on all models.

2.2 THE OIS/VS INTERFACE BOARD

The OIS/VS Interface Board (210-8262) acts as an interface between a Kennedy 6455 or 6470 quarter-inch cartridge tape system and a Wang OIS or VS master, providing high density tape backup for 8 inch and 14 inch Winchester disk drives. It comprises seven major functional blocks: Z80A Central Processor Unit, Z8410 Direct Memory Access Controller, Z80-CTC Counter Timer Chip, Data Link, Memory (64k bytes of RAM and 4k bytes of PROM), and Tape Interface (see Figure 2-1). Information is received and transmitted from the 8262 board serially via the standard dual coaxial cable. Normally in the receive mode, the 8262 can transmit only under master control.

A 4 mHz Z80A CPU is the main processor, with a 16-bit unidirectional address bus, an 8-bit bidirectional data bus, and several control lines. Since the CPU is capable of driving only one TTL load, all address, data, and control lines are buffered by buffer/drivers. The control lines carry information to and from the Z80A specifying the required operation. The wait control line tells the CPU to enter a wait state so that a CPU-independent action can occur. There are two kinds of interrupts; nonmaskable and maskable. When activated, the nonmaskable interrupt causes the CPU to trap automatically to location 66. The five maskable interrupts specify their own trap locations.

The CPU can provide a 7-bit dynamic RAM refresh address, making 128 memory row addresses available for refresh. The 8262, however, has 64k bytes of dynamic RAM memory and therefore requires 256 row addresses for refresh. The 256-row address refresh is accomplished by toggling the A7 Address Bit with a Refresh A7 Bit and multiplexing the Refresh A7 Bit into the row address. This procedure provides an additional address line and, therefore, the necessary 256 row addresses for refresh.

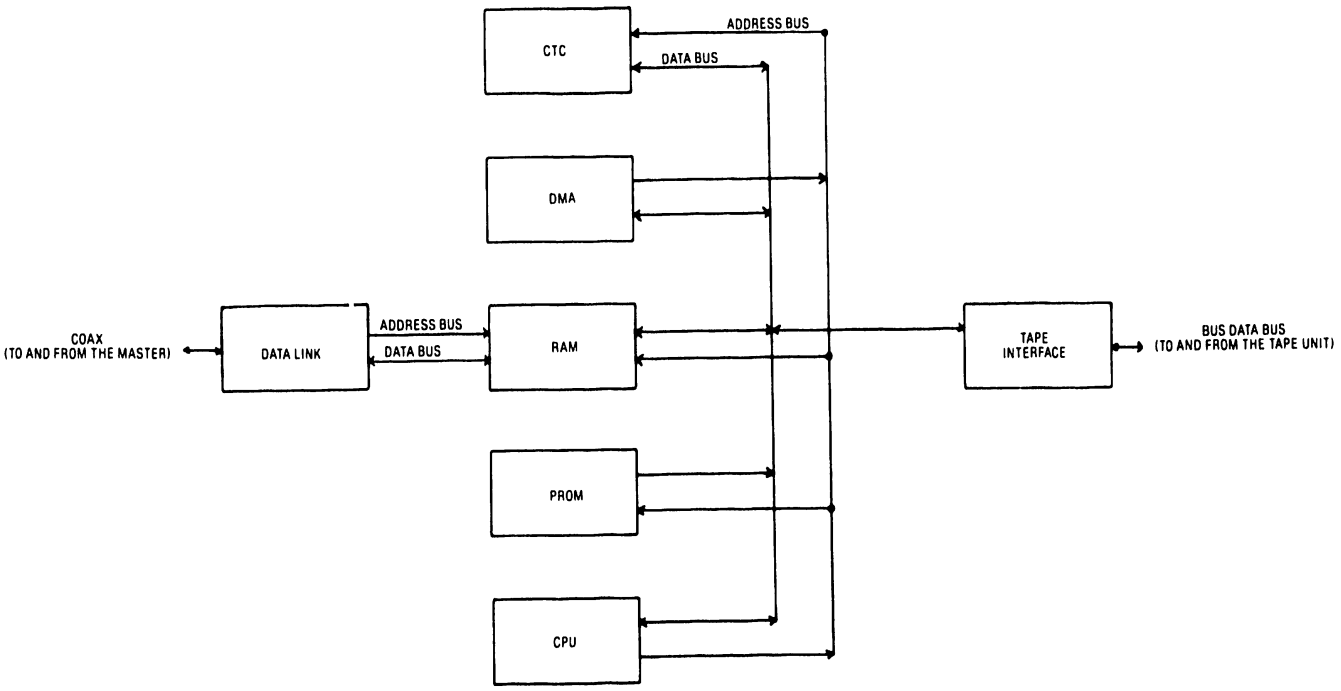


Figure 2-1 OIS/VS Interface Board Block Diagram. Data Link receives data from OIS or VS master via coaxial cable and transfers data and addresses directly to memory via DLDO and DMA buses. CPU, DMA, CTC, RAM, and PROM share D0-7 and D0-7B data buses. Data bus sends and receives data via tape interface, which transmits data to tape unit via /BUS data bus.

Data transfers to and from the tape unit are controlled by a Z8410 DMA Controller that contains a 16-bit address bus, an 8-bit data bus, and 13 control lines for external interfacing. The DMA Controller can generate independent addresses for Port A and Port B. Readable registers contain the current address of each port and a count of the number of bytes transferred. The Z8410 can be programmed via 21 writable control registers, and its status can be checked via seven readable status registers. When it is enabled and needs to transfer data, the Z8410 uses /BUSREQ, which requests the Z80A to relinquish the bus. At the end of the current CPU machine cycle, the CPU releases control of the bus to the Z8410 via /BUSACK, which asserts the DMA Controller. The Z8410 transfers a block of data in the byte transfer mode by transferring one byte and then releasing the bus until the next byte transfer is required. It also can be programmed to generate a maskable interrupt request at the end of a block transfer.

The Counter Timer Chip (CTC) generates and prioritizes Mode 2 maskable interrupts and provides a general purpose event timer. Channels 0, 1, and 3 are used in the counter mode to generate an interrupt for the first strobe pulse indicating that a specific event has occurred. Channel 2, driven by the system clock, is used in the timer mode and has a range of 4 us to 16.384 ms. It generates an interrupt request when the general purpose timer counts down to zero.

The Data Link is an asynchronous receiver/transmitter with a coaxial cable connection to the OIS master or VS serial IOP. It receives serial data from the master, checks data parity, and then assembles the data into a parallel (byte) format. It attaches to an 8-bit data bus and a 16-bit address bus, both of which are routed directly to RAM. The Data Link is normally in the receive mode, waiting for a start bit from the master. The start bit is always followed by an instruction telling the slave what type of operation will follow. The Data Link is transparent to the slave and, therefore, is not tested by the slave's power-up diagnostics.

There are 64k bytes of RAM resident on the 8262 as well as all the timing, multiplexing, refresh, and sequence logic required to interface to the RAM chips. Basically, the 8262 always performs a 256-row refresh regardless of the type of RAM loaded. Parity generation and checking are performed on all CPU memory cycles to check the integrity of data coming from memory. Limited application of power resets the parity generator/checker to even parity by default. The Z80A CPU and the Data Link must access the single-port memory concurrently. A pseudo cycle stealing scheme provides DMA access to memory: the DMA controller accesses memory via the Z80A's memory interface by disabling the Z80A through a Bus Request/Bus Acknowledge cycle.

Four kbytes of PROM contain the power-up diagnostic software. At power on, the CPU is reset to location 0000, the diagnostic PROM shadows the first 4k bytes of addressable CPU memory space, and the Data Link Receiver is disabled. The diagnostic PROM contains all the programs and data needed to verify the correct operation of the 8262 board before the system master can perform Initial Program Load (IPL). The Data Link is transparent to the 8262 and, therefore, is not tested by the power-up diagnostics.

The 8262 interfaces to the Kennedy cartridge tape system via the Kennedy Pico Bus Interface. This interface consists of two separate Write Data Latches, two Read Data Latches, and a bidirectional 8-bit data bus that uses odd write and read parity bits, four handshaking control signals, a data strobe, and a cable interlock signal (Cable Monitor, CMON) that indicates whether the cable between the slave and tape unit is connected. The tape interface can be tested via diagnostic loopback tests without actually being connected to an active tape unit.

Switches resident on the SW2 board provide four device type bits in the Status Word that inform the master that it is communicating with the 8262. SW1 Device Class Switches define additional 8262 characteristics to the master. The 8262 board has its eight device type switches set to a value of 0AH for use with the Kennedy Model 6455 and to 0BH for use with the Model 6470. The switch inputs are placed on the D0-7B bus to be read by the /IN07 command, enabling a Switch Buffer.

Model 6455, a 4-track, 6400-bit/in (30/70-ips) unit, can store a maximum of 23M bytes of unformatted data. Model 6470, a 7-track, 10,000-bit/in (45/90-ips) unit, can store a maximum of 63M bytes of unformatted data. Upward tape read compatibility allows the 6470 to read tapes written by the 6455; the 6455, however, cannot read tapes written on the 6470. Specifications for both models are listed in Table 2-1. (Model 6470 has not yet been released; therefore, its specifications are subject to change.)

Table 2-1: Kennedy Model 6455/6470 Specifications

Specifications Identical For Both Models

Cartridge Type	3M Type DC300A (300 ft), DC300XL (450 ft), DC600A (600 ft) Isoelastic Data Cartridge
Recording Head	Serpentine, Read-After-Write, with Selective Erase
Record Format	Single-Track, Serial
Data Reliability	
- soft error rate	1 in 10^{10} bits
- hard error rate	1 in 10^{11} bits
Power Requirements	5 $\pm$ 0.25 Vdc at 3 A avg and 5 A pk 24 $\pm$ 4 Vdc at 1.5 A avg and 3 A pk
Interface	
- Slave CPU	Pico Bus, TTL low-true, 34-pin 3M flat
- Power	6-pin molex
- Write Current Select	3-pin molex

Table 2-1 (continued)

Specifications Unique To Each Model

	Model 6455	Model 6470
Unformatted Capacity		
- 300 ft	11.5M bytes	31.5M bytes
- 450 ft	17.3M bytes	47.25M bytes
- 600 ft	23.0M bytes	63.0M bytes
Recording Density	6400 bits/in	10,000 bits/in
Number of Tracks	4	7
Normal Tape Speed	30 ips	45 ips
Fast Tape Speed	70 ips	90 ips
Start/Stop Time	25 ms @ 30 ips 65 ms @ 70 ips	50 ms @ 45 ips 75 ms @ 90 ips
Data Transfer Rate	24k bytes/s 41.7 us/byte	56.25k bytes/s 17.8 us/byte
	Cannot read 6470 format	Can read either format

Since the 8262 sees only the data passing between itself and the master, and this data is not system dependent, it detects no difference between an OIS or VS system. An OIS system uses the tape drive strictly for archiving, whereas a VS system also uses it for file backup and restoration procedures. Both VS and OIS systems determine which device they are communicating with by reading a device code that identifies the device as the tape drive and also distinguishes the particular model of the tape drive. The master then loads the device with the appropriate software to bring the tape drive up and running. The tape drive is treated as a batch device, since it does not interact actively with the operator.

2.2.1 CONTROLS AND INDICATORS

Operator controls consist of an AC power switch and an ONLINE membrane switch, both located on the front panel. When the ONLINE switch is operated, a Switch Flip-flop issues the SWITCH signal which asserts the CTC trigger input. The CTC then generates a maskable interrupt request via channel 3. Once the ONLINE pushbutton is pressed, further switch interrupts are disabled until an /OUT00 command reenables the interrupt. To ensure that the switch is properly debounced, the 8262 waits 20 ms before issuing OUT00.

Front panel indicators consist of POWER ON, ONLINE, FAULT, and TAPE LOADED. Four ERROR indicators also located on the board are used to identify particular errors. Of the eight indicator LED's on the ACTD slave, seven are driven by the L51 LED Latch, which is controlled by data bits D0-5B, D7B, and the /OUT0D command. The eighth LED, the ONLINE indicator, goes on when the ONLINE switch is activated and stays on as long as the unit is online. The FAULT indicator indicates to the operator that a hardware error condition exists; the particular error is diagnosed according to the board resident error indicators. The TAPE LOADED light indicates that a tape cartridge is properly loaded. The tape cartridge should not be removed unless this indicator is OFF.

The POWER ON LED blinks on and off during execution of the PROM-resident power-up diagnostics until the /EP (Exit Prom) signal becomes active. At this time, the POWER ON LED comes on steadily, indicating successful completion of the power-up diagnostics. This indicator is not under CPU control; it is driven by the Power-On Monitor.

A speaker generates a beeping signal to alert the operator when the tape unit needs service or when a problem is encountered in the unit. When a 1-Shot receives the /OUT08 command, it issues a signal to activate a Timer (100 ms) which, in turn, generates the SPEAKER signal.

2.2.2 DATA LINK

The Data Link is basically a standard OIS data link that establishes bidirectional, half-duplex, asynchronous communication between interface board memory and an OIS master or VS serial IOP. At one end of the communication path, an 8-bit data bus and a 16-bit address bus carry bytes of parallel data to RAM. At the other end, serial data passes between the Data Link and the master along two coaxial cables. During receive operations, as shown in Figure 2-2, the Data Link accepts serial data from the master, assembles it into a parallel byte format, and stores it into memory. To transmit, as shown in Fig 2-3, the Data Link accepts parallel data from memory, converts it to serial format, and sends it to the master. The serial format for each byte provides a start bit, eight data bits, an odd parity bit, and a stop bit, in that order.

The Data Link responds to six commands from the master: a restart command, a status inquiry, two read commands, and two write commands. Upon receiving the 1-byte restart command code, it performs a hardware initialization sequence. In response to the 1-byte status command code, it returns a byte of device status information. Read and write commands require a 1-byte command code and a 2-byte data address. The Data Link can read or write either a single byte or a block of 256 consecutive bytes. The 2-byte data address is the address of the single byte or the address of the first byte in the 256-byte block. It follows the 1-byte command code, with its high-order byte first.

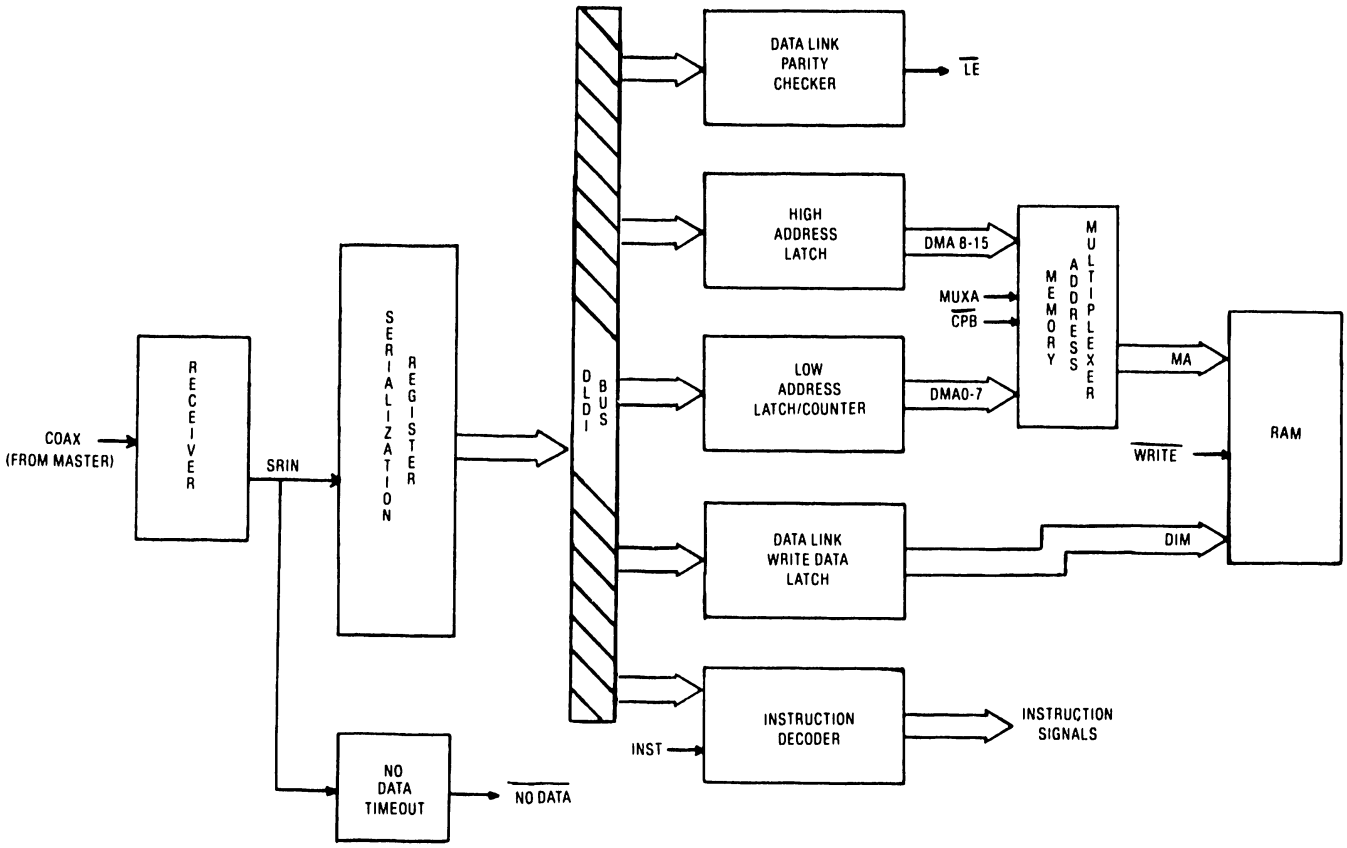


Figure 2-2 Data Link Receive Block Diagram. Serial data from master is received and arranged in parallel by Serialization Register. Input line is monitored by No Data Timeout logic. From DLDI bus, data is checked for parity and decoded to determine instruction. Address is routed to memory via Low and High Address Latches and Address Multiplexer. Data is routed to memory via Data Link Write Data Latch.

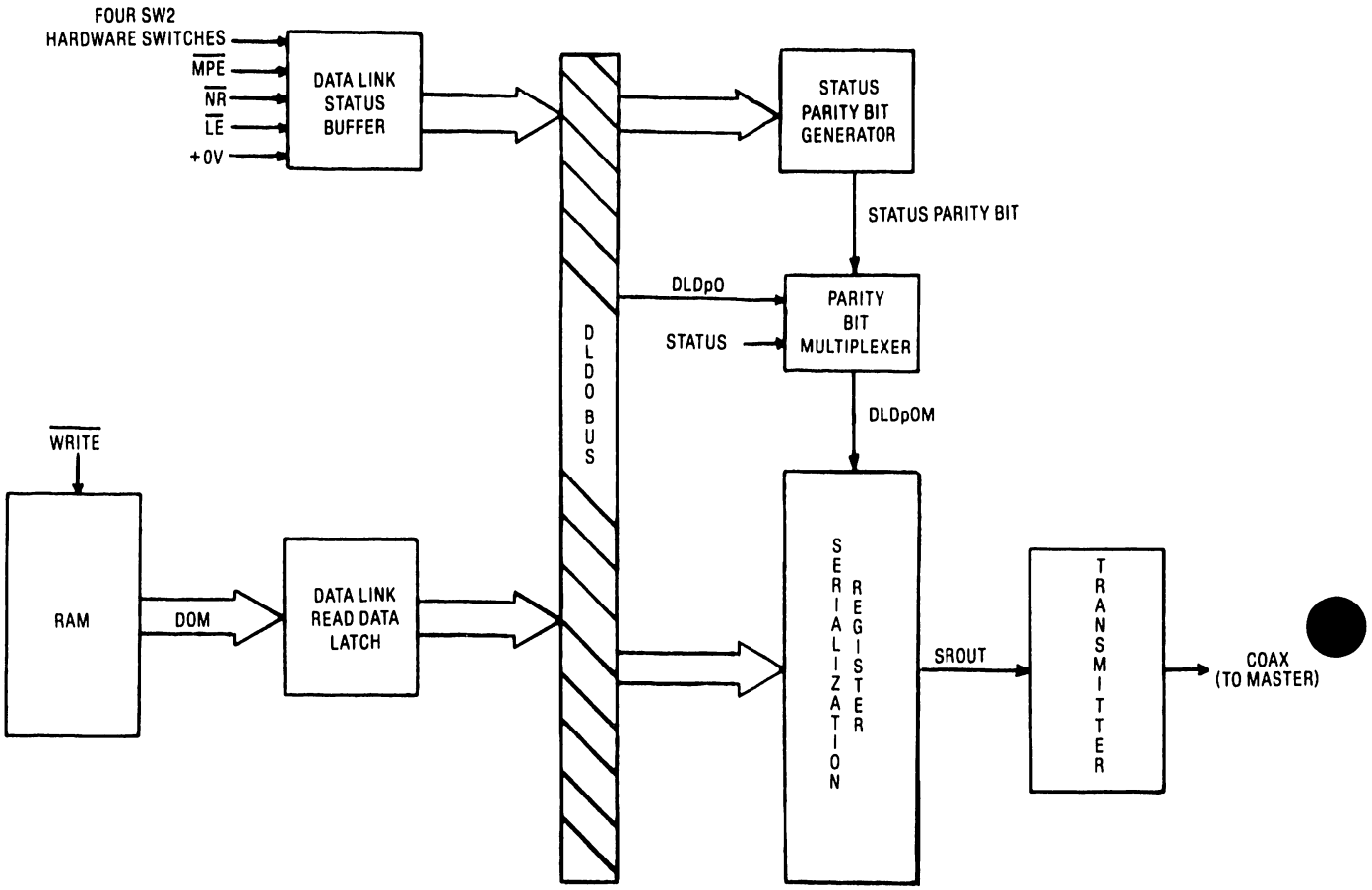


Figure 2-3 Data Link Transmit Block Diagram. Data Link Read Latch places data onto DLDO bus. Data is then passed to Serialization Register, where it is serialized and transmitted. Data Link Status Buffer is used for IN STATUS command only. Status Byte is read from Status Buffer onto DLDO bus. Status Parity Bit Generator provides parity bit, which is multiplexed into Serialization Register, for Status Byte.

The Data Link normally idles in its receive mode, awaiting a start bit from the master. Upon receipt of a start bit, the Data Link accepts and deciphers the 1-byte command code that follows. If the command is a read or write command, it also accepts a 2-byte address. It then executes the command, entering the transmit mode if the command is a write, and returns to the receive mode to await the next command. /LE, the Line Error signal, is generated when the Data Link detects bad parity within the received data. /LE is stored and can be read by the master using the STATUS instruction. STATUS also clears the stored line error condition, enabling the master to detect a line error and then retransmit. A line error prevents any data from being written to memory until the error can be cleared.

Receiver/Transmitter logic moves the serial data it receives between the master and the Serialization Register. The receiver/transmitter also converts data from serial differential data to serial data (Write) and vice versa (Read). The Serialization Register converts data from the receiver from serial to parallel format. Outgoing data is converted from parallel to serial format and sent to the Data Link Transmitter.

There are two unidirectional buses in the Data Link. The Data Link Data Input (DLDI) bus carries inbound data from the receiver to memory; the Data Link Data Output (DLDO) bus carries outbound data to the transmitter from memory or from the Status Buffer. Line Turnaround Delay logic generates a delay to prevent information collisions when the direction of information to or from the Data Link is changed.

2.2.3 Z80A CENTRAL PROCESSOR UNIT

A 4 mHz Z80A CPU is the main processor. At power-on, the processor is reset to begin power-up diagnostics from PROM. It defaults the PROM chip to memory address 0000 and disables the Data Link Receiver logic. When diagnostics are completed, an /OUT03 command enables the Data Link Receiver logic (making the controller visible to the master) and removes the PROM from the memory address space. A HALT instruction then places the CPU into a state in which only NOP instructions are executed. A RESTART command from the Data Link logic terminates NOP execution by resetting the processor, allowing it to begin program execution from memory address 0000. Figure 2-4 is a block diagram of CPU-associated logic.

The CPU has a 16-bit unidirectional address bus (A0-15), an 8-bit bidirectional data bus (D0-7), and several control lines. The address bus, the data bus, and some of the control lines are shared with the DMA Controller. All address, data, and control lines are buffered since the CPU is a MOS device capable of driving only one TTL load.

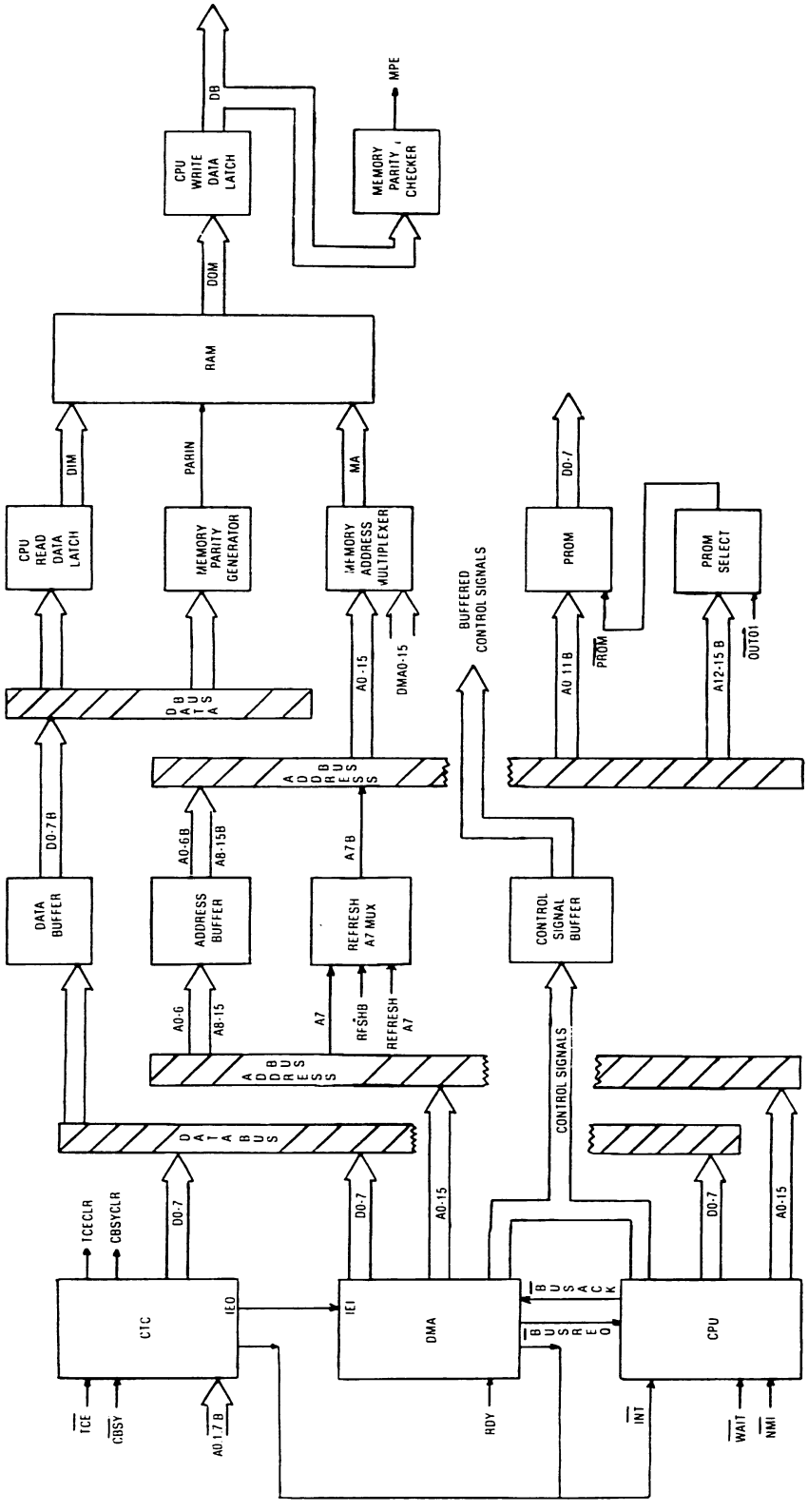


Figure 2-4 CPU, DMA, CTC, PROM and RAM Block Diagram

Referring to Figure 2-4, the CPU, DMA and PROM share address bus AO-15. DO-7 data bus is shared by CPU, DMA, CTC and PROM. Either CPU or DMA, whichever has bus control, issues operation control signals. RAM and PROM are accessed via buffered Address and Data Buses. Data is transferred to and from memory via CPU Read and Write Data Latches. Memory Address Multiplexer provides address. Memory Parity logic establishes and checks incoming data parity.

2.2.4 DIRECT MEMORY ACCESS LOGIC

The Z8410 Direct Memory Access (DMA) Controller contains a 16-bit address bus and an 8-bit data bus, and uses 11 of its 13 control lines in the controller application (see Figure 2-4). The DMA Controller transfers data to and from the tape unit and can generate independent addresses for Input and Output Ports. Twenty-one writable control registers are used to program the Z8410 and seven readable status registers contain the current address of each port and a count of the number of bytes transferred. OUTPUT to PORT 04H writes a command to the controller and INPUT to PORT 04H reads its status registers. Since no reset pin is available, the controller can be reset only via software.

Several of the control lines, as well as all of the address and data buses, are shared between the DMA and CPU. The DMA Controller has two unique control outputs, /BUSREQ and /INT, and five control outputs that it shares with the CPU: /M1, /RD, /WR, /IORQ, and /MREQ. The /M1 signal is active during op-code fetch cycles. The /RD signal goes active when a read operation is pending. When a write operation is pending, /WR goes active. When either the CPU or DMA makes an I/O operation request, /IORQ goes active. When a memory read or memory write is pending, /MREQ goes active.

/BUSREQ and /INT are the two control outputs unique to the DMA Controller. The /BUSREQ signal goes active on pin 15 when the controller requests bus control for a DMA transfer. The /INT signal goes active when the controller must interrupt the CPU.

The DMA Controller uses four unique control input signals: /BAI, /CE,/WAIT, /RDY, and IEI. (The /BAO and /IEO control pins are not used in the controller application.) When the controller obtains bus control, the CPU /BUSACK signal asserts /BAI. The /CE,/WAIT line has two uses: When the DMA Controller is not active, the /CE signal enables the controller; if the controller is already the bus master, a /WAIT signal causes a wait state when the Data Link needs bus access. When a data byte is ready for transfer, the RDY signal initiates the DMA Controller to begin the /BUSREQ-/BUSACK cycle to gain bus access. Since the DMA Controller has the highest priority among non-maskable interrupts, the Interrupt Enable Input (IEI) is tied high. The DMA disables the CTC interrupt by issueing a signal to disable CTC interrupts whenever the DMA has an active interrupt. CTC-generated interrupts have a lower priority than DMA-generated interrupts.

In the byte transfer mode, the DMA Controller transfers a block of data by transferring one byte and then releasing the bus until another byte transfer is required. In this manner, the CPU is disabled for 2.5 of every 41.7 us (Model 6455) or 2.5 of every 17.8 us (Model 6470). In the byte transfer mode, the byte counters are n-1 counters ("n" represents the tape record length); therefore, the smallest record must be at least 2 bytes long.

The DMA Controller Chip governs data transfers between the tape unit and memory. While the CPU is active, the Z8410 is disabled, with its tri-stated signals off the bus (in a high-impedance state). A RDY signal to controller pin 25 enables the controller to request bus control from the CPU. (During diagnostics, an output to PORT OFH generates the RDY signal.) A /BUSREQ signal notifies the CPU of the DMA's request for bus control. At the end of the current CPU machine cycle, the CPU releases control of the bus to the Z8410 via a /BUSACK signal.

The Z8410 is now the bus master, controlling the primary signals to achieve its data transfers. When it is through transferring data, the controller releases the bus and the CPU resumes program execution from where it left off. The Z8410 is programmed to generate a maskable interrupt at the end of a block transfer. Vectored interrupt XX08 notifies the CPU that the End-of-Block has been reached and all transfers have been completed.

2.2.5 COUNTER TIMER CHIP

The Z80A Counter Timer Chip is a programmable, 4-channel device that provides counting and timing functions for the controller. It includes an 8-bit data bus, eight control outputs, and 10 control inputs (including the clock input); three control outputs and the data bus are shared with the CPU and DMA (see Figure 2-4). The chip can be reset by /MR (Master Reset) or by a software reset command.

The Counter Timer Chip (CTC) prioritizes and generates Interrupt Mode 2 maskable interrupts and acts as a general purpose event timer. When the CTC issues an interrupt, it places a unique vector on the data bus to accompany the interrupt to the CPU. This vector combines with information programmed in the CPU's Instruction (I) Register to provide a pointer to a table. The table contains a list of interrupt service routine addresses that point the CPU to the proper service routine.

The CTC receives buffered Address Bits A0B, A1B, and A7B. A0B and A1B provide the CS0 and CS1 (Channel Selection) signals that select one of the four CTC channels to generate prioritized interrupts. A7B provides the /CE (Chip Enable) signal.

In the counter mode, Channels 0, 1 and 3 generate an interrupt upon the arrival of the first strobe pulse to indicate which particular event has occurred. Therefore, the CTC Down Counter for these channels must be set to 1. Four trigger inputs initiate the generation of prioritized outputs. TCE (Tape Command Error) activates trigger 0 to generate an interrupt signal plus output signal TCECLR (1-ms Tape Command Timeout/Tape Command Error). TCE indicates that either an invalid code or a code with bad parity was sent to the tape unit and TCECLR clears the tape operation. An inactive /CBSY (Command Busy) signal activates trigger 1, generating an interrupt signal plus output signal CBYSCLR. When /CBSY goes inactive (high), it indicates that the tape unit has successfully completed a command. CBSYCLR clears the tape operation. SWITCH indicates that the ONLINE switch has been activated on the slave control panel. It asserts trigger 3 to generate an ONLINE interrupt data code from the CTC's data pins.

Channel 2 has a range of 4 us to 16.384 ms and, since it is used in the timer mode off the 250 ns system clock, needs no trigger. It can be loaded with a prescaler that defines the number of clock pulses from 16 to 256 to be counted down before the CTC generates an interrupt at count = 0. The CPU can count these interrupts generated on Channel 2 to timeout long events such as searching for a File Mark. Channel 2 use is controlled entirely by software.

The /RD, /IORQ, and /M1 control outputs from the CTC are shared between the CPU and DMA. They allow a control word to be written to or a status word read from the CTC. /RD goes active on pin 6 when a read operation is pending, /IORQ on pin 10 is active when the CPU or DMA makes an I/O operation request, and /M1 is active on pin 14 during op-code fetch cycles.

The DMA Controller has the highest priority maskable interrupt. When the DMA has an interrupt, a signal to the CTC disables the CTC generated interrupts. Table 2-2 illustrates the established priority among all the maskable interrupts.

Table 2-2: MASKABLE INTERRUPTS

Priority	Type	Vector
1	Tape End of Block	XX08H
2	1-ms Tape Command Timeout/Tape Command Error.	XX00H
3	Tape Command Completion.	XX02H
4	CTC Channel 2 Timeout.	XX04H
5	ONLINE Switch Contact Closure	XX06H

2.2.6 MEMORY

2.2.6.1 Random Access Memory

The controller provides 64k bytes of onboard RAM as well as all the timing, multiplexing, refresh, and sequence logic necessary to interface this memory. To the CPU or the Data Link the RAM is basically a 2-port (input and output) memory. Therefore, the RAM cannot be accessed simultaneously (see Figure 2-5). The RAM chips require a 256-row address refresh (eight row address bits/4-ms refresh time). Refresh occurs when the memory receives both a refresh address on its address pins and a /RAS (Row Address Strobe) signal.

2.2.6.2 Power-Up Diagnostic PROM

When power is first applied, the CPU is reset to location 0000, the first 4k bytes of addressable CPU memory space default to the diagnostic PROM and the Data Link receiver is disabled. The diagnostic PROM contains all the programs and data needed to verify the correct operation of the cartridge tape slave before it can be accessed by the system master. When the PROM is selected by the upper four address bits (A12-15B), the lower 4k bytes of RAM are de-selected, causing the real RAM address space to begin at location 1000H.

Power-up diagnostic software on the controller board is contained in PROM. /POR (Power-On Reset) presets the PROM Select Flipflop, enabling the PROM to begin the diagnostic routine. A /PROM signal is then generated via the logic and this signal enables the PROM.

/RDB and /PROM MREQ (Buffered CPU Memory Read and CPU PROM Memory Request) combine to create a signal that asserts the Output Enable (/OE),thereby enabling the outputs of the diagnostic PROM. /RDB must be active while the PROM is being read, and /PROM MREQ ensures that the PROM is selected and a memory request has been made.

For the diagnostic program to test the lower 4k bytes of RAM, the diagnostic program in PROM is de-selected from the lower 4k bytes of RAM and loaded into the next higher 4k bytes. PROM maintains control of the diagnostic program as the software is loaded into RAM. The PROM is de-selected after the move and diagnosis of the lower 4k bytes of RAM proceeds. During diagnostic testing, PROM is enabled and disabled by a ported output to the PROM Enable logic.

The PROM Select Flipflop handles PROM selection and de-selection: an /OUT01 command and the D7B bit select and de-select the PROM as required. When power is applied, PROM diagnostic routines are located in the lower 4k bytes of RAM. (The lower 4k bytes of RAM are de-selected.) To diagnose the lower 4k bytes of RAM, the /OUT01 command de-selects the PROM when D7B goes low. PROM then loads the diagnostic program code into RAM. The PROM is de-selected, and diagnostics continue via the diagnostic program in the upper RAM. When diagnostics are completed, the PROM is again selected.

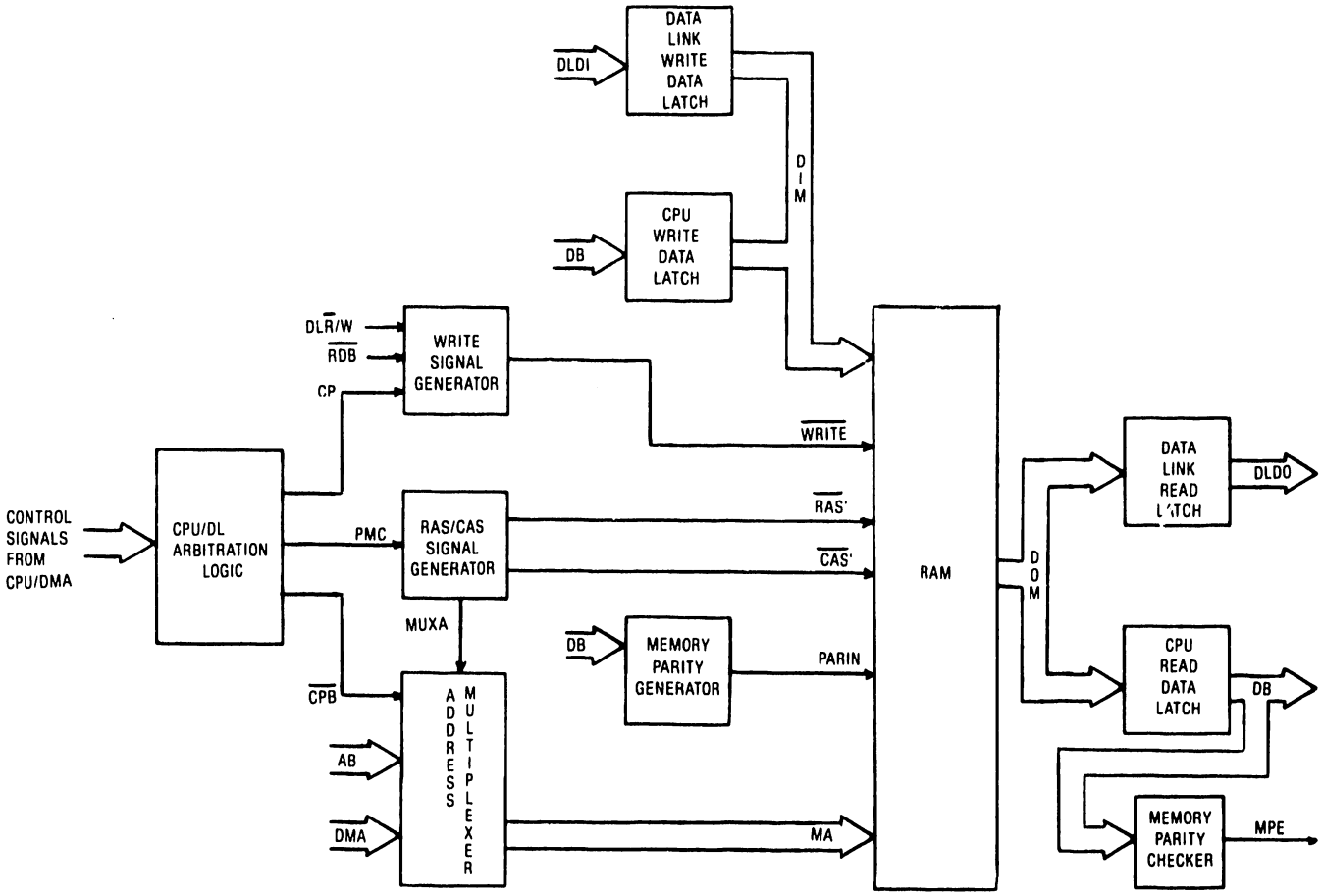


Figure 2-5 Block Diagram of Data Paths To and From RAM. When memory is written, it receives data and parity bits from DIM bus; when it is read, data and parity bits are transmitted out via DOM bus. CPU and Data Link maintain separate routes to and from RAM; there are two data paths into DIM bus and two from DOM bus. Sixteen-bit address used in read or write operations is sent to memory in two address bytes. Four-to-one Memory Address Multiplexer connects either low or high address byte of AB or DMA Address Bus with Memory Address Bus (MA0-7).

The POWER UP indicator on the front panel flashes throughout diagnostic testing. When diagnostics are completed, the I/O Decoder issues an /OUT03 command to turn the POWER ON light on continuously, de-select the PROM from memory space, enable the Data Link Receiver and force a HALT onto the bus to halt the CPU. If the diagnostics fail, the Data Link Receiver will not be enabled. Instead, the FAULT light will be go on and an error code will be issued to the Error LEDs. Fifteen error conditions can be represented in the Error LEDs (see TAble 8-1).

2.2.7 TAPE INTERFACE

The controller provides an interface to Kennedy Model 6455 and 6470 Cartridge Tape Units, both of which consist of a cartridge formatter and a tape drive. The formatter controls read and write operations in a self-clocking mode complete with serial error detection (CRC). It executes 19 commands, including generation of file marks and space one record in either forward or reverse direction.

Interface to the tape unit is provided by the Kennedy Pico Bus Interface which consists of a bidirectional 8-bit data bus using odd parity, write and read parity bits, four handshaking control signals, a data strobe and a cable monitor signal. Any information sent to the controller begins with a command and is followed either by data or the tape unit's response to the command. The tape unit determines whether it is receiving a command or data when it receives either CREQ (Command Request) or DRDY (Data Ready). /CMON (Cable Monitor) indicates whether the cable between the slave and tape unit is connected. When the cable is disconnected, /CMON is high.

The slave CPU initiates all transfers to and from the controller by issuing one of 19 possible commands. /OUT06 sets the Command Request (CREQ) control signal and, after a time delay, the controller responds with CBSY (Command Busy). CBSY remains active until the tape unit is through processing the present command. Commands must NOT be sent while CBSY is active. The controller's course of action after CBSY is set depends upon the particular command. It can return one or two status bytes and latch them into separate registers, it can write a track address to the tape unit, or it can transfer tape read or write data. Fig 2-6 displays a block diagram of the control signal generating logic. Fig 2-7 and 2-8 display block diagrams of the Tape Interface receive and transmit data paths.

During tape data read or write operations, an /IN05 or /OUT05 command sets Data Ready (DRDY), a control signal which is acknowledged by Data Busy (DBSY). The actual data transfer does not take place until DBSY goes active. /OUT05 also latches the next byte of data to be written to the tape unit. /IN05 reads the tape read data latch. Each byte of data (whether command, status, or data) is either clocked in by or acknowledged by a STROBE signal from the tape unit.

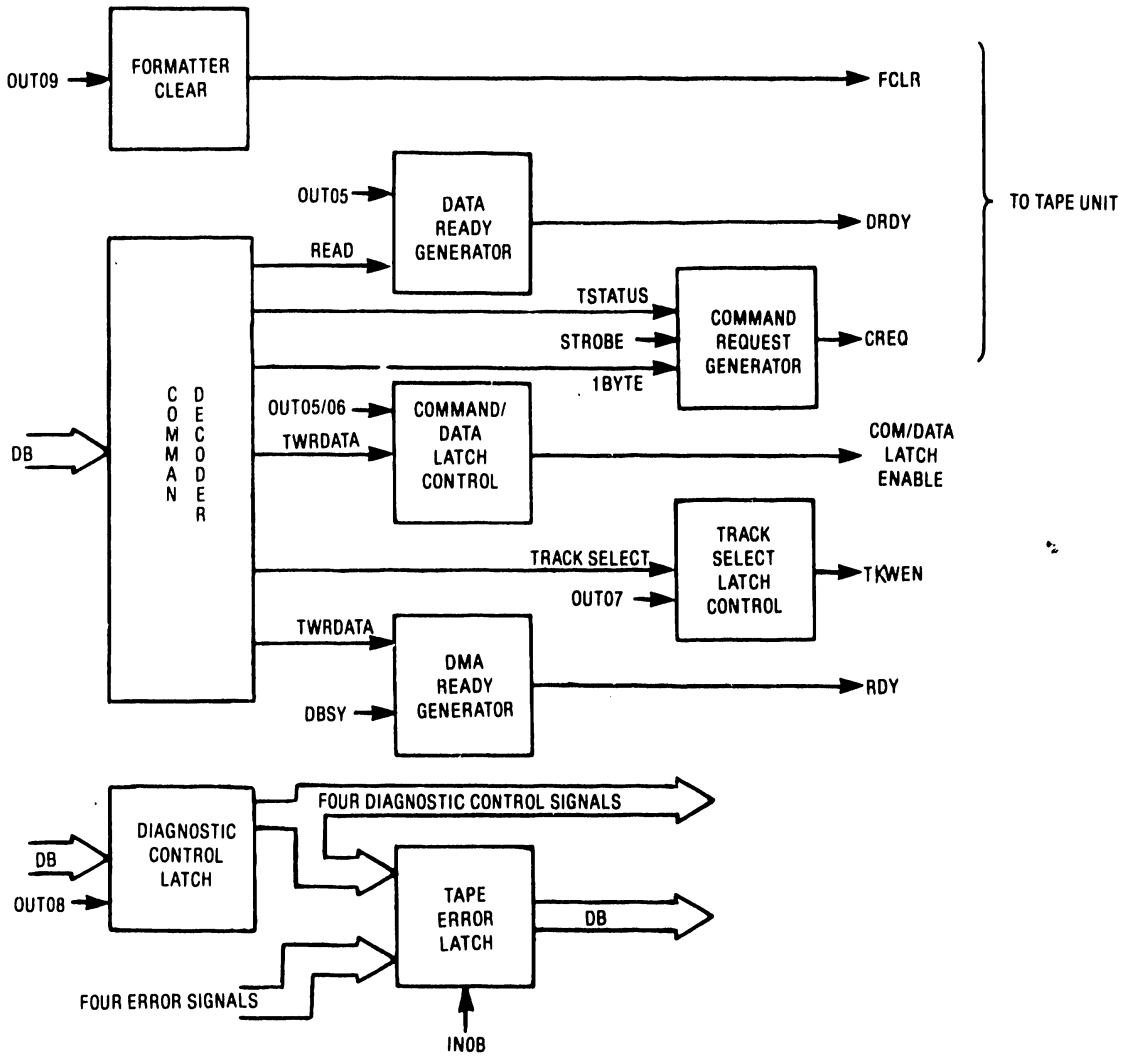


Figure 2-6 Tape Interface Control Block Diagram. Control signals for tape unit-tape interface interaction are generated by Tape Interface Command Decoder and associated logic. Logic decodes commands to issue appropriate control signals to tape unit and within the controller. Diagnostics Control Latch issues signals to control testing of the controller. Formatter Clear logic issues FCLR to clear tape unit via /OUT04 command.

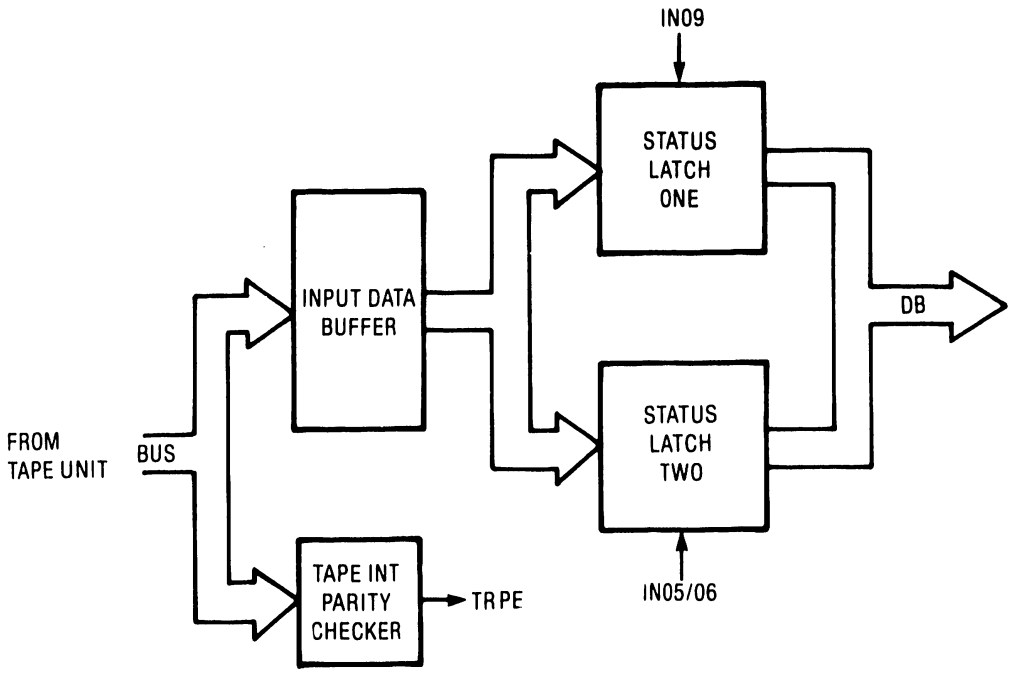


Figure 2-7 Tape Interface Receive Data Path Block Diagram. Data is read from memory into Input Data Buffer and through to Status Latches. All single-byte command data is read through Status Latch Two. Status Latch One is used only for SENSE STATUS Command where two bytes of data are requested. Data is passed from Status Latch to DB Data Bus upon receipt of ported input commands.

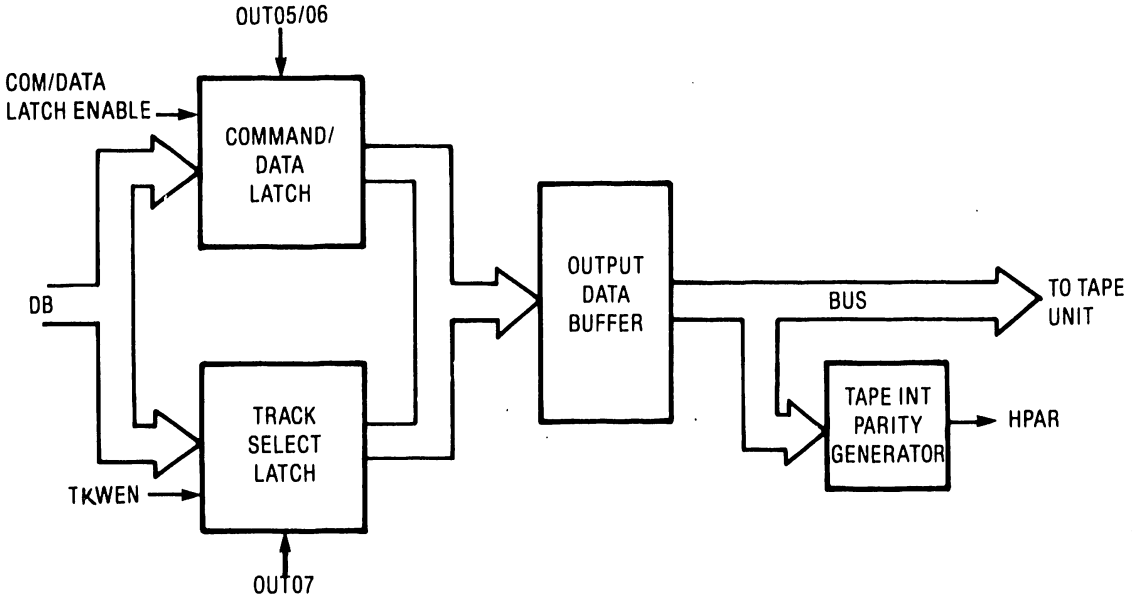


Figure 2-8 Tape Interface Transmit Data Path Block Diagram. Data from DB Data Bus is passed into Command/Data or Track Select Latch. Data is sent to tape unit in appropriate sequence via Output Data Buffer. Control of this operation depends on signals generated from Tape Interface Control logic. See Figure 2-6.

2.2.7.1 Tape Commands

Tape commands are performed by an /OUT06 command with data set to the corresponding function code. Model 6455 has 19 valid function codes in the range of 00-12H. All other function codes are illegal and result in Command Errors. Table 2-3 lists current function codes. (Additional function codes will support Model 6470.)

All motion commands used by the Model 6455 can take advantage of the command "on the fly" feature available in the drive formatter software. When the same command is executed within 300 us of the Command Completion interrupt (CBSY goes off), the new command is executed without the drive beginning its standard ramp to a stop procedure. As a result, command execution overhead delay is reduced from 50 ms (25 ms to ramp down plus 25 ms to ramp back up) to 25 ms. The command "on the fly" does a standard ramp to a stop if the next command is in the opposite direction.

Table 2-3 Command Function Codes

CODE 00H - SENSE IDENTITY. Requests an identity byte from the tape unit. A value of 01H identifies the device as a cartridge tape unit. After the Command Completion interrupt, /IN06 reads the identity byte.

CODE 01H - SENSE CONFIGURATION. Requests a Software Revision Level Byte from the tape unit. After the Command Completion interrupt, /IN06 reads the Software Revision Level Byte. The present value of the Software Revision Level Byte is 0AH.

CODE 02H - SENSE STATUS. Requests two status bytes from the tape unit. After the Command Completion interrupt, /IN09 reads the first status byte (Summary Status) and /IN06 reads the second status byte (Position Status). The tape unit resets the Error Status Bits after status has been sensed.

CODE 03H - REWIND. Causes tape unit to rewind at maximum speed (70 ips) and position the tape at the Logical Load Point (LLP) of Track 0.

CODE 04H - LOAD. Loads a tape cartridge into the tape unit. After the operator inserts the tape cartridge into the tape unit, Summary Status Bit 5 (No Cartridge) goes false to indicate proper insertion. Summary Status Bit 7 (Not Ready) remains active until the LOAD operation is successfully completed. Prior to execution of the LOAD sequence, the tape unit performs a self-test of formatter electronics. Successful completion of this self-test is required to proceed; otherwise, Summary Status Bit 4 (Formatter Error) is set. Finally, the tape is positioned at the Logical Load Point (Track 0) of the tape cartridge.

Table 2-3 Command Function Codes (continued)

CODE 05H - UNLOAD. Causes tape unit to rewind at maximum speed (70 ips) and position the tape at End of Tape (EOT). Summary Status Bit 7 (Not Ready) goes active upon successful completion of the UNLOAD operation, allowing proper removal of the tape cartridge.

CODE 06H - TRACK SELECT. In combination with Track Address/Placement Byte, causes tape unit to select the indicated track and reposition the tape to the Logical Load Point or Logical End of Tape (LEOT) at maximum tape speed (90 ips). Before TRACK SELECT is executed, /OUT07 must be issued to write the Track Address/Placement Byte Register.

CODE 07H - ERASE. Causes tape unit to erase tape in the forward direction at maximum tape speed (70 ips). Tape unit senses the Logical End of Tape and stops automatically.

Code 08H - SPACE FORWARD. Causes tape drive to proceed forward from an Inter-Block Gap (IBG) to the next IBG at normal speed. One record on tape is traversed. SPACE FORWARD is constrained to the current track address.

(In the special case in which records are written past the LEOT of track 3, the READ command must be used to move beyond the LEOT.)

CODE 09H - SPACE REVERSE. Causes tape drive to proceed in the reverse direction from an Inter-Block Gap (IBG) to the previous IBG at normal speed. One record on tape is traversed. SPACE REVERSE is constrained to the current track address.

CODE 0AH - SPACE FORWARD FM. Causes tape drive to proceed forward from an IBG at normal speed until it senses a File Mark (FM) record. The drive then ramps to a stop in the IBG following the File Mark. The Position Status Byte indicates that the File Mark has been found. If the drive does not find a File Mark record, it stops at the Logical End of Track. SPACE FORWARD is constrained to the current track address.

(For the special case in which a File Mark is written past the LEOT of track 3, the Read command must be used to move beyond the LEOT.)

CODE 0BH - SPACE REVERSE FM. Causes tape drive to proceed from an IBG in the reverse direction at normal speed until it senses a File Mark record. The drive then ramps to a stop in the IBG following the File Mark. The Position Status Byte indicates that a File Mark has been found. If no File Mark is found, the drive stops at the Logical Load Point. SPACE REVERSE is constrained to the current track address.

CODE 0CH - READ. Causes the tape unit to read one tape record in the forward direction. Before READ is issued, the DMA Controller Chip must be programmed and enabled. It then issues an /IN05 command that reads in data from the tape and transfers it to memory. The tape unit checks the integrity of the data as it is read off the tape via a CRC check and indicates a Data Error in bit 0 of the Summary Status Byte.

Table 2-3 Command Function Codes (continued)

To read a partial record or if the record being read is longer than anticipated (data overrun), the read byte counter in the DMA Controller Chip must be set to the desired record length (which must be greater than 1). When the read operation occurs, the DMA Controller Chip inputs into memory only the number of bytes programmed into the byte counter. The tape unit, however, continues the read operation until the record has been read completely. When the tape unit has read the entire record, it sets the Tape Command Completion interrupt and the Tape Data Overrun Error Bit (D6), which can be read via an /INOB command). No error condition is indicated in the Summary Status Byte.

When a data underrun situation occurs (in which the length of the record being read is less than that programmed in the read byte counter in the DMA Controller Chip), the read operation terminates normally with no error conditions set in the Summary Status Byte. However, the byte counter in the DMA Controller Chip indicates that less than the desired length has been transferred.

CODE 0DH - WRITE. Causes tape unit to write one tape record in the forward direction with standard IBGs. Before WRITE is issued, the DMA Controller Chip must be programmed and enabled. It then issues the /OUT05 command which reads in data from memory and transfers it to the tape unit. The tape unit performs a read-after-write as the record is written and indicates any data errors in bit 0 of the Summary Status Byte. If the record being written is longer than 17k bytes, the tape unit terminates the operation at 17k bytes and sets the Length Error Bit in the Summary Status Byte.

Any attempt to issue a write command past the LEOT of track 0, 1, or 2 asserts the Command Error Bit in the Summary Status Byte. Records can be written past the LEOT of track 3. However, if the record is written past the physical EOT, the tape unit terminates the operation and sets the Drive Fault Error Bit in the Summary Status Byte.

Before a WRITE is attempted, the Write Protect Bit of the Position Status Byte must be checked. The Command Error Bit of the Summary Status Byte will be set if the tape cartridge is Write Protected.

CODE 0EH - WRITE EXTENDED. Causes tape unit to erase approximately three inches on the tape prior to writing the tape record. This procedure lowers the risk of encountering a physical failure area on the tape that may have caused a Data Error when a previous WRITE was attempted. WRITE EXTENDED should be used after a WRITE operation with a read-after-write error and a subsequent SPACE REVERSE command. This function assumes that blank tape exits beyond the record being written.

The Command Error and LEOT bits of the Status Byte will be set, preventing WRITE EXTENDED from being used when the record to be rewritten had passed the LEOT of track 0, 1, or 2.

Table 2-3 Command Function Codes (continued)

WRITE EXTENDED can write records past the LEOT of track 3. However, if the record is written past the physical EOT, the tape unit terminates the operation and sets the Drive Fault Error Bit in the Summary Status Byte.

NOTE

WRITE EXTENDED should not be used for tape editing as loss of position will result.

CODE 0FH - WRITE FM. Causes tape unit to write a special coded field on the tape to be used as a tape File Mark (FM). Standard IBGs will be placed on either side of the FM.

WRITE FM has the same restrictions as WRITE when it encounters an LEOT.

CODE 10H - WRITE FM EXTENDED. Causes tape unit to erase approximately three inches on the tape prior to writing the File Mark. This procedure lowers the risk of encountering a physical failure area on the tape that may have caused a Data Error when a previous WRITE FM was attempted. WRITE FM EXTENDED should be used after a WRITE FM operation with a read-after-write error and a subsequent SPACE REVERSE command. WRITE FM EXTENDED assumes that blank tape exits beyond the record being written.

WRITE FM EXTENDED has the same restrictions as WRITE EXTENDED when it encounters an LEOT.

CODE 11H - EDIT. Allows the controller CPU to rewrite a previously written record on the tape. The tape must be positioned in the IBG before the record to be edited. EDIT causes the record to be rewritten in the same way as the WRITE command.

CODE 12H - FIXED THREE INCH ERASE. Erases a fixed three inches of tape. FIXED THREE INCH ERASE can be used to pass over bad spots in tape or to erase separate records on tape.

2.2.7.2 Status Latches

During tape read operations, a buffer inverts the tape unit's outgoing signals, which then proceed through the buffer to one of the two Status Byte Latches. In a SENSE STATUS Command, the first Status Byte (Summary Status) contains status information and the second Status Byte (Position Status) provides tape positional information. The Tape Command Sequencer routes the Summary Status Byte into Status Latch One and the Position Status Byte into Status Latch Two. The tape unit resets the error bits of the Summary Status Byte as it is read. Operations other then SENSE STATUS use only Status Latch Two.

To clock Status Latch Two, the STRB signal is asserted when a data/status word is read. Status Latch Two is enabled by either /IN05 (Read Tape Data) or /IN06 (Read Tape Status Byte 2).

To read the Summary Status Byte, a signal from the Tape Command Sequencer clocks Status Latch One. This clocking signal is generated by the second STRB signal as the command is passed through a gate. Receipt of /IN09 (Read Tape Status Byte 1) enables Status Latch One. (/IN09 is generated only during the SENSE STATUS command operation.) The last STRB signal is prevented from clocking Status Latch One.

Summary Status Byte and Positional Status Byte bit assignments that are read with the SENSE STATUS Command are shown in Tables 2-4 and 2-5.

Table 2-4 Summary Status Byte

D0	DE - Data Error	Tape record with either a CRC or format error has been detected during a read or write operation. Faulty erase also issues a Data Error.
D1	LE - Length Error	Tape record larger than 17k bytes (maximum record size) has been written to tape unit.
D2	PE - Parity Error	Tape unit has detected a receive parity error on a command, write data, or track address byte transferred during the last operation.
D3	CE - Command Error	Signals receipt of an illegal function code. Check for parity error (D2).
D4	FE - Formatter Error	Either formatter has failed its self-test or noise has been detected in a gap region during a write operation.
D5	NC - No Cartridge	Tape cartridge is not inserted in the cartridge tape drive.
D6	DF - Drive Fault	Either a physical or electrical fault has occurred in the tape unit, a tape is broken, or the tape has illegally gone beyond the physical end of tape.
D7	NR - Not Ready	Tape drive is not ready because a tape cartridge is not properly loaded.

Table 2-5 Positional Status Byte

D0	TKB0 - Track Bit 0	Track Address Bit 0 of presently selected track
D1	TKB1 - Track Bit 1	Track Address Bit 1 of presently selected track
D2	TKB2 - Track Bit 2	Track Address Bit 2 of presently selected track
D3	EOT - End of Tape	Indicates physical end of tape
D4	WP - Write Protect	Write protect plug on tape cartridge has been detected
D5	FM - File Mark	Special file mark record has been detected on tape
D6	LEOT - Logical End of Tape	Logical End of Tape has been detected
D7	LLP - Logical Load Point	Logical Load Point has been detected

2.3 THE 2200 INTERFACE ASSEMBLY

The 2200 Interface Assembly (WLI #212-3037) provides the interface between the Model 2229 Cartridge Tape Drive and the 2200 CPU. The assembly consists of a Motherboard (210-8260) and Daughterboard (210-8259).

The mother/daughterboard controller interface is plugged into the 2200 system and connected by cable to the Kennedy 1/4" tape drive. The controller contains a Z80A 4MHZ CPU, 64K of RAM with parity, 4K of PROM, Z80A CTC, 9517A-4 DMA, Z80A PIO, and interface logic. Figure 2-9 is a block diagram of the interface assembly circuitry.

PROM occupies the first 4K of memory addressing (0000-0FFF). The RAM occupies the upper 60K of RAM (1000-FFFF). Odd parity is maintained on the 60K array of RAM.

The DMA chip has a total of four transfer channels available. Two channels are dedicated to data transfers between the 2200 and the tape controller while the remaining two channels handle data transfers between the tape controller and the tape drive.

The PIO is used either with or without the DMA to handle command and data transfers between the tape controller and the 2200.

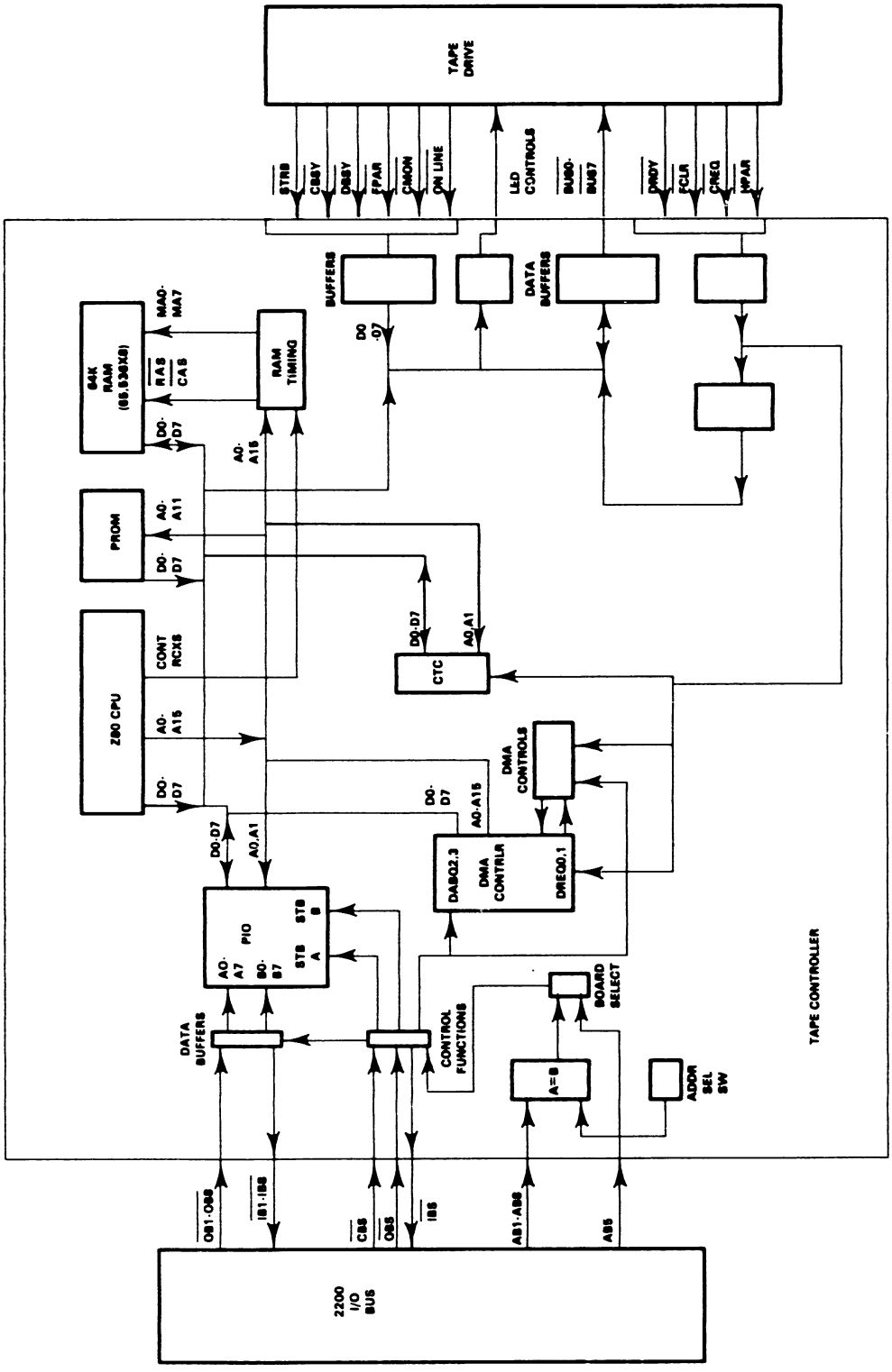


Figure 2-9 Block Diagram of 2200 Interface Assembly

2.3.1 2200/CONTROLLER INTERFACE

Communication between the 2200 and the controller is handled by the PIO. The PIO's A Port is dedicated to CBS byte transfers to the controller. Data transfers to and from the 2200 are handled through the B Port.

The Controller can use either of two methods to handle B Port data transfers to and from the 2200. In one method, the PIO is used to transfer data to the Z80 on an interrupt basis. In the second method, the PIO is used with the DMA to transfer bytes directly to RAM without interrupting the CPU until the end of the transfer.

When the controller receives a command byte which specifies the use of a block data transfer from the 2200, it can set up the DMA to handle the transfer. From that point the DMA chip will handle the block data transfer to or from the 2200 while the CPU is free for other processing. When the transfer is complete the DMA will interrupt the CPU.

2.3.1.1 Port B Data Transfers (DMA mode)

The PIO is used for a holding register during DMA transfers. The PIO receives the OBS strobe and latches the data. The Ready line from the B Port is used to generate a DMA transfer request. The DMA reads the PIO B port and moves the data to RAM. The PIO does not generate an interrupt of the CPU.

2.3.1.2 2200/Controller Data Transfers (Interrupt Mode)

In the interrupt mode, the A Port is set up for CBS characters and the B Port is used to interrupt the CPU when a byte is sent or received.

The CPU sets up the A port and enables interrupts on the A port only. The B Port is not allowed to interrupt the CPU until after being set up for the correct sequence.

2.3.2 TAPE INTERFACE

The Kennedy 6455 Tape Drive assembly consists of a Model 640 Tape Drive and a Model 650 Formatter. The Model 640 Tape drive is the mechanical tape transport and support electronics. The Model 650 Formatter is the microprocessor based electronics board to control the drive. The formatter handles the interfacing of signals and data between the host system and the tape drive system.

The tape drive configured for 2200 systems contains a small interface board (210-8261). This board supplies the power and ground signals for the front panel, separates the signals on the cable from the controller board into the group of signals going to and from the front panel and the tape drive. The board also contains the interface logic for the "On Line" Switch.

2.3.2.1 Control Signals

CREQ Signal -

The CREQ signal (Control Request) is used to indicate to the tape drive that a command or parameter byte transfer is being executed.

CBSY Signal -

The CBSY signal is used by the tape drive to indicate to the controller that the drive is executing a command sequence. This signal will remain active until completion of the command. In cases of one byte operations where no tape motion is involved, CBSY goes inactive shortly after STRB goes inactive. In cases where tape motion is involved, CBSY will not go inactive until after tape motion has stopped. This may be a time period of up to 90 seconds or more depending on the command. During read/write commands, CBSY will stay active after DBSY has gone inactive because tape motion will continue after data transfers are completed.

DBSY -

The DBSY signal is used by the tape drive to indicate to the controller that a transfer of data either to or from the tape drive is in progress. This signal will go active after CBSY to indicate a command sequence in progress. DBSY indicates data transfers within that command sequence.

STRB -

The STRB signal is used by the tape drive to acknowledge receipt of a command or parameter byte from the host, to acknowledge data byte transfers during write operations and as a strobe to transfer data to the controller during read operations.

2.3.2.2 Commmand Transfers to the Formatter

Signals -
- CREQ - (Control Request)
- CBSY - (Controller Busy)
- STRB - (Strobe)
- FCLR - (Formatter Clear)

Commands are sent to the formatter as part of an instruction sequence. The CBSY signal is active for the entire duration of an instruction. When the controller sends a command byte to the formatter, the CBSY line from the formatter goes active. If the command requires additional byte transfers or some activity by the drive, the CBSY line stays active until the last transfer or drive activity is completed. The total number of byte transfers, the direction of each byte, and type of drive activity is determined by the individual instruction.

When CBSY is inactive, the controller sets up the command byte on the data bus to the formatter, waits 150ns to allow for settling of the bus, and asserts CREQ to initiate the transfer to the formatter. The formatter accepts the command (if valid) and turns on CBSY to the controller. When the controller sees CBSY go active, it drops CREQ.

If additional bytes are to be transferred to or from the tape unit, the controller sets up the data bus for correct direction (input or output). If an output (to the formatter) is required, the controller sets up the byte on the bus to the formatter and asserts CREQ. The formatter sees STRB and drops CREQ. If a second byte is to be sent, the sequence repeats. If no additional transfers are required, the formatter turns off CBSY after completing the operation to indicate the end of the instruction. If STRB is not received from the formatter in less than 500us, the host disables CREQ and the sequence terminates.

2.3.2.3 Parameter Transfers to the Host

Signals -
CREQ - (Control Request)
CBSY - (Controller Busy)
STRB - (Strobe)

After the command byte has been sent, the controller sets the data bus to input mode (to the controller) and again asserts CREQ. The formatter places it's data byte on the bus and asserts STRB. The controller acknowledges receipt of the data by turning off CREQ. On seeing CREQ turn off, the formatter turns off the data on the bus and drops STRB.

2.3.2.4 Data Transfers to the Formatter (Write)

Signals -
DRBY - (Data Ready)
DBSY - (Data Busy)
CBSY - (Controller Busy)
STRB - (Strobe)

The host places the first data byte on the bus, waits 150ns, and asserts DRDY to the formatter. When the formatter sees the DRDY line go active, it asserts DBSY to indicate that it is busy with a data transfer, and 1.5us later asserts STRB to acknowledge receipt of the byte. After this, the formatter sends STRB pulses to the controller every 42us. The STRB pulse causes the controller to set up the next data byte on the bus. When the last byte has been transferred, the controller turns off DRDY to indicate the end of transfer to the formatter. The formatter responds by turning off DBSY. After the formatter completes the write operation including writing the gap, CBSY is turned off.

2.3.2.5 Data Transfers to the Host (Read)

Signals -
DRDY - (Data Ready)
DBSY - (Data Busy)
CBSY - (Controller Busy)
STRB - (Strobe)

The host asserts DRDY to the formatter to indicate that it is ready to receive data. When the formatter sees the DRDY line go active, it asserts DBSY to indicate that it is busy with a data transfer, sends the first byte to the controller, and asserts STRB to indicate transfer of the byte. After this, the formatter continues to send bytes and STRB pulses to the controller every 42us. The STRB pulse latches the data byte in the controller and generates a tape transfer DMA request to move the byte to RAM. When the last byte has been transferred, the tape drive stops sending STRB pulses and drops DBSY. After the formatter completes the read operation, CBSY is dropped.

2.3.3 CONTROLLER OPERATIONS

There are three basic groups of operations between the controller and the drive. These groups are:

a. The identity group which transfers status and identifying data from the drive to the controller. No tape motion is involved.

b. The positioning group which involves selecting the head or positioning tape. Tape may be moved to different positions, however no data is transferred.

c. The data transfer group which includes the read and write commands involving data and file marks.

2.3.3.1 The Identity Group

a. SENSE IDENTITY (Code - 00000)
Drive transfers 1 byte of data identifying type of device. Tape drive identifying byte is 0000 0001.

b. SENSE CONFIGURATION (Code - 00001)
Drive transfers 1 byte of data indicating the version number of the particular device.

c. SENSE STATUS (Code - 00010)
Drive transfers 2 bytes of data indicating the status of the device.

2.3.3.2 The Positioning Group

a. REWIND (Code - 00011)
Drive rewinds tape to LLP of Track 0.

b. LOAD (Code - 001000)
Drive establishes tape tension, positions tape at LLP, and after successful self-test, sets status bit 7 (not ready) false. Approx. 1 to 90 secs for execution of LOAD command.

c. UNLOAD (Code - 00101)
Drive rewinds and positions tape off BOT.
Approx. 1 to 90 secs for execution of UNLOAD command.

d. TRACK SELECT (Code - 00110)
Drive selects track and moves tape to position specified by track address/placement byte at a 70 IPS rate. The position status byte is updated.

e. ERASE (Code - 00111)
Drive erases tape at 30 IPS in forward direction. Drive motion stops at LEOT.

f. SPACE FORWARD (Code - 01000)
Drive spaces forward to the next Inter Block Gap at 30 IPS. File marks are sensed and drive motion stops at LEOT.

g. SPACE REVERSE (Code - 01001)
Drive spaces backward to the next Inter Block Gap at 30 IPS. File marks are sensed and drive motion stops at LLP.

h. SPACE FORWARD FM (Code - 01010)
Drive spaces forward to the next File Mark at 30 IPS and stops in the IBG following. If no FM is found, drive motion stops at LEOT.

i. SPACE REVERSE FM (Code - 01011)
Drive spaces backward to the next File Mark at 30 IPS and stops in the IBG following. If no FM is found, drive motion stops at LLP.

2.3.3.3 The Data Transfer Group

a. READ (Code - 01100)
Drive reads one record in forward direction.

b. WRITE (Code - 01101)
Drive writes one record with standard IBGs. Performs read-after-write check. Write commands from LLP will start 3 inches from LLP. Write command attempted while cartridge is write protected will cause command status error.

c. WRITE EXTENDED (Code - 01110)
Drive erases forward approximately 3 inches and then writes one record with standard IBGs. Same as WRITE except for 3 inch spacing before write operation.

d. WRITE FM (Code - 01111)
Drive writes standard file mark with IBGs on either side.

e. WRITE FM EXTENDED (Code - 10000)
Drive erases forward approximately 3 inches and then writes one file mark with standard IBGs on either side. Same as WRITE FM except for 3 inch spacing before write operation.

f. EDIT (Code - 10001)
Drive determines distance between block to be edited and the head: If necessary, the tape is then repositioned to allow the unit to ramp up the speed and edit the block properly.

2.4 TAPE DRIVE POWER SUPPLY

The power supply for the Archiving Cartridge Tape Drive circuitry provides +23V, +5V and -5V to meet various circuit requirements. Conventional series regulator designs were employed for the circuitry. The schematic drawing of the power supply (part no. 210-7770) is provided in chapter 6.

The main power transformer has two 115V primary windings which are connected in parallel for 115V operation and in series for 230V operation by the line voltage switch, SW1. There are two center-tapped secondary windings - one providing 26Vac to the 23V circuits and the other providing 7.6Vac to the 5V ciruits.

2.4.1 THE 23V SUPPLY

The 26Vac from the transformer is rectified and filtered and the unregulated dc is then fed to a LM350T regulator module. An output voltage control for the 23V supply is designated as R20 on the 210-7770 Regulator Board (see Figure 4-2). A LED to indicate the presence of 23V and a 23V test point are also shown on Figure 4-2.

2.4.2 THE -5V SUPPLY

The +5V and -5V supplies are both fed from the 7.6Vac winding on the transformer. For the -5V supply the 7.6Vac is rectified and filtered and the unregulated dc is fed to a 79MO regulator module. A LED is provided to indicate presence of -5V (see figure 4-2) but no votage adjustment is provided.

2.4.3 THE +5V SUPPLY

The +5V supply employs an LM723 regulator module which feeds a two stage pass transistor circuit consisting of a TIP29 a 2N5301. A current limiting circuit employing an LM311 comparator is also included. The LM723 and LM311 are powered by a zener diode regulator circuit which is fed from the +23Vdc supply. The TIP29 and 2N5301 collectors are fed from separate rectifier and filter circuits which are connected to the 7.6Vac winding of the transformer. An adjustment for the +5V output is provided by R16 and the presence of +5V is indicated by a LED (see Figure 4-2).

The 210-7770 board contains large heat sink (see Figure 4-2) on which are mounted the 2N5301 transistor, the rectifiers which supply power to the 2N5301, the LM350T module and a thermal overload switch which is connected in series with the ac power line.

2.4.4. POWER SUPPLY SPECIFICATIONS

2.4.4.1 +5V Supply

Load Regulation	.5% (measured at load)
Load regulation	.07% (measured at reg. board)
Line regulation	less than .002%
Ripple and noise	less than 3 mv.
Minimum adjustment range	.7 volts
Output current	8.0 amps
Current limiting	9.4 to 10.9 amps

2.4.4.2 +23V Supply

Load regulation	.65% (measured at load)
Load regulation	50% (measured at reg. board)
Line regulation	less than .25%
Ripple and noise	less than 3mv
Minimum adjustment reange	4.4 volts
Output current	1.0 amp
Current limiting	3.0 to 4.0 amps

2.4.4.3 -5V Supply

Load regulation	.15% (measured at load)
Line regulation	less than .025%
Ripple and noise	less than 5 mv
Not adjustable, tolerance	4.85V to 5.30V (measured at load)
Output Current	110 ma
Current limiting	.30 to .60 amp

2.4.4.4 A.C. Input

115V Operation	98Vac to 128Vac	1.4A nom @ 128 Vac.
230V Operation	196Vac to 256Vac	.7A nom @ 256 Vac.

CHAPTER 3 OPERATION

CHAPTER 3

OPERATION

3.1 INTRODUCTION

The Archiving Cartridge Tape Drive is a peripheral device that utilizes a 1/4 inch magnetic tape cartridge to store data. It is designed primarily as a slave processor to provide reliable backup for Wang systems having fixed disk drives. There are three stand-alone models available: Model 2229 for use with the 2200 system, Model 6529 for OIS systems and Model 2529V for VS systems.

The tape interface is made to the Kennedy Model 6455 quarter inch cartridge tape system. Models 6529 and 2529V contain their own data link logic for interface to a master, a central processing unit (CPU), memory, tape DMA controller, and interface electronics to the Kennedy tape drive. All this logic is located on a single board that is contained within the tape unit. Model 2229 uses a mother/daughter board arrangement located in the 2200 CPU for interface with the 2200 system in place of the logic board used in the other models.

3.2 CONTROLS, INDICATORS AND EXTERNAL CONNECTIONS

The front panel of all models is shown in Figure 3.1. Figure 3.2 shows the rear panel of Model 2229 and Figure 3.3 shows the rear of Model 6529/2529V. The functions of the various controls, indicators and connectors is described below.

Item	Function
AC Power Switch	Turns main power on/off.
Online Switch	An alternate on/off switch that places the unit on/off line from the CPU.
Power On Indicator	The Power On Indicator will blink on and off during execution of the power-up PROM resident diagnostics and will be ON steady upon successful completion of the diagnostics.
Online Indicator	Used with the Online Switch.
Fault Indicator	Indicates to the operator that a hardware error condition exists.

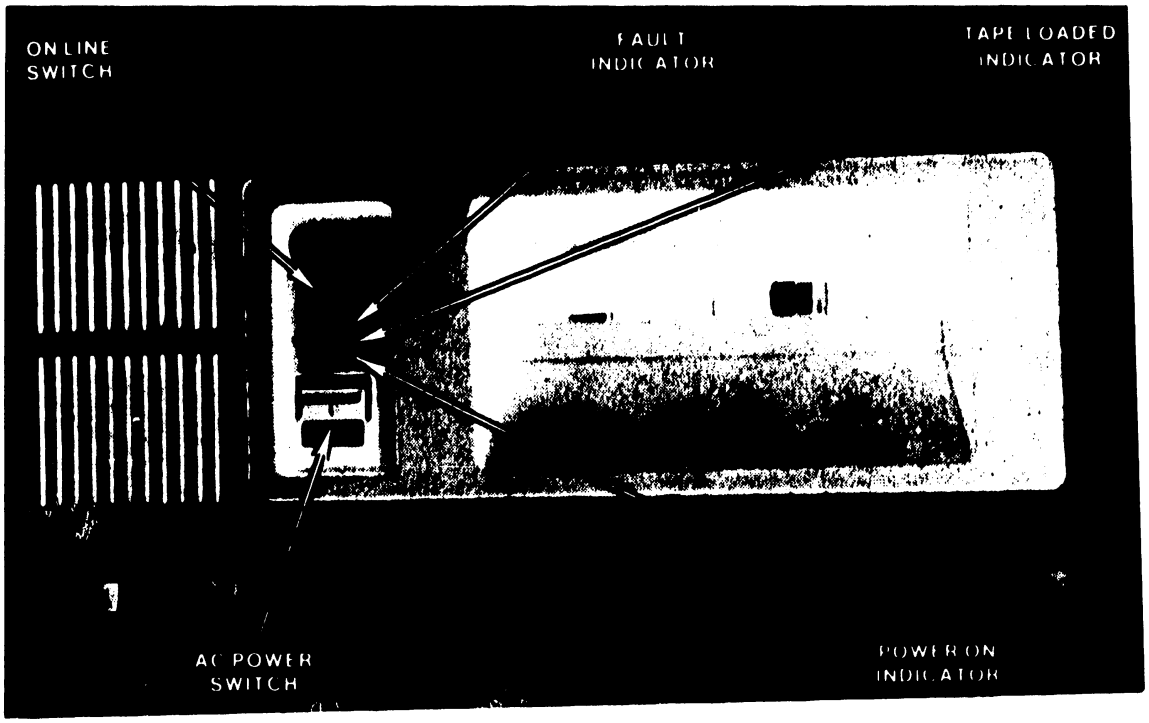


Figure 3-1 Front Panel (all models)

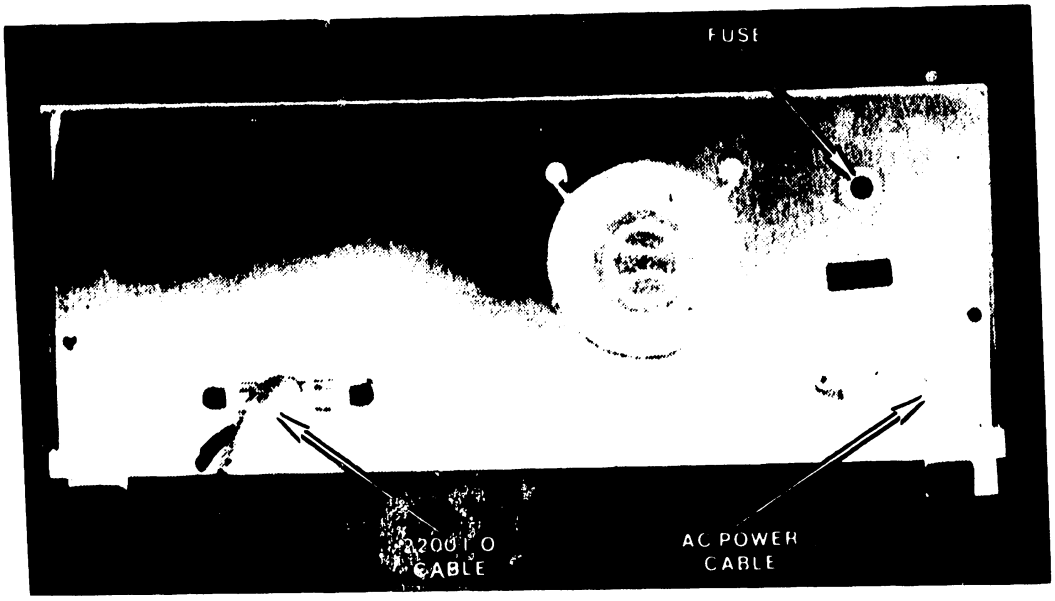


Figure 3-2 Rear Panel of Model 2229

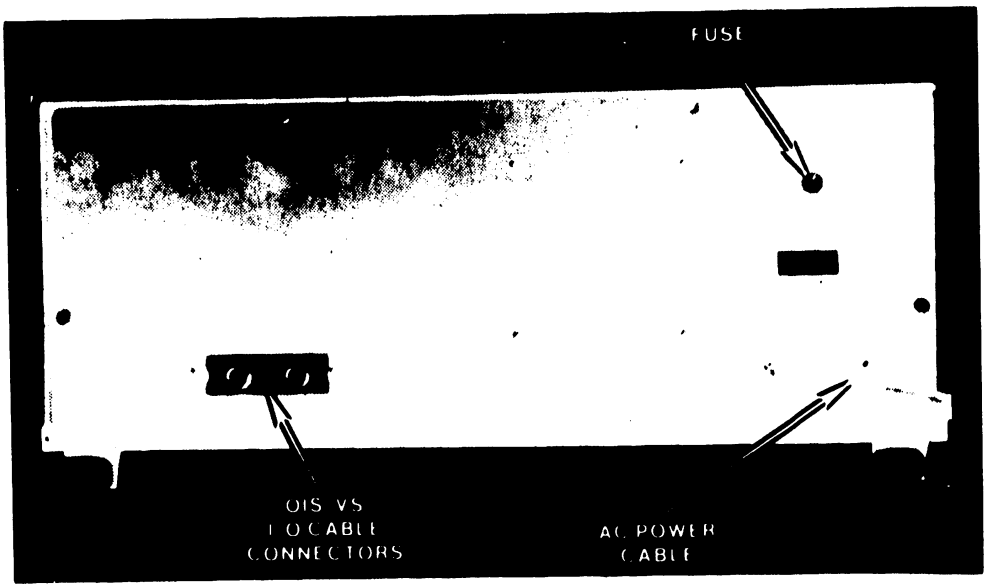


Figure 3-3 Rear Panel of Model 6529/2529V

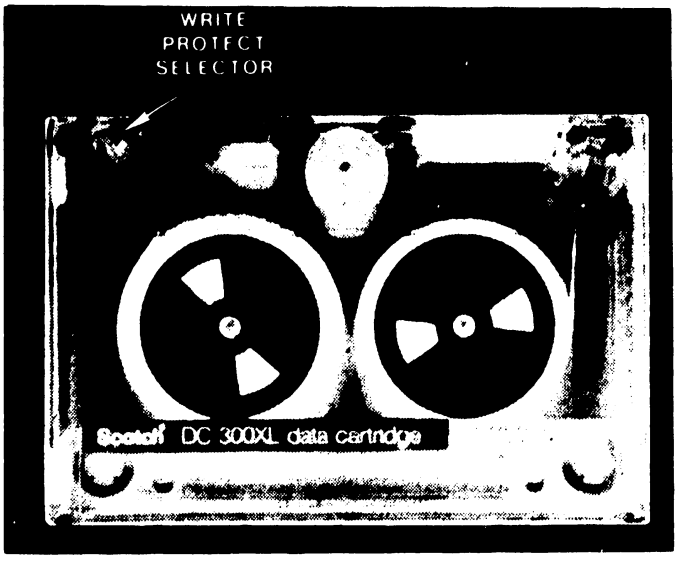


Figure 3-4 Tape Cartridge

Item	Function
Tape Loaded Indicator	Indicates that a tape cartridge is properly loaded.
2200 I/O Connector (Figure 3-2)	Connector for parallel interface cable connecting the Model 2229 to the 2200 CPU.
OIS/VS Connector (Figure 3-3)	Connector for serial interface cables connecting the Model 6529/2529 to the OIS/VS master.

3.3 INITIAL TURN-ON PROCEDURE

Before operating the unit, verify that the interface cables are properly attached (see Chapter 4). The operator should be assured that the line voltage switch (see Figure 4-2) is set for the proper supply voltage. If necessary, remove the cabinet cover (see Chapter 5 for the procedure and Figure 5-3 for the switch location) and check the switch setting. The power switch on the front of the unit may then be turned on.

On applying power to the Model 6529/2529V, a power-up diagnostic will be executed. The Power On Indicator will blink on and off during execution of the diagnostic. After successful completion of the diagnostic, the indicator will be on steady. The software may then be loaded and run (see Chapter 4). Care should be taken to ensure that the protective cover is removed from the magnetic head before inserting a tape cartridge (see paragraph 4.6). If an error should occur during the power-up diagnostic, the Fault Indicator will come on. Refer to Chapter 8 for the procedure in this case.

The Model 2229 does not execute a power-up diagnostic when power is applied. Instead, the diagnostic is executed when the software is run and error messages will appear on the 2200 workstation screen. See Chapter 4 for procedures for loading and running the software.

3.4 HANDLING THE TAPE CARTRIDGE

A tape cartridge can be inserted after power-up or when prompted by the Tape Utilities program. To insert a tape cartridge, place the top of the cartridge into the opening on the front panel and push firmly until the cartridge is fully seated. Following insertion a LOAD command is issued by the system software. To remove a cartridge, an UNLOAD command is issued in which the cartridge is advanced to EOT at high speed. Then grasp the cartridge firmly and pull straight out.

A write-protect selector (see Figure 3-4) is located on the upper left corner of the tape cartridge. When the arrow on the write protect selector is pointing to the SAFE position, the tape cannot be written over. To engage this feature, use a flat-bladed instrument to rotate the selector clockwise until a click is heard, and the arrow is aligned with SAFE. To copy over a tape, rotate the selector counterclockwise until it clicks into position with the arrow facing away from SAFE.

To protect data stored on a tape cartridge, several precautions should be observed. Store the cartridges in a cool, dry place off the floor, in the protective boxes they came in. Do not expose tapes to prolonged direct sunlight, strong magnetic fields, excessive humidity or temperature extremes. To minimize dust contamination, the computer room should be kept clean. Smoking in the computer room is not recommended, as ashes contacting the tape surface can produce permanent damage.

3.5 TAPE UTILITIES

3.5.1 2229 UTILITIES

NOTE

Before running the 2229 Utilities be sure the device address is entered into the Master Device Table. Device address 018 is generally used for the tape controller address.

The 2229 ACTD Utilities are available on either of the following diskettes:

a. 195-2548-3 Single-Sided, Single Density
b. 195-2548-5 Double-Sided, Double Density

The 2229 Utility includes the following procedures:

Backup Platter to Tape
Recover Platter From Tape
Recover File from Platter Backup
Create Reference File
Backup Files to Tape
Recover Files from Tape
Tension Tape Cartridge

The following paragraphs provide a description of these procedures. Additional information can be found in the Model 2229 Cartridge Tape Drive Users Manual (WLI#700-7716).

3.5.1.1 Backup Platter from Tape

This option allows the operator to backup a disk platter to tape. Using 16K data blocks, approximately 15 megabytes of data can be copied onto a 450 ft. tape. If the tape cartridge's capacity is exceeded, the program prompts the operator to mount another tape and assigns the proper sequence number to it.

3.5.1.2 Recover Platter from Tape

Recover Platter from Tape allows the operator to retrieve all data from a tape cartridge and writes it to disk.

3.5.1.3 Recover File from Platter Backup

Retrieves a single file from a platter backup tape and writes it to disk.

3.5.1.4 Create Reference File

Builds a reference file (on disk) of selected file names. Allows you to conveniently back up a series of files by performing Backup Files to Tape.

3.5.1.5 Backup Files to Tape

Uses the reference file created in the previous option to select designated files on disk and back them up to tape.

3.5.1.6 Recover Files from Tape

Allows you to examine files on a tape and specify which one(s) will be written to disk. Recovery options are Add, Replace, Add/Replace, Recover Single File, and Query Each File.

3.5.1.7 Tension Tape Cartridge

Winds, then rewinds a tape cartridge to create a uniform tension on the tape.

3.5.2 6529 UTILITIES

6529 Utilities are available on the following diskettes. All are needed for proper installation. Use the "Install Software Package" method to install the software.

Package Number 195-2498-3, 195-2498-9

a. 703-2291
b. 703-2354
c. 703-2292

The 6529 Utility includes the following procedures:

Initialize Tape
Backup to Tape
Restore from Tape
Copy to Tape
Copy from Tape

The following paragraphs provide a description of these procedures. Additional information can be found in the Model 6529 Cartridge Tape Drive Users Manual (WLI#700-8071).

3.5.2.1 Initialize Tape

Each new tape must be initialized before it can be used to save files. This option will write a valid tape label which includes tape name, expiration date, and tape length.

3.5.2.2 Backup to Tape

Will copy all files from a volume to tape. Files may be selected by a date range.

3.5.2.3 Restore from Tape

Will retrieve all files from the tape and write them to a volume.

3.5.2.4 Copy to Tape

Will copy all files under a partial file name from a selected volume to tape.

3.5.2.5 Copy from Tape

Will copy files from tape to a specified volume. Options include Create/Recreate, copy range of files, or user may select any desired files individually.

3.5.3 2529V UTILITIES

NOTE

Before running the 2529V Utilities be sure the device has been entered into the 'CONFIG' file. Enter the device as model "2529V".

The 2529V ACTD Utilities are a part of the VS Operating System. OS Release 5.3.70 or greater is needed to support the tape drive.

The 2529V can run the following VS utilities:

a. TAPEINIT
b. BACKUP

The following paragraphs provide a description of these procedures. Additional information can be found in the VS Utilities Reference Manual (WLI# 800-1303UT) and the Model 2529V User Summary Card (WLI# 800-6212).

3.5.3.1 Tapeinit

TAPEINIT initializes a tape and writes a label on it. All information stored on the tape is destroyed. A new tape must be initialized before being written on for the first time. The tape name, label type (NOTE: ONLY "NL" (Non-Labeled) LABEL TYPE IS SUPPORTED), and tape length are written to the tape.

3.5.3.2 Backup

BACKUP copies a file, library, or volume from one location to another. It also restores backed up copies.

CHAPTER 4

INSTAL-LATION

CHAPTER 4

INSTALLATION

4.1 UNPACKING

Before unpacking the tape drive, inspect the shipping carton for damage. Then carefully open the carton, remove the unit and inspect it for damage. Also, check that the following items are included and inspect them for damage.

Item	Part No.
Power cable	420-1005
Blank tape (450 ft.)	725-1227
Interface cables:	
For Model 2229 (10 ft.)	220-0105-3
For Model 6529/2529 (25 ft.)	220-0148

If damage is discovered, file an appropriate claim promptly with the carrier involved and notify the WLI Distribution Center (Dept. #90), Quality Assurance Dept., Tewksbury, MA 01876. Inform them of the extent of the damage and arrange for equipment replacement if necessary.

4.2 MINIMUM REVISION LEVELS

The circuit board revision levels should be checked in order to assure system compatibility. The procedure for accessing the boards is covered in Chapter 5. Minimum revision levels for the boards in all models is given below:

Board	Description	Revision
210-8259	2200 Daughter board (2229)	R1
210-8260	2200 Mother board (2229)	R1
210-8261	2200 Adapter board (2229)	R1
210-8262A	OIS/VS Inerface board (6529/2529V)	R1
210-7770	Regulator board (2229/6529/2529V)	R1

Software revsision levels are as follows:

OIS
Starter F5.3 or higher. Release 0.7 utility or higher.
Cartridge Tape Utilities Update 703-2291, 703-2354, 703-2292.

2200
Release 2.4 Basic or higher.

VS
Release OS5.3.70.

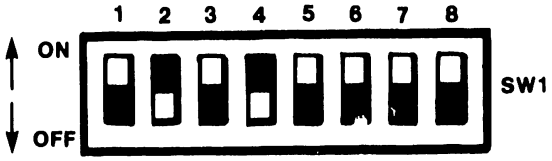
4.3 SWITCH SETTINGS

4.3.1 MODEL 6529/2529V

Before connecting up the tape drive, the various switch settings should be checked to verify that they are set in accordance with system requirements.

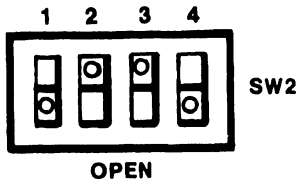
Device Class Switch

This switch is located on the 210-8262 Interface Board (the large board on top of the chassis) and it is designated SW1. Figure 4-1 shows the switch location. It must be set to HEX 0A as shown in the following sketch.



Device Type Switch

This switch is designated SW2 in Figure 4-1. It must be set to HEX 06 as shown in the sketch below.



SW1 on Kennedy Formatter

This switch bank is located at the rear right end of the Kennedy Formatter board. Switch 5 on this bank should be set on: all other switches should be off. (see Figure 5-9).

Line Voltage Switch

The line voltage switch located on the power supply regulator board (see Figures 4-2 and 5-3) should be checked to verify that it is set to the voltage of the mains.

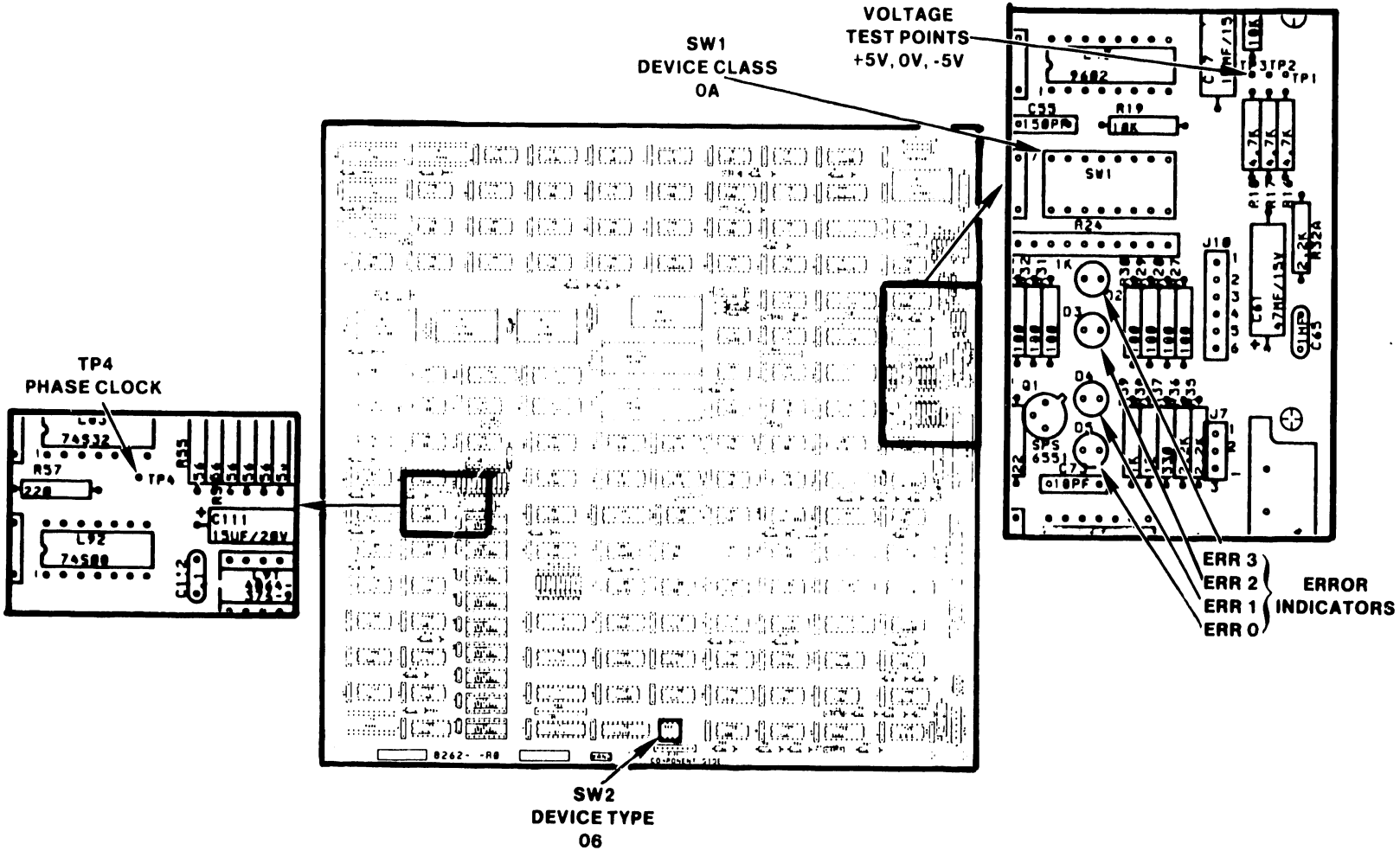


Figure 4-1 210-8262 Interface Board

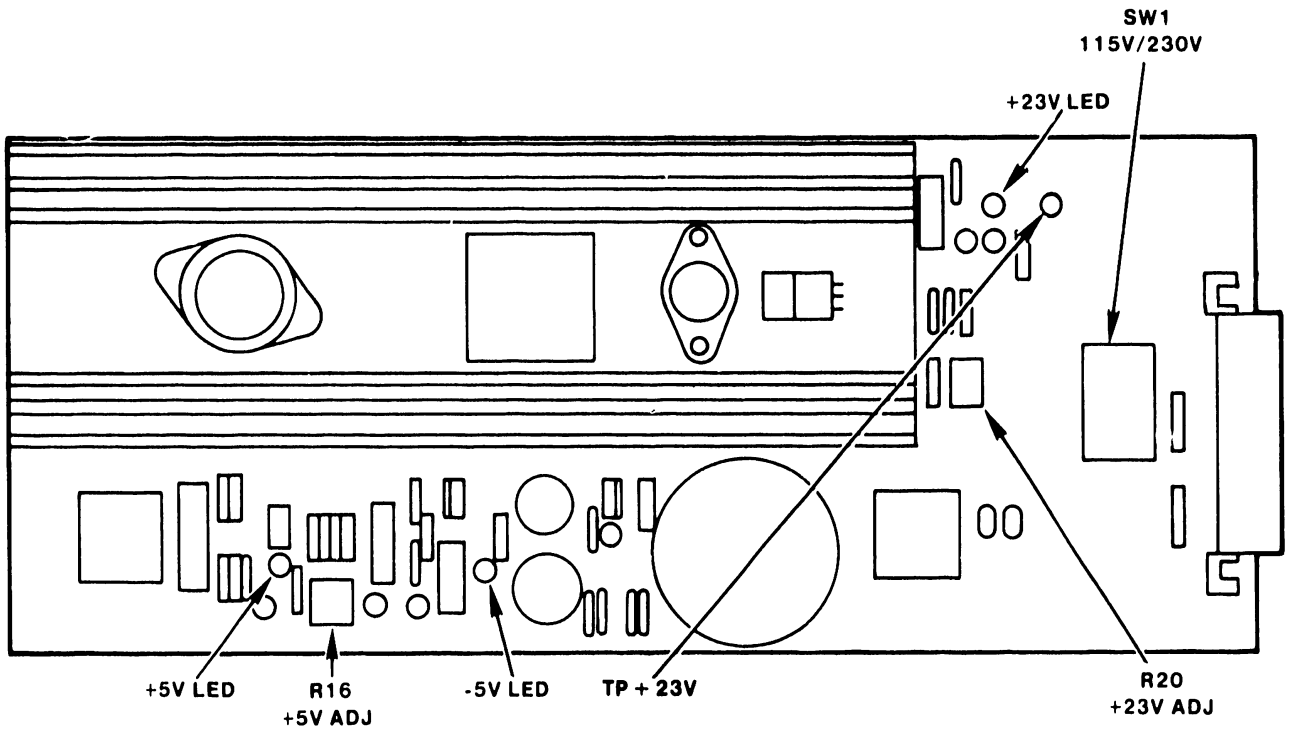


Figure 4-2 210-7770 Regulator Board

4.3.2 MODEL 2229

Option Switch

This switch is located on the 210-8260 motherboard in the 2200 CPU. It is shown as SW1 on Figure 4-3. Switch 1 on this bank is set ON for a 4 track tape drive and OFF for a 7 track drive. Switch 4 is set ON for normal operation and OFF for diagnostic tests. Switches 2 and 3 are not used.

Address Select Switch

This switch is designated SW2 on the 210-8260 motherboard (see Figure 4-3). It should be set to (HEX) 018 (switches 4 and 5 ON; the others OFF).

The settings for SW1 on the Kennedy formatter and line voltage switch on the regulator board are as described under paragraph 4.3.1 for the Model 6529/2529V.

4.4 VOLTAGE CHECKS

With the cabinet cover removed, the power supply regulator board (see Figure 4-2) is accessible. After turning on the power, the +5V and -5V levels may be measured at the voltage test points on the 210-8262 board (see Figure 4-1) on the OIS/VS models. On the Model 2229 the +5V can be measured at the test socket on the Kennedy formatter board. The location of the +5V test pin is shown in Figure 8-X. The Model 2229 does not use -5V.

The +23V can be measured at the +23V test point on the regulator board (see Figure 4-2). In the event that the +5V or +23V is outside of its tolerance, it may be corrected using the voltage adjust controls shown on Figure 4-2. Verify that the three LED voltage indicators are on.

4.5 SYSTEM INTERCONNECTIONS

4.5.1 MODEL 2229

Figure 4-4 shows the internal cabling of the Model 2229 and the external cable connection to the 2200 CPU. The parallel I/O cable connects to the back of the Model 2229 cabinet as shown in Figure 3-2. The installer must insert the 212-3037 I/O Interface assembly into one of the I/O slots in the 2200 CPU and then connect the other end of the I/O cable to the parallel interface connector on the I/O assembly. Figure 4-5 is an aid in identifying the internal cable connections to the 210-8261 Adapter board.

4.5.2 MODEL 6529/2529V

Figure 4-6 shows the internal cabling of the Model 6529/2529V. The rear of the unit contains a BNC/TNC connector pair for connecting it to the OIS/VS master using the standard serial dual coax cable.

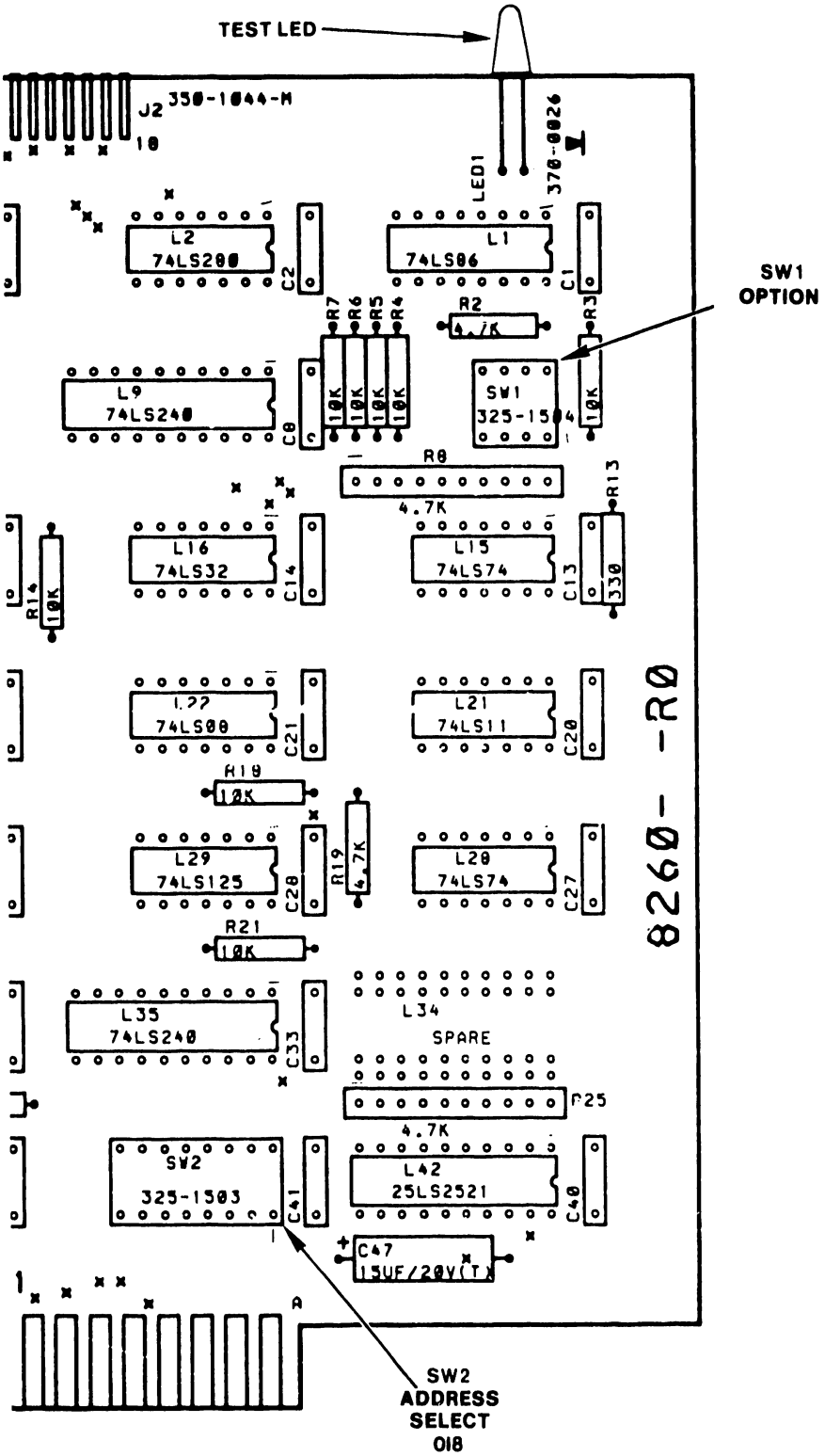


Figure 4-3 210-8260 Motherboard

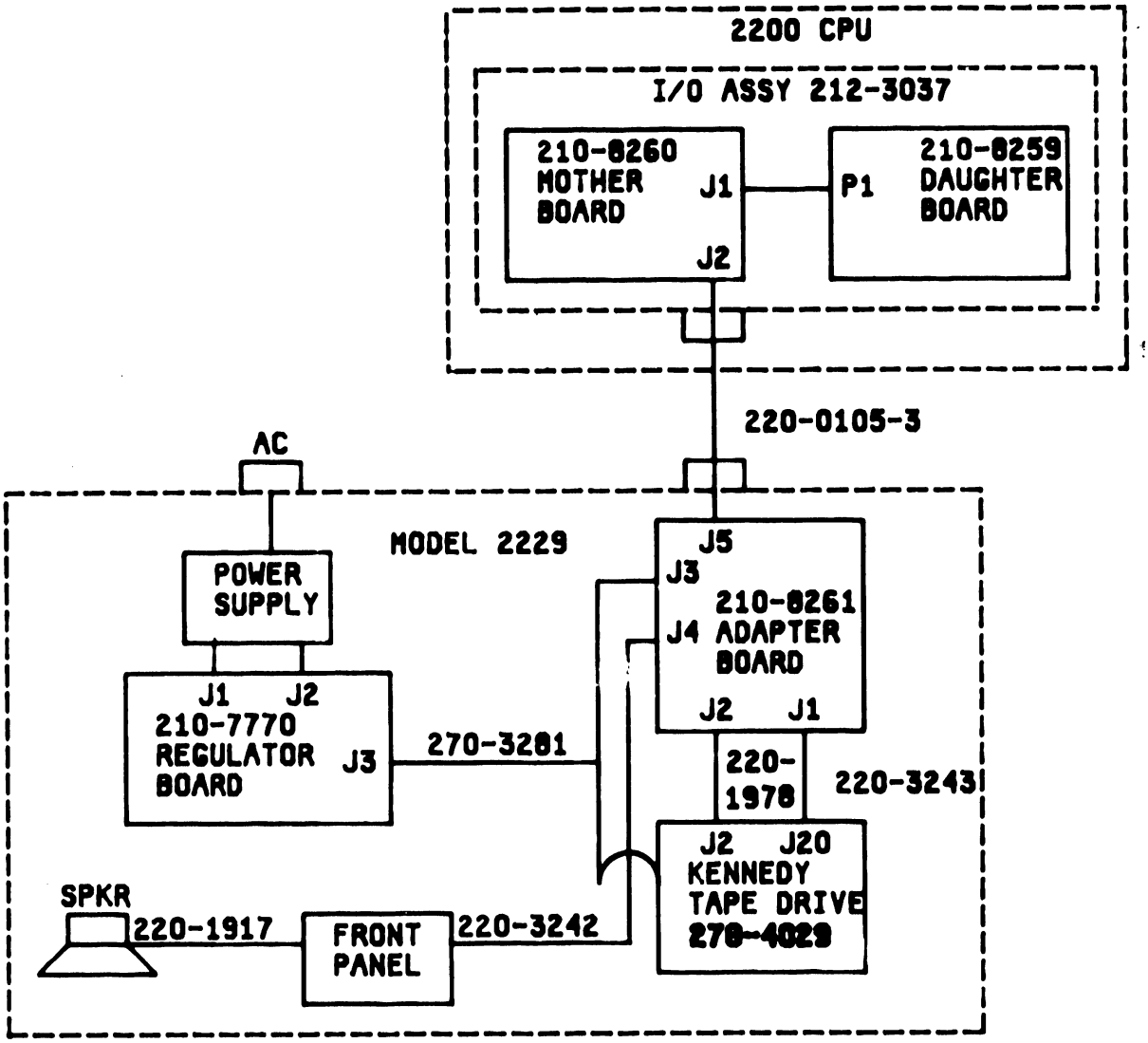


Figure 4-4 Model 2229 Interconnections

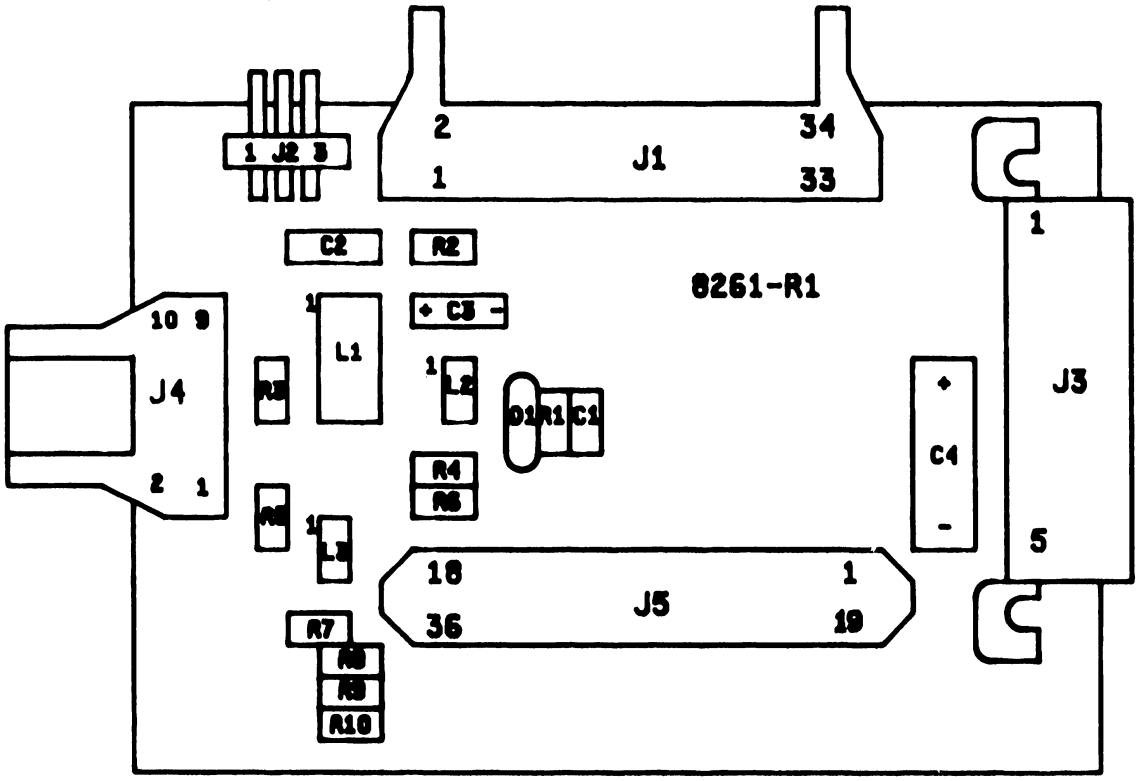


Figure 4-5 210-8261 Adapter Board

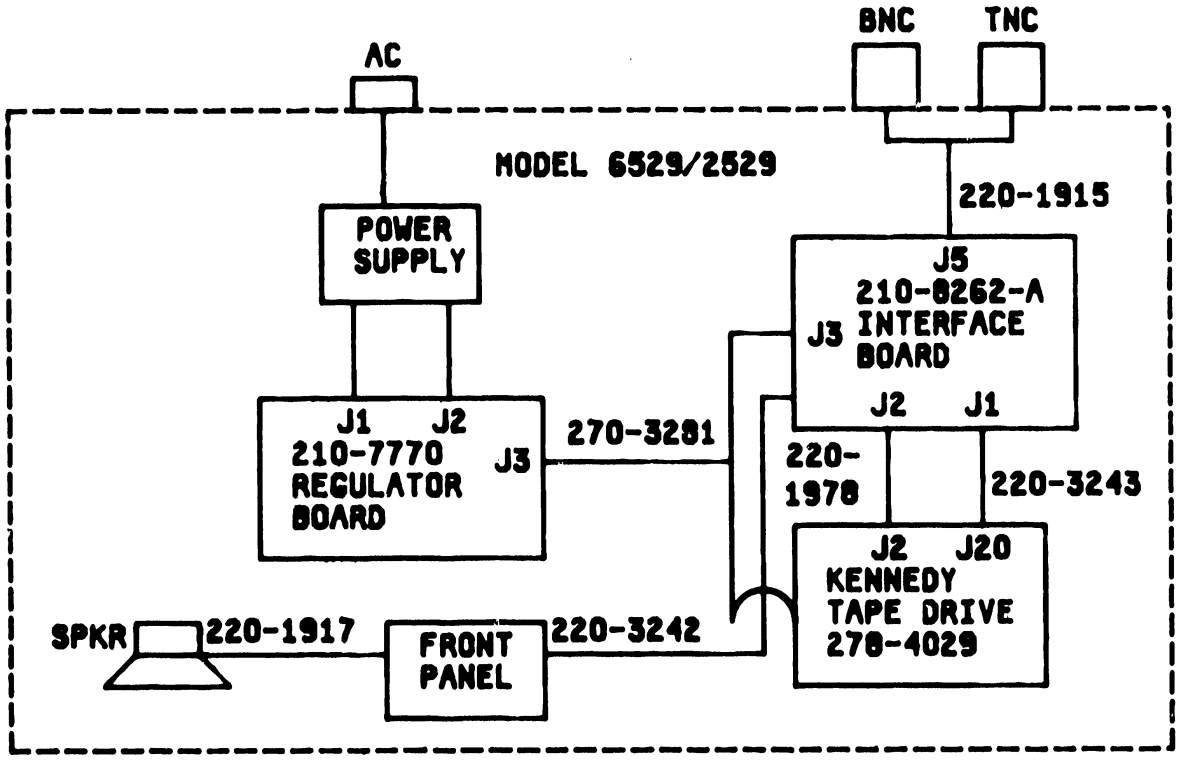


Figure 4-6 Model 6529/2529 Interconnections

4.6 POWER-UP PROCEDURE

Before operating the tape drive, verify that all interface cables are attached. Next, remove the protective cover from the magnetic head. The power switch may then be turned on. Then install a tape cartridge per procedures given in paragraph 3.4. Paragraph 3.3 describes the events immediately following power-on for each model.

4.7 SOFTWARE LOADING

For VS
No loading procedure necessary.
Utility is invoked by running:
a. TAPEINIT
b. BACKUP

For 2200
Run utility from utility diskette.
(195-2548-3: SSSD Diskette)
(195-2548-5: DSDD Diskette)

For OIS
Load installation packages:
703-2291
703-2354
703-2292
via "INSTALL SOFTWARE PACKAGE".

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation, a preventive maintenance schedule should be kept. The items involed are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport, so a rigid schedule applying to all machines is difficult to define.

5.1.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

5.1.2 CLEANING

All items in tape path must be kept scrupulously clean. This is particularly true of the head. When cleaning heads, it is important to be thorough yet gentle and to avoid certain dangerous practices.

5.1.2.1 Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient but must be used with caution. Be sure the wooden portion does not contact head surfaces.

An ideal solvent is 1.1.1 trichloroethane contained in the Kennedy K21 maintenance kit (Wang part no. 726-9660). However, other solvents such as isopropyl alcohol will do.

DO NOT USE - acetone or lacquer thinner
- aerosol spray cans
- rubbing alcohol

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate the ball bearings of the capstan motor, since it will destroy their lubrication.

5.1.2.2 Other Cleaning

Use a vacuum cleaner to remove accumulations of dust. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings.

5.1.3 ROUTINE ADJUSTMENTS

There are no routine adjustments. Need for adjustment becomes manifest when malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than to prevent it.

5.1.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

5.1.5 HEAD WEAR

Head wear is generally signaled by an increase in error rate. Confirmation is a sizable increase in output voltage from the read head as measured at the read preamplifier. When the head becomes worn it must be replaced. Head replacement is described in paragraph 5.2.2.3.

5.1.6 PERIODIC INSPECTION

Every two months, it is advisable to make a more thorough check of machine operating parameters to insure that no progressive degradation goes unnoticed. The recommended sequence for checks is shown in table 5-1.

5.2 CORRECTIVE MAINTENANCE

5.2.1 DISASSEMBLY PROCEDURES

5.2.1.1 Cabinet Cover

The cabinet cover on all models is attached by four screws at the rear (see Figure 5-1). After removing these screws, slide the cover forward a few inches to free the tabs on the bottom of the front cover which engage the bottom chassis. The cover may then be lifted away.

5.2.1.2 210-8261 Adapter Board (Model 2229 only)

The location of the Adapter Board is shown in Figure 5-2. The board is held in place by two hex nuts which are on the screws which are used to secure the I/O cable connector. Since the I/O cable connector is screwed into the heads of these screws, the I/O cable must be removed first. The nuts and screws which hold the board can then be removed. One of these nuts is visible in Figure 5-2.

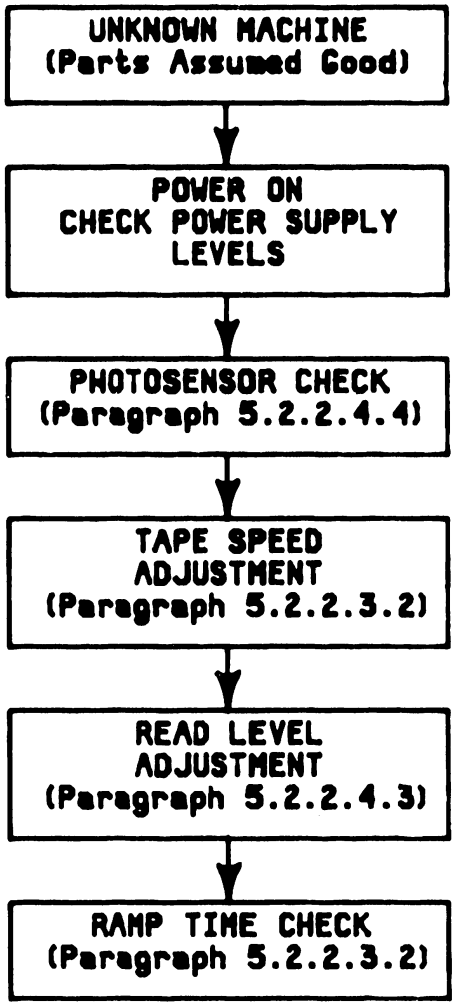


Table 5-1 Adjustment Sequence

5.2.1.3. 210-7770 Regulator Board

Figure 5-3 shows the location of the power supply components (the OIS model is shown in the figure but power supply layout is the same for all models). Figure 5-4 shows the layout of the 210-7770 Regualtor Board. The board is held in place by the two mounting screws shown and two grooved mounting posts which are gripped by tabs which are bent up from the chassis. To remove the board, first remove the two mounting screws and then pull the board straight up out of the tabs.

5.2.1.4 Control Panel and Power Switch

The Control Panel (see Figure 5-5) is attached to the chassis by four screws. The Power Switch is secured to the panel by 4 squeeze tabs.

5.2.1.5 Line Filter

The Line Filter (see Figure 5-3) is attached to the back panel by two studs which also support the power cable connector.

5.2.1.6 210-8262 Interface Board (Model 6529/2529V only)

The Interface Board (see Figure 5-5) is held in place by two screws (one by L47 and one by L150) and four plastic pins. After removing the screws, the board may be swung upward by bending two plastic clips on the pins that secure the front. The two pins that hold the rear of the board have locking splines. The splines will recede when squeezed so that the pins will pass through the holes in the board.

5.2.1.7 Fan

The fan is secured by four screws. The nuts on these screws are not captive. Therefore, care must be taken to retrieve the nuts and lock washers when the screws are removed.

5.2.1.8 Kennedy Tape Drive (278-4029)

The Kennedy tape drive is not to be field serviced and must be replaced as a unit when repairs are required. The drive is secured by five screws in the Model 2229 and by seven screws in the Model 6529/2529V. In all models, the drive is secured to the bottom chassis by four screws indicated in Figure 5-6. Figure 5-3 shows another mounting screw that is common to all models. The tape drive in the Model 6529/2529V is secured by two additional screws which are shown in Figure 5-5. The part numbers of Field Service Center (FSC) replaceable parts are given below:

Wang Part Number	OEM Part Number	Description
726-6202	190-5663-001	F650 Formatter
726-6203	190-4876-001	Infrared Sensor Assembly
726-6204	190-5516-002	Head Assembly
726-6205	190-6478-001	Control/Read/Write Board
726-6206	190-4799-002	Capstan Motor Assembly
726-6207	190-5380-001	Interlock Assembly

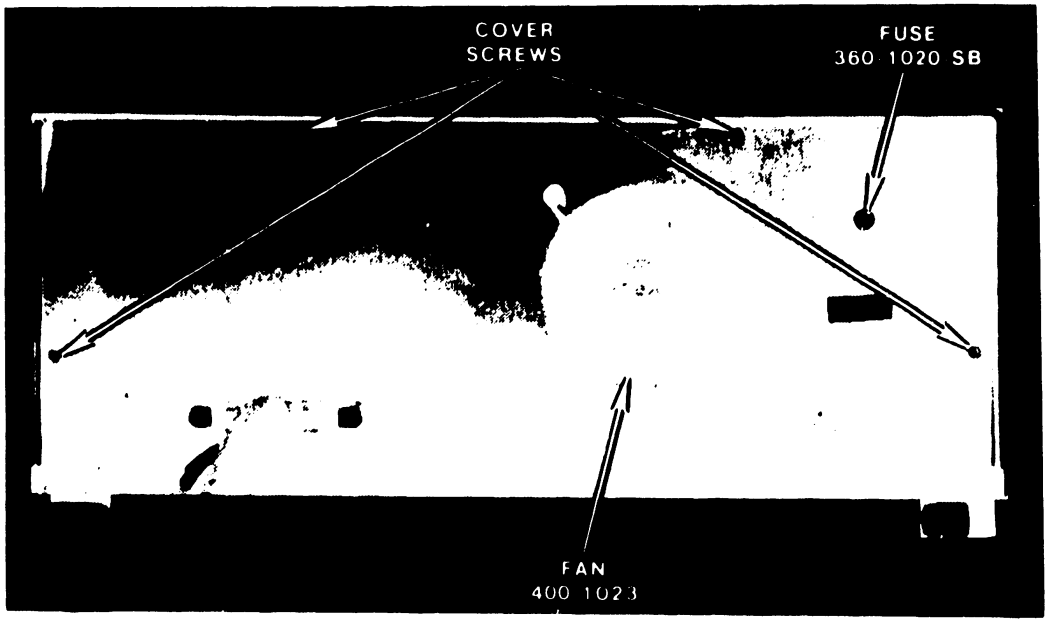


Figure 5-1 Cabinet Cover Screws

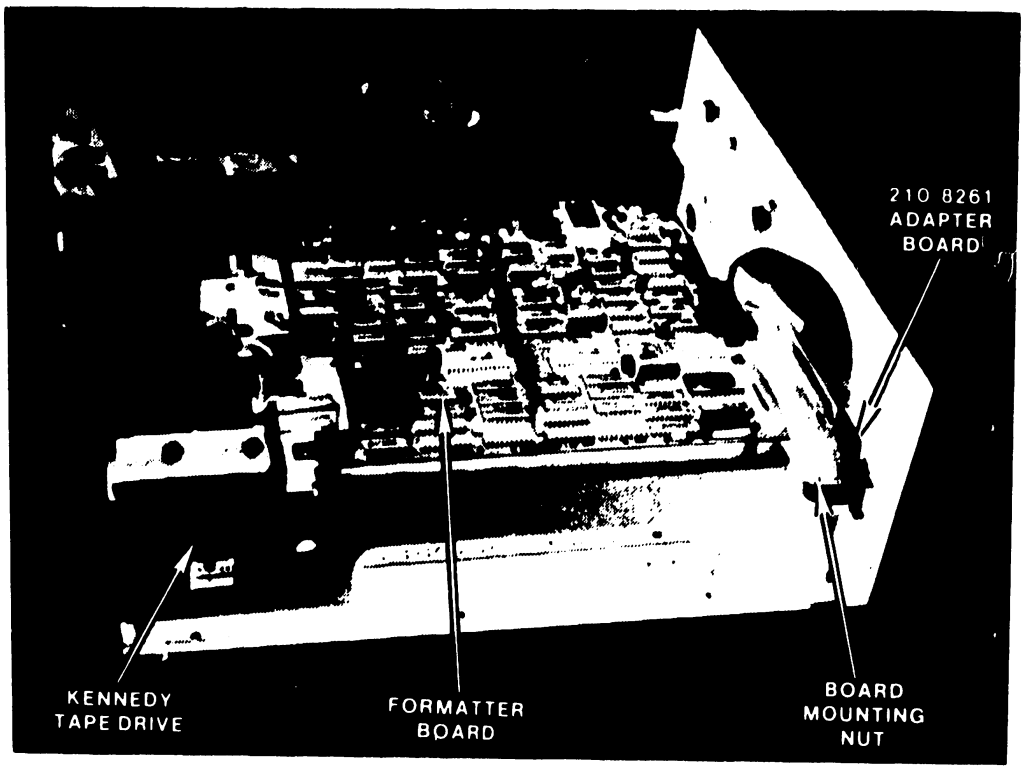


Figure 5-2 Internal Components - Model 2229

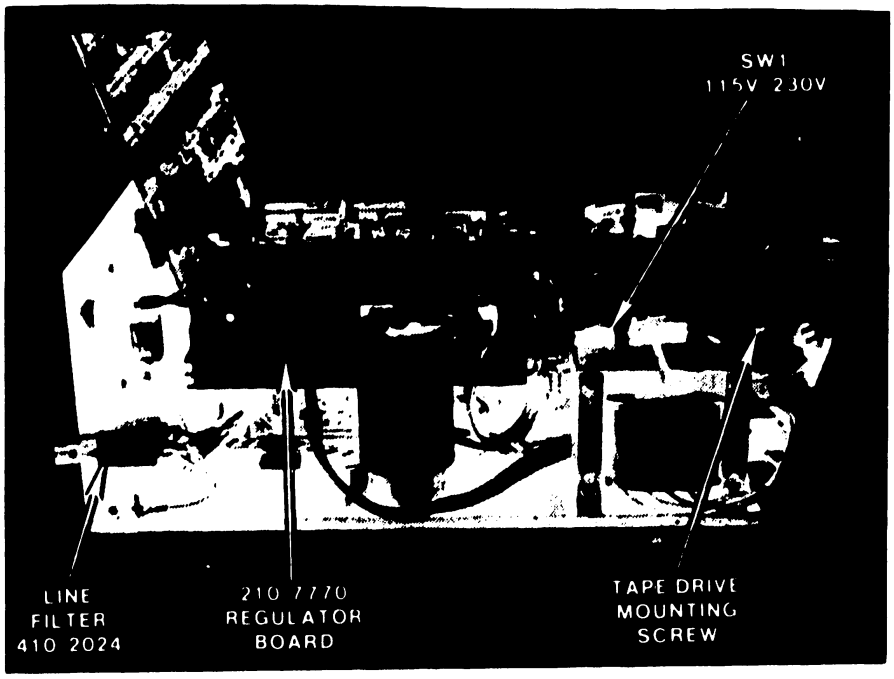


Figure 5-3 Power Supply Components

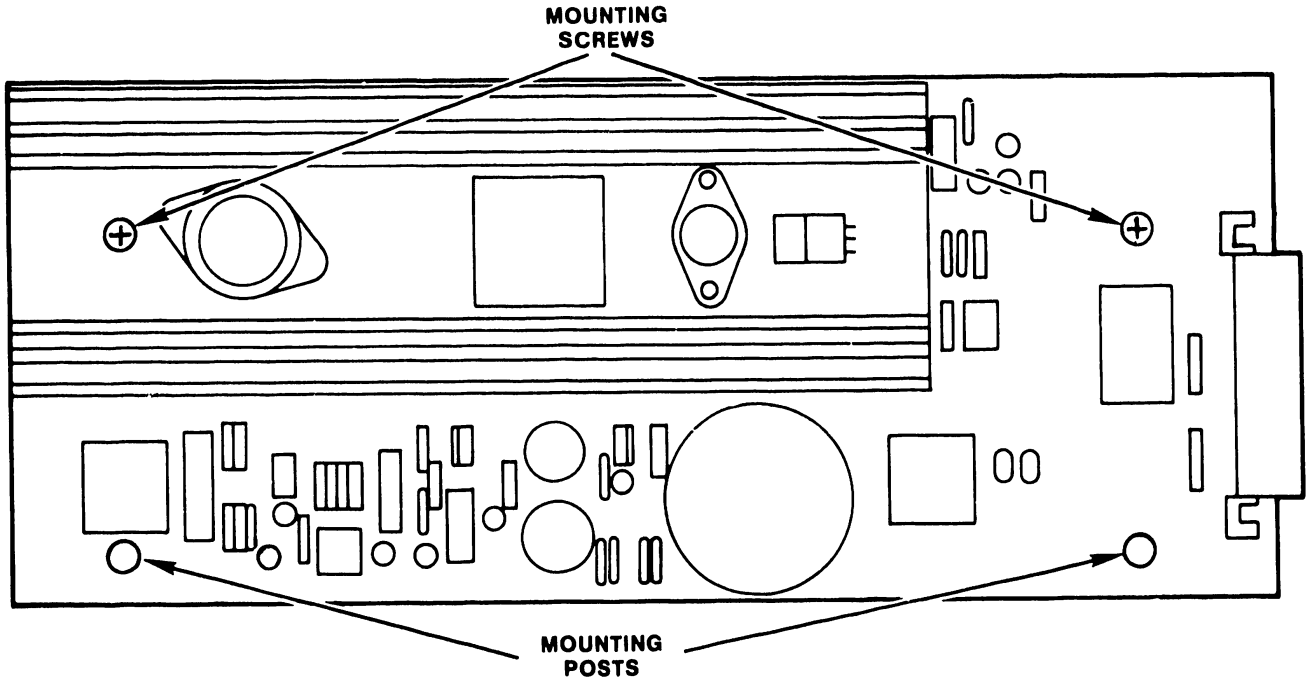


Figure 5-4 210-7770 Regulator Board Mounting

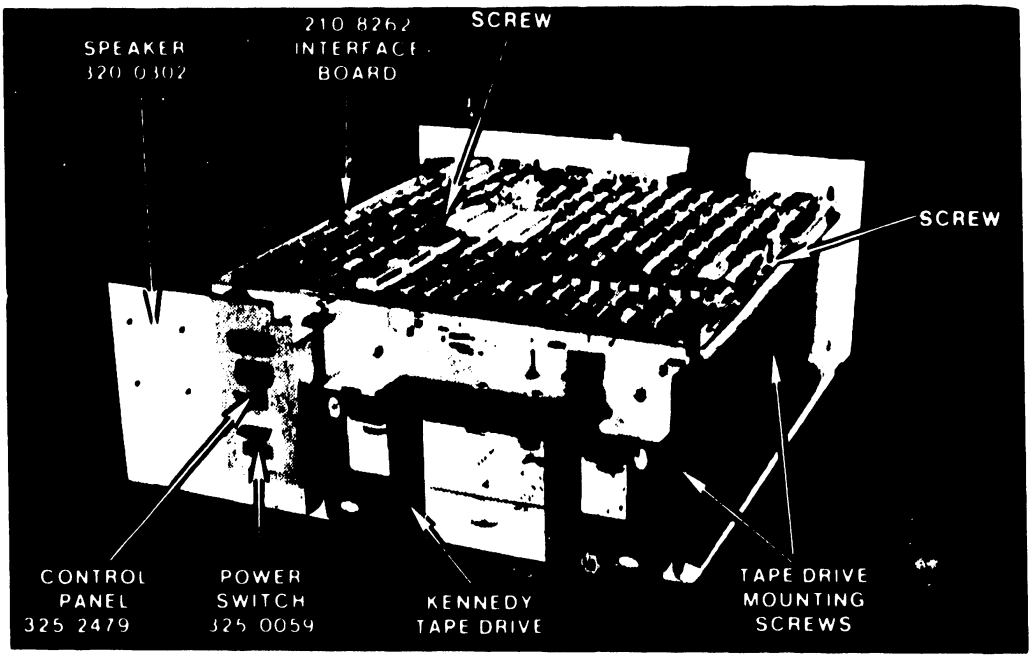


Figure 5-5 Internal Components - Model 6529/2529

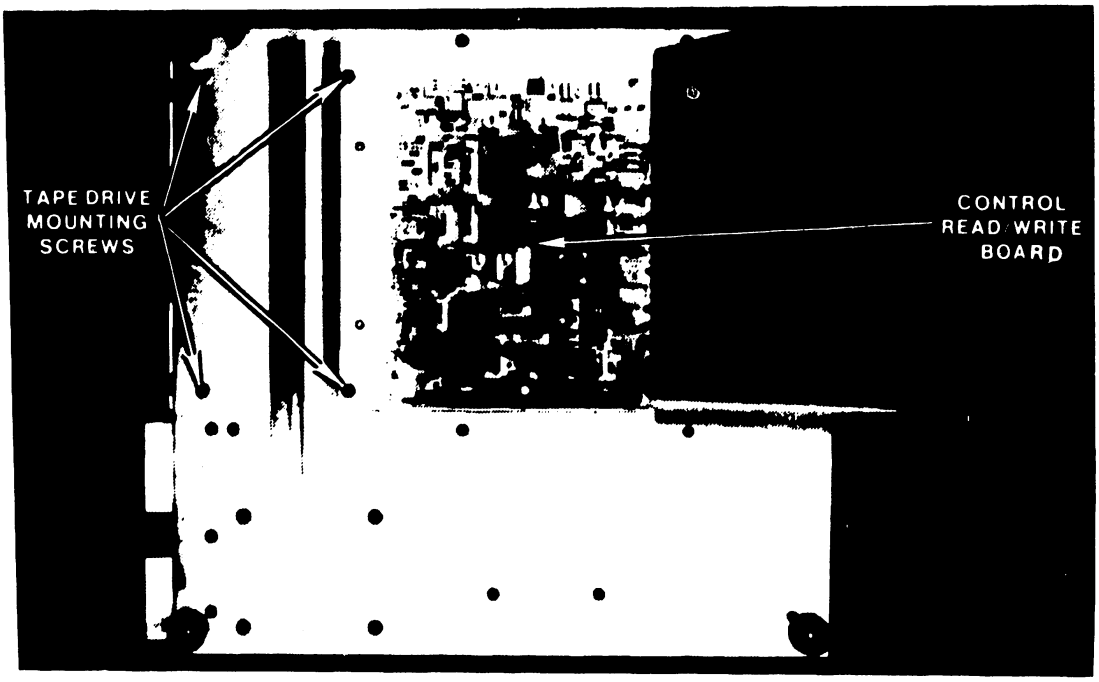


Figure 5-6 Chassis Bottom

5.2.1.8.1 Kennedy Parts Replacement

In order to access the Kennedy replaceable parts it is first necessary to remove the 210-8262 Interface Board (6529/2529V only) and to remove the Kennedy drive from the chassis (see section 5.2.1.8). Ensure that the Interface cable is disconnected but leave the power connector plugged in.

Adjustments and any precautions which should be exercised are described in the procedures which follow. Parts discussed below are shown in Figure 5-7.

5.2.1.8.1.1 Formatter Board Replacement

The formatter board can be removed after removing its four mounting nuts (one in each corner) and all attached cables.

5.2.1.8.1.2 EOT/BOT Infrared Sensor Replacement

a. Remove the formatter PCB (see section 5.2.1.8.1.1).

b. Disconnect the sensor molex connector.

c. Loosen the two sensor retaining screws and remove the sensor.

d. Replace with the new sensor assembly, connecting the sensor molex connector but leaving the retaining screws loose enough for the sensor to be moved.

e. Replace the Formatter PCB.

f. Insert a cartridge and run the "continuous load" test discussed in section 5.2.2.3. When the tape reaches the load point, stop the test and remove the tape.

g. Moving the tape by hand, center the "A" & "B" holes (see Figure 1-1) in front of the reflecting mirror in the cartridge.

h. Place the tape back into the drive. Using an oscilloscope or a voltmeter attached to test point A on the Control/Read/Write board, align the sensor so that the maximum voltage is displayed. (The Control/Read/Write board is located behind the hinged cover on the bottom of the chassis and test points A and B are shown in Figure 5-8).

i. Repeat for hole B using test point B on the Control/Read/Write board.

j. Tighten the sensor retaining screws.

5.2.1.8.1.3 Capstan Motor Replacement

a. Disconnect the motor molex connector from the Control/Read/Write board, located at the bottom of the unit.

b. Using a long Allen wrench (#99-764) loosen the motor clamp screw by gaining access to it via one of the side holes provided for this purpose in the frame (see Figure 5-7).

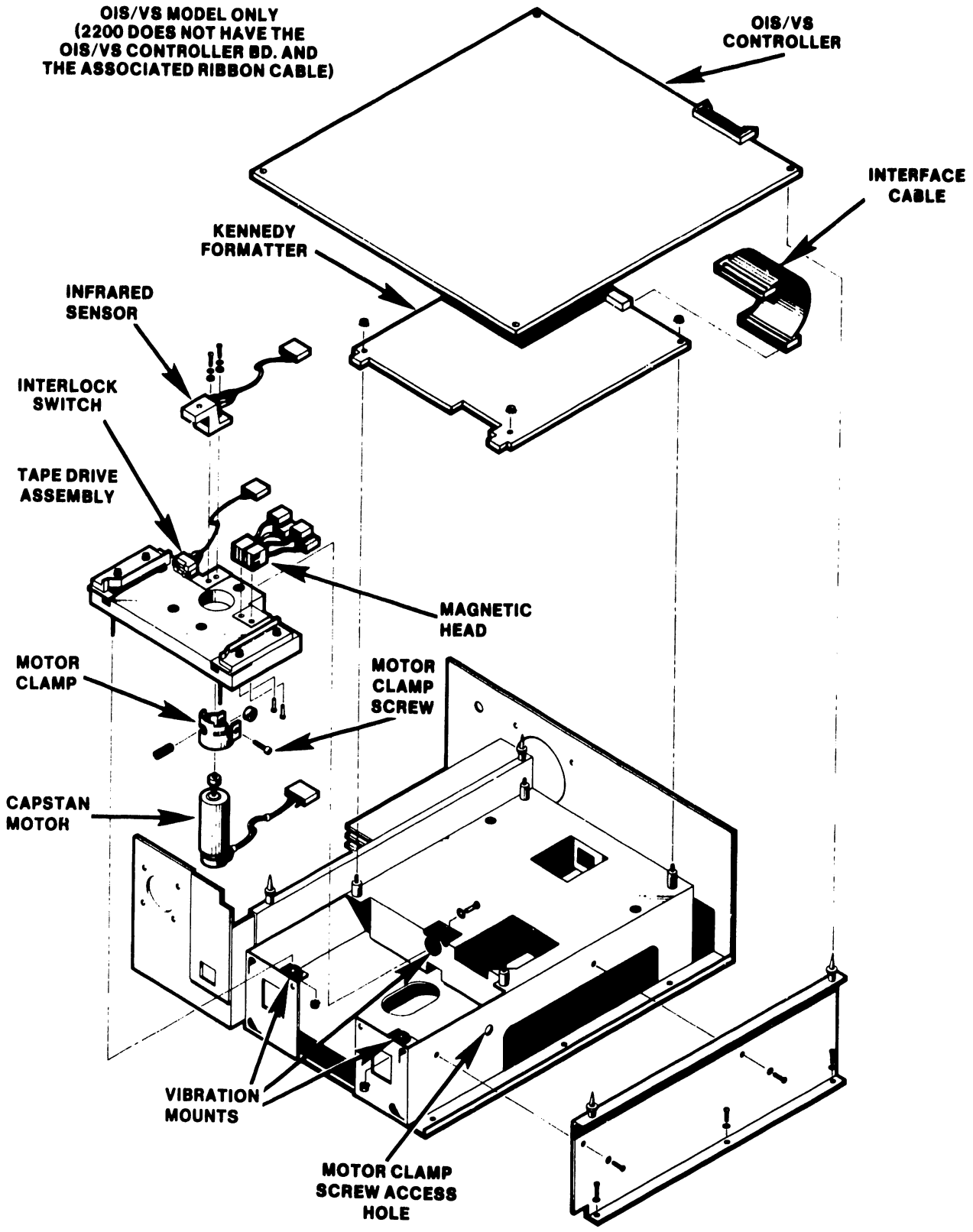


Figure 5-7 Kennedy Replaceable Parts Assembly

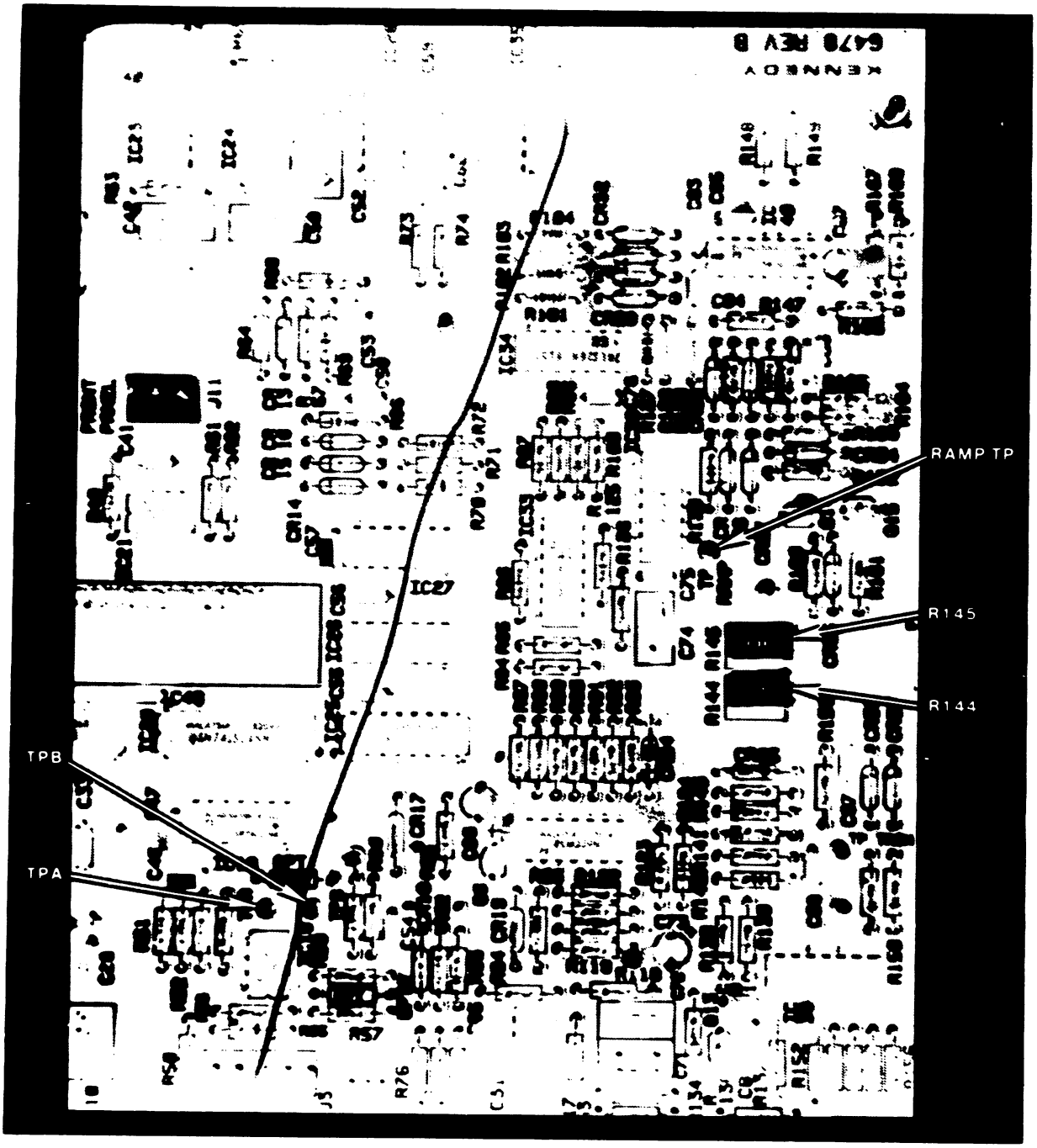


Figure 5-8 Portion of Control/Read/Write Board

c. Slide the old motor out and replace with a new motor, taking care to properly insert the helical tension spring.

d. Insert the tape cartridge and align the motor capstan with the center of the cartridge capstan.

e. Tighten the motor clamp screw, and reconnect the molex connector.

5.2.1.8.1.4 Magnetic Head Replacement

a. Remove the Control/Read/Write board (see section 5.2.1.8.1.6).

b. From underneath the head plate, loosen the head retaining screws and remove the head.

c. Place new head in position, keeping the screws loose enough to allow the head to be relocated.

d. Align the head so that both of its edges are equidistant from the edges of the head plate.

e. Insert the tape cartridge. The tape should make even contact with the read and write head surfaces, and should have equal clearance from the erase head surfaces on both sides.

f. Tighten the head retaining screws, and replace the Control/Read/Write board.

5.2.1.8.1.5 Interlock Assembly Replacement

The interlock assembly is removed by removing the two screws which attach it to the tape drive assembly and then unplugging it from the tape drive assembly.

5.2.1.8.1.6 Control/Read/Write Board Replacement

The Control/Read/Write board board can be removed after removing its four mounting nuts (one in each corner) and all attached cables.

5.2.2 DIAGNOSTICS AND ADJUSTMENTS

5.2.2.1 General

This section describes the on-line and off-line diagnostic routines used to isolate faults within the tape drive.

5.2.2.2 On-Line Diagnostics

The formatter performs a self-test routine prior to each LOAD command. Successful completion of the self-test is required before the rest of the load sequence is allowed to continue. The self-test routine is a loop write to read of a file mark. This effectively stimulates about 80 percent of the formatter circuitry including the data separation circuit. If the self-test fails, further off-line testing is necessary.

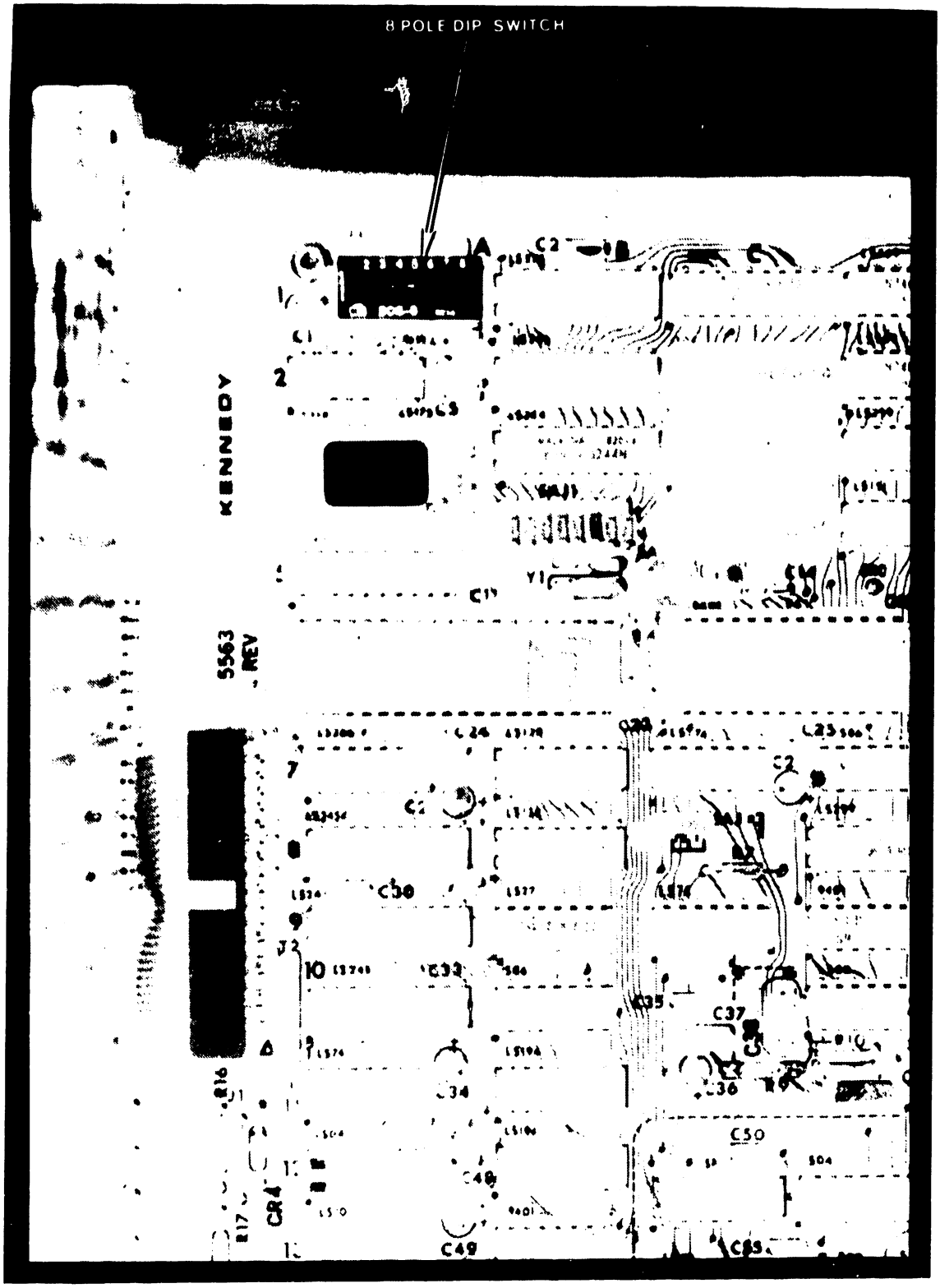


Figure 5-9 Portion of Formatter Board

5.2.2.3 Off-Line Diagnostics

5.2.2.3.1 General

To select the off-line diagnostics, switch 7 of the eight position DIP switch (see Figure 5-9) located on the formatter must be set to the ON position. Ten test routines are then available, as listed in table 5-2. When running the "Continuous Load" test a built-in test is run by the Kennedy formatter to verify the integrity of the 8035 microprocessor and associated PROM. This test asertains that the heart of the system is functional, and ready to execute the selected diagnostics.

a. Set switch 7 to the ON position.

b. Disconnect the interface cable (see Figure 5-7) from the host to protect the formatter interface drivers.

c. Check the tape cartridge to verify that it is NOT in the SAFE position.

d. To run a different test, switch 8 must be set ON then OFF to reset the formatter.

Table 5-2 Off Line Diagnostics Switch Setting Chart

Tape Drive Tests

Test	Switch Setting SW 4321
Continuous Load	0000
Ramp Adjust	0001
Tape Speed Adjust	0010

System Tests

Test	Switch Setting SW 4321
Write File Mark, Continous	0011
Read Continuous	0100
Write Continuous	0101

Formatter Tests
(Remove the tape before running formatter diagnostics)

Test	Switch Setting SW 4321
Controller SA	0110
Read Sequencer SA	0111
Write Sequencer SA	1000
Continous Self-Test	1001

A "1" indicates that the switch should be in the ON position.

5.2.2.3.2 Tape Drive Diagnostics

Continous Load (Switch Setting = 0000)

This routine performs up to 16 continuous LOAD sequences (without the self-test routine). It tests the basic functioning of the 6455 control electronics which allows for the measurement of the duration of the A and B hole signals.

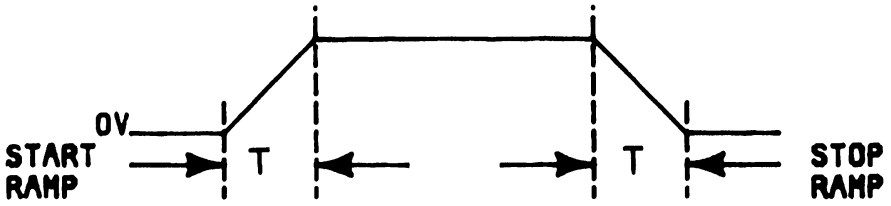
Ramp Adjust (Switch Setting = 0001)

The tape is brought up to speed at a constant, linear acceleration. To control tape velocity, a ramp voltage is generated by the Control/Read/Write board. The voltage rises linearly to the running speed level and falls linearly to zero volt at stop. Ramp time is 25 +0/-3 msec at 30 ips, and varies inversely with speed. The ramp time (T) for different speeds (S) is given by the following formula:

$$T = 30 \times \frac{25}{S} \text{ msec}$$

The ramp adjustment procedure is greatly simplified by using the ramp adjust test in conjunction with potentiometer R145 (see Figure 5-8) which is located on the Control/Read/Write board. NOTE: In some units it may be necessary to remove the tape drive from the Wang chassis (keeping power connected) to access R145. To adjust the ramp, set the diagnostic switch to 0001 and adjust potentiometer R145 until the transport shuttles the tape back and forth. When ramp setting is incorrect, the transport will move the tape in the forward direction only.

Alternately, the ramp time may be observed by placing an oscilloscope probe on the ramp test point (see Figure 5-8) on the Control board and initiating rapid start/stop mode (via the Write Continuous test) long enough to allow the ramp voltage to reach a level. The ramp time is then adjusted using R145 to equal 25 msec as shown below. Make sure the tape is being written in the FORWARD direction before attempting ramp time adjustment with the oscilloscope.



Tape Speed Adjust (Switch Setting = 0010)

This routine initiates continuous writing of file marks to allow for the adjustment of the tape speed using speed adjustment potentiometer R144 (see Figure 5-8) on the Control/Read/Write board. The tape will move in the forward direction until proper speed is achieved, at which point it will shuttle back and forth.

An alternate procedure for setting the speed is described below:

a. Connect channel 1 probe of a dual trace oscilloscope to the write data input. A convenient location would be J1-4 on the Control/Read/Write board, or IC12, pin 17 on the same board (see Figure 5-10). Trigger the scope on channel 1 and select 2 msec/cm time constant and 2V/div. vertical amplitude.

b. Connect channel 2 probe to test point TP1 on the same board and initiate the writing of short blocks (via Write Continuous test) on channel 1, one to ten characters long.

c. Adjust potentiometer R144 on the Control/Read/Write board (clockwise to increase delay or counterclockwise to decrease delay) so that the delay between the leading edges of the read and write data blocks is 10 msec at 30 ips. NOTE: On some units it may be necessary to remove the tape drive from t he Wang chassis (keeping power connected) to access R144. For machines operating at other tape speeds the formula for deriving the proper delay time is:

$$\frac{0.3}{S} = \text{delay in seconds}$$

where S = tape speed in inches per second.

Write File Mark Continous (Switch Setting = 0011)

This routine will write file marks continuously on all tracks. If a bad file mark is written, a space reverse will be performed and a write FM extended.

Read Continuous (Switch Setting = 0100)

This routine will read blocks of data or file marks on all tracks continuously.

Write Continuous (Switch Setting = 0101)

This routine will write short blocks of data on all tracks continuously. If a bad block is written, a space reverse will be performed followed by a write extended routine. This will be repeated, if necessary, until a good block is written.

5.2.2.3.3 Formatter Diagnostics

The formatter diagnostics take advantage of the power of signature analysis (SA) to isolate faults to the component level. Certain jumpers are required to set up the SA tests. These are documented in the user's manual. An HP 5004A signature analyzer is required for these tests as well as for the kernal test for the 8035 processor. The formatter to the drive interface cable must be disconnected to perform SA tests and self-tests. The tape should be removed from the cartridge before operating the following diagnostics.

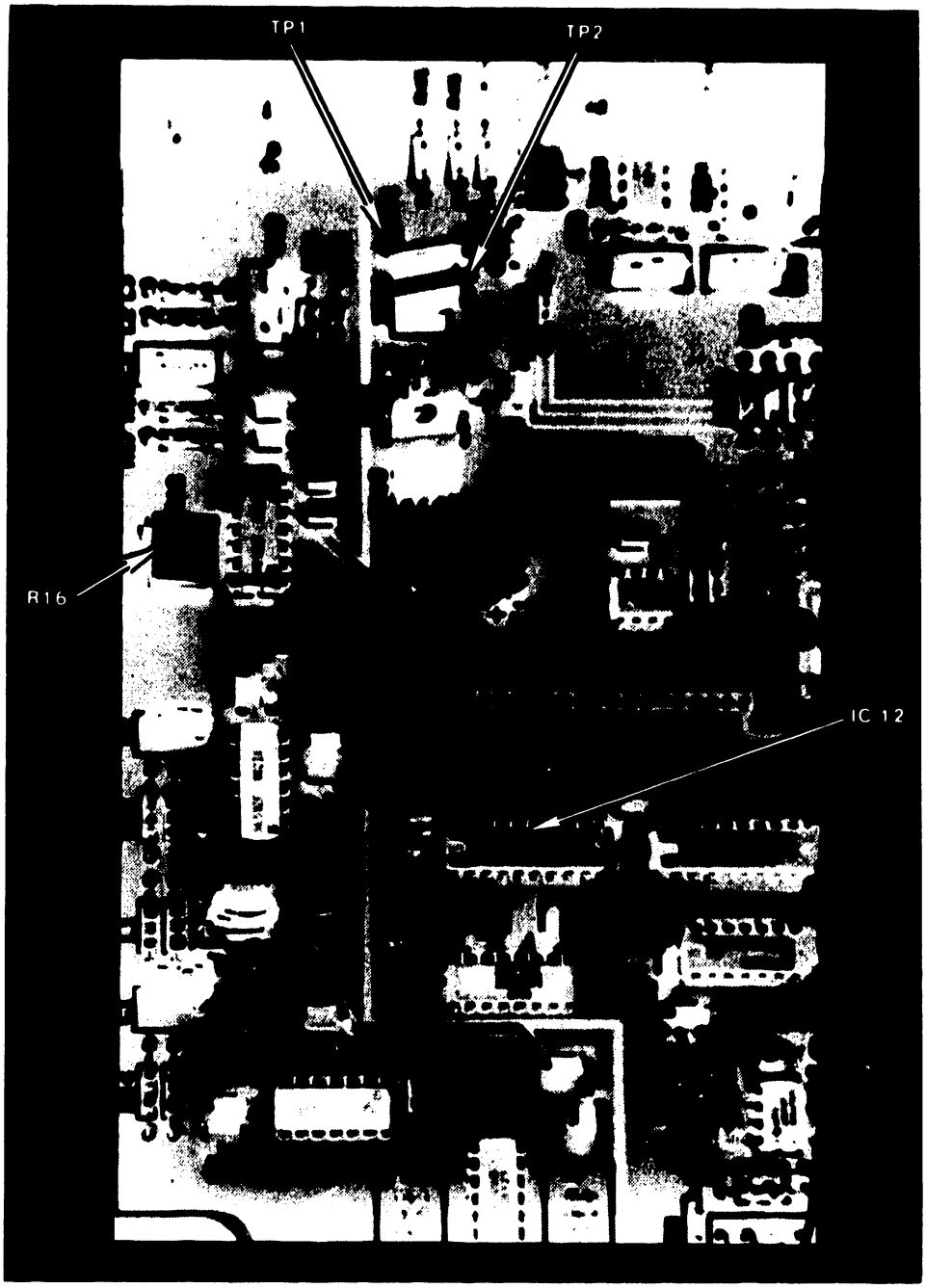


Figure 5-10 Portion of Control/Read/Write Board

Control SA (Switch Setting = 0110)

This routine stimulates all the nodes in the controller section of the formatter so that any faults in this section can be isolated down to the component responsible.

Read Sequencer SA (Switch Setting = 0111)

This routine stimulates all the nodes in the read sequencer section of the formatter so that any faults in this section can be isolated down to the component responsible.

Write Sequencer SA (Switch Setting = 1000)

This routine stimulates all the nodes in the write sequencer section of the formatter so that any fault in this section can be isolated down to the component responsible.

Continuous Self-Test (Switch Setting = 1001)

This routine performs continuous self-test routines that allow the data separator section, including the phase lock loop, to be tested and adjusted. This is also a good verification of the functioning of the formatter as a whole.

Short and Long Loads (Switch Setting = 1xxxxx)

In the ON position, this switch selects the short mode of tape loading. In the OFF position, the long, or normal mode, is selected. In the normal mode, the transport will move the tape forward in high speed to the end of the tape; then rewind it to beginning of tape, optimizing tape tension for data transfer operations. In the short load mode, used in testing and diagnostics, the transport will rewind the tape directly to the load point.

5.2.2.4 Formatter and Deck Adjustment Procedures

5.2.2.4.1 Formatter VCO Center Frequency Adjustment Procedure

Required equipment: frequency counter and adjustable DC power supply.

a. Remove jumpers at SAJ6 and JP1 (see Figure 5-11) on the Formatter board.

b. Measure the regulated output of VCO voltage regulator RG2 and adjust the DC power supply output to the measured value minus 0.8V. Thus, if RG2 ouput measures 5.1V, adjust the power supply to 4.3V.

c. Connect the power supply to top pin of JP1.

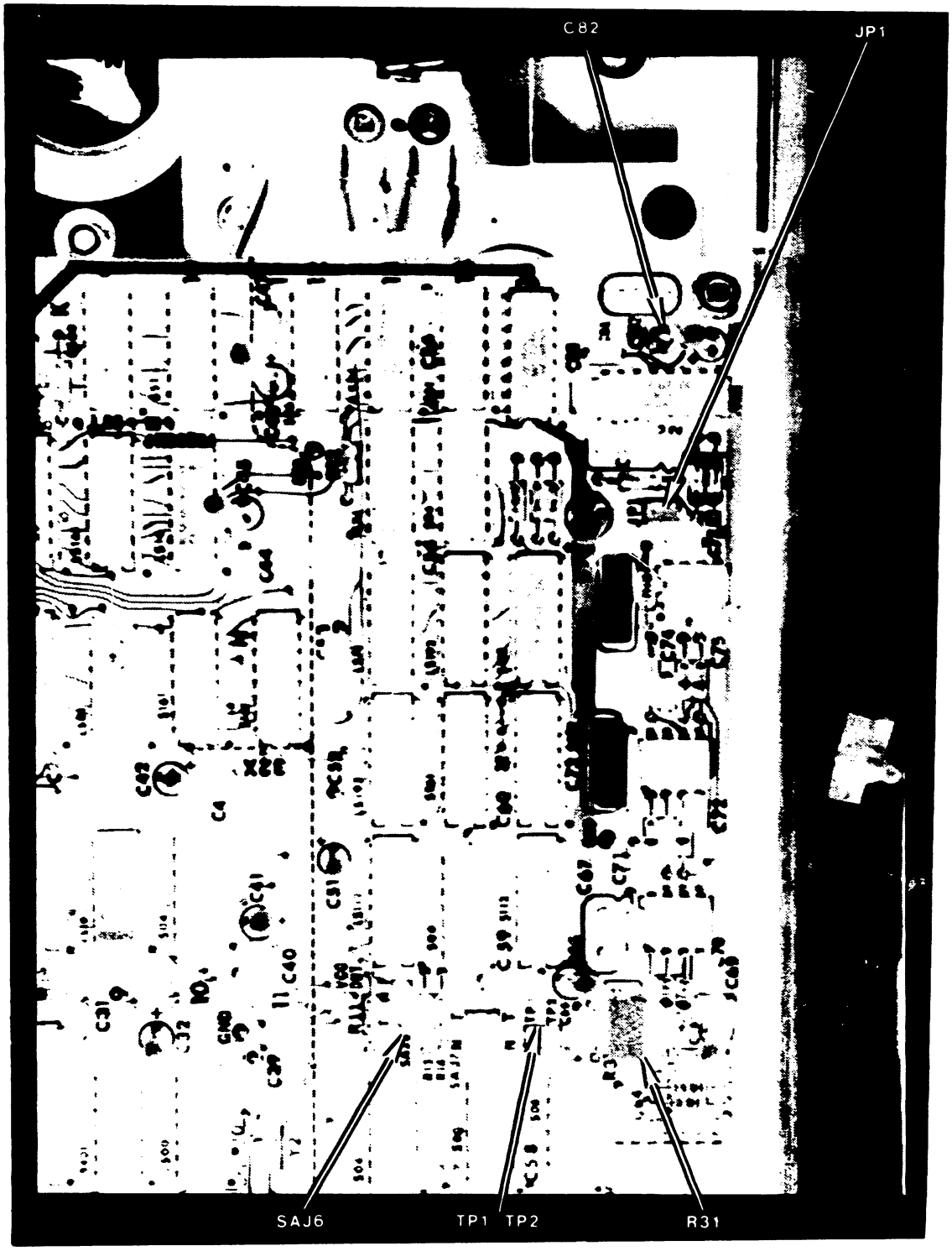


Figure 5-11 Portion of Formatter Board

d. Connect the frequency counter to the left most pin of SAJ6 and adjust trimmer capacitor C82 (see Figure 5-11) until the VCO center frequency measures 3.84 MHz +/-10 KHz.

e. Replace the jumpers at JP1 and SAJ6, the latter in the "normal" N position.

5.2.2.4.2 Formatter Integrator Offset Adjustment

Required equipment: oscilloscope.

a. Set the oscilloscope to 0.1 usec/division, 2V/division, and display channels 1 and 2.

b. Connect oscilloscope probes to TP1 and TP2 (see Figure 5-11) on the Formatter board.

c. Adjust potentiometer R31 (see Figure 5-11) on the Formatter board until the leading edges of the two displayed waveforms coincide.

5.2.2.4.3 Recorder Read Amplitude Adjustment Procedure

Required equipment: oscilloscope.

a. Set switches 1, 2 and 8 of the eight position diagnostic switch located on the Formatter board to the ON position then reset switch 8 OFF.

b. Set the oscilloscope to 0.5V/division, invert channel 2, add channels 1 and 2.

c. Connect the oscilloscope probes to test points 1 and 2 (see Figure 5-10) on the Control/Read/Write PC board located on the bottom of the unit.

d. Adjust potentiometer R16 (see Figure 5-10) on the Control/Read/Write PC board until displayed voltage measures 3V peak to peak (individual channels should read 1.5V). NOTE: On some units it may be necessary to remove the tape drive from the Wang chassis (keeping power connected) to access R16.

5.2.2.4.4 Infrared Sensor Check

The infrared sensors detect the A and B holes in the tape. The sensors are designed for maximum reliability and immunity to ambient light conditions. If the EOT or BOT are not properly detected, check the sensors as follows:

a. Disconnect the capstan motor by unplugging the molex connector.

b. Insert a tape cartridge.

c. Connect an oscilloscope probe or a voltmeter to test point A (see Figure 5-8) of the Control/Read/Write board.

d. Turn the capstan by hand until the small A hole is opposite the A sensor. Voltage at test point A should measure approximately 4 volts.

e. Connect the oscilloscope probe or voltmeter to test point B on the Control/Read/Write board.

f. Turn the capstan by hand to the double set of large holes. Voltage at test point B should measure approximately 4 volts.

g. Reconnect the capstan motor.

5.2.2.4.5 Interlock Switch Check and Adjustment

If the CARTRIDGE IN PLACE (CIP) signal does not go true when the cartridge is inserted:

a. Insert the tape cartridge until it begins to engage with the latching mechanism. Contacts on both interlock switches should begin to open.

b. Press the cartridge inward until it locks in place. Switch contacts should close completely. (This can be checked by gently pressing the switch contact toward the switch body. Any movement indicates contact is not completely closed.)

Adjustment

If the contact will not close completely, loosen the switch mounting screw and readjust the switch position for complete contact closure.

CHAPTER 6 SCHE-MATICS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

7.1 PARTS LIST AND ILLUSTRATIONS REFERENCE NOTE

The part numbers of field replaceable parts are given in the illustrations included in Chapters 4 and 5. Chapter 5 contains illustrations showing the location of the major components and describes how the components are removed.

CHAPTER 8

TROUBLE-SHOOTING

CHAPTER 8

TROUBLESHOOTING

8.1 TROUBLESHOOTING FLOW DIAGRAMS

The diagrams that follow are prepared as an aid in troubleshooting. Figure 8-1 presents a logical troubleshooting procedure for the Model 2229 and Figure 8-2 does the same for Model 2529/6529.

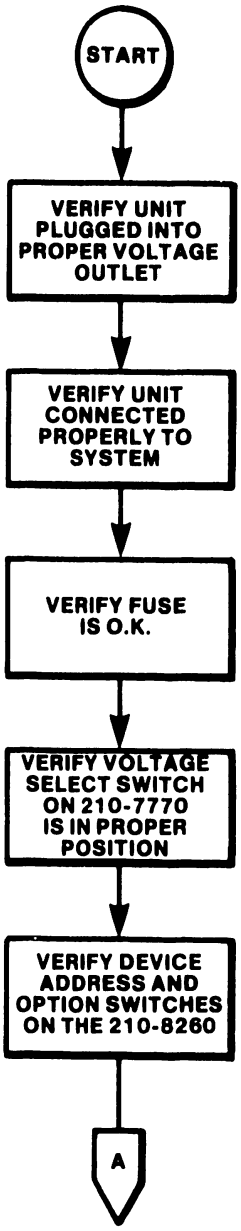


Figure 8-1 Troubleshooting Flow Diagram for Model 2229. (Sheet 1 of 3)

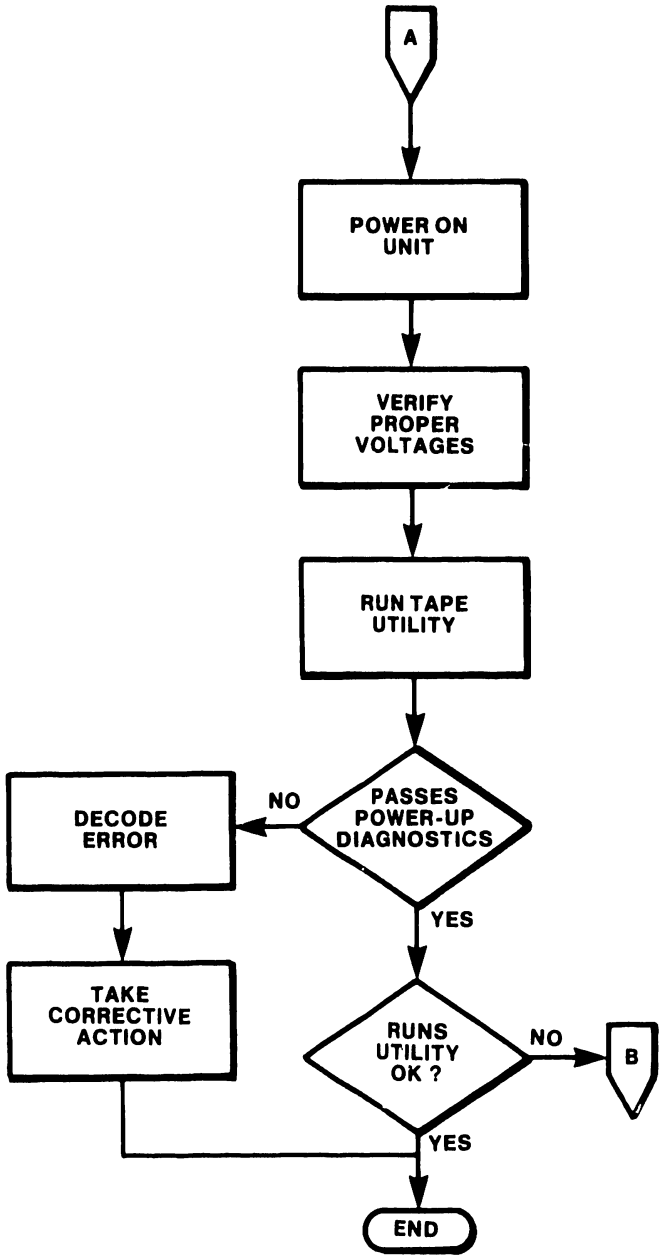


Figure 8-1 Troubleshooting Flow Diagram for Model 2229.
(Sheet 2 of 3)

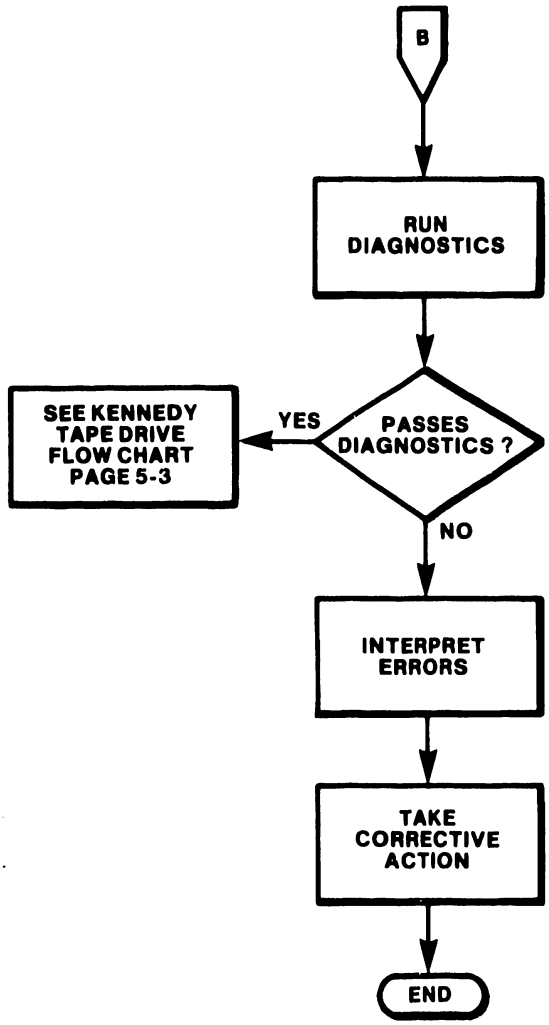


Figure 8-1 Troubleshooting Flow Diagram for Model 2229.
(Sheet 3 of 3)

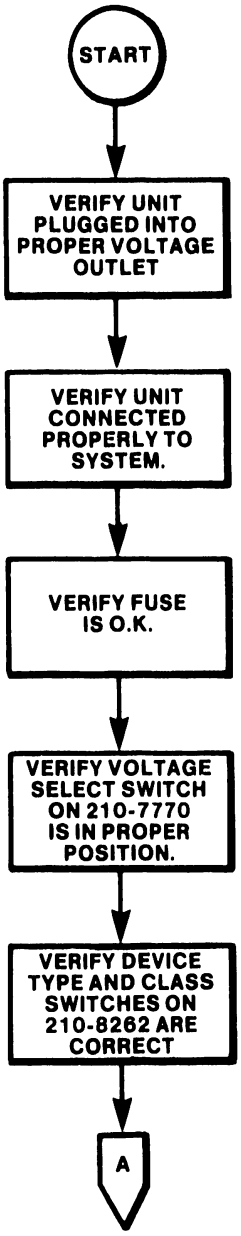


Figure 8-2 Troubleshooting Flow Diagram for Model 2529/6529.
(Sheet 1 of 3)

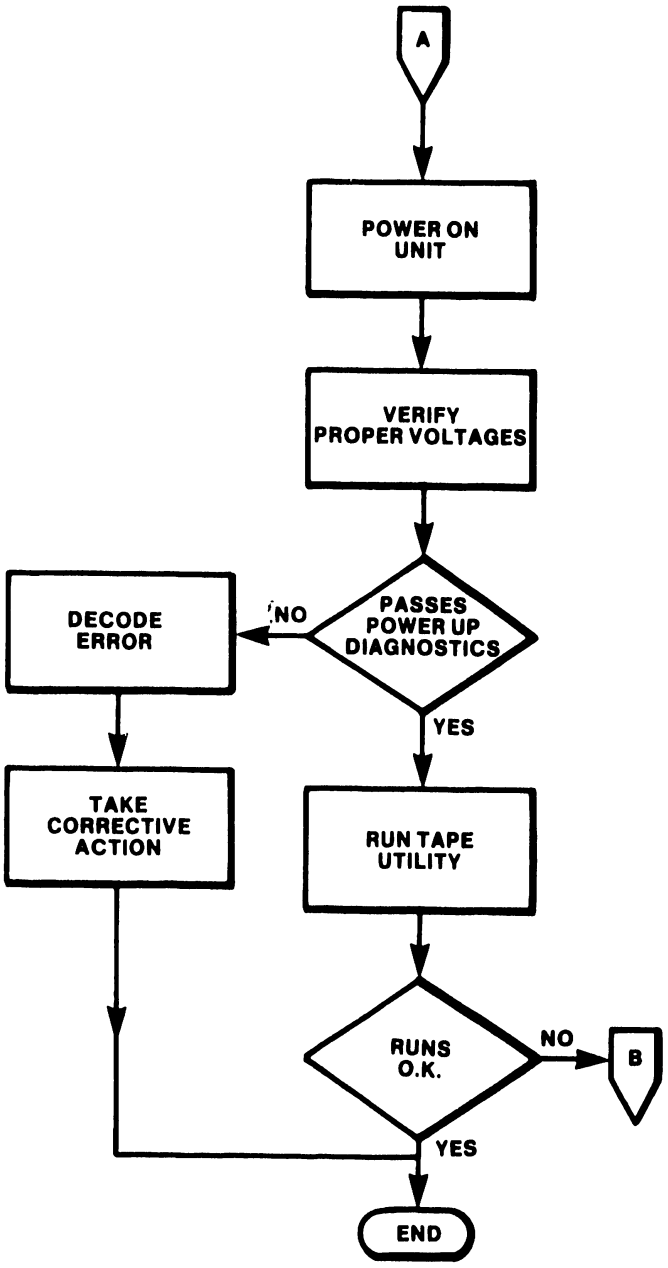


Figure 8-2 Troubleshooting Flow Diagram for Model 2529/6529.
(Sheet 2 of 3)

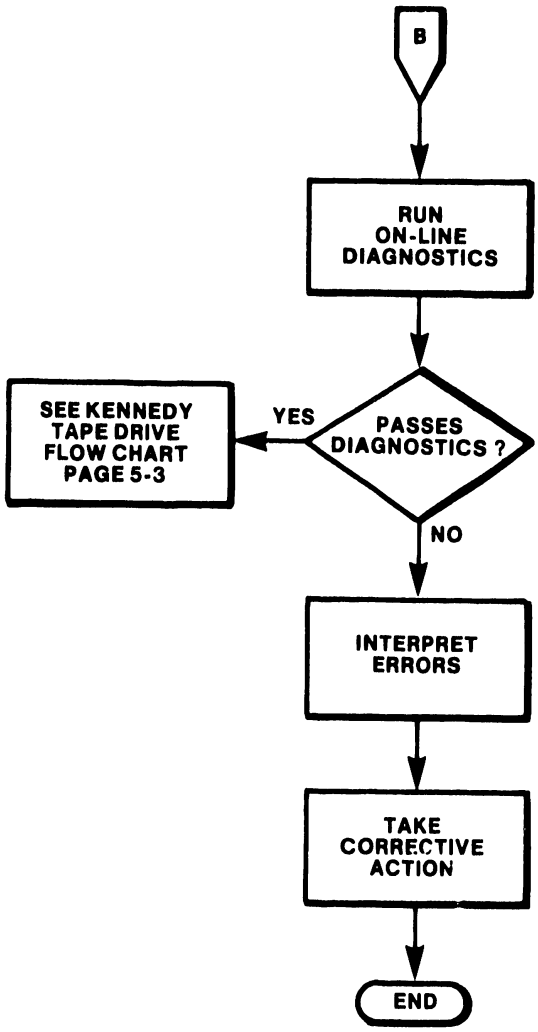


Figure 8-2 Troubleshooting Flow Diagram for Model 2529/6529.
(Sheet 3 of 3)

8.2 DIAGNOSTICS

Part numbers for available diagnostics are as follows:

Model 2529V
VS Online Diagnostic Test Operating System Device 3 Monitor
195-2604-3

Model 6529
OIS Device 3 Monitor
195-2489-3

Model 2229
2200 ACTD Diagnostic
195-2551-3 (Single Sided, Single Density - without listing)
195-2552-3 (Single Sided, Single Density - with listing)

Model 6529/2529V
Archiving Cartridge Tape Built In Test - 195-2477-3
PROM Part Number: 378-8012R1
Software Part Number: 702-0234
Documentation Part Number: 760-1081

NOTE

See Table 8-1 for Built in Test Error Report.
See Table 8-2 for Diagnostic Switch Settings on 210-8262A PCB.

Table 8-1 Built in Test Error Report

LED VALUE	LED3	LED2	LED1	LED0	LOCATION	PROBABALE FAILING UNIT
01	OFF	OFF	OFF	ON	L91	MEM CHIP #1
02	OFF	OFF	ON	OFF	L101	MEM CHIP #2
03	OFF	OFF	ON	ON	L110	MEM CHIP #3
04	OFF	ON	OFF	OFF	L111	MEM CHIP #4
05	OFF	ON	OFF	ON	L121	MEM CHIP #5
06	OFF	ON	ON	OFF	L131	MEM CHIP #6
07	OFF	ON	ON	ON	L132	MEM CHIP #7
08	ON	OFF	OFF	OFF	L142	MEM CHIP #8
09	ON	OFF	OFF	OFF	L152	PARITY CHIP
0A	ON	OFF	ON	OFF	L54	DMA CHIP
0B	ON	OFF	ON	ON	N/A	LOOP BACK CIRCUITRY
0C	ON	ON	OFF	OFF	L47	CTC CHIP
0D	ON	ON	OFF	ON	L54	DMA CHIP
0E	ON	ON	ON	OFF	L47	CTC CHIP
0F	ON	ON	ON	ON	N/A	TAPE INTERFACE CIRCUITRY

Table 8-2 Diagnostic Switch Settings on 210-8262 PCB

SWITCHES 1-4	Used for device selection. Should be configured to 1010 (HEX A) at all times.
SWITCH 5	LOOP ON BUILT IN TEST: Enable switch 5 to loop on the BIT.
SWITCH 6	LOOP ROUTINE: Enable switch 6 to Loop on ROUTINE. With the Z-bug properly connected to the 8262 board, the program counter is set to the beginning og the routine and a trap at the end of the routine is also set. This area of code is executed repeatedly until switch 6 is turned off.
SWITCH 7	LOOP ON ERROR: Enable switch 7 to Loop on ERROR. The test causing the error is executed repeatedly until the error is fixed or the switch is turned off.
SWITCH 8	BY-PASS BIT: Enable switch 8 to by-pass the Built In Test. This will be done when the operator wishes to run 'Master Resident Slave Lower RAM' to diagnose boards.

SWITCH SELECTION FOR 8262 BOARD SW1

!OFF ON!		
! [1] !	-- DEVICE SELECTION	
! [2] !	-- DEVICE SELECTION	*
! [3] !	-- DEVICE SELECTION	
! [4] !	-- DEVICE SELECTION	*
! [5] !	-- LOOP ON BIT	
! [6] !	-- LOOP ON ROUTINE	
! [7] !	-- LOOP ON ERROR	
! [8] !	-- BY-PASS POWER-UP	

NOTE

ALL SWITCHES ARE ON ACTIVE.

HIGH ORDER SWICHES USED FOR DIAGNOSTIC CONTROL ONLY.

* INDICATES SWITCHES MUST BE ON FOR DEVICE SELECTION.

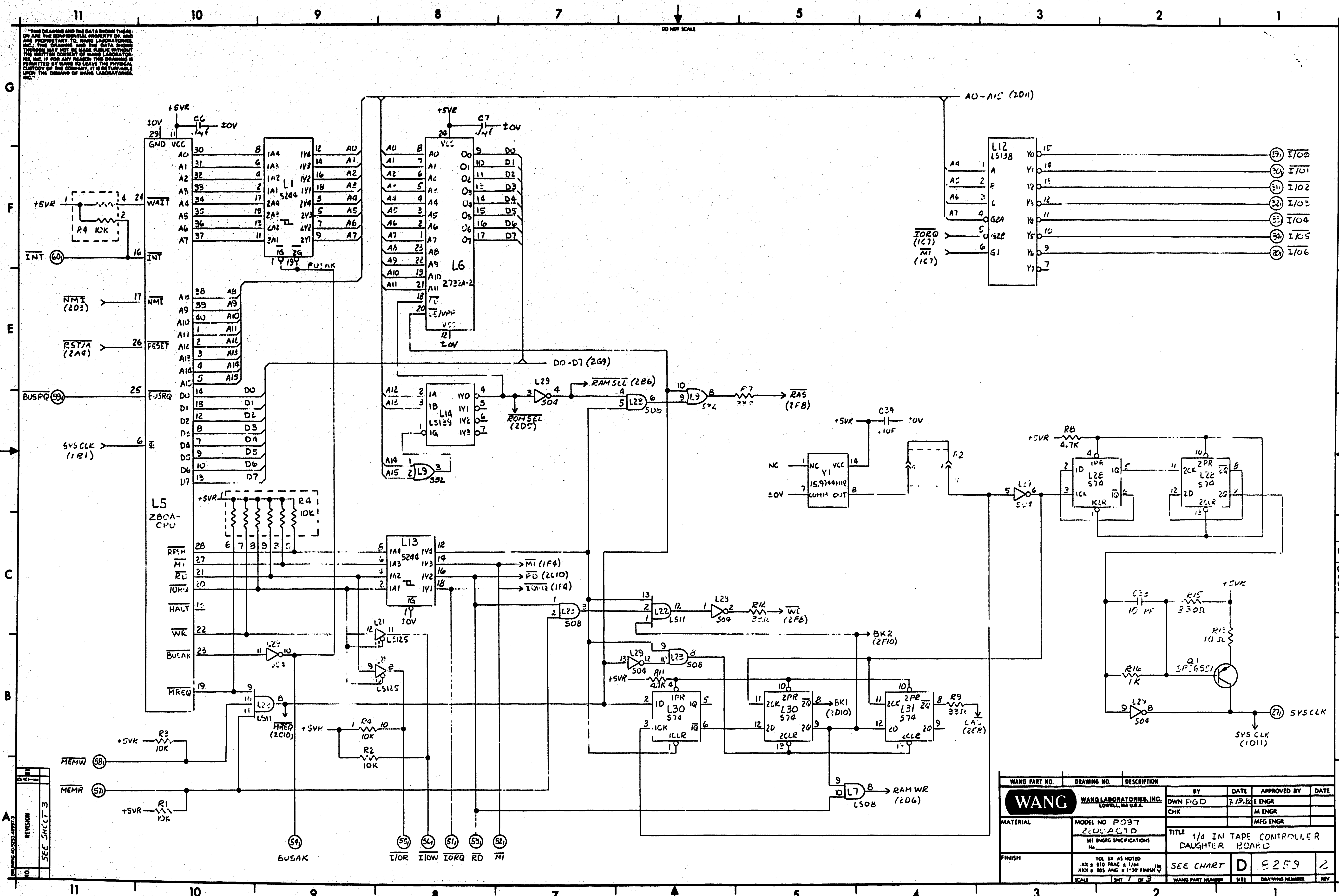
CHAPTER 6 SCHE-MATICS

CHAPTER 6

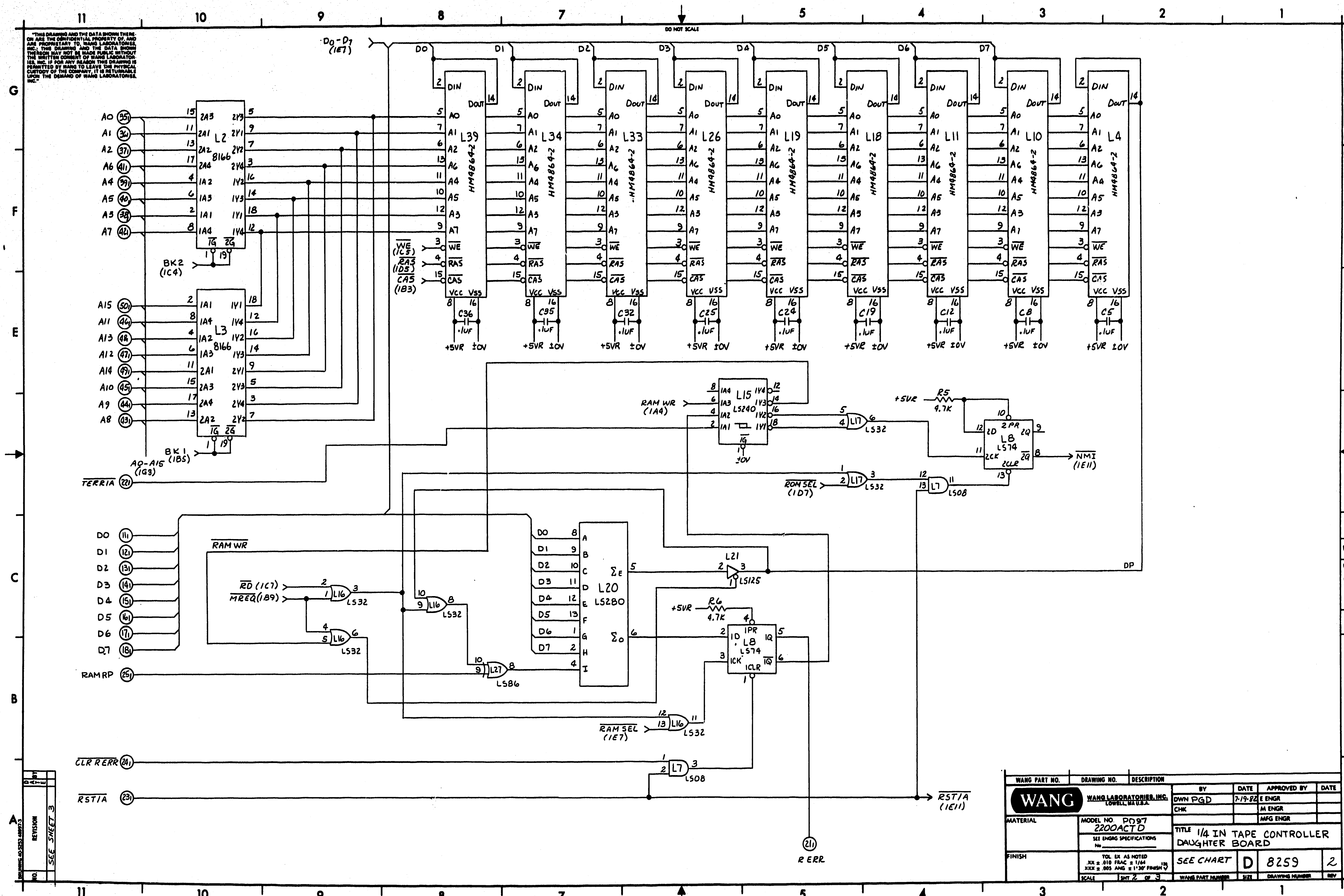
SCHEMATICS

This chapter contains the following schematic drawings:

210-8259	1/4" Tape Controller Daughterboard
210-8260	1/4" Tape Controller Motherboard
210-8261	Tape Interface
210-8262-A	1/4" Cartridge Tape Slave
210-7770	Power Supply
650 Formatter, Type 5563	
Control, Read/Write Board, Type 645	



DO NOT SCALE
A0-A15 (2D11)
D0-D7 (2G9)
L5 Z80A-CPU
L1 S244
L6 2732A-2
L12 LS138
L13 S244
L14 LS139
Y1 15.9744MHZ
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
INT
NMI (2D3)
RST/A (2A9)
BUSRQ
SYS CLK (1E1)
IORQ (1C7)
M1 (1C7)
RAM SEL (2B6)
ROM SEL (2D5)
RAS (2F8)
M1 (1F4)
RD (2C10)
IORQ (1F4)
WE (2F6)
BK2 (2F10)
BK1 (2D10)
CAS (2E8)
RAM WR (2D6)
MREQ (2C10)
MEMW
MEMR
BUSAK
I/OR
I/OW
IORQ
RD
M1
SYS CLK
SYS CLK (1D11)
WANG PART NO.
DRAWING NO.
DESCRIPTION
WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
BY
DATE
APPROVED BY
DATE
DWN PGD
7.19.86
E ENGR
CHK
M ENGR
MFG ENGR
MATERIAL
MODEL NO P097
2200AC1D
SEE ENGRG SPECIFICATIONS No
TITLE 1/4 IN TAPE CONTROLLER DAUGHTER BOARD
FINISH
TOL EX AS NOTED
.XX ± 010 FRAC ± 1/64
.XXX ± 005 ANG ± 1°30' FINISH
SCALE
SHT 1 OF 3
SEE CHART
D
8259
2
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV
REVISION
SEE SHEET 3
D 8259



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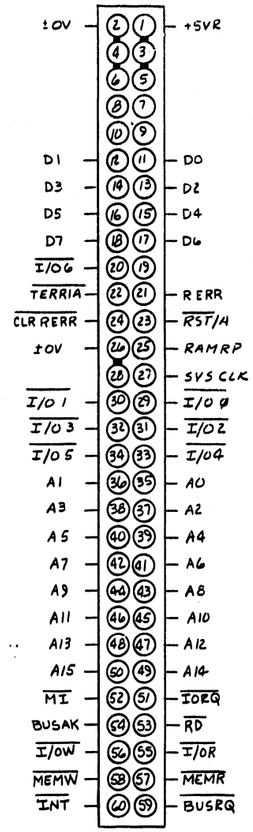
DO NOT SCALE
D0-D7 (1E7)
L2 8166
L3 8166
L39 L34 L33 L26 L19 L18 L11 L10 L4
HM4864-2
BK2 (1C4)
BK1 (1B5)
A0-A15 (1G3)
TERRIA
WE (1C5)
RAS (1D5)
CAS (1B3)
+5VR ±0V
RAM WR (1A4)
L15 LS240
L17 LS32
L8 LS74
NMI (1E11)
ROM SEL (1D7)
L7 LS08
L20 LS280
L21 LS125
L16 LS32
L27 LS86
RD (1C7)
MREQ (1B9)
RAM WR
RAM RP
RAM SEL (1E7)
CLR RERR
RST/A
RST/A (1E11)
R ERR
DP
REVISION
SEE SHEET 3
WANG PART NO.
DRAWING NO.
DESCRIPTION
WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
BY
DATE
APPROVED BY
DATE
DWN PGD
7-19-82
E ENGR
CHK
M ENGR
MFG ENGR
MATERIAL
MODEL NO. PO97
2200ACT D
SEE ENGRG SPECIFICATIONS No.
TITLE 1/4 IN TAPE CONTROLLER DAUGHTER BOARD
FINISH
TOL. EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH
SEE CHART
D
8259
2
SCALE
SHT 2 OF 3
WANG PART NUMBER
SIZE
DRAWING NUMBER
REV

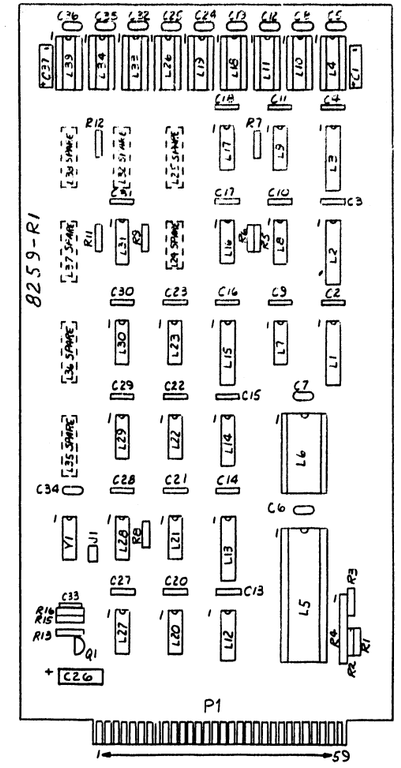
DO NOT SCALE

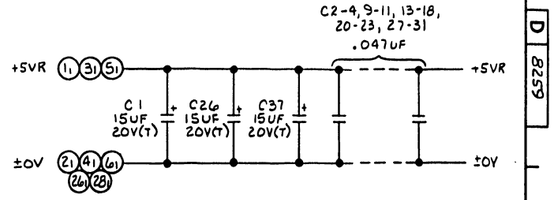
I.C. LOCATION	TYPE	W.L. PART NO.
L1,18	74S244	376-0338
L2,3	8166	376-0553
L4,10,11,18,19, 26,33,34,39	HM4864-2	SEE CHART
L5	Z80A-CPU	SEE CHART
L6	2732A-2	SEE CHART
L7	74LS08	376-0153
L8	74LS74	376-0156
L9	74S32	376-0205
L12	74LS138	376-0294
L14	74LS139	376-0226
L15	74LS240	376-0297
L16,17	74LS32	376-0211
L20	74LS280	376-0242
L21	74LS125	376-0486
L22	74LS11	376-0225
L23	74S08	376-0200
L24,25,32,35-38	SPARE	
L27	74LS86	376-0231
L28,30,31	74S74	376-0202
L29	74S04	376-0197
L4,10,11,18,19, 26,33,34,39	SOCKET, 16 PIN	376-9002
L5	SOCKET, 40 PIN	376-9011
L6	SOCKET, 24 PIN	376-9003

COMPONENT	TYPE	W.L. PART NO.
R1-3	10K 1/4W 5%	330-4011
R4	10K SIP	333-0809
R5,6,8,11	4.7K 1/4W 5%	330-3048
R7,9,12	33Ω 1/4W 5%	330-1034
R13	10Ω 1/4W 5%	330-1011
R15	330Ω 1/4W 5%	330-3334
R16	1K 1/4W 5%	330-3011
C1,26,37	15uF 20V(T)	300-4022
C2-4,9-11, 13-18,20-23, 27-31	.047uF 50V	300-1966
C5-8,12,19,24, 25,32,34-36	.1uF 50V	300-1930
C33	10pF 500V	300-1010
Y1	15.9744MHZ	321-0059
Q1	SPS6551	375-1050

MNEMONICS	COORD.
A1-A15	2G11
BUSAK	1A9
BUSRQ	1D11
CLR RERR	2A11
D0-D7	2C11
INT	1F11
I/OR	1A8
IORQ	1A8
I/OW	1A8
I/O0-I/O6	1F1
MI	1A7
MEMR	1A11
MEMW	1A11
RAMRP	2B11
RD	1A8
RERR	2A5
RST/A	2A11
SYS CLK	1B1
TERRIA	2D11







IC TYPE	LOCATION	SPARES
74S08	L23	1
74LS08	L7	1
74LS11	L22	1
74S32	L9	2
74LS32	L17	2
74S74	L31	1
74LS86	L27	3
74LS125	L21	1
74LS139	L14	1
74LS240	L15	1
74S244	L13	1

210 = 209 + 377 OR 378				
210	209	L4,10,11,18,19,26,33,34,39	L5	L6
8259-A	8259	377-0417	377-0368	378-9037

NOTE: UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W 5%.

E-REV
O

DASH NO.	REVISION	BY	DATE
0	ORIGINATED PER DWG # E1681	P&D	7-19-82
1	REVISED PER ECO # 23211	D.S.	12-6-82
2	APPD: [illegible]	[illegible]	3-12-83

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

BY	DATE	APPROVED BY	DATE
DWN P&D	7-19-82	E ENGR K. BUTLER	8-4-82
CHK [illegible]	8-4-82	M ENGR	
		MFG ENGR	

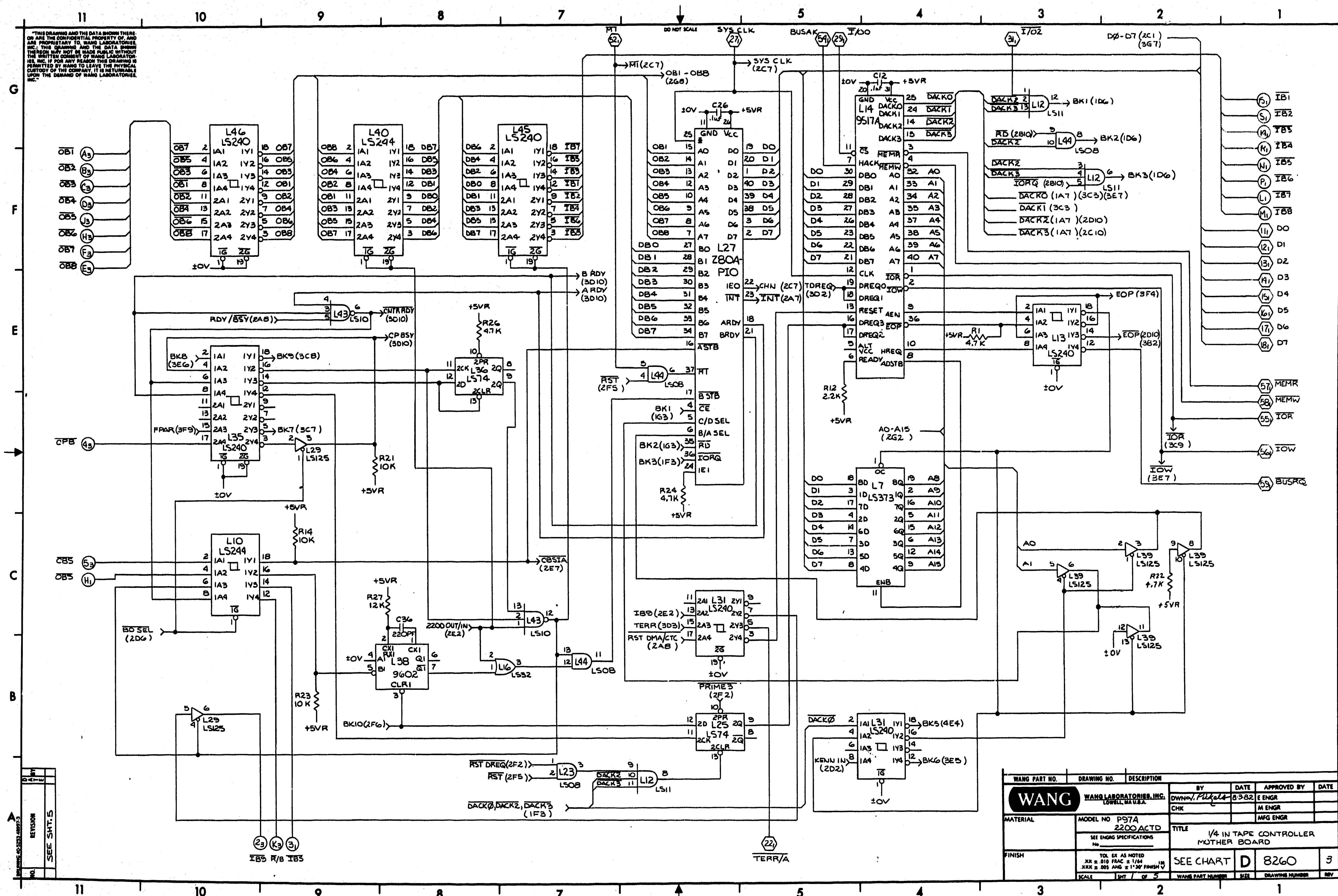
MATERIAL — MODEL NO P097 2200ACTD — SEE ENGRG SPECIFICATIONS No. _____

FINISH — TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH 125

TITLE 1/4 IN TAPE CONTROLLER DAUGHTER BOARD

SCALE — SHT 3 OF 3 — SEE CHART — WANG PART NUMBER — D — SIZE — 8259 — DRAWING NUMBER — 2 — REV

8259



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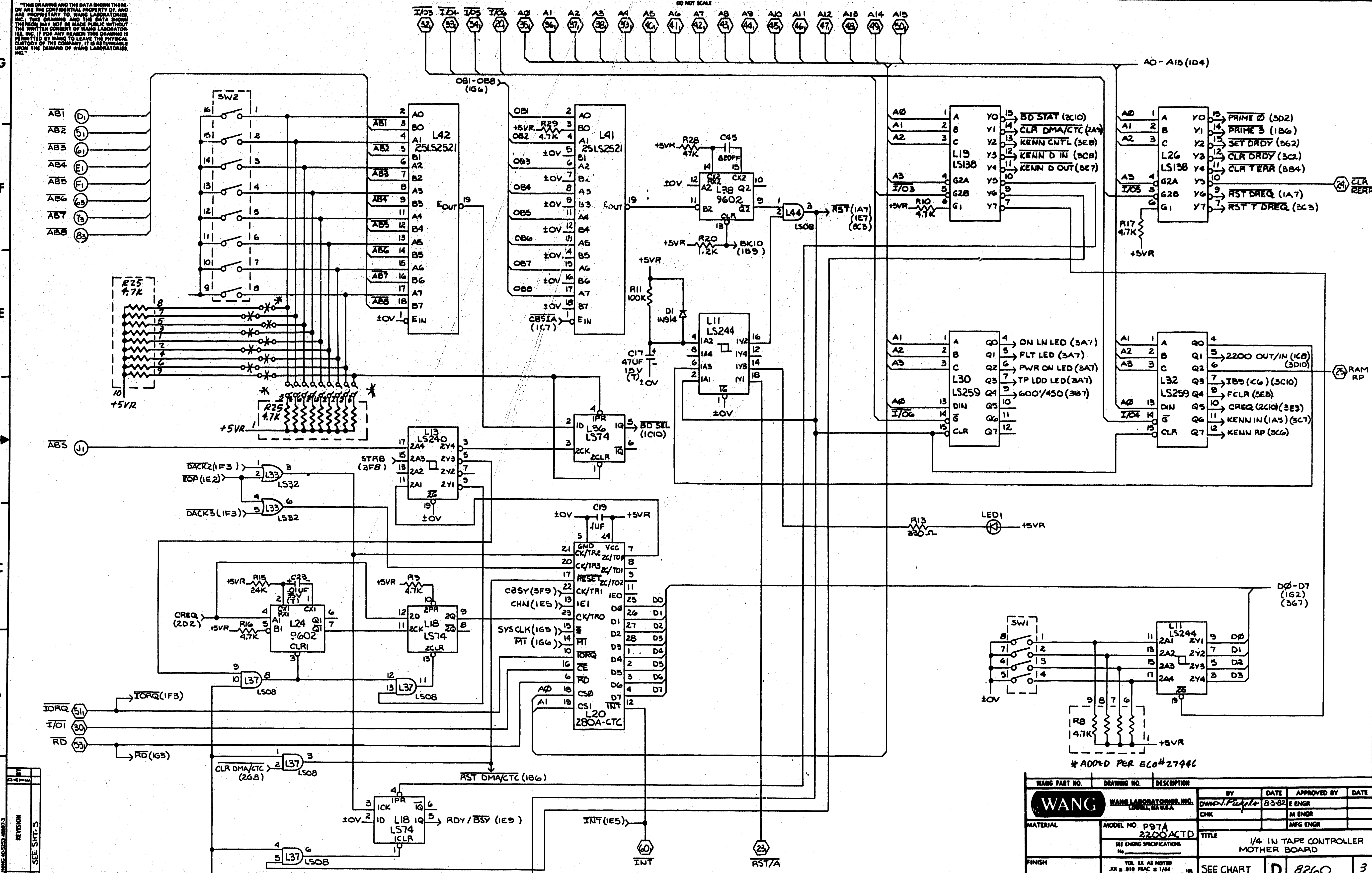
DO NOT SCALE
L14 9517A
L27 Z80A-PIO
L7 LS373
L10 LS244
L38 9602
WANG
WANG LABORATORIES, INC. LOWELL, MA U.S.A.
MODEL NO P97A 2200 ACTD
TITLE 1/4 IN TAPE CONTROLLER MOTHER BOARD
SEE CHART
D
8260
3
SHT 1 OF 5
REVISION SEE SHT. 5



WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG — WANG LABORATORIES, INC. LOWELL, MA U.S.A.

BY	DATE	APPROVED BY	DATE
DWN J. Pickelo	8-3-82	E ENGR	
CHK		M ENGR	
		MFG ENGR	

MATERIAL

MODEL NO. P97A 2200 ACTD

SEE ENGRG SPECIFICATIONS No.

FINISH

TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH

SCALE — SHT 2 OF 5

TITLE 1/4 IN TAPE CONTROLLER MOTHER BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	8260	3

DO NOT SCALE

STRB (1C2) +5VR R4 10K
CBSY (1C2) +5VR R5 10K
DBSY (1C2) +5VR R6 10K
FPAR (1C2) +5VR R7 10K
CMDN (1C2) +5VR R3 10K
ONLN (1C2) R18 10K +5VR

L9 LS240 — 2A1 2Y1, 2A2 2Y2, 2A3 2Y3, 2A4 2Y4; 1G 2G; ±0V
L10 LS244 — 2A1 2Y1, 2A2 2Y2, 2A3 2Y3, 2A4 2Y4; 1G 2G; ±0V

STRB(2D8)
CBSY(2C7)
F PAR (1D10)
KENN CNTL (2F3)
L29 LS125

D0 - D7 (1G2) (2C1)

L5 LS534 — D1 D2 D3 D4 D5 D6 D7 D8; O1 O2 O3 O4 O5 O6 O7 O8; CP OE
L3 LS245 — A1 A2 A3 A4 A5 A6 A7 A8; B1 B2 B3 B4 B5 B6 B7 B8; DIR OE; ±0V
BK6 (1A4)

KENN D OUT (2F3)
DACK0 (1F8)
IOW (1D2)
L33 LS32
L21 LS11
BK8 (1E10)

EOP(1E2) L23
BK5(1B4)

+5VR R2 4.7K
L15 LS74 — 1PR 1CK 1D 1Q 1CLR
SET DRDY (2F2)
L15 LS74 — 2PR 2CK 2D 2Q 2CLR
L22 LS08

BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7

L9 LS240 — 1A3 1Y3, 1A1 1Y1, 1A2 1Y2, 1A4 1Y4; ±0V
FCLR (2D2)
CREQ(2D2)
DRDY FCLR CREQ HPAR

L1 LS86

PRIME Ø (2G2)
L25 LS74 — 1PR 1CK 1D 1Q 1CLR
TDREQ(1E5)

L6 LS244 — 1A1 1Y1, 1A2 1Y2, 1A3 1Y3, 1A4 1Y4, 2A1 2Y1, 2A2 2Y2, 2A3 2Y3, 2A4 2Y4; 1G 2G
2200 OUT/IN (2E2)
B RDY (1E7)
CNTR RDY (1E9)
A RDY (1E7)
CP BSY (1E9)
IBS (2E2)
RERR
BD STAT (2G3)

L4 LS534 — D1 D2 D3 D4 D5 D6 D7 D8; O1 O2 O3 O4 O5 O6 O7 O8; OE CP
KENN DIN (2F3)
L22 LS08
IOR (1D2)
L33 LS32
BK9(1E9)
L16 LS32

L2 LS280 — A B C D E F G H I; Σ even, Σ odd
R19 4.7K +5VR
L28 LS74 — 2PR 2CK 2D 2Q 2CLR
TERR (1C6)
BK7 (1D9)
L21 LS11
L1 LS86
KENN RP (2D2)
KENN IN (2D2)
L43 LS10
L.RT ERR (2F2)
L23 LS08

RST (2F3)
RSTT DREQ (2F2)
L23 LS08
L22 LS08
DACK0 (1F8)
DACK1 (1F3)
L22 LS08
CLR DRDY (2F2)
L21 LS11
L16 LS32
EOP (1E2)

L17 LS240 — 1A1 1Y1, 1A2 1Y2, 1A3 1Y3, 1A4 1Y4, 2A1 2Y1, 2A2 2Y2, 2A3 2Y3, 2A4 2Y4; 1G 2G; ±0V
600/450(2D3)
ON LN LED (2E3)
FTL LED (2E3)
PWR ON LED (2E3)
TP LDD LED (2D3)
TL LED PO LED FLT LED OL LED 450/600

NO.	REVISION	BY	DATE
	SEE SHT 5		

WANG PART NO.	DRAWING NO.	DESCRIPTION
WANG	WANG LABORATORIES, INC. LOWELL, MA U.S.A.	

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	8-3-82	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL
MODEL NO. P974 2200 ACTD
SEE ENGRG SPECIFICATIONS No.
FINISH
TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH 125
TITLE 1/4 IN TAPE CONTROLLER MOTHER BOARD
SCALE SHT 3 OF 5
WANG PART NUMBER SEE CHART
SIZE D
DRAWING NUMBER 8260
REV 3

D 8260

DO NOT SCALE

J2 358-1044-M

LED1 370-0826

L0 SPARE

L7 74LS373 — L6 74LS244 — L5 74LS534 — L4 74LS534 — L3 74LS245 — L2 74LS208 — L1 74LS06

L14 9517A-4/DMA 376-9811

L13 74LS240 — L12 74LS11 — L11 74LS244 — L10 74LS244 — L9 74LS240

L20 Z80A/CTC 376-9815

L19 74LS138 — L18 74LS74 — L17 74LS240 — L16 74LS32 — L15 74LS74

L27 Z80A/PIO 376-9811

L26 74LS138 — L25 74LS74 — L24 9602 — L23 74LS00 — L22 74LS00 — L21 74LS11

L33 74LS32 — L32 74LS259 — L31 74LS240 — L30 74LS259 — L29 74LS125 — L28 74LS74

L41 25LS2521 — L40 74LS244 — L39 74LS125 — L38 9602 — L37 74LS00 — L36 74LS74 — L35 74LS240 — L34 SPARE

L48 SPARE — L47 SPARE

L46 74LS240 — L45 74LS240 — L44 74LS00 — L43 74LS10 — SW2 325-1503 — L42 25LS2521

R1 4.7K — R2 4.7K — R3 10K — R4 10K — R5 10K — R6 10K — R7 10K — SW1 325-1504

R8 4.7K — R9 4.7K — R10 10K — R11 10K — R12 2.2K — R13 330 — R14 10K — R15 24K — R16 4.7K — R17 4.7K — R18 4.7K — R19 4.7K — R20 1.2K — R21 10K — R22 4.7K — R23 10K — R24 4.7K — R25 4.7K — R26 4.7K — R27 4.7K — R28 1.2K — R29 4.7K

D1 1N914

C1 .1UF H/F — C2 .1UF H/F — C3 .1UF H/F — C4 .1UF H/F — C5 .1UF H/F — C6 .1UF H/F — C7 .1UF H/F — C8 .1UF H/F — C9 .1UF H/F — C10 .1UF H/F — C11 .1UF H/F — C12 .1UF H/F — C13 .1UF H/F — C14 .1UF H/F — C15 .1UF H/F — C16 .1UF H/F — C17 47uf 15V — C18 .1UF H/F — C19 .1UF H/F — C20 .1UF H/F — C21 .1UF H/F — C22 .1UF H/F — C23 1UF/35V(T) — C24 .1UF H/F — C25 .1UF H/F — C26 .1UF H/F — C27 .1UF H/F — C28 .1UF H/F — C29 .1UF H/F — C30 .1UF H/F — C31 .1UF H/F — C32 .1UF H/F — C33 .1UF H/F — C34 .1UF H/F — C35 .1UF H/F — C36 .22PF — C37 .1UF H/F — C38 .1UF H/F — C39 .1UF H/F — C40 .1UF H/F — C41 .1UF H/F — C42 .1UF H/F — C43 .1UF H/F — C44 .47K — C45 .47PF — C46 .1UF H/F — C47 15UF/28V(T) — C48 15UF/28V/T

J1 — P1 — P2 — P3

8260-R1

*CHANGE PER ECO# 27446

REVISION	BY	DATE	APPROVED BY	DATE
SEE SHT 5	DWN J. Pikela	8-3-82	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

MATERIAL

MODEL NO. P97A
2200 ACTD
SEE ENGRG. SPECIFICATIONS
No.

FINISH

TOL. EX. AS NOTED
.XX ± FRAC. ±
.XXX ± ANG. ± FINISH √

TITLE 1/4 IN TAPE CONTROLLER MOTHER BOARD

SCALE SHT 4 OF 5 | SEE CHART | D | 8260 | 3

WANG PART NUMBER | SIZE | DRAWING NUMBER | REV.

8260

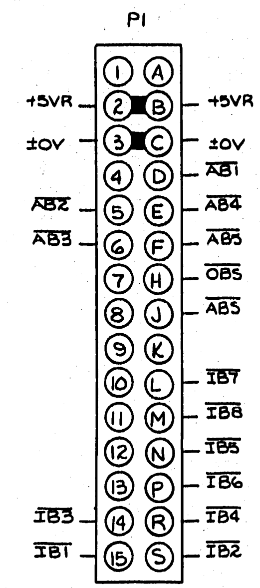
"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.; THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

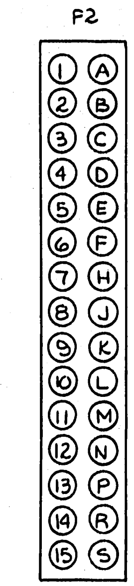
DO NOT SCALE

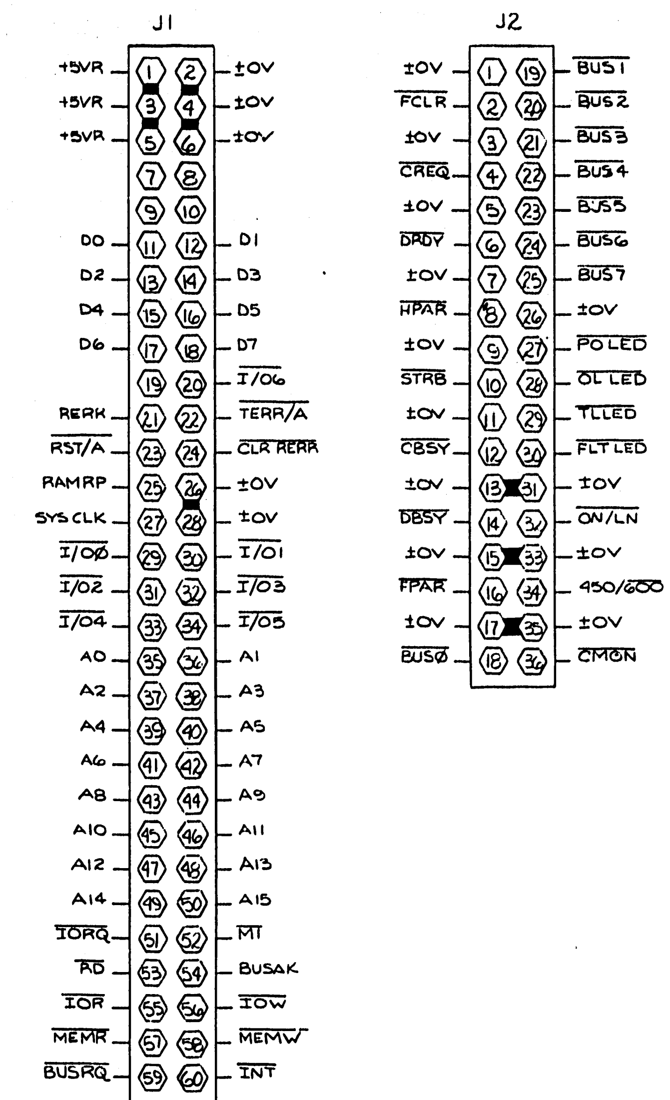
COMPONENT	TYPE	W.L. PT. NO.
R3-7,14,18,21,23	10K 1/4W 5%	330-4011
R2,9,10,16, R1 17,19,22,24, 26,29	4.7K 1/4W 5%	330-3048
R8,25	4.7K SIP	383-0812
R11	100K 1/4W 5%	330-5011
R12	2.2K 1/4W 5%	330-3023
R13	330Ω 1/4W 5%	330-2034
R15	24K 1/4W 5%	330-4025
R20	1.2K 1/4W 5%	330-3013
R27	12K 1/4W 5%	330-4013
R28	47K 1/4W 5%	330-4048
C1-11,13-16,18, 20-22,24,25,27-35,37-44,46	.047uF 50V	300-1966
C12,19,26	.1 UF (H.F.)	300-1930
C17	47UF 15V(T)	300-4020
C23	.1 UF 35V(T)	300-4002
C36	220PF 500V	300-1220
C45	820PF 500V	300-1820
C47,48	15UF 20V(T)	300-4022
D1	IN914A	380-1012
SW1	4 POS	325-1504
SW2	8 POS	325-1503
LED1	RED	370-0026

I.C. LOCATION	TYPE	W.L. PT. NO.
L1	74LS86	376-0231
L2	74LS280	376-0242
L3	74LS245	376-0285
L4,5	74LS534	376-0544
L6,10,11,40	74LS244	376-0288
L7	74LS373	376-0310
L8,34,47,48	SPARES	
L9,13,17,31, 35,45,46	74LS240	376-0297
L12,21	74LS11	376-0225
L14	9517-A	SEE CHART
L15,18,25,28,36	74LS74	376-0155
L16,33	74LS32	376-0211
L19,26	74LS138	376-0294
L20	Z80A-CTC	SEE CHART
L22,23,37,44	74LS08	376-0153
L24,38	9602	376-0104
L27	Z80A-PIO	SEE CHART
L29,39	74LS125	376-0486
L30,32	74LS259	376-0495
L41,42	25LS2521	376-0317
L43	74LS10	376-0209
L14,27	40 PIN SKT	376-9011
L20	28 PIN SKT	376-9015

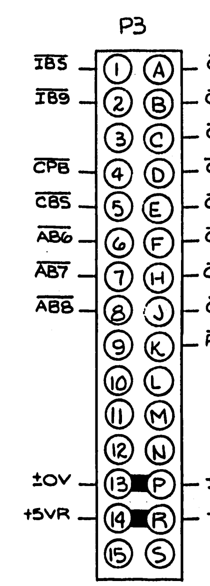
MNEMONICS	COORD
A0-A15	2G7
AB1-AB8	2G11
ABS	2D11
BUSØ-BUS7	3G1
BUSAK	1G5
BUSRQ	1D1
CBS	1C11
CBSY	3F11
CLR RERR	2F1
CMON	3F11
CPB	1D11
CREQ	3E1
DØ-D7	1F1
DRDY	3E1
FCLR	3E1
FPAR	3F11
FLT LED	3A5
HPAR	3E1
I/OØ	1G5
I/O1	2B11
I/O2	1G3
I/O3-I/O6	2G8
IB1-IB8	1G1
IB9	1A9
IBS	1A9
INT	2A6
IOR	1D1
IORQ	2B11
IOW	1D1
MEMR	1E1
MEMW	1D1
M1	1G7
OB1-OB8	1F11
OBS	1C11
OBSV	3F11
OL LED	3A5
ON LN	3E11
PO LED	3A6
RAM RP	2E1
R/B	1A9
RD	2B11
RERR	3C11
RST/A	2A5

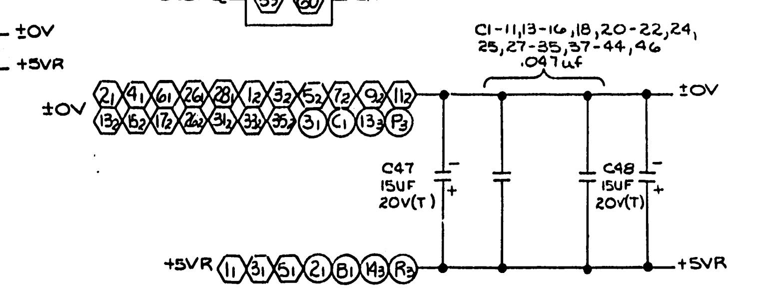






MNEMONICS	COORD
STRB	3F11
SYS CLK	1G6
TERR/A	1A5
TL LED	3A6
450/600	3A5





NOTE:
1. ALL RESISTORS ARE 1/4 W 5% UNLESS OTHERWISE SPECIFIED.

210 = 209 + 377 OR 378				
210	209	L14	L20	L27
8260A	8260	377-0435	377-0371	377-0373

TYPE	I.C. LOCATION	SPARES
74LS08	L23	1
74LS32	L16	1
74LS74	L28	1
74LS86	L1	2
9602	L24	1

E REV 0

N

REVISION	BY	DATE
0 ORIGINATED PER DWR# E6088 APP'D: [illegible] 8-6-82	JEF	8-3-82
1 REVISED PER ECO# 25196 APP'D [illegible]	[illegible]	11-22-82
2 REVISED PER ECO# 26521D APP'D [illegible]	A.B.	1-12-83
3 REVISED PER ECO# 27446 APP'D [illegible]	[illegible]	3/1/83

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG — WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	[illegible]	8-3-82	E ENGR K. BUTLER	8-6-82
CHK	[illegible]	8-6-82	M ENGR	
			MFG ENGR	

MATERIAL — MODEL NO P97A 2200 ACTD — SEE ENGRG SPECIFICATIONS No.

TITLE: 1/4 IN TAPE CONTROLLER MOTHER BOARD

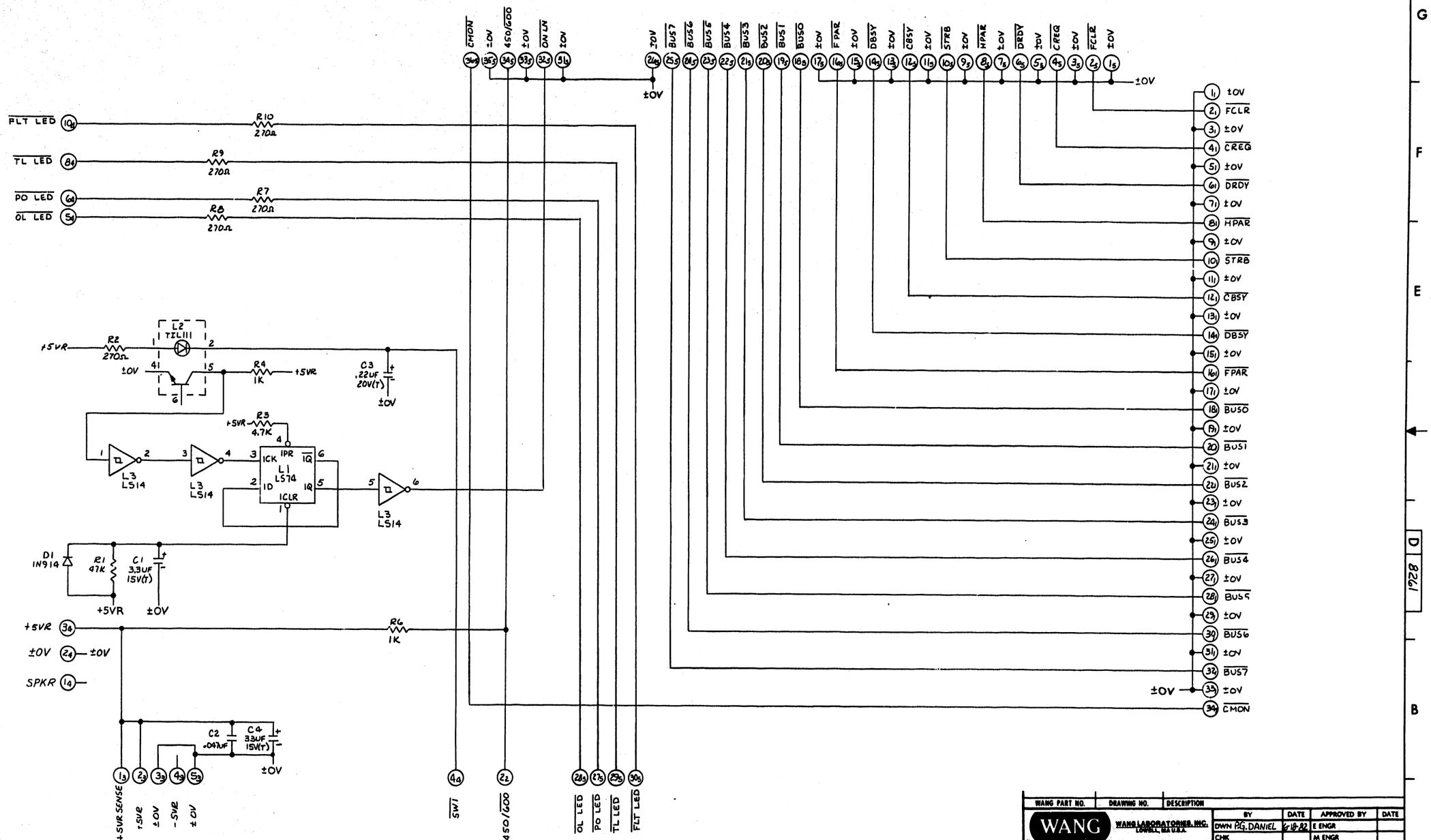
FINISH — TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH √

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	8260	3

SCALE — SHT 5 OF 5

D 8260

DO NOT SCALE



REVISION	DATE	BY
SEE SHEET 2		

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN P.G. DANIEL	6-18-82		E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO P197A 2200 ALTD

SEE ENGRG SPECIFICATIONS No.

TITLE TAPE INTERFACE

FINISH

TOL EX AS NOTED
.XX ± .010 FRAC ± 1/64
.XXX ± .005 ANG ± 1°30' FINISH

SCALE	SHT 1 OF 2	210-8261	D	8261	4
		WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

D 8261

DO NOT SCALE

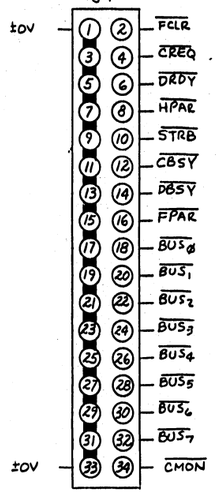
IC LOCATION	TYPE	WL. PART NO.
L1	74LS74	376-0155
L2	TIL111	375-2109
L3	74LS14	376-0322

IC TYPE	LOCATION	SPARES
74LS74	L1	1
74LS14	L3	3

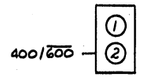
COMPONENT	TYPE	W.L.PART NO.
R1	47K 1/4W 5%	330-4048
R2,7,8,9,10	270Ω 1/4W 5%	330-2028
R3	4.7K 1/4W 5%	330-3048
R4,6	1K 1/4W 5%	330-3011
C1	3.3UF 15V(T)	300-4016
C2	.047UF 50V	300-1966
C3	.22 UF 20V(T)	300-4060
C4	33UF 15V(T)	300-4019
D1	1N914A	380-1012
J1	CONN.,34 PIN	350-0429
J2	CONN.,2 PIN	350-0499
J3	CONN.,5 PIN	350-0234
J4	CONN.,10 PIN	350-0460
J5	CONN.,36 PIN	350-0085-M

MNEMONICS	COORD.
$\overline{BUS0}$	1D2, 1G5
$\overline{BUS1}$	1D2, 1G5
$\overline{BUS2}$	1D2, 1G5
$\overline{BUS3}$	1C2, 1G5
$\overline{BUS4}$	1C2, 1G6
$\overline{BUS5}$	1C2, 1G6
$\overline{BUS6}$	1C2, 1G6
$\overline{BUS7}$	1B2, 1G6
$\overline{CBSY}$	1E2, 1G4
$\overline{CMON}$	1B2, 1G7
$\overline{CREQ}$	1F2, 1G3
$\overline{DBSY}$	1E2, 1G4
$\overline{DRDY}$	1F2, 1G3
$\overline{FCLR}$	1F2, 1G3
$\overline{FLT\ LED}$	1F10, 1A6
$\overline{FPAR}$	1D2, 1G5
$\overline{HPAR}$	1E2, 1G4
$\overline{OLLED}$	1E10, 1A7
$\overline{ONLN}$	1G7
$\overline{POLED}$	1F10, 1A6
SPKR	1B10
$\overline{STRB}$	1G4, 1E2
$\overline{SWI}$	1A7
$\overline{TLLED}$	1F10, 1A6
450/600	1A7, 1G7

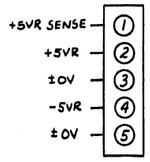
J1



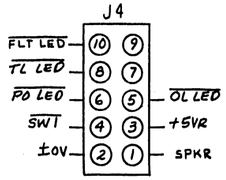
J2



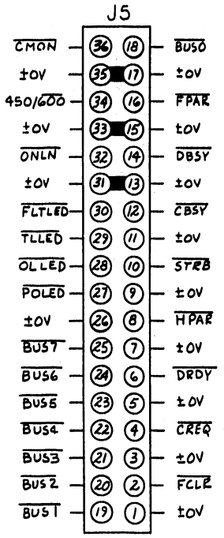
J3

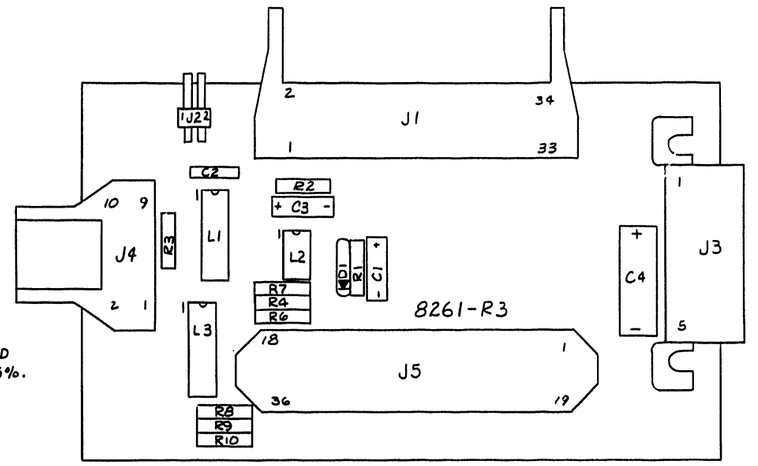


J4



J5





NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4W, 5%.

E-REV
0

NO.	REVISION	D ENGR	PGD	EMP	KTH	FSS	EMW
0	ORIGINATED PER DWG# 1685 APP'D: 6-18-82	6/18	6-18-82	10/21/82	11-27-82	12-15-82	6-30-83
1	REVISED PER ECO# 24567 APP'D: MAY-10-1983	1/0					
2	REVISED PER ECO# 25703 APP'D: MAY-10-83	2/0					
3	REVISED PER ECO# 27867 APP'D: 6-30-83	3/0					
4	REVISED PER ECO# 27867 APP'D: 6-30-83	4/0					

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

BY	DATE	APPROVED BY	DATE
DWN RG. DANIEL	6-18-82	E ENGR K. BUTLER	6-18-82
CHK	6/18/82	M ENGR	
		MFG ENGR	

MATERIAL

MODEL NO P197A
2200 ACTD
SEE ENGRG SPECIFICATIONS
No.

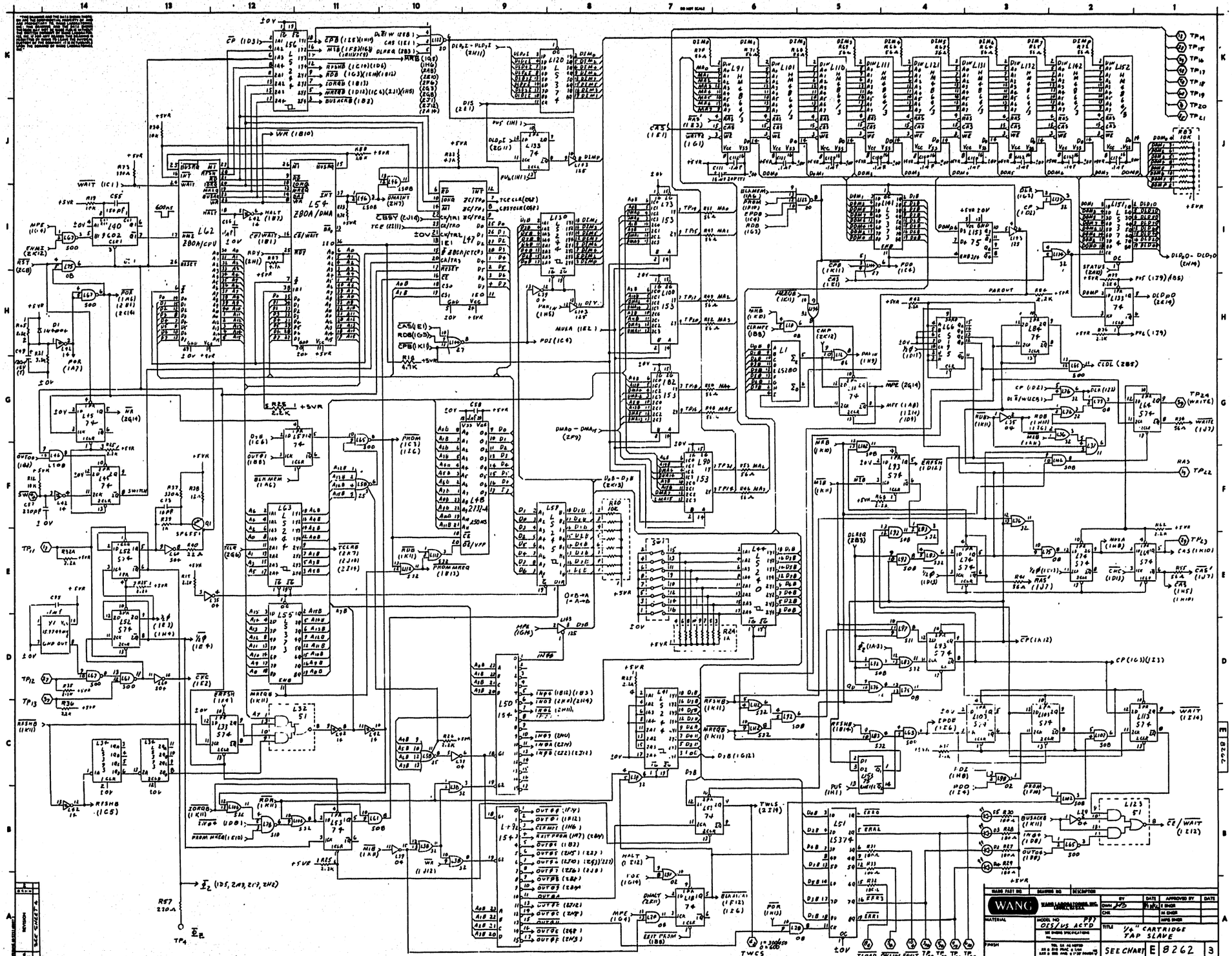
FINISH

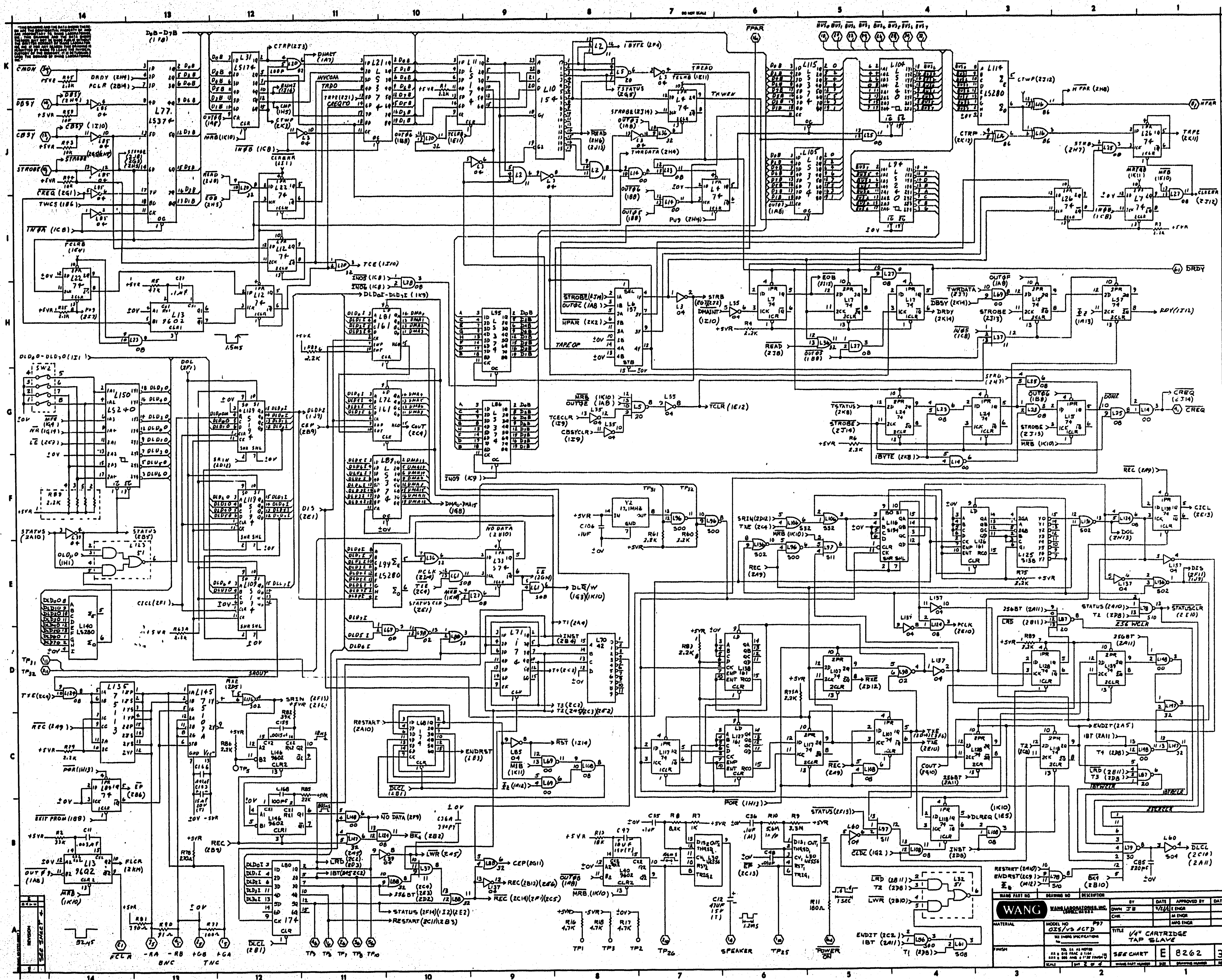
TOL EX AS NOTED
XX ± 010 FRAC ± 1/64
XXX ± 005 ANG ± 1°30' FINISH √

TITLE: TAPE INTERFACE

SCALE	SHT 2 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
		210-8261	D	8261	4

D 8261

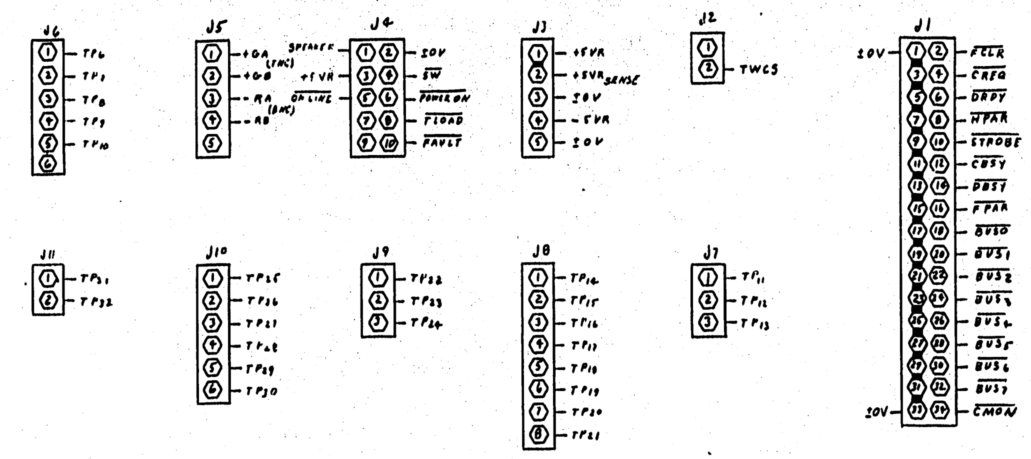

Z80A/CPU
Z80A/DMA
Z80A/PIO
Z80A/CTC
WANG
SEE CHART
E 8262
3

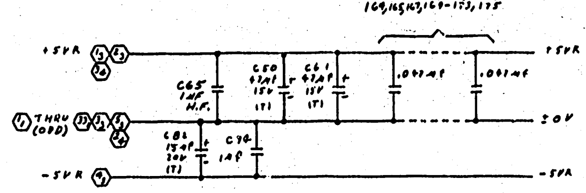


WANG LABORATORIES, INC. LOWELL, MASS.			
MODEL NO P97 OIS/VS ACTD	DWN JB	4/22/	
TITLE	1/4" CARTRIDGE TAP SLAVE		
SEE CHART	E	8262	3
SHT 2 OF 4			

WANG	BY	DATE	APPROVED BY	DATE
	DRN K.FFF.	11/84	E ENGR	
	CHK		M ENGR	
MATERIAL	MODEL NO. 99 OFS/VS ACTO		MFG ENGR	
FINISH		TITLE 1/4" CARTRIDGE TAP SLAVE		
		SUB CHART	E 8262	3
		NEXT PART NUMBER	DO	DRAWING NUMBER

REVISION E ENG. RELEASE





210 = 209 + 377 OR .370							
210	209		L47	L48	L54	L62	L94,101,110,111,121, 131,132,142,152
8262-A	8262		377-0371	378-8012	377-0421	377-0360	377-0415

I.C. LOCATION	TYPE	W.L. PART NO
L1,99,114,140	74LS280	376-0242
L2,37	7411	376-0194
L3,35,39,85,137	7404	376-0010
L4,7,12,15,17,18,22,24,26,45, 53,83,89,107,117,118,120, 133,139	7474	376-0006
L5,87,122	7420	376-0004
L6	74157	376-0082
L8,9,19,29,154		SPARE
L10,49,50	74164	376-0090
L11,31	74LS174	376-0159
L13,40,146	9602	376-0104
L14,69,148	7400	376-0002
L16	7486	376-0036
L20,36,38,88,134,76,147	7432	376-0093
L21,51,77,86,89,95,105,115, 120,151	74LS374	376-0286
L23,25,27,28, 75,108,124	7408	376-0081
L30	NE556	376-0341
L32,123	7451	376-0012
L33,52,64,74,93,103,113	74574	376-0202
L34	74LS393	376-0307
L41,56,63,130	74LS244	376-0288
L42	7414	376-0139
L44,74,104,150	74LS240	376-0297
L46	74LS08	376-0153
L47	Z80A/CTC	SEE CHART
L48	2732-A	SEE CHART
L54	Z80A/DMA	SEE CHART
L55,141	74LS373	376-0310
L58	7425	376-0092
L57	74LS245	376-0285
L60	74504	376-0197
L62	Z80A/CPU	SEE CHART
L65,67,96	74S00	376-0228
L66	74S135	376-0427
L68,71,80	74174	376-0018
L70	7442	376-0008
L72,81,126,127,138	74161	376-0094
L73,82,90,100	74153	376-0048
L78	74S10	376-0238
L79	7430	376-0031
L83,106,112	74532	376-0205
L91,101,110,111,121,131,132, 142,152	4864-3	SEE CHART
L92,102,61	745AB	376-02C0
L97	7451	376-0277
L98	7432	376-0016
L109,116,119,129	74194	376-0221
L125	74S138	376-0298
L135	75113	376-0256
L136	74S02	376-0199
L143	74125	376-0324
L144	7427	376-0125
L145	75107A	376-0146
L153	7475	376-0013
L48	24 PIN SKT	376-1003
L47	28 PIN SKT	376-9015
L54,62	40 PIN SKT	376-9011
L91,101,110,111,121,131,132, 142,152	16 PIN SKT	376-9002

I.C. TYPE	LOC	SPARE
74S04	L60	2
74LS08	L46	1
7427	L144	1
7432	L134	1
74574	L113	1
7432	L147	1
7400	L148	1

COMPONENT	TYPE	W.L. PART NO.
R1,3,4,6,15,26,35,36,42, 45, 58,60,61-63,74-76,79, 84,86,63A,75A,33A	2.2K 1/4W 5%	330-3023
R2	33K 1/4W 5%	330-4034
R5	47K 1/4W 5%	330-4048
R7,39	1K 1/4W 5%	330-3011
R8	6.2K 1/4W 5%	330-3083
R9	3.3M 1/4W 5%	330-6034
R10	5.6M 1/4W 10%	330-6056
R11,27-33	180Ω 1/4W 5%	330-2019
R12,19,34,43,44,59	10K 1/4W 5%	330-4011
R13	18K 1/4W 5%	330-4019
R14,16,17,18,22,23,87	4.7K 1/4W 5%	330-3048
R24	1K (9) SIP	333-0837
R25,89	2.2K (7) SIP	333-0806
R37	330Ω 1/4W 5%	330-2034
R38	12Ω 1/4W 5%	330-1013
R44,46-55,69-72	56Ω 1/4W 5%	330-1057
R57	220Ω 1/4W 5%	330-2023
R73,81	390Ω 1/4W 5%	330-2040
R77	110Ω 1/4W 5%	330-2011
R78	270Ω 1/4W 5%	330-2028
R80	91Ω 1/4W 5%	330-1092
R82	39K 1/4W 5%	330-4040
R83,20	10K (9) SIP	333-0809
R88	1.8K 1/4W 5%	330-3019
R21	3.3K 1/4W 5%	330-3034
R40	22Ω 1/4W 5%	330-1023
R85	22Ω 1/4W 5%	330-4023
C1-10,13-22,24-26,28-34,37-46, 51-54,59,60,62-64,66-72, 79-81,83, 96-105, 107-110,113-120,123-128, 131-139,141-149,151,153, 154,156-161,164-167, 169-173,175,84,86-93	.047MF 50V	300-1966
C11	.003MF	300-1905
C12, 50,61	47MF 15V (T)	300-4020
C27,35	.01MF 12V	300-1901
C36	.1MF 50V MYLAR	300-2213
C47	10MF 15V (T)	300-4018
C48	.01MF 25V	300-1903
C55	150PF 500V	300-1150
C56,58, 95,106,112,121, 129,130,140,150,162,163, 174	.1MF 5V	300-1930
C57,85	220PF 500V	300-1220
C73	10PF 500V	300-1010
C82,111,153	15MF 20V (T)	300-4022
C155	.0015MF	300-1907
C168	100PF 500V	300-1100
C36A	390PF 500V	300-1390
C65,94	1MF	300-1931
Y1	15.9744 MHZ	321-0054
Y2	17.1 MHZ	321-1006
D1	1N4004	300-4000
Q1	SPS6551	375-1050
D2-5	LED RED	370-0026
C49	120μf 15V (T)	300-4031
J7,9	3POS HEADER	654-0104
J1	34 PIN CONN	350-0439
J2	2POS HEADER	350-0499
J3	5PIN CONN	350-0234
J4	10 PIN CONN	350-0460
J5	5POS HEADER	350-0249
J8	8POS HEADER	350-0244
J6,10	6POS HEADER	654-0106
J11	2POS HEADER	350-0203
TP1-5	TERM	654-3022
SW1	8 POS SLIDE SPST	325-1503
SW2	4 POS SLIDE SPST	325-1504
J3	SCREW 6-32X 3/8	650-3120
J3	WASHER FLAT	653-2500
J3	WASHER	653-3002
J3	NUT 6-32	652-3000

MNEMONICS	COORD
BUS0-BUS7	2 A 5
CBSY	2 J 14
CMON	2 K 14
CREQ	2 G 1
DBSY	2 K 14
DRDY	2 J 1
FAULT	1 A 4
FCLR	2 K 14
FPAR	2 K 6
+GA	2 A 12
+GB	2 A 13
HPAR	2 J 1
ON LINE	1 A 4
POWER ON	2 A 5
-RA	2 A 13
-RB	2 A 13
SPEAKER	2 A 6
STROBE	2 J 14
SW	1 F 14
FLOAD	1 A 5
TWCS	1 A 6
TP6-TP10	2 A 11
TP11	1 E 14
TP12	1 D 14
TP13	1 C 14
TP14-TP21	1 K 1
TP22	1 F 1
TP23	1 E 1
TP24	1 G 1
TP25	2 A 6
TP26	2 A 7
TP27-TP30	1 A 4
TP31,32	2 D 12

E-REV
1

NOTE:
ALL RESISTORS ARE 1/4W 5%
UNLESS OTHERWISE SPECIFIED

WANG LABORATORIES, INC.
LOWELL, MA U.S.A.

MODEL NO: 0I5/VS ACTD

TITLE: 1/4" CARTRIDGE TAP SLAVE

WANG PART NUMBER: SEE CHART | SIZE: E | DRAWING NUMBER: 8262 | REV: 3

DO NOT SCALE

MOUNTED EXTERNALLY

3A LINE FILTER

F1 2.0A SB. -115V
F1A 1.0A SB. 230V

HOT
GND
NEUT.

F1 = 360-1020-SB
F1A = 360-1011-SB

SW2

SP3 SP2

SW1

RV2 130V

RV1 130V

115V 230V

FAN

MOUNTED EXTERNALLY

BRN
YEL
YEL/BLK
YEL
BRN/YEL
BLK
BLU
BLU/BLK
BLK/YEL

26.0VAC
26.0VAC
7.6VAC
BLU 7.6VAC

D3 A15A
D4 A15A
D2A PAC10

SP1

* 31.5V
* 8.1V
±0V

R2 2.2K 1W 10%
C4 6800μF 50V (E)
C1 .047μF 100V
C2 10μF 50V (E)

D2 IN4004
VR1 LM350T ADJ
D1 IN4004

* 23.0V
* 22.75V

R3 121Ω 1/8W 1%
R7 330Ω 1W 10%
R20 500Ω
R4 15.1K 1/8W 1%

C9 10μF 50V (E)
D10 15V 5% IN4744

LED1
R1 1.8K 1/2W 10%
C3 10μF 50V (E)
TP1 +23V

+23VR
+23V RETURN
GND

R5 270Ω 1/2W 10%
40K.uF 12V

D5 IN4004
VR2 IN OUT 79M05 COMM

* -9.4V
C6 470μF 35V (E)

D6 IN4004
D7 IN4004
D9 IN4004
D8 IN4004

* 8.6V

R18 220Ω

R6 220Ω
LED2
C5 10μF 50V (E)

-5VR OUT

C7 2200μF 16V (E)

Q2 TIP29
Q1 2N5301
*6.9V
*6.2V
*5.2V

R8 1.0K
R13 100Ω
R15 .01Ω 3W 3%
R14 681Ω 1/8W 1%
R17 220Ω
LED3
C11 10μF 50V (E)

+5VR OUT

+5V SENSE

R11 120K
R12 120K
R19 39.2K 1/8W 1%
D11 IN4004
R16 500Ω
R10 681Ω 1/8W 1% *7.15V
R9 2.21K 1/8W 1%
C10 10μF 50V (E)
C8 .01μF 100V

U1 LM311
L1 LM723
Vcc+ Vc Vout VREF Vz Vcc- CL NII CS FC

VR1 LM350T — ADJ OUT IN
VR2 79M05 — COMM IN OUT
Q2 TIP-29 — BASE COLLECTOR EMITTER

FRONT VIEWS

*VOLTAGES SHOWN REPRESENT AN INPUT VOLTAGE OF 115V.A.C. AT 60 Hz, AND WITH THE FOLLOWING LOADS:

+5VR – 8 AMP
+23VR – .7 AMP
-5VR – .025 AMP

NO.	REVISION	DATE	BY
	SEE SHEET 2.		

DRAWING 40-5253-48897-3

	BY	DATE	APPROVED BY	DATE
DWN	D. Smith	6-24-82	E ENGR	
CHK			M ENGR	
			MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

MATERIAL —

MODEL NO 7097 ACTD

SEE ENGRG SPECIFICATIONS No.

FINISH —

TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH √

TITLE POWER SUPPLY

SCALE — SHT 1 OF 2

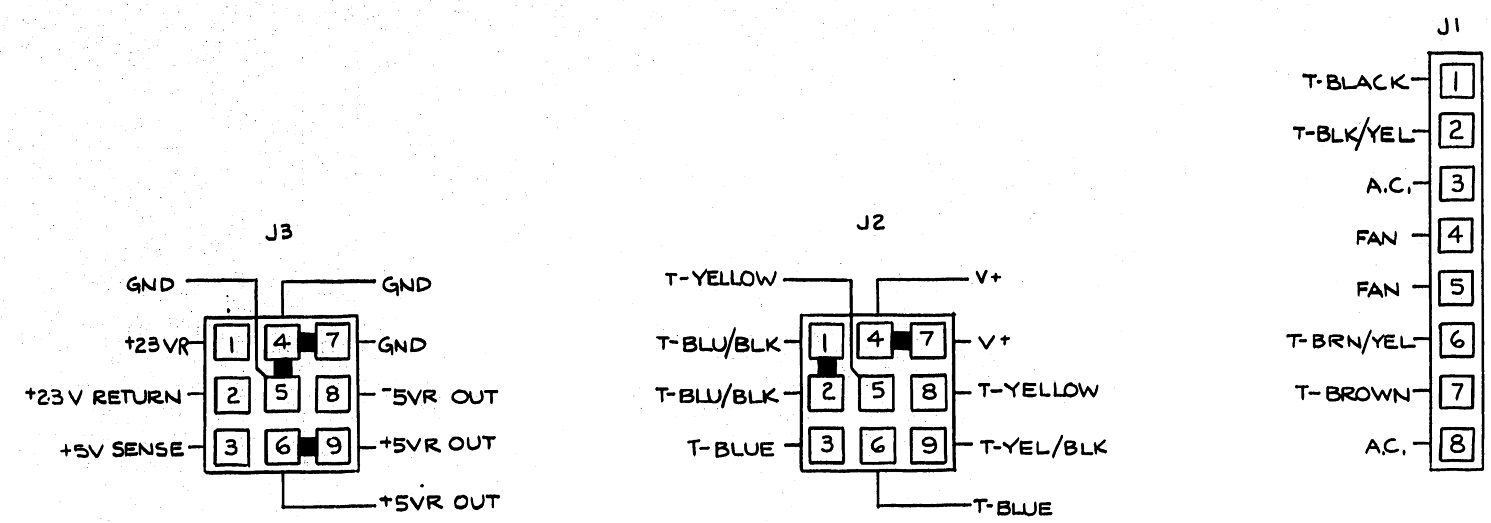
210-7770 WANG PART NUMBER | D SIZE | 7770 DRAWING NUMBER | 4 REV

7770

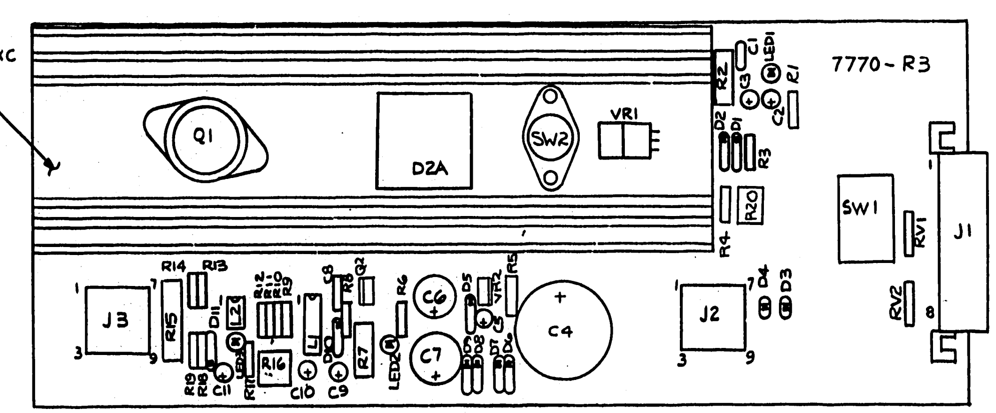
DO NOT SCALE

I.C. LOCATION	TYPE	W.L. PART NO.
L1	LM723	376-0978
L2	LM311	376-0974

COMPONENT	TYPE	W.L. PART NO.
R1	1.8K, 1/2W, 10%	331-3018
R2	2.2K, 1W, 10%	332-3022
R3	121Ω, 1/8W, 1%	333-0101
R9	2.21K, 1/8W, 1%	333-0183
R7	330Ω, 1W, 10%	332-2033
R6,17,18	220Ω, 1/4W, 5%	330-2023
R8	1.0 K, 1/4W, 5%	330-3011
R10,14	681Ω, 1/8W, 1%	333-0058
R11,12	120K, 1/4W, 5%	330-5013
R13	100Ω, 1/4W, 5%	330-2011
R15	.01Ω, 3W, 3%	334-0041
R16,20	500Ω, VAR1	336-1025
R19	39.2K, 1/8W, 1%	333-0151
R4	1.91K 1/8W 1%	333-0172
R5	270Ω 1/2W 10%	331-2027
C1	.047μF, 100V	300-1919
C2,3,5,9,10,11	10μF, 50V, (E)	300-3321
C4	6800μF, 50V, (E)	300-3137
C7	2200μF, 16V, (E)	300-3141
C8	.01μF 100V	300-1934
C6	47OUF 35V (E)	300-3322
D1,2,5-9,11	1N4004	380-4000
D2A	PAC10	380-4005
D3,4	A15A	380-3008
D10	1N4744, 15V, 5%	380-2132
Q1	2N5301	375-1048
Q2	TIP-29	375-1063
VR1	LM 350 T	374-0044
VR2	79M05	374-0012
RV1,2	130V	380-5000
LED1,2,3	RED	370-0026
SW1	DTDP, SLIDE	325-0064
SW2	THERMAL SWITCH	325-2480
J1	8 POS., HEADER	350-0235
J2,3	9 POS. HEADER	350-0219



HEATSINK 47A-0830-XC (REFERENCE)



NOTE:
ALL RESISTORS ARE 1/4W, 5% UNLESS OTHERWISE SPECIFIED.

E-REV Ø

NO.	REVISION	DATE	BY
0/0	ORIGINATED PER DWR # E 1664 APPD: D.J.C. 7-1-82	6-25-82	D.S.S.
-/0	REVISED PER ECO # 24111, 24365 APP'D: RLL 9/24/82	9-22-82	JEP
2/0	REVISED PER ECO# 25507 APP'D: RLL 1-4-83	1/3/83	KMP
3/0	REVISED PER ECO#26754 APP'D: DJC 3-22-83	3-9-83	JDE
4/0	REVISED PER ECO No. 27513 APPD.	4/4/83	G.S.

BRUNING 40-5253 483097-3

WANG LABORATORIES, INC. LOWELL, MA U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN D. Smith	6-25-82	E ENGR D. PARADIS	7-1-82
	CHK D. J. CORRIN	7-1-82	M ENGR	
			MFG ENGR	

MATERIAL —

MODEL NO P097 ACTD

SEE ENGRG SPECIFICATIONS No.

FINISH —

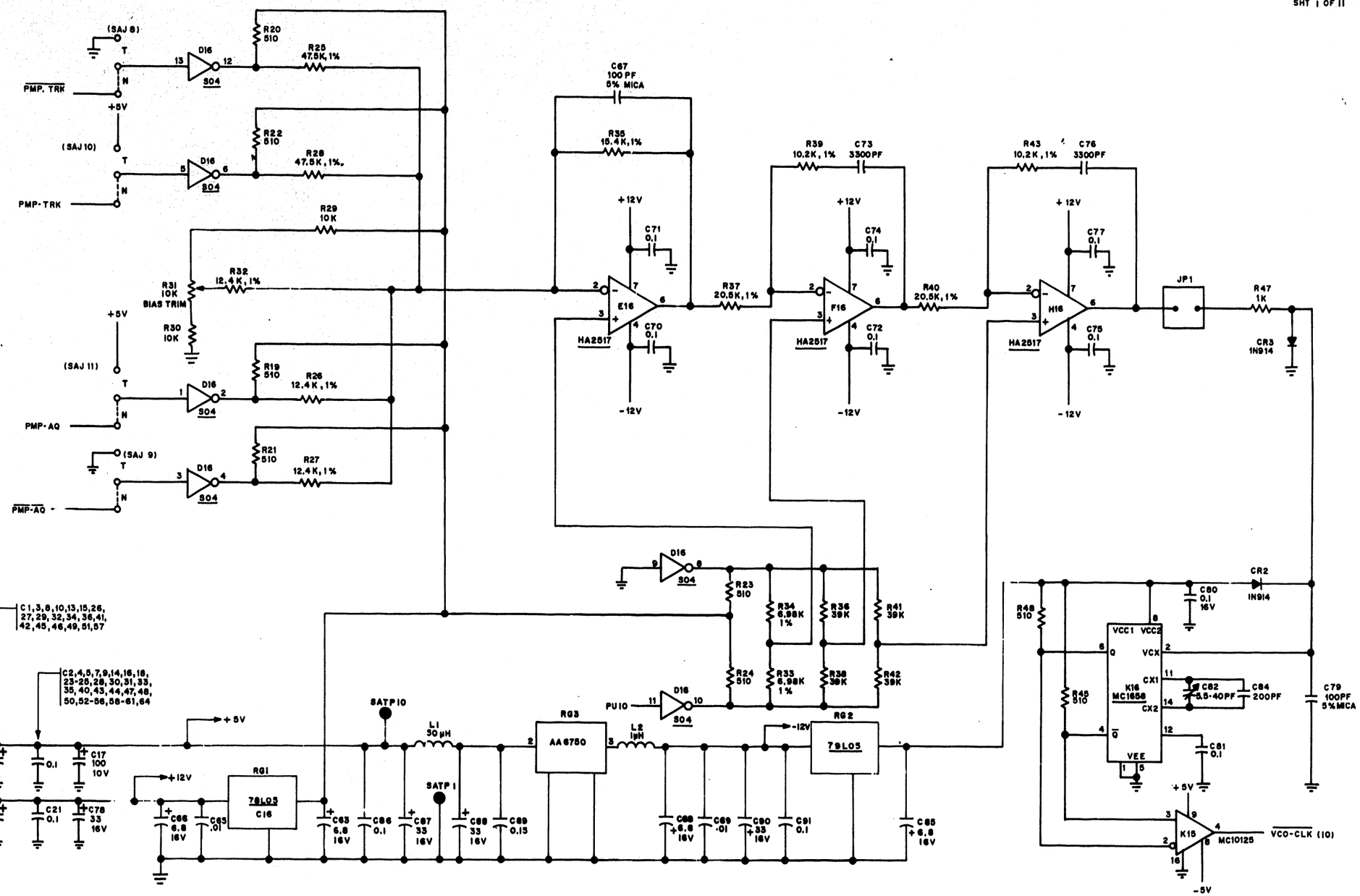
TOL EX AS NOTED .XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG ± 1°30' FINISH 125

SCALE — SHT 2 OF 2

TITLE POWER SUPPLY

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7770	D	7770	4

D 7770



650 Formatter
Type 5563
Schematic Diagram

* S1 (SWITCH) USED ON -001 ASSY
XS11 SOCKET) USED ON -100 ASSY

+5V

T1 10K

S1

A1

SYSTEM CLR (8)

B1 LS374

CNTRL BUS 0
CNTRL BUS 1
CNTRL BUS 2
CNTRL BUS 3
CNTRL BUS 4
CNTRL BUS 5
CNTRL BUS 6
CNTRL BUS 7
(3,4,5,7)

A12 LS04

RD ID EN (8039-3)

+5V

T2 10K

J20
HOST HEADER

H. FMTR. CLR
H. CMD. REQ
H. DRDY
H. HPAR
H. STRB
H. CBSY
H DBSY
H FPAR
H. BUS 0
H BUS 1
H BUS 2
H BUS 3
H. BUS 4
H. BUS 5
H. BUS 6
H. BUS 7
H. CMON

A10 LS245

FRMT CLR (8)
CMD. REQ (3)
DRDY (5)

A12 LS04

CMD BSY (3)

B9 LS27

CMC STRB (3)
W STRB (5)
R STRB (7)

B9 LS27

W DBSY (5)
R DBSY (7)

A7 LS280

B10 S86

FMTR · PAR (3,5)

DATA · BUS · IN (3)

A8 LS245

DATA BUS 0
DATA BUS 1
DATA BUS 2
DATA BUS 3
DATA BUS 4
DATA BUS 5
DATA BUS 6
DATA BUS 7
(3,6)

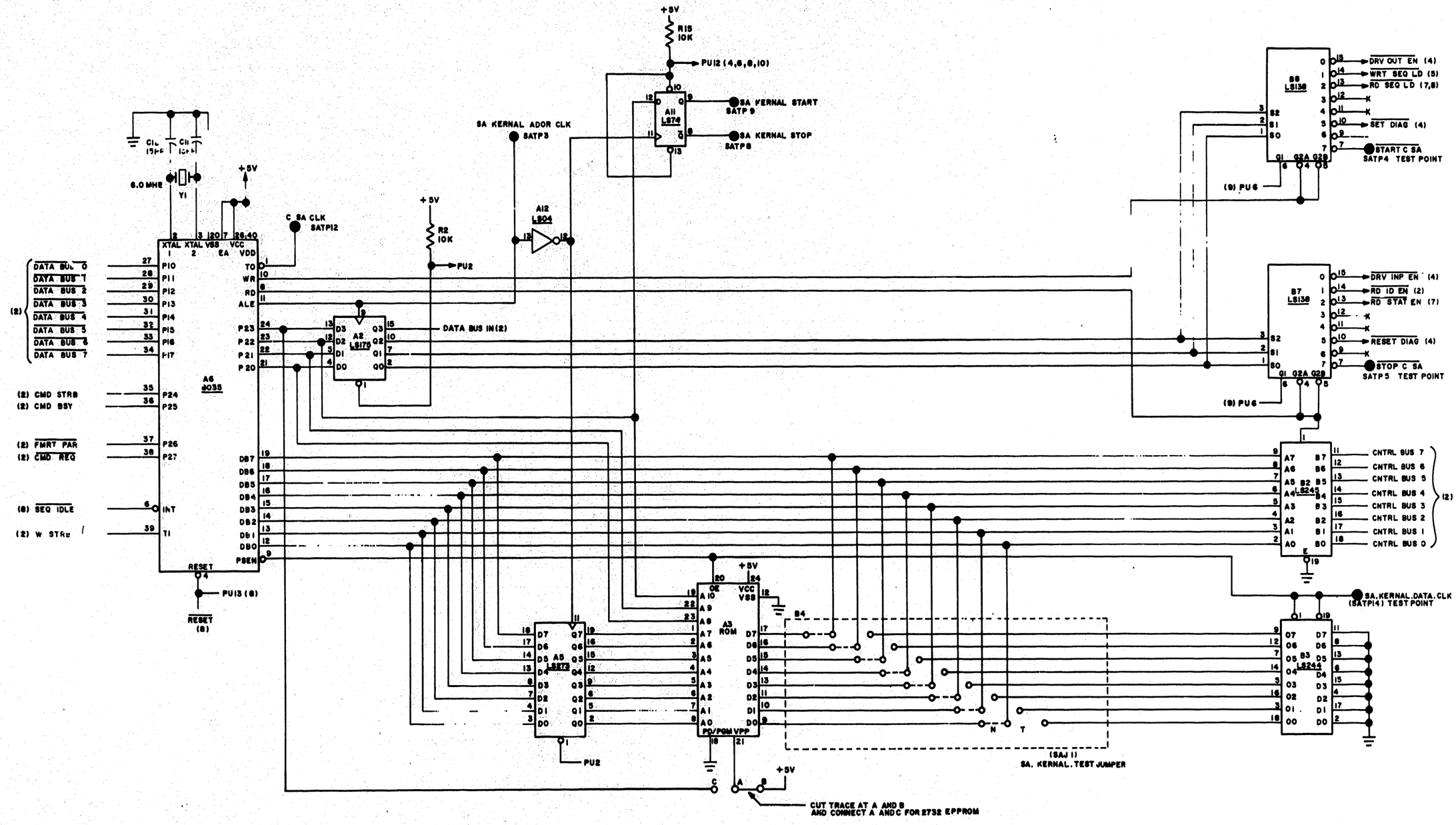
A9 LS244

R DBSY (7)

RD 0
RD 1
RD 2
RD 3
RD 4
RD 5
RD 6
RD 7
(8)

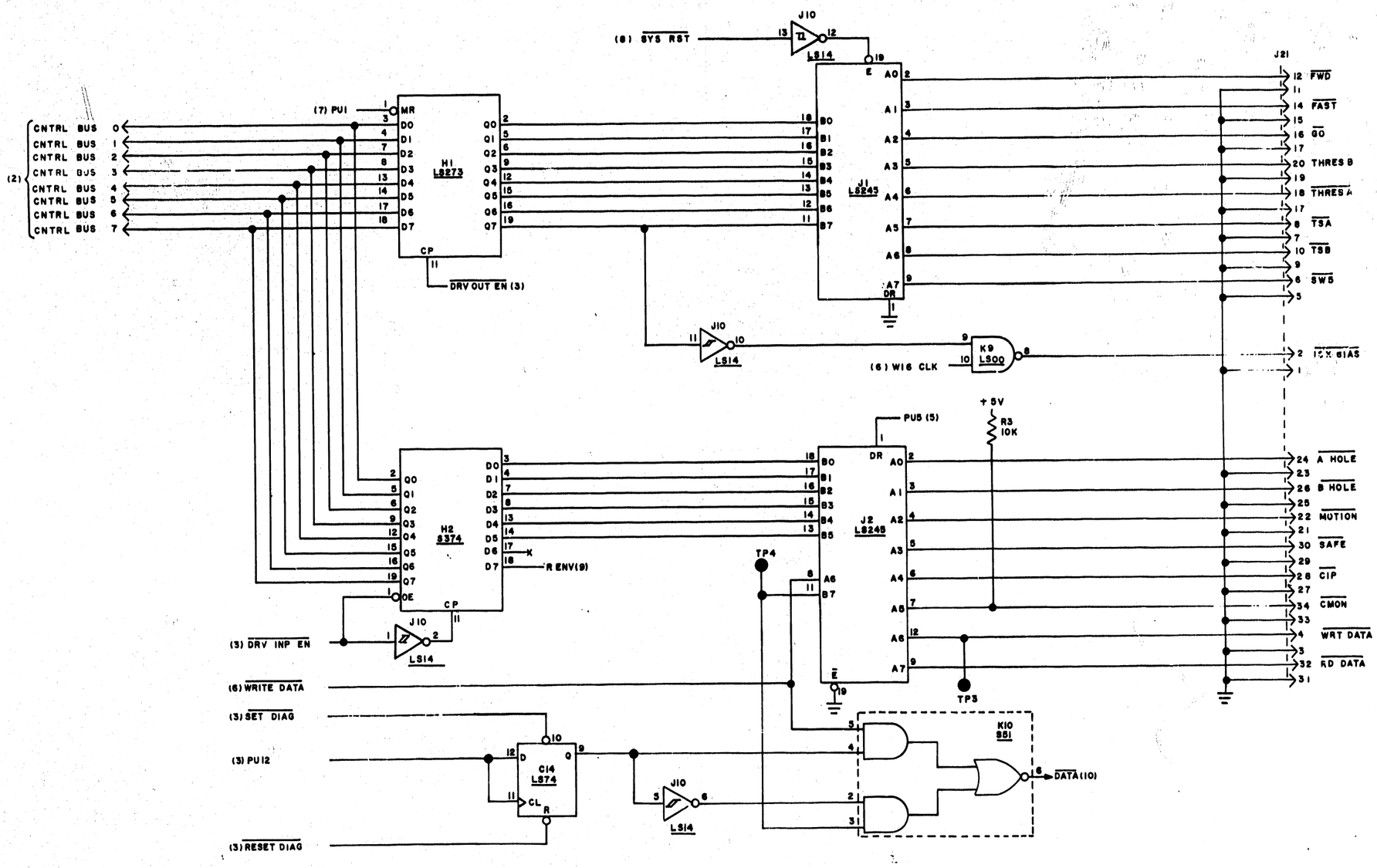
SHEET 2 of 11

650 Formatter
Type 5563
Schematic Diagram



SHEET 3 OF 11

650 Formatter
Type 5563
Schematic Diagram

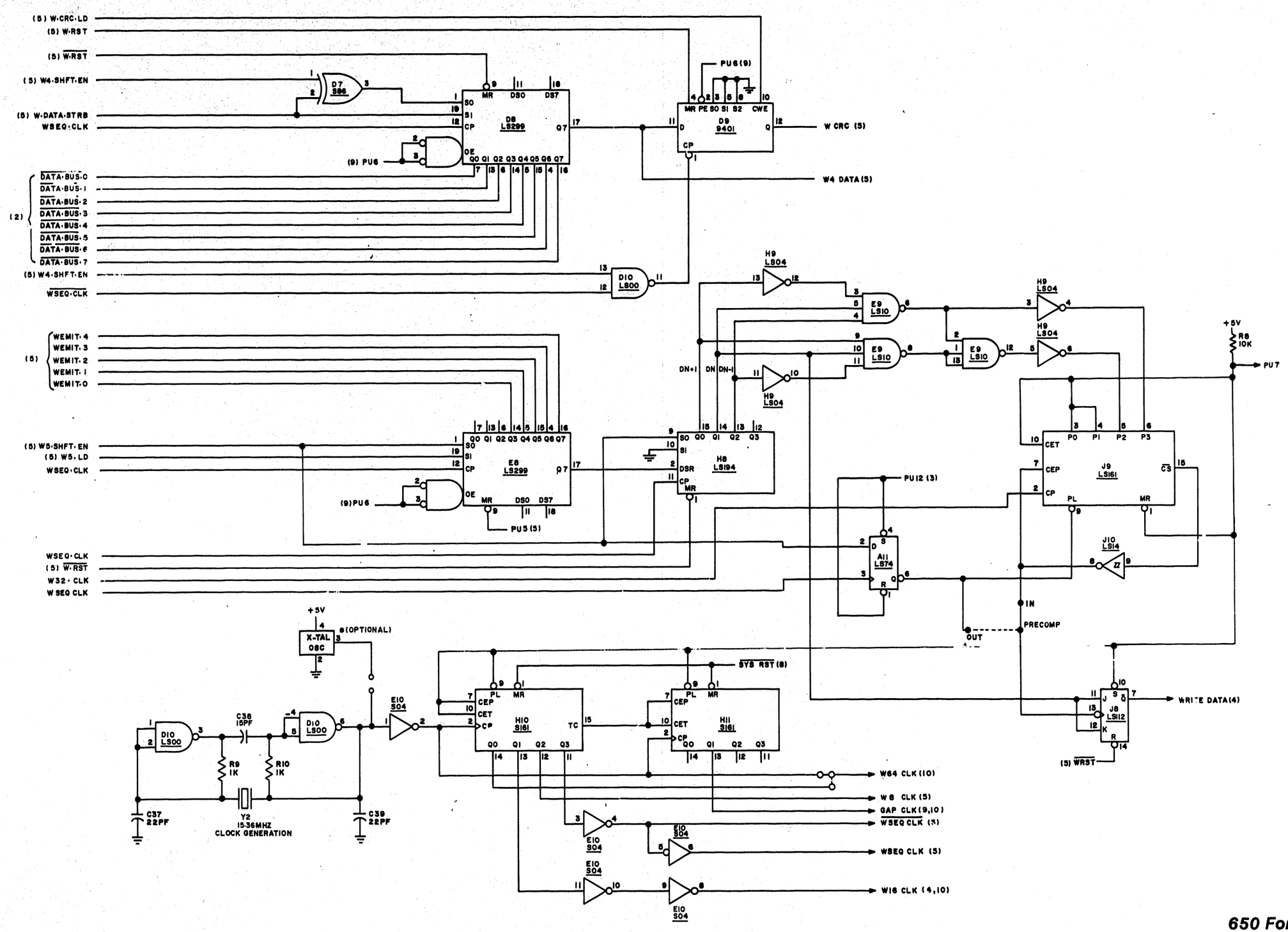


650 Formatter
Type 5563
Schematic Diagram

SHT. 4 OF 11

(8) SYST·RST
(3) WRT·SEQ·LD
(6) WSEQ·CLK
TEST POINT (SATP15)
(6) W8·CLK
H7 LS74
C7 LS74
K9 LS00
(SAJ5)
(3) WRT SEQ LD
+5V
R6 10K
PU5(4,6)
(9) PU6
(2)
CNTRL·BUS·0
CNTRL·BUS·1
CNTRL·BUS·2
CNTRL·BUS·3
CNTRL·BUS·4
CNTRL·BUS·5
CNTRL·BUS·6
CNTRL·BUS·7
E1 S 374
OE CP D0 D1 D2 D3 D4 D5 D6 D7 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
R 52 4.7K
W·SA·STOP TEST POINT (SATP11)
W·SA·START TEST POINT (SATP16)
WAC·2
WAC·1
WAC·0
R5
E6 8X02
CL AC2 AC1 AC0 T EN VCC A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
WA 8
WA 7
WA 6
WA 5
WA 4
WA 3
WA 2
WA 1
WA 0
WEMIT 0
WEMIT 1
WEMIT 2
WEMIT 3
WEMIT 4
WEMIT 5
WEMIT 6
WEMIT 7
(6)
E2 146-0101-001
E3 146-0102-001
E4 146-0103-002
W-CRC-LD
W5-LD
W5-SHIFT-EN
W4-SHIFT-EN
WAC-2
WAC-1
WAC-0
WCNTR-LD
WEMIT·7
WEMIT·6
WEMIT·5
WEMIT·4
WEMIT·3
WEMIT·2
WEMIT·1
WEMIT·0
WTSEL·0
WTSEL·1
WTSEL·2
WTSEL·3
W·DLTC
(2) DRDY
(2) FMTR·PAR
(6) W4·DATA
(6) W·CRC
W FLAG
H4 LS151
D7 S86
W·CNTR·LD
(6) W5·LD
PU5
(6) WSEQ·CLK
E7 LS161
PL P0 P1 P2 P3 CEP CET CP MR TC
PU6
(6) WLATCH·EN
(6) WSEQ.CLK
K9 LS00
H3 LS259
S Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
E10 LS04
W·RST (6)
W·DATA·STRB (6)
W·FLAG
W·RST (6)
W·PAR(7)
W·DBSY(2)
W·STRB(2)
(8) SYST·RST

650 Formatter
Type 5563
Schematic Diagram



* NOTE: IF X-TAL OSC IS USED REMOVE R9, R10, C37, C38, C39 & Y2.

SHEET 6 OF 11

650 Formatter
Type 5563
Schematic Diagram

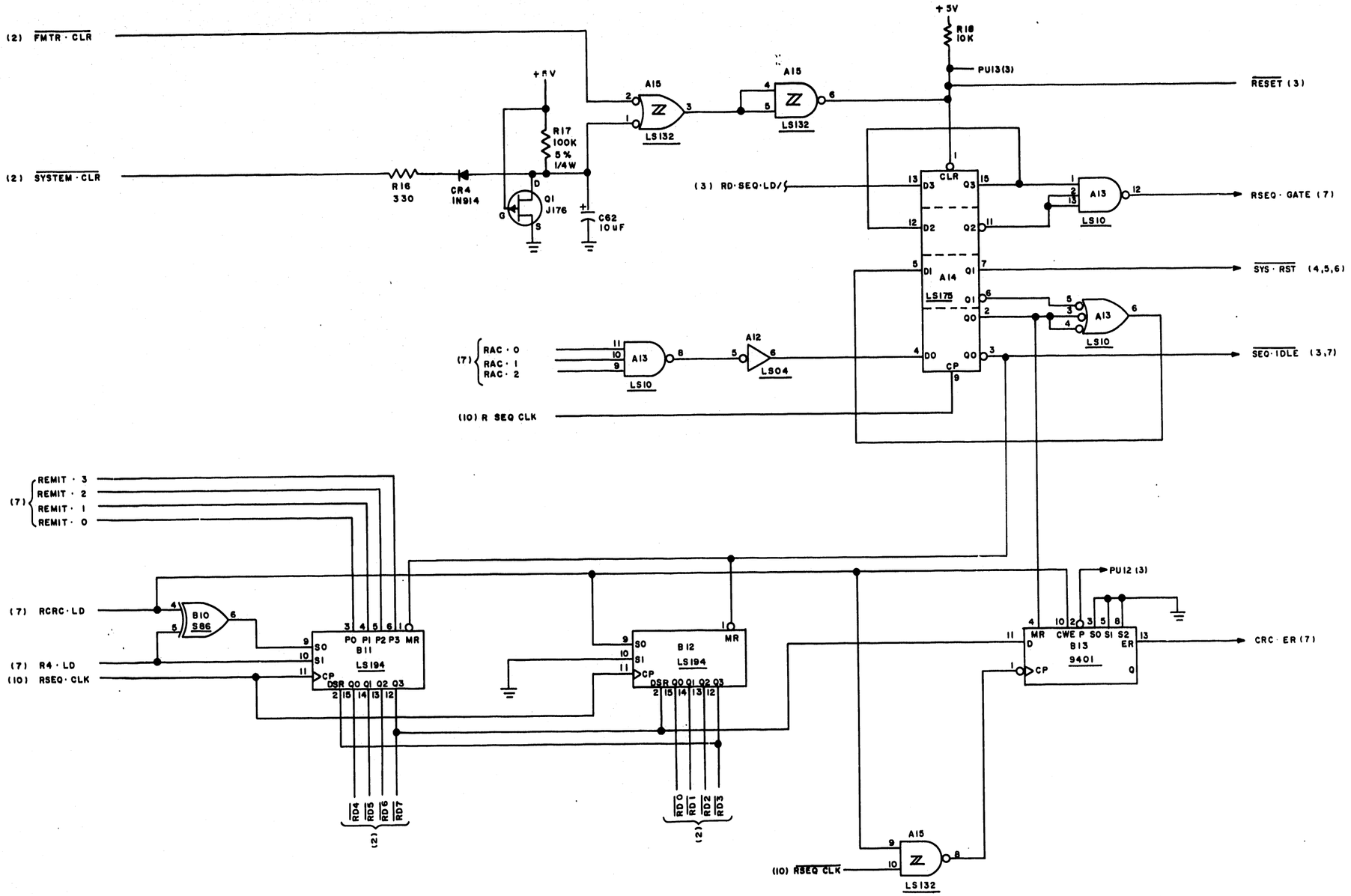
(3) RD.SEQ.LD/
(8) RSEQ.GATE
(10) VCO.CLK/
(10) RSEQ.CLK
RAC.2
RAC.1
RAC.0
RT.INP
(9) PU6
(SATP 2) TEST POINT
(SAJ3)
+5V
R4 10K
+5V
(SATP 1) TEST POINT R.SA.STOP
R.SA.START TEST POINT (SATP6)
R51 4.7K
(2)
CNTRL.BUS.0
CNTRL.BUS.1
CNTRL.BUS.2
CNTRL.BUS.3
CNTRL.BUS.4
CNTRL.BUS.5
CNTRL.BUS.6
CNTRL.BUS.7
C7 LS74
C1 8374
C6 8X02
C2 146-0104-001
C3 146-0105-001
C4 146-0106-002
RAD 8
RAD 7
RAD 6
RAD 5
RAD 4
RAD 3
RAD 2
RAD 1
RAD 0
RLATCHEN
R4LD
CRCR.LD
(8)
RTSEL.3
RTSEL.2
RTSEL.1
RTSEL.0
(RAC.1
(RAC.0
REMIT 0
REMIT 1
REMIT 2
REMIT 3
REMIT 4
REMIT 5
REMIT 6
REMIT 7
REMIT 8

R.TSEL.0
R.TSEL.1
R.TSEL.2
R.TSEL.3
D4 LS151
RDLTC
(9) R.DATA
(8) CRC.ER
(9) R.ENV.ENBL
FWRT
(5) W.PAR
R.FLAG
D7 S86
RT.INP
+5V
R1 10K
PU1(4)
PU1
D2 LS569
D1 LS569
TC
RDLTC/
(10) RSEQ.CLK
(8) RD.STAT.EN
CNTRL.BUS.0
CNTRL.BUS.1
CNTRL.BUS.2
CNTRL.BUS.3
CNTRL.BUS.4
CNTRL.BUS.5
CNTRL.BUS.6
CNTRL.BUS.7

RLATCH.EN
(10) RSEQ.CLK
D10 LS00
D3 LS259
R.TSEL.3
R.TSEL.2
R.TSEL.1
R.TSEL.0
CLR
(8) SEQ.IDLE
ENV EN (9)
FWRT
R.FLAG
PLO.JAM (9)
PLO.TRK EN (10)
RD.GATE (10)
R.DBSY (2)
R.STRB (2)
B9 LS27
R.DBSY (2)

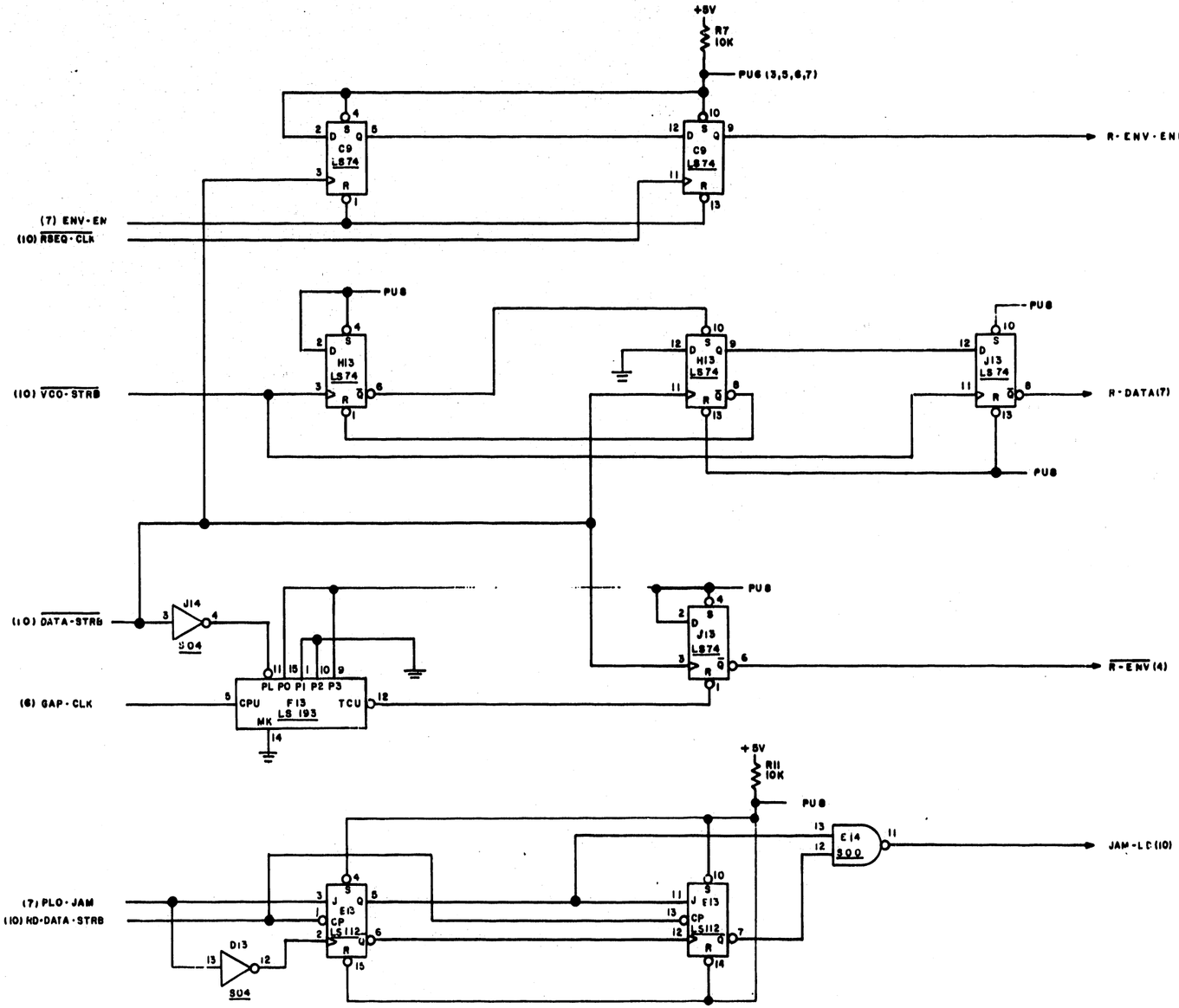
650 Formatter
Type 5563
Schematic Diagram

SHEET 7 OF 11



SHT. 8 OF 11

650 Formatter
Type 5563
Schematic Diagram



SHEET 9 OF 11

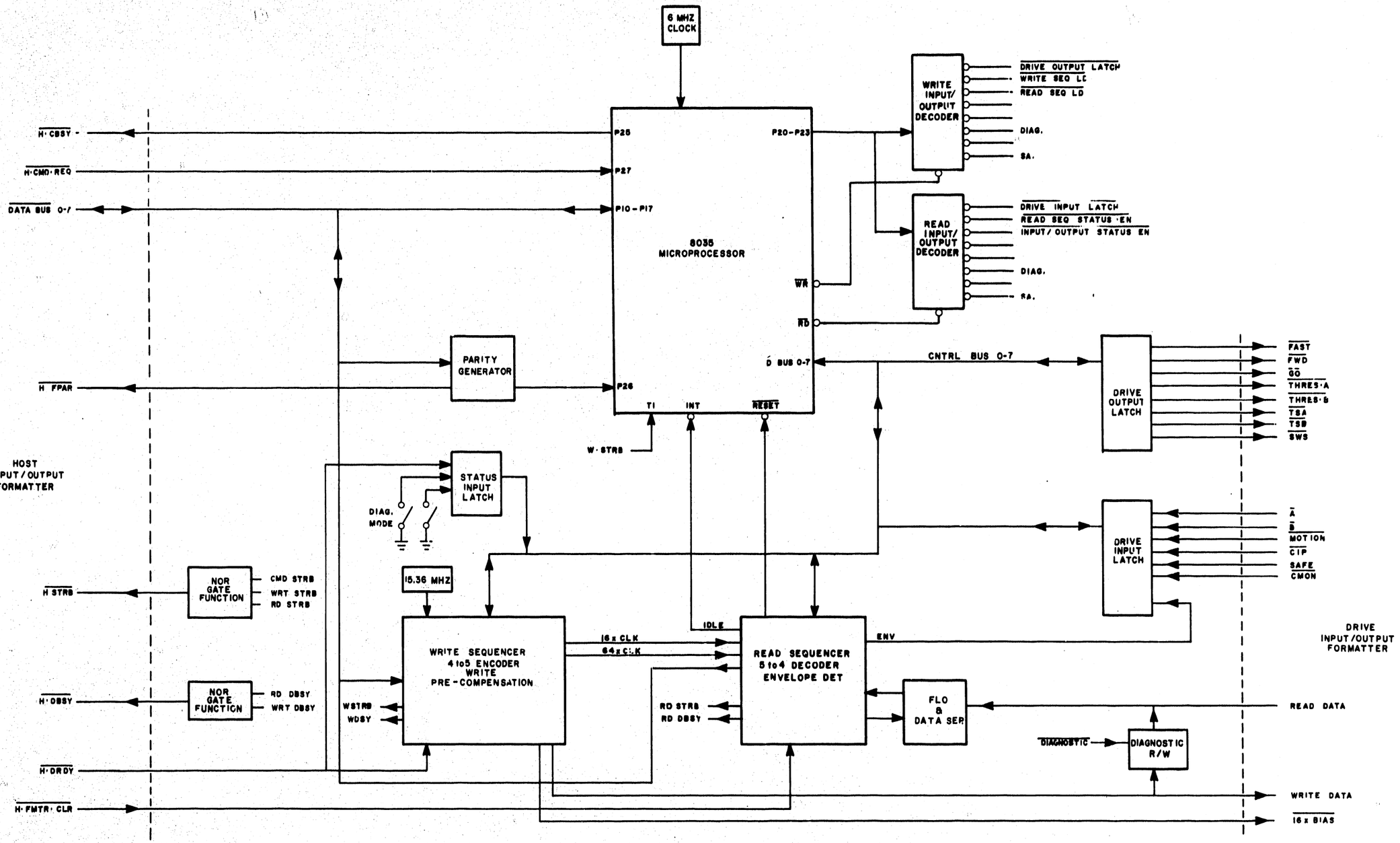
650 Formatter
Type 5563
Schematic Diagram

401-5563-001 V 2
SHT 10 OF 11

+5V
R12 10K
PU9
K13 LS74
(6) W64-CLK
(4) DATA
(7) RD-GATE
(6) GAP-CLK
(9) JAM-LD
(6) W16-CLK
(1) VCO-CLK
N T SA JUMPER (SAJ 6)
D13 S04
K12 S86
DATA STRB (9)
K14 S51
J14 S04
+5V
R14 10K
PU11
F15 S112
E15 S112
+5V
R13 10K
PU14
H14 LS193
PL CPL P0 P1 P2 P3 MR
CPU TCU
VCO-CLK (7)
PU10 (11)
C13 S112
PU9
K12 S86
VCO STRB (9)
R SEQ CLK (7,8)
R SEQ CLK (7,8,9)
RD-DATA-STRB (9)
R44 10K
PU14
H15 S112
PU11
F14 S181
PU11
F15 S112
CLR
32
E14 S00
D15 S08
D14 S00
PMP-TRK (11)
PMP-TRK (11)
PMP-AQ (11)
PMP-AQ (11)
TP1 TP2
E14 S00
D14 S00
D14 S00
(7) PLO-TRK-EN
(9) DATA-STRB
PU12 (3)
C14 LS74
(SAJ 7) PLO SETUP JUMPER
T T BT
N N

SHT 10 OF 11

650 Formatter
Type 5563
Schematic Diagram



SHEET 11 OF 11

650 Formatter
Type 5563
Schematic Diagram

NOTES:

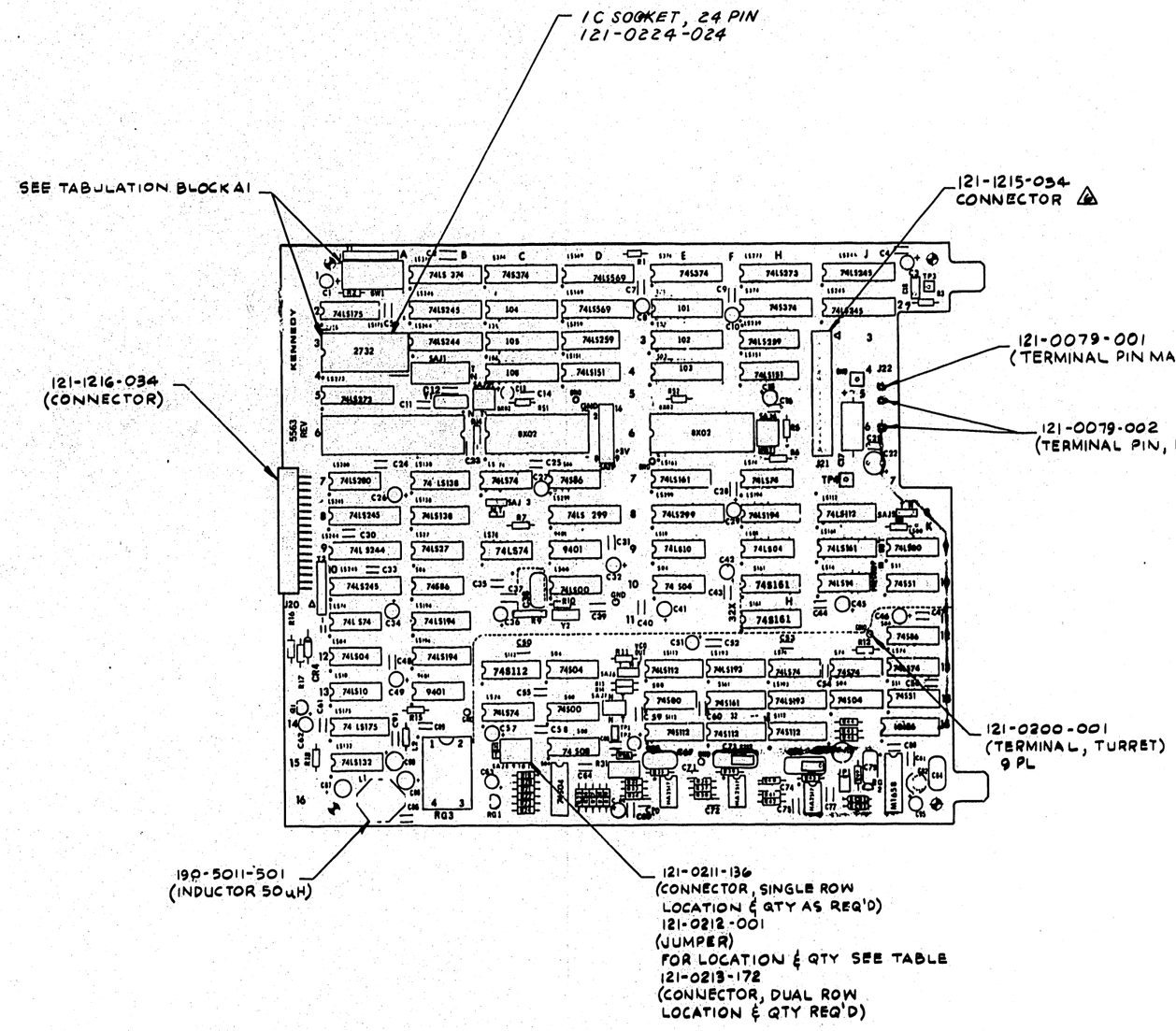
1. INK STAMP DASH NO. AND LATEST B/M REVISION LETTER.

[redacted]

2. REFERENCE: P.C. BOARD 391-5563-001
PHOTOMASTER 405-5563-001
BILL OF MAT'L 190-5563-001
SCHEMATIC 401-5563-001

⚠5 INSTALL AT TEST LEVEL
⚠6 MOUNT ON FARSIDE

KENNEDY P/N	DESCP.	LOCATION
115-0016-101	100pF	C67, 79
115-0016-150	15pF	C11, 12, 38
115-0016-201	200pF	C84
115-0026-003	0.01	C69, 69
115-0026-005	0.1	C2, 4, 5, 7, 9,
115-0026-009	0.1	C14, 16, 18, 21, 23,
115-0026-009	0.1	C24, 25, 28, 30, 31,
115-0026-009	0.1	C33, 35, 40, 43, 44,
115-0026-009	0.1	C47, 49, 50, 52, 00,
115-0026-009	0.1	C54, 55, 56, 58, 59,
115-0026-009	0.1	C60, 61, 64, 70, 71,
115-0026-009	0.1	C72, 74, 75, 77, 80,
115-0026-009	0.1	C81, 86, 91
115-0026-011	0.15	C89
115-0026-015	22pF	C37, 39
115-0199-106	10 16V	C62
115-0204-002	6.8 16V	C1, 3, 8, 10, 13,
115-0204-002	6.8 16V	C15, 26, 27, 29, 32,
115-0204-002	6.8 16V	C34, 36, 41, 42, 45,
115-0204-002	6.8 16V	C46, 49, 51, 57, 63,
115-0204-002	6.8 16V	C66, 68, 85
115-2516-336	33 16V	C22, 78, 87, 88, 90
115-0276-002	5.5-40pF	C82
115-1510-107	100	C17
115-5040-332	0.0033	C73, 76
116-0002-026	6.00MHz	Y1
116-0002-027	15.36MHz	Y2
116-0006-101	1.00uH	L2
140-0013-001	-12VDC REG	RG3
146-0101-001	PROM 101	E2
146-0102-001	PROM 102	E3
146-0103-002	PROM 103	E4
146-0104-002	PROM 104	C2
146-0105-002	PROM 105	C3
146-0106-002	PROM 106	C4
147-0002-102	1K	R9, 10, 47
147-0002-103	10K	R1, 2, 3, 4, 5,
147-0002-103	10K	R6, 7, 8, 11, 12,
147-0002-103	10K	R13, 14, 15, 18, 29,
147-0002-103	10K	R30, 44
147-0002-104	100K	R17
147-0002-331	330	R16
147-0002-393	39K	R36, 38, 41, 42
147-0002-472	4.7K	R51, 52
147-0002-511	510	R19, 20, 21, 22, 23,
147-0002-511	510	R24, 45, 48
147-0009-274	6.98K	R33, 34
147-0009-290	10.2K	R39, 43
147-0009-298	12.4K	R26, 27, 32
147-0009-307	15.4K	R35
147-0009-319	20.5K	R37, 40
147-0009-334	47.5K	R25, 28
147-0036-103	SIP 10K	T1, 2
147-0037-103	POT 10K	R31
148-0177-001	J1746	Q1
148-7500-001	1N914	CR2, 3, 4
149-0045-003	74851	K10, K14
149-0108-101	74LS194	B11, B12, H8
149-0126-001	74800	D14, E14
149-0126-002	74L800	D10, K9
149-0132-001	74LS112	E13, J8
149-0132-002	748112	C13, E15, F15, H15
149-0136-002	74LS27	B9
149-0138-002	74LS138	B7, B8
149-0151-002	74LS151	D4, H4
149-0154-002	74LS14	J10
149-0161-001	74LS161	E7, J9
149-0170-001	74S74	J13
149-0170-002	74LS74	A11, C7, C9, C14, H7,
149-0170-002	74LS74	H13, K13
149-0175-002	74LS175	A2, A14
149-0176-001	74LS280	A7
149-0178-001	2917	E16, F16, H16
149-0183-001	748374	C1, E1, H2
149-0183-002	74LS374	B1
149-0184-001	74S04	B10, D7, K12
149-0189-001	74LS259	D3, H3
149-0191-001	74LS244	A9, B3,
149-0192-001	74LS245	A8, A10, B2, J1, J2
149-0193-001	74LS193	F13, H14
149-0194-001	74LS299	D8, E8
149-0196-001	74LS569	D1, D2
149-0198-001	8X02	C6, E6
149-0201-001	9401	B13, D9
149-0204-001	74S04	D13, D16, E10, J14
149-0204-002	74LS04	A12, H9
149-0208-001	74S08	D15
149-0210-002	74LS10	A13, E9
149-0261-001	748161	F14, H10, H11
149-0273-001	74LS273	A5, H1
149-0332-002	74LS132	A15
149-1129-001	MC10125	K15
149-1698-001	MC1698	K16
149-7805-001	78L05	RG1(C16)
149-7905-001	79L05	RG2(J16)
149-8035-001	8035	A6

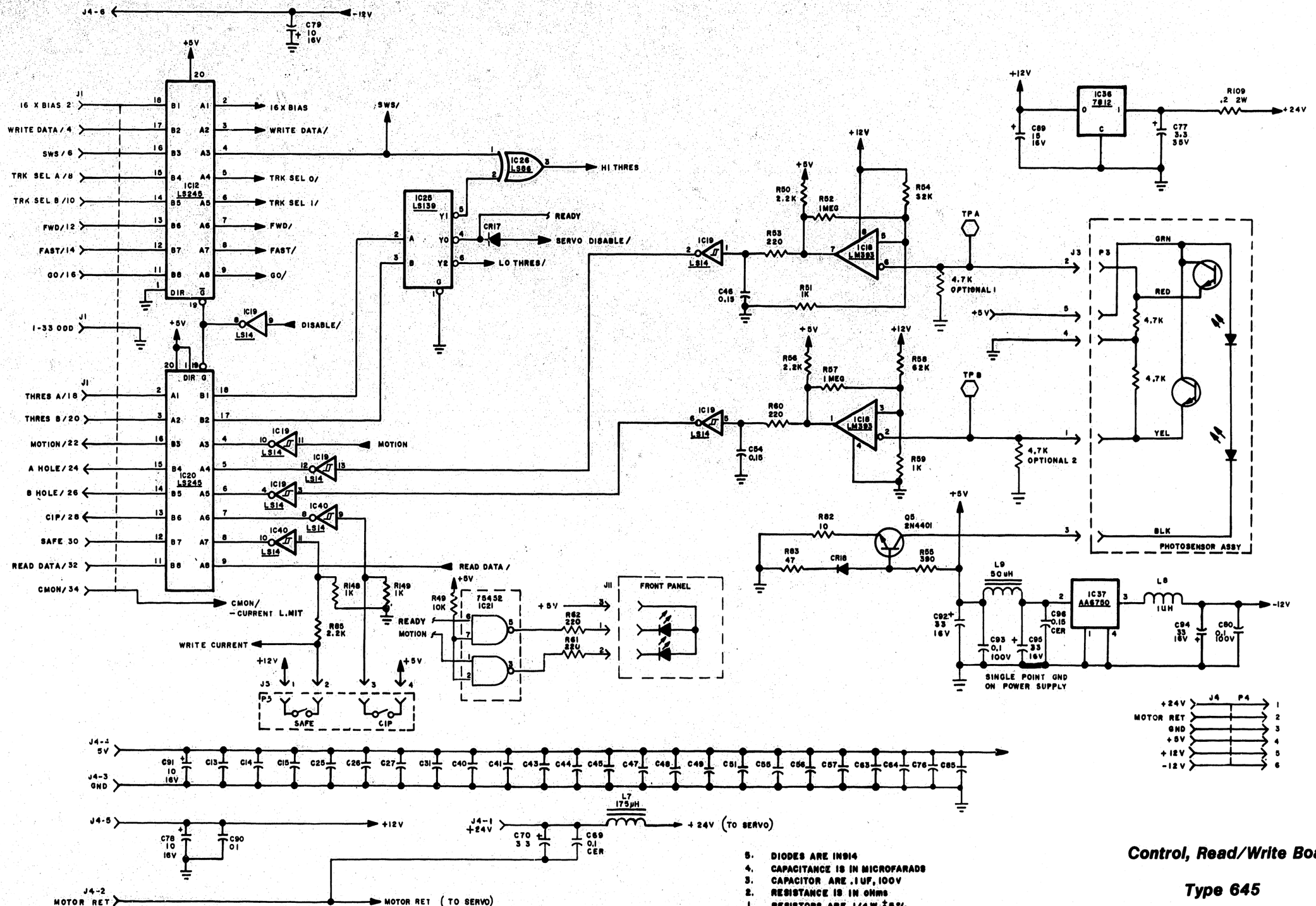


FORMATTER BOARD

JUMPER INSTL. TABLE		
LABEL	LCTN	QTY
SAJ1	B4	8
SAJ2	C5	3
SAJ3	C8	1
SAJ4	H6	3
SAJ5	K8	1
SAJ6	D13	1
SAJ7	D14	2
SAJ8	C15	1
SAJ9	C15	1
SAJ10	C15	1
SAJ11	C15	1
JP1	J16	1

TYPICAL SA JUMPER INSTL

N T
N= NORMAL
T= TEST



5. DIODES ARE IN914
4. CAPACITANCE IS IN MICROFARADS
3. CAPACITOR ARE .1 UF, 100V
2. RESISTANCE IS IN ohms
1. RESISTORS ARE 1/4 W, ±5%

NOTES: UNLESS OTHERWISE SPECIFIED

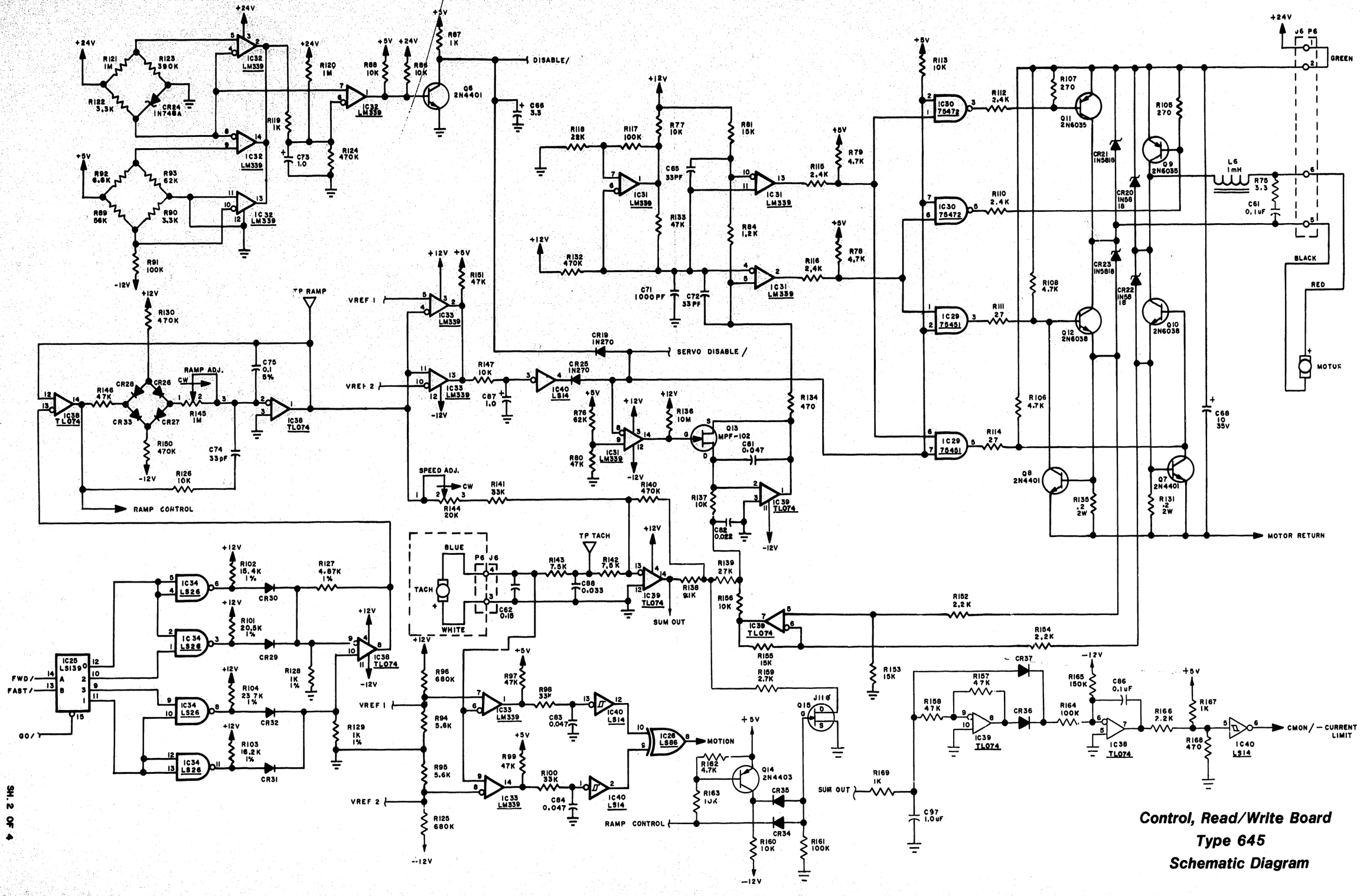
SH. 1 OF 4

Control, Read/Write Board

Type 645

Schematic Diagram

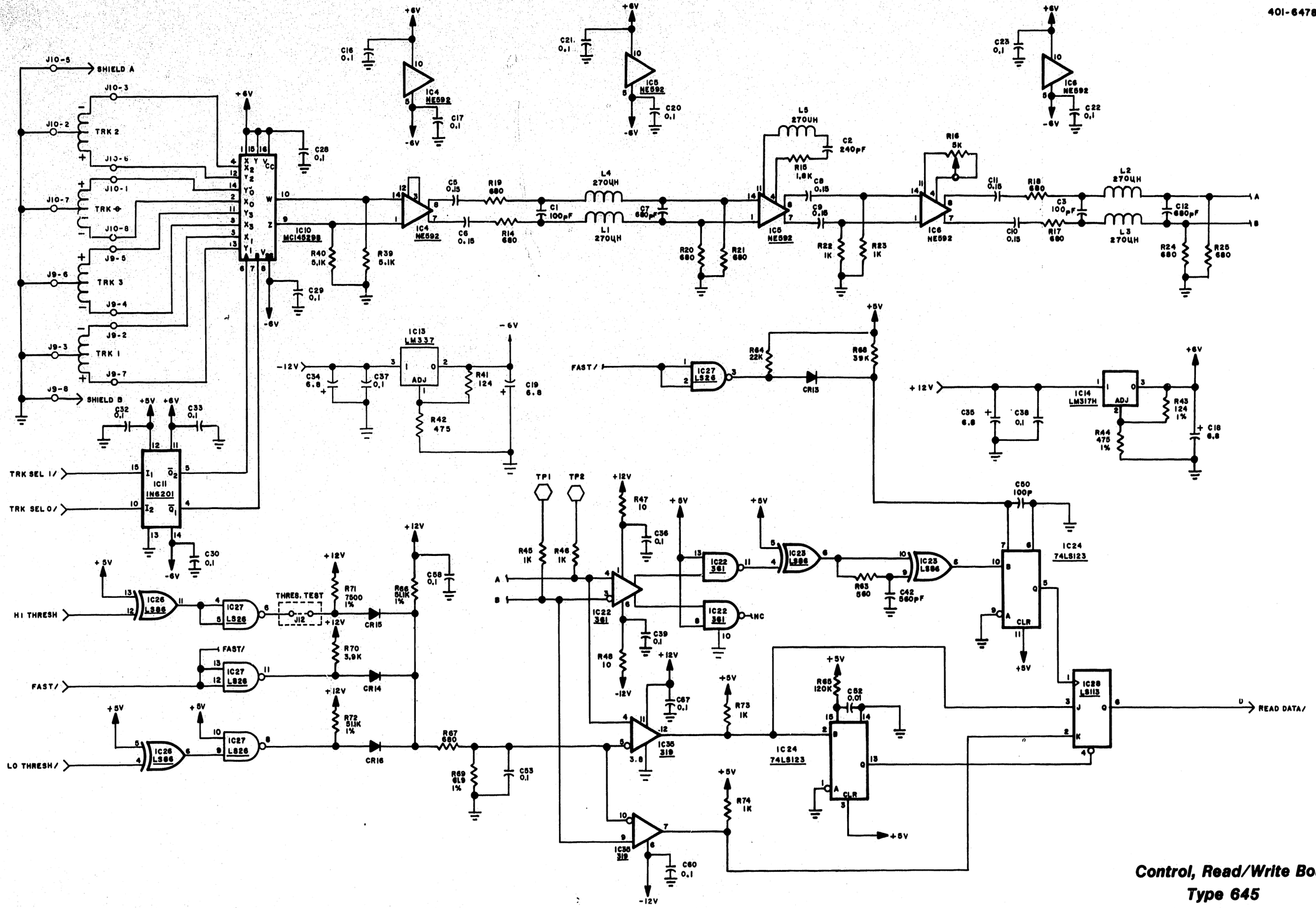
401-6478-001 NI



SH. 2 OF 4

Control, Read/Write Board
Type 645
Schematic Diagram

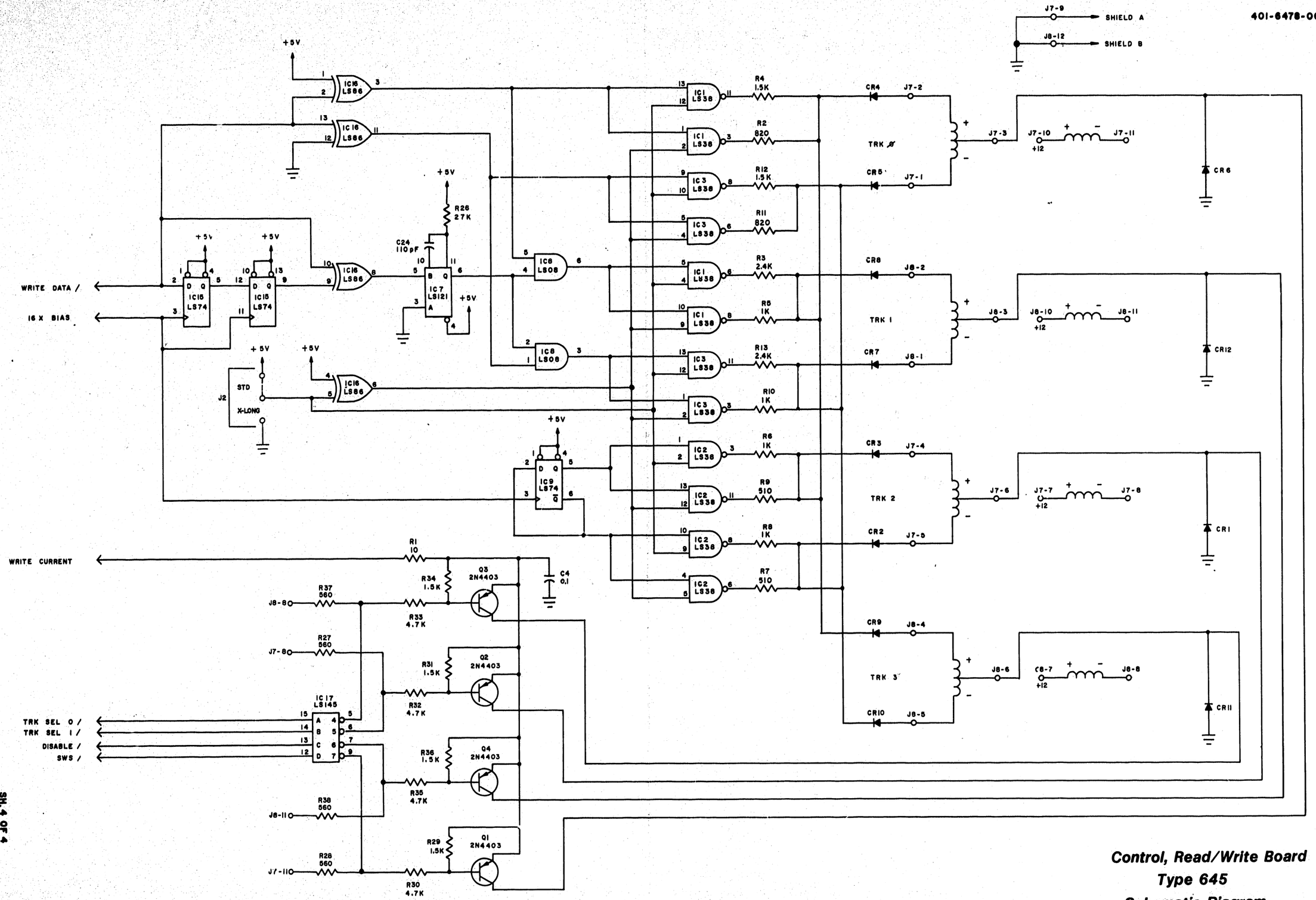
401-6478-001NI



SH 3 OF 4

Control, Read/Write Board
Type 645
Schematic Diagram

401-6478-001N1



SH. 4 OF 4

Control, Read/Write Board
Type 645
Schematic Diagram

WANG LABORATORIES, INC.
ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL. (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

PRINTED IN U.S.A.

END