XEBEC - XFD 108

XEBEC SYSTEMS, INC.

MODEL XFD-108

FLEXIBLE DISK SYSTEM

OPERATION AND MAINTENANCE MANUAL

XEBEC PART NUMBER: 350227

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SECTION 1
INTRODUCTION

1.1 GENERAL

The Xebec XFD-108 Flexible Disk System is an auxiliary medium-capacity random-access storage system specifically designed for the PDP-8/E digital computers, manufactured by Digital Equipment Corporation. The modular XFD-108 consists of an I/O card and up to four moving-head, compliant-disk recorders. One or two disk drive units can be mounted in a single chassis. Two chassis units are required for a system with three or four recorders.

The recording medium is an oxide-coated Mylar[R] disk enclosed in a plastic sheath. Each disk is easily changed for fast, convenient data storage or playback. Access to stored data is faster than conventional sequential recording media (such as magnetic tape) and the recording medium cost is held at a low level.

1.2 EQUIPMENT SUPPLIED

The XFD-108 System is shipped with all equipment necessary for operation with the PDP-8/E minicomputer. The system consists of the following units:

1.2.1 Disk Recorder Chassis Unit(s)

Each chassis unit contains a power supply for one or two disk drives, a fan, the disk drive logic, disk formatter, the disk electronics, power switching controls, ac line cord and all internal cables. Slides and brackets are supplied for installation in a standard 19" RETMA rack.

For systems with three or four disk drive units, the one or two additional drive units are supplied in a second chassis unit, with a cable that interconnects the two chassis units.

1.2.2 Coupler Circuit Card

The coupler card fits into one of the I/O slots in the PDP-8/E computer. It plugs into the computer main frame bus or expansion chassis bus, and controls the following functions:

- Program interrupt
- Device decoding
- Data break control
- Automatic program loading

Table 1-1. XFD-108 Specifications

Capacity per Disk	163,840 12-bit words (not including preamble or CRC words)
Number of Tracks	64
Number of Sectors	10 standard, with 16 and 8 also available
Words/Sector	256 data + 1 preamble + 1 CRC word
Rotational Speed	375 RPM
Access Time	10 ms track-to-track
Settling Time on Last Track Moved	10 ms
Data Transfer Rate	20.5 kilo words per second
Word Size	12 bits
Number of Drives Controlled	Up to 4
Mode of Data Transfer	Data break (single cycle)
Device Address	30_8 may be changed to any address from $0-77_8$
I/O Slots Required	1
Size	10-1/2" H x 19-1/8" x 17-1/2" wide; fits 19" RETMA rack
Operating Temperature Range	60^oF to 95^oF
Relative Humidity	20% to 80%
AC Power Requirement	115V ac, 0 to 60 Hz, 5 amp; 230V ac optional
Weight	75 pounds (with 2 drives installed)

1.2.2.1 Optional ROM/RIM/IPL Bootstrap Circuits. The coupler card is used to mount the circuit components (logic and ROM) for implementing the bootstrap program loaders. This circuitry is capable of hardware loading of programs using the SW switch on the PDP-8/E front panel or with a special toggle switch (with the IPL option only) near the power switch on the recorder chassis. The ROM option also allows bootstrap loading with the RIM.

1.2.3 System Interconnect Cable Assemblies

The standard cable assembly consists of two cables. One connects the coupler circuit card directly to the recorder chassis. The other interconnects the formatter circuit and drive logic cards in the recorder chassis. A third cable is provided to connect the main recorder chassis to the optional recorder chassis for systems with more than two disk drives.

1.3 AVAILABLE SOFTWARE

Two standard programs are available for use with the Xebec XFD-108 and the PDP-8/E series computers. The programs are briefly described below; for additional details, See Section 4.

1.3.1 Diagnostic Program

The diagnostic program verifies correct system operation, and provides a first level of fault isolation if malfunctions occur. The diagnostic is also used to initialize new disks by writing header words and zeroing the data field on each sector of every track.

The diagnostic program 1) exercises all position and data transfer functions provided by the controller, 2) checks all status and error flags returned by the controller, 3) verifies proper operation of all units connected to the controller, and 4) checks that part of the computer interrupt system used by the controller. Some of the tests included in the diagnostic are designed to isolate errors which depend on the data content or mode of a data transfer. Another set of tests is devoted to forcing error conditions and checking to see that they are properly reported by the controller. Tests are also provided to check for proper sector formatting and unit-to-unit compatibility.

1.3.2 OS/8 Program Configuration

The OS/8 is the DEC disk operating system used for the PDP-8/E series of computers. The XFD-108 uses version 3 of OS/8. Within this system, the XFD-108 can be used as a system device (i.e., the system resides on the disk storage) or as a non-system device (i.e., the disk is used for storage only. program resides in the PDP-8/E memory or elsewhere). The XFD-108 provides 640 or 1200_8 OS/8 standard 256(12-bit) word memory blocks. Because of Xebec's unique 10-sector format, 25% more data storage is provided than with 8 sectors. The XFD-108 is also capable of hardware bootstrapping the OS/8 program with the ROM option described above in Section 1.2.2.1.

SECTION 2
FUNCTIONAL DESCRIPTION

2.1 CONTROL FUNCTIONS

Each of the recorder chassis units is computer-controlled. Except for the line power switch operation and flexible disk loading, there are no operator actions required. For additional details on the recorder controls, see Section 3.

2.2 RECORDING MEDIUM

The Xebec XFD-108 Flexible Disk System uses flexible magnetic disk cartridges, such as the Memorex FD/IV. The disk has a Mylar[R] substrate, and is coated with a magnetic iron oxide material. For protection, the disk is enclosed in a flexible vinyl envelope that is sealed around the edges, and lined with a self-cleaning wiper. The read/write head has access to the disk through an oval slot in the envelope. See Figure 2-1. One corner of the cartridge has a notch, which ensures that the cartridge is installed in the drive properly. To prevent further recording on the disk, a write-protect tab may be affixed to the cartridge. See Section 3.

2.3 RECORDING FORMAT

Each recorder chassis unit normally holds two disk drive recorder units for a maximum of four units within the XFD-108 system. Each disk drive unit has a single moving-head recorder that will record up to 64 tracks on one side of a single disk. Each disk – and hence, each track – is divided into 10 sectors. The number of sectors may be changed to 8 or 16 by changing jumpers on the coupler card that plugs into the PDP-8/E Computer (See Section 3). In operation, each sector is identified by a sector hole, which is counted by electro-optical sensor logic from the index hole. The disk sector and track configuration is shown in Figure 2-2.

2.4 SECTOR FORMAT

2.4.1 General

The standard disk format has 10 sectors. On any track, each sector can store 256 user-accessible data words (12 bits each), plus non-accessible overhead words. The overhead words are added by the control logic to ensure disk interchangeability and synchronization.

The formats are listed in Table 2-1, which provides track capacity as a function of sector divisions. Note that if the overhead words are discounted, the track capacity per revolution is a constant (2560), which equals the product of the number

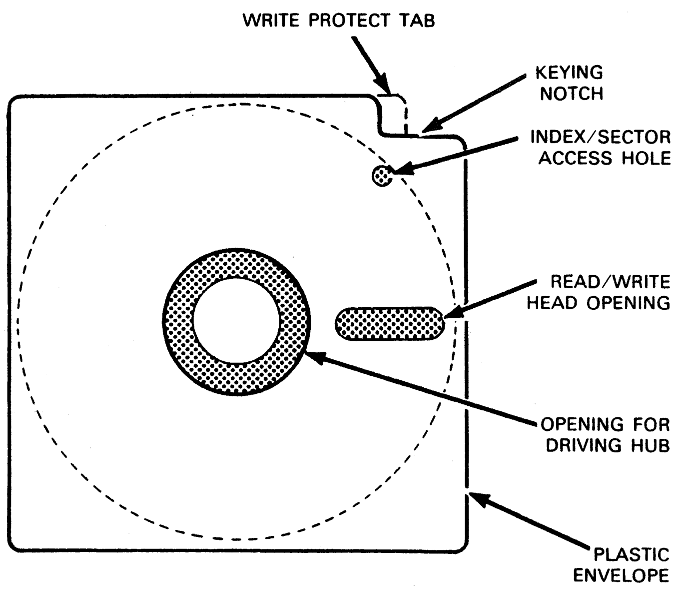


Figure 2-1 Disk Cartridge Configuration

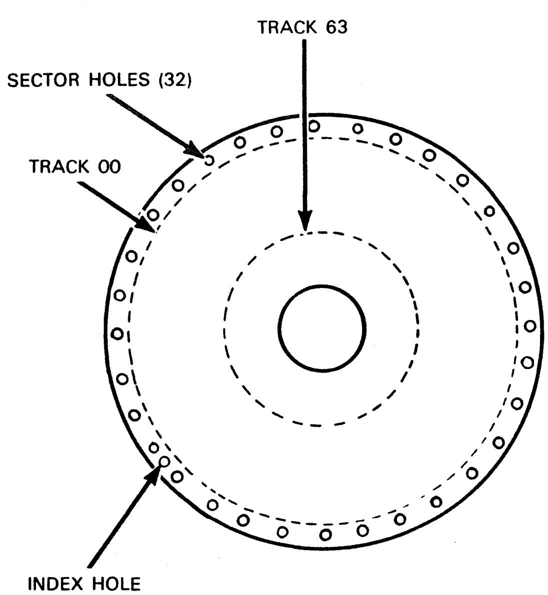


Figure 2-2 Disk Configuration and Recording Format

of sectors and the words per data field. The sector format is shown in Figure 2-3, and described in the following paragraphs. Section 3 contains jumper wiring instructions for other formats.

Table 2-1. Allowable Sector Configuration

Sectors	Data Words/Block Words/Sector	Number of Blocks
8	320	512
10*	256*	640*
16	160	1024

* Standard with OS/8.
** Number of Tracks is 64.

2.4.2 Bit Synchronization

The bit sync field consists of a series of 128 data zeros recorded at the beginning of the sector. It synchronizes the self-clocking circuit of the read data decoder, and ensures interchangeability between cartridges and disk drives. This field is not user-accessible.

2.4.3 Accessible Data

This field is user-accessible and its contents are not restricted. In the standard 10-sector recording format, this field can store 256 data words of 12 bits, which are recorded serially.

2.4.3.1 Error Checking. For checking data field errors Xebec uses a hard-wired CRC error-checking polynomial, which has the form:

$$X^{16} + X^{15} + X^2 + 1$$

It is the industry standard and provides error checking for bursts of up to 16 consecutive dropouts.

2.4.4 Postamble

The hardware generates additional data after the last word of the accessible data field to ensure that no bit crowding exists on the last word of useful data. The postamble is not accessible by software.

2.4.5 End Space

Space at the sector end allows for worst-case speed variation, media tolerances, and drive-to-drive interchangeability.

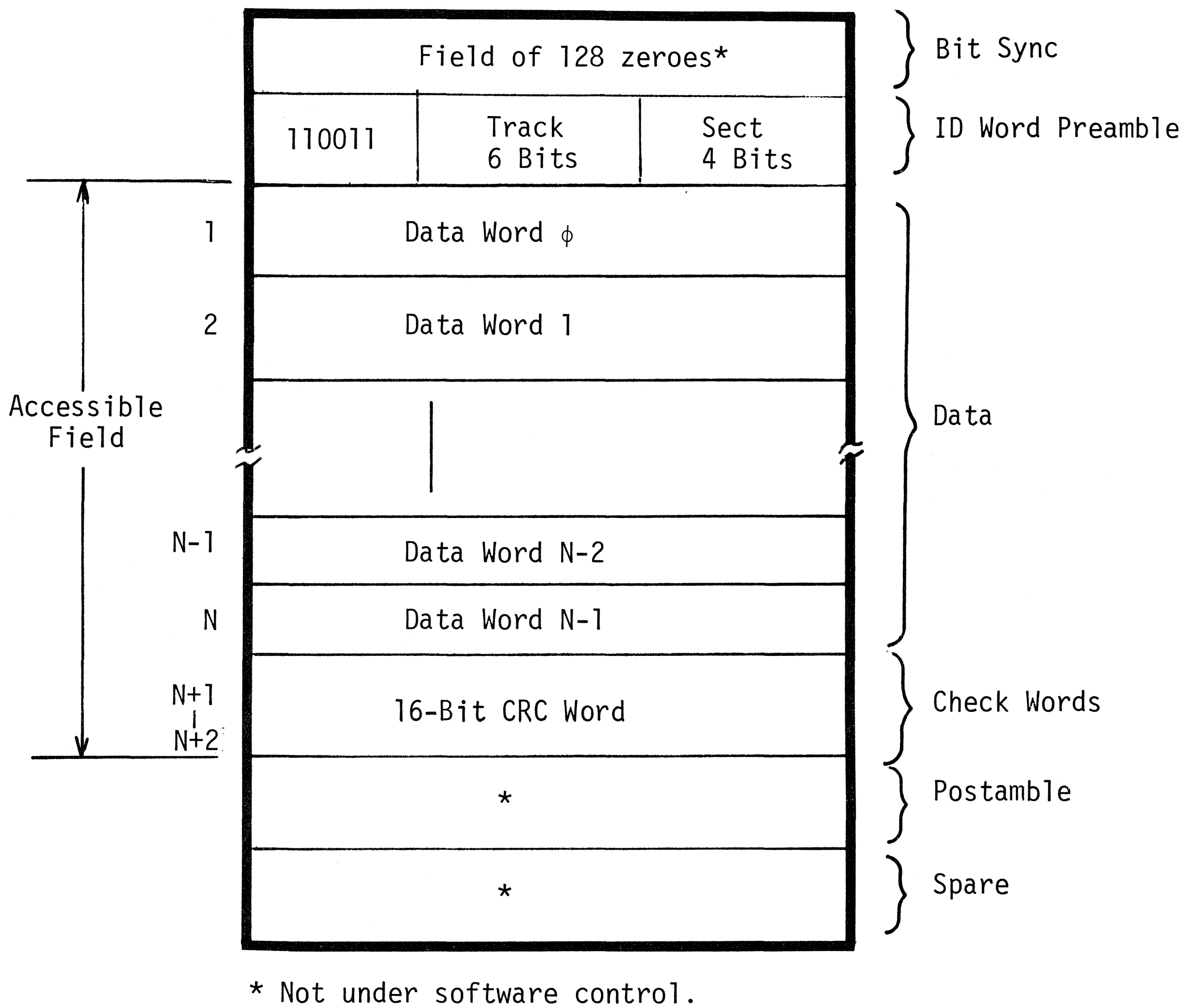


Figure 2-3. XFD-108 Sector Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	0	1	1	TRACK ADDRESS						SECTOR ADDRESS			

WORD SYNCH — SPECIFIES BLOCK 0-639

10 sectors/track

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	0	1	1	TRACK ADDRESS						SECTOR ADDRESS			

WORD SYNCH — SPECIFIES BLOCK 0-1023

16 sectors/track

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	0	1	1	TRACK ADDRESS						0	SECTOR ADDRESS		

WORD SYNCH — SPECIFIES BLOCK 0-511

8 sectors/track

Figure 2-4. ID Word Formats

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION PROCEDURES

3.1.1 Unpacking

1) Cut the tape securing the top of the shipping container; be careful not to cut deeper than is necessary to cut the tape.

2) Remove and save box on top of the unit; it contains the coupler card, cables, etc.

3) Remove the rack mount slides from the top of the unit, and the manual and disk packs from the sides of the unit.

4) Lift the unit and the foam shipping pads from the box.

5) Remove the foam shipping pads and the plastic sheet from the unit.

6) Remove the coupler card, cables, etc. from the box that was on top of the unit.

7) Replace all foam pads, plastic sheets, box and other packing materials in the shipping containers and save. If the unit is to be reshipped (e.g., for factory service), it must be shipped in this container to avoid shipping damage. See Para. 3.3 for repacking instructions.

3.1.2 Receiving Inspection

1) Remove the unit from the plastic bag and inspect for shipping damage. If any damage is noted, contact the shipping carrier immediately to file an insurance claim.

2) Check all system components against the configuration sheet, which was taped to the top of the box containing the control card and cables. Report any missing items immediately.

3) Loosen the screws on both sides and the back of the chassis and remove the top cover. It is not necessary to remove these screws.

4) Check the chassis interior to ensure that all screws are tight, the printed circuit cards are secure, the internal cables are in place, and the interior and exterior fuses are in place.

3.1.3 Preliminary Setup and Tests

This test verifies that the power supply is operational and that the recorders are properly connected.

3.1.3.1 Line Power. The XFD-108 system is designed for operation on 115V ac, 50 to 60 Hz, single phase line power. Do not attempt to convert the XFD-108 system for 230V operation. (230V systems are available upon original order from the Xebec Systems factory.) Line power is supplied via a single power input cable to each recorder chassis in the system. Maximum current is 5 amperes per chassis unit.

3.1.3.2 Grounding. All chassis units are equipped with a standard 3-wire power cable that connects the chassis to earth ground when plugged into the appropriate receptacle. For use with a 2-contact receptacle, use an adapter and connect the third (ground) lead to earth ground.

3.1.3.3 DC Power Check. Plug in the line power cord at the rear of the chassis, and then connect the cord to the appropriate ac receptacle. Do not connect any other cables to the chassis, and do not place any disk in the drive. Turn the front panel POWER switch to ON. If the POWER indicator light is ON, the power supply is operational. If the indicator is not ON, check for:

Blown fuse
Burned-out bulb
Defective power supply

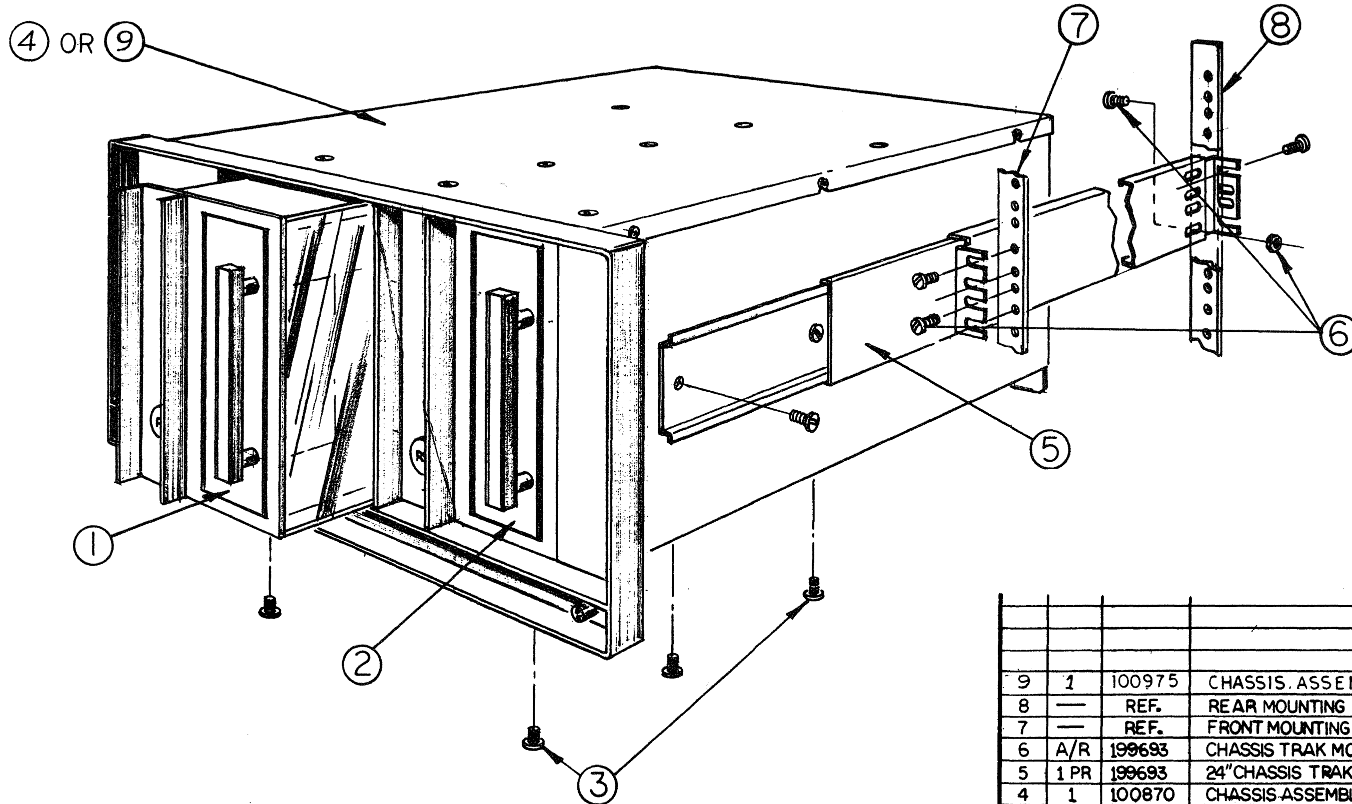
Check the dc power supply voltages on the power supply terminals. See Para. 5.5. The voltage tolerances are listed in Table 5-1. The power supplies are not field-adjustable. If they are out of tolerance, they should be returned to the factory for repair. See Para. 5.3. If the system has two recorder chassis units, check each chassis unit.

3.1.3.4 Drive Cable Check. Depress the front panel RUN pushbutton on each disk drive unit in each chassis. The front panel RUN indicator light should come on.

3.1.4 Rack-Mounting Procedure

1) The Xebec XFD-108 chassis unit(s) are normally mounted in a standard 19" rack; all necessary mounting hardware is supplied. During installation, be sure that the chassis units are close enough to the PDP-8/E computer so that the cables are not subject to unnecessary stress when the chassis units are extended from the rack for service. Allow at least 2-1/2 feet of cable slack.

2) Separate the chassis slide and mount it on chassis as shown in Figure 3-1. Use the 10-32 x 3/8 screws supplied.



9	1	100975	CHASSIS. ASSEMBLY
8	—	REF.	REAR MOUNTING RAIL
7	—	REF.	FRONT MOUNTING RAIL
6	A/R	199693	CHASSIS TRAK MOUNTING HDWR.
5	1 PR	199693	24" CHASSIS TRAK SLIDE KIT
4	1	100870	CHASSIS ASSEMBLY
3	6	199352	8/32X3/8 UNIT MOUNTING SCREWS
2	1	100872	UNIT 1 ASSEMBLY
1	1	100871	UNIT Ø ASSEMBLY
ITEM	QUAN.	XPN	DESCRIPTION

XEBEC SYSYSTEMS INC

FLEXIBLE DISK SYSTEM

UNIT AND SLIDE KIT ASSEMBLY

DRAWN B. Kadzewick DATE 6-29-73 | X.P.N. 100820 | C

Figure 3-1
Rack Mounting and Chassis
Hardware Configuration

3) Attach the rear slide mount bracket to the rear tapped rail. The center line of the bracket will be 5.25" below the top of the XFD-108 chassis when installed. Use 10-32 x 3/8 screws.

4) Attach the front slide mounting bracket to the inside of the front tapped rail with 10-32 x 3/8" screws.

5) Connect the rear extension bracket to the back end of the cabinet slide section with 10-32 x 3/8" screws and nuts.

6) Before the XFD-108 is inserted in the cabinet, back out the pawl fasteners to their full extension by turning the right-hand pawl fastener fully CCW, and the left-hand fastener fully CW.

7) Extend the cabinet slide sections fully, until they are locked.

8) Slide the chassis onto the extended slide sections. Release the locks as the unit is pushed forward.

9) Push the unit forward until the front panel is in contact with the tapped rails. It may be necessary to loosen the screws holding the slides to the tapped rails, to allow the unit to center. Be sure to tighten the screws after centering.

10) When all adjustments are complete, tighten pawl fasteners to retain chassis in cabinet.

3.1.5 System Interconnection

The XFD-108 uses flat, flexible cables. The coupler card connector plugs directly into wire wrap pins. The recorder chassis connectors plug directly onto the edge connectors of the formatter and drive logic drive PCB's. The cables are connected through slots in the chassis as shown in Figure 3-2. If only one recorder chassis is used, connect the coupler to J3 on the recorder chassis. Use the short jumper cable to connect J4 to J2. If a second recorder chassis is used, connect J1 of the main recorder chassis to J2 of the second chassis.

3.1.6 Coupler Card Installation

If the coupler card is to be used with non-standard priority, address or format, wiring changes will be required before installation. These changes are outlined in Section 3.1.7. For standard operation in a PDP-8E computer, proceed as follows:

3.1.6.1 <u>I/O Slot Selection.</u> The XFD-108 coupler card may be installed in any available I/O slot in the PDP-8/E main frame. It can also be installed in the I/O extender chassis. The I/O slot should be selected for convenience in cable routing.

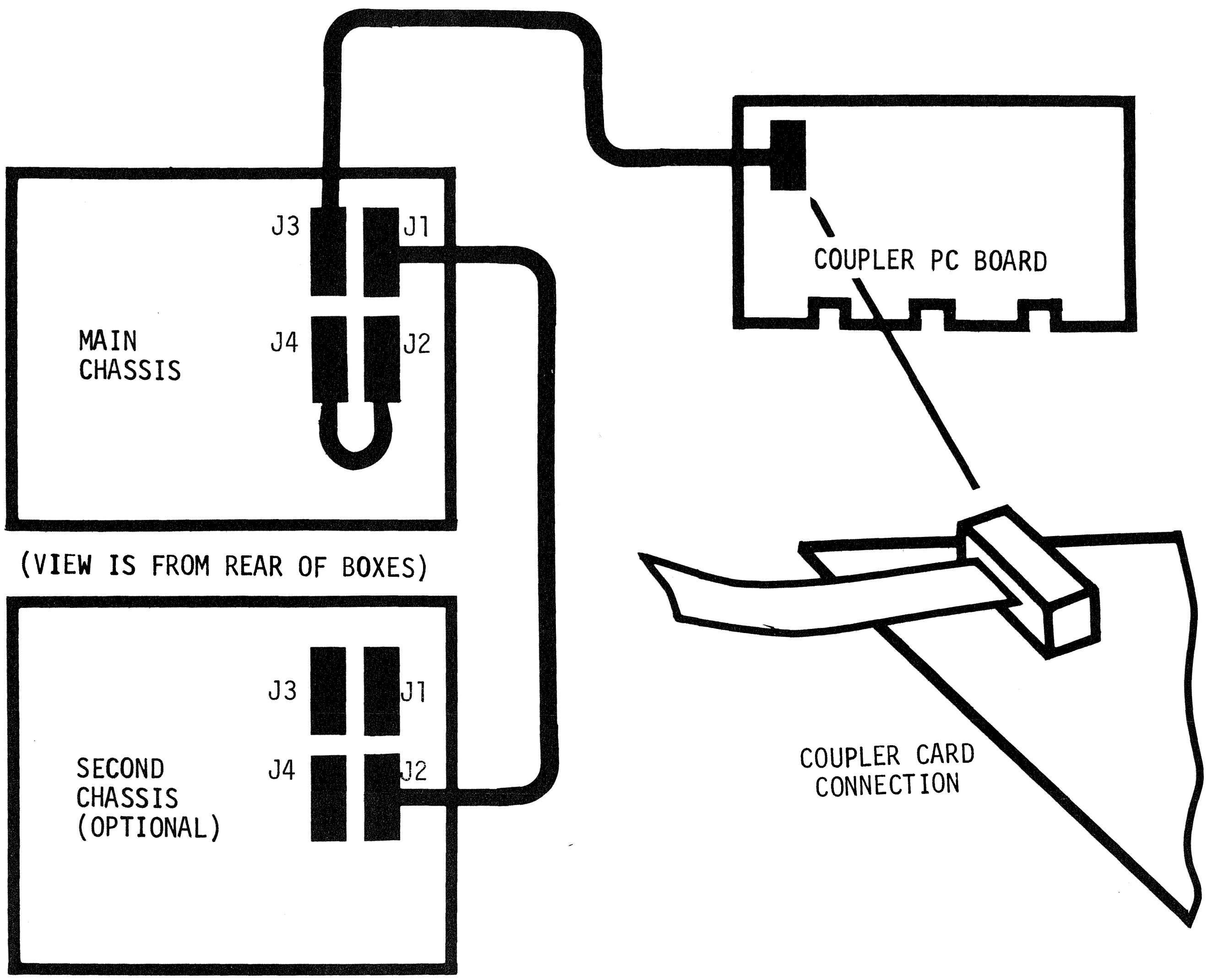


Figure 3-2. Cable Interconnection

3.1.6.2 Coupler Card Plug-in. Install the coupler card into the selected I/O slot. Be sure the edge connectors are properly positioned before seating the board. This will prevent damage to the connectors. Dress down the cable. Keep the cables to the various I/O boards neatly packed.

3.1.7 Coupler Card Modifications

To modify the data format, device address, device priority, or the paper tape loader speed (IPL/ROM option only), certain wiring trace changes must be made on the coupler board. (Data format changes may also require wiring changes on the formatter board as discussed in Section 3.1.8). The coupler PCB is etched with coordinates as shown in Figure 3-3. The IC address is given in the form AX-Y, where A is the vertical position with the board plugged in, X is the horizontal coordinate, and Y is the IC pin number. Pin numbers increase from 1 to 7 or 8 going down the left side of the IC (looking from the top), and from 8 to 9 to 14 or 16 going up the right side. The edge connector pins have the address form AB-X, where A is the pin group (A to D), and B is the pin within the group (A to V). All pins on the front of the board have X = 1; on the back, X = 2 for all pins. The wiring modifications are all made on larger than normal pads for ease in location and soldering.

3.1.7.1 Device Priority Modifications. There are three levels of priority allowed in the PDP-8/E. The XFD-108 is normally provided with device priority 1. The priority can be changed to 2 or 3 by the method illustrated in Figure 3-4. To effect a priority 2, first disground C5-5 and reconnect C5-5 to A9-13. Now, disconnect C8-11 from AR-1 and reconnect C8-11 to AS-1. To effect a priority 3, first disground C5-5 and reconnect it to A9-13 as with priority 2. In addition, disground C5-3 and reconnect it to A9-10. Now, disconnect C8-11 from AS-1 and reconnect it to AU-1.

3.1.7.2 Device Address Modification. The device address for the XFD-108 is two octal digits, and is normally set at 30_8. The PCB traces for changing the device address are shown in Figure 3-5. To change the address to any octal number up to 77_8, cut the appropriate traces and reconnect the correct zeros and ones to the output pads.

3.1.7.3 Paper Tape Reader Speed Change. The XFD-108 optional ROM/IPL (Implemented Program Loader) is capable of controlling the PDP-8/E paper tape loader. It is normally set for a slow reader, but can be modified for a fast reader. This is done by cutting the PCB trace between E9-1 and ground as shown in Figure 3-6.

3.1.7.4 Sector Format Changes. The XFD-108 normally comes with a 12-bit word, and 10 sectors of 256 words each on 64 tracks. To change to allow 8 or 16 sectors, it is necessary to disconnect B6-1 from C7-11 and reconnect B6-1 to ground as shown in Figure 3-7. The connection of B6-1 must be consistent with connections on the formatter which control word size, sector size, and number of sectors (See Table 3-1). For proper connections and format options, see Section 3.1.8 below.

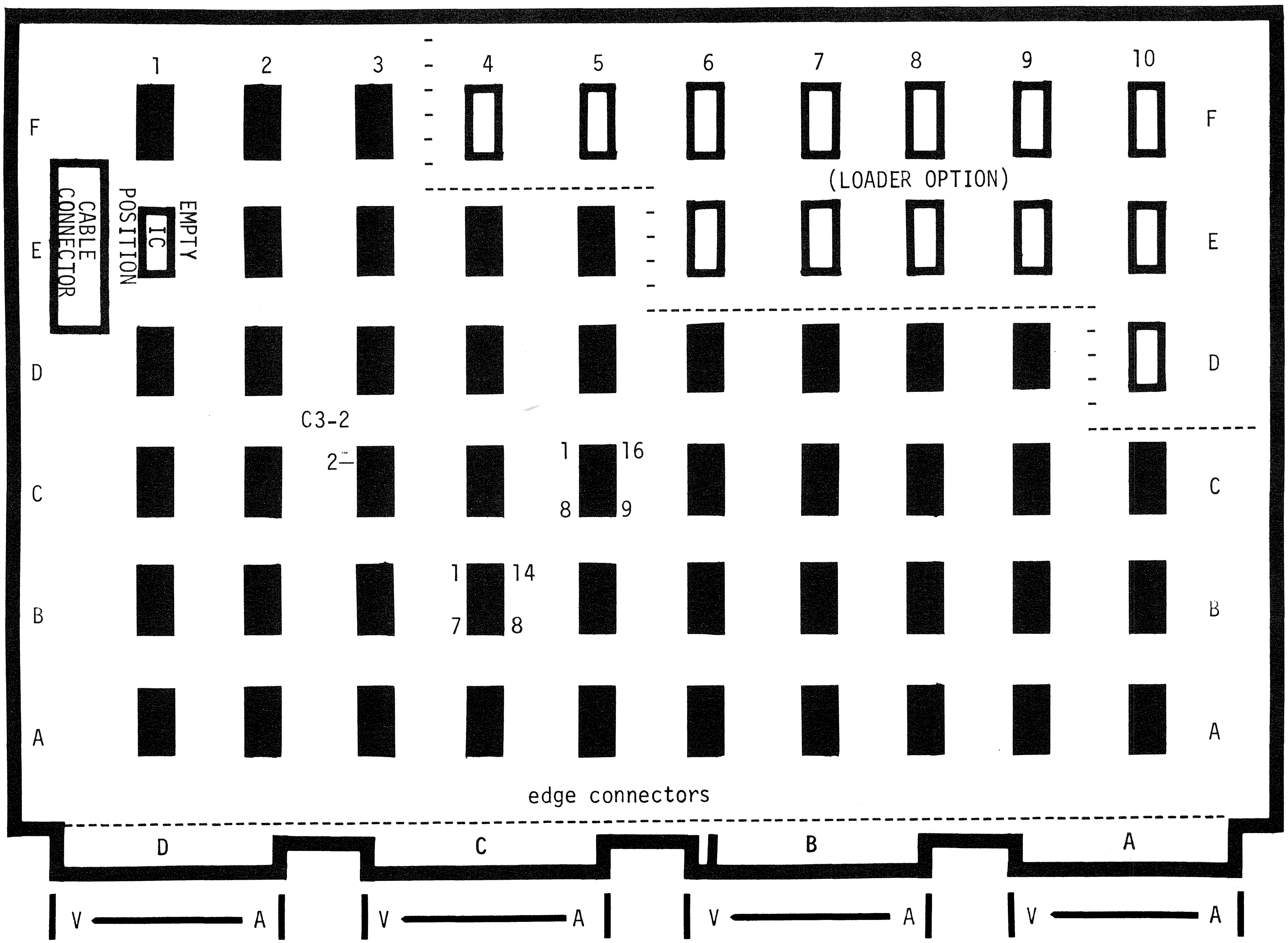


Figure 3-3. Front View of Coupler Board

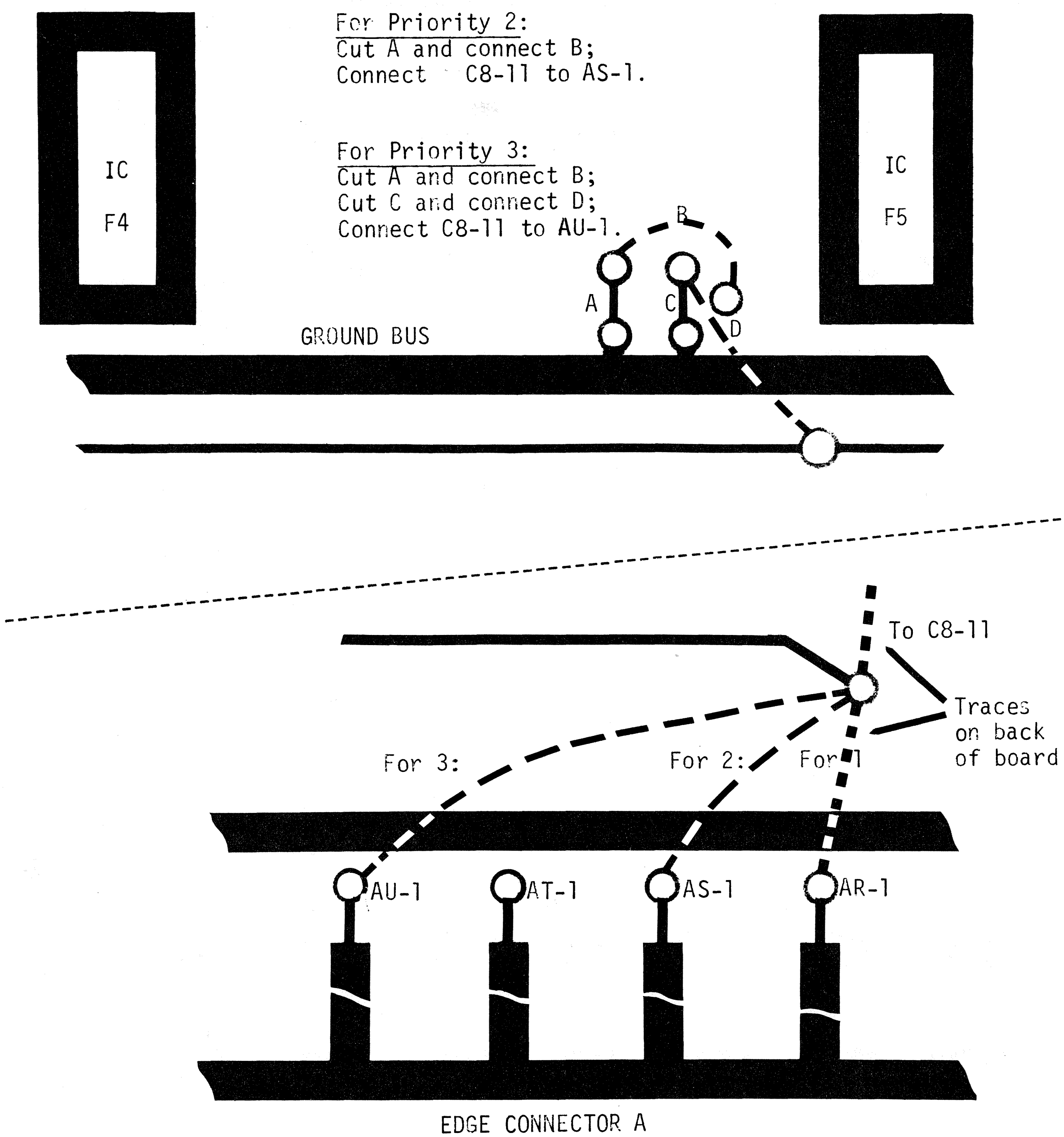


Figure 3-4. Wiring Changes for Device Priority

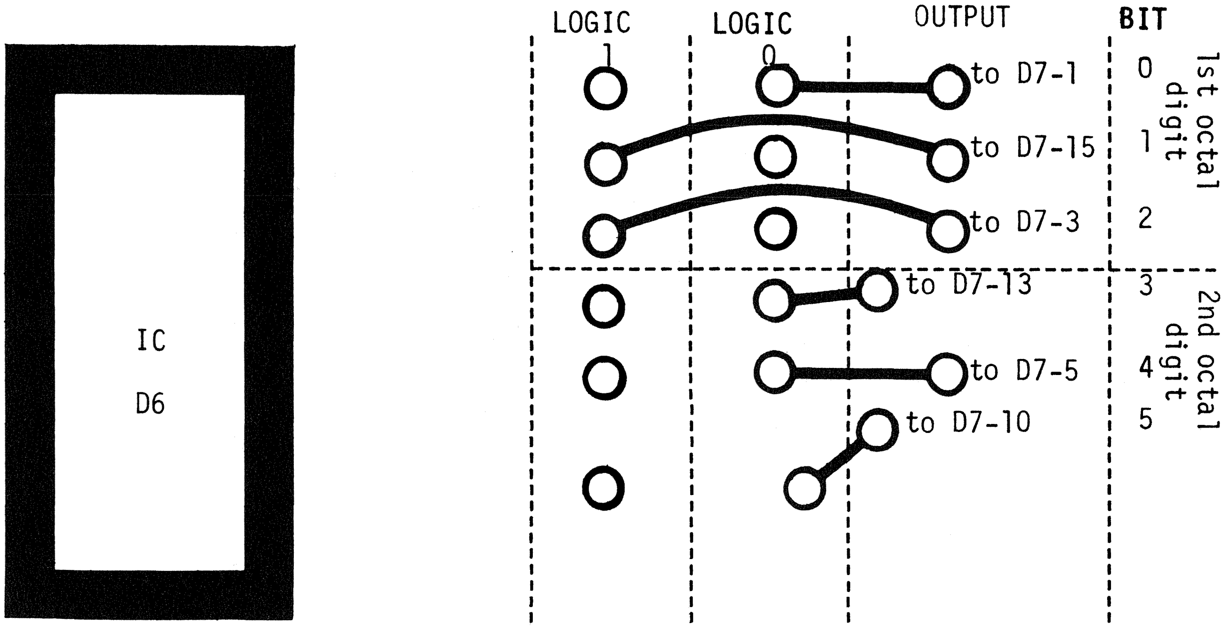


Figure 3-5. Wiring Changes for Device Address

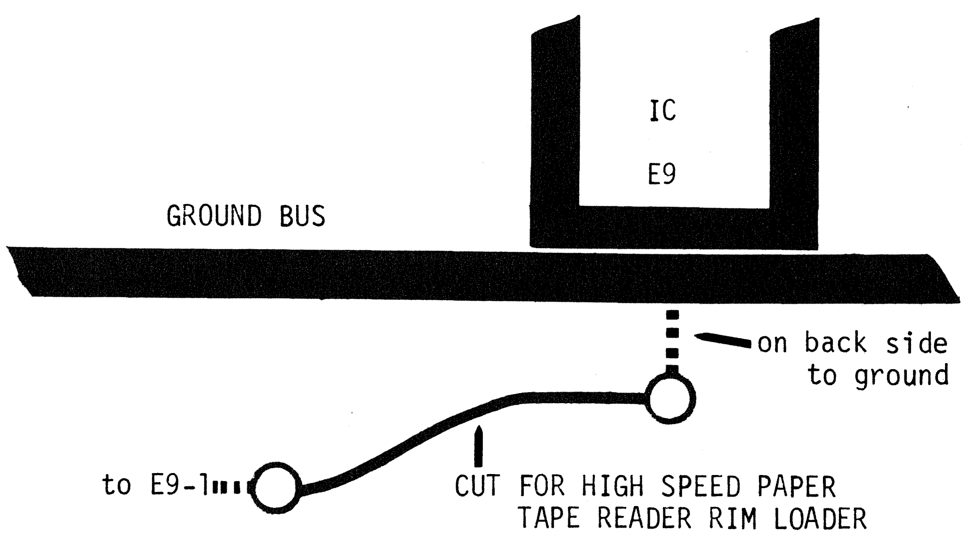


Figure 3-6. Wiring Change For High Speed Paper Tape Reader

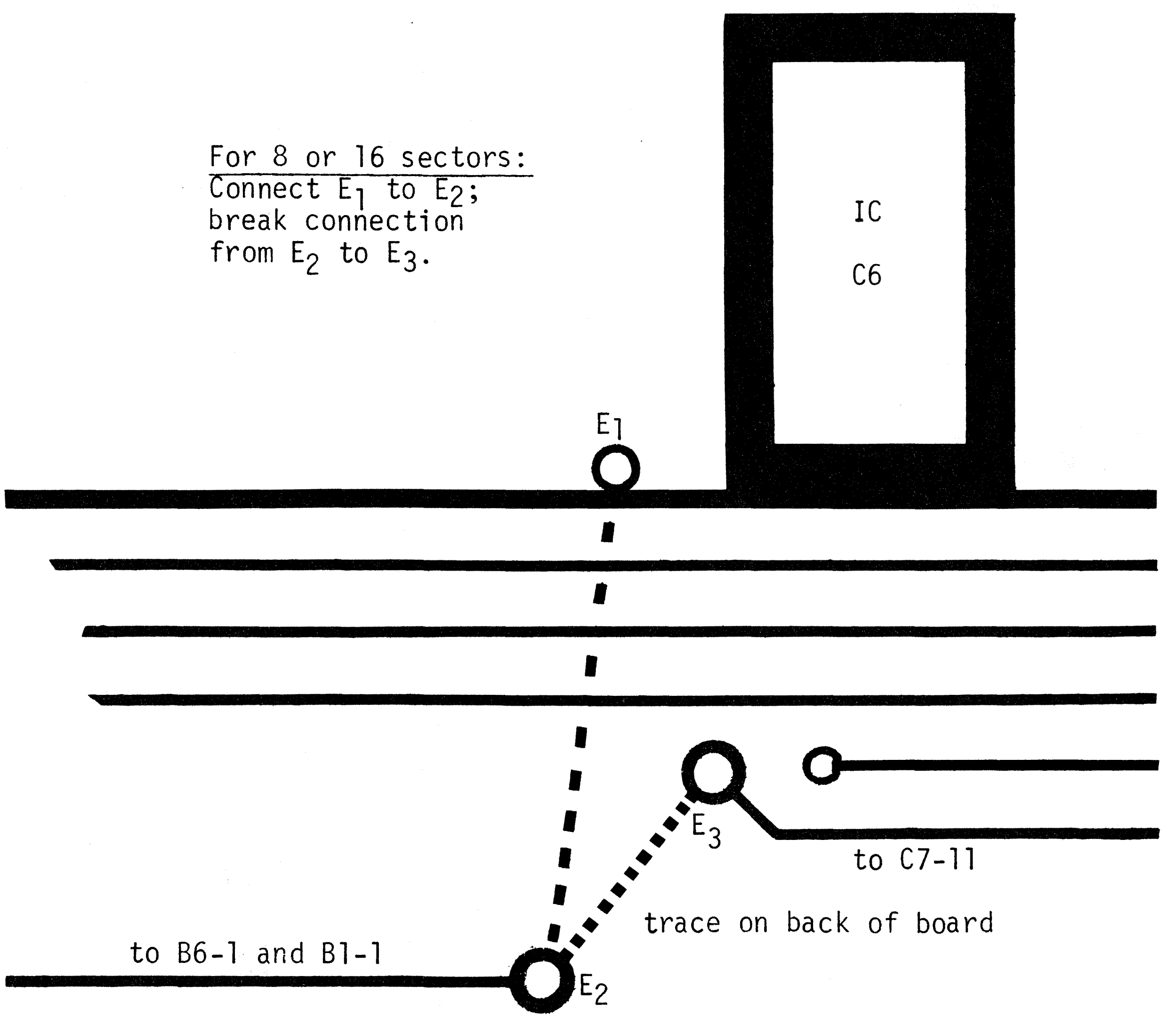


Figure 3-7. Sector Format Change on Coupler Card

3.1.8 Format Modifications

The XFD-108 is normally supplied with 12-bit words, 10 sectors, and 256 words/sector/track. These can all be changed by proper connection of four jumpers provided on the formatter PCB in the recorder chassis. The jumpers are:

Jumper	Pin
12-Bit	S/B K2-5
$\overline{OS}$	H3-12
16-Sector	H4-2
8-Bit	H4-1

These jumpers are activated when the pins are jumped to ground. Their effect on the format and word size is given in Table 3-1.

Table 3-1. Word and Sector Formats

Jumpers Activated	Word Size	Number of Sectors	Words/ Sector	Coupler Card Format Jumper
12 Bit	12 Bit	10	256	10 Sector
12 Bit • OS	12 Bit	8	320	8 or 16 Sector
12 Bit • OS • 16 Sect.	12 Bit	16	160	"
8 Bit*	8 Bit	16	256	"
16 Sect.*	16 Bit	16	128	"
No Jumpers*	16 Bit	8	256	"

* For computers other than PDP-8/E.

3.2 OPERATING INFORMATION

3.2.1 General

After the XFD-108 is installed, operation consists of loading the appropriate software, loading the disks, and turning ON the power to the chassis unit(s). Software instructions are included in Section 4; the operating information in this section covers disk loading instructions (Para. 3.2.2) and the control and indicator operating information (Table 3-2).

3.2.2 Disk Loading and Handling

3.2.2.1 General. Each flexible disk is enclosed in a plastic jacket. Wipe cushions are bonded to the inside of the jacket, so that the disk is housed and rotates between the cushions. To insert a disk in the recorder unit, open the door, slide the disk all the way into the guide. Do not close the door (See Figure 3-8). Turn the disk drive on (Depress RUN button) before closing the door. This ensures proper registration of the disk. When the disk is in place and the disk drive on, close the door slowly to engage the drive spindle.

3.2.2.2 Disk Interchangeability. To ensure interchangeability, store the disks in a location that is within ±5°F of the using system ambient temperature, and within ±10% of the using system humidity. Disks stored outside these ranges must be placed in the using system environment at least 20 minutes prior to use.

Table 3-2. XFD-108 Controls and Indicators

Control	Function
POWER	Alternate-action pushbutton switch and indicator lamp. Depress to turn ON chassis unit line power. When power is ON, indicator lamp and fan are both on. Depress again to turn line power OFF. NOTE: One switch per chassis assembly.
RUN*	Alternate-action pushbutton switch and indicator lamp. Depress to start the disk drive motor. When the motor is running, indicator lamp is ON. Depress again to stop the disk drive motor.
WRITE*	Indicator is ON when drive unit is writing (recording) data.
READ* (indicator)	Indicator is ON when the drive unit is reading data.

* Note that there is one set of controls for each disk drive unit, for a maximum of four per system, and two per chassis unit.

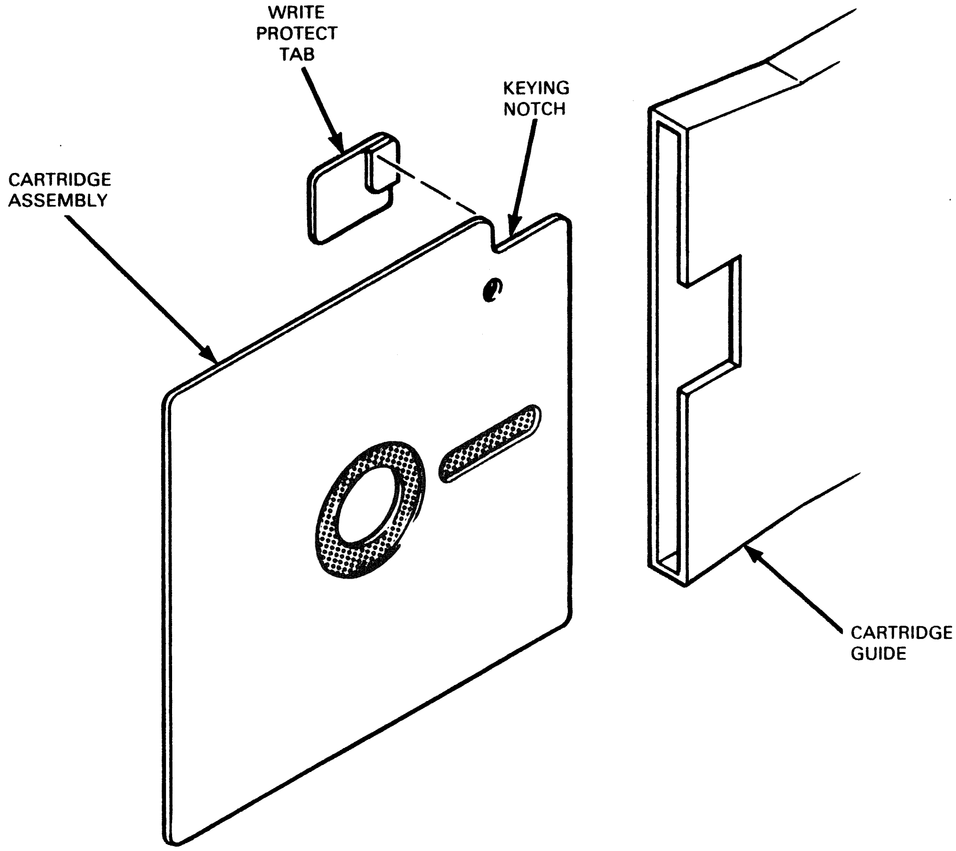


Figure 3-8. Insertion of Disk Cartridge in Guide

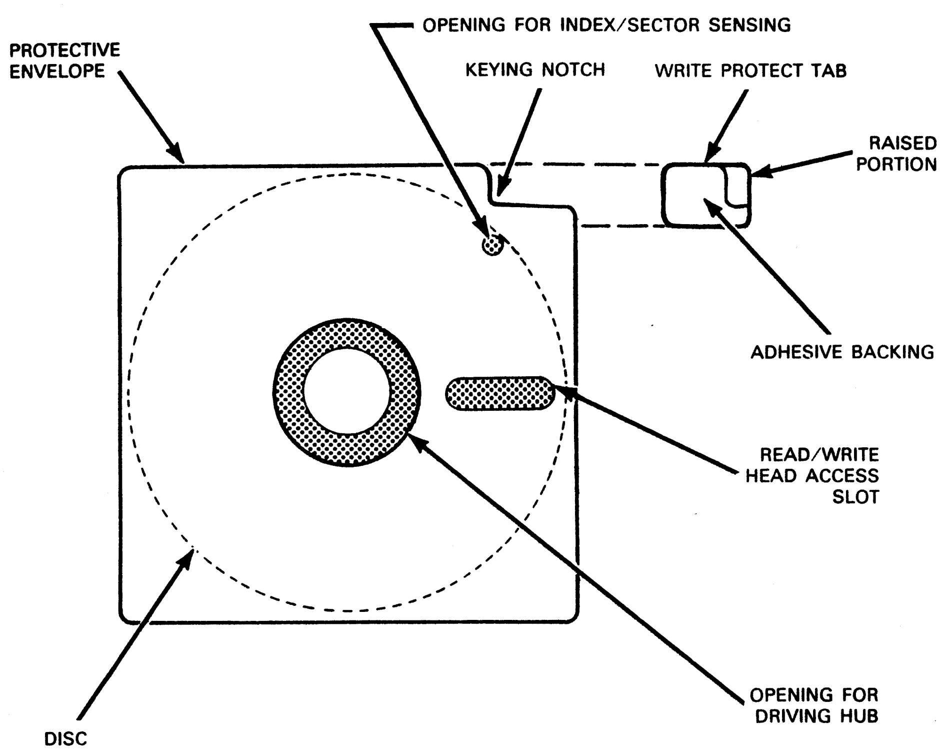


Figure 3-9. Write Protect Tab Insertion

3.2.2.3 Disk Precautions. After removing a disk from the recorder, it should be stored in a plastic-coated paper envelope. To protect the disk, use the same care and handling procedures specified for computer magnetic tapes. For best results, observe the precautions in Table 3-3 below.

Table 3-3. Disk Handling Precautions

1)	Return the disk to its storage envelope whenever it is removed from file.
2)	Store disks vertically.
3)	Keep disks away from magnetic fields and from ferromagnetic materials that might become magnetized. Magnetic fields greater than 50 Oersteds can distort recorded data on the disk.
4)	Replace storage envelopes when they become worn, cracked, or distorted.
5)	Do not write on the plastic cartridge. Writing pressure may damage the disk.
6)	Do not smoke while handling disks. Heat and contamination from a carelessly dropped ash can damage the disk.
7)	Do not expose disks to heat or sunlight. The recorder read/write head cannot properly track a warped disk.
8)	Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

3.2.2.4 Disk Write Protection. To inhibit writing on any disk, remove the covering on the plastic write-protect tab, and slide the tab into the keying notch of the vinyl envelope containing the disk (Figure 3-8). The tab is removable. With the tab in position, and the disk in the drive unit, the raised portion of the tab pushes an actuator that closes the write-protect switch, and the drive unit does not write. To restore the full read/write operation, remove the write protect tab from the disk.

3.2.3 System Start-up/Performance Test

3.2.3.1 General. Following installation and turn-on, the system should be given a thorough performance check. Use tests 1 through 17_8 of the Flexible Disk Diagnostic. Section 4 has a description of the diagnostic, and instructions for performing the diagnostic. The diagnostic will test and verify correct operation of the mechanical system, interconnections, and electronic system.

3.2.3.2. New Disk Initialization. Each time a new disk is used in the XFD-108 system, it must be formatted or initialized. Formatting consists of running diagnostic tests 1 through 3 before using the disk in the system. On disks that have been strongly degaussed, test 1 should be run three times before tests 2 and 3 are run, to ensure that that the disks are properly formatted. See Section 4 for the diagnostic procedure.

3.3 PACKING INSTRUCTIONS

If the XFD-100 is to be shipped by common carrier, use the original container and pack it according to the following procedure:

1) Remove the XFD-108 chassis unit(s) from the rack, and take off the chassis half of the slide rails prior to packing.

2) Wrap the XFD-108 in a plastic sheet to prevent scratching.

3) Place the XFD-108 chassis unit(s) in foam pads, as shown in Figure 3-9 and place the chassis and pads in the container. Note that there is a right-hand and a left-hand pad; the cutout goes to the bottom of the chassis unit.

4) Put manuals on the side next to the chassis unit. Wrap the rack-mount slides in cardboard and place them on top of the chassis unit.

5) Place the PC cards, cables, etc. in the cardboard box, and seal with tape. Place the box on top of the foam pads. Seal the box, even if it's empty, and place it on top of the chassis as filler for the shipping container.

6) Close the shipping container and seal it with glass-reinforced paper tape (See Figure 3-10).

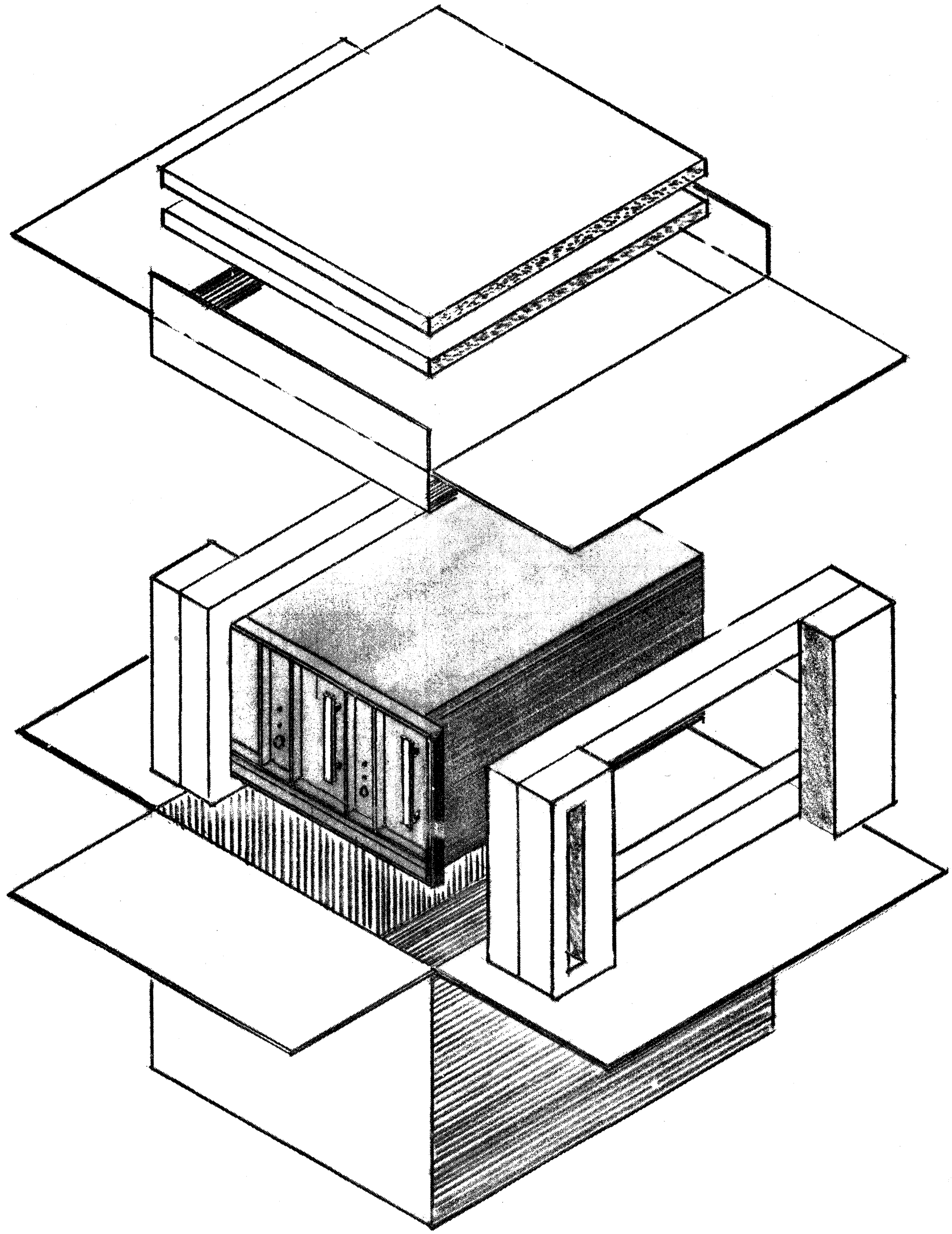


Figure 3-10
Packing Diagram

SECTION 4

SOFTWARE DATA

4.1 SCOPE

The following section describes the XFD-108 Input/Output instructions for users wishing to write their own drivers (including programming examples). Also included are descriptions of disk diagnostic programs and OS/8 Version 3 System and Non-System Handlers.

4.2 XFD-108 INPUT/OUTPUT INSTRUCTIONS

The detailed input/output machine instructions are included below for users desiring to write their own drivers. The standard device address (represented by XX below) assigned at the factory is 30_8. If desired, this address can be easily changed to any other 6-bit value by jumpers on the coupler card (reference Section 3.1.7.2 – Device Address Modification – for details).

4.2.1 Input/Output Instruction Summary

6XX0	SKNB	Skip if not busy.
6XX1	SKNI	Skip if not interrupting.
6XX2	SKNE	Skip if no error.
6XX3	LDMA	Load memory address.
6XX4	LDCM	Load command.
6XX5	LDDA	Load disk address.
6XX6	RDST	Read status.

The controller uses single-cycle data break for data transfer. The smallest addressable quantity on an XFD-108 disk is a <u>sector</u> (or <u>block</u>). For a system with n 12-bit words/sector, the sector format is given in Figure 4-1. Program-accessible areas of a sector are fully described in later sections.

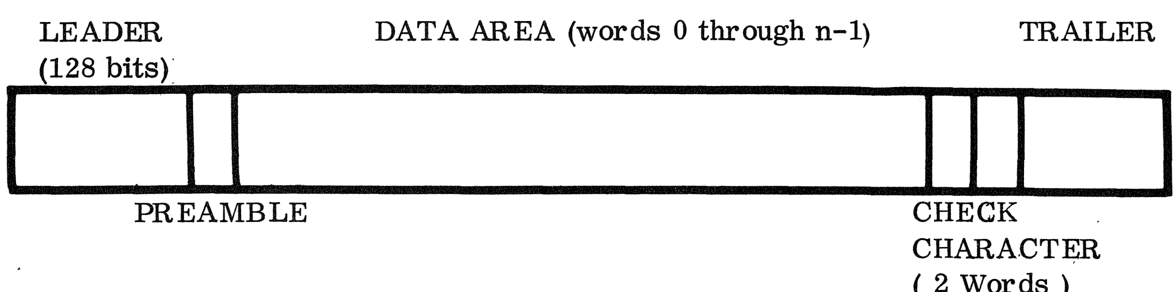


Figure 4-1. Sector Format

4.2.2 6XX3 – Load Memory Address

Loads the controller memory address register with the contents of the accumulator. This instruction must not be executed while BUSY is set. The contents of the accumulator are treated as shown in Figure 4-2.

	MEMORY ADDRESS (MA)											
AC	0	1	2	3	4	5	6	7	8	9	10	11

Figure 4-2. Memory Address

The value MA specifies the starting address of a buffer in the computer memory to be used by the controller during a WRITE or READ operation. After the operation is initiated, MA is incremented by the controller as successive words are transferred to or from memory.

NOTE: The memory address register is set to zero when the CLEAR switch is depressed.

4.2.3 6XX4 – Load Command Word

This instruction loads the controller command register with the contents of the accumulator, clears certain controller status flags, sets BUSY (reference Section 4.2.6 for details), and then initiates the operation specified by the command code. When the operation is completed, BUSY is cleared and if interrupts are enabled, an interrupt is generated. This instruction must not be executed while BUSY is set. The contents of the accumulator are treated as shown in Figure 4-3.

			I		C	R	MF			S/H	OP	
AC										0/1		
	0	1	2	3	4	5	6	7	8	9	10	11

Figure 4-3. Command Word

Bits 10-11:	Operation Code (OP)	Operation
	0	Read
	1	Write
	2	Check
	3	Seek/No-Op

Bit 9: Sector/half-sector transfer (S/H)

0 = One sector of data
1 = Half sector of data

Bits 6-8: Memory field select (MF)

Bit 5: Restore to track 0 (R)

Bit 4: Read/write (C) CRC

Bit 2: Interrupt Enable/Disable (I)

0 = Disable disk interrupts
1 = Enable disk interrupts

Each of the fields is described in detail on the following pages.

4.2.3.1 Read Operation (OP = 0). Causes the controller to input data from the selected unit directly to computer memory. Either one sector (S/H = 0) or one half-sector (S/H = 1) of data is read from the sector specified by the Disk Address word into a buffer beginning at MA in the memory field MF. Data words from the specified sector are input to consecutive memory locations beginning at the initial values of MA and MF.

When the command word is loaded, BUSY is set, a seek to the track given in the Disk Address word is initiated, and the SEEK indicator of the Status Word is set until the seek is completed. If the R (Restore) bit is set, the Read/Write head on the specified unit is first restored to track 0. The seek to the selected track is then initiated. In either case the seek bit remains set until head motion stops.

During each read operation, the sector preamble is automatically hardware-compared and the CRC is calculated over each data word in the sector (regardless of how many words are transferred). The CRC is then hardware-compared against the CRC generated during the last write operation on the sector.

BUSY is set when the operation is initiated and reset after all the words specified by the S/H bit have been transferred (and the CRC has been compared). If the I (Interrupt enable) bit has been set in the command word, an interrupt is generated at the time that BUSY is reset (See Section 4.2.3.7 for effect of setting the Read/Write CRC bit during a read operation).

4.2.3.2 Write Operation (OP = 1). Causes the controller to output data from computer memory to the selected unit. Either one sector (S/H = 0) or one-half sector (S/H = 1) of data is written from a buffer beginning at MA in memory field MF to the sector specified by the Disk Address word. Data words are output to the specified sector from consecutive memory locations beginning at the initial values of MA and MF.

When the command word is loaded BUSY is set, a seek to the track given in the Disk Address word is initiated and the SEEK indicator of the Status Word is set until the seek is completed. If the R (Restore) bit is set the Read/Write head on the specified unit is first restored to track 0. The seek to the selected track is then initiated. In either case the SEEK bit remains set until head motion stops.

During each Write operation the sector preamble is automatically rewritten by the controller and the CRC is calculated over each data word of the sector (regardless of how many words are transferred). If a half-sector of data is written the remainder of the sector is automatically "padded" with zeros and the CRC is still calculated over each word of the sector.

BUSY is set when the operation is initiated and reset after all the words specified by the S/H bit have been transferred (and the check character has been generated). If the I (Interrupt enable) bit has been set in the command word, an interrupt is generated at the time that BUSY is reset.

If the Read/Write CRC bit (bit 4) is set, the CRC is written from two additional words in the memory buffer (reference Section 4.2.3.7).

4.2.3.3 Check Operation (OP = 2). Causes the controller to compare the preamble and CRC words on a given sector without transferring data. The sector checked is given by the Disk Address word.

When the command word is loaded BUSY is set, a seek to the track given in the Disk Address word is initiated and the SEEK indicator of the Status Word is set until the seek is completed. If the R (Restore) bit is set the Read/Write head on the specified unit is first restored to track 0. The seek to the selected track is then initiated. In either case the SEEK bit remains set until head motion stops.

During each check operation the sector preamble is automatically hardware-compared and the CRC is calculated over each data word in the sector. The CRC is then hardware-compared against the CRC generated during the last Write operation on the sector. A full sector is always checked independent of the S/H bit.

BUSY is set when the operation is initiated and reset after the sector has been checked. If the I (Interrupt enable) bit has been set in the command word an interrupt is generated at the time that BUSY is reset.

4.2.3.4 Seek/No-Op (Op = 3). Causes the controller to select the unit given in the Disk Address word and to position that unit to the track given in the Disk Address Word.

When the command word is loaded a seek to the track given in the Disk Address word is initiated and the SEEK indicator of the Status Word is set until the seek is completed. If the R(Restore) bit is set the Read/Write head on the specified unit is first restored to track 0. The seek to the specified track is then initiated. In either case the SEEK bit remains set until head motion stops.

BUSY is not affected by the SEEK/NO-OP operation. No checking is done of either preamble or CRC words, no data is transferred, and no preamble is written.

This operation is used primarily as a unit select operation and to effect restore.

4.2.3.5 Sector/Half-Sector Transfer (Bit 9). If this bit is set for a READ or WRITE operation a half sector of data is transferred as follows:

WRITE: A half-sector of data is transferred starting at MA and the remainder of the sector is zeroed ("padded with zeros").

READ: A half-sector is read into a buffer starting at MA.

Sector word count can be determined from the following table:

Sector/Track	Words/Sector	Words/Half-Sector
16	128	64
16	160	64
10	256	128
8	256	128
8	320	128

Half-sector operations are incompatible with reading or writing the check character and should not be attempted (reference Section 4.2.3.7).

4.2.3.6 RESTORE (Bit 5). If RESTORE is set, the selected unit automatically seeks to the home position. Any additional seeking (as specified in the Disk Address Word) is then performed.

BUSY is set if the rest of the command word requires it; otherwise it is unaffected.

4.2.3.7 READ/WRITE CRC (Bit 4). If this bit is set when a WRITE operation is requested (OP = 1), two more words containing the CRC are written at the end of a sector. If there are n words per sector (i.e., words 0 through n-1), then words n and n + 1 of the memory buffer should contain the 16-bit CRC as shown in Figure 4-4. If this bit is set when a READ operation is requested (OP = 0) the two words containing the CRC are transferred into memory after the data words of the sector.

Reading or writing the CRC is incompatible with half-sector operations and should not be attempted.

Word n	High-Order 12 Bits of Check Character
Word n + 1	Low Order (bits 0 1 2 3)

Figure 4-4. CRC Format

4.2.3.8 Interrupt Enable/Disable (Bit 2). If this bit is set and the operation sets BUSY then an interrupt is generated at the time that BUSY is reset (i.e., at completion or error). Note that this means that a Seek/No-Op does not generate an interrupt.

The computer does not detect the interrupt, of course, unless system interrupts are enabled with a 6001 (ION).

See Section 4.4 for an example of programming under interrupt control.

4.2.4 6XX5 – LOAD DISK ADDRESS

Loads the Disk Address register of the controller uniquely specifying a disk sector by its unit and block address (See Figure 4-5).

	UNIT (UN)	BLOCK ADDRESS
AC	0 1	2 3 4 5 6 7 8 9 10 11

Figure 4-5. Disk Address Format

Bits 2-11 BLOCK ADDRESS

Sectors may be thought of as arranged sequentially from Block 0 to Block (Max).

Sectors/Track$_{10}$	Block (Max)$_{10}$
16	1024
10	640
8	512

For 8 and 16 sector systems the block address-to track/sector address correspondence is given in Figure 4-6.

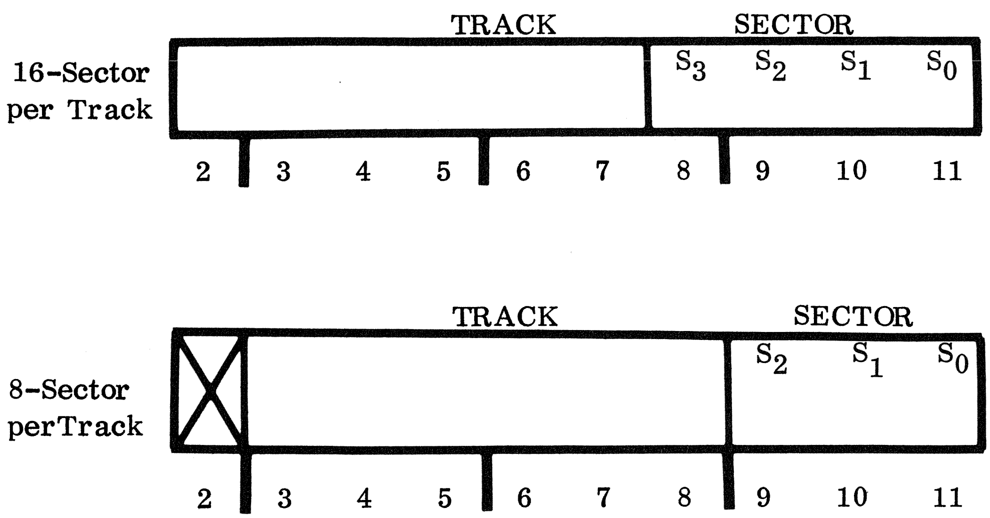


Figure 4-6. Disk Address Formats for 8 and 16 Sector Systems

Although the correspondence is different for the 10-sector/track system the sectors are still sequentially addressed.

Bits 0-1	Unit Select	Unit
	00	Unit 0
	01	Unit 1
	10	Unit 2
	11	Unit 3

The value of UN selects the disk unit on which the requested command code is to be performed. The correlation between unit address and the physical disk unit is shown in Figure 4-7.

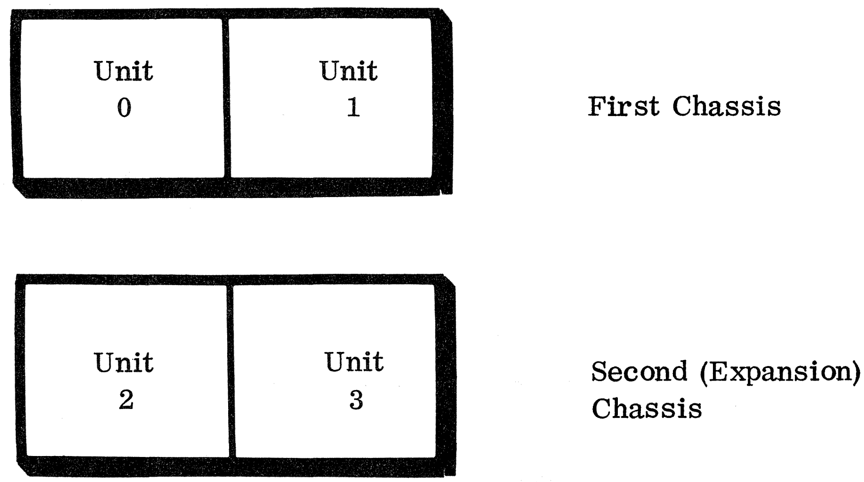


Figure 4-7. Disk Unit Address

4.2.5 6XX6 – READ Status

Loads the accumulator with the contents of the controller status register. This instruction should not be executed when BUSY is set. Status is for the unit currently selected. (See Figure 4-8.)

	0	1	2	3	4	5	6	7	8	9	10	11
	NOT USED				NRDY	TMO	WPE	FMTE	RATE	PCE	CKCE	SEEK
AC	0	0	0	0								

Figure 4-8. Status Word

Bits 0-3:	Not used: Set to 0		
Bit 4:	200_8	NRDY	Not Ready
Bit 5:	100_8	TMO	Time Out Error
Bit 6:	40_8	WPE	Write Protect Error
Bit 7:	20_8	FMTE	Format Error
Bit 8:	10_8	RATE	Rate Error
Bit 9:	4	PCE	Preamble Compare Error
Bit 10:	2	CRCE	CRC Error
Bit 11:	1	SEEK	Unit Seeking

4.2.5.1 Errors Always Indicating Premature Termination of an Operation:

1) NRDY – (200_8) – Not Ready

   The specified unit is not plugged in, the unit is not up to speed, or a disk is not in place.

2) TMO – (100_8) – Time Out Error

   The last operation was not completed because the sector address specified was not found within 2.5 seconds. This can be caused by specifying a non-existent sector address or by a hardware malfunction.

3) WPE – (40_8) – Write Protect Error

   The WRITE operation was terminated because the disk in the specified unit is physically write protected or certain fault indicators have been detected within the drive itself.

4) FMTE – (20_8) – Format Error

   During WRITE, READ, or CHECK operation an end of sector was detected before the specified operation was completed. Error may occur if pack was formatted with wrong number of sectors for the the controller type.

5) RATE – (10_8) – Rate Error

   During the last data transfer operation data was improperly transferred. A word of data was not transferred at the time it was required. BUSY is immediately reset at the time this error occurs.

6) PCE – (4) – Preamble Compare Error

During the last READ or CHECK operation the sector preamble at the beginning of the sector was not what it should have been. No data transfer occurs.

4.2.5.2 Status Indicators Reported After Operation is Completed

1) CRCE– (2) – CRC Compare Error

The CRC calculated during the last READ or CHECK operation did not match the one previously written on the sector.

2) SEEK – (1)– Unit Seeking

The unit currently selected is seeking or restoring. If BUSY is reset this indicator is considered an error unless the last operation was a SEEK/NO-OP. = .

4.2.6 6XX0 – Skip if not Busy

If BUSY is zero skip the next instruction, otherwise do not skip. This instruction may be executed at any time. BUSY (a formatter flag) is set only when a READ, WRITE, or CHECK operation is being performed; BUSY is reset when the operation is complete or when an error condition is detected. BUSY is also reset when the CLEAR switch is depressed.

4.2.7 6XX1 – Skip if not Interrupting

Skips the next instruction if the controller is not interrupting. If the controller is interrupting no skip occurs but the interrupt is cleared and disk interrupts are disabled. The interrupt occurs when BUSY is reset (after having been set by loading the command word) and disk interrupts are enabled. The skip occurs then if either BUSY is set or disk interrupts are disabled (I = 0 in command word).

NOTE: Executing this instruction is the only way to disable/clear interrupts other than issuing I = 0 in a load command instruction (6XX4) or depressing the CLEAR switch.

4.2.8 6XX2 – Skip if no Error

Skips the next instruction if no error condition is detected. The "error" condition is detected whenever any of the status indicators, except for the SEEK indicator, is set. That is, "error" is the inclusive OR of status bits 4-10 of the Status Word – NRDY, TMO, WPE, FMTE, RATE, PCE, or CRCE.

4.3 BOOTSTRAPPING FROM THE XFD-108

4.3.1 Hardware Bootstrap Options

A variety of hardware options may be included in the XFD-108 coupler including a choice of two types of disk bootstrap and a choice of high or low speed paper tape (RIM) bootstraps.

4.3.1.1 Implemented Program Load (IPL). The IPL option, if included, allows the user to bootstrap from the XFD-108 and begin execution of a program by means of an external switch. The format of the bootstrap block read into core is given in Section 4.3.1.2 under the description of the XFD/ROM bootstrap option. IPL is intended for use with a PDP-8/E family computer with no front panel and does not operate if a front panel is present unless SW is up.

4.3.1.2 ROM Bootstrap Option (XFD/ROM). The XFD/ROM option is intended for use with a PDP-8/E family computer with a front panel with an SW switch. If included, it allows the user to move one bootstrap block from the XFD-108 to memory and begin execution of the data in this block.

The XFD/ROM when executed moves one sector (block) of data from Block 0 (sector 0 of track 0 of unit 0) of the XFD-108 to memory locations 0 through (sector size-1) of memory field 0. When the transfer is complete a jump to location 1 occurs and program execution begins at that location. Therefore the bootstrap block must be written on Block 0 in such a way that the first executable instruction will be read into location 1 (the second word of the block). The foregoing description also applies to the IPL option.

To execute the XFD/ROM bootstrap:

Halt the computer.
Set the SW switch UP.
LOAD ADDRESS 7740_8.
Depress CLEAR.
Depress CONTINUE (or START).
Set the SW switch DOWN.

4.3.1.3 Paper Tape Bootstrap Options (RIM/ROM). If the XFD/ROM bootstrap option is included, the user has a choice of hardware-implemented RIM bootstraps. Only one of the high speed or low speed RIM loaders may be implemented at any time; the choice is made by a single jumper on the coupler card.

To execute the RIM/ROM bootstrap:

Halt the computer; insert the Binary Loader tape in the appropriate tape reader.
Set the SW switch UP.
LOAD ADDRESS 7756_8.
LOAD MEMORY FIELD as desired.
Depress CLEAR.
Depress CONTINUE (or START).
Set the HALT switch DOWN to half RIM loader.
Set the SW switch DOWN.

4.3.2 Key-in Bootstrap

If the XFD/ROM (and RIM/ROM) bootstrap is unavailable, the following bootstrap may be keyed into memory from the front panel Switch Register:

Location	Contents
XX00	6305
XX01	6304
XX02	6300
XX03	5202
XX04	5001

Begin execution at location XX00. The key-in simulates the action of the IPL and XFD/ROM bootstrap options with the exception of Memory Field Selection. Note that depressing CLEAR when beginning execution both clears the Memory Address register and the accumulator, setting up the proper Memory/Disk addresses.

4.3.3 OS/8 Key-in Bootstrap

If the Xebec Systems version of OS/8 is resident on an XFD-108 disk (as systems device) the following abbreviated bootstrap is useful:

Location	Contents
20	6305
21	6304
22	5022

LOAD ADDRESS 20, LOAD MEMORY FIELD 0, depress CLEAR and CONTINUE. OS/8 will be bootstrapped into memory and respond in the usual way with a dot (.) at the left-hand margin of the keyboard console.

```
              /   PROGRAMMING EXAMPLE 1

              /
              /   THIS PROGRAM COPIES EACH SECTOR OF THE
              /   DISK IN UNIT 0 TO THE CORRESPONDING SECTOR
              /   OF UNIT 1.  TRANSFERS ARE DONE WITHOUT INTERRUPTS.
              /   FULL SECTOR TRANSFERS ARE DONE IN EACH CASE,
              /   AND IT IS ASSUMED THAT A 10-SECTOR/REVOLUTION
              /   DRIVE IS USED(THUS THERE ARE 640 BLOCKS
              /   TO TRANSFER.).

              /
       6300            SKNB=6300       /SKIP ON NOT BUSY
       6302            SKNE=6302       /SKIP ON NO ERROR
       6303            LDMA=6303       /LOAD MEMORY ADDRESS
       6304            LDCM=6304       /LOAD COMMAND
       6305            LDDA=6305       /LOAD DISK ADDRESS
       6306            RDST=6306       /READ STATUS

       0200            *200
00200  7200   INITL,   CLA
00201  1247            TAD BLKLM       /SET UP BLOCK
00202  3250            DCA BLKCT       /--COUNTER
00203  3251            DCA BLOCK       /ZERO BLOCK #
00204  4221   RESTR,   JMS DRIVER      /RESTORE ON
00205  0103            0103            /--UNIT 0
00206  4221            JMS DRIVER      /RESTORE ON
00207  2103            2103            /--UNIT 1
00210  7200   START,   CLA
00211  4221            JMS DRIVER      /READ BLOCK
00212  0000            0000            /--FROM UNIT 0
00213  4221            JMS DRIVER      /WRITE BLOCK
00214  2001            2001            /--TO UNIT 1
00215  2251            ISZ BLOCK       /BUMP BLOCK #
00216  2250            ISZ BLKCT       /MORE TO DO?
00217  5210            JMP START       /--YES: LOOP
00220  7402            HLT             /--NO: HALT
```

```
             /
             /  XFD-108 DRIVER
             /
00221  0000  DRIVER, 0
00222  7200          CLA
00223  1621          TAD I DRIVER     /MASK UNIT #,
00224  0253          AND UNMSK        /--ADD TO BLOCK #
00225  1251          TAD BLOCK        /--TO CREATE DISK ADDRESS
00226  6305          LDDA             /LOAD DISK ADDRESS

00227  7200          CLA
00230  1252          TAD MEMAD        /LOAD
00231  6303          LDMA             /--MEMORY ADDRESS

00232  7200          CLA
00233  1621          TAD I DRIVER     /MASK OP AND
00234  0254          AND OPMSK        /--RESTORE BITS
00235  6304          LDCM             /LOAD COMMAND

00236  6300          SKNB             /DISK BUSY?
00237  5236          JMP .-1          /--YES:  WAIT
00240  6302          SKNE             /--NO: ANY ERROR?
00241  5244          JMP ERROR        /---YES: GO READ STATUS
00242  2221          ISZ DRIVER       /---NO: EXIT DRIVER
00243  5621          JMP I DRIVER

00244  6306  ERROR,  RDST             /READ STATUS
00245  7402          HLT              /--AND HALT
00246  5204          JMP RESTR        /RESTORE BOTH UNITS
                                      /--AND RETRY

00247  6600  BLKLM,  -1200
00250  0000  BLKCT,  0
00251  0000  BLOCK,  0
00252  0400  MEMAD,  400
00253  6000  UNMSK,  6000
00254  0777  OPMSK,  777
             /
             $$$$
```

```
                / PROGRAMMING EXAMPLE 2

                /
                / THIS PROGRAM COPIES EACH SECTOR OF THE
                / DISK IN UNIT 0 TO THE CORRESPONDING SECTOR
                / OF UNIT 1.  TRANSFERS ARE DONE UNDER INTERRUPTS.
                / FULL SECTOR TRANSFERS ARE DONE IN EACH CASE,
                / AND IT IS ASSUMED THAT A 10-SECTOR/REVOLUTION
                / DRIVE IS USED(THUS THERE ARE 640 BLOCKS
                / TO TRANSFER.).

                /
       6300             SKNB=6300       /SKIP ON NOT BUSY
       6301             SKNI=6301       /SKIP IF NOT INTERRUPTING
       6302             SKNE=6302       /SKIP ON NO ERROR
       6303             LDMA=6303       /LOAD MEMORY ADDRESS
       6304             LDCM=6304       /LOAD COMMAND
       6305             LDDA=6305       /LOAD DISK ADDRESS
       6306             RDST=6306       /READ STATUS

       0001             *1
00001  5402             JMP I 2
00002  0263             INTRPT

       0200             *200
00200  7200     INITL,  CLA
00201  1276             TAD BLKLM       /SET UP BLOCK
00202  3277             DCA BLKCT       /--COUNTER
00203  3300             DCA BLOCK       /ZERO BLOCK #
00204  3305             DCA INTFL       /ZERO INTERRUPT FLAG
00205  4232     RESTR,  JMS DRIVER      /RESTORE ON
00206  0103             0103            /--UNIT 0
00207  4232             JMS DRIVER      /RESTORE ON
00210  2103             2103            /--UNIT 1
00211  7200     START,  CLA
00212  4232             JMS DRIVER      /READ BLOCK
00213  1000             1000            /--FROM UNIT 0
00214  4224             JMS WAITI       /WAIT FOR INTERRUPT
00215  4232             JMS DRIVER      /WRITE BLOCK
00216  3001             3001            /--TO UNIT 1
00217  4224             JMS WAITI       /WAIT FOR INTERRUPT
00220  2300             ISZ BLOCK       /BUMP BLOCK #
00221  2277             ISZ BLKCT       /MORE TO DO?
00222  5211             JMP START       /--YES: LOOP
00223  7402             HLT             /--NO: HALT
                /
                / WAIT FOR INTERRUPT
                /
00224  0000     WAITI,  0
00225  7200             CLA
00226  1305     WAITL,  TAD INTFL
00227  7640             SZA CLA         /HAS INTERRUPT COME?
00230  5226             JMP WAITL       /--NO: WAIT
00231  5624             JMP I WAITI     /--YES
                /
```

```
              /
              /  XFD-108 DRIVER
              /
00232  0000  DRIVER, 0
00233  7200          CLA
00234  1632          TAD I DRIVER     /MASK UNIT #,
00235  0302          AND UNMSK        /--ADD TO BLOCK #
00236  1300          TAD BLOCK        /--TO CREATE DISK ADDRESS
00237  6305          LDDA             /LOAD DISK ADDRESS
00240  7200          CLA
00241  1301          TAD MEMAD        /LOAD
00242  6303          LDMA             /--MEMORY ADDRESS
00243  7200          CLA
00244  1632          TAD I DRIVER     /MASK OP AND
00245  0303          AND OPMSK        /--RESTORE BITS
00246  6304          LDCM             /LOAD COMMAND
00247  7200          CLA
00250  1632          TAD I DRIVER     /WAS INTERRUPT
00251  2232          ISZ DRIVER       /--REQUESTED?
00252  0304          AND INMSK
00253  7450          SNA
00254  5260          JMP DRIVA        /--NO: JUST RESTORE
00255  3305          DCA INTFL        /--YES: TURN ON
                                      /----INTERRUPT FLAG
00256  6001          6001             /ENABLE SYSTEM INTS.
00257  5632          JMP I DRIVER     /EXIT DRIVER
00260  6302  DRIVA,  SKNE             /IS UNIT SEEKING?
00261  5260          JMP .-1          /--YES: WAIT
00262  5632          JMP I DRIVER     /--NO: EXIT DRIVER
              /
              /  INTERRRUPT PROCESSOR
              /
00263  6002  INTRPT, 6002             /DISABLE SYSTEM INTS.
00264  7200          CLA
00265  3305          DCA INTFL        /ZERO INTERRUPT FLAG
00266  6301          SKNI             /WAS IT DISK?
00267  5273          JMP ERROR        /--NO: ERROR
00270  6302          SKNE             /ANY ERROR?
00271  5273          JMP ERROR        /--YES:
00272  5400          JMP I 0          /RETURN FROM INTERRUPT

00273  6306  ERROR,  RDST             /READ STATUS
00274  7402          HLT              /--AND HALT
00275  5205          JMP RESTR        /RESTORE BOTH UNITS
                                      /--AND RETRY
00276  6600  BLKLM,  -1200
00277  0000  BLKCT,  0
00300  0000  BLOCK,  0
00301  0400  MEMAD,  400
00302  6000  UNMSK,  6000
00303  1777  OPMSK,  1777
00304  1000  INMSK,  1000
00305  0000  INTFL,  0
             $$$$
```

4.5 FLEXIBLE DISK DIAGNOSTIC PROGRAMS

4.5.1 Program Description

The disk diagnostic program enables the user to 1) exercise all positioning and data transfer functions provided by the controller, 2) check all status and error flags returned by the controller, 3) verify proper operation of all units connected to the controller and 4) check that part of the computer interrupt system used by the controller. Some of the tests included in the diagnostic are designed to isolate errors which depend on the data content or mode of a data transfer. Another set of tests are devoted to forcing error conditions and checking to see that they are properly reported by the controller. Tests are also provided to check for proper sector formatting and unit-to-unit compatibility.

Error reporting is accomplished via the console teletype. In general, errors are reported when either status information or data input from the controller differs from that expected by the program. The operator has the ability to inhibit error message outputs as required. In addition, the operator specifies the order in which tests are performed and the sequence in which certain tests select units.

The program operates in a minimum memory configuration of 4K but will automatically utilize extra memory to test data break/memory field addressing. The upper 200_8 words of memory are reserved by the program for loaders and are not overwritten.

4.5.2 Operating Instructions

The diagnostic executes in a sequence of well defined steps that are described below. All communications between the operator and the program are via the console teletype and, in some cases, the computer switch register. All replies to specific input requests are entered from the keyboard and are terminated by the RETURN key. The program ignores any characters other than the 64 printing characters (including space), RUBOUT, RETURN, and the "break" characters Control-F, Control-P, Control-E, Control-T, and Control-N.

Three of the recognized keyboard characters are input line-editing characters that may be used by the operator to correct errors made while typing. The editing characters function as follows:

RUBOUT	Deletes one character to the left for each input and echoes back as \.
@	Deletes the entire input line to the left and echoes back as @.

The break characters are used to alter the execution sequence of the diagnostic as follows:

Control-F	Echoes back as ↑F and then returns the program to the FMPR request (Step 3 below).
Control-P	Echoes back as ↑P and then returns the program to the PACK request (Step 4 below).
Control-E	Echoes back as ↑E and then returns the program to the EMSK request (Step 5 below).
Control-T	Echoes back as ↑T and then returns the program to the TEST request (Step 6 below).
Control-N	Echoes back as ↑N, stops execution of the test in progress, and then starts execution of the next test in the sequence specified by the last TEST request.

Not all of the break characters are recognized at each step in the program's execution sequence; therefore, those break characters that are recognized are specifically indicated in the steps described below.

All numeric values input to or output from the program, unless otherwise specified, are in octal. If more than 4 digits are input for a numeric value then the program will recognize only the low ordered 12 binary bits of the value specified.

If any operator reply to an input request cannot be recognized by the program or is outside of the allowed set of values, then the program will output the error message ? ? and repeat the request. Similarly, for input requests in which the operator may input a variable number of parameters the program will output the error message:

? ?

and repeat the request if the number of parameters exceeds the maximum allowed.

In the steps below the symbols { and } are used to enclose operator inputs that are optional. Examples that are given use underlining to indicate operator inputs and the ↲ symbol to indicate a RETURN

1) Make sure the console teletype is on in the LINE position and that each disk drive to be tested is loaded with a disk pack. Load the diagnostic using the DEC PDP-8 Binary Loader. The user may start the program at memory location 00200.

2) The program then types out the size and locations of the I/O buffers as:

   WBUF = a
   RBUF = b
   BUFL = c
   LAST MEM. FIELD = d

where a is the starting address of the write buffer, b is the starting address of the read buffer, c is the buffer length, and d is the number of the last memory field available to the program. Following this step the program enters its normal execution sequence.

Example:

WBUF = 5301
RBUF = 6321
BUFL = 1020
LAST MEM. FIELD = 1

The write buffer starts at 5301_8, the read buffer at 6321_8, the length of each buffer is 1020_8, and 8K of core memory was found.

3) The program requests the disk formatter configuration by typing:

FMPR =

The operator replies by entering from 2 or 3 numeric parameters in the form:

w, s{ , {d}}

where the individual parameters are defined as:

w = Number of words per sector
s = Number of sectors per track
d = Device address of the controller

The parameters w and s must be specified and are normally entered as one of the following pairs:

$\text{Sectors/Track}_{10}$	w	s
8	400	10
10	400	12
16	200	20

The parameter d is optional but if required, should be entered as a number in the range $1\text{-}76_8$. If omitted the default value of 30_8 will be assumed.

The program recognizes the break character Control-F during this step.

Example: FMPR = <u>200, 20, 30</u>

Specifies the words per sector, sectors per track, and coupler device address as 200_8, 20_8, and 30_8, respectively.

4) The program requests the identity and sequence of the packs to be tested by typing:

PACK =

Allowing definition of up to 8 packs on which tests are to be run. The format of each specifier is

D/L-U or D/U

where D is a drive number (0-3), L is the lowest track to use, and U is the highest track to use. L and U must satisfy $0 \leq L \leq U \leq 77$. It is possible to specify different track ranges on the same drive, e.g., 0/0-4, 0/10-70, 1/40-40, 0/0↲ specifies that tests are to be run on tracks 0-4 and 10-70 inclusive on drive 0, then track 40 (only) on drive 1, then track 0 (only) on drive 0. Note that the sector addresses used will depend on the FMPR response identifying number of sectors per track as well as the track information in the PACK sequence.
If L is omitted track 0 will be the lowest used.
If instead of a drive number the operator types

U↲

as the response to PACK = , the user test mode (Section 4.5.8) is entered. The control characters ↑P and ↑F are recognized during this step.

5) The program requests the parameters to be used to control error message printing by typing:

EMSK =

The operator responds with up to two numbers. The first is a mask for the status bits which should be reported A "1" in a bit position requests reporting of the given error, a "0" inhibits the printout. The right-hand 8 bits correspond to the 8 defined hardware status bits. Bit 3 (400_8) allows or inhibits reporting of failure of the SKNE sense instruction. Bit 2 (1000_8) controls time outs not detected by the controller while busy and bit 1 (2000_8) controls time outs while the drive is seeking to a new track position. Default of this parameter is 7777, report all errors.

The second parameter is the verify error detail limit indicating the maximum number of lines to report when data read from a given sector does not compare with the expected value. A VED limit of 0 effectively inhibits all verify error printouts. Default is 10_8 causing a maximum of eight lines of detail information to be printed for each sector in error. Control keys ↑P, ↑F & ↑E are recognized.

6) The program requests the tests to be performed by typing:

TEST =

Allowing specification of the order and number of repetitions of tests or groups of tests. Up to one full line (72 characters) of test information may be entered.

The basic building block is a character string B, of the form G [,] or C*G [,] (followed by a comma or ↲) where G is a test group and C is a count. If C is omitted a count of 1 is assumed. If G is omitted a standard sequence (tests 1-16) is assumed repeated C times. If C is given as 0 the tests in G will be repeated indefinitely.

Allowed forms for G are:

T
T1 - T2
(B [, B [---]])

The parentheses allow test groups to be nested up to four levels deep. sired. The only times parentheses are needed are when, within the parentheses, a non-unit count C is given or a discontinuous sequence of tests is to be performed. In both cases a non-unit count precedes the parenthesis. Thus,

2* (1-3, 5-15)

and

1000* (1000 * 6)

are cases where the parentheses are needed;

2* (1-5)

and

1* (1, 3, 5)

are cases where the parentheses are redundant (but legal), being equivalent to

2 * 1-5

and

1, 3, 5

respectively.

EXAMPLES:

TEST = ↲

causes the standard sequence to be performed once.

TEST = 0, 0 * ↲

causes test 0 to be performed once, then the standard sequence to be repeated indefinitely.

TEST = 0 * (0,) , 20↲

causes tests 0-16 to be repeated indefinitely. (Test 20 will never be reached.)

TEST = 0 * 0-15↲

causes tests 0-15 to be repeated indefinitely.

TEST = 0 * (4, 3*5, 3* (6-7, 2* 10-17, 6, 7, 2* (10-13, 14-17)))↲

causes the sequence of tests

4, 5, 5, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,
6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,
6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,
6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,
6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,
6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 10, 11, 12, 13, 14, 15, 16, 17,

to be repeated indefinitely.

4.5.3 Diagnostic Test Sequence – Non-interactive Tests

Normally the diagnostic tests are run in sequence from 1 through 23_8 but they can be run in any order unless otherwise noted. If no test sequence is entered (carriage return only) the sequence will run tests 1 through 16_8. Tests 20_8 through 23_8 require operator interaction.

<u>Test 0:</u> <u>Check Read</u>

Function: To verify that the disk is readable and that the preamble, data and checksum are correct

Test Procedure: Test 0 check-reads (i.e., no data transferred into core) the contents of the disk in sequence starting at Track t_1, Sector 0, and continues through each sector until all tracks and sectors, defined by PACK specifiers, are read. Besides reporting errors detected by the formatter and coupler, this test checks to see that the "dummy" buffer area was in fact not modified by this operation. A "verify error", if reported on this test, means that data was actually transferred into core.

Test 1: Format Sectors

Function: To format a new disk or prepare a disk for a series of diagnostic tests. There is no prerequisite for Test 1 which is normally the first test to be run in the diagnostic sequence.

Test Procedure The test writes a correct preamble, known data field and correct CRC for each sector, for each track, of each drive as specified by the input parameters to the diagnostic program. In the data field the first word contains the unit number, the second word the drive number, the third word the track number, and the fourth the sector number. Remaining words in the sector are left at zero. The CRC is generated by the formatter.

Test 2: Verify Sector Addresses

Function: To check Test 1 to verify that data previously created can be read correctly. Test 2 ensures unique, correct addressability of each unit, track and sector.

Test Procedure: The data pattern recorded in Test 1 is read and matched by Test 2 for verification.

Error Messages: When Tests 1 and 2 pass, the system both reads and writes on the disk and all sectors, encompassed by PACK specifiers, can be correctly addressed. Error messages output in the following tests indicate data sensitivity, dropped bits, or errors other than drive and multiplexer card malfunction. Most errors found after Tests 1 and 2 will be found in the controller card of the computer.

Test 3: Seek and Restore

Function: To check the head positioning logic.

Prerequisite: Formatted disk pack(s).

Test Procedure: A pseudo-random sequence of track addresses are generated (the same sequence is repeated for each PACK specified). For each track address that lies within the limits of the PACK specifier two seeks are issued. The first is to the given track from the current position whatever it happens to be (state counter is an even number). The second is to the given track from the given track, with a "restore" preceding the actual seek (state counter is an odd number). Track addresses outside the specified range are ignored. The sequence is such that each track address is generated at least once and none is generated more than three times.

Error Messages: A PCE probably indicates the positioning logic (including servos, etc., in the drive) is failing. Failures only in the even numbered states may mean head position memory is failing.

Test 4: Write Half-Sector

Function: To check the half-sector logic of the formatter.

Test Procedure: A single sector is written with the all-ones pattern in "half-sector" mode. It is then read back in full-sector mode and checked to see that the first part of the data was written correctly, and the rest of the sector was padded with zeros (Ø's) as required. Then a full-sector write is done, with verification, to see that the half-sector mode can be cleared.

Enter Messages: A verify error here may indicate failure to divide the sector correctly. Note that the expected data is always 0000 or 7777. If one of these numbers appears when the other is expected it is symptomatic of the above; on the other hand any other pattern (e.g. 7757) probably indicates an ordinary data error. A verify error not preceded by a hardware error (CRC) also indicates the sector-splitting logic has failed.

Test 5: Read Half-Sector

Function: To test half-sector input logic.

Test Procedure: A full sector of the ONES pattern is written and compared. Then the upper half of the read buffer is zeroed out and a half-sector read is undertaken. Correct input into the first half of the buffer, and integrity of the second half, are then verified.

Test 6: CRC Generation

Function: To validate the mod-2 polynomial divider in the formatter.

Test Procedure: All standard data patterns are generated and output with standard write commands. After each output the program reads the sector in diagnostic mode getting back the CRC as well as data. The CRC is simultaneously calculated by the program and the software and hardware versions are compared.

Error Messages: A verify error with one comparand at loc. 00055 or 00056 indicates an invalid CRC. If this occurs consistently, without associated hardware errors, the formatter is a "hermit formatter". This formatter can read disks written by itself, but cannot read a disk written by another formatter, or write on a disk to be read by another formatter.

Test 7: Memory Addressing

Function: To test the CPU addresses generated by the coupler during data transfer.

Test Procedure: A sector is written with the ascending count pattern and is then read back to every possible buffer area between the top of the program and loc. 7600 (the last 200_8 words of memory are unchanged unless an error occurs). The last buffer's starting address will be 7600-WPSEC, where WPSEC is the (octal) number of words per sector. (Hence this test goes through 100_8 more iterations for a disk with 400_8 words per sector than it does for a disk with 500_8 words per sector.)

Error Messages: Carry propagation from one 4-bit counter to another is the occurrence most likely to account for systematic failures in this test. Look for runs of 16 numbers in ascending order, starting with the wrong number, or for a run of errors starting at location 7400.

Test 10: Worst Case Data

Function: To check recording surface integrity and data recovery under severest conditions of pulse crowding.

Test Procedure: A test pattern (binary 110110110...) is written on each sector in each PACK specification, read back, and verified.

Error Messages: A zero dropout is the error most likely to result in this pattern. For example 6666 (expected) unexpectedly becomes 6755 or 6675 or something similar, followed by the (out of phase) pattern 5555.... The latter may suffer another dropped zero, leading to ...5573 3333 ... which may eventually re-synchronize as ...3376 6666 ... (now one full octal digit out of phase). There should be a hardware error (CRC) message before any verify error messages on a sector.

Tests 11 and 12: Random Data Tests

Function: To ensure that the recorder can position and reach back at random the recorded data. The drive and controller card are tested for mechanical positioning and data transfer capabilities.

Test Procedure: Tests 11 and 12 are run in sequence. Test 11 writes pseudo random data in each sector on every track of each unit specified. Once the data is written it is then read in one complete pass to verify accuracy. Test 12 uses the data established in Test 11 as a base and selects a unit, track and sector number at random to read back and verify. Verification occurs when data read back is compared to a pattern determined as a function of the first two words of the sector. The random select is repeated for 256 sectors.

Error Messages: Multiple errors on a sector, especially in the absence of a hardware error message, may indicate failure of the track select, unit select, or rotational position logic

Caution: Test 11 will report failures if any two PACK specifications include one or more tracks in common, as in

PACK = 0/1-11, 0/6

Test 13: Memory Fields

Function: To test exhaustively the ability of the PDP-8/E coupler to select each possible memory field, and to increment the field address on an address counter overflow from 7777 to 0000.

Test Procedure: State XØ writes a count pattern starting with ØXØØ and increasing to ØXØØ + WPSEC - 1, to the first usable sector of the first specified pack. (X is the field currently being used and ranges from 0 to 7; the buffer for this step is in field X.)

State X1 reads the sector back into field 0 and compares it with the data in the write buffer in field X.

State X2 reads the sector back into field X and compares it with the output buffer in field X.

State X3 reads the sector into a buffer which overlaps field X and X + 1 (modulo 10_8) and verifies that the field address advance when the 12-bit address rollover occurred.

Note: Where a designated field does not in fact have any memory, state XØ becomes effectively write zeros, state X1 validates this, state X2 conveys no information, and state X3 conveys information only if field X + 1 has real memory (as when X = 7, X + 1 = 0.)

States X4, X5, X6, and X7 do not occur. The last state is 73 (increment from field 7 to field 0.)

If the memory field option is not installed in the computer, the diagnostic switches off access to test 13 entirely; e.g.,

TEST = <u>1, 13</u> ⤶
TEST 1
TEST = (test 13 was bypassed)

Error Messages: Receiving all zeros in state X1 when the memory really exists (indicated by verify errors without hardware errors) probably means the field select logic is faulty. Failures only in the X3 steps may mean the carry propagation is too slow, or that it is blocked completely.

Test 14: CRC Error Forcing

Function: To verify error detection for every bit position in the CRC logic.

Test Procedure: Using each defined data pattern the program writes a sector in diagnostic mode complementing in turn each of the 16 bits of the CRC word. After each write operation the sector is read back in normal mode and the program checks for CRC error status from the hardware. After the 16th bit for the 6th data pattern has been tested, the sector is re-set with an ordinary WRITE command.

Test 15: Interrupt Functions

Function: To test the coupler interrupt logic

Test Procedure:

State 0: Test SKNI when an operation is done but interrupts are inhibited.

State 1: Test SKNI after SKNI to see that second time is always a skip.

State 2: Test SKNI when an operation is done and interrupts are allowed from the XFD-108.

State 3: Test that SKNI cleared interrupt request although the CPU did not recognize the request.

State 4: Test that interrupt occurs under the conditions that in State 2 caused SKNI to report an interrupt request.

State 5: Test that SKNI works after the interrupt generated in State 4.

State 6: Test that a No-Op command with the interrupt-enable bit OFF, can clear a pending interrupt without the help of SKNI.

State 7: Test that BUSY stayed false after the No-Op command of state 6.

Error Messages: The information content is complete in the state number of the IE message format. Refer to the above list for error status.

Test 16: Status Interference

Function: To test the accurate inter-mix of CPU data requests with programmed status interrogation.

Test Procedure: Under the three conditions of writing, reading and check-reading, the program enters a wait loop in which it continually requests status. The coupler should relay all core-to-disk or disk-to-core data correctly and still respond to all the status queries (In state 2 it should transfer no data, only status). The data is a count pattern.

Error Messages: A skipped number in the count pattern indicates that the coupler "forgot" a pending data transfer while responding to a status query. In state 0 the data verification pass is done without interrogating status, therefore a verify error during state 0 implies interference during output. A verify error during state 1 (without errors during state 0) implies that interference occurs only on input. During state 2 a verify error implies that data was transferred into memory on a check read with status interrogation; in this case the results of test 0 are also significant.

"Rate error" status is not expected to be set as a result of this test.

Test 17: Time Out Error Circuit

Function: To test the error detection circuit for systems with less than 16 sectors per revolution.

Test Procedure: Test attempts to read from sector 1777 of the first specified pack. If this sector does not exist (8 or 10-sector formatter) the TMO status bit should be set.

This test should not be specified for formatters with 16 sectors per revolution.

4.5.4 Diagnostic Test Sequence – Interactive Tests

The following tests all use the first drive of the first PACK specification, and all halt for operator intervention.

<u>Test 20: Rate Error</u>

Function: To check that the RATE status bit can be set on both reading and writing.

Test Procedure: The program starts a write and halts. When CONT is pressed it starts a read and halts. The status register is checked in each case for the rate error bit.

Operator Action: Press CONT after each HALT.

<u>Test 21: Write Protection Check</u>

Function: To test the write-protection logic.

Test Procedure: Attempt a write on a protected pack and look for WPE status.

Operator Action: On the first HALT after the "TEST #21" message attach a write-protect tab on the pack in the first unit given in the PACK specifications. When the unit is up to speed again, press CONT. On the second HALT, remove the tab, wait for the unit to come up to speed, and press CONT again.

<u>Test 22: Not Ready</u>

Function: To test the ready status logic.

Test Procedure: The program halts to allow the operator to disable the primary drive, checks for not-ready status on an attempted READ, then monitors the status until the drive is again ready.

Operator Action: When the program halts, disable the unit of the first PACK specifier. Press CONT. Any time after this, press the RUN switch on the drive.

Test 23: Format Error

Function: To validate the FMTE status logic.

Test Procedure: The program halts for the operator to insert a pack that has been formatted for a different number of sectors per revolution. The program continues and tries to read a sector, which should have a sector gap too soon or not soon enough. In either case the format error status bit should be set.

Operator Action: On the first halt insert the mis-formatted pack and press CONT. On the second halt replace the regular pack in the drive and press CONT.

4.5.5 Status Error Reporting

When received status differs from expected status in bit positions enabled by the EMSK word a hardware error message is produced having the format:

HE nnnn ssss cccc dddd mmmm

where nnnn is the state counter for the test in progress;

ssss is the status

cccc is the command word

dddd is the disk address

mmmm is the memory address.

The bits in ssss include the 8 defined hardware status flags (values 1-200_8) and three software-generated bits:

400_8 SKNE claimed an error when there were no error bits in the status register, or claimed no error when some status register error bit was set;

1000_8 BUSY stayed true beyond the limits that should have caused a TMO error;

2000_8 Time out on a seek or restore operation, with BUSY false.

(These bits, like the hardware error bits, may be enabled or inhibited by corresponding bits in the EMSK word.)

4.5.6 Verify Error Reporting

When data disagrees (with or without hardware errors) a message in the form

VE nnnn dddd wwwww = yyyy ggggg = zzzz

is output,

where nnnn is the test state

dddd is the disk address

wwwww is the address of the expected data (including the field digit)

yyyy is the expected data

ggggg is the address of the data actually retrieved

zzzz is the data in error.

Ordinarily the right-hand 4 digits of wwwww and ggggg will be within the read and write buffers but may take special values, e.g., 00055 and 00056 for the computed value of a CRC. The VE message will be repeated no more times on a given disk sector than the detail limit allows (See EMSK).

4.5.7 Interrupt Error Reporting

A message of the form

IE nnnn cccc

is output,

where nnnn is the test state and

cccc is the disk command.

This message only appears during Test 15 and the information content of the message centers in the state number. Each state has exactly one error exit. Refer to the program listing for details of the tests.

4.5.8 User Specified Tests

A response of U↵ to the PACK = prompting message puts the program in a special mode allowing the construction of test sequences tailored to a specific problem. Up to eight test steps can be defined and execution can be controlled such that each one is repeated indefinitely until the operator instructs otherwise or all tests are repeated cyclically.

The tests are set up by two supplementary prompting messages as follows:

OP = cmd [, data type [, expected status [, mask [, field]]]]

Cmd is the disk command (including all modifier bits) and cannot be defaulted.

Data type specifies the pattern with which the buffer is filled before activating the disk. The choices for this parameter are

- 0 - Set all locs in buffer to 0
- 1 - Set all locs in buffer to 1
- 2 - Set to 5252/2525...
- 3 - Ascending count
- 4 - Descending count
- 5 - Pseudo-random
- 6 - Worst case (binary 110110110...)

the default is 0.

Expected status may be any octal value, default is 0.

Mask is the error mask, default is 7777.

Field specifies the memory field for the coupler to use.

NOTE: This is useful primarily for reading, since the data pattern is always loaded into field 0, and writing from another field will not access the desired data pattern. This parameter may range in value from 0 to 7 with a default of 0.

AD = unit [, sector [, X1 [, X2]]]

Unit selects the drive and cannot be defaulted. Range is 0-3.

Sector selects a sector number, default is 0. Range is $0\text{-}1777_8$.

X1, X2 are exclusive OR masks for the software CRC generator.

The computed checksum bits will be inverted wherever there is a "1" in the corresponding bit of X1 (most significant 12 bits of the CRC) or X2 (least significant 4 bits of the CRC). If the command is some form of write with checksum this will have the effect of generating an invalid checksum on the indicated sector.

After responding to the OP and AD messages one or more times (up to 8), the operator may end the user test definition phase by responding

↙

to the OP - prompt. The program then enters test execution mode.

During user test execution mode sequence control is effected by the teletype and by front panel data switches 0 and 1. The control options are as follows:

Switch 0 If reset (down) the program halts before executing the next test step (but after the data buffer is filled). If set (up) the program executes the test step without halting.

Switch 1 If reset (down) the program loops on the current test. If set (up) the program advances (cyclically) to the next test in the list.

Teletype Keys:

CTRL N Advances to next test (has the same effect as momentarily setting switch 1 up).

CTRL P Return to PACK prompting message

CTRL F Return to FMPR prompting message

4.6 OS/8 VERSION 3 SYSTEM AND NON-SYSTEM HANDLERS

The Xebec Systems OS/8 Version 3, System and Non-System Handlers for the XFD-108 Flexible Disk System are designed to operate under BUILD. Once inserted into the OS/8 system via BUILD they allow the inclusion of a system device (SYS), up to two coresident non-system devices (F0 and F1), and up to four non-coresident non-system devices (FO, F1, F2, and F3). Each device contains 640_{10} (or 1200_8) OS/8 blocks of 256_{10} (400_8) 12-bit words, for a total of $163,340_{10}$ words of storage.

Two handlers are supplied at nominal cost either on paper tape or on diskette. It is assumed that the customer has his own OS/8 software kit (on paper tape, DEC tape or magnetic tape).

Paper Tape	Xebec Part Number
XFD-108 System Handler	350176
XFD-108 System Handler, Source	350177
XFD-108 Non-System Handlers, Binary	350178
XFD-108 Non-System Handlers, Source	350179

As supplied on diskette, Xebec Part Number 350180, these handlers are filed as follows:

File Name	Handler
SYFDV3. BN	XFD-108 System Handler, Binary
SYFDV3. PA	XFD-108 System Handler, Source
NONSFD. BN	XFD-108 Non-System Handler, Binary
NONSFD. PA	XFD-108 Non-System Handler, Source

4.6.1 Using Handlers — General Description

All standard procedures for BUILD apply to the Xebec Systems XFD-108 Handlers. See the OS/8 Handbook (DEC-S8-OSHBA-A-D) for standard procedures. Specifically, either handler may be LOADed, and any device may be INERTed in the normal BUILD execution.

4.6.2 Xebec Systems OS/8 System Handler for XFD-108

Device Type Name	OS/8 Device Name	XFD-108 Disk Unit Number	Entry Point Offset	Device Type
FD10	SYS	0	(7)	40
FD10	F0	0	30	40
FD10	F1	1	31	40

4.6.3 Xebec Systems OS/8 Non-system Handler for XFD-108

Device Type Name	OS/8 Device Name	XFD-108 Disk Unit Number	Entry Point Offset	Device Type
XFD	F0	0	30	40
XFD	F1	1	31	40
XFD	F2	2	32	40
XFD	F3	3	33	40

4.6.4 Changing Formatter Addresses in the Handlers

Both handlers, as distributed, assume that the XFD-108 address for I/O purposes is 30_8. In each handler the first non-comment line is:

BASE = 6300

If it is necessary to change the formatter address by jumpering (reference Section 3.1.7.2 — Device Address Modification) the change may be reflected in the handlers by changing the middle two octal digits in the statement. For example, for a device address of 65_8 edit both sources so that the statement reads:

BASE = 6650

then assembly both new sources and use in the normal manner with BUILD.

4.6.5 Bootstrapping the XFD-108

OS/8 on the XFD-108 disk system may be bootstrapped in four different ways:

1) Implemented Program Load
2) ROM Bootstrap
3) General Key-in Bootstrap
4) OS/8 Key-in Bootstrap

For convenience, the OS/8 Key-in Bootstrap is given below:

Location	Contents
00020	6305
00021	6304
00022	5022

OPERATING INSTRUCTIONS: LOAD ADDRESS 20; LOAD MEM. FIELD 0; Depress CLEAR and CONTINUE.

SECTION 5
MAINTENANCE INFORMATION

5.1 GENERAL

The Xebec Systems XFD-108 Flexible Disk System is designed for dependable, maintenance-free operation; there are no periodic (preventative) maintenance requirements, and system adjustments (or alignments).

5.2 MAINTENANCE CONCEPT

Xebec Systems, Inc. has attempted to make maintenance and repair of the XFD-108 system as easy as possible Recommended maintenance for the Xebec XFD-108 consists of periodic system performance checks with the standard flexible disk diagnostic program. To verify system performance, the diagnostic should be run following system installation, and periodically thereafter.

Similarly, if a system malfunction is suspected, use the diagnostic program as a guide to isolating the malfunction to one particular section of the hardware. Section 4 describes the diagnostic program and procedures. Once an error message is printed out for any given test, that information can be analyzed with the information in the diagnostic description, in order to isolate the malfunction to one of five probable areas:

1) Disk drive assembly (two per chassis unit)
2) Power supply (one per chassis unit)
3) Drive logic card assembly (one per chassis unit)
4) Formatter card assembly (one per system in the main recorder chassis unit)
5) Coupler card assembly (one per system; located in the PDP-8/E Computer)

If a malfunction is isolated to one of these subassemblies, remove it from the system, and replace it with a spare subassembly that is operating properly. Return the malfunctioning subassembly to the factory for repair. The disassembly procedures are included in this section of the manual; follow the procedures for removing any of the subassemblies.

5.3 FACTORY REPAIR

After a subassembly has been removed, ship it to:

Customer Service Department
Xebec Systems, Inc.
566 San Xavier Avenue
Sunnyvale, Ca. 94086

For additional information, write, call or TWX the Xebec Systems Customer Service Department at the following numbers:

Telephone:	(408) 732-9444
TWX:	910-339-9292

When shipping any unit or component, send the following information:

1) Name and address of owner.
2) Brief discussion of symptoms or trouble.
3) If possible, send the name and telephone number of someone familiar with the problem, and who may be contacted if more information is necessary.
4) Special shipping instructions, if any. Include your return shipping address and department mail address, if necessary.

5.4 PACKING/SHIPPING INSTRUCTIONS

If the entire system is to be shipped, pack it according to the instructions in Para. 3.3. If a subassembly is being shipped, use the following packing procedure:

1) Wrap the subassembly in plastic.
2) Place the subassembly in a sturdy container; add packing material around all sides of the subassembly.
3) Seal the shipping container with reinforced tape.
4) Mark the shipping container to indicate that it contains fragile electronic equipment.

5.5 POWER SUPPLY CHECKS

Table 5-1 lists nominal power supply voltages for reference. Power supply voltages should be checked during initial or subsequent installation, and whenever the system is malfunctioning. In case of system failure, check and replace the fuses as necessary, according to Table 5-2. If fuse(s) continue to blow, or the voltages are out of tolerance, replace the power supply.

WARNING

Always disconnect the 115V ac line power when checking or replacing power supplies or fuses within the chassis unit (Section 5.7.3).

To check the power supply voltages, or the interior fuses, remove the chassis unit top cover for interior access. Power supply voltages can be checked on the power supply PC board, which is located on the bottom panel of the chassis interior (See Figure 5-1).

5.6 ADJUSTMENTS

There are no adjustments required for the normal operation and maintenance of the XFD-108 system. Note, however, that there are adjustments or alignments required for the repair of the disk drive units. These are normally performed as part of the factory repair services.

Table 5-1. Power Supply Voltages

Supply	Voltage Tolerance
+5V	+0.2; -0.4
+24V*	+2.0; -0
-12V	+2; -0

* Unregulated

Table 5-2. System Fuses

Supply	Rating (Amps)
Rear Panel ac	5
-12V dc	3
+5V dc	10
+24V ac	10

5.7 RECORDER CHASSIS UNIT DISASSEMBLY

The drive logic card, the formatter card, the power supply and the disk drive units are located in the chassis unit; for access, use the following procedure:

1) Loosen the pawl fasteners on the front panel of the disk drive chassis assembly, and slide the chassis unit out from the rack.

2) Remove the top cover of the chassis for access to the chassis unit interior. To remove the cover, loosen the Phillips-head cover retainer screws at the chassis and back. After loosening the screws, lift the cover off the chassis.

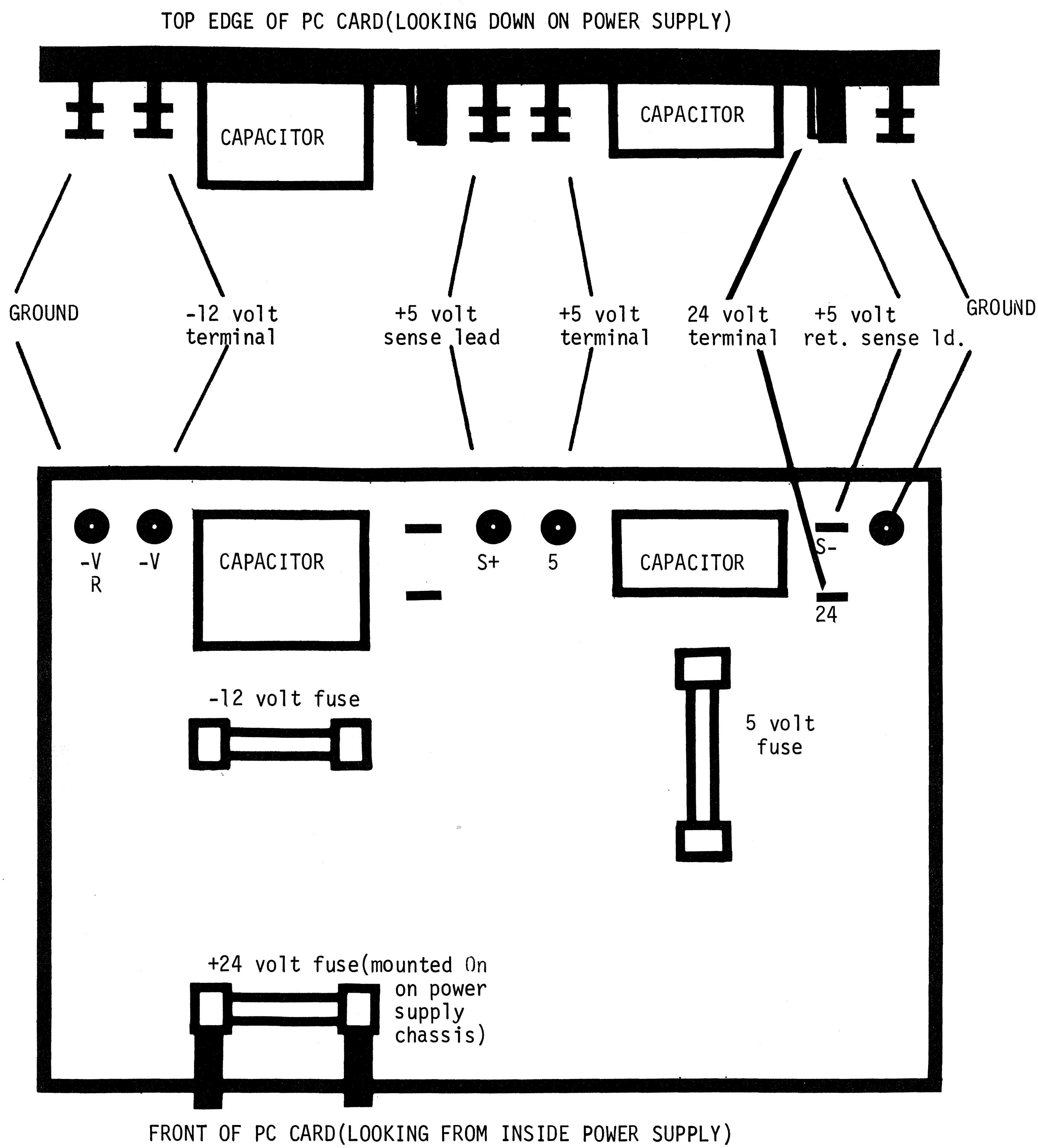


Figure 5-1. Test Points and Fuses on Power Supply PC Board

5.7.1 Disk Drive Assembly Removal

1) Disconnect the two cable connectors at the rear of each drive assembly. One of the connectors has thumb screws that secure it to the drive assembly; loosen the thumb screws and slide the connector off. The other connector is not secured, and slides off.

2) On the bottom of the disk drive assembly unit, there are three Phillips-head screws that secure each of the drives. Remove the corresponding three screws, and slide the drive unit out from the front of the disk recorder chassis assembly.

5.7.2 Removal of Drive Logic and Formatter Cards

1) Disconnect cables connected to J1, J2, J3 and J4 on the rear panel of the chassis. Remove the line cord that connects ac power to the chassis.

2) Remove the small phenolic cover that protects the ac power connectors to the drive units. This will reveal two connectors marked L1 and L3. Unplug the two connectors.

CAUTION

Before attempting to remove the formatter or drive logic circuit cards, be sure to disconnect all 115V ac line power from the disk recorder chassis unit.

3) To remove the formatter card, pull straight up. The formatter card should come loose.

4) To remove the drive logic board, remove the four nylatches that secure the PC board, and lift it from the recorder chassis assembly.

5.7.3 Power Supply Disassembly

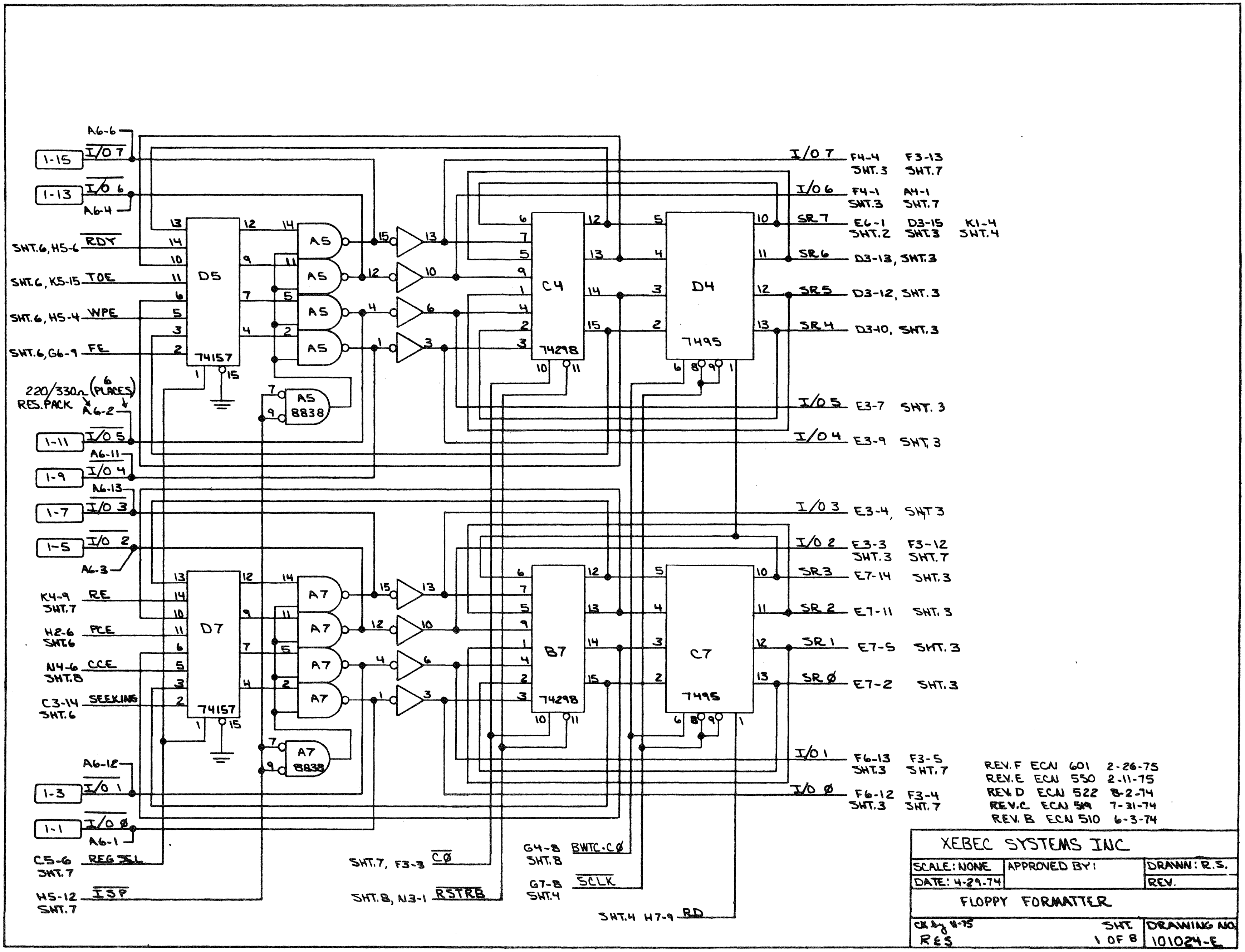
To remove the power supply, unplug the two connectors and remove the base plate screws. The power supply can then be lifted out.

CAUTION

When replacing the power supply, be sure that all transformer cables will remain clear of the belt drive mechanism on the disk recorder drive.

5.7.4 Coupler Card

If trouble is isolated to the coupler card, remove it from the PDP-8/E computer. Remove the covers of the computer and locate the Xebec Systems, Inc. I/O coupler card assembly, which is etched on the card. When replacing the coupler card, make sure that it is positioned correctly in the guidance slots, and that the connectors are aligned properly.



A6-6
I/O 7
1-15
I/O 6
1-13
A6-4
SHT.6, H5-6 RDY
SHT.6, K5-15 TOE
SHT.6, H5-4 WPE
SHT.6, G6-9 FE
D5
74157
A5
A5 8838
220/330Ω (6 PLACES) RES. PACK A6-2
1-11 I/O 5
A6-11
1-9 I/O 4
A6-13
1-7 I/O 3
1-5 I/O 2
A6-3
K4-9 SHT.7 RE
H2-6 SHT.6 PCE
N4-6 SHT.8 CCE
C3-14 SHT.6 SEEKING
D7
74157
A7
A7 8838
A6-12
1-3 I/O 1
1-1 I/O Ø
A6-1
C5-6 SHT.7 REG SEL
H5-12 SHT.7 ISP
C4
74298
D4
7495
B7
74298
C7
7495
I/O 7 F4-4 SHT.3 F3-13 SHT.7
I/O 6 F4-1 SHT.3 A4-1 SHT.7
SR 7 E6-1 SHT.2 D3-15 SHT.3 K1-4 SHT.4
SR 6 D3-13, SHT.3
SR 5 D3-12, SHT.3
SR 4 D3-10, SHT.3
I/O 5 E3-7 SHT. 3
I/O 4 E3-9 SHT. 3
I/O 3 E3-4, SHT 3
I/O 2 E3-3 SHT.3 F3-12 SHT.7
SR 3 E7-14 SHT.3
SR 2 E7-11 SHT. 3
SR 1 E7-5 SHT. 3
SR Ø E7-2 SHT. 3
I/O 1 F6-13 SHT.3 F3-5 SHT.7
I/O Ø F6-12 SHT.3 F3-4 SHT.7
SHT.7, F3-3 CØ
SHT.8, N3-1 RSTRB
G4-8 SHT.8 BWTC·CØ
G7-8 SHT.4 SCLK
SHT.4 H7-9 RD
REV.F ECN 601 2-26-75
REV.E ECN 550 2-11-75
REV.D ECN 522 8-2-74
REV.C ECN 519 7-31-74
REV.B ECN 510 6-3-74
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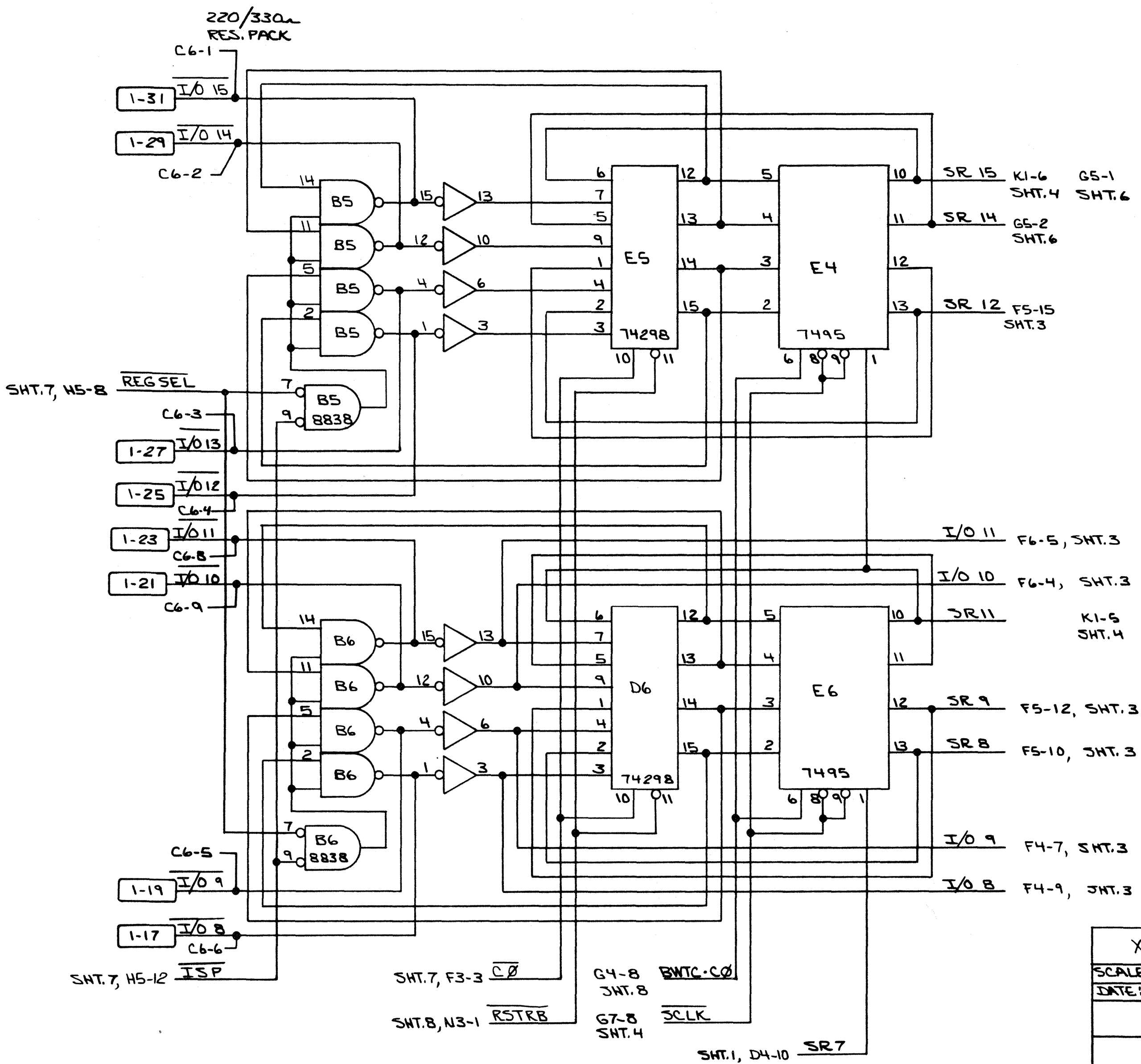
DATE: 4-29-74
REV.
FLOPPY FORMATTER
CK by 4-75 RES
SHT. 1 OF 8
DRAWING NO. 101024-E



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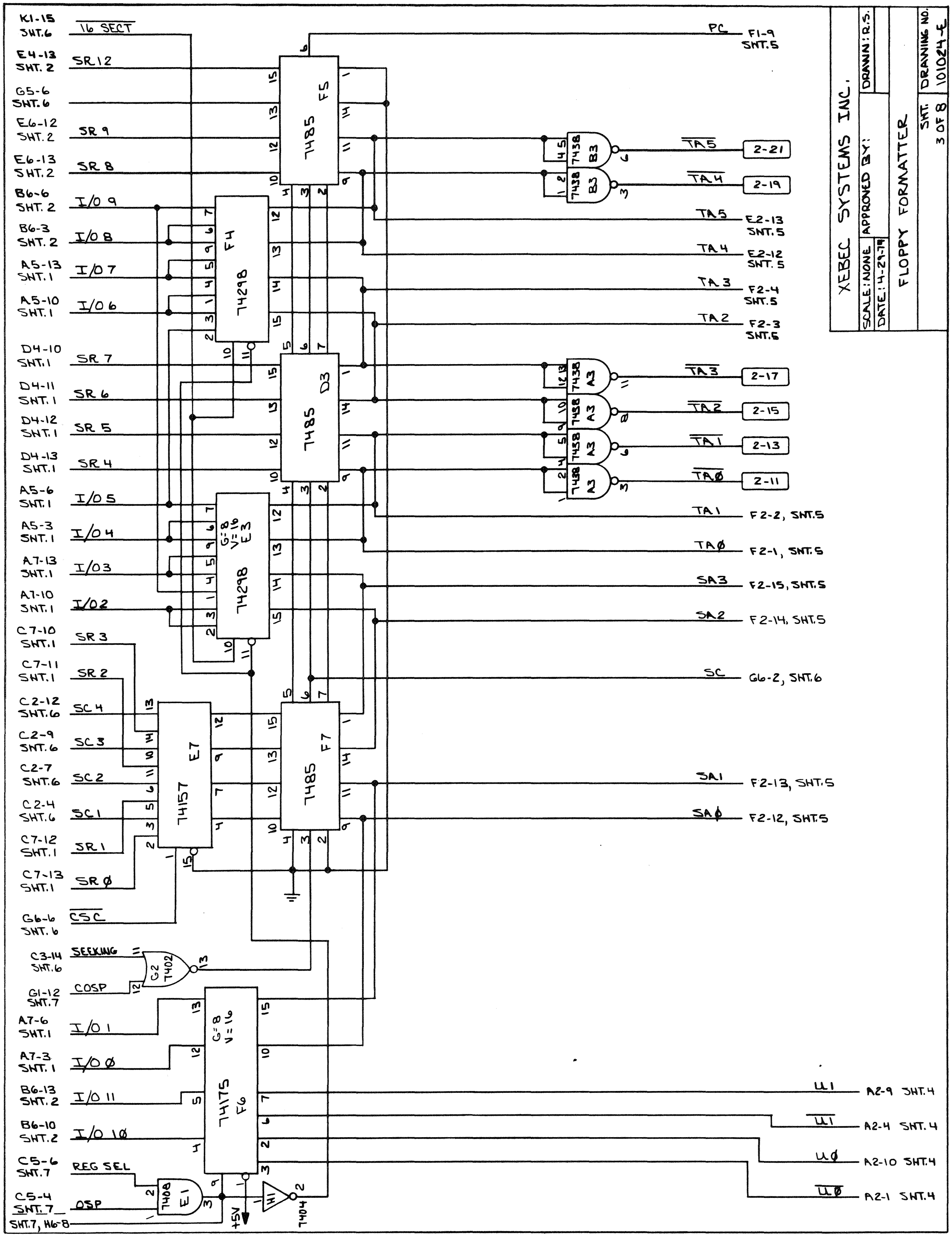
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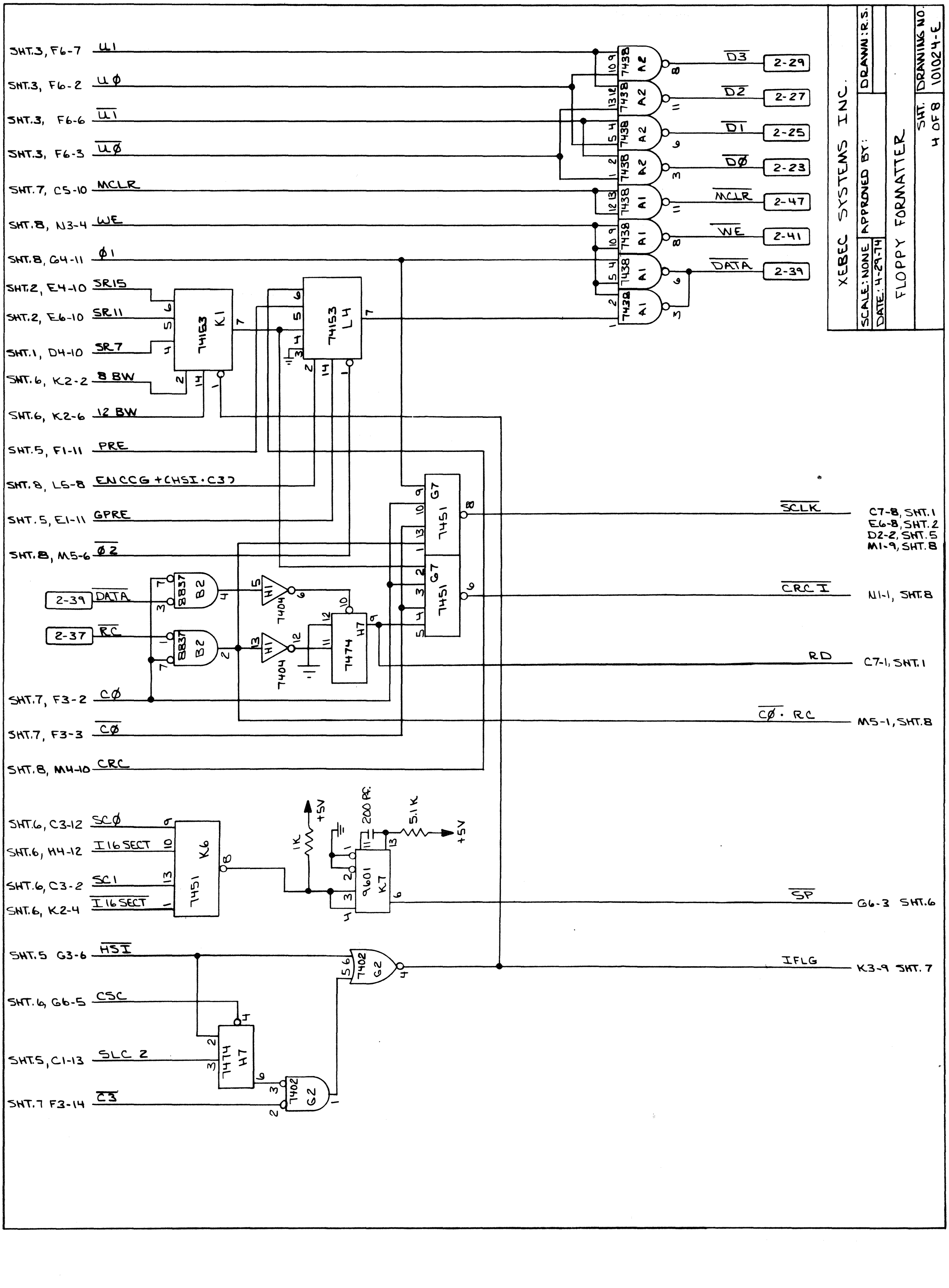
E4-13 SHT.2 SR12
G5-6 SHT.6
E6-12 SHT.2 SR9
E6-13 SHT.2 SR8
B6-6 SHT.2 I/O 9
B6-3 SHT.2 I/O 8
A5-13 SHT.1 I/O 7
A5-10 SHT.1 I/O 6
D4-10 SHT.1 SR7
D4-11 SHT.1 SR6
D4-12 SHT.1 SR5
D4-13 SHT.1 SR4
A5-6 SHT.1 I/O 5
A5-3 SHT.1 I/O 4
A7-13 SHT.1 I/O 3
A7-10 SHT.1 I/O 2
C7-10 SHT.1 SR3
C7-11 SHT.1 SR2
C2-12 SHT.6 SC4
C2-9 SHT.6 SC3
C2-7 SHT.6 SC2
C2-4 SHT.6 SC1
C7-12 SHT.1 SR1
C7-13 SHT.1 SRØ
G6-6 SHT.6 CSC
C3-14 SHT.6 SEEKING
G1-12 SHT.7 COSP
A7-6 SHT.1 I/O 1
A7-3 SHT.1 I/O Ø
B6-13 SHT.2 I/O 11
B6-10 SHT.2 I/O 10
C5-6 SHT.7 REG SEL
C5-4 SHT.7 OSP
SHT.7, H6-8
7485 F5
74298 F4
7485 D3
74298 E3 G:8 V:16
7485 F7
74157 E7
74175 F6 G:8 V:16
7402 G2
7408 E1
7404 H1
7438 B3
7438 A3
+5V
PC F1-9 SHT.5
TA5 2-21
TA4 2-19
TA5 E2-13 SHT.5
TA4 E2-12 SHT.5
TA3 F2-4 SHT.5
TA2 F2-3 SHT.5
TA3 2-17
TA2 2-15
TA1 2-13
TAØ 2-11
TA1 F2-2, SHT.5
TAØ F2-1, SHT.5
SA3 F2-15, SHT.5
SA2 F2-14, SHT.5
SC G6-2, SHT.6
SA1 F2-13, SHT.5
SAØ F2-12, SHT.5
U1 A2-9 SHT.4
U1 A2-4 SHT.4
UØ A2-10 SHT.4
UØ A2-1 SHT.4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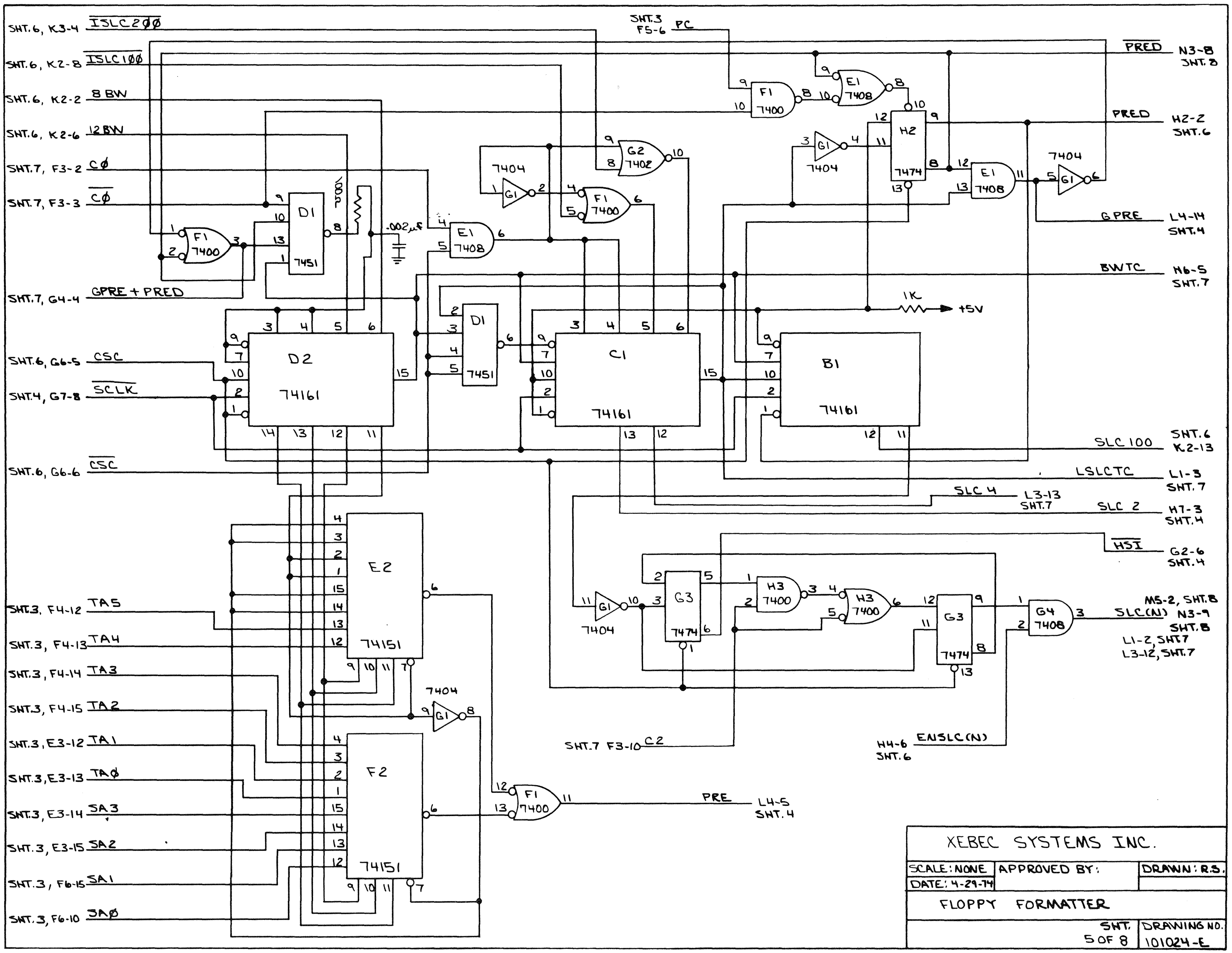
SHT.3, F6-2 U0
SHT.3, F6-6 U1
SHT.3, F6-3 U0
SHT.7, C5-10 MCLR
SHT.8, N3-4 WE
SHT.8, G4-11 Ø1
SHT.2, E4-10 SR15
SHT.2, E6-10 SR11
SHT.1, D4-10 SR7
SHT.6, K2-2 8 BW
SHT.6, K2-6 12 BW
SHT.5, F1-11 PRE
SHT.8, L5-8 ENCCG+(HSI·C3)
SHT.5, E1-11 GPRE
SHT.8, M5-6 Ø2
SHT.7, F3-2 CØ
SHT.7, F3-3 CØ
SHT.8, M4-10 CRC
SHT.6, C3-12 SCØ
SHT.6, H4-12 I16 SECT
SHT.6, C3-2 SC1
SHT.6, K2-4 I16 SECT
SHT.5 G3-6 HSI
SHT.6, G6-5 CSC
SHT.5, C1-13 SLC 2
SHT.7 F3-14 C3
D3 2-29
D2 2-27
D1 2-25
DØ 2-23
MCLR 2-47
WE 2-41
DATA 2-39
2-39 DATA
2-37 RC
SCLK C7-8, SHT.1 E6-8, SHT.2 D2-2, SHT.5 M1-9, SHT.8
CRC I N1-1, SHT.8
RD C7-1, SHT.1
CØ · RC M5-1, SHT.8
SP G6-3 SHT.6
IFLG K3-9 SHT. 7
7438 A2
7438 A1
74153 K1
74153 L4
7451 G7
8837 B2
7404 H1
7474 H7
7451 K6
9601 K7
7402 G2
+5V
1K
200 PF.
5.1 K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SHT.6, K2-8 ISLC1ØØ
SHT.6, K2-2 8 BW
SHT.6, K2-6 12 BW
SHT.7, F3-2 CØ
SHT.7, F3-3 CØ
SHT.7, G4-4 GPRE + PRED
SHT.6, G6-5 CSC
SHT.4, G7-8 SCLK
SHT.6, G6-6 CSC
SHT.3, F4-12 TA5
SHT.3, F4-13 TA4
SHT.3, F4-14 TA3
SHT.3, F4-15 TA2
SHT.3, E3-12 TA1
SHT.3, E3-13 TAØ
SHT.3, E3-14 SA3
SHT.3, E3-15 SA2
SHT.3, F6-15 SA1
SHT.3, F6-10 SAØ
SHT.3 F5-6 PC
PRED N3-8 SHT.8
PRED H2-2 SHT.6
GPRE L4-14 SHT.4
BWTC H6-5 SHT.7
1K +5V
SLC 100 SHT.6 K2-13
LSLCTC L1-3 SHT.7
SLC 4 L3-13 SHT.7
SLC 2 H7-3 SHT.4
HSI G2-6 SHT.4
M5-2, SHT.8
SLC(N) N3-9 SHT.8
L1-2, SHT.7
L3-12, SHT.7
SHT.7 F3-10 C2
H4-6 SHT.6 ENSLC(N)
PRE L4-5 SHT.4
.002µf
100Ω
D1 7451
F1 7400
E1 7408
G1 7404
G2 7402
H2 7474
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E2 74151
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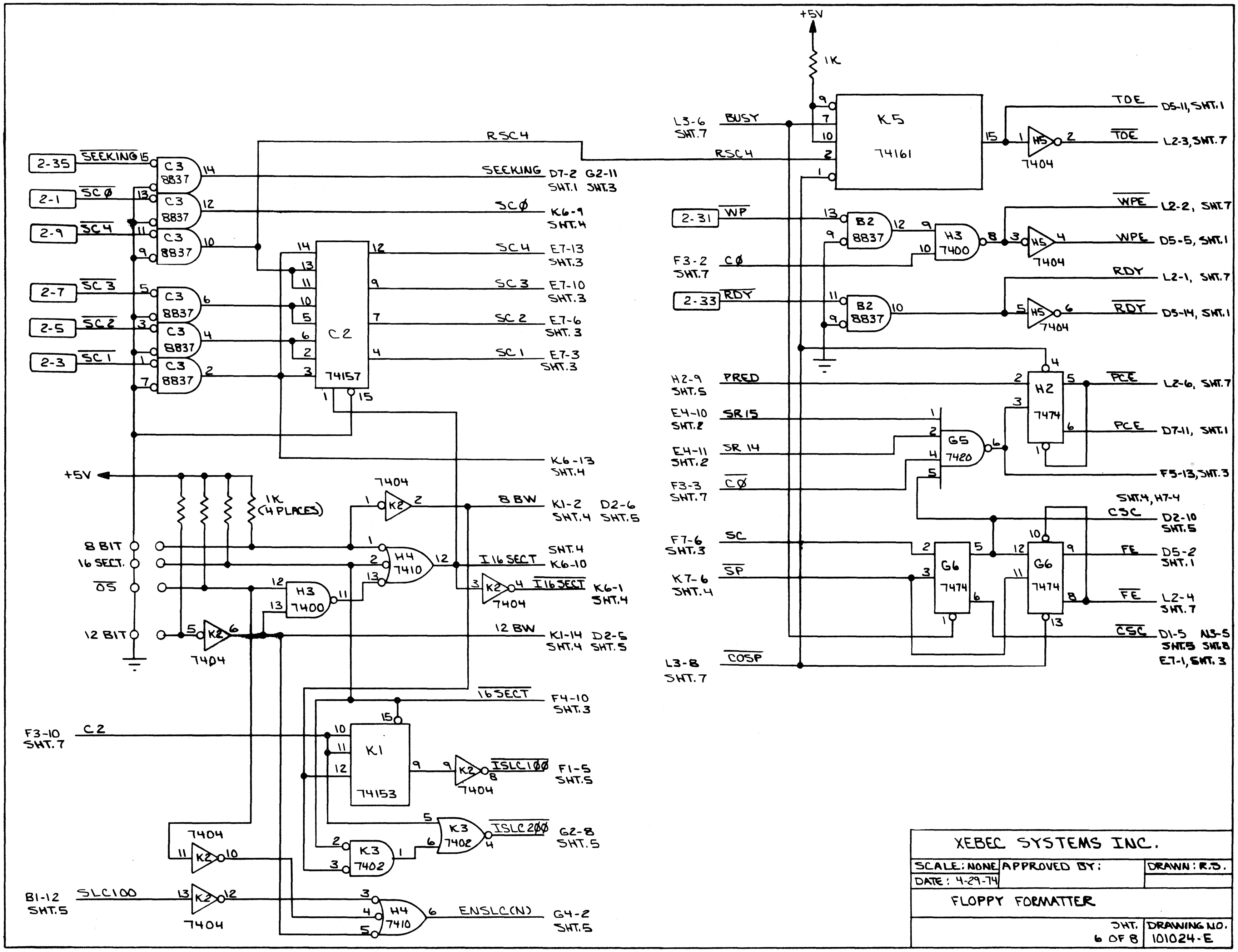
G3 7474
H3 7400
G4 7408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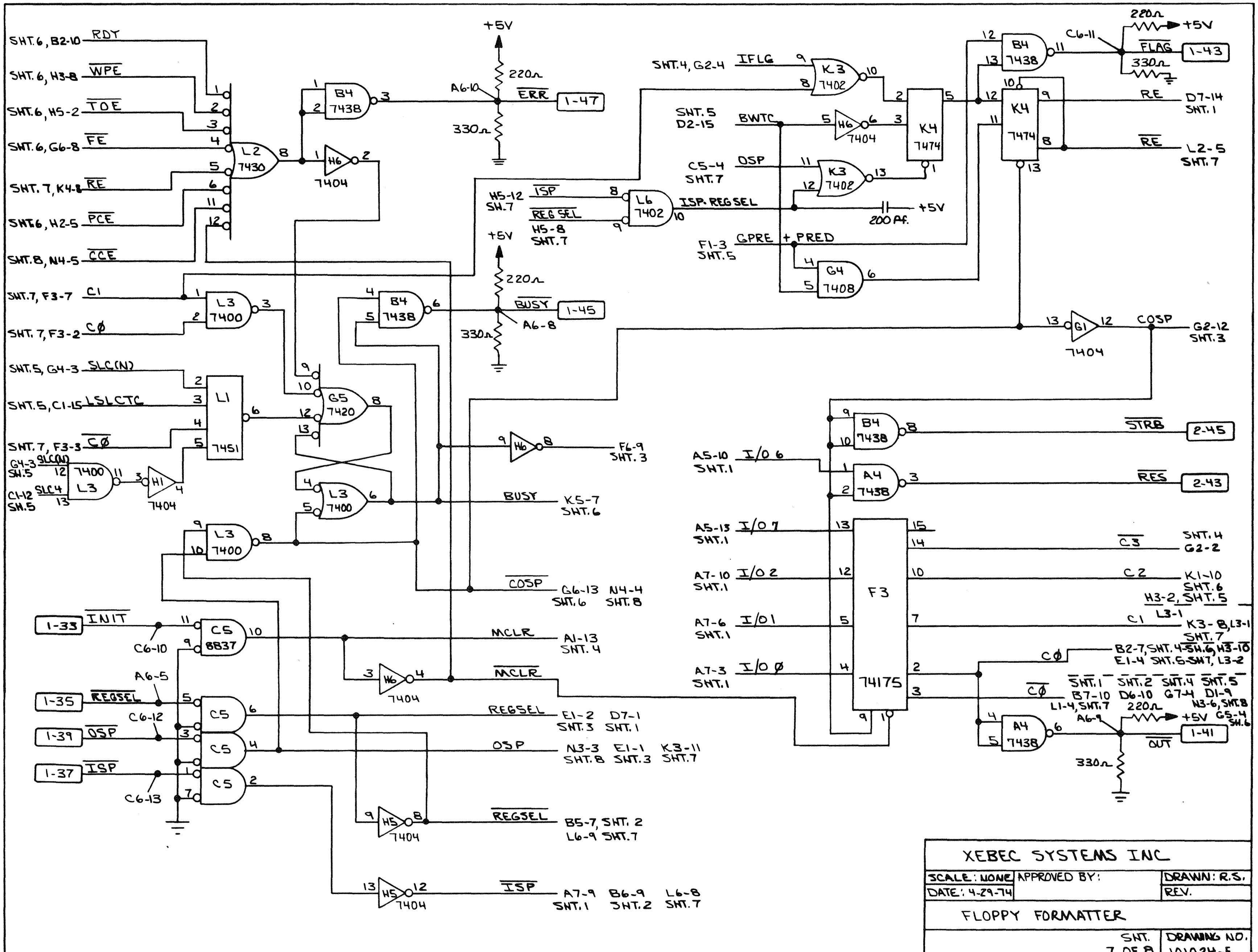
SEEKING
SC Ø
SC 4
SC 3
SC 2
SC 1
RSC 4
C3 8837
C2 74157
K5 74161
BUSY
WP
RDY
TOE
WPE
PRED
SR 15
SR 14
C Ø
SC
SP
COSP
PCE
CSC
FE
8 BIT
16 SECT.
OS
12 BIT
8 BW
12 BW
I 16 SECT
16 SECT
C 2
SLC100
ISLC100
ISLC200
ENSLC(N)
K1 74153
+5V
1K
1K (4 PLACES)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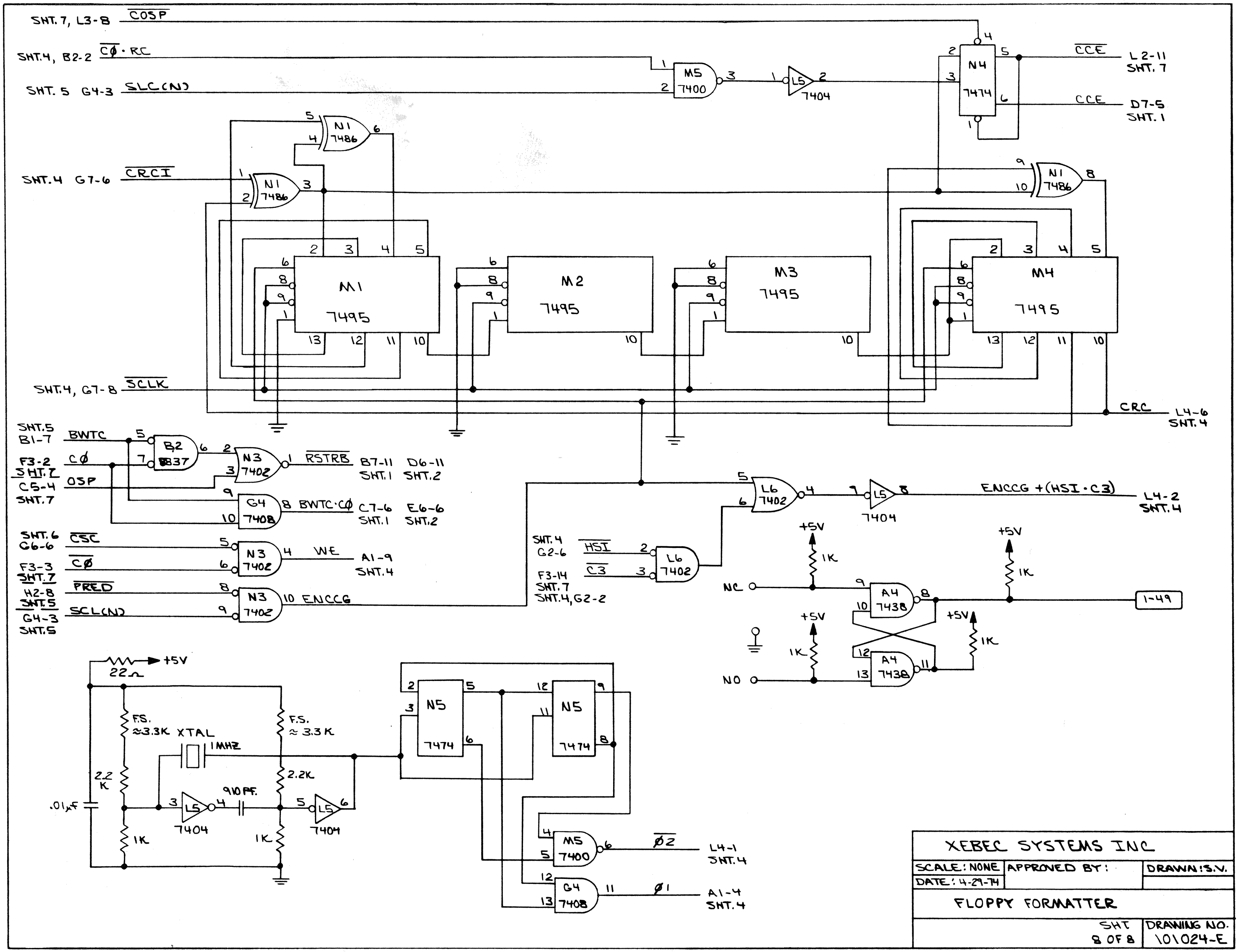
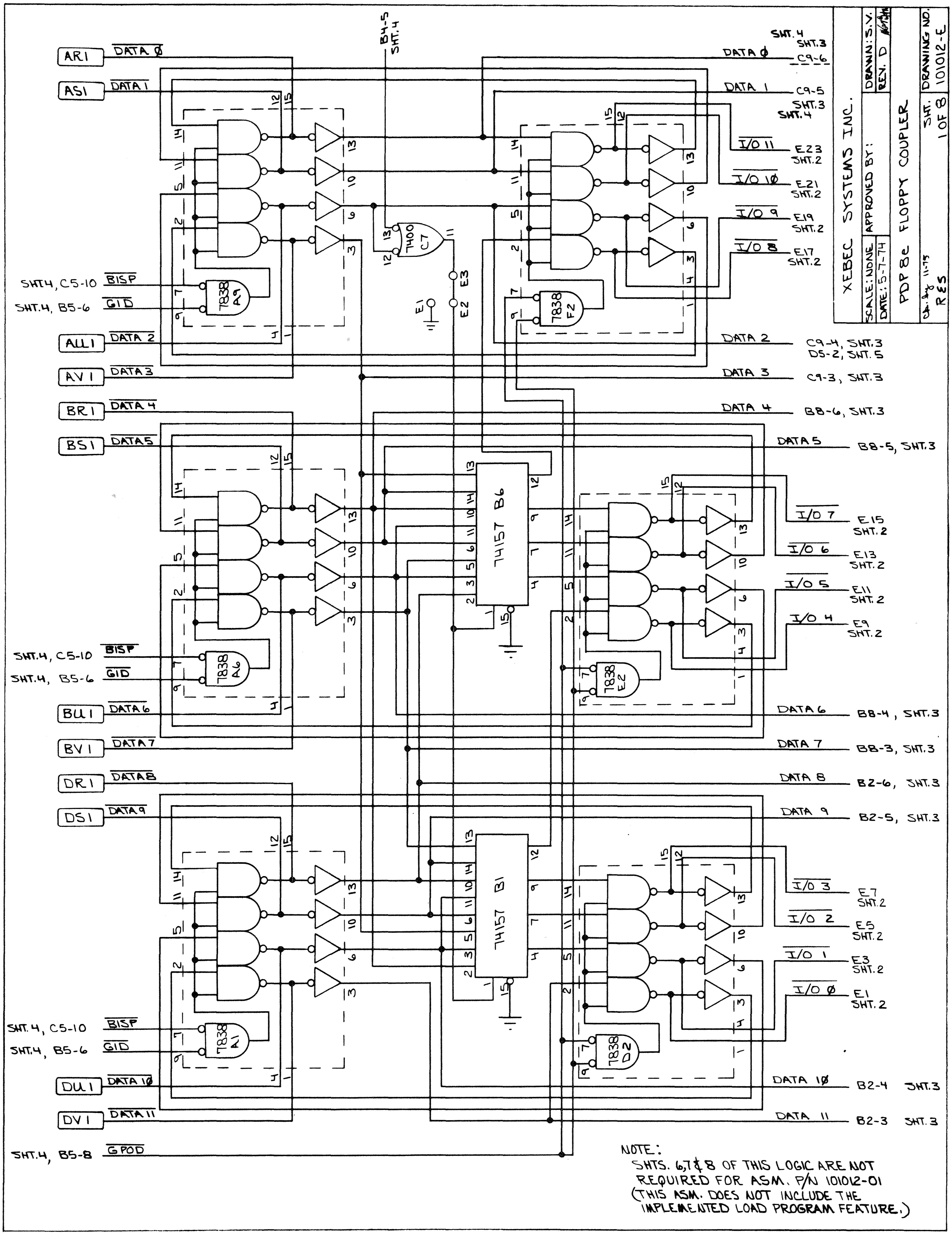
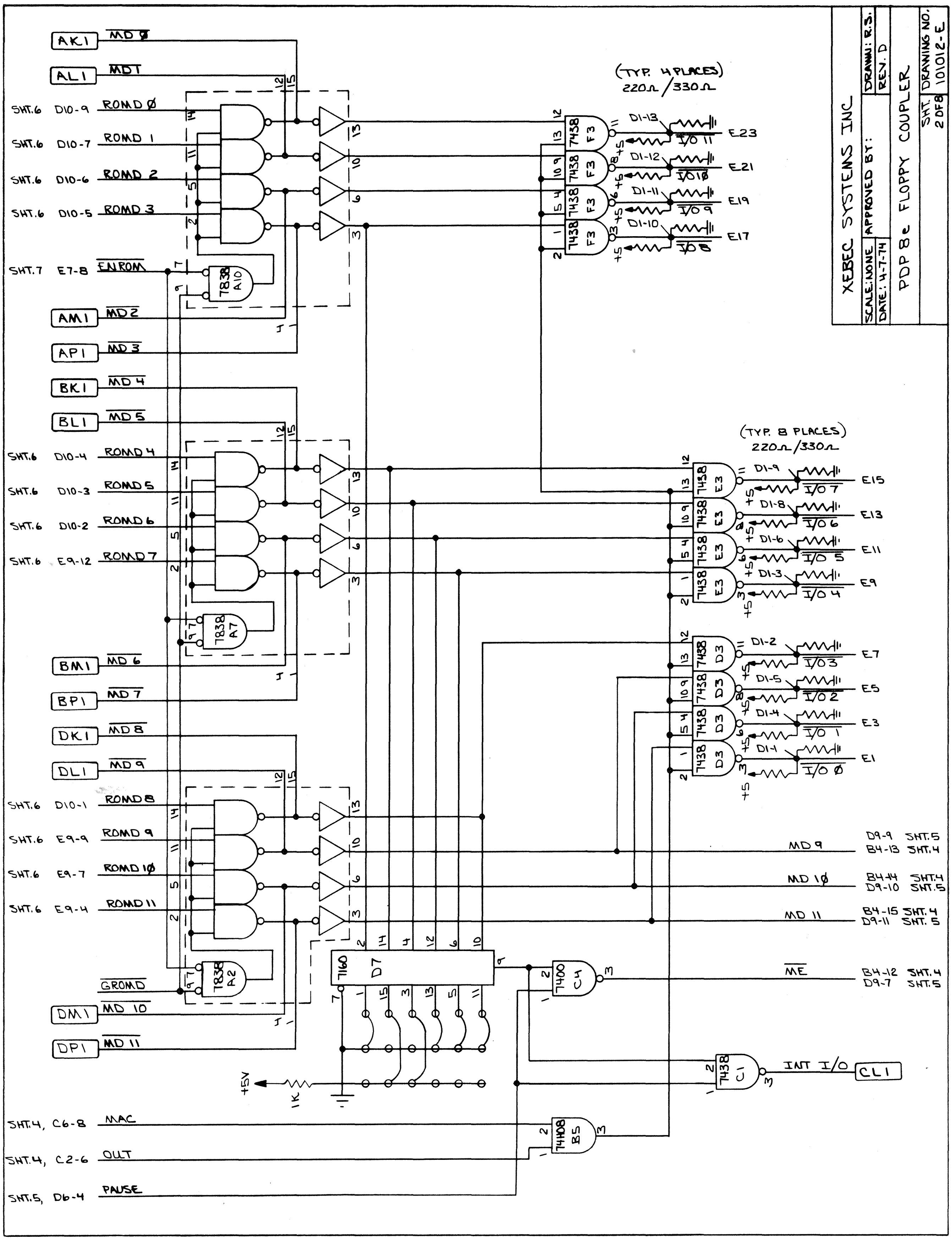
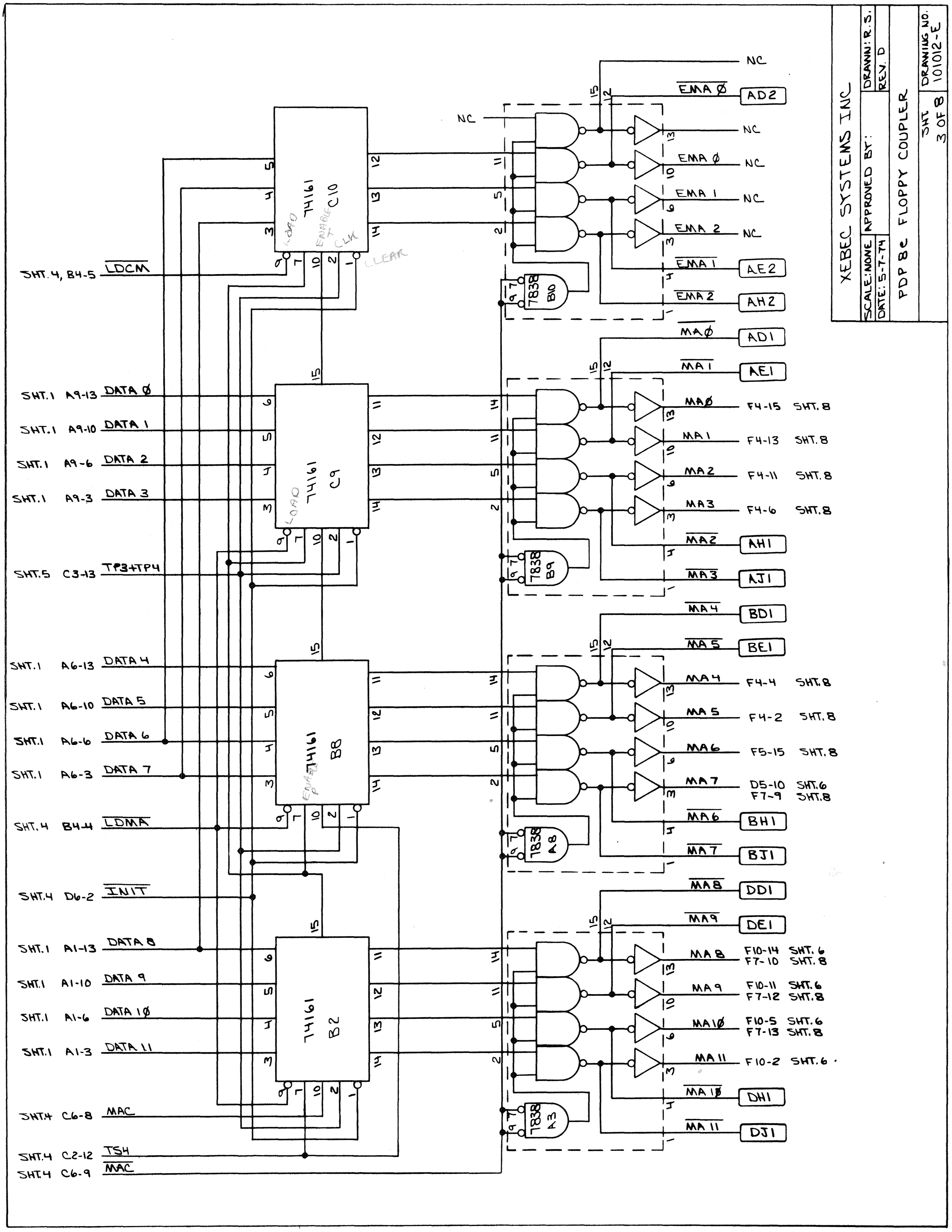
SHT.6, B2-10 RDY
SHT.6, H3-8 WPE
SHT.6, H5-2 TOE
SHT.6, G6-8 FE
SHT.7, K4-8 RE
SHT.6, H2-5 PCE
SHT.8, N4-5 CCE
SHT.7, F3-7 C1
SHT.7, F3-2 CØ
SHT.5, G4-3 SLC(N)
SHT.5, C1-15 LSLCTC
SHT.7, F3-3 CØ
L2 7430
B4 7438
H6 7404
L3 7400
L1 7451
G5 7420
H1 7404
+5V
220Ω
330Ω
A6-10
ERR
1-47
BUSY
1-45
A6-8
F6-9 SHT.3
BUSY K5-7 SHT.6
COSP G6-13 N4-4 SHT.6 SHT.8
INIT
1-33
C6-10
C5 8837
MCLR A1-13 SHT.4
MCLR
1-35 REGSEL
A6-5
C6-12
1-39 OSP
1-37 ISP
C6-13
REGSEL E1-2 D7-1 SHT.3 SHT.1
OSP N3-3 E1-1 K3-11 SHT.8 SHT.3 SHT.7
REGSEL B5-7, SHT.2 L6-9 SHT.7
ISP A7-9 B6-9 L6-8 SHT.1 SHT.2 SHT.7
SHT.4, G2-4 IFLG
K3 7402
SHT.5 D2-15 BWTC
C5-4 SHT.7 OSP
H5-12 SH.7 ISP
REG SEL H5-8 SHT.7
L6 7402
ISP. REG SEL
200 Pf.
F1-3 SHT.5 GPRE + PRED
G4 7408
K4 7474
C6-11
FLAG
1-43
RE D7-14 SHT.1
RE L2-5 SHT.7
G1 7404
COSP G2-12 SHT.3
A5-10 SHT.1 I/O 6
A4 7438
STRB 2-45
RES 2-43
A5-13 SHT.1 I/O 7
A7-10 SHT.1 I/O 2
A7-6 SHT.1 I/O 1
A7-3 SHT.1 I/O Ø
F3 74175
C3 SHT.4 G2-2
C2 K1-10 SHT.6
H3-2, SHT.5
C1 L3-1 K3-8, L3-1 SHT.7
CØ B2-7, SHT.4 SH.6, H3-10 E1-4 SHT.5 SHT, L3-2
CØ B7-10 D6-10 G7-4 D1-9 L1-4, SHT.7
SHT.1 SHT.2 SHT.4 SHT.5
N3-6, SHT.8
G5-4 SH.6
OUT
1-41

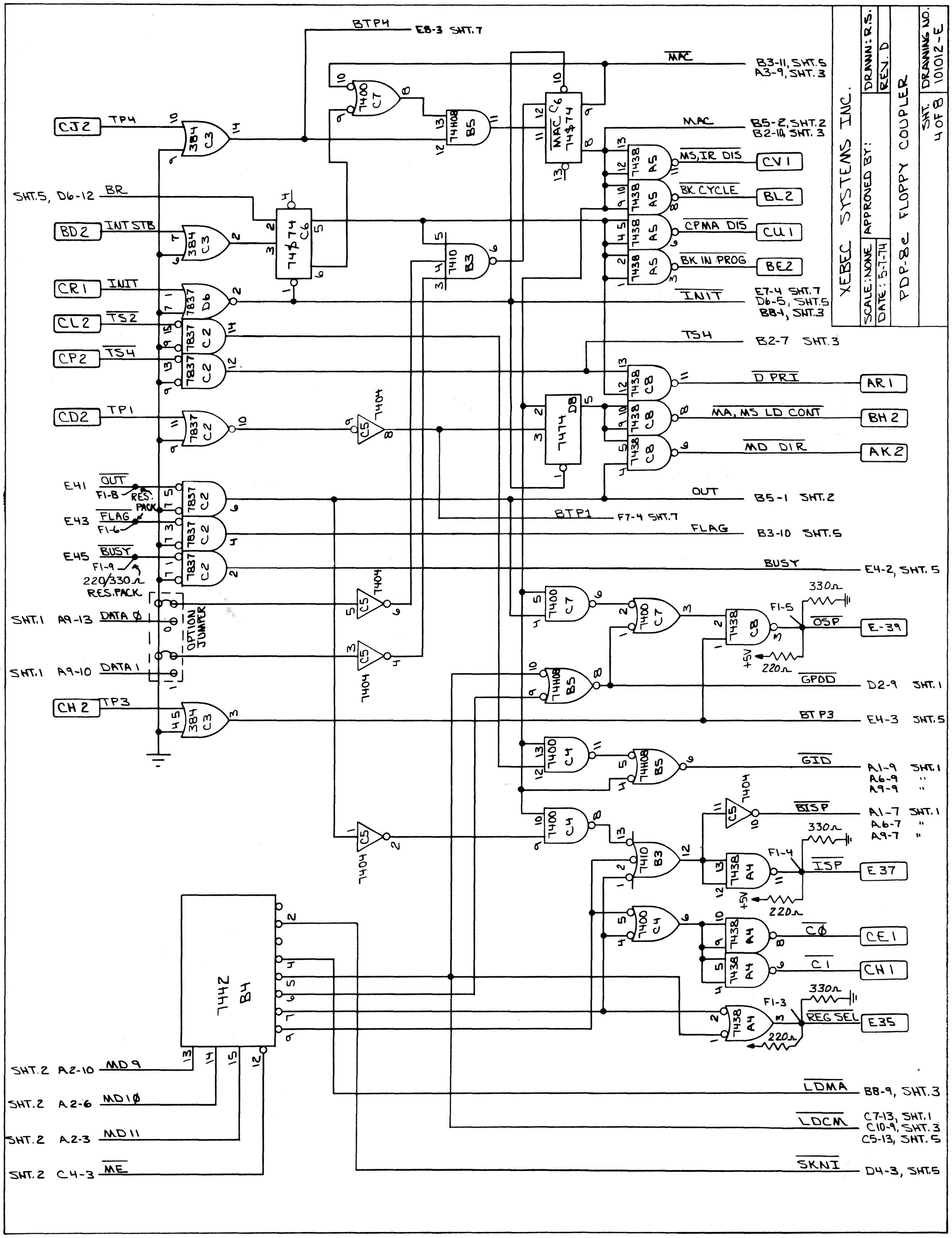

SHT. 7, L3-8 COSP
SHT.4, B2-2 CØ · RC
SHT. 5 G4-3 SLC(N)
SHT.4 G7-6 CRCI
SHT.4, G7-8 SCLK
M5 7400
L5 7404
N4 7474
CCE L2-11 SHT. 7
CCE D7-5 SHT. 1
N1 7486
M1 7495
M2 7495
M3 7495
M4 7495
CRC L4-6 SHT. 4
SHT.5 B1-7 BWTC
F3-2 SHT.7 CØ
C5-4 SHT.7 OSP
B2 8837
N3 7402
RSTRB B7-11 SHT.1 D6-11 SHT.2
G4 7408
BWTC·CØ C7-6 SHT.1 E6-6 SHT.2
SHT.6 G6-6 CSC
F3-3 SHT.7 CØ
H2-8 SHT.5 PRED
G4-3 SHT.5 SCL(N)
WE A1-9 SHT.4
ENCCG
L6 7402
ENCCG + (HSI · C3) L4-2 SHT.4
SHT.4 G2-6 HSI
F3-14 SHT.7 C3
SHT.4, G2-2
+5V
1K
NC
NO
A4 7438
1-49
22Ω
F.S. ≈3.3K
XTAL 1MHZ
2.2K
910PF.
.01µF
N5 7474
M5 7400
Ø2 L4-1 SHT.4
Ø1 A1-4 SHT.4
XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY:
DRAWN: S.V.
DATE: 4-29-74
FLOPPY FORMATTER
SHT 8 OF 8
DRAWING NO. 101024-E

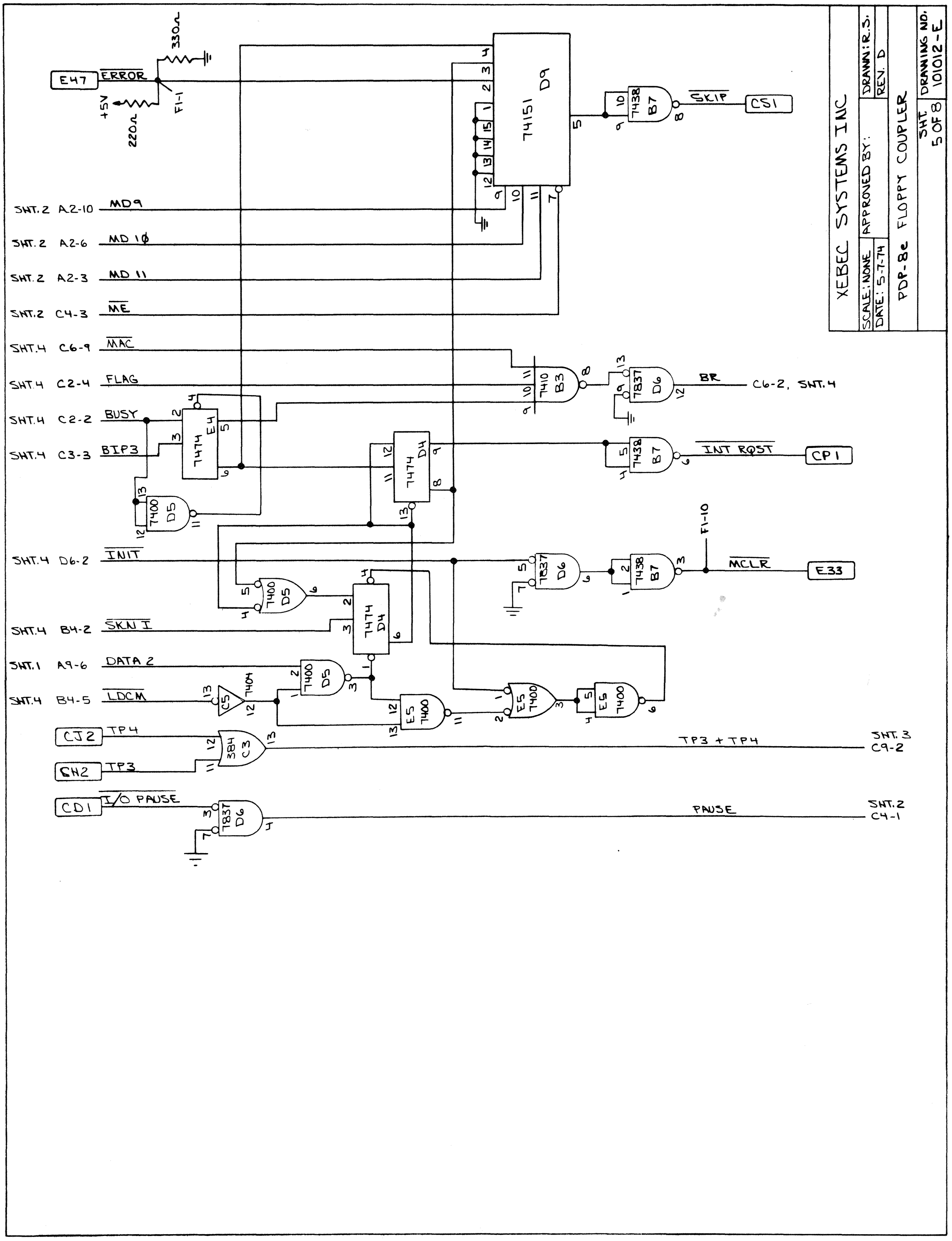

XEBEC SYSTEMS INC.
DRAWN: S.V.
REV. D
APPROVED BY:
SCALE: NONE
DATE: 5-7-74
PDP 8e FLOPPY COUPLER
SHT. 1 OF 8
DRAWING NO. 101012-E
RES
AR1 DATA Ø
AS1 DATA 1
AL1 DATA 2
AV1 DATA 3
BR1 DATA 4
BS1 DATA 5
BU1 DATA 6
BV1 DATA 7
DR1 DATA 8
DS1 DATA 9
DU1 DATA 1Ø
DV1 DATA 11
SHT.4, C5-10 BISP
SHT.4, B5-6 GID
SHT.4, B5-8 GPOD
B4-5 SHT.4
7400 C7
7838 A9
7838 F2
7838 A6
7838 E2
7838 A1
7838 D2
74157 B6
74157 B1
E1
E2
E3
DATA Ø C9-6 SHT.4 SHT.3
DATA 1 C9-5 SHT.3 SHT.4
I/O 11 E23 SHT.2
I/O 1Ø E21 SHT.2
I/O 9 E19 SHT.2
I/O 8 E17 SHT.2
DATA 2 C9-4, SHT.3 D5-2, SHT.5
DATA 3 C9-3, SHT.3
DATA 4 B8-6, SHT.3
DATA 5 B8-5, SHT.3
I/O 7 E15 SHT.2
I/O 6 E13 SHT.2
I/O 5 E11 SHT.2
I/O 4 E9 SHT.2
DATA 6 B8-4, SHT.3
DATA 7 B8-3, SHT.3
DATA 8 B2-6, SHT.3
DATA 9 B2-5, SHT.3
I/O 3 E7 SHT.2
I/O 2 E5 SHT.2
I/O 1 E3 SHT.2
I/O Ø E1 SHT.2
DATA 1Ø B2-4 SHT.3
DATA 11 B2-3 SHT.3
NOTE:
SHTS. 6,7 & 8 OF THIS LOGIC ARE NOT REQUIRED FOR ASM. P/N 101012-01 (THIS ASM. DOES NOT INCLUDE THE IMPLEMENTED LOAD PROGRAM FEATURE.)

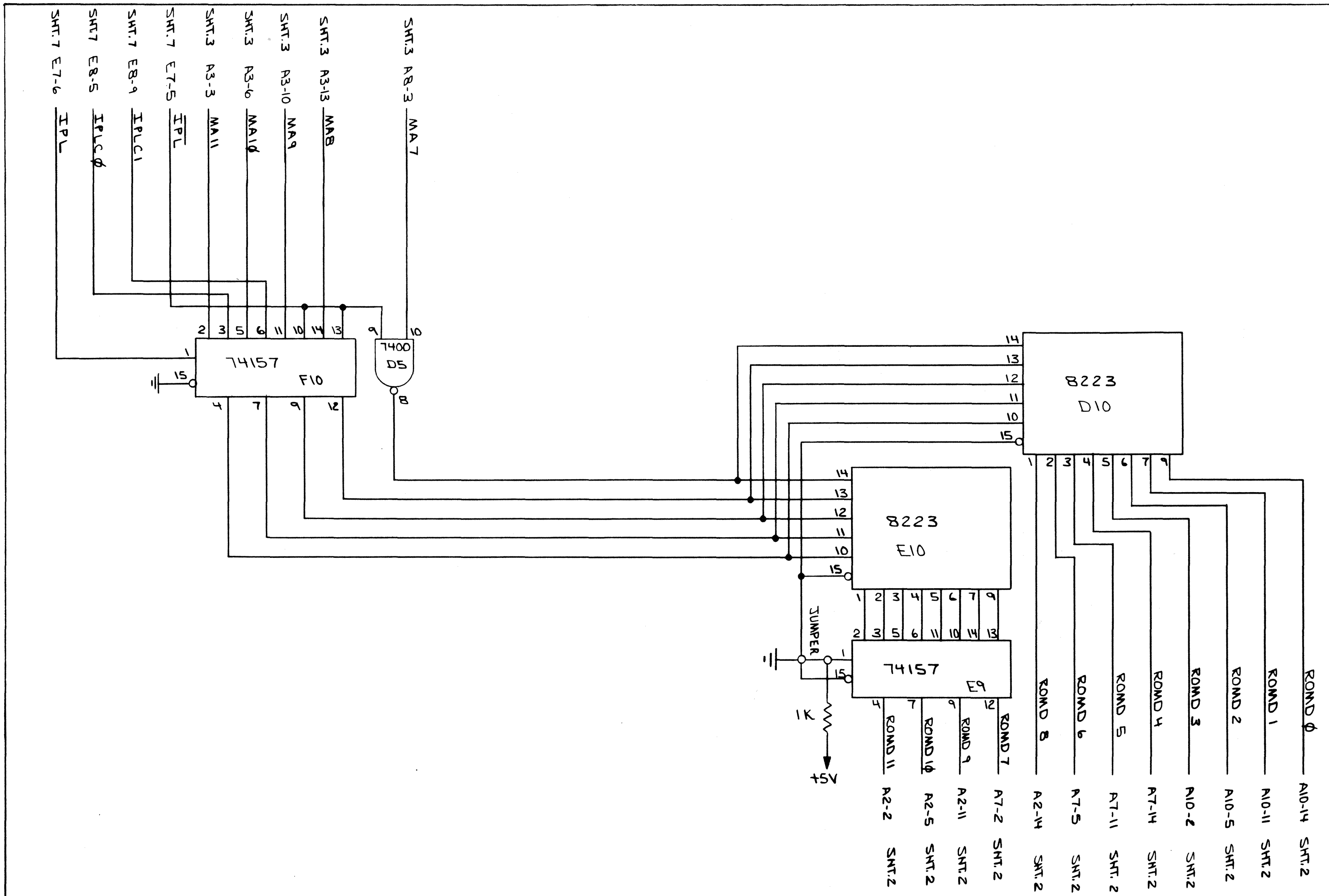

XEBEC SYSTEMS INC
DRAWN: R.S.
REV. D
APPROVED BY:
SCALE: NONE
DATE: 4-7-74
PDP 8e FLOPPY COUPLER
SHT. 2 OF 8
DRAWING NO. 101012-E
(TYP. 4 PLACES) 220Ω/330Ω
(TYP. 8 PLACES) 220Ω/330Ω
AK1 MD Ø
AL1 MD1
SHT.6 D10-9 ROMD Ø
SHT.6 D10-7 ROMD 1
SHT.6 D10-6 ROMD 2
SHT.6 D10-5 ROMD 3
SHT.7 E7-8 ENROM
AM1 MD2
AP1 MD3
BK1 MD4
BL1 MD5
SHT.6 D10-4 ROMD4
SHT.6 D10-3 ROMD5
SHT.6 D10-2 ROMD6
SHT.6 E9-12 ROMD7
BM1 MD6
BP1 MD7
DK1 MD8
DL1 MD9
SHT.6 D10-1 ROMD8
SHT.6 E9-9 ROMD 9
SHT.6 E9-7 ROMD 10
SHT.6 E9-4 ROMD11
GROMD
DM1 MD 10
DP1 MD 11
SHT.4, C6-8 MAC
SHT.4, C2-6 OUT
SHT.5, D6-4 PAUSE
E23 E21 E19 E17
E15 E13 E11 E9
E7 E5 E3 E1
MD 9 D9-9 SHT.5 B4-13 SHT.4
MD 10 B4-14 SHT.4 D9-10 SHT.5
MD 11 B4-15 SHT.4 D9-11 SHT.5
ME B4-12 SHT.4 D9-7 SHT.5
INT I/O CL1
+5V 1K



XEBEC SYSTEMS INC
SCALE: NONE
DATE: 5-7-74
APPROVED BY:
DRAWN: R.S.
REV. D
PDP 8e FLOPPY COUPLER
SHT. 3 OF 8
DRAWING NO. 101012-E
74161 C10
74161 C9
74161 B8
74161 B2
7838 B10
7838 B9
7838 A8
7838 A3
LOAD
ENABLE
CLK
CLEAR
SHT. 4, B4-5 LDCM
SHT. 1 A9-13 DATA Ø
SHT. 1 A9-10 DATA 1
SHT. 1 A9-6 DATA 2
SHT. 1 A9-3 DATA 3
SHT. 5 C3-13 TP3+TP4
SHT. 1 A6-13 DATA 4
SHT. 1 A6-10 DATA 5
SHT. 1 A6-6 DATA 6
SHT. 1 A6-3 DATA 7
SHT. 4 B4-4 LDMA
SHT. 4 D6-2 INIT
SHT. 1 A1-13 DATA 8
SHT. 1 A1-10 DATA 9
SHT. 1 A1-6 DATA 1Ø
SHT. 1 A1-3 DATA 11
SHT. 4 C6-8 MAC
SHT. 4 C2-12 TS4
SHT. 4 C6-9 MAC
NC
EMA Ø AD2
EMA Ø NC
EMA 1 NC
EMA 2 NC
EMA 1 AE2
EMA 2 AH2
MA Ø AD1
MA 1 AE1
MAØ F4-15 SHT. 8
MA 1 F4-13 SHT. 8
MA 2 F4-11 SHT. 8
MA 3 F4-6 SHT. 8
MA 2 AH1
MA 3 AJ1
MA 4 BD1
MA 5 BE1
MA 4 F4-4 SHT. 8
MA 5 F4-2 SHT. 8
MA 6 F5-15 SHT. 8
MA 7 D5-10 SHT. 6
F7-9 SHT. 8
MA 6 BH1
MA 7 BJ1
MA 8 DD1
MA 9 DE1
MA 8 F10-14 SHT. 6
F7-10 SHT. 8
MA 9 F10-11 SHT. 6
F7-12 SHT. 8
MA 1Ø F10-5 SHT. 6
F7-13 SHT. 8
MA 11 F10-2 SHT. 6
MA 1Ø DH1
MA 11 DJ1

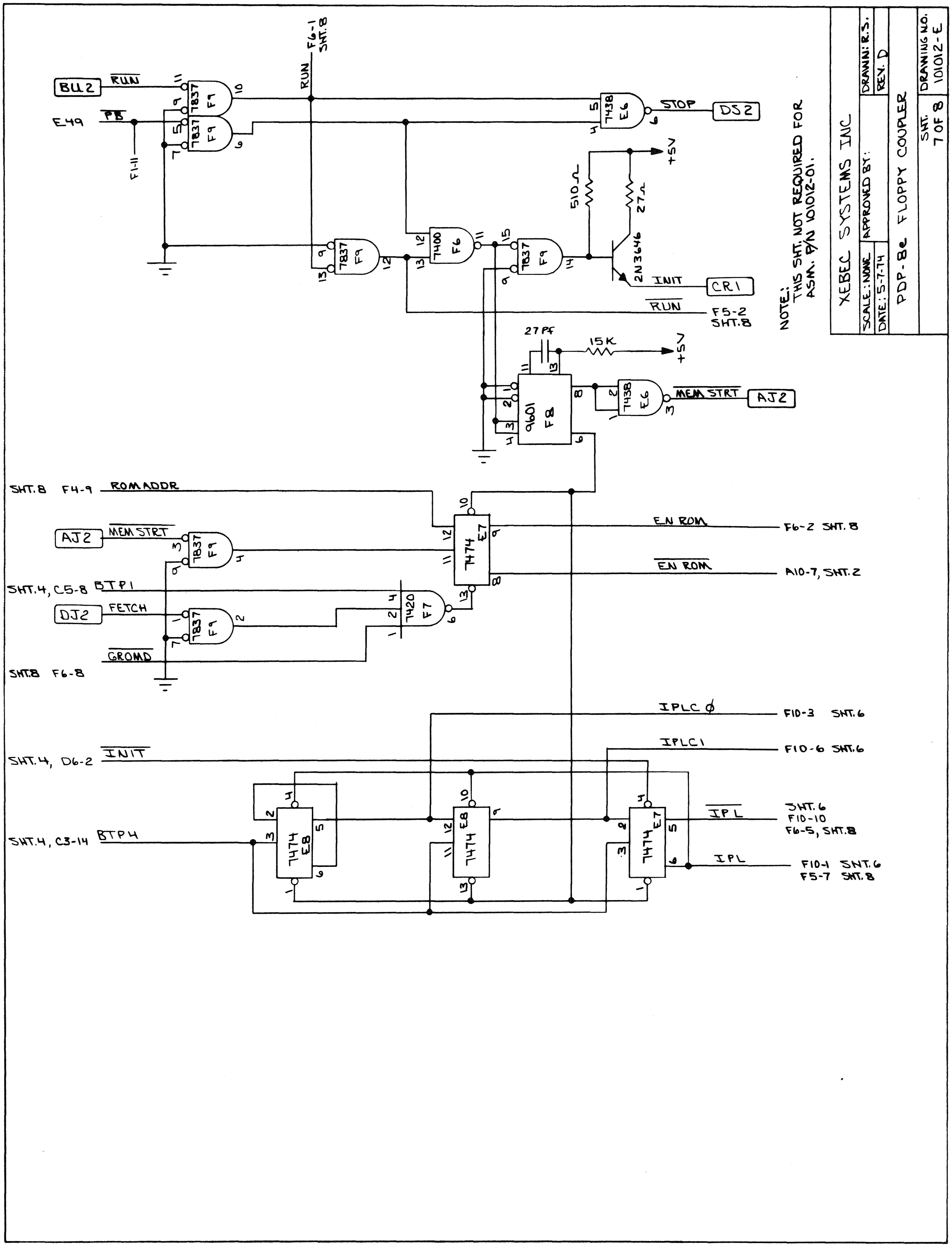

XEBEC SYSTEMS INC.
DRAWN: R.S.
REV. D
APPROVED BY:
SCALE: NONE
DATE: 5-7-74
PDP-8e FLOPPY COUPLER
SHT. 4 OF 8
DRAWING NO. 101012-E
BTPH E8-3 SHT.7
MAC
B3-11, SHT.5
A3-9, SHT.3
MAC
B5-2, SHT.2
B2-10, SHT.3
MS, IR DIS
CV1
BK CYCLE
BL2
CPMA DIS
CU1
BK IN PROG
BE2
INIT
E7-4 SHT.7
D6-5, SHT.5
B8-4, SHT.3
TS4
B2-7 SHT.3
D PRI
AR1
MA, MS LD CONT
BH2
MD DIR
AK2
OUT
B5-1 SHT.2
BTP1 F7-4 SHT.7
FLAG
B3-10 SHT.5
BUSY
E4-2, SHT.5
OSP
E-39
GPDD
D2-9 SHT.1
BTP3
E4-3 SHT.5
GID
A1-9 SHT.1
A6-9
A9-9
BISP
A1-7 SHT.1
A6-7
A9-7
ISP
E37
CØ
CE1
C1
CH1
REG SEL
E35
LDMA
B8-9, SHT.3
LDCM
C7-13, SHT.1
C10-9, SHT.3
C5-13, SHT.5
SKNI
D4-3, SHT.5
CJ2
TP4
SHT.5, D6-12
BR
BD2
INT STB
CR1
INIT
CL2
TS2
CP2
TS4
CD2
TP1
E41
OUT
F1-8
RES. PACK
E43
FLAG
F1-6
E45
BUSY
F1-9
220/330Ω RES. PACK
SHT.1 A9-13
DATA Ø
OPTION JUMPER
SHT.1 A9-10
DATA 1
CH2
TP3
SHT.2 A2-10
MD9
SHT.2 A2-6
MD10
SHT.2 A2-3
MD11
SHT.2 C4-3
ME
7442 B4
330Ω
220Ω
+5V
F1-5
F1-4
F1-3


XEBEC SYSTEMS INC
SCALE: NONE
DATE: 5-7-74
APPROVED BY:
DRAWN: R.S.
REV. D
PDP-8e FLOPPY COUPLER
SHT. 5 OF 8
DRAWING NO. 101012-E
E47
ERROR
330Ω
220Ω
+5V
F1-1
74151 D9
7438 B7
SKIP
CS1
SHT.2 A2-10 MD9
SHT.2 A2-6 MD 10
SHT.2 A2-3 MD 11
SHT.2 C4-3 ME
SHT.4 C6-9 MAC
SHT.4 C2-4 FLAG
SHT.4 C2-2 BUSY
SHT.4 C3-3 BIP3
7410 B3
7837 D6
BR
C6-2, SHT.4
7474 E4
7474 D4
7400 D5
INT RQST
CP1
F1-10
SHT.4 D6-2 INIT
MCLR
E33
SHT.4 B4-2 SKN I
SHT.1 A9-6 DATA 2
SHT.4 B4-5 LDCM
7404 C5
7400 E5
CJ2 TP4
SH2 TP3
384 C3
TP3 + TP4
SHT. 3 C9-2
CD1 I/O PAUSE
PAUSE
SHT.2 C4-1

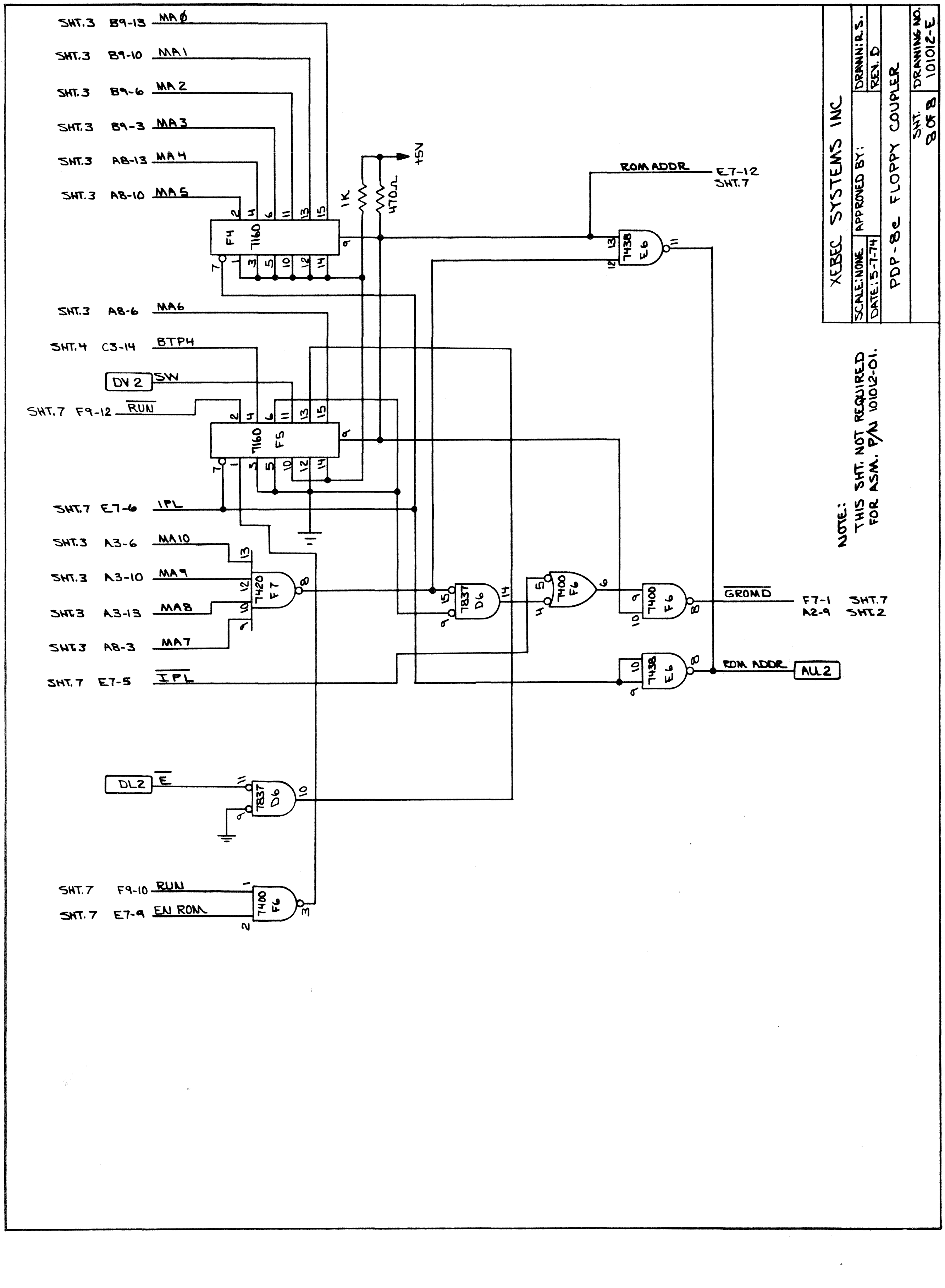


NOTE:
THIS SHT. NOT REQUIRED FOR
ASM. P/N 101012-01.

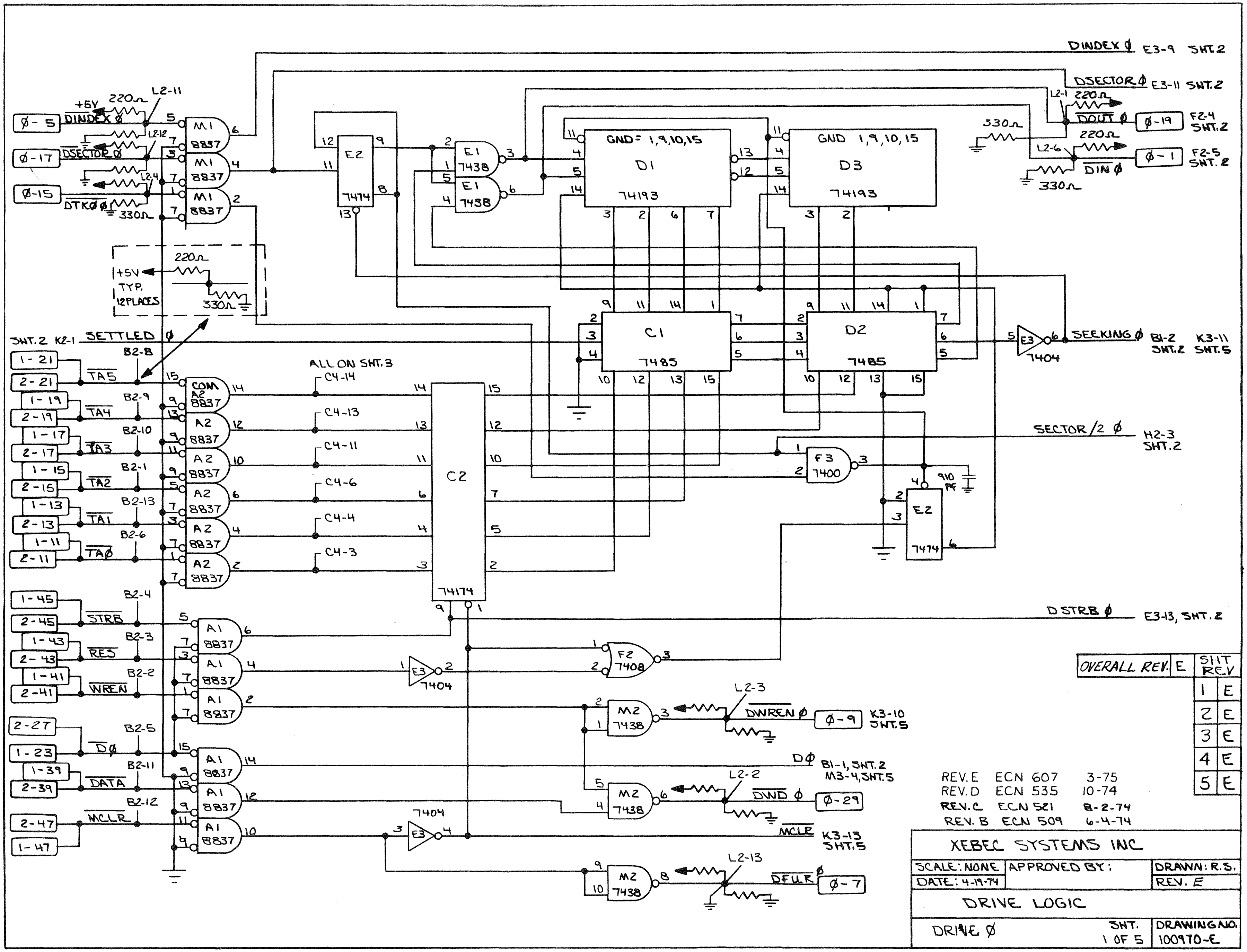
XEBEC SYSTEMS INC		
SCALE: NONE	APPROVED BY:	DRAWN: R.S.
DATE: 5-7-74		REV. D
PDP-8e FLOPPY COUPLER		
	SHT. 6 OF 8	DRAWING NO. 101012-E

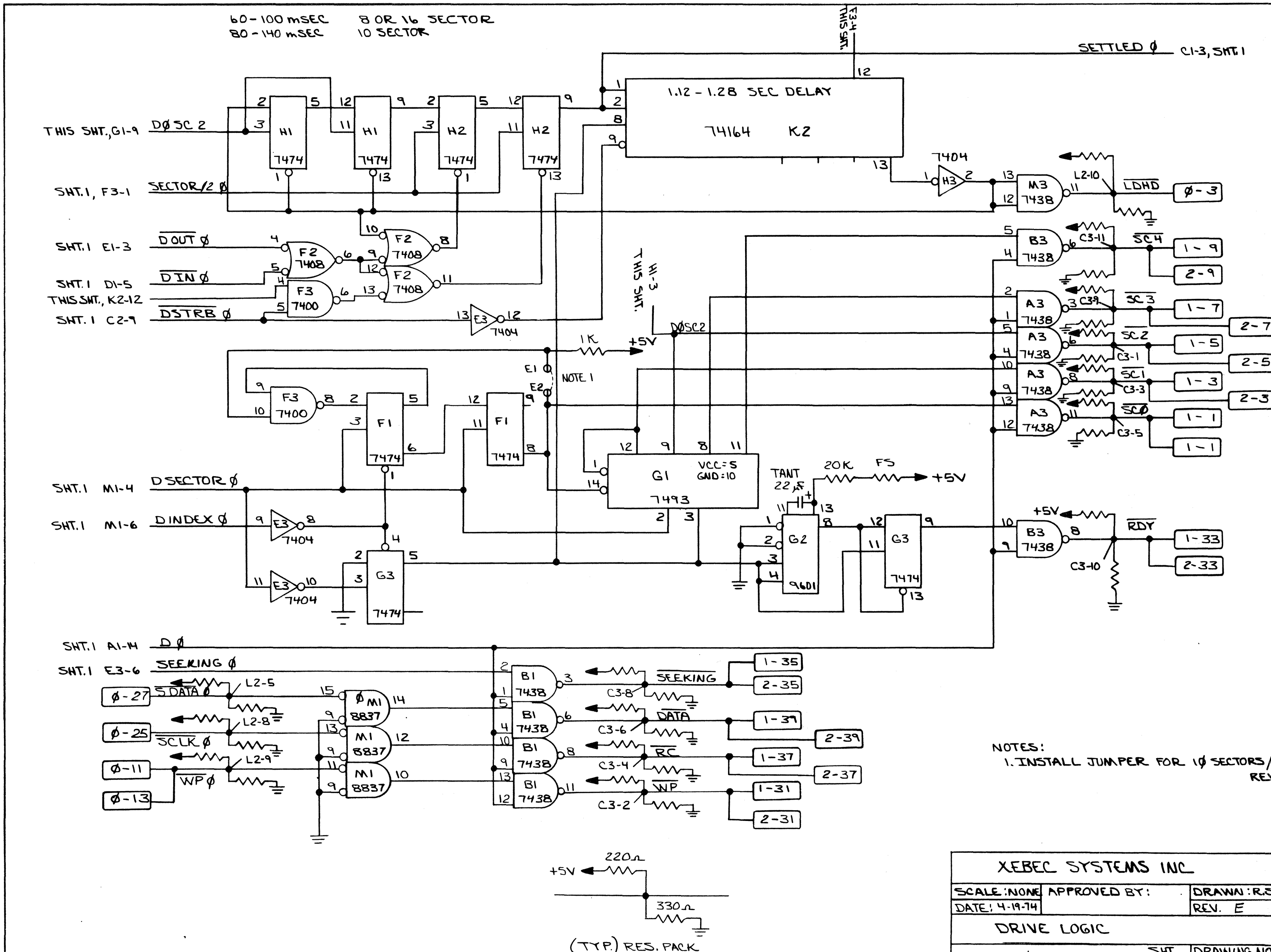


BU2
RUN
E49
PB
F1-11
RUN F6-1 SHT.8
7837 F9
7438 E6
STOP
DS2
+5V
510Ω
27Ω
7400 F6
2N3646
INIT
CR1
RUN
F5-2 SHT.8
27PF
15K
9601 F8
MEM STRT
AJ2
SHT.8 F4-9 ROMADDR
7474 E7
EN ROM
F6-2 SHT.8
EN ROM
A10-7, SHT.2
SHT.4, C5-8 BTP1
DJ2
FETCH
7420 F7
GROMD
SHT.8 F6-8
IPLC Ø
F10-3 SHT.6
IPLC1
F10-6 SHT.6
SHT.4, D6-2 INIT
SHT.4, C3-14 BTP4
7474 E8
IPL
SHT.6 F10-10 F6-5, SHT.8
IPL
F10-1 SHT.6 F5-7 SHT.8
NOTE: THIS SHT. NOT REQUIRED FOR ASM. P/N 101012-01.
XEBEC SYSTEMS INC
DRAWN: R.S.
REV. D
SCALE: NONE
APPROVED BY:
DATE: 5-7-74
PDP-8e FLOPPY COUPLER
SHT. 7 OF 8
DRAWING NO. 101012-E



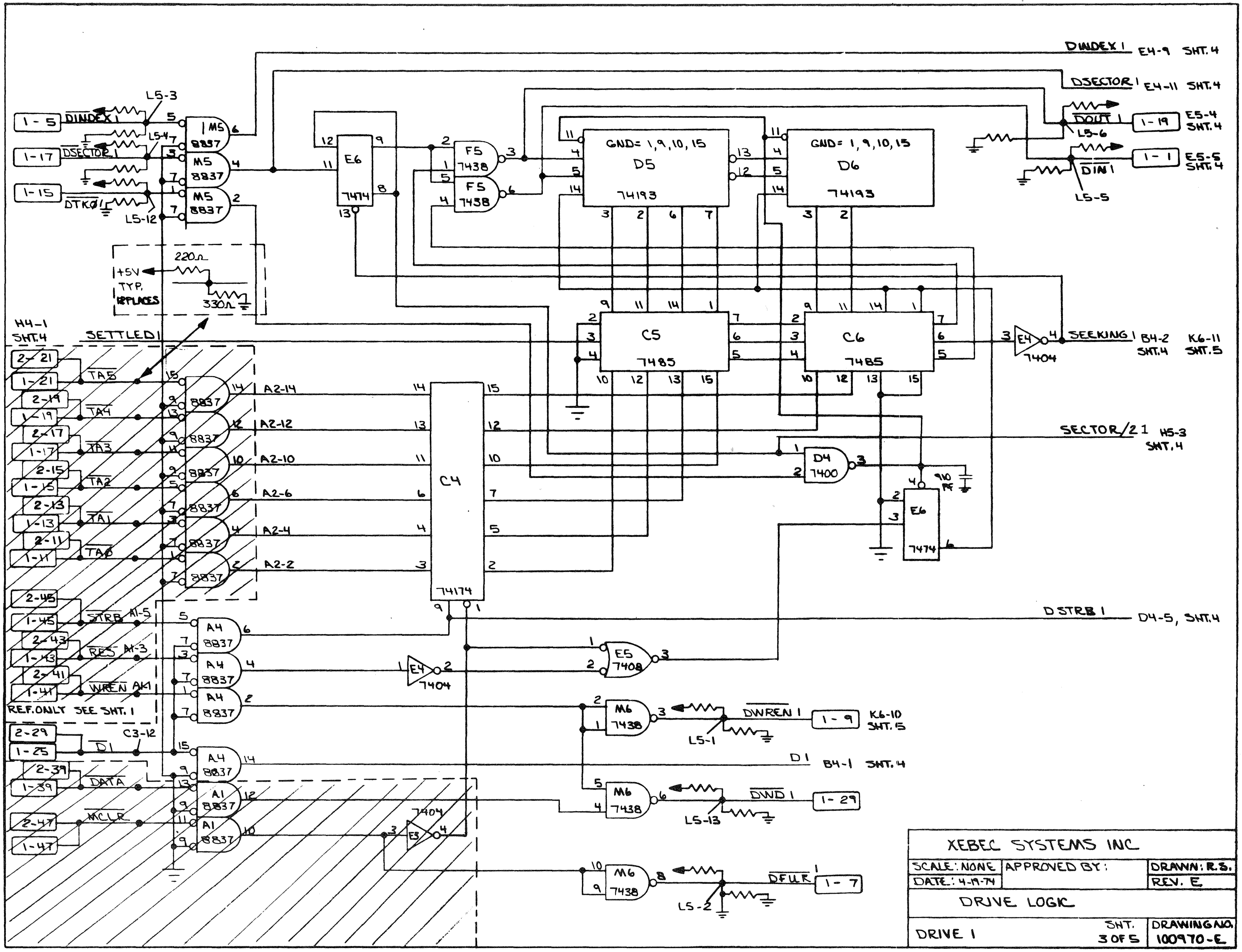
XEBEC SYSTEMS INC
SCALE: NONE
DATE: 5-7-74
APPROVED BY:
DRAWN: R.S.
REV. D
PDP-8e FLOPPY COUPLER
SHT. 8 OF 8
DRAWING NO. 101012-E
NOTE:
THIS SHT. NOT REQUIRED FOR ASM. P/N 101012-01.
SHT.3 B9-13 MAØ
SHT.3 B9-10 MA1
SHT.3 B9-6 MA2
SHT.3 B9-3 MA3
SHT.3 A8-13 MA4
SHT.3 A8-10 MA5
SHT.3 A8-6 MA6
SHT.4 C3-14 BTP4
DV2 SW
SHT.7 F9-12 RUN
SHT.7 E7-6 IPL
SHT.3 A3-6 MA10
SHT.3 A3-10 MA9
SHT.3 A3-13 MA8
SHT.3 A8-3 MA7
SHT.7 E7-5 IPL
DL2 E
SHT.7 F9-10 RUN
SHT.7 E7-9 EN ROM
+5V
1K
470Ω
F4 7160
F5 7160
7438 E6
7420 F7
7837 D6
7400 F6
ROM ADDR E7-12 SHT.7
GROMD F7-1 SHT.7 A2-9 SHT.2
ROM ADDR AL2


DINDEX Ø E3-9 SHT.2
DSECTOR Ø E3-11 SHT.2
DOUT Ø
Ø-19 F2-4 SHT.2
DIN Ø
Ø-1 F2-5 SHT.2
+5V 220Ω L2-11
Ø-5 DINDEX Ø
Ø-17 DSECTOR Ø
Ø-15 DTKØØ
330Ω
M1 8837
E2 7474
E1 7438
GND= 1,9,10,15
D1 74193
GND 1,9,10,15
D3 74193
+5V TYP. 12PLACES 220Ω 330Ω
SHT.2 K2-1 SETTLED Ø
C1 7485
D2 7485
E3 7404
SEEKING Ø B1-2 SHT.2 K3-11 SHT.5
TA5 TA4 TA3 TA2 TA1 TAØ
COM A2 8837
ALL ON SHT.3
C4-14 C4-13 C4-11 C4-6 C4-4 C4-3
C2 74174
SECTOR/2 Ø H2-3 SHT.2
F3 7400
910 PF
DSTRB Ø E3-13, SHT.2
STRB RES WREN DØ DATA MCLR
A1 8837
F2 7408
M2 7438
DWREN Ø Ø-9 K3-10 SHT.5
DØ B1-1, SHT.2 M3-4, SHT.5
DWD Ø Ø-29
MCLR K3-13 SHT.5
DFLR Ø Ø-7
OVERALL REV. E
SHT REV 1 E 2 E 3 E 4 E 5 E
REV. E ECN 607 3-75
REV. D ECN 535 10-74
REV. C ECN 521 8-2-74
REV. B ECN 509 6-4-74
XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-19-74
REV. E
DRIVE LOGIC
DRIVE Ø
SHT. 1 OF 5
DRAWING NO. 100970-E

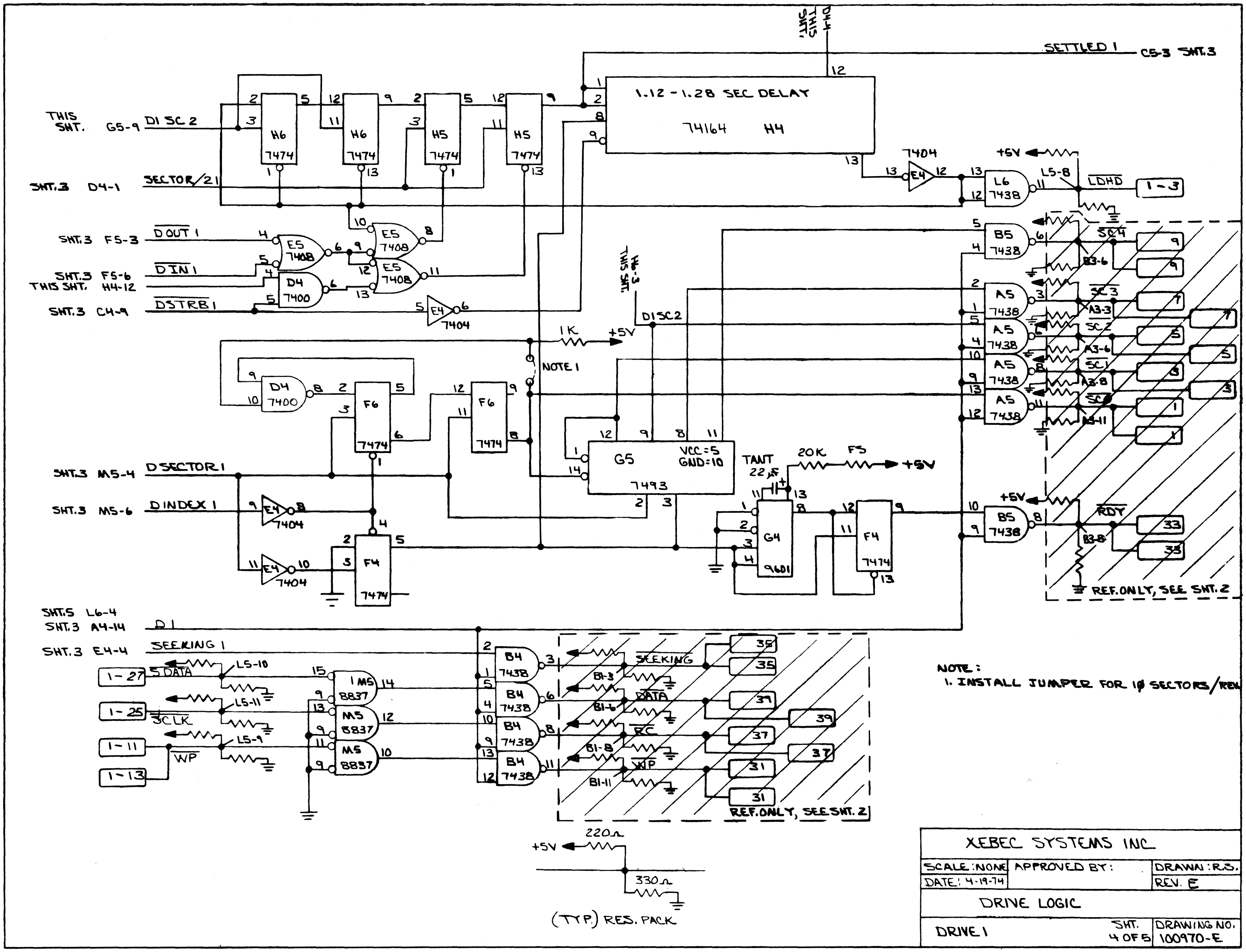


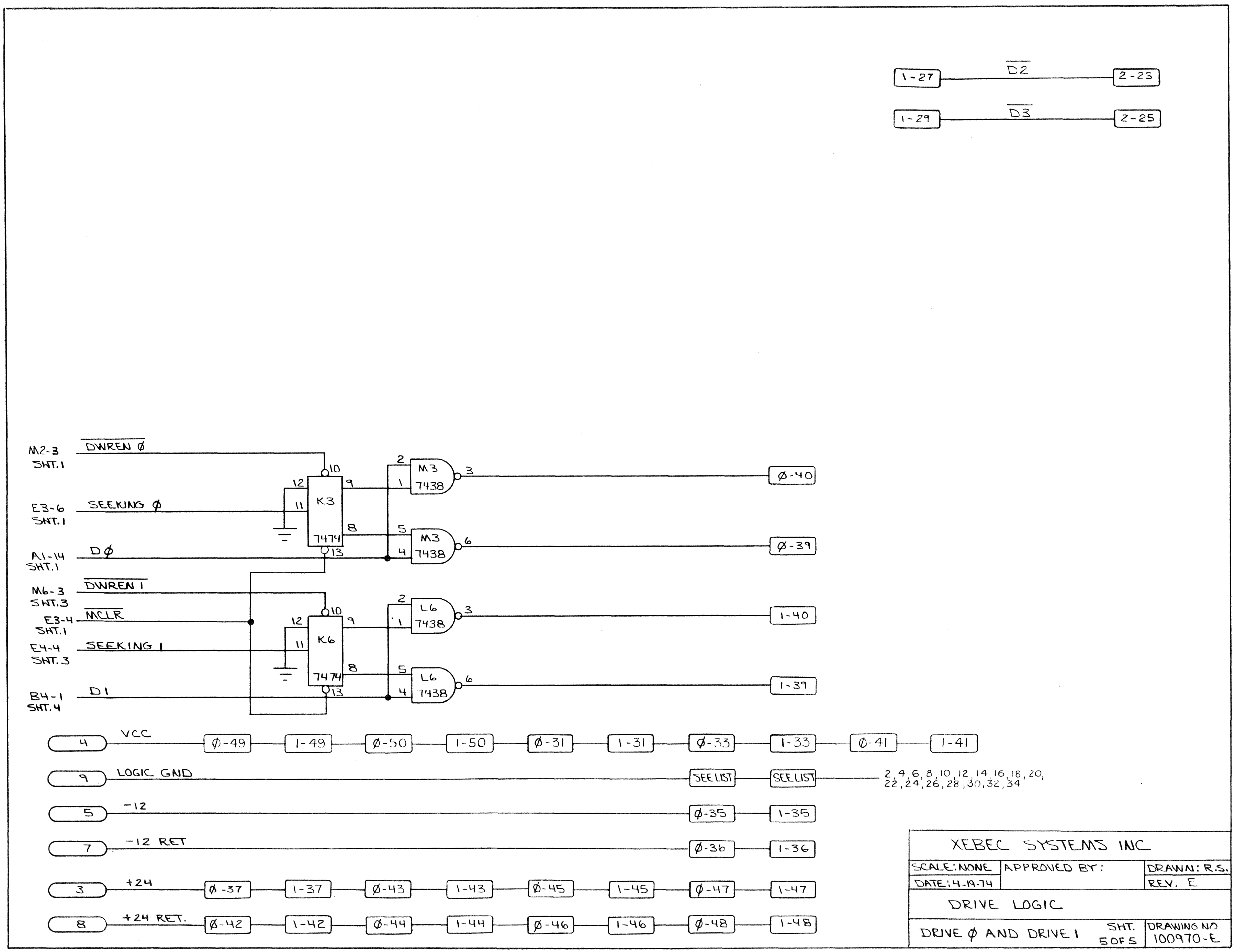
NOTES:
1. INSTALL JUMPER FOR 1Ø SECTORS/REV.

XEBEC SYSTEMS INC		
SCALE: NONE	APPROVED BY:	DRAWN: R.S.
DATE: 4-19-74		REV. E
DRIVE LOGIC		
DRIVE Ø	SHT. 2 OF 5	DRAWING NO. 100970-E



XEBEC SYSTEMS INC		
SCALE: NONE	APPROVED BY:	DRAWN: R.S.
DATE: 4-19-74		REV. E
DRIVE LOGIC		
DRIVE 1	SHT. 3 OF 5	DRAWING NO. 100970-E


1.12 - 1.28 SEC DELAY
74164 H4
SETTLED 1
C5-3 SHT.3
THIS SHT. D4-4
THIS SHT. G5-9 DISC 2
SHT.3 D4-1 SECTOR/2 1
SHT.3 F5-3 DOUT 1
SHT.3 F5-6 DIN 1
THIS SHT. H4-12
SHT.3 C4-9 DSTRB 1
H6 7474
H5 7474
E5 7408
D4 7400
E4 7404
L6 7438
L5-8
LDHD
1-3
+5V
B5 7438
A5 7438
SC4
SC3
SC2
SC1
SC0
B3-6
A3-3
A3-6
A3-8
A3-11
THIS SHT. H6-3
DISC2
1K
NOTE 1
F6 7474
G5 7493
VCC=5 GND=10
TANT 22μf
20K
FS
SHT.3 M5-4 DSECTOR 1
SHT.3 M5-6 DINDEX 1
F4 7474
G4 9601
RDY
B3-8
REF. ONLY, SEE SHT. 2
SHT.5 L6-4
SHT.3 A4-14 D1
SHT.3 E4-4 SEEKING 1
L5-10
L5-11
L5-9
SDATA
SCLK
WP
M5 8837
B4 7438
SEEKING
DATA
RC
B1-3
B1-6
B1-8
B1-11
REF. ONLY, SEE SHT. 2
NOTE:
1. INSTALL JUMPER FOR 10 SECTORS/REV
220Ω
330Ω
(TYP.) RES. PACK
XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-19-74
REV. E
DRIVE LOGIC
DRIVE 1
SHT. 4 OF 5
DRAWING NO. 100970-E


1-27
D2
2-23
1-29
D3
2-25
M2-3 SHT.1
DWREN Ø
E3-6 SHT.1
SEEKING Ø
A1-14 SHT.1
DØ
M6-3 SHT.3
DWREN 1
E3-4 SHT.1
MCLR
E4-4 SHT.3
SEEKING 1
B4-1 SHT.4
D1
K3 7474
K6 7474
M3 7438
L6 7438
Ø-40
Ø-39
1-40
1-39
4 VCC
Ø-49
1-49
Ø-50
1-50
Ø-31
1-31
Ø-33
1-33
Ø-41
1-41
9 LOGIC GND
SEE LIST
SEE LIST
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34
5 −12
Ø-35
1-35
7 −12 RET
Ø-36
1-36
3 +24
Ø-37
1-37
Ø-43
1-43
Ø-45
1-45
Ø-47
1-47
8 +24 RET.
Ø-42
1-42
Ø-44
1-44
Ø-46
1-46
Ø-48
1-48
XEBEC SYSTEMS INC
SCALE: NONE
APPROVED BY:
DRAWN: R.S.
DATE: 4-19-74
REV. E
DRIVE LOGIC
DRIVE Ø AND DRIVE 1
SHT. 5 OF 5
DRAWING NO 100970-E

XEBEC
SYSTEMS INCORPORATED

2985 KIFER ROAD, SANTA CLARA, CA. 95051 (408) 988-2550 TWX 910-338-0130