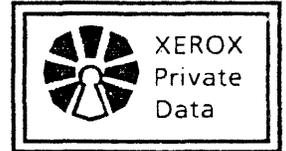


XEROX



Dove

System Requirements Specification

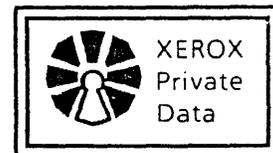
Version 1.0
October 2, 1984

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XEROX



Dove

System Requirements Specification

Version 1.0 -
October 2, 1984

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Scope

This document is an update of the earlier Daisy System Requirements Specification (SRS) (Ref. [1]) for a new family of workstation products, the first of which is expected to be launched August 1985. This SRS supercedes all the earlier versions and should serve as the baseline for further technical and marketing developments of this product line.

The "baseline workstation" of this family will serve as the Xerox entry-level workstation for office professionals, and will be used by other SBUs within Xerox as part of their systems. The workstation will execute Star software, and will provide essentially the same functionality as the 8010, except for those functions requiring devices that are not present on the new workstation.

The configurations defined here other than the baseline workstation will provide capabilities not currently offered on the 8010 workstation. These products may be available some time after the baseline product. It may be possible to define and to develop many other configurations not included in this document. The scope of the current development program is restricted to the configurations specified here.

This System Requirements Specification (SRS) responds to the draft Goals document generated by OSD Product Planning (Ref. [2]).

1.1 Introduction

Xerox requires a low-cost workstation to introduce prospective customers to the capabilities of Xerox hardware and software products and to be our entry-level workstation product into the expanding office automation market. In this dual role, this low-cost workstation will compete not only with other workstations but also with networked, high-end personal computers such as the Apple Lisa, IBM PC-XT, and IBM PC-AT.

The low-cost workstation should be expandable at extra cost, so that customers can enhance the functionality and/or performance of their workstations as they find new ways to increase their productivity using Xerox Network Systems resources.

The rationale for the selection and prioritization of product enhancements follows from the Xerox business definitions, objectives, and strategy. In general, the focus is on individual user needs and the needs of work groups sharing resources and information. The product strategy supports document-oriented features while recognizing that

requirements for electronic information access and manipulation are highly important to overall productivity.

First priority is our existing business of Integrated Office Systems for document-oriented professional work groups. Next priority is support of a possible new workstation business aimed at individual professional document-oriented users.

1.2 References

Miscellaneous

- [1] *Daisy System Requirements Specification*, Version 7.0, October 14, 1983.
- [2] *Goals for Office Systems Workstations Hardware*, Lynch *et al*, OSBU North:Xerox [Iron]<HDW Public> Workstations Goals Interpress, 3/24/83.
- [3] *Voice Box Functional Specification*, OSBU North:Xerox [Iron]<HDW Public> Voice Box Functional Specification.
- [4] *Critical Planning Assumptions for the OSD Workstation Product Line*, C. Henderson, March 3, 1983.
- [5] *Dandelion Hardware Manual*, March 1982.
- [6] *Dynamic RAM Status*, Van Cheong, Components and Reliability Engineering Technical Report, Xerox Electronics Division, March 1983.
- [7] *Multinational Ergonomic Requirements*, Gordon Young, OSBU North:Xerox [Iron]<HDW-Public>Ergonomics Memo, June 10, 1983.
- [8] *Fault Handling and Recovery*, Brian Inouye, OSBU North:Xerox [McKinley]<Diagnostics>Public>Diagnostics Methodology>Fault Handling and Recovery.
- [9] *Mesa Processor Principles of Operation*. Version 11.0, May 1984, Wick, John; 11.0 revisions by Daniels, Andrew.
- [10] *DOVE Program Diagnostics Goals*. Version Number 5: OSD Dove Diagnostic Team, May 18, 1984.
- [11] *DOVE Program Diagnostic Strategy*, Version Number 6: OSD Dove Diagnostic Team, September 4, 1984.
- [12] *PC Emulation on Dove Development Plan*, Version Number 1 (in preparation), Joe Binkley.
- [13] *PC Emulation on Dove Functional Specification*, Version Number 1 (in preparation), Joe Binkley.

Audible Noise Standards

- [14] *Xerox Corporate Environmental Health and Safety Manual*, Section 8.7.0, Audible Noise Limit Specification, effective date, March 1, 1982.
- [15] *IEEE Standard P802.3*, Rev. F, November 1984, IEEE Computer Society.

Electromagnetic Emissions Standards

- [16] US: *FCC Docket, 20780, Class B*.
- [17] RX: *VDE 0871, Class B, PVFG 1115 and VDE 0875 (82/499/EEC)*.
- [18] FX: *TBD*

Ergonomic Guidelines

- [19] *No. ZH 1/618 Edition 10.80 Safety Regulations for Display Workplaces in the Office Sector*.

Safety Standards

- [20] *UL 478, Underwriters Laboratories Standard, Electronic Data Processing*.
- [21] *CSA Standard C22. No. 154, Data Processing Equipment*.
- [22] *IEC Standard, Publication 435, Second Edition 1981, Safety of Data Processing Equipment*.



Competition

2.1 Environment

When Xerox announced the 8010 workstation, it was hailed as a revolution in office workstations and user friendliness in computer interfaces. Xerox was the acknowledged technology leader in office systems. As the result of a successful Ethernet campaign, Xerox also sensitized the marketplace to the advantages of networked office systems. Our overall marketing and public relations activity was so successful that there are now many competitors of our software, and the marketplace frequently hears of new "revolutions" in computer friendliness originating from our competitors.

Hardware and software cost reductions have enabled a proliferation of personal computers. Many companies have bought hundreds of low-end personal computers, mostly IBM PC's, or compatibles, in the quest for higher productivity. The productivity gains achieved, however, have hit a plateau because of the lack of efficient communication and sharing of resources.

The IBM 5150 Personal Computer and the IBM XT have become *de facto* standards in personal computers. Many companies are producing clones of these computers much as they are for the IBM mainframes. There are a large number of IBM PC-DOS programs which implement generic applications that could also be implemented on Star workstations. Even though these applications do not generally have the functionality or flexibility of the Star, or even of Apple's Lisa workstation, their presence in the office of our intended customers is an economic reality.

By the year 1985, there may be as many as 3,000,000 IBM PCs in the marketplace. Approximately 40% of these machines will be in the office, and we will have to coexist and interface gracefully with them. The recent introduction of the Ethernet hardware for the IBM-PC confirms this point.

New competitors are announcing alternatives to Xerox systems at increasing rates. These competitors are using hardware technology that is at least three years newer than the current Xerox 8010 hardware.

The computer interface model developed by Xerox is rapidly becoming an industry standard, however, and many of the systems on the market today exhibit facets of the Star

system. There is clearly an emphasis on the development of better user interfaces and seamless software packages such as exists in our system.

In the realm of user interfaces, the Apple systems, both Lisa and the Macintosh, are virtual copies of our interface, and many large software houses are working on user interfaces much like ours.

In the past year, there have been many releases and announcements about "integrated software packages." Although most of these are rather crude attempts, they indicate that our competition is becoming more sophisticated. The new 7/7 release for the Lisa is probably the most sophisticated of these packages.

Xerox conditioned the office systems marketplace about what functionality to expect of good office systems. The fair price for such a system has been clouded by the competition offering alternative definitions of office systems for professionals and of what determines professional productivity gains. Customers' willingness to pay for these systems has not been determined. The Xerox exposure is that our competitors are developing office systems with less function, at less cost and representing these as alternatives to Xerox hardware and software systems.

2.2 Motivation

Buyers of the low-cost workstation will expect the system to increase overall office productivity. Buyers will select the vendor who can best support the installation after it is delivered and installed. The successful system will be cost effective versus the existing systems and processes it replaces. The system must be cost competitive with similar systems in the market, although not necessarily the least expensive. Users desire strongly that this system be compatible with other information systems to which it must interface.

The buyer will be most concerned about:

- | | |
|--|--|
| <i>Ease of use:</i> | The user interface must be friendly and uncumbersome, and allow the user to feel in command of the system at all times. |
| <i>Ease of training requirements:</i> | The system must provide fast, accurate on-line and hardcopy training. |
| <i>Vendor strength / staying power:</i> | The user must feel that the vendor has a long-term commitment to the marketplace. Also, the user must perceive that the vendor has a long-term strategy for continued customer growth. |
| <i>System reliability:</i> | The user must feel the system is reliable versus other existing and/or competitive systems in the marketplace. |
| <i>Current and future Xerox compatibility:</i> | The system must be compatible with Xerox products both on and off the Ethernet. |
| <i>Non-Xerox compatibility:</i> | The user must feel secure that his investment has the capability to |

interface to non-Xerox devices, if advances in technology or user-specific needs arise that Xerox cannot meet.

*Ease of continued
growth:*

The user must feel the system allows for expansion into other needed areas of his environment. Additionally, the user must perceive incremental costs to be competitive in the marketplace.

The buyer will be influenced in the decision-making process by the perceived strengths and weaknesses of Xerox systems capabilities, overall market commitment, technical and application-oriented support capabilities, documentation and journals. In addition, the buyer will compare Xerox to its competitors in all aspects of the business.

It is absolutely critical to users that they can configure systems and workstations best suited to their particular applications, starting at the lowest possible cost. The users' overall goal will be to insure that systems purchased today can and will remain compatible with future office automation purchases.



Product description

Dove is the new "low-cost" office workstation product line for the time period through 1988. The foundation of the product line is a "baseline configuration" of the workstation. This baseline configuration can be upgraded with additional hardware to different configurations that have higher performance and capability. These machines will run Star at approximately the same performance level as the Dandelion machines. Configurations that include IBM-PC emulation (PCE) will allow the users to run many commercially available application programs.

Due to constraints of market entry, Dove will be introduced in two phases--a version known as Daybreak, based on an MSI implementation of the Mesa processor, and a VLSI version known as Daisy. The goals document for this SRS is Goals for Office Systems Workstations Hardware, by Lynch et al. (Ref. [2]). The deviations from the goals as discussed in the goals document are itemized in Section 3.2.

3.1 Features

Following are the highlights of the features of this product. Under the main headings are the section numbers where exact definitions and more detailed information may be found.

Type: (Ref. [9])	MesaPrincOps (D-class), operating standalone, remote, or networked.
Main processor: (6.1.1 & 6.2)	Mesa processor, MSI or VLSI versions.
Control Store: (6.1.1 & 6.2.1.1)	4 KWords, 48 bits per word, expandable to 8 KWords, Daybreak only
Memory: (6.1.2 & 6.2.1.3)	Up to 4 Mbytes, minimum configuration 512 kbytes, baseline configuration 640 kbytes. Daybreak memory expansion beyond 1 Mbyte requires Memory Expansion Board.
Display Buffer:	Separate display buffer of 128 kbytes is required to achieve Dandelion performance.

Rigid Disk: (6.4.1)	One 5.25" Rigid, 10 Mbytes minimum with ST 412/ 506 interface.
Floppy Disk: (6.4.2)	Optional. One 5.25" Floppy, 360 kbytes, 48 tpi, IBM compatible, or one 737 kbyte, 96 tpi, not IBM compatible. Sizes are formatted capacities.
Displays: (6.4.5)	15" and 19" monochrome, 13" auxiliary color display (Daisy only).
Keyboard: (6.4.3)	Low profile, adjustable tilt (see proposed key layout in Section 6.6).
Mouse: (6.4.4)	Optical.
Local Network: (6.3.1.5)	IEEE 802.3, not required for workstation operation.
IBM-PC emulation: (6.3.1.9)	Optional.
Floating Point Capability:	To be implemented in microcode; may require optional 8K word of control store. Not planned for Daybreak launch.
Xerox Software: (5.1)	Star 4.0, BWS 3.0, XDE, applications, diagnostics, utilities.
IBM Software: (5.2)	Some popular packages that run under MS-DOS 2.0.
Options:	Rigid disk capacity (must conform to ST 412/506), floppy disk type, IBM PC emulation, memory size, display size/type, local printers.
Option slots: (6.3.1.9)	Daybreak: 2 plus PCE (includes MEB slot); Daisy: 3 plus PCE.
Configurations: (8.0)	Configurable to customer requirements using options above. See proposed initial configurations in Section 8.0.
Telephone/Voice:	Not planned for Daybreak launch.
Time/Date:	Supported on option board only. Not available for Daybreak launch.
Encryption:	Not currently planned.
Serial Port: (6.3.1.7)	Two ports available (one DCE, one DTE). Synchronous or asynchronous. RS-232 compatible. Baud rates: 110 to 9600 baud. software selectable.

Multinational: (6.6)	Configurable for multinational use with change of power supply in system unit and display. Keycap kits for different languages available.
Environmental/ Safety: (9)	Passes applicable UL, FCC, VDE, etc., specifications.
Power: (6.6)	300W output, switching supply. Optimum power supply sizes will be determined by 4Q84.
Performance: (7)	Substantially the same performance as the Dandelion Mesa machine when executing Xerox software. Substantially the same performance as an IBM XT when executing IBM or IBM-compatible software.
Cabinetry: (4.3)	A four-piece package for the baseline configuration, consisting of a floor-mounted system unit, display, keyboard, and mouse. The optional floppy disk will be a fifth piece mounted to the system unit or located remotely within six feet of the system unit.
Reliability: (10)	To currently accepted industry norms for this type of equipment.
Installation: (10)	Customer installed in 90% + applications.
Maintenance: (10)	System diagnostics to allow customer troubleshooting to the customer replacement unit level.
Future Capability:	In the design of this product, we have allowed space and defined interfaces for the addition of other, currently undefined, hardware at a later date that would conform to the interface standards. Concurrent operation of these options and Star cannot be assumed.

3.2 Deviations from the product Goals document

This section itemizes deviations from the product goals as expressed in the Goals document. (See Ref. [2]) The deviations discussed here include a number of open issues which will have to be resolved later.

Original Goals document section numbers are indicated in italics before a verbal description of each deviation.

Section 3.3 Software Requirements – No work has been done toward the inclusion of Unix and "C" programs.

Section 3.4.2 Displays – There is currently no 12" or 17" display targeted for Dove. Such a display can be fully supported by the electronics. Cabinetry will need to be developed.

Section 3.4.3 Keyboards - No provision is made for inclusion of a telephone cradle or telephone handset connector.

No provision is made for Daisy chain connection of multiple keyboards.

Section 3.4.6.2 Memory - Expansion to 4 Mbytes is available, but manufactured configurations may be limited to achieve consistent memory strategy between Daybreak and Daisy.

Section 3.4.6.3 Disks - The selection of disk drives includes a half height 10 Mbyte, 5¼" rigid disk drive, and full height 20, 40, and 80 Mbyte, 5¼" rigid disk drive, and a half height, 5¼" floppy disk drive. Larger rigid disks that fit into a full height, 5¼" package can be used if they meet the same interface standard.

Section 3.4.6.4 Packaging - The package is described in Sections 4.3 and 6.7. This design deviates from the Workstation Goals which require a footprint of 14" by 12".

Section 6.1 Environmental - We are currently committed to a 47dBA standby noise level.

Dove is specified as meeting VDE 0871 Class B, in contrast to the Goals Class A. VDE does not specify (nor care) which classification is requested for the product in question. The class requested will have an effect on the marketability of the product. Class B is desirable from a marketing standpoint in that it allows open placement of equipment with no notification to the German post office being required.

Shock and vibration: Manufacturing will design the shipping containers of this product for shipment and perform sufficient testing to verify the design. Shipment packaging must be sufficient for customer delivery by parcel post.

Section 6.2 Reliability and Maintainability - We intend to improve on the installation requirements. Customers should be able to do all installations once the network is installed. They should be able to perform all service through CRU replacement procedures.

Complete run time for fault isolation diagnostics will be longer than 5 minutes. Dandelion diagnostics frequently take more than 10 minutes to isolate some faults. Our best estimates are based on Dandelion diagnostics.

Unscheduled maintenance is expected to be about 0.9 instead of 0.5 per machine year (1750 hours/year). This rate is mostly based on comparison to Dandelion parts of similar complexity and technology. The numbers here have limited applicability to Dove. More comprehensive analysis is needed. It is expected that the Daybreak and Daisy configurations will exhibit different performance in this regard. It is expected that the Daisy configuration will be more reliable because it has fewer parts and modules.

machine design On-going maintenance costs are not provided. This data is completely dependent on service method. We have provided the unscheduled maintenance expectations and service alternatives.

3.3 Dove as Daybreak and Daisy

The Dove project is divided into two major hardware phases: the MSI implementation of the Mesa processor known as Daybreak, and the VLSI implementation known as Daisy. Although these two phases will be transparent to the customer, they represent radically different Mesa processor hardware implementations.

The Daybreak-specific hardware consists of a three board set: the Mesa processor board (MPB), the Display control and memory board (DCM), and an optional Memory expansion board (MEB). This implementation relies on conventional MSI parts, and several gate arrays. It consumes more power, is more expensive, and will be inherently less reliable, than the later VLSI version. It will, however, be available for launch earlier than the VLSI version.

The Daisy-specific hardware consolidates the functionality of the Daybreak-specific hardware on a single board. There are two types of VLSI chips on the SAM board: the Mesa processor (the S chip), and a display and memory controller (the A chip). On each board, there will be one S chip and 1 to 4 A chips, depending on memory size. These chips, the control store, display buffer, interface circuitry, and up to 4.0 Mbytes of memory, will be on the SAM board.

All other hardware, except power supplies, is common to both systems. The Daybreak configuration will require a larger power supply than Daisy.

The projected timing of the introduction of these two phases is Daybreak to launch in August 1985, with Daisy to follow in April 1986.



System architecture

4.1 Hardware architecture

The hardware system architecture is shown in the following block diagram (Figure 4.1A). There are three major subsystems: the Mesa Processor, the Memory/Display, and the I/O.

4.1.1 Mesa processor

The Daybreak Mesa Processor is modeled after the Dandelion Central Processor. (See Ref. [5]: Dandelion Hardware Manual.) The major difference is that microcode support for I/O devices ("tasking") has been removed. All Mesa opcodes will be supported. The Daisy Mesa Processor, however, represents a significant departure from the Dandelion architecture. The microinstruction format and data paths were redesigned to facilitate implementation in VLSI.

Virtual memory is implemented using microcode as in the Dandelion. The virtual memory map is kept in main memory. It is explicitly referenced by the Mesa Emulator and I/O Processor when necessary.

4.1.2 Memory subsystem

The display controller, the main memory, and memory controller are included in the memory subsystem. The display controller will be capable of driving all the black and white, and auxiliary color displays (Daisy only) specified in the SRS. The parameters (line length, number of visible lines, etc.) of a particular display are communicated to the display controller under software control.

Memory for the Dove, both Daybreak and Daisy configurations, is packaged in 512 kbyte banks. In Daisy, each block of 1 MByte requires a memory controller. Each memory controller includes a display controller and a refresh controller. Unused display controllers consume no memory bandwidth. In Daybreak, there are 3 memory controllers: 2 on the DCM board, and 1 for the Memory Expansion Board.

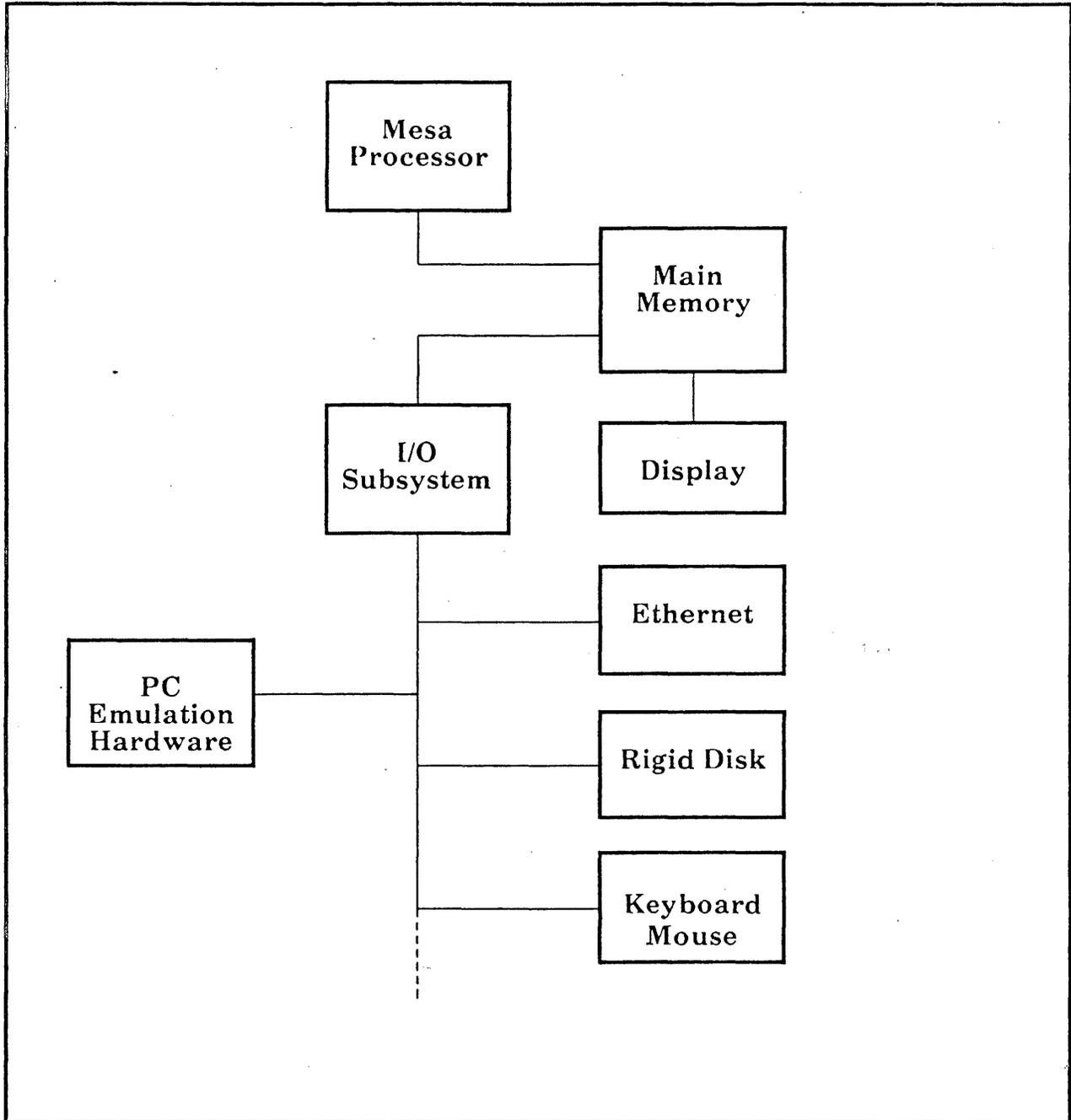


Figure 4.1A Daisy logical architecture

4.1.3 I/O subsystem

The I/O subsystem consists of a commercial microprocessor (Intel 80186), local memory, and all I/O controllers for the workstation except the display controller. Because of its memory bandwidth requirements, the display controller is part of the Memory Subsystem.

To the extent possible, the I/O controllers are commercially-available devices directly compatible with the microprocessor bus. Some controllers, such as the rigid disk, require

direct channels to main memory to satisfy their strict latency requirements and require special features not present on commercial controllers.

The microprocessor bus acts as a convenient medium for connecting the I/O controllers to the system. The microprocessor itself is responsible for handling the controllers and organizing the transfer of data between the local memory and main memory.

Additional hardware will be added to the I/O Subsystem to support PC Emulation. (See Section 6.3.1.9.)

4.2 Software architecture

To the Mesa application program, the machine appears the same as the current architecture to the level of the device faces (interfaces, or DEFINITIONS modules, in the Mesa sense--see Ref. [9]). The faces are implemented by a combination of low-level Mesa code executed by the Mesa processor (these modules are called heads), and IOP code executed by the I/O subsystem, communicating through shared main memory. The two processors also communicate through directly-connected interrupt lines.

By definition, the device faces are common to all implementations of the Mesa architecture. We expect that the current faces will have to be extended to support the additional devices and the configurability of the Dove. These extensions (but not the devices themselves) will be retrofitted to all of the existing Mesa processors. Using these extensions and the existing interface, it will be possible for software above the level of the faces to determine the hardware configuration of each machine.

The architecture has been designed to prevent IBM PC emulation from endangering the integrity of the Star and BWS software environment.

4.3 Physical architecture

The workstation is assembled using four major subassemblies. (See Figure 4.3A.) These are a floor-mounted system assembly containing the PWBAs, rigid disk, and power supply; the display assembly; the keyboard and mouse assembly; and the optional floppy disk assembly. The dimensions of the system unit are 9.5" wide, 12" deep, and 21" high. Connectors and cables are on the rear of the system unit. The optional, half-height, floppy disk drive will mount either on the top of the system unit or remotely within six feet of the system unit. The power switch, indicator lights, and boot switches are on the front of the system unit.

The keyboard is a low profile, adjustable tilt keyboard, with sculpted key caps, and will conform with applicable ergonomic guidelines. The proposed key layout is in Section 6.6 of this document.

The display housing will be considerably different from the ones used for Dandelion. (See Figure 4.3A.)

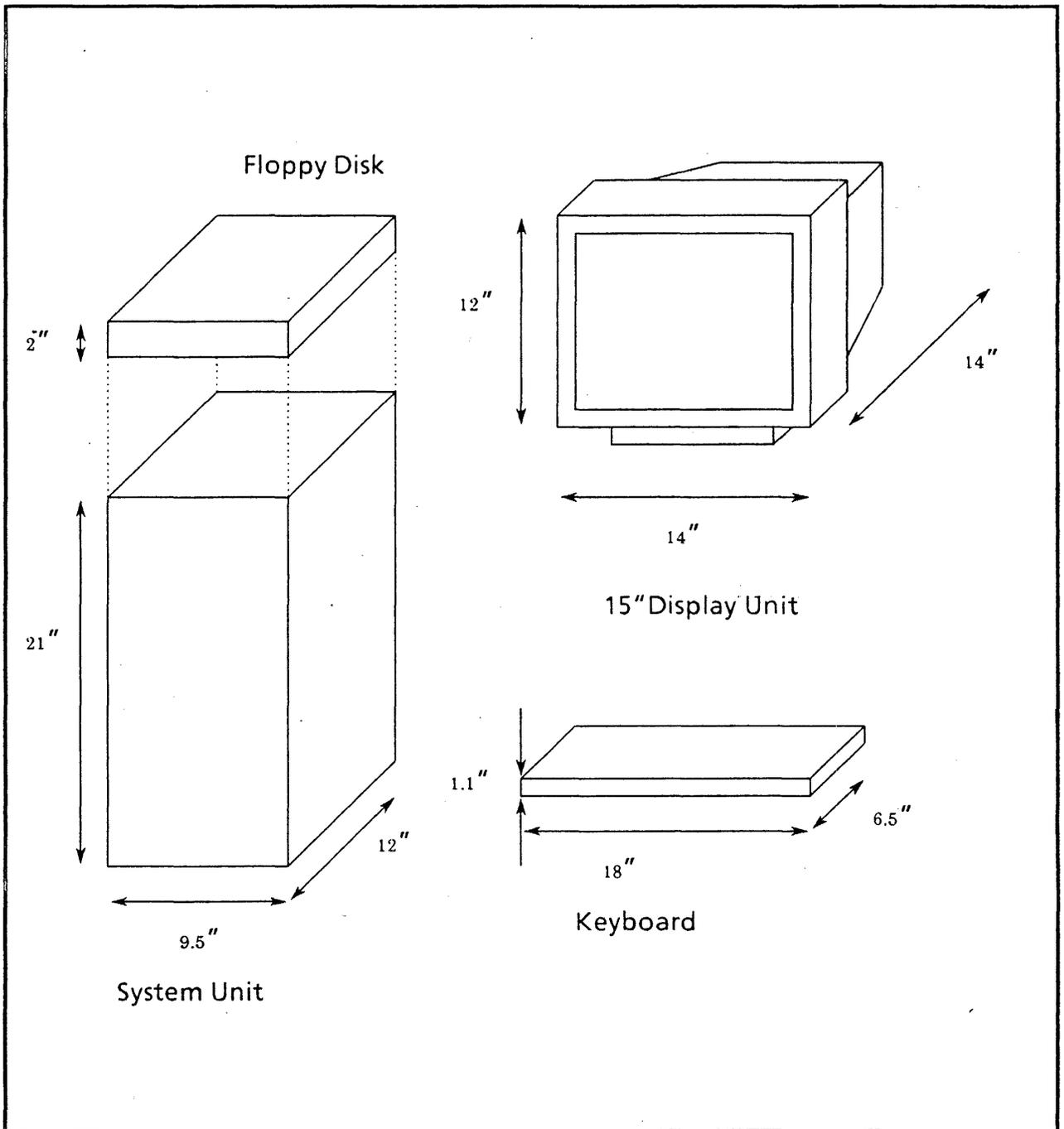


Figure 4.3A System physical size and shape

Cabling will be lightweight and unobtrusive. There will be six external cables in a basic unit: the system power cord, display power cord, display signal cable, keyboard signal cable, keyboard to display cable, and mouse tail. If the Ethernet and/or floppy disk options are present, there will be an Ethernet cable, and floppy disk power and signal cables. The floppy disk is designed to fit on top of the system unit, but can be located up to six feet away from the system unit for operator convenience. (See Figure 4.3B for interconnect schematic.)

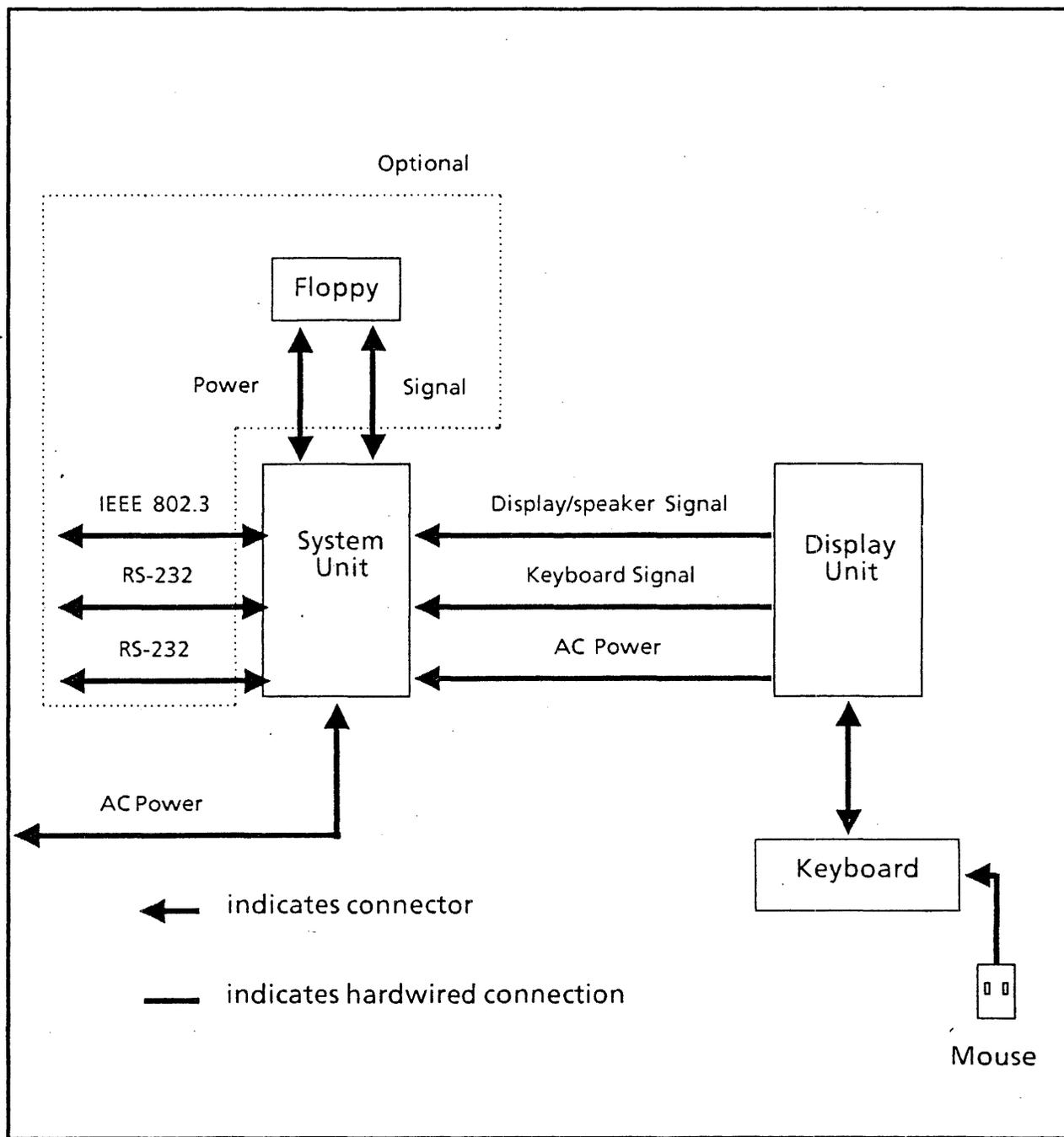


Figure 4.3B Dove cabling schematic



Software

Dove workstation software can be divided into two classes,

- Xerox software that implements the Star workstation facilities, or other workstation facilities such as the Xerox development environment (XDE), the Versatec Expert 1000 and 2000 systems, Hobson B (IPD), or software developed by XSIS.
- Software that allows the execution of IBM PC application programs inside a Star window, that is, IBM PC emulation software.

5.1 Xerox software

Most Xerox workstation software is written in one of three high level languages: Mesa, LISP, or Smalltalk. Only the Mesa systems will be discussed here. The LISP and Smalltalk systems are structured in a similar way to the Mesa systems, so similar software efforts will be required to port LISP and Smalltalk to Dove. Porting LISP or Smalltalk to the Dove machines is beyond the scope of this project.

The Dove workstations will execute all Mesa workstation software, including Star, Hobson B, the Xerox development environment, and the Expert 1000 and 2000 systems. Very little of this software will require source changes to run on a Dove workstation, because the Mesa software architecture is designed to make almost all of the software independent of the particular hardware on which it is running. It requires only what is known as the "Mesa virtual machine," an abstract machine that by definition implements the Mesa language and provides access to input/output devices via generalized interfaces. These interfaces, called "faces," are general enough to allow access to multiple variants of a particular I/O device such as a disk drive, without changes to the software above the interface.

In the course of the Dove program, however, minor architectural oversights are expected to be uncovered in the faces. For example, there may be a lack of sufficient generality or abstraction, or insufficient facilities to use unforeseen Dove device features. The PC emulation project is also expected to lead to new face requirements. Hence the faces will need to be fine tuned and refined in the course of developing the Dove software. Pilot, the machine-independent Mesa operating system, will have to be adapted to the face refinements. Some of these changes could conceivably even require minor modifications to Star or other workstation application software.

Faces are Mesa-level interface modules. For each new hardware implementation, a relatively small layer of software must be written that implements the Mesa virtual machine, that is, the Mesa language and the faces. This software typically includes microcode, I/O processor software, a layer of Mesa software above the I/O processor software that implements the faces, and diagnostics. Much of diagnostic software is hardware-specific because it is required to isolate hardware failures to specific parts of the hardware, which requires intimate knowledge of the hardware.

5.1.1 Mesa emulator microcode

Both Daybreak and Daisy configurations of Dove will execute Mesa software by means of Mesa emulator microcode that implements the Mesa machine architecture defined in the *Mesa Processor Principles of Operation* [9]. These implementations will differ significantly between Daybreak and Daisy. The Daybreak Mesa processor provides a micro-instruction set very similar to that of the Dandelion Mesa processor, so the Daybreak Mesa emulator microcode will be derived fairly directly from the Dandelion microcode.

The Daisy Mesa processor is sufficiently different from the Daybreak and Dandelion processors to require all-new Mesa emulator microcode. It is similar enough to the Dandelion, however, to allow the emulator to be implemented in approximately the same number of micro-instructions. The Daisy Mesa emulator is expected to be within five percent of the size of the Dandelion Mesa emulator, which has 3176 micro-instructions.

5.1.2 I/O software architecture

In a Mesa machine, the operating system, Pilot, provides the application code, such as Star or XDE, with a high-level view of the I/O devices on the system--for example, the disk is presented as a filing system. Pilot itself is machine independent and relies on the faces as standard interfaces to devices. The implementation of a face on a particular machine is called a "head." The head is responsible for interpreting commands given to the face and somehow passing them on to the appropriate device hardware. A Dove-specific head will be written for each device on Dove: rigid disk, floppy disk, Ethernet, keyboard, mouse, display, RS-232-C ports, PC emulation option card, and Mesa processor.

On Dove, the devices are connected to an I/O subsystem controlled by an 80186 microprocessor (the I/O processor, or IOP). All IOP software for Dove is Dove-specific and, therefore, new. Most of the devices are connected by intelligent device-specific controllers, and the IOP merely provides the interface between the heads and the controllers, setting up control registers and fielding interrupts, for example. This IOP software component is called a "handler." A handler will be written for each device, including the Mesa processor and the debugging umbilical hardware. The Mesa processor handler is responsible for initialization and control of the Mesa processor and its microcode control store.

In addition to the device handlers, a relatively small and simple IOP operating system kernel will be implemented. It will manage the IOP resources that are shared among the handlers, principally memory, interrupt controllers, timers, and IOP processor cycles.

The Mesa machine is the primary client of the I/O subsystem: this is reflected in the overall system architecture in Figure 5.1. Other clients are booting code, PC application

programs running on the optional PC emulation hardware, and the intimate microcode debugger interface.

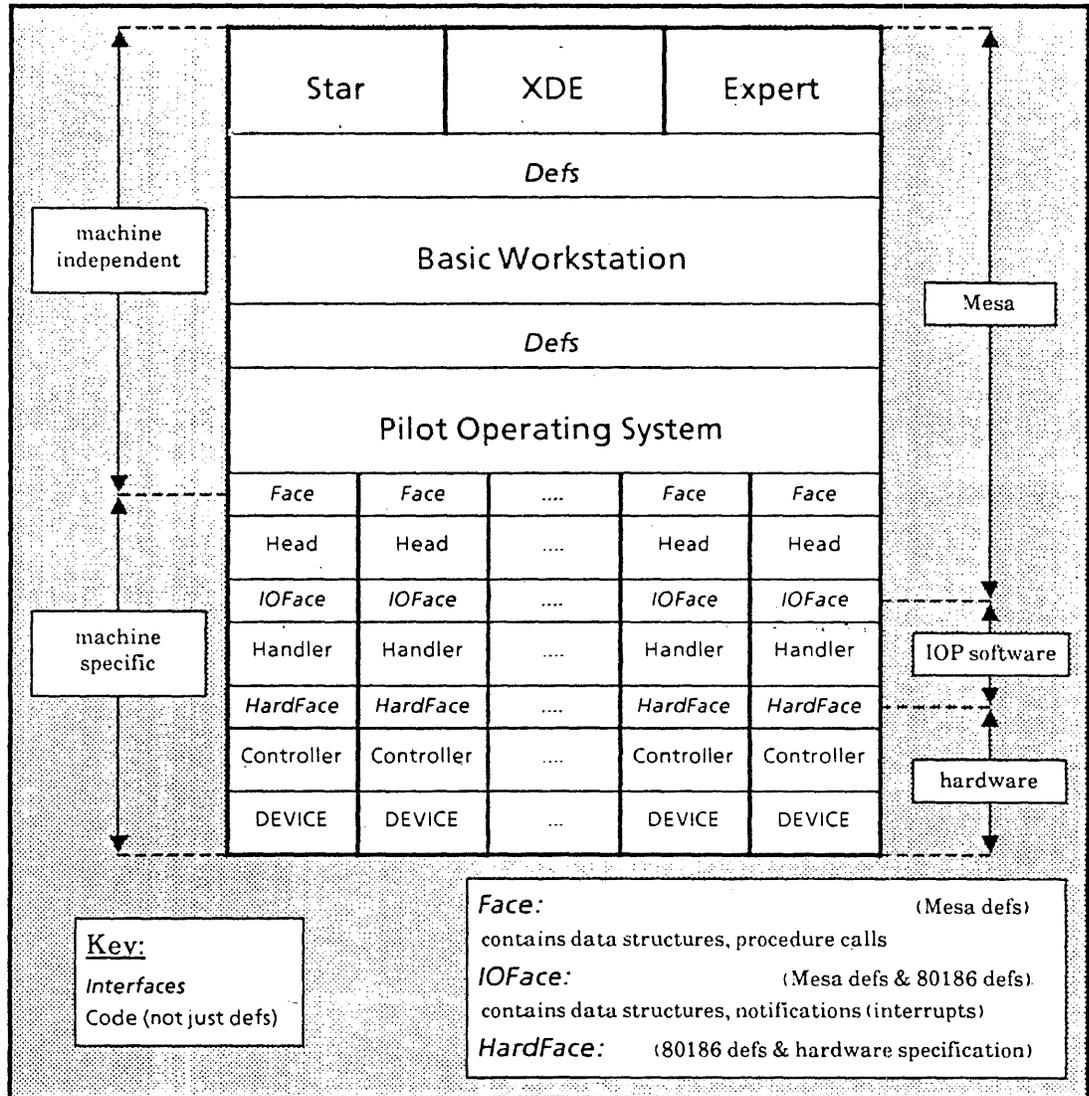


Figure 5.1 Mesa view of system structure

Each head keeps a certain amount of state to describe the device(s) it controls. An important part of this state is the set of I/O control blocks (IOCBs), each of which, in general, corresponds to a request for action by the device. IOCBs are passed via the IOFace to the IOP system and to the specific device handler. Whereas the face is a single Mesa definitions module used by both Pilot and the head, the IOFace exists both as a Mesa definitions module for use by the head and as a set of assembler definitions for use by the device handler. The handler takes that IOCB and performs the requested operation. With its intelligent controllers, this is often very simple on Dove: it may merely be necessary to set up the controller, as defined in the HardFace (i.e., hardware specification) and wait for the 'done' interrupt to occur. On the other hand, some devices will require interrupt level

processing during the operation itself--such as loading up the data buffer of a UART for the RS-232-C port for each byte to be transferred.

It is desirable that as little processing as possible be done on the control blocks in the IOP--the heads are a much better environment for such work. The IOP software, therefore, only does low-level device scheduling, passing command and status information between the control blocks and the device controllers, and passing the control blocks back to the heads. The IOP software can be almost completely event (i.e., interrupt) driven: when a control block arrives from a head, it will be put on an appropriate queue; when a device interrupt such as end-of-block occurs, the device status will be put in the control block, and the control block passed back to the head. All high-level scheduling, error handling, and other processing of results will be done in the heads and not by the IOP software.

5.1.3 Rigid disk firmware

The rigid disk controller hardware includes a microprogrammed 8X305 processor. This processor will manage the interfaces to the rigid disk handler IOP software and the rigid disk drive. Firmware will be written implementing these functions.

5.1.4 Booting

It will be possible to boot software from a variety of boot devices: rigid disk, floppy disk, Ethernet, and an IOP debugging umbilical. The IOP EPROMs will contain a generic, simple-minded, bootstrap loader and device-specific code to read in code from fixed locations or files on each boot device.

The Dove booting user interface will be significantly different from that on the Dandelion. Rather than using an alternate boot button to choose one of a number of booting options represented solely by maintenance panel numbers, Dove booting will allow the user to select booting options via display icons and the mouse. This user-friendly booting interface will be backed up by an alternate keyboard method, in case the display or mouse is broken.

5.1.5 Diagnostics overview

Diagnostics are defined to be software and hardware used to identify a hardware malfunction, aid in isolating the problem to a replaceable unit, and verify after replacement that the machine has been returned to operating condition. For Dove, ordinary customers, customer-employed service persons, and Xerox-employed service persons are expected to be users of diagnostics.

Ordinary customers will be the least sophisticated users of diagnostics and are expected to be able to diagnose and isolate failures only to customer replaceable units (CRUs). CRUs are defined to be all systems components which the user is expected to install. Thus, the display, keyboard, and mouse are CRUs. The typical user is not expected to diagnose or service failures within the system unit itself.

Trained service persons, employed by either the customer or Xerox, will be more sophisticated users of diagnostics. Using the diagnostic hardware and software, they will be able to diagnose and isolate failures to a more specific set of hardware units called "field replaceable units" (FRUs), including components making up the system unit. FRUs

typically do not go below the level of printed wiring board assemblies (PWBAs), with the exception of memory chips.

The above information is derived from the *DOVE Program Diagnostic Goals* document [10], which also contains other information such as fault isolation targets and a full enumeration of FRUs.

Five types of diagnostics software are planned for Dove: preboot, boot, offline, online, and acceptance tests. The discussion below of each type is based in part on the *DOVE Program Diagnostic Strategy* document [11].

5.1.6 Preboot diagnostics

Preboot diagnostics isolate and identify failures in the hardware required for loading and running IOP boot software: the IOP, IOP EPROM and RAM, the interrupt controllers, the timer, the controller for the boot device, and the boot device itself (rigid disk, floppy disk, Ethernet). The tests on the boot device controllers and the devices themselves are not intended to be extensive. They are typically limited to verifying the device is present and ready. These diagnostics do not check the Mesa processor, since it is not needed for the initial stages of booting.

Preboot diagnostics reside in the IOP EPROMs and are initiated anytime the system is powered up or the system reset switch is pressed. They execute before any software is booted into memory from the boot device, hence they are called "preboot." They consist of IOP software only. Interaction with the user is done via the LED status indicators, the display cursor, the speaker, the keyboard, the mouse, and a special maintenance panel to be used by manufacturing and service depots. Expected users include both ordinary customers and trained service personnel.

5.1.7 Boot diagnostics

Boot diagnostics isolate and identify failures in the hardware required to load and run Mesa software, as well as failures in hardware not accessible to the Mesa software. The former category includes the Mesa processor, its control store, the main memory controller, and the main memory itself. The latter category covers mostly the IO subsystem, including the IOP, the IOP bus arbiter, the IOP interrupt controllers, and the various device controllers. Both a short and long version are supported. These diagnostics reside on any of the boot devices and are initiated optionally by the user during booting. They have both automatic load-and-go and interactive modes.

Boot diagnostics consist of both IOP software and Mesa processor microcode. Interaction with the user is done via the LED status indicators, the display and its cursor, the speaker, the keyboard, the mouse, and the optional maintenance panel. Both ordinary users and trained service personnel are expected to use these diagnostics, although ordinary users may be given access to only a subset of the tests.

5.1.8 Offline diagnostics

Offline diagnostics isolate and identify failures in the peripheral I/O devices and their controllers. They cover the rigid disk, floppy disk, Ethernet, RS-232-C, keyboard, mouse, display, and options such as the PC emulation option card and optional local printers.

These diagnostics reside on any of the boot devices and are initiated by booting a special boot file from that boot device. The operational software must be shut down before booting these diagnostics, hence they are called "offline." They may be invoked in either automatic load-and-go or interactive mode.

Offline diagnostics are written exclusively in Mesa. Interaction with the user is done via the display, keyboard, and mouse. Turnaround plugs and other special hardware may be used with offline diagnostics. Only trained service personnel are expected to use this type of diagnostics.

5.1.9 Online diagnostics

Online diagnostics isolate and identify failures in the peripheral I/O devices and their controllers. They cover the floppy disk, Ethernet, RS-232-C, keyboard, mouse, display, and options such as the PC emulation option card and optional local printers. These diagnostics are part of operational software systems such as Star, XDE, or Expert 1000 or 2000. They are initiated like other application programs in the respective environments without booting up a special boot file, hence they are called "online." They are strictly interactive. They may not be as extensive or complete as offline diagnostics, because they have to live within the constraints of a running non-diagnostic system. They will not use any turnaround plugs or special add-on hardware.

Online diagnostics are written exclusively in Mesa. Interaction with the user is done via the display, keyboard, and mouse. Both ordinary customers and trained service personnel are expected to use online diagnostics.

5.1.10 Acceptance tests diagnostics

The acceptance tests procedures package (ATP) is used by manufacturing for system-level testing of newly-manufactured systems. It is run on systems in the extended run area at the end of the assembly line to identify and isolate system failures. It is an automated, network-based package, with a master station that downloads software to a number of machines being tested simultaneously, and collects hardware failure information from them. It runs a battery of tests on each system for several hours, testing the major system components such as both processors, memory, and I/O devices.

ATP is written completely in Mesa. Interaction with the user is via the display, keyboard, and mouse. Only manufacturing is expected to use ATP.

5.2 IBM PC emulation software

This section describes the software which implements the IBM PC Emulation feature on Dove. This body of software includes operating systems and application programs written for the IBM PC, a program equivalent to the IBM PC ROM BIOS (called the Xerox BIOS), and a combination of 80186, Mesa, and microcode programs which implement a virtual hardware environment for the IBM PC. It does not describe programs which support the PC Emulation window in the Star environment or the conversion of files (data) between Star and the PC environment.

This section does not provide a detailed description of the implementation strategy. The implementation strategy will be found in the PC Emulation on Dove Development Plan (Ref. [12]).

5.2.1 IBM PC applications

The PC Emulation feature will support the execution of IBM PC application programs in an unmodified state. Since many of these programs are written in a manner that makes them extremely hardware dependent, the PC Emulation feature must provide an environment which looks as closely as possible like the hardware environment of the IBM PC.

It is unrealistic to support *all* programs written for the IBM PC. Programs which are not expected to execute correctly on the emulated PC are those which do timing by counting processor cycles and those which require unsupported devices. It appears that with only a few exceptions, the unsupported programs are in the game market. We do expect to be able to run a large portion of the programs currently available for the PC and many of the "interesting" business application programs. A more exact description of supported programs will be found in the PC Emulation on Dove Functional Specification (Ref. [13]).

[While this is an IOS SBU issue, engineering currently (8/27/84) believes: Xerox will not supply all application programs. (There may be a limited set of special applications supplied.) Customers are expected to supply application programs through the currently available channels: distributors, mail-order houses, and in-house programming endeavors.]

5.2.2 MS DOS and operating systems

[While this remains an IOS SBU issue, engineering currently (8/27/84) believes: Xerox will supply a version of MS DOS configured similarly to PC DOS. Also supplied will be various utilities which are normally supplied with PC DOS when purchased from IBM. The version supplied will be MS DOS 3.0.]

No other operating systems will be supplied. Other IBM PC-compatible operating systems (e.g., CPM, etc.) may execute without modification, but this is *not* a requirement.]

5.2.3 Xerox BIOS

On the IBM PC, the ROM BIOS is a program which provides the machine bootstrap program and the basic interface between operating systems or application programs and the IBM PC hardware. For Dove, Xerox will acquire a license to use an IBM PC-compatible BIOS. The Xerox BIOS will be modified to include boot operations specific to the PC Emulation 80186. Otherwise, the Xerox BIOS will be substantially unchanged in a functional sense from one that would execute in a real IBM PC.

The Xerox BIOS will be loaded into an area of Dove (RAM) memory which is mapped to respond to the addresses normally associated with the ROM. Installation of this software will occur when the PC Emulation feature is invoked. It will not require any memory resources when the PC Emulation feature is not active.

5.2.4 PC emulation support

The PC Emulation feature is largely dependent upon emulating the hardware environment of the IBM PC. Special trapping and address mapping hardware on the PCE PWBA will assist in this task. The IOP186 will execute programs which "catch" trapped I/O operations and cause the appropriate emulation procedures to be executed. There are two kinds of programs required to provide this function: a dispatcher and a set of PCE I/O Handlers.

The dispatcher services an interrupt from the PC Emulator which indicates that an I/O operation has been executed by a PC program. (The PC is held during the service of this interrupt.) By reading the trapped address and status, the dispatcher determines the correct PCE I/O handler to call for emulation of the I/O operation.

Upon activation, most PCE I/O handlers immediately make an up-call through the Mesa PCE Head and Face to the PCE Support Program. The PCE Support program hierarchically is above the Pilot Faces, so that it may call Pilot functions to emulate the I/O operation.

Support will be provided for the following devices in the PCE Support Program: the display controller, the keyboard, the floppy disk, the rigid disk, the RS232C port, and a logical parallel printer port. The interrupt controller, the PC speaker and associated logic, and the timer will not require support above the dispatcher level.

The PCE Support program will include a map which associates device requests with the mechanism for emulating devices. (A floppy request to drive A may be routed to the real floppy disk while a floppy request to drive B may be routed to a "virtual" floppy disk.) A description of the possible device mappings and supporting service routines will be found in the PC Emulation on Dove Functional Specification (Ref. [13]).

5.2.5 Special display microcode

In order to transform the emulated PC display memory into a bitmap on Dove's display, a special version of BITBLT may need to be written, which does a transformation of 1 horizontal line to 2 horizontal lines. Different, but similar, microcode will be required for Daybreak and Daisy.



Hardware

This section includes details on all the hardware that will be in the Dove systems. As mentioned previously in this document Dove will exist in two versions: Daybreak, an MSI Mesa processor version that will be the unit shipped at launch (August 1985), and Daisy, a VLSI version that will ship beginning in April 1986. The reason for these two versions is that the VLSI version that meets the program UMC requirements will not be ready until the later date, and it is required that market introduction be as soon as possible. The different versions will be transparent to most users. Except for the Mesa processor, memory subsystem, and power supply, the rest of the hardware is common to both versions.

6.1 Daybreak specific hardware

The Daybreak-specific hardware is three PWBA's: the MPB, DCM, and the MEB, which respectively are the Mesa Processor Board, Display Control and Memory board, and the Memory Expansion Board.

Each of these PWBA's is full size (10.9" x 16"). Greater than half of the initial system UMC is accounted for in these assemblies. The boards are extremely complex and require high-density interconnects to achieve a two-signal layer PWBA.

6.1.1 Daybreak Mesa processor (MPB)

The architecture of the Mesa Processor is modeled almost exactly after that of the Dandelion central processor. It will execute a slightly different version of the Dandelion micro-instruction set. Small portions of the Dandelion Mesa Emulator will be modified for Daybreak.

The MPB contains the same registers as in the Dandelion. The full complement of the 256 U-registers remains intact. The major elements of the Dandelion data path, ALU, rotator, RH registers, 8-bit constants, and so on, are present in the Daybreak MPB.

The clocking scheme remains the same as that used in the Dandelion, except for the faster 125 ns clock rate.

The Instruction Buffer in the MPB remains the same as in the Dandelion. It is handled the same way in microcode as in the Dandelion. A custom gate array is used to decode and

latch the micro-instructions. The translation of virtual to real addresses is done explicitly in microcode.

The MPB communicates to the rest of the workstation via the Mesa bus. Through this link, the MPB can read and write main memory. It may also directly exchange interrupts with the I/O subsystem. A custom gate array is used to perform bus controller functions for the MPB. The Mesa bus is a synchronous bus, optimized for performance between the MPB and system memory.

The control store is 4096 48-bit words. This is optionally expandable to 8KWords.

6.1.2 Daybreak display control and memory (DCM)

The display controller, display memory, memory controller, and part of system memory are implemented on the DCM board.

The display controller performs two tasks:

- Retrieves display data from display memory and sends it to the display monitor.
- Mixes the cursor pattern with the display data on output.

The read section reads display data from display memory mostly in nibble mode and pushes data into the output FIFO. The output section pulls display data from the FIFO and loads the data into a Video Shift Register, which then shifts the data out to the display in a serial format. The display data and cursor data are mixed in certain intervals during a number of scan lines determined by the location of the cursor.

The DCM will determine which display is attached by reading a code that is hardwired in the display cable. It will then select the appropriate display frequency from on board crystal oscillators. No user or field service intervention will be required.

The DCM control parameters, control registers, and control RAM are written and read by the IOP.

The display memory is located in the first bank of memory and may be implemented with 64 kbit DRAMs, or 256 kbit DRAMs. In the minimum configuration, the display and processor will compete for the same memory bank with resulting degradation of processor performance.

The Mesa processor, 80186, display controller, and memory all operate independently. These subsystems are logically joined by the synchronous memory arbiter within the memory controller. The arbiter grants memory access to the highest priority requesting device. In order of priority, these devices are: memory refresh, display, 80186, Mesa processor. IOP and Mesa processor memory requests are initiated by bus transactions. The memory controller counts down from the 16 MHz input clock and requests refresh cycles when necessary. At the Mesa bus port, all signals are synchronized with the Mesa processor.

When the memory is not busy, the arbiter grants access to the first requesting device. Otherwise, arbitration is performed during the DRAM RAS precharge time. Such arbitration pipelining allows continuous memory cycles. The 80186 bus cannot cycle fast

enough to saturate the memory with requests; therefore, the Mesa processor can obtain at least every other memory cycle when the display is not demanding memory cycles.

Once a memory cycle is granted, the memory controller is started. The memory controller multiplexes the addresses, controls memory timing, delivers data, and starts the arbiter when memory again is available. It generates and checks byte parity. A parity error interrupts the IOP 80186 if the 80186 has accessed memory; it traps the Mesa Processor if the Mesa processor has accessed memory. DRAM strobes are generated from shift registers in the gate-array chip.

The memory controller is implemented with a synchronous state machine running at an effective 32 MHz rate. The memory controller state machine will accept reads and writes. The memory controller is capable of running 4 types of cycles: display, 80186 bus, Mesa Processor, and refresh.

Display cycles are mostly quadword read. Address generation is pipelined so that the display controller is prepared to use all the available memory bandwidth. There are four variations on the 80186 bus memory cycles: read word, write word, write high byte, and write low byte. There are also two variations on Mesa processor memory cycles: read word and write word.

As much as 1.5 Mbyte of system memory can be placed on the DCM card. This memory must be placed in 512 kbyte blocks.

6.1.3 Memory expansion board (MEB)

The memory expansion board provides for system memory expansion of 3 Mbytes in 512 kbyte sections to a total of 4 Mbytes. This board is to be populated with 256 kbit DRAMs.

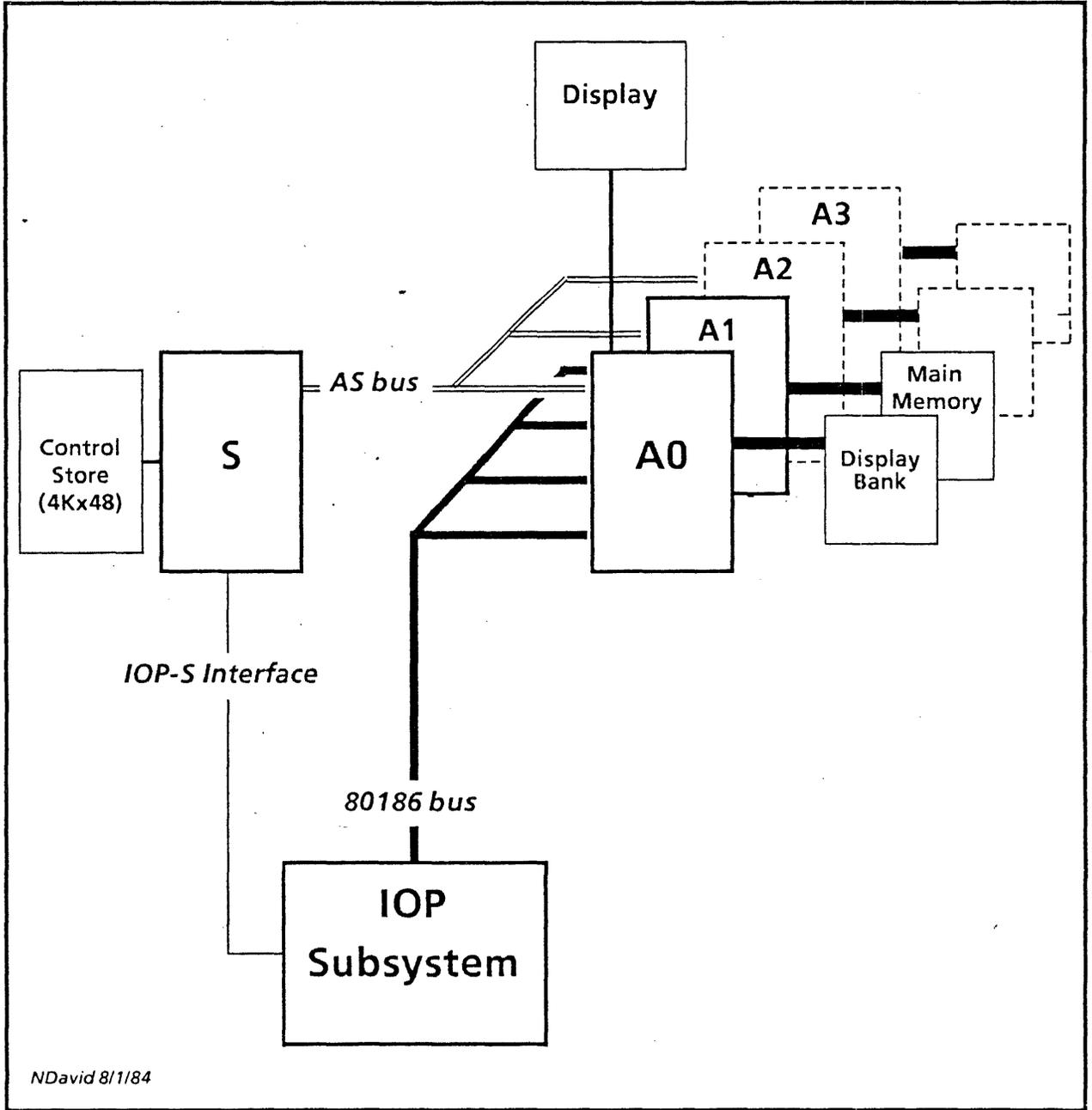
6.2 Daisy module

The Daisy Mesa processor module for the Dove workstation provides the same functions as the Daybreak MPB, DCM, and MEB modules on a single PWBA. By consolidating the Mesa processor, display controller, and memory controller functions into two VLSI integrated circuits, Daisy reduces the unit manufacturing cost of the Dove workstation by \$450, or more, per machine. The Daisy module will be available for "cut in" to the Dove manufacturing process in 1986.

The following sections describe the Daisy module and the two VLSI integrated circuits which provide most of its functionality. Block diagrams at the end of the sections illustrate the Daisy Mesa processor module.

6.2.1 Daisy board (SAM)

The Daisy PWBA that replaces the Daybreak PWBA is named SAM for *S* chip, *A* chip and *Memory*. The board has very little MSI logic; the bulk of the logic is contained in the custom VLSI chips. The *S* chip is a Mesa processor; the *A* chip is a memory controller, 80186 bus controller, and display controller. The functional block diagram of the SAM board is shown in Figure 6.2.1A.



NDavid 8/1/84

Figure 6.2.1A Daisy block diagram (two A chip configuration)

The SAM board contains control store, an S chip, multiple A chips, display interface, and the Daisy main memory.

6.2.1.1 Control store

The baseline configuration of the SAM board holds 4096 48-bit words of S chip control store, implemented using 4K x 4, 55 nS static RAMs.

6.2.1.2 The S chip

The S chip, which executes Mesa bytecodes for Daisy, is a custom VLSI chip being designed to our specification by Silicon Compilers Inc. (SCI). The Daisy board holds exactly one S chip. Normally, data transfer between the S chip and the rest of the system is accomplished using the AS bus to all the A chips and using two interrupt lines to the IOP.

While booting and debugging, the IOP uses additional control signals to read and write control store and to start, stop, and reset the S chip. The S chip contains the data paths used when reading and writing control store.

The S chip is described in more detail in Section 6.2.2.

6.2.1.3 A chips and main memory

The SAM board holds one to four A chips. Associated with each A chip is one or two banks of 16-bit wide memory with byte parity. Depending on the size of the RAM chips (64K x 1 and 256K x 1 are supported), each A chip can control from 128 kbytes to 1 Mbyte of memory. Each A chip acts as a memory controller for its memory bank on behalf of the IOP and S chip.

Two of the A chips may also have active display controllers. External circuitry on the SAM board allows one of the active display controllers to drive either a 15" or a 19" monochrome display. A different type of circuitry connects the other active controller to a 13" auxiliary color display. See Section 6.4.5 for display specifications. The SAM board will operate correctly with 0, 1, or 2 displays attached. At most, one monochrome and, at most, one color display can be connected.

The SAM board will determine which display is attached by reading a code that is hardwired in the display cable. It will then select the appropriate display frequency from onboard crystal oscillators. No user or field service intervention will be required.

A chip 0 is responsible for driving the monochrome display, and also provides bus control signals for the IOP bus. This A chip is included on all SAM boards. Other A chips and memory banks are optional. Significant Mesa performance gains (approximately 10%) can be achieved if at least two A chips are present; the S chip is then not competing with the display controller for use of a single memory bank.

The A chip is described in more detail in Section 6.4.

6.2.2 The S chip

The Sirius, or S chip, executes Mesa bytecodes for the Daisy processor. The chip contains:

- the Mesa evaluation stack
- 76 16-bit data registers, 8 24-bit address registers, and 7 miscellaneous registers and counters
- a 16-bit ALU, an 8-bit adder for address calculations, and a 16-bit rotator
- a micro-instruction address sequencer
- the AS bus interface

6.2.2.1 Control store

Like all previous Mesa processors, the S chip is microprogrammed. It uses a 48-bit micro-instruction word. Both the S chip architecture and the format of the micro-instruction are unique to this design.

The S chip itself is capable of addressing four banks of control store, each containing 4096 48-bit words. The SAM board has room for one banks.

6.2.2.2 Design and processing responsibility

SCI is designing the S chip to our specification. As part of the design process, SCI has written a software simulator of the S chip and OSD's Systems Development Department (SDD) has designed a hardware simulator. Test vectors and microcode diagnostics will be run on both simulators to ensure that they are complete, correct, and identical.

SCI is negotiating with foundries to secure prototyping and production facilities. The design is currently being done assuming VLSI Technology's 3 micron process. Other processes supplied by Xerox and Motorola are under investigation.

6.2.2.3 Power and space requirements

The S chip will dissipate no more than 3 watts.

The S chip is very close to the size of the ED Mesa Chip at 355 mils on a side. It has 119 pins and will be housed in the same pin-grid array package being used for the ED Mesa and Cache chips.

6.2.3 The A chip

The A chip controls memory, expands memory address space for the 80186s, and controls display.

- The A chip arbitrates between three major memory clients: the IOP subsystem, S chip, and the display controller. A client can request memory access at any time (asynchronously); the memory arbiter grants access on a priority basis.
- The A chip is programmable by the IOP, for example, to control display size, to change memory mapping, to relocate the display bank in memory, to control the cursor, and to run diagnostics.
- 80186 memory address space is expanded by a set of address map registers in each A chip. Logical address space is divided into eight banks of 128 kbytes/A chips. A chips are programmed so that exactly one A chip responds to a particular address. The responding A chip maps the logical bank to one of its eight *real banks*.
- Through its mapping capabilities, the A chip isolates PC emulation from Mesa applications.
- A display controller fetches display data from memory, buffers the data in a FIFO, and sends it synchronously to the display. The cursor pattern and location are stored in A chip registers. The display controller mixes the cursor into the video stream.

6.2.3.1 Dynamic RAM controller

The A chip directly controls either 18 or 36 dynamic RAM chips (see the following subsection). All strobes are generated from internal clocks. Addresses and data are multiplexed internally. Memory is automatically refreshed.

When a memory cycle is granted, the memory controller is started. The memory controller runs four types of cycles, as follows.

1. Display cycles: always quadword read. Address generation is pipelined so that the display controller is prepared to use all the available bandwidth.
2. 80186 bus memory cycles: with four variations--read word, write word, write high byte, write low byte.
3. S chip memory cycles: with four variations--read word, write word, read double word, write double word.
4. Refresh cycles: RAS--only cycle using an address maintained by the A chip.

6.2.3.2 Memory organization

Each A chip controls either one or two banks of memory, 16 bits wide with byte parity. The design supports 64K x 1 and 256K x 1 RAM chips with 150 ns access times and with nibble mode. For example, to save costs, the A chip 0 with the display controller might be loaded with 64 kbit chips, and the A chip 1 loaded with 256 kbit chips.

Parity is generated and checked for 80186 and S chip memory references. Each byte has separate parity. The parity used (even or odd) is programmable.

6.2.3.3 A chip internal registers

A chip internal registers are accessible via I/O space 80186 bus cycles. Each A chip fully decodes the I/O space addresses. These addresses are qualified by the internal A chip ID so that the A chip addresses are independent.

6.2.3.4 80186 bus control

Each A chip uses the main 80186 clock and bus control strobes to follow the progress of each bus cycle. In doing so, all four chips generate internal strobes; A chip 0 drives these internal signals off-chip for the benefit of the rest of the system. The timing is similar to that of the Intel 8288 bus controller.

Each A chip is programmed for the size of the IOP 80186 local memory, and generates a signal (LCS') to indicate when the 80186 local memory is addressed. A chip 0 drives this signal off-chip.

6.2.3.5 80186 processor memory references

The A chip expands the 80186 address space and provides limited memory protection to multiprocessors. One of the memory ports connects to an 80186 bus and supports its protocol.

6.2.3.6 Display controller

The parameters of the display controller are set from the 80186 bus; in other respects, the display controller is transparent to the programmer.

A set of parameter registers in the A chip generates display controller addresses. The parameter registers specify the bitmap by location in memory (quadword aligned), by the number of lines, and by length of a horizontal line in quadwords. Another bit specifies interlaced or noninterlaced scan. For a noninterlaced scan, the horizontal line length restriction is relaxed to word boundaries.

Another set of registers contains the cursor and border patterns. Auxiliary registers specify the cursor location and the rule with which the cursor is mixed into the video stream. The display controller supports cursor-only display on top of the border pattern. Color cursors and borders are not supported.

Two of the A chips may have active display controllers. External circuitry on the SAM board allows an active display controller to drive either a 15" or a 19" monochrome display. A different type of circuitry connects the other active controller to a 13" auxiliary color display.

6.2.3.7 Auxiliary color display

The A chip will provide an internal 4-bit color palette that generates analog RGB (Red, Green, Blue) signals suitable for driving a medium resolution color monitor. (See Section

6.5.5.) Development of the color features will follow completion of the rest of the A chip design.

6.2.3.8 Mesa processor memory requests

Memory cycles are requested from the A chip(s) by the S chip via the AS bus. The S chip initiates memory requests, and can read and write single word, read double word, and write double word.

6.2.3.9 Power and space requirements

The A chip will dissipate approximately 2.4 watts and will require the use of a fan and/or heat sink. Power supply voltage of +5V is required.

The A chip is approximately 260 mils x 290 mils. It has 119 pins and will be housed in the same pin-grid array package being used for the ED Mesa and Cache chips.

6.3 Dove I/O subsystem

The I/O subsystem is one of the major subsystems of the Dove workstation. The subsystem is common to both the Daisy and Daybreak implementations of the workstation. The I/O subsystem is controlled by the I/O processor (IOP), a commercial VLSI microprocessor. This section describes the various blocks that comprise the I/O subsystem.

The main functions of the I/O subsystem are as follows:

- It controls all the I/O devices associated with the Dove workstation during system operation. With the exception of the bitmap display controller, all hardware associated with the peripheral devices is embodied in the I/O subsystem. All software that directly controls the I/O devices runs on the IOP. The display controller is programmed by the IOP, but most of the hardware associated with it is found outside the I/O subsystem.
- It controls the Mesa processor during power-up and initialization. The IOP is responsible for bringing the Mesa processor up to a functional state after the machine is powered up or booted. This process ensures that the various processor states are correctly initialized, and then starts the Mesa processor.
- The IOP writes and reads the Mesa processor control store. The write function is used to initialize control store with microcode before the Mesa processor operates. The read function is used primarily as a diagnostic function to check the correctness of control store.
- The I/O subsystem provides the system booting function. This function involves the multi-stage bring-up of the system using the boot files stored on one of several boot devices. The IOP runs the software that bootstraps from the raw machine to a fully-functional Star workstation.

- The I/O subsystem forms the basis of the diagnostic capability of the Dove workstation. Since the IOP can, to some degree, control all other subsystems, it can, therefore, selectively exercise and diagnose problems in these subsystems.
- The I/O subsystem provides the hardware and most of the software for the PC emulation function.
- The I/O subsystem provides the framework by which optional devices can be attached to the Dove workstation. Control of the various Options slots is exercised by the IOP.
- The I/O subsystem contains a 128-byte EAROM for storage of system configuration information (see Ref. [11]).

6.3.1 I/O subsystem functional blocks

The I/O subsystem is based on a high-performance microprocessor with a small amount of local memory. A logical block diagram of the Dove workstation indicating the I/O subsystem is shown in Figure 6.3.1A. The subsystem has a traditional microprocessor bus architecture to which different memory devices and I/O controllers can be connected. All I/O devices planned for Dove, except the display controller, will interface to this bus. This includes high-speed devices like the Ethernet controller and rigid disk controller, medium-speed devices like the floppy disk controller and serial communication controllers, and low-speed devices like the keyboard and mouse. The microprocessor bus will also be extended to the Options slots, where additional peripheral controllers can be added.

To the extent possible, the I/O controllers are commercially-available devices directly compatible with the microprocessor bus. Some controllers, such as the rigid disk controller, require direct channels to main memory to satisfy their bandwidth and latency requirements. In addition, special features, not normally found in commercial controllers, have been added to several controllers.

The I/O subsystem, therefore, essentially consists of the I/O Processor (IOP) and the various device controllers. In addition, there is hardware to interface to the other Dove workstation subsystems, such as the Mesa processor and memory controller. The rest of this section describes these functional blocks in more detail.

6.3.1.1 I/O processor

The Dove I/O Processor (IOP) is based on the 8 MHz Intel 80186 microprocessor. The 80186 contains an enhanced 8086 processor, as well as several other devices normally found in microprocessor-based systems. A so-called integrated microprocessor, the 80186 also contains an on-board DMA controller, interrupt controller, timers, and clock generator.

The IOP, therefore, uses a traditional microprocessor bus architecture augmented by the special functions needed to support the Dove I/O requirements. The processor has access to its local memory, as well as to the main system memory via the memory controller. The IOP is fully interrupt driven. The IOP bus structure can be extended through additional Option slots.

As mentioned above, the IOP controls and communicates with the Mesa processor. The control function involves the resetting, halting, and starting of the Mesa processor, as well

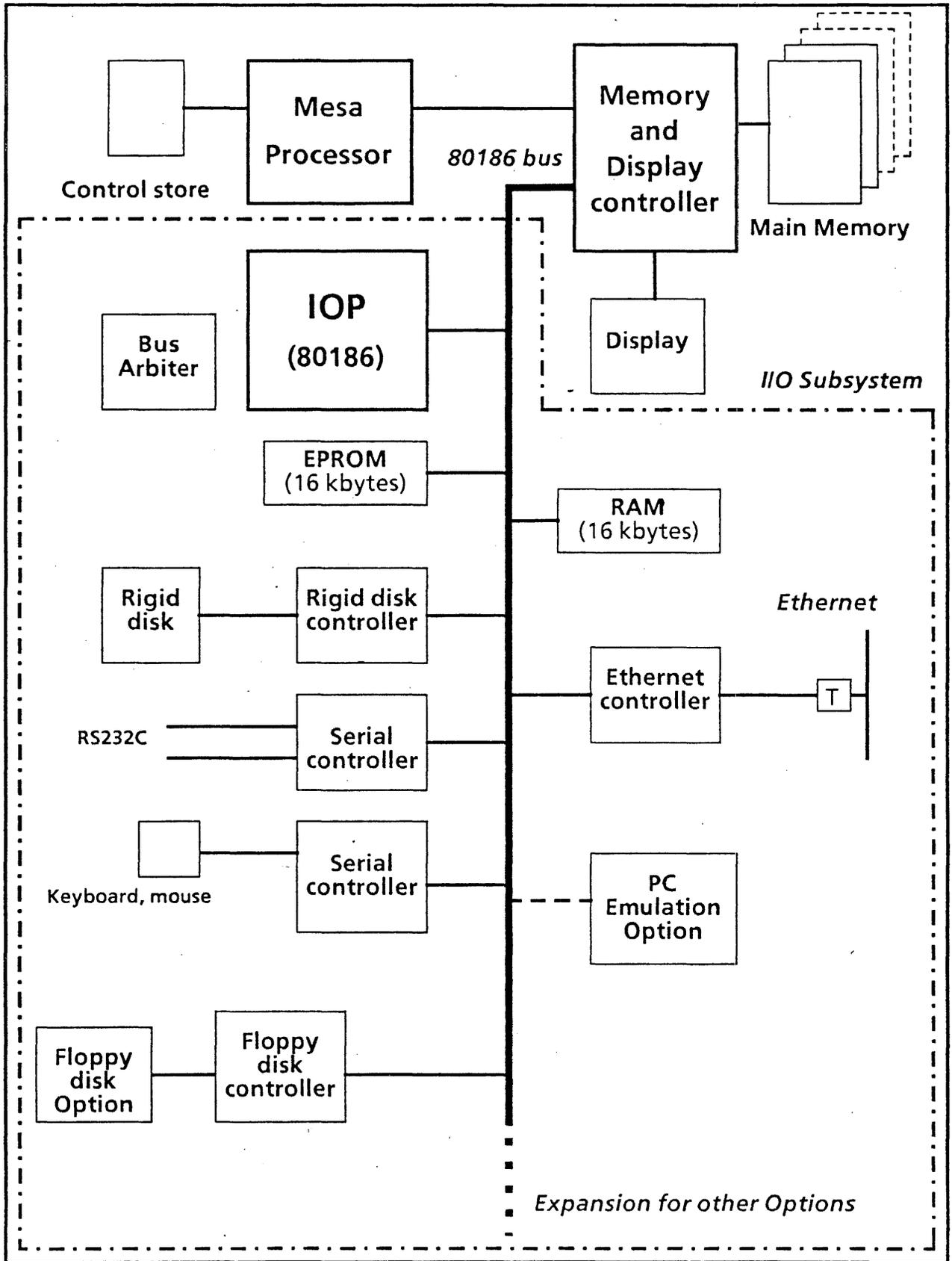


Figure 6.3.1A Dove workstation block diagram

as the reading and writing of control store. The interface to control store differs between the Daisy and Daybreak Mesa processors. The IOP can interrupt the Mesa processor, as well as receive interrupts from the Mesa processor

6.3.1.2 Local memory

The IOP contains a small amount of local memory. The local memory consists of 16 kbytes of EPROM and 16 kbytes of static RAM. The EProm contains booting and initialization software, minimal diagnostics, and the debugger kernel. The RAM is used for the operating system software, the interrupt vector table, and for local buffering.

6.3.1.3 IOP bus arbiter and mode control

The 80186 can support a single external (to the 80186) bus master. (Internal bus masters are the 80186 processor and the integrated DMA controller. The 80186 itself takes care of the bus arbitration function between internal bus masters.) The I/O subsystem, however, requires the use of three external bus masters, viz. the rigid disk DMA controller, the Ethernet controller, and the PC emulation (PCE) processor (also an 80186). There is, therefore, a need of an external arbiter to handle the four bus masters. In addition, a function called *mode control* is required to switch the bus between the IOP 80186 and the PCE 80186 execution.

The function of the bus arbiter can be summarized as follows. First, the arbiter fields HOLD requests from the rigid disk and Ethernet controllers. It determines the highest priority device; Ethernet is given first priority, the rigid disk is second. The arbiter then passes the HOLD request to the mode control function. HOLDA is then passed from the mode control to the controller being granted the bus. When the Ethernet requests service, the arbiter suspends rigid disk DMA activity.

The mode control functions are: Determine which of the two 80186s should be bus master. Pass the HOLD request from the arbiter to the current 80186 bus master. Pass HOLDA from the bus master to the arbiter.

The IOP to PCE bus switch is under IOP control (caused by an output instruction). The PCE to IOP switch is caused by any interrupt, PCE I/O trap, or RESET.

6.3.1.4 Rigid disk subsystem

The rigid disk subsystem in the IOP provides support for rigid disk operation on the Dove workstation. The rigid disk is used on the workstation for the following functions:

- Local permanent file storage
- Virtual memory swapping for the Pilot operating system
- System booting

The subsystem supports labels and the various disk operations required by the Pilot operating system. This requires the use of a customized controller. The main components

of the rigid disk subsystem are: the disk drive, the rigid disk controller (RDC), the DMA controller, and the rigid disk FIFO. (See Figure 6.3.1.4A)

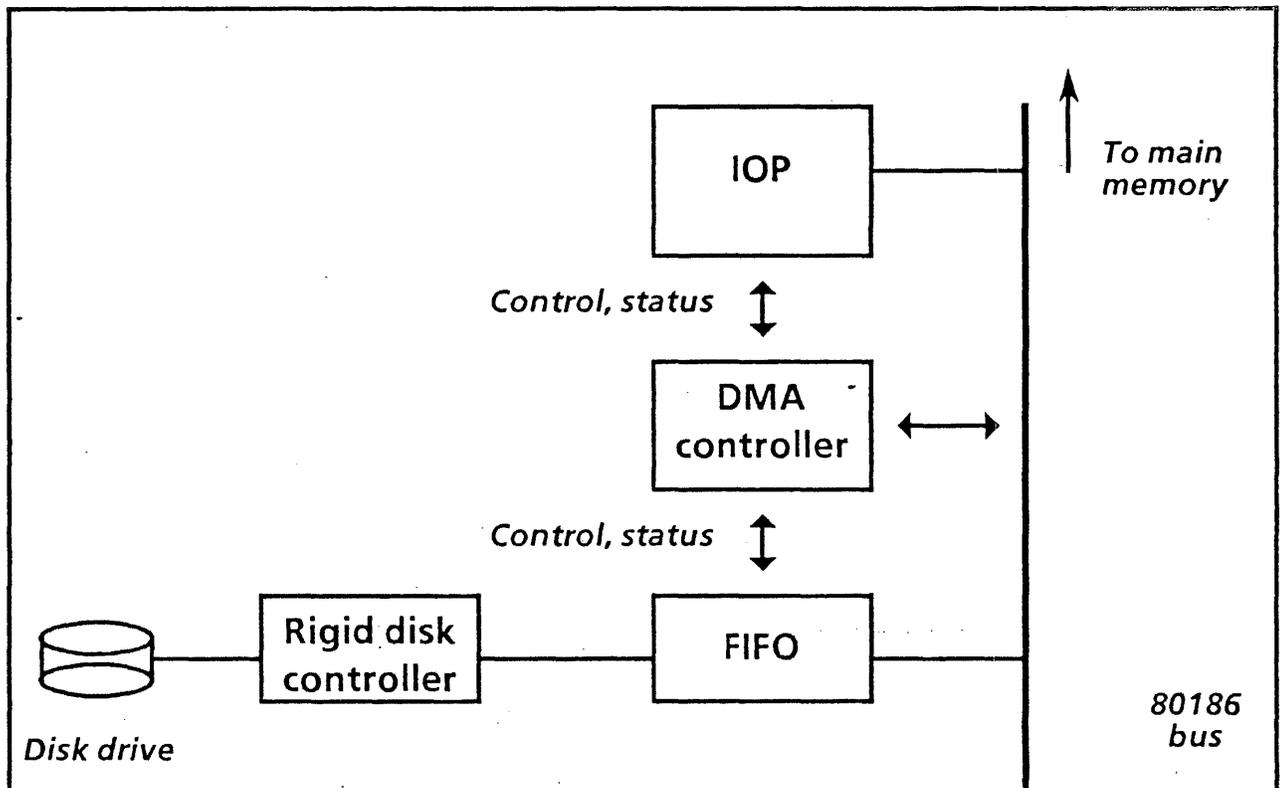


Figure 6.3.1.4A Rigid disk subsystem block diagram

Rigid Disk Drives

Only a single drive is supported, either half- or full-height. The performance requirements of the drive should meet or exceed the Shugart SA1004 performance characteristics. The drive is a 5¼" Winchester unit with the ST412/ST506 interface. The data rate is 5 Mbps. The nominal unformatted capacities are 10 MBytes (baseline), 20, 40, and 80 MBytes (optional). Potential drives that can be used (together with their unformatted capacities) are:

- Seagate ST 212 (12.8 MB), Quantum 520, 540 (21 MB, 42 MB)
- Micropolis-1303 (35 MB), Atasi 3075 (75 MB), Maxstor XT-2085 (89 MB)

Rigid Disk Controller

The rigid disk controller (RDC) provides direct control of the drive. It is implemented using an 8X305 microcontroller and a Western Digital rigid disk controller chip set. The 8X305 is a fast 8-bit microcontroller with a 256 byte scratchpad memory and a 1Kx24 PROM control store. All RDC components are off-the-shelf components. The support of the nonindustry-standard format and operations are implemented by customized controller microcode. The controller will work with any 5¼" drive which supports the ST412/ST506 interface. Control, data, and status blocks are transferred between main

memory and the rigid disk controller using the DMA controller and FIFO. The controller can read, write, or verify any number of contiguous sectors; it will switch heads if necessary. The commands supported are: Format, Verify, Write Data, Write Label, Read Data, Read Label, Check Sector, Read Next Sector.

DMA Controller

The function of the DMA controller is to effect the direct data transfers between the rigid disk controller, FIFO, and the main memory. Performance requirements of the rigid disk subsystem are such that the integrated DMA controller on the 80186 is not suitable for this function. Therefore, an external, faster DMA controller has been implemented. This DMA controller is an 80186 bus master, and completes the data transfer in a single bus cycle (as opposed to two bus cycles in the internal DMA controller). Other features are: it is programmable by the IOP (Starting Address, Word Count, and Transfer Direction); it can transfer up to 256 words (of 16 bits) at a time; it provides 24 bits of address to the main memory controller; it can transfer data at the full 80186 bus rate; and it provides an end-of-transfer interrupt to the IOP.

Rigid Disk FIFO

The function of the rigid disk FIFO is to buffer the data between the rigid disk controller and main memory. This is needed in order to isolate the processor main-memory subsystem from the inherent latency characteristics of the rigid disk. The FIFO is 512 words long (2 sectors), and supports bidirectional access (memory-to-disk and disk-to-memory). It is simultaneously and asynchronously accessible by the DMA and RDC.

6.3.1.5 Ethernet controller

The Ethernet controller provides a connection between the Dove workstation and the Ethernet. See Figure 6.3.1.5A for a block diagram. The controller is implemented using an integrated data link controller (Intel 82586) and an integrated serial interface (SEEQ 8002). The controller is, therefore, essentially implemented using two off-the-shelf chips. The Ethernet controller is compatible with the IEEE 802.3 standard (see Ref. [15]).

The controller acts as one of the I/O subsystem bus masters. All data and control transfers are performed under DMA control. The DMA controller is implemented within the data link controller chip.

The controller functionality can be briefly described as follows: All communication between the controller and the IOP occurs through common memory (either local IOP memory or system memory). All commands, data, and status information are communicated through memory data structures. The IOP can interrupt the Ethernet controller and vice versa. The controller thus requests the I/O bus whenever it needs information from or has information for the IOP. In addition, several diagnostic features such as error checking and loopback modes are available.

The Ethernet host address is stored in a PROM in the I/O subsystem.

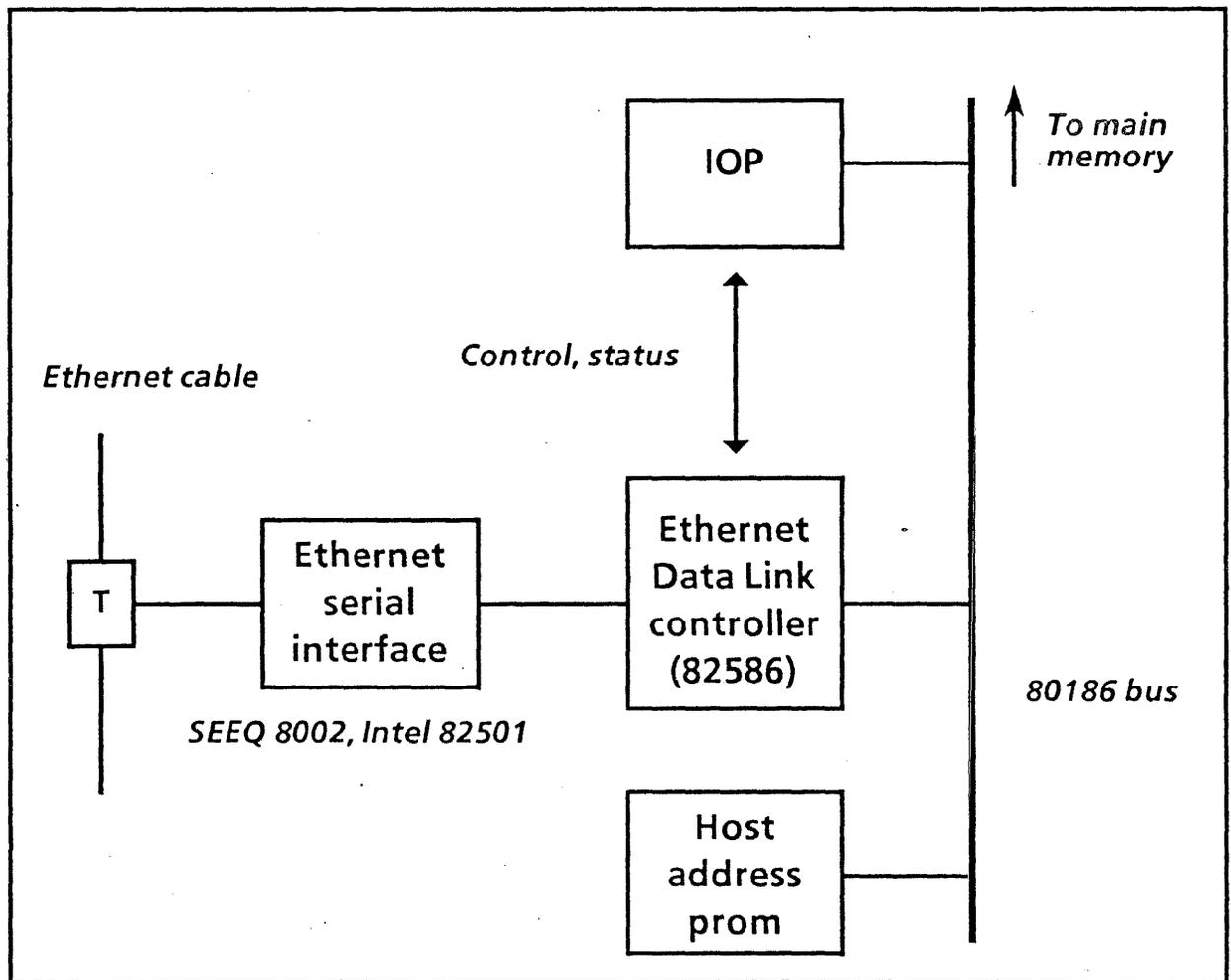


Figure 6.3.1.5A Ethernet controller block diagram

6.3.1.6 Floppy disk subsystem

Floppy Disk Drives

The floppy disk subsystem can support one 5¼", double-sided and single/double density floppy disk drive at a time. The drive is a half-height device. The interface to the drive is compatible with the Shugart SA455/465 drives. The drives have a 250 kbit/s transfer rate. Two types of drives can be supported, viz. 48 tpi drives (IBM PC compatible), and 96 tpi drives (not IBM PC compatible). The drives rotate at 300 rpm. These correspond to the following drives:

48 tpi: Shugart SA455 (double-sided, double density, 40 tracks per side)

Unformatted capacity/diskette: 500 kbytes

Formatted capacity/diskette (9 sectors per track): 360 kbytes (actually 368.6 kbytes)

Note that the 320 kbytes capacity is the earlier IBM PC formatting (pre-DOS 2.0) of 8 sectors per track.

96 tpi: Shugart SA465 (double-sided, double density, 80 tracks per side)

Unformatted capacity/diskette: 1,000 kbytes
Formatted capacity/diskette (9 sectors per track): 720 kbytes (actually 737.3 kbytes)

Floppy Disk Controller

The controller is implemented using an off-the-shelf integrated floppy disk controller chip (Intel 8272A) and a phase lock, loop chip (Standard Microsystems). The controller transfers its data under control of the integrated DMA controller in the 80186. Control and status transfers are provided directly by the 80186 processor. The controller interrupts the IOP for service. The controller is directly compatible with the IBM PC floppy disk controller.

6.3.1.7 RS-232 controller

The RS-232C controller will have two serial channels available. Asynchronous, byte- and bit-synchronous transfers are supported; data rates up to 9600 bps are possible. Byte-synchronous protocols will include IBM Bisync, while bit-synchronous protocols will include SDLC/HDLC.

The controller is implemented using an integrated, multi-protocol serial controller (Intel 8274). This chip supports the above requirements directly and also provides parity and CRC generation and checking. Two bytes of buffering is provided in the controller.

The RS-232 controller will have the first port configured as a DCE port; the other will be configured as a DTE port. The DTE port is intended to connect to communication equipment for remote and standalone workstations. The DTE port is primarily intended for local printers, and will typically operate in asynchronous mode as a TTYPort.

6.3.1.8 Keyboard and mouse controllers

This controller supports a low-profile keyboard interface. The interface is an asynchronous serial interface with a data rate of 9600 bps. The IOP communicates over this interface to the keyboard processor. The keyboard itself will contain a mouse controller. The information transferred over the keyboard link will, therefore, contain both keyboard and mouse data.

6.3.1.9 I/O subsystem options

The IOP architecture is extendable to provide for future addition of devices to the system. These devices, termed Options, are of two types, viz. the special PC emulation (PCE) option, and the general options. The PCE emulation function employs an additional 80186 processor and interfaces directly to the inner 80186 bus. The general options interface to a derived IOP bus. The options devices are housed in the Options slots. The Daisy workstation has three general options slots and the special PCE slot. The Daybreak workstation has one general options slot, together with the special PCE slot.

PC Emulation Option

The PC emulation option uses a coprocessor identical to the IOP (i.e., an 80186). It shares the inner IOP system bus with the IOP and acts as a bus master when executing. It executes from a restricted memory address space in main memory. The allocation of bus control to the IOP 80186 or the PCE 80186 is controlled by the arbiter and mode control. (See Section 6.3.1.3.)

All PCE 80186 I/O operations are trapped and serviced by the IOP. The PCE processor does, therefore, not have direct control of the PCE I/O devices. In addition, there is Mesa microcode support for the PCE display emulation.

The main components of the PCE function are as follows:

- PCE 80186: This is the processor that executes the actual PC software. It executes using the 80186 system bus, and executes only out of main memory.
- IOP/PCE
Mode Control: This logic determines which of the 80186 processors should have control of the 80186 bus. (The logic is located on the IOP board.)
- I/O Trapper: This device latches all PCE I/O operations, latches 80186 status to distinguish read or write operations, and converts I/O operations to memory operations in the PC bank in main memory. The IOP is then interrupted, and the PC processor is removed as the bus master.
- Display Trapper: A 16 kbyte area of main memory contains the PC display bit map. The PC display memory is divided into 50 areas with a dirty bit for each area in the display trapper. A master dirty bit is set by the IOP to alert Mesa processor microcode of any change to the bitmap. Mesa microcode will maintain the PC display bit map in the PCE window.

General Options

A buffered IOP bus is provided at the general Options slots. This bus is, therefore, not the internal systems bus, but is a derived IOP bus. Therefore, not all I/O system functions are available on the options bus. The bus has a buffered address bus (16 bits), and a buffered data bus (16 bits). 16 kbytes of 80186 I/O address space is allocated to the Options slots. Eight interrupts are available. No bus master or DMA capability is currently provided.

The options devices are thus intended to be moderate-to-low bandwidth devices. No high-speed data paths are provided to the system, since the bandwidth availability is limited.

No general options have been defined in detail, but likely candidates that have been identified are: digital voice and telephone management, time and date support, and data encryption.

6.3.1.10 I/O subsystem physical implementation

All components of the I/O subsystem are common to both Daybreak and Daisy, and the boards plug into an identical backplane. All the IOP electronics are located in the System Unit. The electronics are housed on the IOP PWBA (size 16" x 10.9"), the PCE PWBA (size 5" x 10.9"), and any options PWBA's (each size 5" x 10.9"). Figure 6.3.1.10A indicates the location of the I/O subsystem PWBA's in the backplane.

The locations of the IOP peripheral devices are as follows: the rigid disk drive is housed in the System Unit; the floppy disk drive is located in a separate module that sits on top of the System Unit; the keyboard and mouse are located on the user's desktop near the display unit; and the Ethernet transceiver is located at some remote distance from the System Unit, typically in the area above the ceiling where the Ethernet cable is situated. The external I/O connections to the electronics are made at the rear of the System Unit.

6.4 Peripherals

The Dove peripherals include the following parts of the system:

- Rigid disk drive
- Optional floppy disk drive
- Keyboard
- Mouse
- Displays

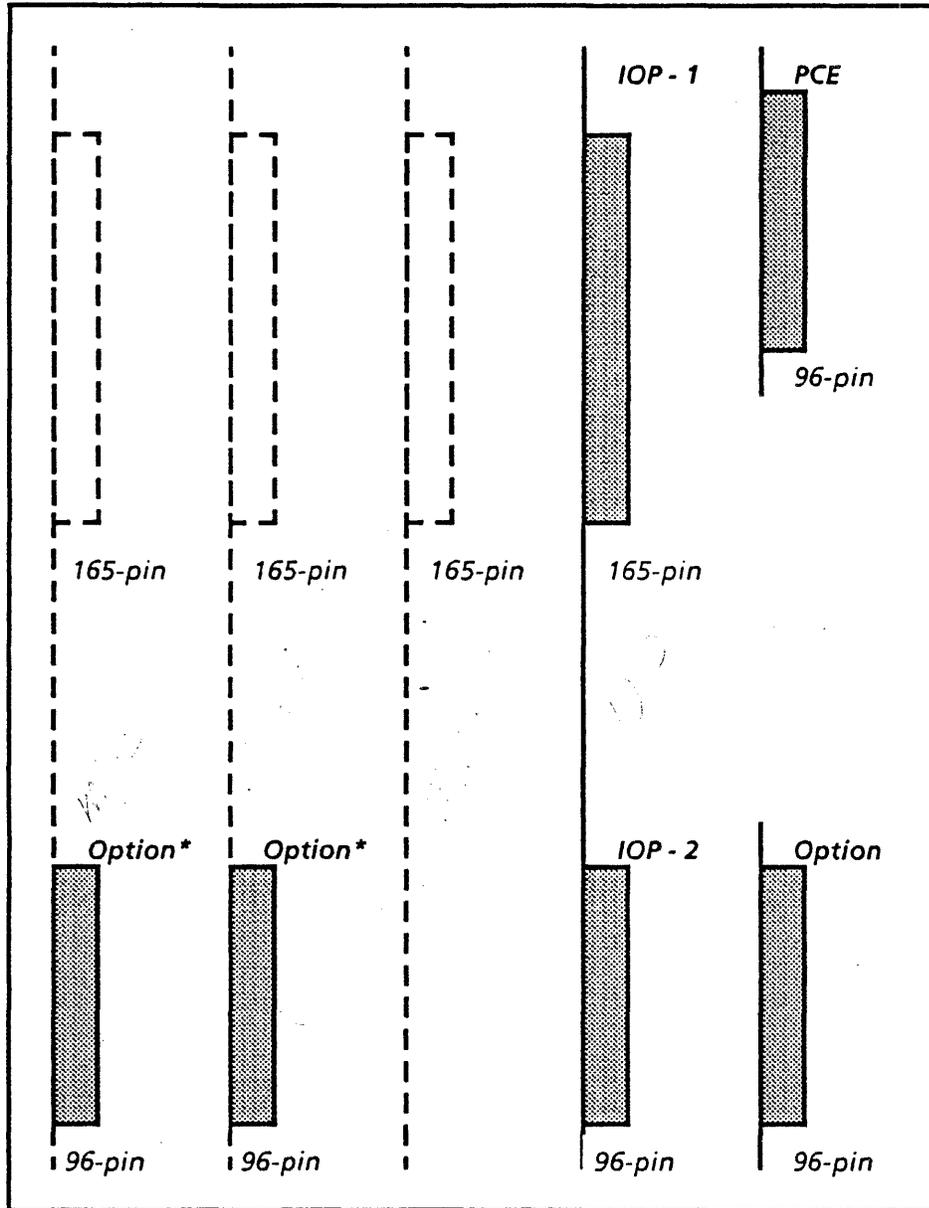
6.4.1 Rigid disk drives

Only a single drive is supported, either half- or full-height. The performance requirements of the drive should meet or exceed the Shugart SA1004 performance characteristics. The drive is a 5¼" Winchester unit with the ST412/ST 506 interface. The data rate is 5 Mbps. The nominal unformatted capacities are 10 MBytes (baseline), 20, 40, and 80 MBytes (optional). Potential drives that can be used (together with their unformatted capacities) are:

- Seagate ST 212 (12.8 MB), Quantum 520, 540 (21 MB, 42 MB)
- Micropolis 1303 (35 MB), Atasi 3075 (75 MB), Maxstor XT-2085 (89 MB)

6.4.2 Floppy disk drives

The floppy disk subsystem can support one 5¼", double-sided and single/double density floppy disk drive at a time. The drive is a half-height device. The interface to the drive is compatible with the Shugart SA455/465 drives. The drives have a 250 kbit/s transfer rate. Two types of drives can be supported, viz. 48 tpi drives (IBM PC compatible), and 96 tpi drives (not IBM PC compatible). The drives rotate at 300 rpm. These correspond to the following drives:



* Daisy only

Figure 6.3.1.10A I/O subsystem in backplane

48 tpi: Shugart SA455 (double-sided, double density, 40 tracks per side)

Unformatted capacity/diskette:	500 kbytes
Formatted capacity/diskette (9 sectors per track):	360 kbytes (actually 368.6 kbytes)

Note that the 320 kbytes capacity is the earlier IBM PC formatting (pre-DOS 2.0) of 8 sectors per track.

96 tpi: Shugart SA465 (double-sided, double density, 80 tracks per side)

Unformatted capacity/diskette:	1,000 kbytes
Formatted capacity/diskette (9 sectors per track):	720 kbytes (actually 737.3 kbytes)

6.4.3 Keyboard

The Daisy keyboard will be a low-profile keyboard with an adjustable tilt. In addition, it will be developed to conform with applicable ergonomic standards. (See Ref. [7].) The keyboard will connect to the display unit via a single coiled cord. The cord will assume an unobtrusive position whenever the keyboard is aligned with and in front of the display. Keystroke codes will be communicated to the IOP serially by a microprocessor in the keyboard. The mouse will connect to the keyboard, and the mouse tail can be dressed for right- or left-handed operation.

The keyboard will have an integral ten-key pad. The choice to include the ten-key pad in the keyboard housing is based on several factors. The built-in pad reduces the number of boxes in front of the display from three to two, thus reducing the clutter. Marketing estimates that 70% of the users will want a ten-key pad. Building in the ten-key pad reduces the UMC by \$30 for 70% of the customers, and increases the UMC by \$10 for the remaining 30%.

A new keyboard layout will be required to accommodate the present Star keyboard, PC emulation, and the ten-key pad. A proposed keyboard layout is shown in Figure 6.4.3A.

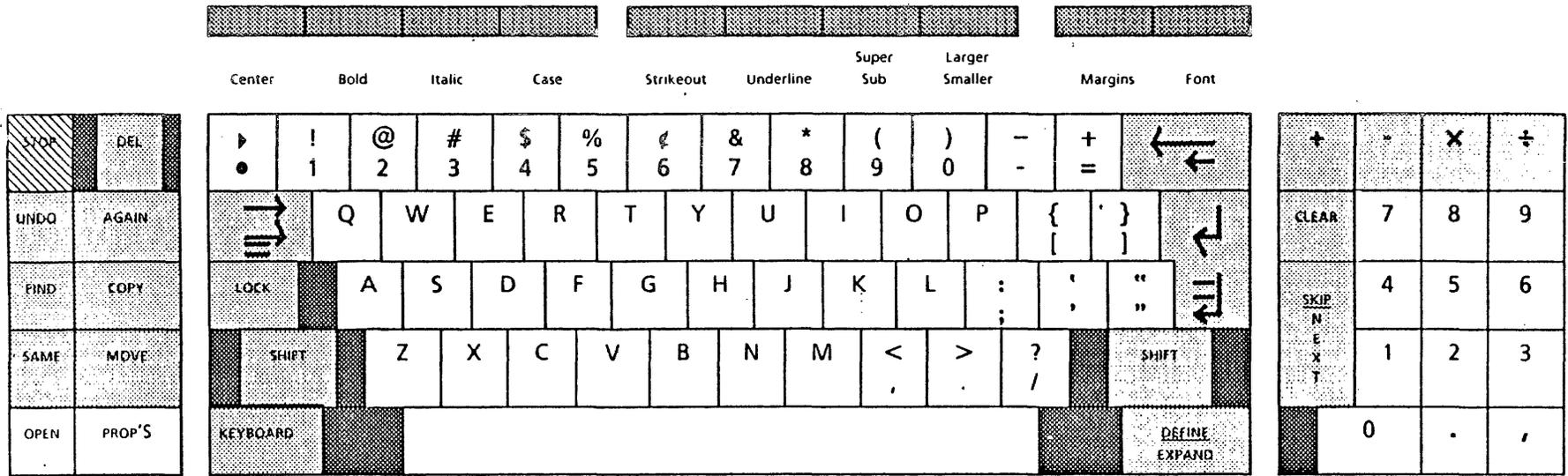
6.4.4 Mouse

The ED optical mouse will be used on this machine and connects to the keyboard. No changes in the design of the mouse are anticipated at this time. Two- and three-button mice will be supported.

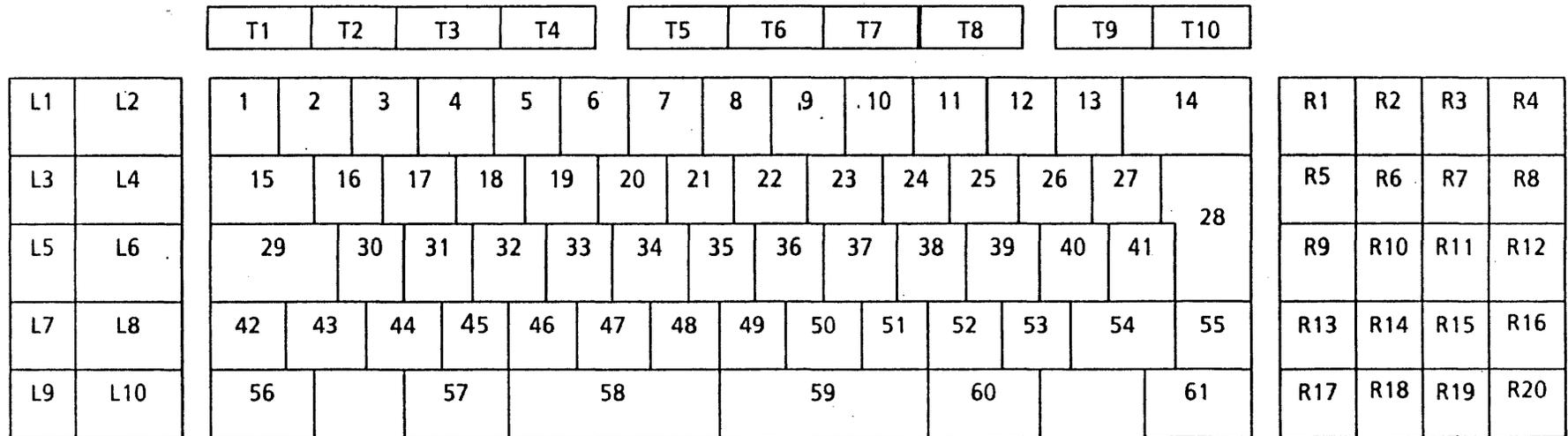
6.4.5 Displays

This section describes the various display options for Dove. Two monochrome bit-mapped displays are available for Dove: a 19" Very Large Format display (VLF), and a 15" Medium Format display (MF). The VLF display and the MF display are both new to the Xerox product line. While both displays have the same resolution of 80 bits/inch, the MF is physically smaller, displaying fewer bits and, therefore, having a lower bandwidth requirement than the VLF.

The electrical interface will be implemented using ECL techniques, similar to those used in Dandelion.



US Key assignments



Total Key numbering

- Grey key tops for "function" keys.
- Dark grey areas represent depressions which aid in locating hands without looking.
- The STOP key should be red.

Variations:
 Japanese layout has all the keys shown with normal width typing keys at 42 and 55.
 US and EUR layouts have only one space-bar (57, 58, 59, 60).
 EUR layout has a normal width typing key at 43 with a small shift at 42, one key on 54 and 55.

Key counts:

	<u>Japan</u>	<u>US</u>	<u>EUR</u>
Typing array	61	56	57
Left functions	10	10	10
Right functions	20	20	20
<u>Top functions</u>	<u>10</u>	<u>10</u>	<u>10</u>
Total	101	96	97

The Dove displays are powered by their own internal switching power supplies designed by the display manufacturer. AC power is routed through the system unit to the displays. There are two different power supplies for 110 and 220 volt operation. Each display will be configured when manufactured for 110 or 220 volt operation.

Very Large Format Display (VLF)

Video bit rate:	55.47MHz
Physical size:	11.56" high by 14.8" wide bitmap display
Visible area:	925 lines by 1184 bits
Refresh rate:	38 Hz
Border area:	32 bits wide by 32 lines high
H-line blanking bits:	304 bits
H-front porch bits:	0 bits
H-sync pulse bits:	304 bits
H-back porch bits:	0 bits
Active scan line bits:	1184
Total bits per line:	1488
Active lines per field:	462.5
V-blanking time:	28 lines
V-front porch bits:	0
V-sync pulse bits:	28 lines
V-back porch bits:	0
Total lines per field:	490.5
Field rate:	76Hz
Resolution:	80 bits/inch

It should be noted that all figures for the VLF display are preliminary, and the actual figures may vary slightly.

Medium Format Display (MF)

Video Bit Rate:	30.919MHz
Physical size:	approx. 8.7 " by 11 " bitmap display.
Visible area:	697 lines by 880 bits.
Refresh rate:	38Hz
Border area:	32 bits wide by 32 lines high
H-line blanking bits:	224 bits
H-front porch bits:	64 bits
H-sync pulse bits:	160 bits

H-back porch bits:	0 bits
Active scan line bits:	880 bits
Total bits per line:	1104
Active lines per field:	348.5
V-blanking time:	20 lines
V-front porch bits:	0 lines
V-sync pulse bits:	20 lines
Total lines per field:	368.5
Field rate:	76Hz
Resolution:	80 bits/inch

It should be noted that all figures for the 15" monitor are approximate at present, and may vary slightly when finally determined.

Auxiliary Color Monitor

Selection of a suitable color monitor for the requirements of OSD needs to be planned. The PARC designers have settled on a 440 line by 680 bit monitor with a color palette of 16 colors (4 bits) to be suitable for their particular application. This unit may or may not be suitable for the needs of OSD, but at the present time, these needs are not known. However, the aforementioned unit could be used by OSD internally to help determine their eventual requirements.

Monitor Description

The color monitor, which PARC has selected for use with the A-chip display controller in Daisy, is a Hitachi 2713. This is a 13" monitor with a built-in power supply (which does not appear to have any regulatory agency approvals aside from X-ray DHEW approval). The unit does, however, have a power supply that is capable of using 50/60 Hz, 100V, 120V, 200V, 220V, and 240V. These are selectable by varying the transformer taps as required. The unit also employs interlacing to reduce flicker apparent to the user.

The following characteristics are the maximums that the A chip is designed to drive.

Characteristics

Physical size:	8.6 " by 6.5 " approx. bitmap display
Visible area:	440 lines by 680 bits by 4 bit color palette
Refresh rate:	30 Hz interlaced
Scanning frequency:	15.75 KHz +/- 300 Hz
Border area:	To be determined
Video bandwidth:	25 MHz
H-line retrace:	10 µsecs or approx. 256 bits
Active scan line bits:	680 + border

Total bit times per line:	256 + 680 + border
Active lines per field:	220 + top border + bottom border
V-line retrace:	1000 μ secs or approx 16 lines
Total lines per field:	236 + both borders (approx. 268)
Field rate:	60 Hz

6.5 Packaging/cabling

The packaging strategy for this product calls for a four-unit basic package, with a fifth optional unit for a floppy disk drive.

The four units in the basic package are the system unit (housing the main electronics and rigid disk), the display, the keyboard, and the mouse.

6.5.1 System unit packaging

The system unit will contain the electronics, rigid disk, and the power supply. It is a floor standing unit that is 9.5x12x21". It is divided into three internal spaces, one for the PWBA's, one for the power supply and one for the rigid disk. (See Figure 6.5.1A.)

The only controls on the system unit are the power switch and boot switch, with appropriate indicator lights showing system status.

All PWBA's will be inserted from the rear of the unit, with the backplane accessible with removal of the front cover.

All connections to the system unit will be on the rear panel.

6.5.2 Display packaging

The display housing will be considerably different from the ones used for Dandelion. (See Figure 4.3A.) The housings for each of the displays will be similar in form. They will, however, vary considerably in size due to the size of the CRT. The displays will tilt 5° down and 15° up from horizontal and swivel 90°.

6.5.3 Keyboard

The keyboard will be low profile and will be variable tilt (5° or 11°). The main keyboard will be dished slightly with contoured keycaps. Special function keys will be color coded. There will be different keycap kits available for other languages.

6.5.4 Mouse

The system will use an optical mouse that communicates with the keyboard. No change is anticipated from current optical mouse design.

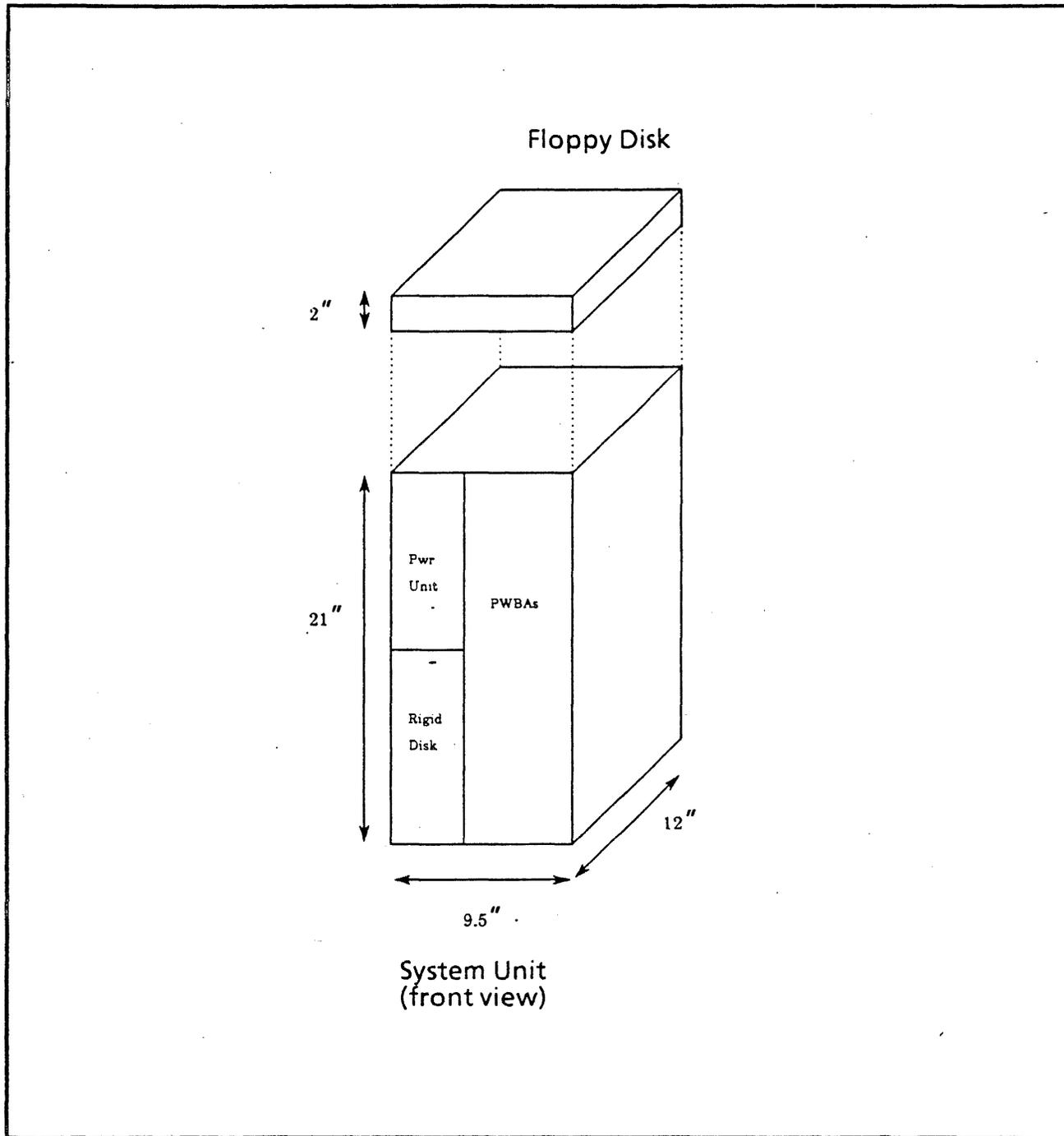


Figure 6.5.1A System physical layout

6.5.5 Floppy disk drive

The optional floppy disk drive may be mounted on top of the system unit or may be located up to four feet away from the system unit. The overall package dimensions are 9.5x12x2". The drive package is designed to blend with the system unit to give the impression of an integrated unit.

6.5.6 Cabling

In a basic unit without Ethernet or floppy disk, there will be five external cables: the system power cord, the display power cord, the display signal cable, the keyboard cable, and the mousetail. In Ethernet connected systems, there will be the net cable, and in systems with floppy disk drives, there will be two additional for power and signals to the floppy drive. The floppy, although designed to mount on top of the system unit, can be located as far as 4 feet away from the system unit.

All cabling will be light and unobtrusive, and connect to the rear of the systems unit.

6.6 Power supply

A single power supply unit provides power for Dove's system unit, keyboard, mouse, and disk drives. Enough power is budgeted to support three options cards. A separate power supply, integral to the display unit, will power the CRT.

In order to meet the requirements of all multinational AC power inputs, two slightly different configurations of the power supply have been designed. The difference is in the power supply input assembly fuses and rectifiers. (A national power cord will be provided.) There is currently a design effort to make a single power supply meet all multinational requirements.

The domestic version has a voltage doubler rectifier for 110 VAC input while the international version has a full bridge rectifier for 220 VAC input. An EME filter is an integral part of the purchased power supply. Smaller line voltage changes are accommodated by the pulse width modulation of the DC to DC converter. The DC to DC converter circuit is the same for both configurations.

The Dove system power cord will plug into a receptacle on the rear of the cabinet. The power cabling is routed to the on/off switch located on the front of the system cabinet, and from there to the actual input of the switching power supply.

Due to the UIB requirements for a power-on indicator, there will be an LED on the front panel, driven from the power supply output lines, thus indicating when power is on/off.

6.6.1 Summary of power requirements

Table 6.6.1B contains a summary of the power requirements of the various modules in Daybreak. The display is to be powered separately. The total power requirements for Daisy will be less than the total shown here. It is not known at this time what Daisy's power consumption will be.

The commercial supplies will meet all safety and emission requirements applicable to domestic and foreign qualifications. These requirements include the following:

- UL 478
- CSA22.2 No154

Module	Power (avg) (watts)	Power (max) (watts)
MPB PWBA		41
DCM PWBA (Max. Configuration)		50
IOP PWBA		54
PCE (optional)		18
Rigid disk (sufficient for Micropolis 1304)		44
Ethernet transceiver		12
Keyboard/Mouse		2
System cooling (2 DC fans)		6
Speaker/LEDs		1
Floppy disk		19
MEB PWBA (Max. Configuration)		20
Option 1		18
Total		285

Table 6.6.1B Summary of Daybreak power estimates

- IEC435 CLASS II
- VDE 0871 CLASS B
- FCC 2070 CLASS B
- SELV

6.6.2 Cooling

The system has been designed to be cooled with two fans. This was chosen to satisfy both cooling and noise constraints.



Performance requirements

In general, the requirement is that the new workstation will run Star application software at the same level of performance as a Dandelion, with identical memory size and peripherals. The hardware architecture redesign (minimal in Daybreak, but significant in Daisy) changes the set of hardware performance parameters which govern the performance as seen by the user. Accordingly, the specific measurement criteria for the product performance must be chosen carefully.

In the interim, the Star performance requirements for the baseline configuration should be that it runs Star 3.3 as fast as a Dandelion, with identical memory size and peripherals. The Star performance tests used in the Star 3.3 performance evaluation shall be used to verify that this requirement has been satisfied.

Performance requirements for the low-level software, the rigid disk, the Ethernet controller, the low-speed peripheral controller(s), and other internal hardware components are subsumed in the performance requirement specified above.

The performance requirements for the extended baseline workstation running IBM PC software should ensure that for "legal" programs, the workstation runs as fast as an IBM PC. Legal programs exclude programs which "depend in a subtle way on system timing, or which are capable of detecting very subtle differences in the hardware implementations" (Ref. [2]).

7.1 Performance analysis

It is very difficult to estimate the performance of a complicated system such as the Dove. The difficulty is compounded by the asynchronous, arbitrated interfaces. Unlike the Dandelion, the bandwidth available to an I/O device depends on the current activity in the machine. In the Dandelion, only the Mesa emulator experiences changing bandwidths with changing I/O loading. Even so, the calculation of the typical emulator performance is accurately done by considering the I/O bandwidth to be very small. Only memory refresh has a significant effect upon the Dandelion Mesa speed.

There are two main cases to be viewed in the performance analysis. The first is when the Mesa processor is locally bound. This case can be described, for example, as a case where the Mesa processor is performing computations and working in main memory. This case assumes no I/O to disks or networks. This case has been analyzed in detail for both Daybreak and Daisy, and the expected performance can be presented with considerable

confidence. This case is important as it represents the performance a user would experience in working with the system when no swapping or external communication is in process, such as during document generation.

The second is when the processor is externally bound. This case can be described as a case when the IOP bus is performing data transfers. This is the larger, more interesting and less well-known case. It is of great importance, because it represents the case when the system is multi-tasking. It is a multi-variable problem, and the total solution, comparing Dandelion with Daybreak with Daisy, is extremely complex. The knowledge of the dependencies involves both hardware and software, and all dependencies are not well defined at this time. Emulating such an ill-defined problem is difficult and time consuming at best, and we have not had the resources for an exhaustive study. We have chosen instead to examine several cases of interest and attempt to make reasonable estimates of relative performance. The first case described is, of course, a subset of the second, when external dependencies have gone to zero. Final performance analysis will be done by measurement on the actual system.

With the foregoing in mind, performance estimates are presented for the two cases. The special case of simultaneous disk and Ethernet transfers is presented. Notably missing is an estimate for "PC within Star" operation.

This section contains subsections detailing case one information on both Daybreak and Daisy relative to Dandelion, and case two information on Mesa, 80186 Bus, and Disk and Ethernet throughput. Performance estimates will be made with appropriate caveats. The estimates will generally use typical numbers instead of worst case.

7.1.1 Daybreak Case 1

Assumptions

No IOP accesses

No MESA write cycles

Memory nibble mode cycle time = 718 ns

Display nibble mode cycle time = 718 ns

Memory single word read cycle time = 312 ns

Mesa single word read cycle time = 375 ns

Mesa memory utilization = 70%

Dandelion refresh overhead = 5%

Daybreak refresh overhead = 2%

This performance analysis, and the ones following show dependencies on the display size. This is because the displays each have equal numbers of pixels per inch. This means that larger displays need more data on every line, and, consequently, require more of the machine's time for data output.

There are also dependencies on the number of memory banks. This is because each bank has its own controller, and if the display can operate out of one bank and the processor from the other, the amount of contention is less, and, consequently, performance is higher.

Case A: One bank of memory shared by both Mesa and Display.

DISPLAY	% of Dandelion
15" display:	76%
19" display:	63%

Case B: Two banks of memory, one for Display and one for Mesa.

DISPLAY	% of Dandelion
15" display:	113%
19" display:	113%

Case C: Two banks of memory one for Display and one for Mesa, but 10% of Mesa memory in display memory.

DISPLAY	% of Dandelion
15" display:	104%
19" display:	101%

7.1.2 Daisy Case 1

Assumptions

No IOP accesses

Case A: One bank of memory shared by both Mesa and Display.

DISPLAY	% of Dandelion
15" display:	82%
19" display:	71%
13" color	72%

Case B: Two banks of memory, one for Display and one for Mes.

DISPLAY	% of Dandelion
15" display:	94%
19" display:	94%

13" color

94%

For cases where memory is shared, one should interpolate between the values shown.

7.2 Case 2 (Daybreak and Daisy)

The following analysis was done specifically for the Daisy configuration only, but it is considered valid for Daybreak as well.

The analysis for this section proceeded along the lines of bus utilization. As detailed in the system block diagram (Figure 6.3.1A), the 80186 bus structure is the I/O bus for the entire machine. Therefore, analysis of this bus and the utilization of the bus under varying loads would indicate the efficiency of the data transfers. The performance numbers indicated compare different types of I/O under various loading conditions, to 100% bus efficiency, defined as transactions occurring in the minimum number of cycles of which the system is capable. In this system, 100% bus efficiency would be transactions occurring in 5 machine cycles. The performance figures shown are not related to Dandelion performance.

Several simulations were run for different configurations and scenarios. The total simulation time was 2.1 msec for every run. This figure was chosen to obtain a practical program run time and it was thought that it was acceptable for reasonable worst case statistics. For each subsystem, the following cases were considered:

1. SChip (Mesa Emulator): an almost 70% bus utilization random pattern was always considered.
2. Display: simulations were run with and without the display, which consisted of a 15" MF display where the display FIFO was 32 bytes deep starting full with a 5-byte threshold level.
3. Refresh: main memory refresh occurs every 15.6 μ s and is equivalent to a one-word read.
4. IOP186: a random bus utilization pattern was considered with 5% and 70% bus utilizations.
5. Ethernet: simulations were run with and without three Ethernet packets of medium size (312 bytes) arriving to the system. The Ethernet FIFO threshold level is eight bytes.
6. Rigid Disk: simulations were run with and without five sectors of 512 words read by the system. The disk FIFO depth is 512 words.

Following is a listing of the configurations simulated, and, in the last column, the expected bus performance. The performance percentages indicated is the bus performance relative to a 5 state bus service, the best that can be achieved by the A chip. The absolute minimum required by the 80186 for a bus service is 4 states. These figures, therefore, show the bus efficiencies and are a strong indicator of overall performance.

Display	IOP186	Ethernet	Rigid Disk	Performance
NO	5%	YES	NO	104%
NO	70%	YES	NO	90%
NO	5%	NO	YES	115%
NO	70%	NO	YES	96%
NO	5%	YES	YES	96%
NO	70%	YES	YES	89%
YES	5%	YES	NO	98%
YES	70%	YES	NO	80%
YES	5%	NO	YES	113%
YES	70%	NO	YES	89%
YES	5%	YES	YES	86%
YES	70%	YES	YES	80%

Table 7.1.3A Simulation configurations and performance



Product configuration

The product configuration for the new family of workstations includes a baseline configuration and optional configuration. Section 4.6.1 describes the baseline configuration. Section 8.2 describes hardware options which can be used to create other configurations, and Section 8.3 gives some sample configurations.

8.1 Product requirements

The *requirements* for the new workstation product are embodied in the baseline configuration and its extensions. Requirements are the necessary and sufficient conditions for the product to be acceptable. If any of the requirements is not achieved, the product will be inadequate for the market (according to the marketing analysis and the applicable definition of success). In all cases, the objective of the development effort will be to exceed the requirements and attain more aggressive goals.

8.2 Baseline hardware requirements

In addition to the Mesa processor, the baseline configuration will support a small choice of peripherals and memory sizes.

The baseline configuration (without options) includes:

Processor: CP that executes the Mesa instruction set, with 4K control store.

Memory: 640 kbytes, including virtual memory map and display bank

Peripherals:

Display: 15" MF, bit-mapped, b/w,
approx. 80 bits/inch resolution

Rigid disk: 10 Mbyte disk with SA1004 performance or better

Keyboard: 8010 functionality, low profile, integral ten-key pad

Mouse: Optical

Ethernet: Controller for 10 Mb/sec Ethernet (transceiver, drop cable
excluded)

RS232C: Two ports, asynchronous and synchronous (maximum 9600 bps)

Packaging: Electronics and rigid disk drive in a system unit with separate display, keyboard, and mouse.

8.3 Options

Options may be added to the baseline at **additional cost** to the customer.

The options include:

Control Store: 4K words Daybreak only

Memory: Additional memory in 512 kbyte units up to 3.0 Mbytes on Daisy and 3.5 Mbytes on Daybreak. 4.0 Mbytes on Daybreak and Daisy is feasible if 256 kbit chips are used for display buffer and system memory in the first memory bank of the DCM.

Peripherals:

Display: 19" (bit-mapped, b/w, same resolution as 15")

13" color (bit-mapped, same resolution as 15")

Rigid disk: 20 MB disk with SA1004 performance or better

40 MB disk (full height)

80 MB disk (full height)

Floppy disk: 360KB or 737 KB (formatted) half-height floppy drive

Floppy controller: Housed on IOP board; components may be removable from sockets.

Ethernet: Components may be removable from sockets.

The rigid disk controller will support all configurations of rigid disks that comply with specifications ST 412/506. To exchange rigid disks in the baseline configuration, we will switch the physical disk drive and, at most, change an internal cable.

8.4 Configuration flexibility

The new workstation product will offer significantly more configurability than the current product. The customer can create special configurations by choosing from the baseline options. In addition, customers with greater demands and applications can purchase an expansion unit to increase the number of options available to them. At present, only those options described in this section are actually being developed. However, the workstation's built-in configurability will permit Xerox to respond to future market demands when they arise.



Product safety

The product shall be designed to comply with all applicable community, state, federal, international, and Xerox standards for product safety, and shall adhere to "good practice" where no general, recognized standards exist.

The system hardware shall be designed and constructed so that under normal use, it will function without hazard to anyone operating it and without hazard to the surroundings in which it is placed. Protection will be provided for careless use and application that may occur in normal day-to-day usage. Any single failure in the system will leave the system in a condition safe for the operator.

System and subsystems shall be approved by the appropriate safety authorities as specified and shall not violate those approvals when interconnected with other systems intended to be so interconnected.

It is the intention that this system meet the requirements of SELV (Safety Extra Low Voltage).

9.1 Safety standards to be met by this product

- UL 478, Underwriters Laboratories Standard, Electronic Data Processing
- CSA Standard C22. No. 154, Data Processing Equipment
- IEC Standard, Publication 435, Second Edition 1981, Safety of Data Processing Equipment
- Xerox Environmental Health and Safety Manual, Section 8.0

9.1.1 Ergonomics

This product will be designed with the intention of meeting the ergonomic requirements in the multinational marketplace. The precise regulatory requirement(s) in the area of ergonomics is not well defined. This product will be developed using the following document as a guideline:

No. ZH 1/618 Edition 10.80 Safety Regulations for Display Workplaces in the Office Sector

The above document references a number of DIN standards, many of which are in draft form. A request will be made for change to this SRS if any requirements of this document are found to be unfeasible or unreasonable for the U.S. marketplace. It is recommended that Rank Xerox review these documents/requirements and prepare a single ergonomic specification for application to this product. A preliminary version of Rank Xerox' inputs is available in Ref. [7].

9.2 Environmental requirements, maintainability, reliability

9.2.1 Environmental

Environmental requirements in this specification are defined, in the broad sense, to indicate the conditions under which this product will operate, as well as the effect this product has on the surrounding environment.

The following paragraphs identify the environmental parameters of particular concern to meet regulatory requirements and/or Xerox standards. The parameters or the standards to be met are identified along with the description of how this is to be accomplished and/or verified.

The following general principle applies to all environmental requirements except those which are regulatory in nature. This product will use subsystems and components which are standard in the industry, in addition to those unique to this product. To remain cost competitive and to produce products that are technologically in pace with or ahead of the industry, it remains desirable and sometimes necessary to avoid uniqueness in subsystems and components purchased from outside vendors. The result is often that environmental goals must be compromised. These compromises will be reviewed as and when they occur, and specifications will be modified accordingly.

9.2.1.1 Audible noise

The noise level of this product will be measured in accordance with the Xerox Corporate Environmental Health and Safety Manual, Section 8.7.0, Audible Noise Limit Specification, effective March 1, 1982. We are currently committed to achieving a 47 dBA stand-by noise level.

9.2.1.2 Electromagnetic emissions

This product will meet the following regulatory requirements for the marketing areas identified.

U.S.	FCC Docket, 20780, Class B
RX	VDE 0871, Class B/PVFG 1115, VDE 0875 (82/499/EEC)
FX	No stated requirements

The above regulations will be met by appropriate subsystem/component selection, shielding of internal and external harnesses, shielded cabinet construction if necessary and an appropriate ground design. Prototype level hardware will be tested to identify

problem areas and allow corrective design. Final production equivalent hardware will be tested to provide FCC qualification data and to demonstrate qualification to VDE for VDE listed approval.

9.2.1.3 Power line electromagnetic susceptibility

The product shall remain operational and not be electrically or mechanically damaged when subjected to Surge Withstand Capability tests as outlined in the ANSI/IEEE Standard 472-1974. The following pulse characteristics will be applied to insure that the system is not input transient susceptible:

Frequency	1.0 to 1.5 MHZ
Amplitude, crest value	2.5 KV to 3.0 KV
Decay to 50% crest value	6 microseconds minimum
Repetition rate	50 bursts per second, minimum
Test duration	2-10 seconds

For system configurations which may have subsystems deriving power from other system elements, the above transient pulses will be applied to any combination of units simultaneously. System soft errors should not occur at input amplitude levels below 2.5 KV. Hard failures should not occur at input levels below 3 KV.

This requirement will be met primarily by appropriate design of the line filter used on each subsystem that is separately powered. Verification of the design will be performed during "B" level qualification testing.

9.2.1.4 Electrostatic discharge

The system shall remain operational with no electrical or physical damage when subjected to a test designed to simulate an operator's static discharge of 7 KV to 15 KV into both conductive and non-conductive exposed parts. The discharge generator shall consist of a voltage source and a handheld single-point discharge unit of 150pF to 500pF in series with a suitable resistor, so as to generate a current of 30 amps.

Selection of discharge points on the system to be tested shall be based upon realistic considerations of where such discharges can occur in normal product use. Soft errors should not occur below 7 KV, and hard errors should not occur below 15 KV. Verification of the design will be performed during "B" level qualification testing on a system which is representative of a production unit.

9.2.1.5 Input power requirements

This system shall meet all functional requirements when operated from a power source anywhere in the operating ranges below.

The power subsystem shall not be damaged when operated continuously at any voltage from zero to its minimum operating voltage.

	Voltage Range	Frequency	Nominal Voltage
US/XCI	98 - 127 VAC	60 ± 0.5 Hz	115 VAC
RX	194 - 264 VAC	50 ± 0.5 Hz	220/240 VAC
FX	90 - 110 VAC	50 ± 0.5 Hz	100 VAC
FX	90 - 110 VAC	60 ± 0.5 Hz	100 VAC

Where possible, the design of this system will be insensitive to input line frequency within the 49 to 61 Hz range. Voltage range variations may be accommodated by use of input voltage tap adjustment, or by some scheme that in effect accomplishes this adjustment. Verification of the design will be performed during "A" level engineering model test and "B" level qualification testing on a system which is representative of a production unit. Input voltage variation will be performed on systems as they are being subjected to other environmental tests.

9.2.1.6 Temperature/humidity requirements

This system shall meet all functional requirements when operated or stored in the environment shown in Table 9.2.1.6A.

	Temperature °F	RH (%)	Altitude (feet)
Operating	50 to 90	15 to 85*	6,000
Non-operating	-20 to 150	15 to 90	25,000

Table 9.2.1.6A Temperature/humidity requirements

*with a maximum wet bulb of 26°C

The system will be designed to dissipate minimal heat. Cooling requirements will be calculated and verified in engineering model systems. Prototypes or production equivalent systems will be oven tested in the range specified above as part of "B" level qualification testing. Thermal profiles will be measured in search of hot spots which might affect system reliability. Thermal rating of the components or subsystems will not be exceeded in any condition of the system operating in the specified range.

9.2.1.7 Vibration and shock

All systems and subsystems, packaged and unpackaged, shall withstand shock and vibration that simulate conditions which may be experienced during handling or transportation. The specified impulse must be measured on a frame member nearest the side or edge for unpackaged units, and at the package exterior for a packaged unit.

For shock tests, the packaged and unpackaged systems and subsystems shall not be damaged when exposed to shock quantity, amplitude and direction as described in the

following table. The shock input pulses are sawtooth in nature and, therefore, have an energy content determined by:

$$\text{Pulse (GSEC)} = (\text{Shock Amplitude (G)} \times \text{Shock Duration (SEC)}) / 2$$

The shock duration shall normally be in the range of 10-15 milliseconds, but limited to the range of 5-50 milliseconds.

System or Subsystem Mass	Shock Input to Base	Shock Input to Each Side	Shock Input to Top
0 to 40 kg	2 @ 0.165 GSEC	1 @ 0.110 GSEC	1 @ 0.033 GSEC
40 to 105 kg	2 @ 0.125 GSEC	1 @ 0.100 GSEC	----
105 kg and up	2 @ 0.112 GSEC	1 @ 0.058 GSEC	----

Table 9.2.1.7A Vibration and shock requirements

Packaged and unpackaged systems and subsystems shall not be damaged when exposed to vibration frequencies between 3.0 and 4.4 Hz at 25 mm constant displacement, but not to exceed an acceleration of 1.25G and 4.4 to 15 Hz at 1.0 to 1.25G (maximum acceleration). The vibration test time of 1 hour should be divided proportionately to vibrate in all normally expected orientations. For example, a product which is normally transported or handled both upright and tipped on one side should be vibrated 30 minutes upright and 30 minutes on the one side. Additionally, three sweeps for resonance shall be made from 3-15 Hz and return in 1 Hz steps, at a nominal 0.5G peak acceleration. Dwell time at each frequency shall be 5 seconds. If resonance is encountered, then vibration shall be conducted at the resonant point(s) for 0.25 hours (at each point) at 1-1.25G.

At least two production equivalent systems will be subjected to shock and vibration tests on a calibrated table as part of "B" level qualification testing. Manufacturing will design the packaging of this product for shipment and perform sufficient testing to verify the design. Shipment packaging must be sufficient for customer delivery by parcel post.

9.2.1.8 Secure systems for government agencies

Some government agencies require systems which meet a unique level of security. The definition of requirements to qualify for this level of security cannot be publically discussed. Only a test house, qualified and authorized by the U.S. government, may actually test this product and make an application verifying the product meets this level of security. To minimize the hardware changes required for this product to pass this test, the product will:

1. be designed to accommodate removable storage media,
2. be designed to carefully shield all serial information path,
3. be tested by an approved test house for preliminary review as soon as a unit which reasonably represents a production system is available.



Installation, service, and maintenance

Installation, service, and maintenance can be performed by the customer. This will be realized by a combination of package design, circuit board factoring, diagnostic hardware features, diagnostic software, and documentation.

10.1 Package design and circuit board factoring

Packaging will be determined that will allow Dove to be assembled and disassembled from modules called "Customer Removable Units" (CRUs). CRUs are defined as component parts which can be removed and installed by the customer. The only tool required to assemble or disassemble Dove into CRUs will be a screwdriver. No individual CRU will weigh more than 35 lbs. The CRUs are: memory boards, processor boards (containing the Mesa processor, control store, 86 processor, and associated circuitry), various options boards, disk drive assemblies, display assemblies, keyboard assemblies, power supply assemblies, cables, and housings.

The connectors and housing will be designed such that there will be a minimal risk of incorrect installation. Whenever there is visual similarity between components, connectors will either be keyed to prevent user error, or interchangeability will be acceptable. Illustrated documentation will be available which explains installation and removal of each CRU.

Safety interlocks on high-voltage components will be provided which will prevent customers from injuring themselves or damaging the machine. Since the display will contain high voltage circuits, the case surrounding the display must be part of the display CRU.

10.2 Diagnosability

A combination of diagnostic hardware and software will be provided, which the customer can use to troubleshoot an ailing system.

The hardware will include a diagnostic feedback device which will provide status information in the event that diagnostics determine an error which prevents display of information on the screen.

Five types of diagnostic software will be provided: installation verification software, diagnostics integral to the machine booting sequence, fault handling software, fault isolation software, and extended fault isolation software.

The *installation verification software* will determine whether or not a newly-assembled (or reassembled) machine is working. It will report to the user the machine configuration and its Ethernet address.

Low level *diagnostics integral to the boot sequence* will verify the health of components by using them and reporting the boot progress on the diagnostic feedback device. As soon as enough machinery is available to report progress on the display, the display will show this status information.

Where possible, hardware failures during program execution will be caught by *fault handling software* which will report the nature of the fault to the user. (See Ref. [10].)

Fault isolation diagnostics will be provided which will isolate faults to a specific CRU with a 95% accuracy. *Extended fault isolation diagnostics* will be provided which will isolate faults to specific FRUs on the faulty CRU.

Except for the extended isolation diagnostics, all of the diagnostic software described will be designed for use by the customer. Documentation to guide the intelligent layman through the troubleshooting process will be available. The extended isolation diagnostics are intended for use by trained service personnel. They may require the use of tools not normally available to a customer.

Extended isolation diagnostics tools include turn-around connectors, oscilloscopes, voltage meters, and chip removal tools.

In addition to diagnostic software, there will be a maintenance program and associated documentation as a guide for the alignment and adjustment of the display. This package will include illustrations of test patterns and corrections for particular deviations from the patterns.

10.3 Service strategy

~~Several installation and service strategies are anticipated.~~ The strategies differ in level of user involvement: Customer Provided Service, Depot Service, and Field Service. A scenario for each strategy is provided below.

10.3.1 Customer-Provided Service

In this strategy, the customer is the primary provider of service. The customer will install the machine when it arrives at the site and repair the machine when it fails.

Installation - The machine will be packaged in units which can be shipped ~~via parcel post~~ ^{Commercial} to the site. After unpacking and reading the documentation package, the customer will unpack the other packages. These packages will contain CRUs partially assembled together. The customer will finish assembling each unit of the system and install connecting cables.

The last step in the assembly process will be the installation of the power cord. The hardware installation process terminates with the customer successfully running the installation verification program. If the installation verification program fails, the customer will use the troubleshooting guide as an aid in correcting the situation. After successful hardware installation, the software installation procedure begins.

Service - Hardware failure will be indicated by fault handling software, failure of the boot sequence, and erroneous system behavior. When the customer suspects a failure, the fault isolation software will be used to determine the CRU most likely needing repair. The customer will remove the suspect CRU and take it (or send it) to a repair center where it can be repaired or replaced. After installing the new CRU, the customer will execute the diagnostic programs to verify the correction. (For some failures, there may be an iteration through more than one CRU. The first indicated CRU will be the successful choice 95% of the time.)

10.3.2 Depot Service

In this strategy, the customer is still the primary provider of service. The customer will install the machine and remove it to the service center when a failure is suspected.

Installation - The installation procedure is as described above for Customer-Provided Service. If the installation verification program fails, the customer removes the unit to a service center for guidance and assistance.

Service - Hardware failures will be indicated as described above. However, the customer will not attempt fault isolation. The customer brings the entire machine (some disassembly will be required) to a service center for fault isolation and repair. The service center personnel will then execute the same diagnostic package that the customer is supplied in the Customer-Provided Service. They will also have extended fault isolation software. On isolating the fault, the machine will be repaired, and the customer will return it to the customer site.

10.3.3 Field Service

Some customers require and are willing to pay a premium price for service at the customer site by Xerox Technical Representatives. These customers will be provided installation and service in a manner similar to that used for Dandelion. All of the diagnostic software described above will be applicable when Field Service is the provider of service instead of the customer. Field Service technicians will also use the extended isolation diagnostic programs and may replace FRUs.

10.4 Service time and reliability estimates

This section describes the expected installation and service times, the frequency of unscheduled maintenance, the cost of service, and the preventive maintenance required for Dove. The estimates in this section are preliminary. Service strategies for Dove will be quite different, and this complicates predictions. (Service cost estimates are not provided; they cannot be accurately calculated until we better understand the nature of the service arrangements.) Where possible, reliability rates are derived from Dandelion data. Dove is expected to improve on these numbers.

10.4.1 Installation time

The following estimates of worst-case installation time are derived from "educated guesses" about the time required to perform common tasks, and the assembly of six to ten separately-packaged components.

Reading of assembly instructions	10 minutes
Unpacking of components	5
Assembly	10
<u>Execution of verification program</u>	<u>5</u>
Total	30

10.4.2 Removal time

Disassembly	10 minutes
<u>Packing</u>	<u>5</u>
Total	15

10.4.3 Repair time

The following estimates are derived by examining the repair times for the Dandelion. The Dandelion estimates for fault isolation to a single PWB are used for fault isolation estimates here. The Dandelion estimates for the replacement of a 10 Mbyte disk drive are probably most similar to a customer's replacement of a CRU for Dove. (Complete disk replacement is almost the worst case item for Dandelion; the signal harness actually takes longer to repair.) Since the impact of Customer-Provided Service is not well understood, these numbers are very rough. Travel time, parts procurement, and administrative time are unknowns.

Execution of fault isolation software	12 minutes
Machine open	3
CRU replacement	25
<u>Machine close and checkout</u>	<u>5</u>
Total	45

10.4.4 Scheduled and preventive maintenance

Dove requires no scheduled or preventive maintenance.

10.4.5 Unscheduled maintenance

Reliability estimates for CRUs are provided below in Table 10.4.5A. The estimates are derived from reliability estimates available for Dandelion. The source of most of these rates is a report generated by ED Reliability Engineering. The rates reflect the number of times a subassembly should cause a service call. Subassembly predictions are made by totaling reliability data on each component. We have assumed, in the absence of better methods, that boards of similar complexity on Dandelion and Dove will have similar failure rates.

CRU	Engineering /1000 hrs	Program /1000 hrs	2600 Hour Year	1750 Hour Year
MPB PWBA	0.03	0.04	0.111	0.075
DCM PWBA	0.05	0.06	0.162	0.109
IOP PWBA	0.04	0.05	0.139	0.093
SAM PWBA	TBD	TBD	TBD	TBD
MEB PWBA	TBD	TBD	TBD	TBD
Display Assembly	0.08	0.11	0.286	0.193
Rigid Disk Assembly	0.10	0.14	0.364	0.245
Floppy Disk Assembly	0.10	0.14	0.364	0.245
Keyboard Assembly	0.08	0.11	0.286	0.193
Power Supply Assembly	0.03	0.04	0.104	0.070
Cables & Harnesses	0.01	0.01	0.026	0.018
Optical Mouse Assembly	0.00	0.00	0.000	0.000
PC Emulation Option PWB	0.01	0.01	0.026	0.018

Table 10.4.5A Expected CRU failure rates

These estimates are suspect and represent "educated guesses" at best. It is thought that actual reliability will be better than the quoted rates. Reliability is unknown for the S chip, A chip, 80186 processor chip, and many of the components.

The Engineering/1000 hours column indicates expected failure rates due to actual component failures. The Program/1000 hours column indicates failures caused by other factors. This number is 30% higher than the Engineering/1000 hours number. The last two columns refer to annual failure rates. Field Service considers a year to be 2600 hours, while the workstation goals use a 1750-hour year figure.

The reliability estimates available for Dandelion include a row for "software-caused service calls." We have not included this information, since it is actually unrelated to the hardware described here.

The expected failure rates for all rotating memories are thought to be the same (0.10 failures per 1000 hours).

The expected failure rates for displays represent actual repairs and do not include adjustments. All displays are assumed to have similar failure rates (.08 failures per 1000 hours).

The expected failure rates for optical mice are 1.6442 failures per million hours.