820DIFF
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10/6/85

This small file is a composite difference description between the 820-I Etch 1 and 820-I Etch 2. An assumption is made that you have one or the other (hopefully, both) of the 820 schematics. In addition, I would like to thank Dan Costello for helping me out with this document by providing some nicely drawn difference schematics to work from.

Briefly, the first board Xerox released was the Etch 1 (which had a serial number ending in 629A). About a year later, Etch 2 was phased into production (which had a serial number ending in 644A). There were a number of minor technical differences between them; it is these items that this article addresses.

Note that with the sole exception of being able to detect double-sided 460 drives (special input line), there are NO programming differences between the two versions. All software which works on Etch 1 will work on Etch 2. However, the only item to observe is that there was a slightly different ROM release which coincided with the Etch 2 (v1.0 ROMs replaced by v2.0 ROMs). Although all jump vectors perform the same operation, there were many more added in v2.0. In addition, location of monitor variables (real-time clock, track, sector, etc.) appear elsewhere in the later release.

There are four topic areas which are different in the two etch versions: processor clock, CRT display generator, system port, and floppy controller circuitry. Each will be addressed.

820 ROMs 63 U45
64 U46

92 U92

820-I ROMs V1.5 #1 U33
2 U34
3 U35
4 U36

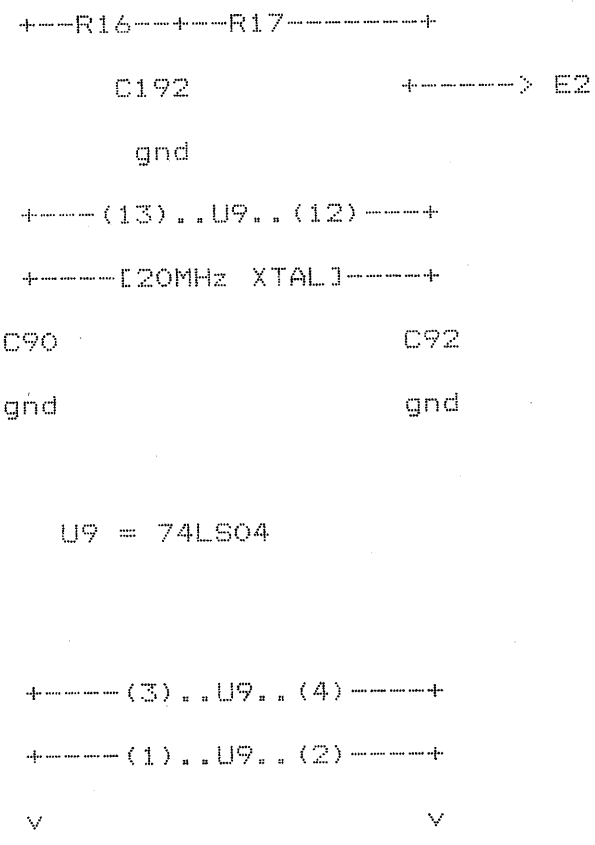
1405831408 11073

V1.02 U57
4.01 U58 537p2849

PROCESSOR CLOCK

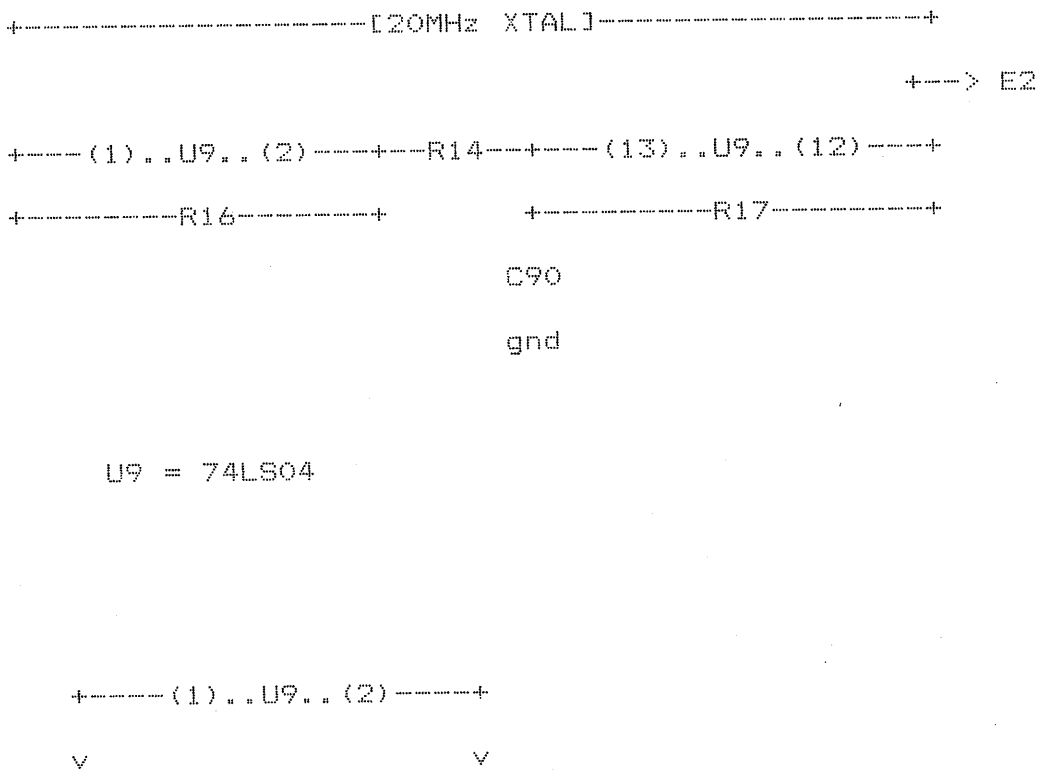
The clock and clock driver are slightly different between the two versions.

ETCH 1: R16, R17 = 1k
C90 = 47pf
U9 = 74LS04
C192 = .01uF
C92 = 100pF



U9 = 74LS04

ETCH 2: U9 = 74LS04 R14 = 100
R16, R17 = 470 C90 = 47pF
U9 = 74LS04

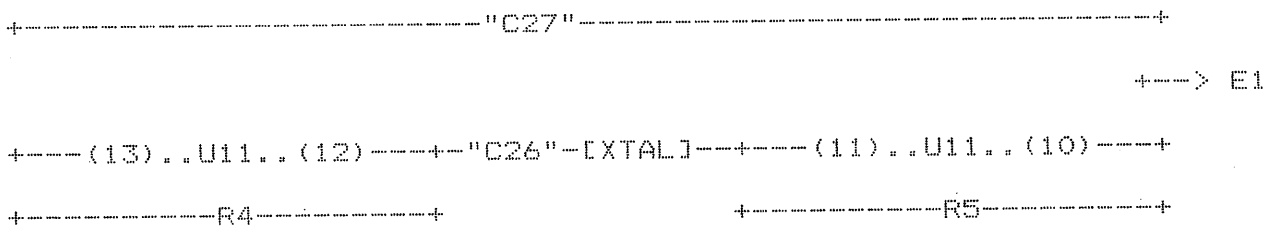


U9 = 74LS04

CRT DISPLAY GENERATION

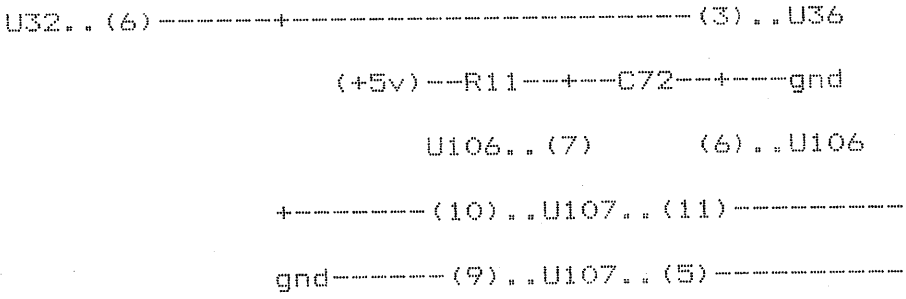
The clock is again different here. Also, the Not Vertical Sync (NVSync) is processed through a one-shot 74LS123 in Etch 1, but directly taken to the output gate (U117) in Etch 2. The earlier version used the 'LS123 to extend the NVSync signal to work with the Ball monitors which required it for clocking. Most present monitors could care less; hence, Etch 2 removed it.

ETCH 1: U11 = 74LS04 R4, R5 = 470
C26 = marked as 33pF BUT IS a jumper wire
XTAL = 10.69425MHz
C27 = marked as .01uF BUT IS 100 ohm

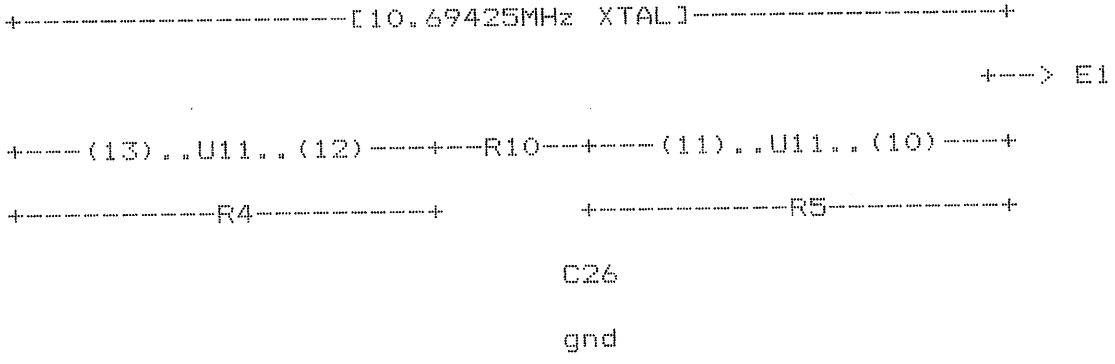


U32 = 74LS08
U36 = 74LS10
R11 = 47k
U117 = 7406

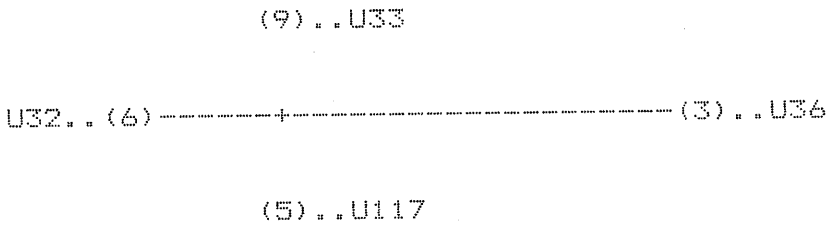
U33 = 74LS32
U106 = 74LS123
C72 = .01uF



ETCH 2: U11 = 74LS04 R4, R5 = 470
R10 = 100 C26 = 100pF



U32 = 74LS08 U33 = 74LS32
U36 = 74LS10 U117 = 7406



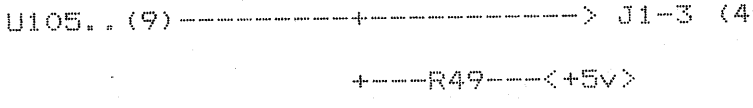
SYSTEM PORT

On Etch 1, bit 5 of the system PIO (PA5; port 1CH) was not used. Etch 2 added an input from 5.25" drives to detect double-sided disks.

ETCH 1: U105 = Z80 PIO

U105..(9)---------- n/c

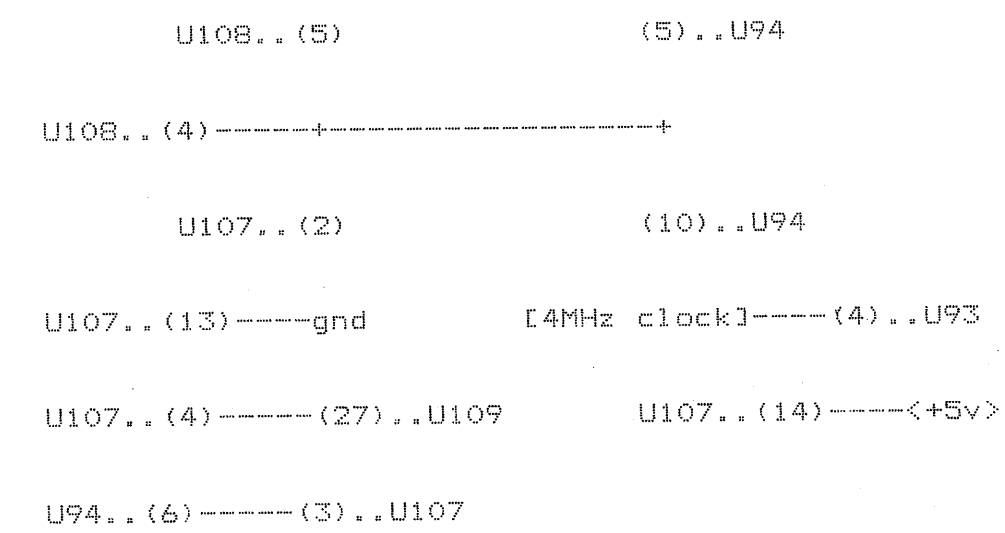
ETCH 2: U105 = Z80 PIO R49 = 10k



FLOPPY CONTROLLER

Etch 1 and 2 differed in the data seperation circuitry. Etch 2 saw the addition of a one-shot to improve clock/data seperation as well as extensive re-routing of the RAW DATA signal as part of the improved circuitry.

ETCH 1: U107 = 74LS157
U94 = 74LS08
U109 = FD1771
U108 = 74LS14
U93 = 74LS193



ETCH 2: U107 = 74LS157 U108 = 74LS14
U94 = 74LS08 U92 = 74LS193
U106 = 74LS123 C72 = 100pF
R11 = 7.5k U109 = FD1771