This is a manual transcription from the Stanford prints of 12-Jan-82. Beware of BUGS!

Phantom signals:
- R.FWE' is really Adrs.WE'
- T.ReadyReq' is really Tx.Ready
- Status.Clr' is really Adrs.OE'

P1 signals names were standardized

Bug fixes:
- Pg 2: T.AbortAck' clears Tx.Inhibit
- Pg 2: Tx.Jam feeds T.Interrupt
- Pg 5: Flush P.WriteAck', Needs new microcode

DICENTRA SCHEMATICS

~~T1 Board~~ 3meg mb ewet

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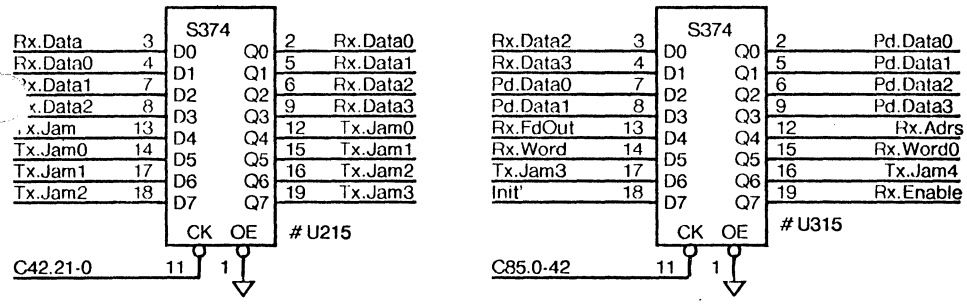
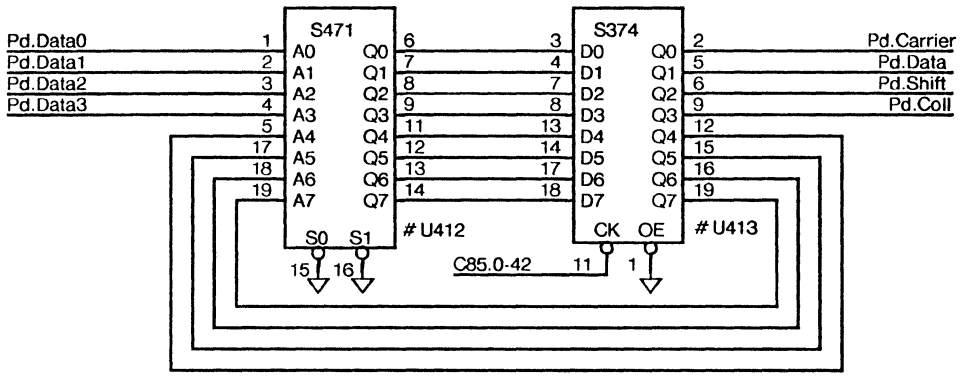
These drawings use the following [SIL] User.cm parameters:
- 0: Helvetica10
- 1: Helvetica7
- 2: Template64
- 3: Gates32
- 5: Dicentra.lb5
- 6: Dicentra.lb6
- 7: Dicentra.lb7
- 8: Dicentra.lb8
- A: Dicentra.Analyze
- Y: 712

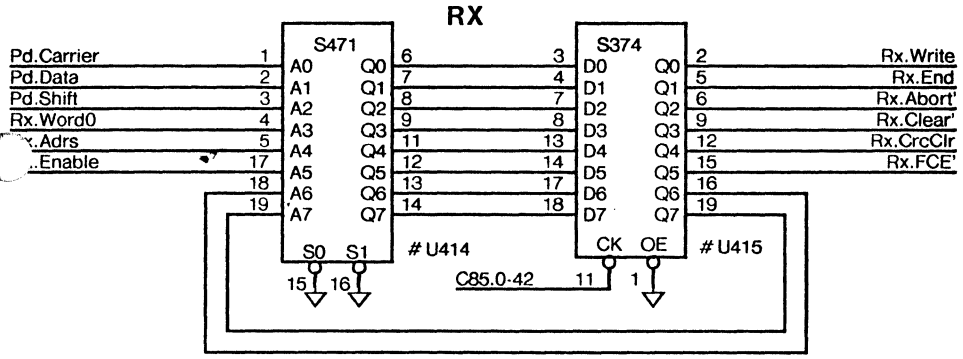
All files are kept on [Indigo]<Dicentra>

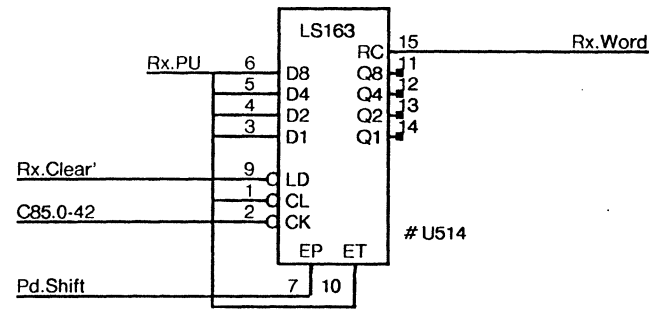


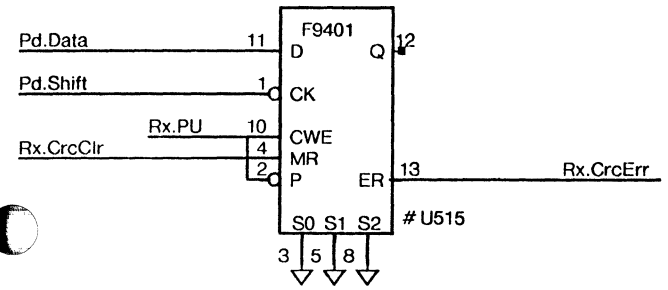
PD



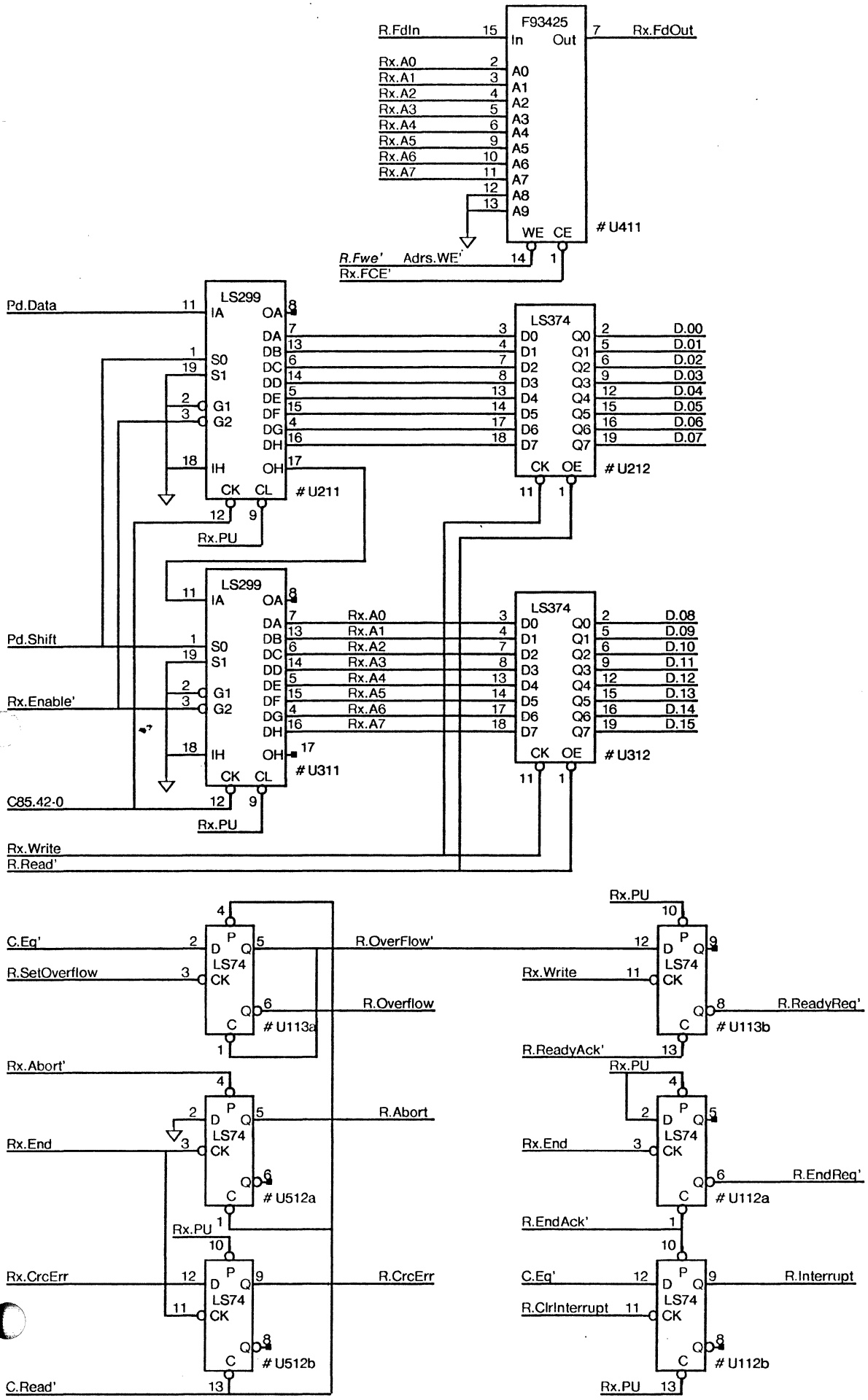
RX



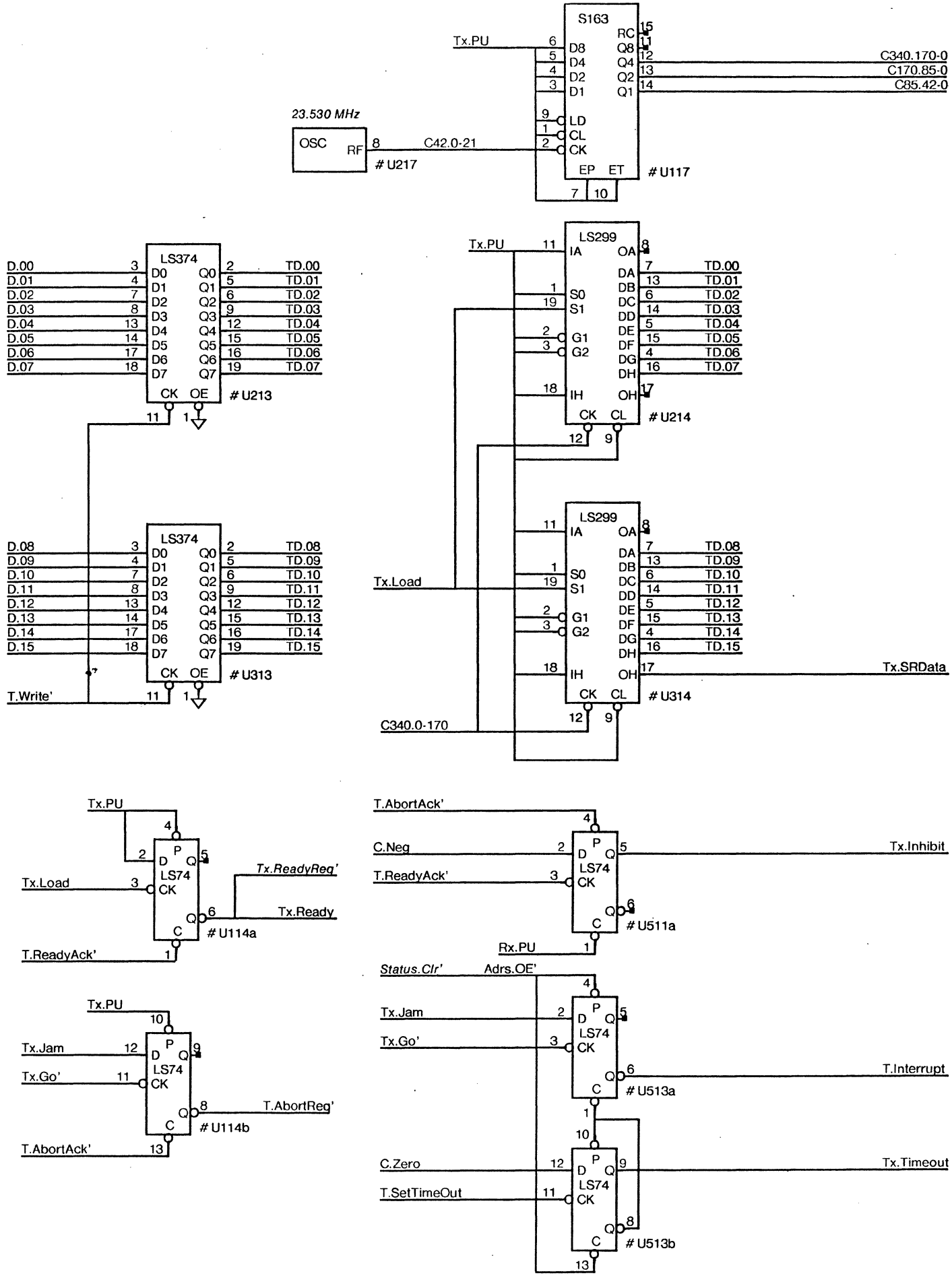




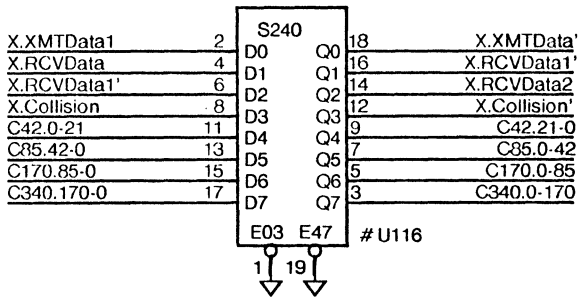
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Ethernet Interface Receiver	DT1-01.sil	Hal Murray	A	8/05/84	01

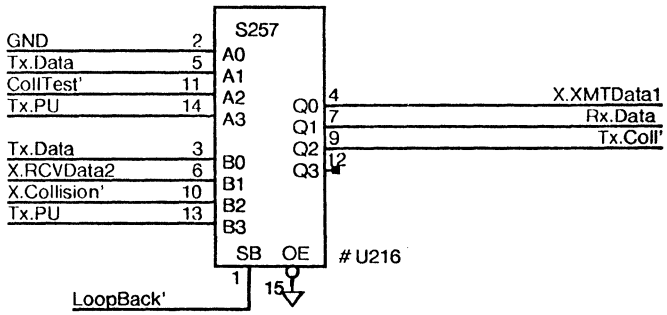


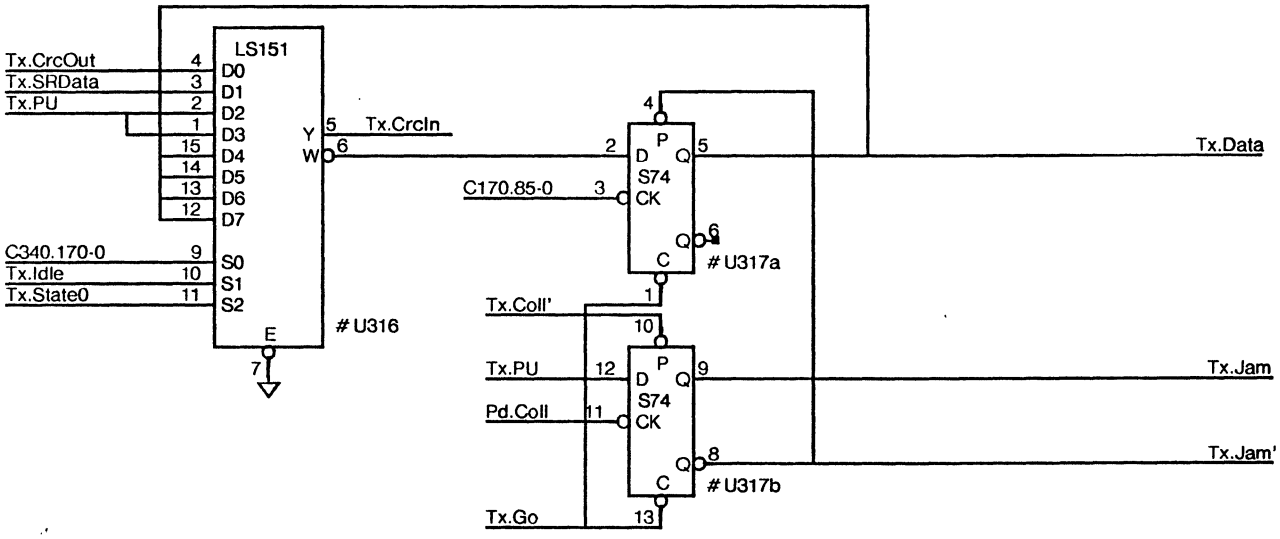
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Ethernet Interface Receiver	DT1-02.sil	Hal Murray	A	8/05/84	02

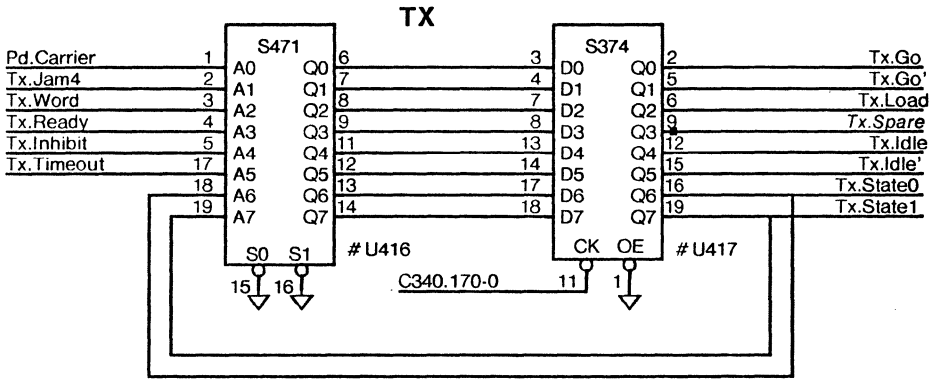


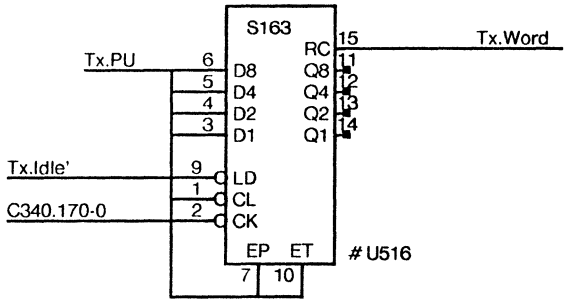
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Ethernet Interface Transmitter	DT1-03.sil	Hal Murray	A	8/05/84	03

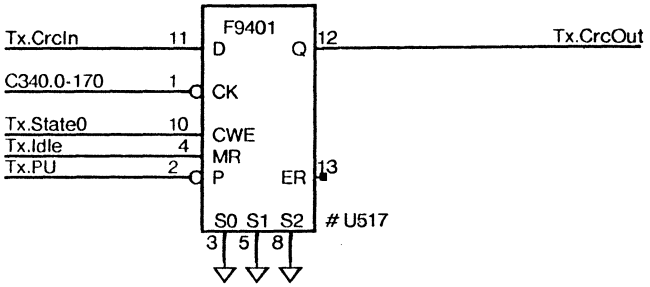




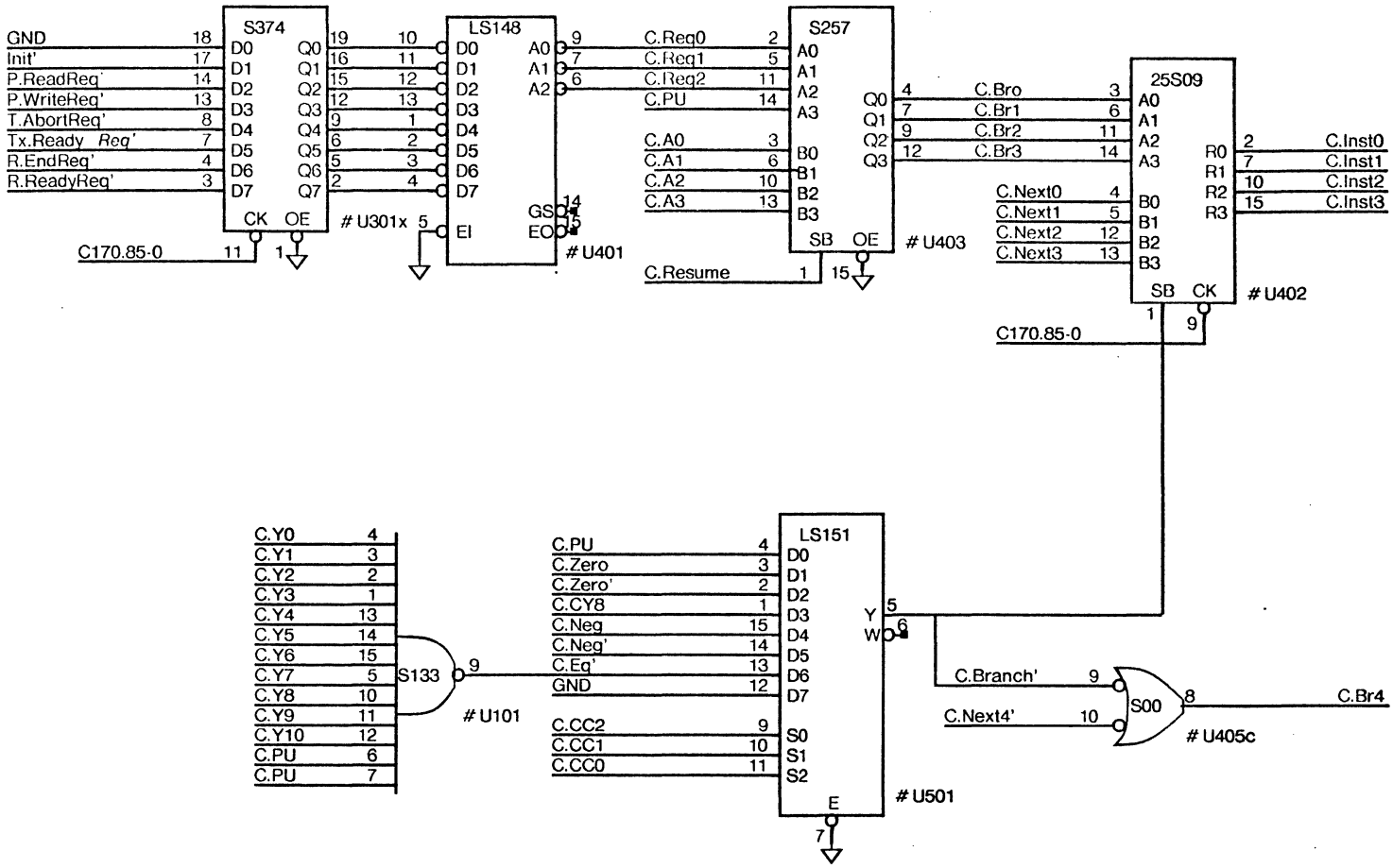




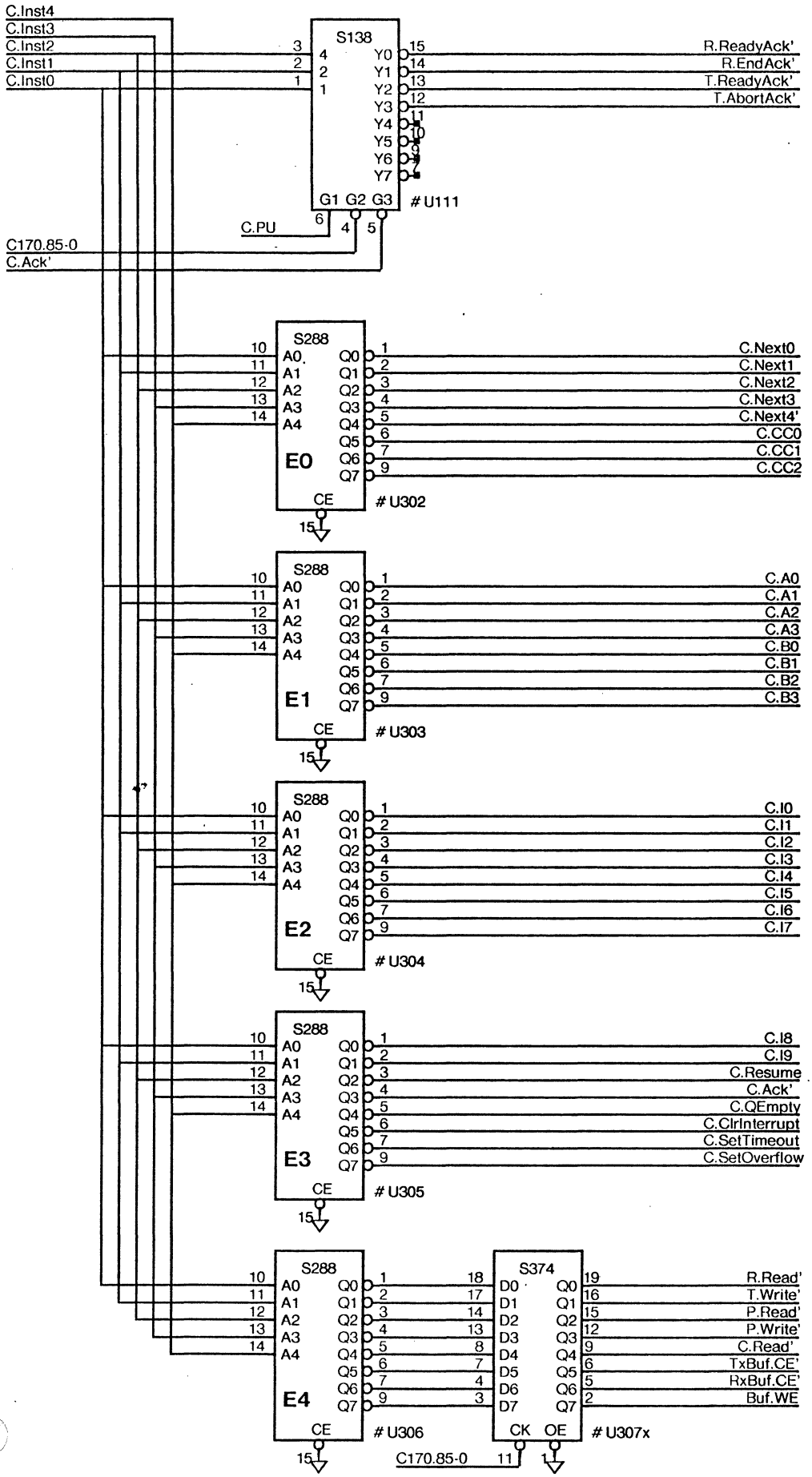




XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Ethernet Interface Transmitter	DT1-04.sil	Hal Murray	A	8/05/84	04



XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Control Store Address	DT1-05.sil	Hal Murray	A	8/05/84	05



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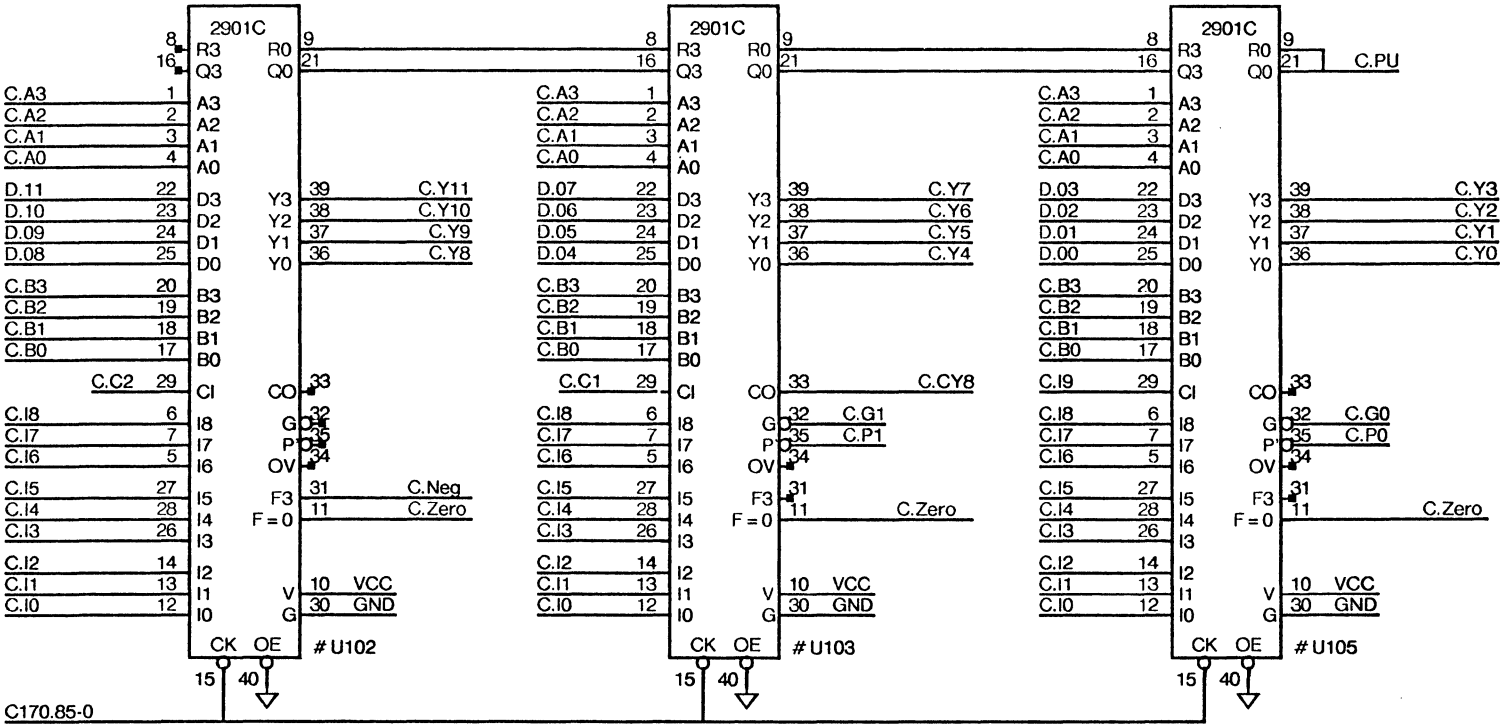
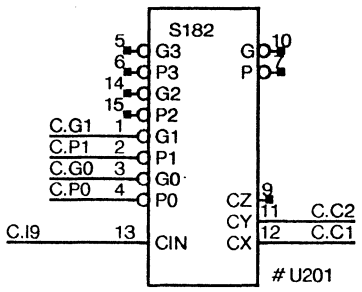
	Dicentra	Control Store	DT1-06.sil	Hal Murray	A	8/05/84	06





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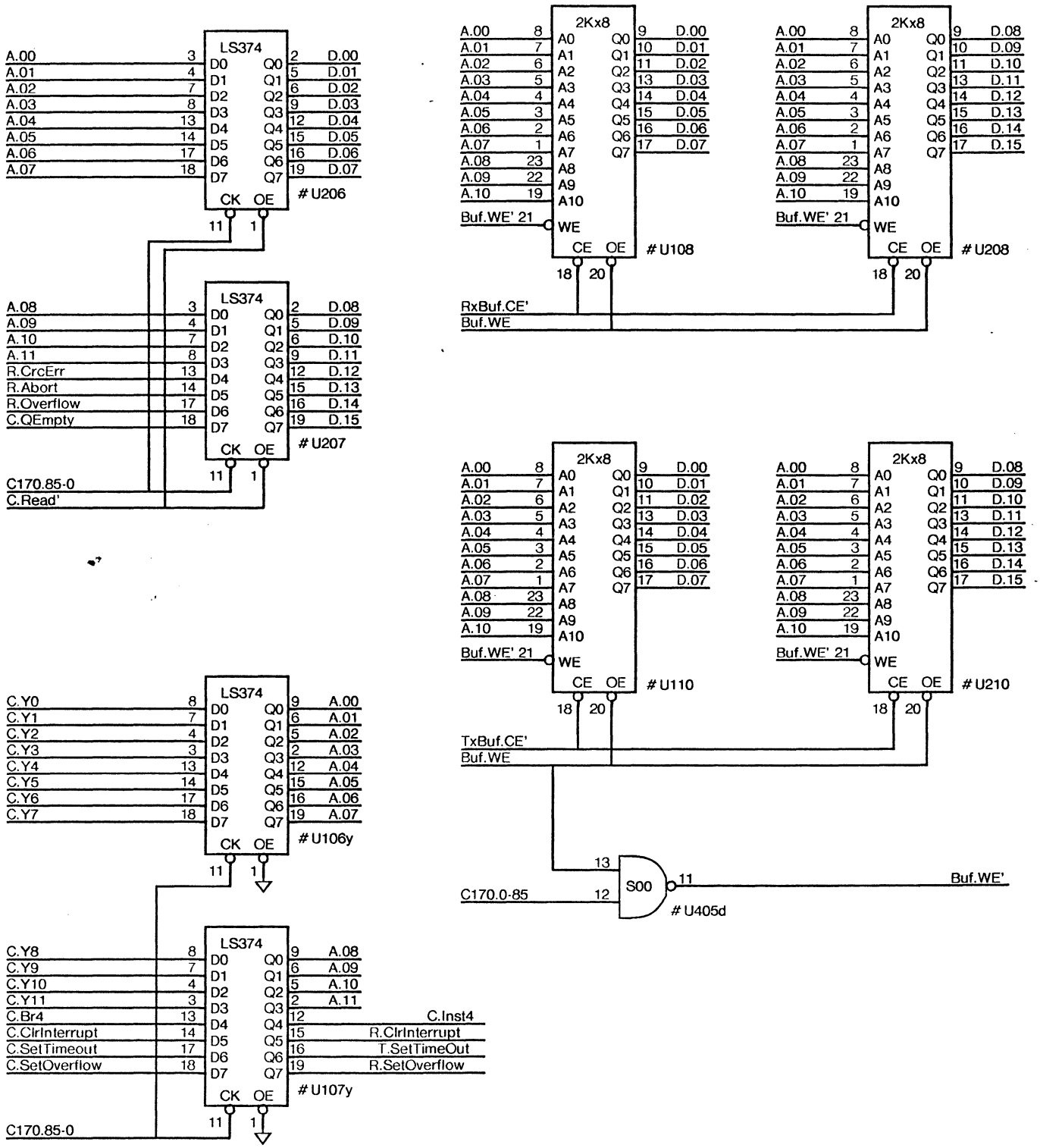
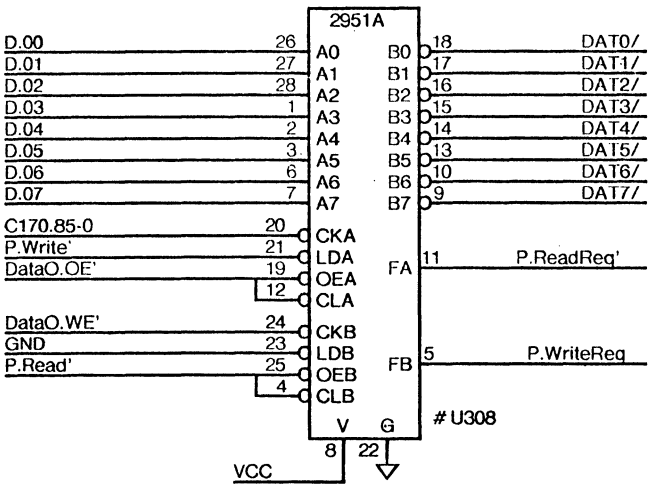
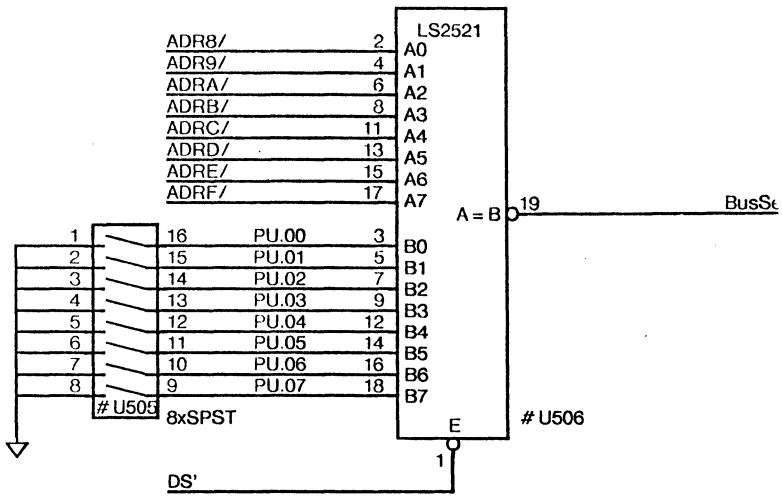
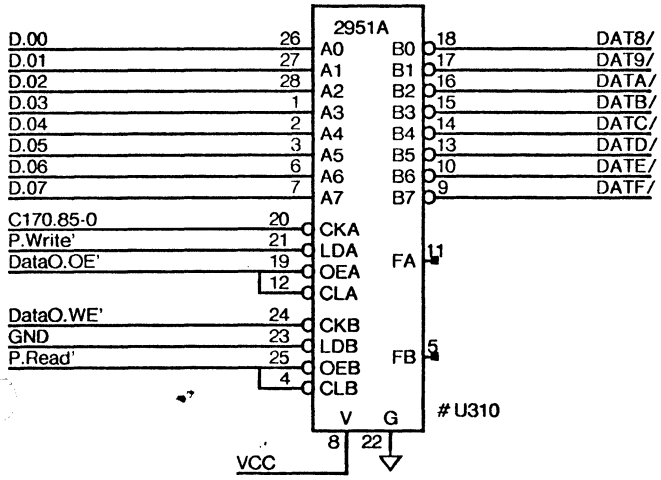
	Dicentra	2901s	DT1-07.sil	Hal Murray	A	7/24/84	07

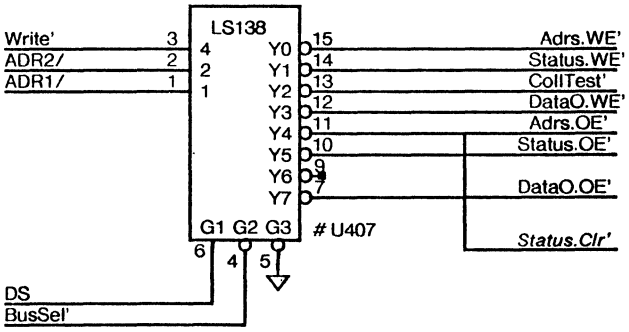


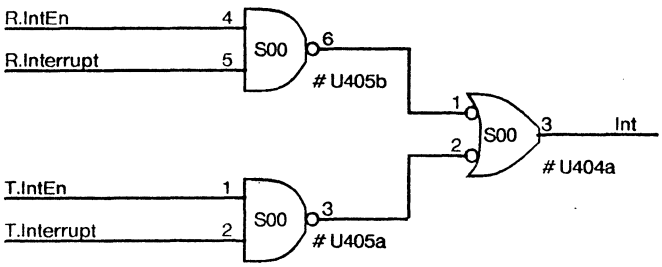
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Packet Buffers	DT1-08.sil	Hal Murray	A	8/05/84	08



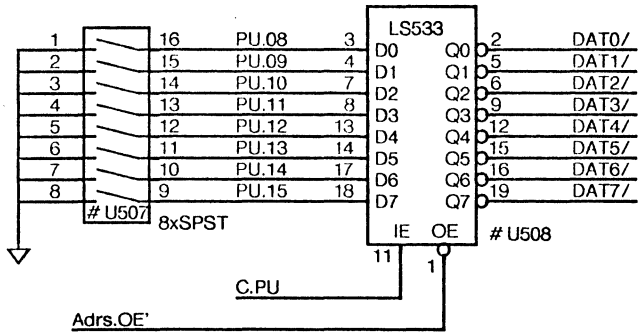


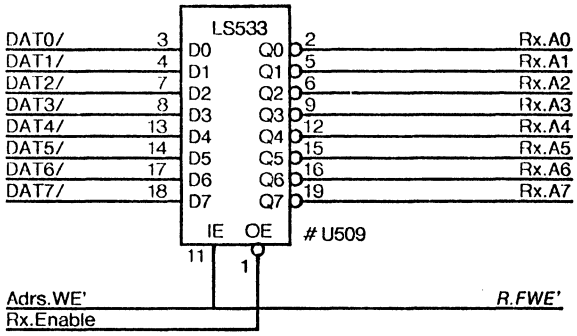


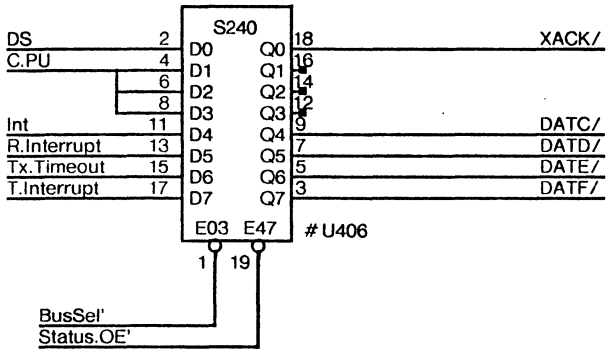


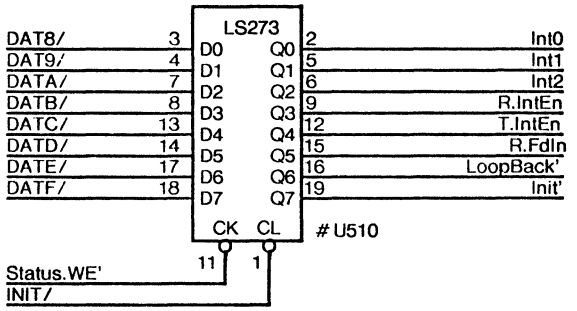


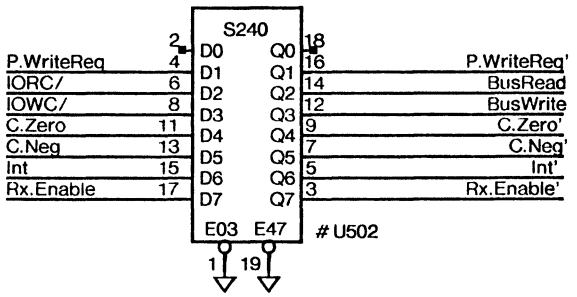
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Front Porch, Board Select	DT1-09.sil	Hal Murray	A	8/05/84	09

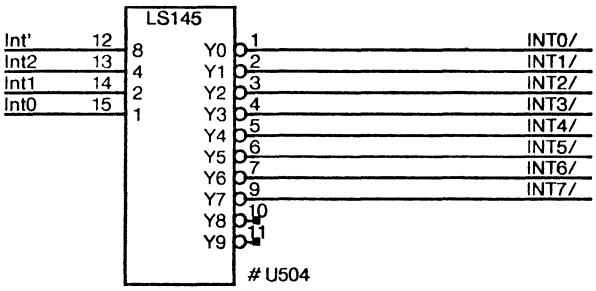


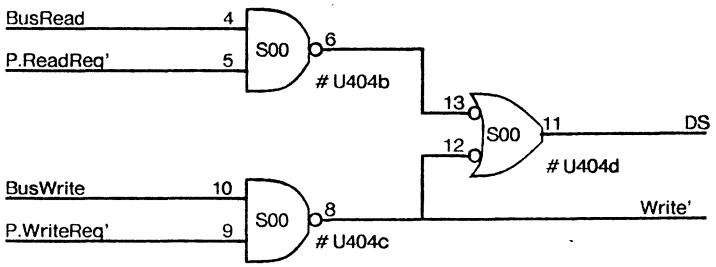


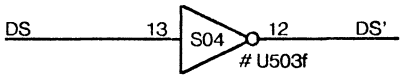




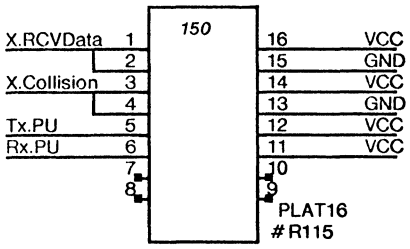


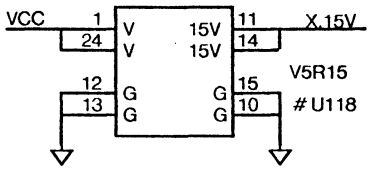


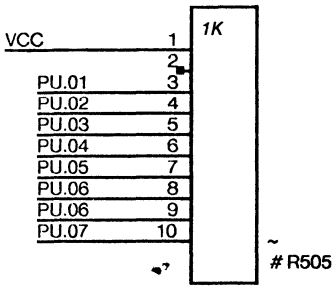


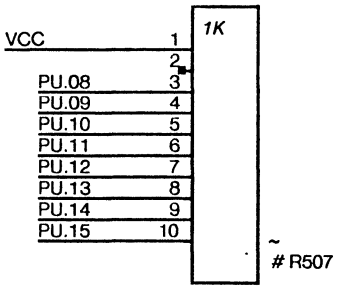


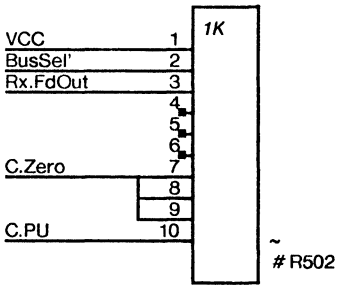
XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Multibus Interface - Control	DT1-10.sil	Hal Murray	A	8/05/84	10

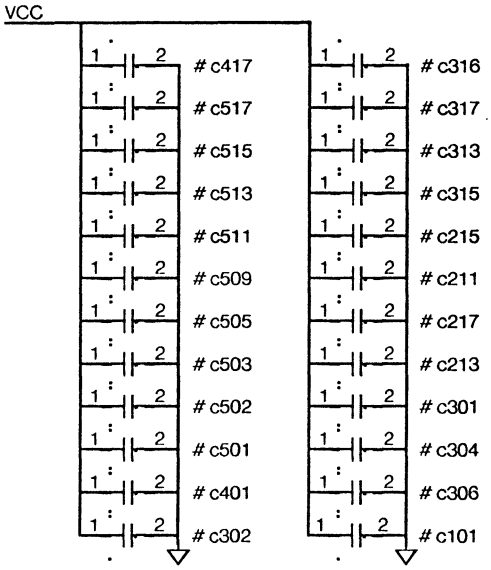




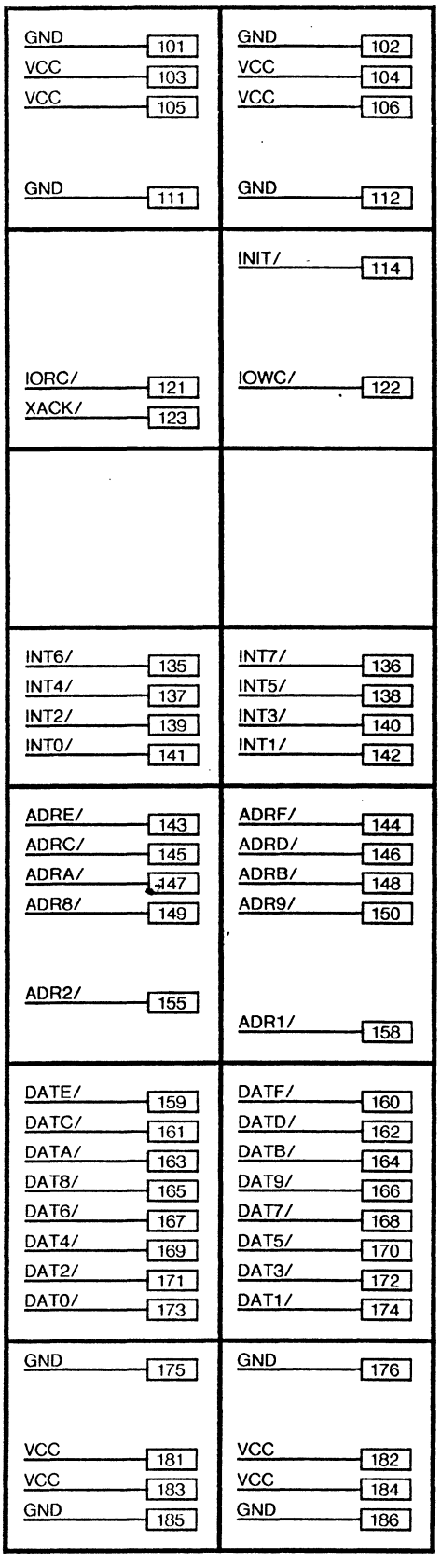


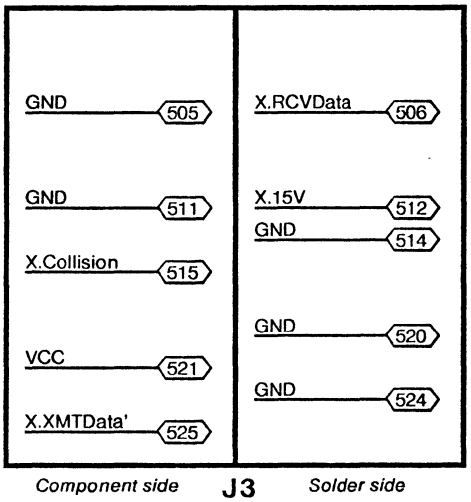






XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Dips, Sips, Caps, Power	DT1-11.sil	Hal Murray	A	8/05/84	11

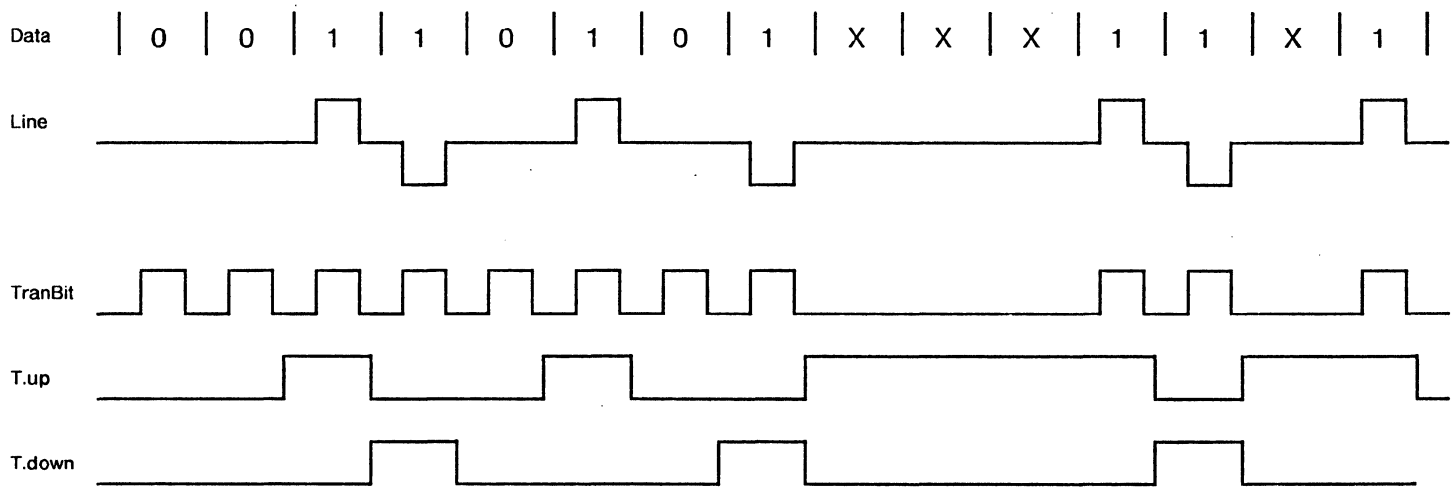




XEROX PARC	Project	Title	File	Designer	Rev	Date	Page
	Dicentra	Connectors	DT1-12.sil	Hal Murray	A	8/05/84	12

Transmitter

An extranal signal (TranBit) is used for multiplexing and speed selection.
It's frequency determines the bit rate.
It's duration determines the width of the transmitted pulses.
Provide a 50% duty cycle clock to use the whole line.
Withhold arbitrary pulses for multiplexing.



T.up and T.down are setup shortly after the falling edge of TranBit.

T1 rules:

Bit rate: 1.544 Mhz + /- 100 bits/second. (647 ns/bit)
Pulse width: 325 ns + /- 50 ns.
At least 3 pulses in any 24 bit interval.
Not more than 15 consecutive zeros.

No pulse suring a bit cell is a 0.
A pulse of either polarity is a 1.
The polarity reverses on each pulse.

Bit stuffing rules:

All 1s is no carrier.
A flag is 1, n 0s, 1.
Packets begin and end with a flag.
If the data in a packet contains more than n-1 0s, insert a 1.
n-1 0s, 0 => flag.
n-1 0s, 1 => ignore the 1.
If n is 7, there will always be at least 1 one in every byte.

Multiplexing:

2 bit streams may be multiplexed by interleaving alternate bits.
With more than 2, you might get more than 15 zeros in a row.
Many bit streams can be multiplexed a byte at a time.
SDLC uses 01111110 for a flag. (That's n = 6 with everything inverted.)

Clock accuracy:

0.005% is 77 bits/second.
At that rate, a DPPL with 10 samples per bit will be within a single sample after hundreds of bits.

Qty	Manufacturer	Part Number	Description	Location
3	AMD	2901	IC	U102, U103, U105
4	Hitachi	HM6116P-4	Ram 2Kx8	U108, U110, U208, U210
2	AMD	2951	IC	U308, U310
8	TI	74LS374	IC	U106-7, U206-7, U212-3, U312-3
7	TI	74S374	IC	U301, U307, U215, U315, U413, U415, U417
4	TI	74LS299	IC	U211, U311, U214, U314
3	TI	74S240	IC	U502, U406, U116
1	TI	74LS273	IC	U510
2	TI	74LS533	IC	U508, U509
3	TI	TBP28L22	Prom 256x8	U412, U414, U416
5	TI	TBP18S030	Prom 32x8	U302-6
1	AMD	25LS2521	IC	U506
2	TI	74LS00	IC	U404, U405
1	TI	74LS04	IC	U503
6	TI	74LS74	IC	U112-4, U511-4
1	TI	74S74	IC	U317
1	TI	74S133	IC	U101
1	TI	74LS148	IC	U401
1	TI	74S151	IC	U501
1	TI	74LS151	IC	U316
2	TI	74LS138	IC	U407, U111
2	TI	74S163	IC	U117, U514
1	TI	74LS145	IC	U504
1	TI	74LS163	IC	U516
2	TI	74S257	IC	U403, U216
1	AMD	2902	IC	U201
1	AMD	25S09	IC	U402
2	Fairchild	9401	IC	U515, U517
1	Fairchild	93425	Ram 1K	U411
1	Motorola	K1115A	Oscillator 23.53 MHz	U217
1	Bourns	4R-001-151	150 Ohm Dip	U115
3	Bourns	4310R-101-472	4.7K Sip	R502, R505, R507
2	GrayHill	76-SB08	Rocker Dip Swicth	S502, S507
1	Reliability	V5R15	Voltage Converter	U118
1	3M Scotchflex	3593-5002	Header, Right Angle	
2	Sanbe	S-203	Card Extractor & pins	
33	Emcon	501M50DP104M	Bypass Cap. .1uf	
5	EMC	10316-01-445	16 Pin Socket	U302-6
3	EMC	10320-01-445	20 Pin Socket	U412, U414, U416
1	?	?	PC Board	

Page Numbers: Yes First Page: 1
Columns: 2 Edge Margin: .8" Between Columns: .0"
Heading:
DT1--Rev-A.ps
COMPONENTS:

-:	11			
25S09:	5			
2901C:	7			
2951A:	9			
2Kx8:	8			
8xSPST:	9	10		
C:	2	3	4	
F93425:	2			
F9401:	1	4		
LS138:	9			
LS145:	10			
LS148:	5			
LS151:	4	5		
LS163:	1			
LS2521:	9			
LS273:	10			
LS299:	2	3		
LS374:	2	3	8	
LS533:	10			
LS74:	2	3		
OSC:	3			
PLAT16:	11			
S00:	6	8	9	10
S04:	10			
S133:	5			
S138:	6			
S163:	3	4		
S182:	7			
S240:	4	10		
S257:	4	5		
S288:	6			
S374:	1	4	5	6
S471:	1	4		
S74:	4			
V6R15:	11			
~:	11			

SIGNAL NAMES:

+:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
A.00:	8(6)					
A.01:	8(6)					
A.02:	8(6)					
A.03:	8(6)					
A.04:	8(6)					
A.05:	8(6)					
A.06:	8(6)					
A.07:	8(6)					
A.08:	8(6)					
A.09:	8(6)					
A.10:	8(6)					
A.11:	8(2)					
ADR1/:	9(1)	12(1)				
ADR2/:	9(1)	12(1)				
ADR8/:	9(1)	12(1)				
ADR9/:	9(1)	12(1)				
ADRA/:	9(1)	12(1)				
ADRB/:	9(1)	12(1)				
ADRC/:	9(1)	12(1)				
ADRD/:	9(1)	12(1)				
ADRE/:	9(1)	12(1)				
ADRF/:	9(1)	12(1)				
Adrs.OE':	3(1)	9(1)	10(1)			
Adrs.WE':	2(1)	9(1)	10(1)			
Buf.WE:	6(1)	8(2)				
Buf.WE':	8(5)					
BusRead:	10(2)					
BusSel':	9(2)	10(1)	11(1)			
BusWrite:	10(2)					
C.A0:	5(1)	6(1)	7(3)			
C.A1:	5(1)	6(1)	7(3)			
C.A2:	5(1)	6(1)	7(3)			
C.A3:	5(1)	6(1)	7(3)			
C.Ack':	6(2)					
C.B0:	6(1)	7(3)				
C.B1:	6(1)	7(3)				
C.B2:	6(1)	7(3)				
C.B3:	6(1)	7(3)				
C.Br1:	5(1)					
C.Br2:	5(1)					
C.Br3:	5(1)					
C.Br4:	5(1)	8(1)				
C.Branch':	5(1)					
C.Bro:	5(1)					
C.C1:	7(2)					
C.C2:	7(2)					
C.CC0:	5(1)	6(1)				
C.CC1:	5(1)	6(1)				
C.CC2:	5(1)	6(1)				
C.ClrInterrupt:	6(1)	8(1)				
C.CY8:	5(1)	7(1)				
C.Eq':	2(2)	5(1)				
C.G0:	7(2)					

```
C.G1:            7(2)
C.I0:            6(1)   7(3)
C.I1:            6(1)   7(3)
C.I2:            6(1)   7(3)
C.I3:            6(1)   7(3)
C.I4:            6(1)   7(3)
C.I5:            6(1)   7(3)
C.I6:            6(1)   7(3)
C.I7:            6(1)   7(3)
C.I8:            6(1)   7(3)
C.I9:            6(1)   7(2)
C.Inst0:         5(1)   6(1)
C.Inst1:         5(1)   6(1)
C.Inst2:         5(1)   6(1)
C.Inst3:         5(1)   6(1)
C.Inst4:         6(1)   8(1)
C.Neg:           3(1)   5(1)   7(1)   10(1)
C.Neg':          5(1)   10(1)
C.Next0:         5(1)   6(1)
C.Next1:         5(1)   6(1)
C.Next2:         5(1)   6(1)
C.Next3:         5(1)   6(1)
C.Next4':        5(1)   6(1)
C.P0:            7(2)
C.P1:            7(2)
C.PU:            5(4)   6(1)   7(1)   10(2)   11(1)
C.QEmpty:        6(1)   8(1)
C.Read':         2(1)   6(1)   8(1)
C.Req0:          5(1)
C.Req1:          5(1)
C.Req2:          5(1)
C.Resume:        5(1)   6(1)
C.SetOverflow:   6(1)   8(1)
C.SetTimeout:    6(1)   8(1)
C.Y0:            5(1)   7(1)   8(1)
C.Y1:            5(1)   7(1)   8(1)
C.Y10:           5(1)   7(1)   8(1)
C.Y11:           7(1)   8(1)
C.Y2:            5(1)   7(1)   8(1)
C.Y3:            5(1)   7(1)   8(1)
C.Y4:            5(1)   7(1)   8(1)
C.Y5:            5(1)   7(1)   8(1)
C.Y6:            5(1)   7(1)   8(1)
C.Y7:            5(1)   7(1)   8(1)
C.Y8:            5(1)   7(1)   8(1)
C.Y9:            5(1)   7(1)   8(1)
C.Zero:          3(1)   5(1)   7(3)   10(1)   11(1)
C.Zero':         5(1)   10(1)
C170.0-85:       4(1)   8(1)
C170.85-0:       3(1)   4(2)   5(2)   6(2)   7(1)   8(2)
                 9(2)
C340.0-170:      3(1)   4(2)
C340.170-0:      3(1)   4(4)
C42.0-21:        3(1)   4(1)
C42.21-0:        1(1)   4(1)
C85.0-42:        1(4)   4(1)
C85.42-0:        2(1)   3(1)   4(1)
CollTest':       4(1)   9(1)
D.00:            2(1)   3(1)   7(1)   8(3)   9(2)
D.01:            2(1)   3(1)   7(1)   8(3)   9(2)
D.02:            2(1)   3(1)   7(1)   8(3)   9(2)
D.03:            2(1)   3(1)   7(1)   8(3)   9(2)
D.04:            2(1)   3(1)   7(1)   8(3)   9(2)
D.05:            2(1)   3(1)   7(1)   8(3)   9(2)
D.06:            2(1)   3(1)   7(1)   8(3)   9(2)
D.07:            2(1)   3(1)   7(1)   8(3)   9(2)
D.08:            2(1)   3(1)   7(1)   8(3)
D.09:            2(1)   3(1)   7(1)   8(3)
D.10:            2(1)   3(1)   7(1)   8(3)
D.11:            2(1)   3(1)   7(1)   8(3)
D.12:            2(1)   3(1)   8(3)
D.13:            2(1)   3(1)   8(3)
D.14:            2(1)   3(1)   8(3)
D.15:            2(1)   3(1)   8(3)
DAT0/:           9(1)   10(2)  12(1)
DAT1/:           9(1)   10(2)  12(1)
DAT2/:           9(1)   10(2)  12(1)
DAT3/:           9(1)   10(2)  12(1)
DAT4/:           9(1)   10(2)  12(1)
DAT5/:           9(1)   10(2)  12(1)
DAT6/:           9(1)   10(2)  12(1)
DAT7/:           9(1)   10(2)  12(1)
DAT8/:           9(1)   10(1)  12(1)
DAT9/:           9(1)   10(1)  12(1)
DATA/:           9(1)   10(1)  12(1)
DataO.OE':       9(3)
DataO.WE':       9(3)
DATB/:           9(1)   10(1)  12(1)
DATC/:           9(1)   10(2)  12(1)
DATD/:           9(1)   10(2)  12(1)
DATE/:           9(1)   10(2)  12(1)
DATF/:           9(1)   10(2)  12(1)
DS:              9(1)   10(3)
DS':             9(1)   10(1)
Gnd:             1(1)   2(1)   3(1)   4(1)   5(1)   6(1)
                 7(1)   8(1)   9(1)   10(1)  11(1)  12(1)
GND:             4(1)   5(2)   7(3)   9(2)   11(2)  12(13)
Init':           1(1)   5(1)   10(1)
INIT/:           10(1)  12(1)
Int:             9(1)   10(2)
Int':            10(2)
```

```
Int0:           10(2)
INT0/:          10(1)   12(1)
Int1:           10(2)
INT1/:          10(1)   12(1)
Int2:           10(2)
INT2/:          10(1)   12(1)
INT3/:          10(1)   12(1)
INT4/:          10(1)   12(1)
INT5/:          10(1)   12(1)
INT6/:          10(1)   12(1)
INT7/:          10(1)   12(1)
IORC/:          10(1)   12(1)
IOWC/:          10(1)   12(1)
LoopBack':       4(1)   10(1)
P.Read':         6(1)    9(2)
P.ReadReq':      5(1)    9(1)   10(1)
P.Write':        6(1)    9(2)
P.WriteReq:      9(1)   10(1)
P.WriteReq':     5(1)   10(2)
Pd.Carrier:      1(2)    4(1)
Pd.Coll:         1(1)    4(1)
Pd.Data:         1(3)    2(1)
Pd.Data0:        1(3)
Pd.Data1:        1(3)
Pd.Data2:        1(2)
Pd.Data3:        1(2)
Pd.Shift:        1(4)    2(1)
PU.00:           9(1)
PU.01:           9(1)   11(1)
PU.02:           9(1)   11(1)
PU.03:           9(1)   11(1)
PU.04:           9(1)   11(1)
PU.05:           9(1)   11(1)
PU.06:           9(1)   11(2)
PU.07:           9(1)   11(1)
PU.08:          10(1)   11(1)
PU.09:          10(1)   11(1)
PU.10:          10(1)   11(1)
PU.11:          10(1)   11(1)
PU.12:          10(1)   11(1)
PU.13:          10(1)   11(1)
PU.14:          10(1)   11(1)
PU.15:          10(1)   11(1)
R.Abort:         2(1)    8(1)
R.ClrInterrupt:  2(1)    8(1)
R.CrcErr:        2(1)    8(1)
R.EndAck':       2(1)    6(1)
R.EndReq':       2(1)    5(1)
R.FdIn:          2(1)   10(1)
R.IntEn:         9(1)   10(1)
R.Interrupt:     2(1)    9(1)   10(1)
R.Overflow:      2(1)    8(1)
R.OverFlow':     2(1)
R.Read':         2(1)    6(1)
R.ReadyAck':     2(1)    6(1)
R.ReadyReq':     2(1)    5(1)
R.SetOverflow:   2(1)    8(1)
Rx.A0:           2(2)   10(1)
Rx.A1:           2(2)   10(1)
Rx.A2:           2(2)   10(1)
Rx.A3:           2(2)   10(1)
Rx.A4:           2(2)   10(1)
Rx.A5:           2(2)   10(1)
Rx.A6:           2(2)   10(1)
Rx.A7:           2(2)   10(1)
Rx.Abort':       1(1)    2(1)
Rx.Adrs:         1(2)
Rx.Clear':       1(2)
Rx.CrcClr:       1(2)
Rx.CrcErr:       1(1)    2(1)
Rx.Data:         1(1)    4(1)
Rx.Data0:        1(2)
Rx.Data1:        1(2)
Rx.Data2:        1(3)
Rx.Data3:        1(2)
Rx.Enable:       1(2)   10(2)
Rx.Enable':      2(1)   10(1)
Rx.End:          1(1)    2(2)
Rx.FCE':         1(1)    2(1)
Rx.FdOut:        1(1)    2(1)   11(1)
Rx.PU:           1(2)    2(6)    3(1)   11(1)
Rx.Word:         1(2)
Rx.Word0:        1(2)
Rx.Write:        1(1)    2(2)
RxBuf.CE':       6(1)    8(1)
Status.OE':      9(1)   10(1)
Status.WE':      9(1)   10(1)
T.AbortAck':     3(2)    6(1)
T.AbortReq':     3(1)    5(1)
T.IntEn:         9(1)   10(1)
T.Interrupt:     3(1)    9(1)   10(1)
T.ReadyAck':     3(2)    6(1)
T.SetTimeOut:    3(1)    8(1)
T.Write':        3(1)    6(1)
TD.00:           3(2)
TD.01:           3(2)
TD.02:           3(2)
TD.03:           3(2)
TD.04:           3(2)
TD.05:           3(2)
TD.06:           3(2)
```

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TD.07:          3(2)
TD.08:          3(2)
TD.09:          3(2)
TD.10:          3(2)
TD.11:          3(2)
TD.12:          3(2)
TD.13:          3(2)
TD.14:          3(2)
TD.15:          3(2)
Tx.Coll':       4(2)
Tx.CrcIn:       4(2)
Tx.CrcOut:      4(2)
Tx.Data:        4(3)
Tx.Go:          4(2)
Tx.Go':         3(2)    4(1)
Tx.Idle:        4(3)
Tx.Idle':       4(2)
Tx.Inhibit:     3(1)    4(1)
Tx.Jam:         1(1)    3(2)    4(1)
Tx.Jam':        4(1)
Tx.Jam0:        1(2)
Tx.Jam1:        1(2)
Tx.Jam2:        1(2)
Tx.Jam3:        1(2)
Tx.Jam4:        1(1)    4(1)
Tx.Load:        3(2)    4(1)
Tx.PU:          3(4)    4(6)   11(1)
Tx.Ready:       3(1)    4(1)    5(1)
Tx.SRData:      3(1)    4(1)
Tx.State0:      4(3)
Tx.State1:      4(1)
Tx.Timeout:     3(1)    4(1)   10(1)
Tx.Word:        4(2)
TxBuf.CE':      6(1)    8(1)
VCC:            7(3)    9(2)   11(9)   12(9)
Write':         9(1)   10(1)
X.15V:         11(1)   12(1)
X.Collision:    4(1)   11(1)   12(1)
X.Collision':   4(2)
X.RCVData:      4(1)   11(1)   12(1)
X.RCVData1':    4(2)
X.RCVData2:     4(2)
X.XMTData':     4(1)   12(1)
X.XMTData1:     4(2)
XACK/:         10(1)   12(1)
```

```
Universal
;File=DT1--Rev-A.sil Rev=A Date=8/05/84 Page=00 Reference  -MARKED BUILT-
;File=DT1-01.sil Rev=A Date=8/05/84 Page=01  -MARKED BUILT-
;File=DT1-02.sil Rev=A Date=8/05/84 Page=02  -MARKED BUILT-
;File=DT1-03.sil Rev=A Date=8/05/84 Page=03  -MARKED BUILT-
;File=DT1-04.sil Rev=A Date=8/05/84 Page=04  -MARKED BUILT-
;File=DT1-05.sil Rev=A Date=8/05/84 Page=05  -MARKED BUILT-
;File=DT1-06.sil Rev=A Date=8/05/84 Page=06  -MARKED BUILT-
;File=DT1-07.sil Rev=A Date=7/24/84 Page=07  -MARKED BUILT-
;File=DT1-08.sil Rev=A Date=8/05/84 Page=08  -MARKED BUILT-
;File=DT1-09.sil Rev=A Date=8/05/84 Page=09  -MARKED BUILT-
;File=DT1-10.sil Rev=A Date=8/05/84 Page=10  -MARKED BUILT-
;File=DT1-11.sil Rev=A Date=8/05/84 Page=11  MARKED BUILT
;File=DT1-12.sil Rev=A Date=8/05/84 Page=12  -MARKED BUILT-
;File=DT1-pict.sil Rev=A Date=8/05/84 Page=13 Reference  -MARKED BUILT-
;File=DT1-parts.sil Rev=A Date=8/05/84 Page=14 Reference  -MARKED BUILT-
; Implicitly generated wiring ...

#c101: (-/2/J) ;
#c211: (-/2/J) ;
#c213: (-/2/J) ;
#c215: (-/2/J) ;
#c217: (-/2/J) ;
#c301: (-/2/J) ;
#c302: (-/2/J) ;
#c304: (-/2/J) ;
#c306: (-/2/J) ;
#c313: (-/2/J) ;
#c315: (-/2/J) ;
#c316: (-/2/J) ;
#c317: (-/2/J) ;
#c401: (-/2/J) ;
#c417: (-/2/J) ;
#c501: (-/2/J) ;
#c502: (-/2/J) ;
#c503: (-/2/J) ;
#c505: (-/2/J) ;
#c509: (-/2/J) ;
#c511: (-/2/J) ;
#c513: (-/2/J) ;
#c515: (-/2/J) ;
#c517: (-/2/J) ;
#R115: (PLAT16/16/J) ; 7,8,9,10
#R502: (10SIP/10/J1W) ; 4,5,6
#R505: (10SIP/10/J1W) ; 2
#R507: (10SIP/10/J1W) ; 2
#U101: (74S133/16/N) ;
#U102: (AMD2901C/40/J6W) ; 8,16,32,33,34,35
#U103: (AMD2901C/40/J6W) ; 31,34
#U105: (AMD2901C/40/J6W) ; 31,33,34
#U106: (74LS374/20/N) ;
#U107: (74LS374/20/N) ;
#U108: (2Kx8/24/N6W) ;
#U110: (2Kx8/24/N6W) ;
#U111: (74S138/16/N) ; 7,9,10,11
#U112: (74LS74/14/N) ; 5,8
#U113: (74LS74/14/N) ; 9
#U114: (74LS74/14/N) ; 6,9
#U116: (74S240/20/N) ;
#U117: (74S163/16/N) ; 11,15
#U118: (V5R15/24/J6W) ; 2,3,4,5,6,7,8,9,16,17,18,19,20,21,22,23
#U201: (74S182/16/N) ; 5,6,7,9,10,14,15
#U206: (74LS374/20/N) ;
#U207: (74LS374/20/N) ;
#U208: (2Kx8/24/N6W) ;
#U210: (2Kx8/24/N6W) ;
#U211: (74LS299/20/N) ; 8
#U212: (74LS374/20/N) ;
#U213: (74LS374/20/N) ;
#U214: (74LS299/20/N) ; 8,17
#U215: (74S374/20/N) ;
#U216: (74S257/16/N) ; 12
#U217: (OSCILLATOR/14/N) ; 1,2,3,4,5,6,9,10,11,12,13
#U301: (74S374/20/N) ;
#U302: (74S288/16/N) ;
#U303: (74S288/16/N) ;
#U304: (74S288/16/N) ;
#U305: (74S288/16/N) ;
#U306: (74S288/16/N) ;
#U307: (74S374/20/N) ;
#U308: (AMD2951/28/J6W) ;
#U310: (AMD2951/28/J6W) ; 5,11
#U311: (74LS299/20/N) ; 8,17
#U312: (74LS374/20/N) ;
#U313: (74LS374/20/N) ;
#U314: (74LS299/20/N) ; 8
#U315: (74S374/20/N) ;
#U316: (74LS151/16/N) ;
#U317: (74S74/14/N) ; 6
#U401: (74LS148/16/N) ; 14,15
#U402: (AMD25S09/16/N) ;
#U403: (74S257/16/N) ;
#U404: (74S00/14/N) ;
#U405: (74S00/14/N) ;
#U406: (74S240/20/N) ; 12,14,16
#U407: (74LS138/16/N) ; 9
#U411: (93425A/22/F4W) ; 16,17,18,19,20,21
#U412: (74S471/20/N) ;
#U413: (74S374/20/N) ;
#U414: (74S471/20/N) ;
#U415: (74S374/20/N) ;
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#U416: (74S471/20/N) ;
#U417: (74S374/20/N) ; 9
#U501: (74LS151/16/N) ; 6
#U502: (74S240/20/N) ; 2,18
#U503: (74S04/14/N) ; 1,2,3,4,5,6,8,9,10,11
#U504: (74LS145/16/N) ; 10,11
#U505: (8xSPST/16/J) ;
#U506: (74LS2521/20/N) ;
#U507: (8xSPST/16/J) ;
#U508: (74LS533/20/N) ;
#U509: (74LS533/20/N) ;
#U510: (74LS273/20/N) ;
#U511: (74LS74/14/N) ; 6,8,9,10,11,12,13
#U512: (74LS74/14/N) ; 6,8
#U513: (74LS74/14/N) ; 5
#U514: (74LS163/16/N) ; 11,12,13,14
#U515: (F9401/14/N) ; 6,9,12
#U516: (74S163/16/N) ; 11,12,13,14
#U517: (F9401/14/N) ; 6,9,13
@

CALIBRATE: <1>   ; INSTALL welder nose, board wiring side up ...
    #TopRight {0,0}       #TopLeft {0,0}        #? {0,0}              #? {0,0}

A.00: <76> (992)
    #U206.3i {0,152}      #U106.9o {48,176}     #U210.8i {64,172}     #U110.8i {92,172}
    #U108.8i {856,92}     #U208.8i {884,92}

A.01: <74> (976)
    #U206.4i {0,156}      #U106.6o {48,164}     #U210.7i {64,168}     #U110.7i {92,168}
    #U108.7i {856,88}     #U208.7i {884,88}

A.02: <75> (976)
    #U206.7i {0,168}      #U106.5o {48,160}     #U210.6i {64,164}     #U110.6i {92,164}
    #U108.6i {856,84}     #U208.6i {884,84}

A.03: <134> (1000)
    #U206.8i {0,172}      #U106.2o {48,148}     #U210.5i {64,160}     #U110.5i {92,160}
    #U108.5i {856,80}     #U208.5i {884,80}

A.04: <90> (976)
    #U206.13i {12,172}    #U106.12o {60,176}    #U210.4i {64,156}     #U110.4i {92,156}
    #U108.4i {856,76}     #U208.4i {884,76}

A.05: <56> (968)
    #U206.14i {12,168}    #U106.15o {60,164}    #U210.3i {64,152}     #U110.3i {92,152}
    #U108.3i {856,72}     #U208.3i {884,72}

A.06: <57> (968)
    #U206.17i {12,156}    #U106.16o {60,160}    #U210.2i {64,148}     #U110.2i {92,148}
    #U108.2i {856,68}     #U208.2i {884,68}

A.07: <25> (960)
    #U206.18i {12,152}    #U106.19o {60,148}    #U210.1i {64,144}     #U110.1i {92,144}
    #U108.1i {856,64}     #U208.1i {884,64}

A.08: <135> (1016)
    #U107.9o {32,176}     #U207.3i {16,152}     #U210.23i {88,148}    #U110.23i {116,148}
    #U108.23i {880,68}    #U208.23i {908,68}

A.09: <92> (992)
    #U208.22i {908,72}    #U108.22i {880,72}    #U110.22i {116,152}   #U210.22i {88,152}
    #U107.6o {32,164}     #U207.4i {16,156}

A.10: <91> (984)
    #U207.7i {16,168}     #U107.5o {32,160}     #U210.19i {88,164}    #U110.19i {116,164}
    #U108.19i {880,84}    #U208.19i {908,84}

A.11: <183> (40)
    #U107.2o {32,148}     #U207.8i {16,172}

ADR1/: <308> (244)
    E158 {120,4}          #U407.1i {224,144}

ADR2/: <316> (260)
    E155 {108,4}          #U407.2i {224,148}

ADR8/: <313> (252)
    E149 {84,4}           #U506.2i {192,148}

ADR9/: <315> (256)
    E150 {88,4}           #U506.4i {192,156}

ADRA/: <318> (276)
    E147 {76,4}           #U506.6i {192,164}

ADRB/: <319> (280)
    E148 {80,4}           #U506.8i {192,172}

ADRC/: <330> (312)
    E145 {68,4}           #U506.11i {204,180}

ADRD/: <326> (300)
    E146 {72,4}           #U506.13i {204,172}

ADRE/: <329> (304)
    E143 {60,4}           #U506.15i {204,164}

ADRF/: <322> (292)
    E144 {64,4}           #U506.17i {204,156}
```

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Adrs.OE': <70> (148)
    #U407.11o {236,164}   #U508.1i {272,144}    #U513.4i {276,76}     #U513.13i {288,68}

Adrs.WE': <259> (192)
    #U411.14i {208,96}    #U407.15o {236,148}   #U509.11i {316,180}

Buf.WE: <133> (924)
    #U208.20i {908,80}    #U108.20i {880,80}    #U307.2o {740,68}     #U405.13i {592,68}
    #U110.20i {116,160}   #U210.20i {88,160}

Buf.WE': <132> (900)
    #U208.21i {908,76}    #U108.21i {880,76}    #U405.11o {592,76}    #U110.21i {116,156}
    #U210.21i {88,156}

BusRead: <283> (136)
    #U502.14o {300,168}   #U404.4i {176,156}

BusSel': <129> (604)
    #U506.19o {204,148}   #U407.4i {224,156}    #U406.1i {320,144}    #R502.2i {784,148}

BusWrite: <280> (128)
    #U502.12o {300,176}   #U404.10i {188,160}

C.A0: <122> (284)
    #U403.3i {548,72}     #U303.1o {644,64}     #U102.4i {756,76}     #U103.4i {784,76}
    #U105.4i {812,76}

C.A1: <121> (284)
    #U403.6i {548,84}     #U303.2o {644,68}     #U102.3i {756,72}     #U103.3i {784,72}
    #U105.3i {812,72}

C.A2: <120> (272)
    #U403.10i {560,88}    #U303.3o {644,72}     #U102.2i {756,68}     #U103.2i {784,68}
    #U105.2i {812,68}

C.A3: <118> (264)
    #U403.13i {560,76}    #U303.4o {644,76}     #U102.1i {756,64}     #U103.1i {784,64}
    #U105.1i {812,64}

C.Ack': <65> (20)
    #U305.4o {692,76}     #U111.5i {676,80}

C.B0: <117> (216)
    #U303.5o {644,80}     #U102.17i {756,128}   #U103.17i {784,128}   #U105.17i {812,128}

C.B1: <116> (216)
    #U303.6o {644,84}     #U102.18i {756,132}   #U103.18i {784,132}   #U105.18i {812,132}

C.B2: <115> (216)
    #U303.7o {644,88}     #U102.19i {756,136}   #U103.19i {784,136}   #U105.19i {812,136}

C.B3: <114> (204)
    #U303.9o {656,92}     #U102.20i {756,140}   #U103.20i {784,140}   #U105.20i {812,140}

C.Br1: <261> (84)
    #U402.6i {628,84}     #U403.7o {548,88}

C.Br2: <267> (88)
    #U402.11i {640,84}    #U403.9o {560,92}

C.Br3: <266> (88)
    #U402.14i {640,72}    #U403.12o {560,80}

C.Br4: <357> (632)
    #U107.13i {44,172}    #U405.8o {592,88}

C.Branch': <229> (120)
    #U501.5o {532,80}     #U405.9i {592,84}     #U402.1i {628,64}

C.Bro: <262> (84)
    #U402.3i {628,72}     #U403.4o {548,76}

C.C1: <251> (72)
    #U103.29i {808,108}   #U201.12o {852,80}

C.C2: <269> (96)
    #U201.11o {852,84}    #U102.29i {780,108}

C.CC0: <274> (116)
    #U302.6o {660,84}     #U501.11i {544,84}

C.CC1: <275> (116)
    #U302.7o {660,88}     #U501.10i {544,88}

C.CC2: <279> (128)
    #U302.9o {672,92}     #U501.9i {544,92}

C.ClrInterrupt: <360> (732)
    #U107.14i {44,168}    #U305.6o {692,84}

C.CY8: <328> (304)
    #U103.33o {808,92}    #U501.1i {532,64}

C.Eq': <208> (420)
    #U101.9o {608,92}     #U501.13i {544,76}    #U112.12i {256,72}    #U113.2i {212,68}

C.G0: <100> (28)
    #U105.32o {836,96}    #U201.3i {840,72}

C.G1: <239> (64)
    #U103.32o {808,96}    #U201.1i {840,64}
```

```
C.I0: <109> (148)
    #U304.1o {708,64}     #U102.12i {756,108}   #U103.12i {784,108}   #U105.12i {812,108}

C.I1: <108> (148)
    #U304.2o {708,68}     #U102.13i {756,112}   #U103.13i {784,112}   #U105.13i {812,112}

C.I2: <107> (148)
    #U304.3o {708,72}     #U102.14i {756,116}   #U103.14i {784,116}   #U105.14i {812,116}

C.I3: <112> (172)
    #U304.4o {708,76}     #U102.26i {780,120}   #U103.26i {808,120}   #U105.26i {836,120}

C.I4: <111> (160)
    #U304.5o {708,80}     #U102.28i {780,112}   #U103.28i {808,112}   #U105.28i {836,112}

C.I5: <110> (160)
    #U304.6o {708,84}     #U102.27i {780,116}   #U103.27i {808,116}   #U105.27i {836,116}

C.I6: <105> (112)
    #U304.7o {708,88}     #U102.5i {756,80}     #U103.5i {784,80}     #U105.5i {812,80}

C.I7: <104> (96)
    #U304.9o {720,92}     #U102.7i {756,88}     #U103.7i {784,88}     #U105.7i {812,88}

C.I8: <106> (140)
    #U305.1o {692,64}     #U102.6i {756,84}     #U103.6i {784,84}     #U105.6i {812,84}

C.I9: <207> (216)
    #U105.29i {836,108}   #U201.13i {852,76}    #U305.2o {692,68}

C.Inst0: <43> (180)
    #U306.10i {736,88}    #U304.10i {720,88}    #U305.10i {704,88}    #U302.10i {672,88}
    #U303.10i {656,88}    #U402.2o {628,68}     #U111.1i {676,64}

C.Inst1: <40> (144)
    #U306.11i {736,84}    #U304.11i {720,84}    #U305.11i {704,84}    #U111.2i {676,68}
    #U302.11i {672,84}    #U303.11i {656,84}    #U402.7o {628,88}

C.Inst2: <29> (120)
    #U306.12i {736,80}    #U304.12i {720,80}    #U305.12i {704,80}    #U111.3i {676,72}
    #U302.12i {672,80}    #U303.12i {656,80}    #U402.10o {640,88}

C.Inst3: <39> (104)
    #U402.15o {640,68}    #U303.13i {656,76}    #U302.13i {672,76}    #U305.13i {704,76}
    #U304.13i {720,76}    #U306.13i {736,76}

C.Inst4: <54> (796)
    #U306.14i {736,72}    #U304.14i {720,72}    #U305.14i {704,72}    #U302.14i {672,72}
    #U303.14i {656,72}    #U107.12o {44,176}

C.Neg: <273> (632)
    #U102.31o {780,100}   #U501.15i {544,68}    #U511.2i {292,68}     #U502.13i {300,172}

C.Neg': <338> (352)
    #U502.7o {288,168}    #U501.14i {544,72}

C.Next0: <192> (44)
    #U302.1o {660,64}     #U402.4i {628,76}

C.Next1: <191> (44)
    #U302.2o {660,68}     #U402.5i {628,80}

C.Next2: <97> (28)
    #U302.3o {660,72}     #U402.12i {640,80}

C.Next3: <63> (20)
    #U302.4o {660,76}     #U402.13i {640,76}

C.Next4': <244> (68)
    #U302.5o {660,80}     #U405.10i {592,80}

C.P0: <27> (12)
    #U105.35o {836,84}    #U201.4i {840,76}

C.P1: <205> (48)
    #U103.35o {808,84}    #U201.2i {840,68}

C.PU: <8> (828)
    #U508.11i {284,180}   #U406.8i {320,172}    #U406.6i {320,164}    #U406.4i {320,156}
    #U501.4i {532,76}     #U403.14i {560,72}    #U101.6i {596,84}     #U101.7i {596,88}
    #U111.6i {676,84}     #U105.9o {812,96}     #U105.21o {836,140}   #R502.10i {784,180}

C.QEmpty: <361> (736)
    #U207.18i {28,152}    #U305.5o {692,80}

C.Read': <55> (852)
    #U206.1i {0,144}      #U207.1i {16,144}     #U113.4i {212,76}     #U512.1i {228,64}
    #U512.13i {240,68}    #U307.9o {740,96}

C.Req0: <271> (100)
    #U403.2i {548,68}     #U401.9o {624,92}

C.Req1: <250> (72)
    #U403.5i {548,80}     #U401.7o {612,88}

C.Req2: <220> (52)
    #U403.11i {560,84}    #U401.6o {612,84}

C.Resume: <287> (152)
    #U305.3o {692,72}     #U403.1i {548,64}
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C.SetOverflow: <359> (720)
    #U107.18i {44,152}    #U305.9o {704,92}

C.SetTimeout: <358> (716)
    #U107.17i {44,156}    #U305.7o {692,88}

C.Y0: <312> (888)
    #U105.36o {836,80}    #U101.4i {596,76}    #U106.8i {48,172}

C.Y1: <311> (888)
    #U105.37o {836,76}    #U101.3i {596,72}    #U106.7i {48,168}

C.Y10: <292> (832)
    #U102.38o {780,72}    #U101.12i {608,80}    #U107.4i {32,156}

C.Y11: <362> (832)
    #U107.3i {32,152}    #U102.39o {780,68}

C.Y2: <310> (880)
    #U105.38o {836,72}    #U101.2i {596,68}    #U106.4i {48,156}

C.Y3: <309> (880)
    #U105.39o {836,68}    #U101.1i {596,64}    #U106.3i {48,152}

C.Y4: <303> (848)
    #U103.36o {808,80}    #U101.13i {608,76}    #U106.13i {60,172}

C.Y5: <302> (848)
    #U103.37o {808,76}    #U101.14i {608,72}    #U106.14i {60,168}

C.Y6: <301> (840)
    #U103.38o {808,72}    #U101.15i {608,68}    #U106.17i {60,156}

C.Y7: <306> (832)
    #U103.39o {808,68}    #U101.5i {596,80}    #U106.18i {60,152}

C.Y8: <294> (840)
    #U102.36o {780,80}    #U101.10i {608,88}    #U107.8i {32,172}

C.Y9: <293> (840)
    #U102.37o {780,76}    #U101.11i {608,84}    #U107.7i {32,168}

C.Zero: <7> (776)
    #R502.9i {784,176}    #R502.8i {784,172}    #R502.7i {784,168}    #U103.11o {784,104}
    #U105.11o {812,104}    #U102.11o {756,104}    #U501.3i {532,72}    #U513.12i {288,72}
    #U502.11i {300,180}

C.Zero': <337> (352)
    #U502.9o {288,176}    #U501.2i {532,68}

C170.0-85: <285> (148)
    #U405.12i {592,72}    #U116.5o {452,80}

C170.85-0: <58> (1004)
    #U206.11i {12,180}    #U207.11i {28,180}    #U107.11i {44,180}    #U106.11i {60,180}
    #U308.20i {144,176}    #U310.20i {172,176}    #U117.13o {400,76}    #U317.3i {420,72}
    #U116.15i {464,84}    #U301.11i {576,100}    #U402.9i {640,92}    #U111.4i {676,76}
    #U307.11i {752,100}    #U102.15i {756,120}    #U103.15i {784,120}    #U105.15i {812,120}

C340.0-170: <42> (180)
    #U517.1i {500,64}    #U116.3o {452,72}    #U214.12i {368,96}    #U314.12i {352,96}

C340.170-0: <41> (148)
    #U316.9i {496,92}    #U417.11i {480,100}    #U116.17i {464,76}    #U516.2i {404,68}
    #U117.12o {400,80}

C42.0-21: <86> (116)
    #U117.2i {388,68}    #U217.8o {384,88}    #U116.11i {464,100}

C42.21-0: <345> (444)
    #U116.9o {452,96}    #U215.11i {12,100}

C85.0-42: <52> (488)
    #U514.2i {48,68}    #U415.11i {44,100}    #U315.11i {28,100}    #U413.11i {124,100}
    #U116.7o {452,88}

C85.42-0: <49> (336)
    #U311.12i {172,96}    #U211.12i {188,96}    #U117.14o {400,72}    #U116.13i {464,92}

CollTest': <320> (284)
    #U407.13o {236,156}    #U216.11i {448,84}

D.00: <139> (1156)
    #U105.25i {836,124}    #U108.9o {856,96}    #U213.3i {308,72}    #U212.2o {128,68}
    #U308.26i {144,152}    #U310.26i {172,152}    #U110.9o {92,176}    #U206.2o {0,148}

D.01: <138> (1140)
    #U206.5o {0,160}    #U110.10o {92,180}    #U310.27i {172,148}    #U308.27i {144,148}
    #U212.5o {128,80}    #U213.4i {308,76}    #U108.10o {856,100}    #U105.24i {836,128}

D.02: <210> (1268)
    #U310.28i {172,144}    #U206.6o {0,164}    #U110.11o {92,184}    #U308.28i {144,144}
    #U212.6o {128,84}    #U213.7i {308,88}    #U108.11o {856,104}    #U105.23i {836,132}

D.03: <137> (1116)
    #U108.13o {880,108}    #U105.22i {836,136}    #U213.8i {308,92}    #U212.9o {128,96}
    #U308.1i {120,144}    #U310.1i {148,144}    #U110.13o {116,188}    #U206.9o {0,176}

D.04: <136> (1036)
    #U206.12o {12,176}    #U110.14o {116,184}    #U308.2i {120,148}    #U310.2i {148,148}
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    #U212.12o {140,96}    #U213.13i {320,92}    #U103.25i {808,124}   #U108.14o {880,104}

D.05: <153> (1100)
    #U108.15o {880,100}   #U103.24i {808,128}   #U213.14i {320,88}    #U212.15o {140,84}
    #U310.3i {148,152}    #U110.15o {116,180}   #U308.3i {120,152}    #U206.15o {12,164}

D.06: <59> (1092)
    #U206.16o {12,160}    #U110.16o {116,176}   #U308.6i {120,164}    #U310.6i {148,164}
    #U212.16o {140,80}    #U213.17i {320,76}    #U103.23i {808,132}   #U108.16o {880,96}

D.07: <26> (1124)
    #U206.19o {12,148}    #U110.17o {116,172}   #U308.7i {120,168}    #U310.7i {148,168}
    #U212.19o {140,68}    #U213.18i {320,72}    #U103.22i {808,136}   #U108.17o {880,92}

D.08: <256> (1088)
    #U207.2o {16,148}     #U210.9o {64,176}     #U312.2o {144,68}     #U313.3i {324,72}
    #U102.25i {780,124}   #U208.9o {884,96}

D.09: <247> (1072)
    #U207.5o {16,160}     #U210.10o {64,180}    #U312.5o {144,80}     #U313.4i {324,76}
    #U102.24i {780,128}   #U208.10o {884,100}

D.10: <246> (1064)
    #U207.6o {16,164}     #U210.11o {64,184}    #U312.6o {144,84}     #U313.7i {324,88}
    #U102.23i {780,132}   #U208.11o {884,104}

D.11: <265> (1072)
    #U207.9o {16,176}     #U210.13o {88,188}    #U312.9o {144,96}     #U313.8i {324,92}
    #U102.22i {780,136}   #U208.13o {908,108}

D.12: <245> (992)
    #U207.12o {28,176}    #U210.14o {88,184}    #U312.12o {156,96}    #U313.13i {336,92}
    #U208.14o {908,104}

D.13: <254> (1008)
    #U207.15o {28,164}    #U210.15o {88,180}    #U312.15o {156,84}    #U313.14i {336,88}
    #U208.15o {908,100}

D.14: <255> (1016)
    #U207.16o {28,160}    #U210.16o {88,176}    #U312.16o {156,80}    #U313.17i {336,76}
    #U208.16o {908,96}

D.15: <264> (1032)
    #U207.19o {28,148}    #U210.17o {88,172}    #U312.19o {156,68}    #U313.18i {336,72}
    #U208.17o {908,92}

DAT0/: <168> (416)
    #U509.3i {304,152}    #U508.2o {272,148}    #U308.18o {144,184}   E173 {180,4}

DAT1/: <167> (416)
    #U509.4i {304,156}    #U508.5o {272,160}    #U308.17o {144,188}   E174 {184,4}

DAT2/: <166> (408)
    #U509.7i {304,168}    #U508.6o {272,164}    #U308.16o {144,192}   E171 {172,4}

DAT3/: <165> (408)
    #U509.8i {304,172}    #U508.9o {272,176}    #U308.15o {144,196}   E172 {176,4}

DAT4/: <171> (456)
    #U509.13i {316,172}   #U508.12o {284,176}   #U308.14o {120,196}   E169 {164,4}

DAT5/: <172> (464)
    #U509.14i {316,168}   #U508.15o {284,164}   #U308.13o {120,192}   E170 {168,4}

DAT6/: <169> (432)
    #U509.17i {316,156}   #U508.16o {284,160}   #U308.10o {120,180}   E167 {156,4}

DAT7/: <170> (440)
    #U509.18i {316,152}   #U508.19o {284,148}   #U308.9o {120,176}    E168 {160,4}

DAT8/: <299> (400)
    #U510.3i {336,152}    #U310.18o {172,184}   E165 {148,4}

DAT9/: <298> (400)
    #U510.4i {336,156}    #U310.17o {172,188}   E166 {152,4}

DATA/: <297> (408)
    #U510.7i {336,168}    #U310.16o {172,192}   E163 {140,4}

DataO.OE': <30> (132)
    #U308.12i {120,188}   #U310.12i {148,188}   #U308.19i {144,180}   #U310.19i {172,180}
    #U407.7o {224,168}

DataO.WE': <103> (92)
    #U308.24i {144,160}   #U310.24i {172,160}   #U407.12o {236,160}

DATB/: <296> (408)
    #U510.8i {336,172}    #U310.15o {172,196}   E164 {144,4}

DATC/: <151> (432)
    #U510.13i {348,172}   #U406.9o {320,176}    #U310.14o {148,196}   E161 {132,4}

DATD/: <124> (424)
    #U510.14i {348,168}   #U406.7o {320,168}    #U310.13o {148,192}   E162 {136,4}

DATE/: <150> (424)
    #U510.17i {348,156}   #U406.5o {320,160}    #U310.10o {148,180}   E159 {124,4}

DATF/: <123> (416)
    #U510.18i {348,152}   #U406.3o {320,152}    #U310.9o {148,176}    E160 {128,4}
```

```
DS: <195> (156)
    #U404.11o {188,156}   #U407.6i {224,164}    #U503.13i {268,148}   #U406.2i {320,148}

DS': <263> (84)
    #U503.12o {268,152}   #U506.1i {192,144}

DT1-01.sil+1: <179> (40)
    #U414.18i {76,72}     #U415.16o {44,80}

DT1-01.sil+10: <177> (40)
    #U415.13i {44,92}     #U414.11o {76,100}

DT1-01.sil+11: <156> (36)
    #U415.8i {32,92}      #U414.9o {64,96}

DT1-01.sil+12: <155> (36)
    #U415.7i {32,88}      #U414.8o {64,92}

DT1-01.sil+13: <189> (44)
    #U415.4i {32,76}      #U414.7o {64,88}

DT1-01.sil+14: <188> (44)
    #U415.3i {32,72}      #U414.6o {64,84}

DT1-01.sil+15: <141> (32)
    #U413.18i {124,72}    #U412.14o {108,88}

DT1-01.sil+16: <140> (32)
    #U413.17i {124,76}    #U412.13o {108,92}

DT1-01.sil+17: <79> (24)
    #U413.14i {124,88}    #U412.12o {108,96}

DT1-01.sil+18: <78> (24)
    #U413.13i {124,92}    #U412.11o {108,100}

DT1-01.sil+19: <61> (20)
    #U413.8i {112,92}     #U412.9o {96,96}

DT1-01.sil+2: <142> (32)
    #U414.19i {76,68}     #U415.19o {44,68}

DT1-01.sil+20: <60> (20)
    #U413.7i {112,88}     #U412.8o {96,92}

DT1-01.sil+21: <94> (28)
    #U413.4i {112,76}     #U412.7o {96,88}

DT1-01.sil+22: <93> (28)
    #U413.3i {112,72}     #U412.6o {96,84}

DT1-01.sil+3: <190> (44)
    #U413.12o {124,96}    #U412.5i {96,80}

DT1-01.sil+4: <81> (24)
    #U412.17i {108,76}    #U413.15o {124,84}

DT1-01.sil+5: <80> (24)
    #U412.18i {108,72}    #U413.16o {124,80}

DT1-01.sil+6: <31> (16)
    #U412.19i {108,68}    #U413.19o {124,68}

DT1-01.sil+7: <200> (48)
    #U415.18i {44,72}     #U414.14o {76,88}

DT1-01.sil+8: <199> (48)
    #U415.17i {44,76}     #U414.13o {76,92}

DT1-01.sil+9: <178> (40)
    #U415.14i {44,88}     #U414.12o {76,96}

DT1-02.sil+1: <180> (40)
    #U311.11i {172,100}   #U211.17o {188,76}

DT1-02.sil+2: <235> (64)
    #U212.3i {128,72}     #U211.7o {176,88}

DT1-02.sil+3: <252> (76)
    #U212.4i {128,76}     #U211.13o {188,92}

DT1-02.sil+4: <214> (52)
    #U212.7i {128,88}     #U211.6o {176,84}

DT1-02.sil+5: <234> (64)
    #U212.8i {128,92}     #U211.14o {188,88}

DT1-02.sil+6: <201> (48)
    #U212.13i {140,92}    #U211.5o {176,80}

DT1-02.sil+7: <213> (52)
    #U212.14i {140,88}    #U211.15o {188,84}

DT1-02.sil+8: <157> (36)
    #U212.17i {140,76}    #U211.4o {176,76}

DT1-02.sil+9: <224> (56)
    #U212.18i {140,72}    #U211.16o {188,80}

DT1-03.sil+1: <21> (36)
    #U513.1i {276,64}     #U513.10i {288,80}    #U513.8o {288,88}
```

```
DT1-04.sil+1: <232> (60)
    #U417.3i {468,72}     #U416.6o {516,84}

DT1-04.sil+2: <231> (60)
    #U417.4i {468,76}     #U416.7o {516,88}

DT1-04.sil+3: <217> (52)
    #U417.7i {468,88}     #U416.8o {516,92}

DT1-04.sil+4: <237> (64)
    #U417.17i {480,76}    #U416.13o {528,92}

DT1-04.sil+5: <236> (64)
    #U417.18i {480,72}    #U416.14o {528,88}

DT1-04.sil+6: <216> (52)
    #U417.8i {468,92}     #U416.9o {516,96}

DT1-04.sil+7: <226> (56)
    #U417.13i {480,92}    #U416.11o {528,100}

DT1-04.sil+8: <257> (80)
    #U317.2i {420,68}     #U316.6o {484,84}

DT1-04.sil+9: <225> (56)
    #U417.14i {480,88}    #U416.12o {528,96}

DT1-05.sil+1: <243> (68)
    #U401.10i {624,88}    #U301.19o {576,68}

DT1-05.sil+2: <219> (52)
    #U401.11i {624,84}    #U301.16o {576,80}

DT1-05.sil+3: <218> (52)
    #U401.12i {624,80}    #U301.15o {576,84}

DT1-05.sil+4: <242> (68)
    #U401.13i {624,76}    #U301.12o {576,96}

DT1-05.sil+5: <258> (80)
    #U401.1i {612,64}     #U301.9o {564,96}

DT1-05.sil+6: <238> (64)
    #U401.2i {612,68}     #U301.6o {564,84}

DT1-05.sil+7: <228> (56)
    #U401.3i {612,72}     #U301.5o {564,80}

DT1-05.sil+8: <227> (56)
    #U401.4i {612,76}     #U301.2o {564,68}

DT1-06.sil+1: <161> (36)
    #U307.18i {752,72}    #U306.1o {724,64}

DT1-06.sil+2: <160> (36)
    #U307.17i {752,76}    #U306.2o {724,68}

DT1-06.sil+3: <194> (44)
    #U307.14i {752,88}    #U306.3o {724,72}

DT1-06.sil+4: <193> (44)
    #U307.13i {752,92}    #U306.4o {724,76}

DT1-06.sil+5: <99> (28)
    #U307.8i {740,92}     #U306.5o {724,80}

DT1-06.sil+6: <64> (20)
    #U307.7i {740,88}     #U306.6o {724,84}

DT1-06.sil+7: <98> (28)
    #U307.4i {740,76}     #U306.7o {724,88}

DT1-06.sil+8: <85> (24)
    #U307.3i {740,72}     #U306.9o {736,92}

DT1-07.sil+1: <148> (32)
    #U103.8i {784,92}     #U102.9o {756,96}

DT1-07.sil+2: <147> (32)
    #U105.8i {812,92}     #U103.9o {784,96}

DT1-07.sil+3: <67> (20)
    #U103.16i {784,124}   #U102.21o {780,140}

DT1-07.sil+4: <66> (20)
    #U105.16i {812,124}   #U103.21o {808,140}

DT1-09.sil+1: <350> (464)
    #U404.1i {176,144}    #U405.6o {580,84}

DT1-09.sil+2: <353> (480)
    #U405.3o {580,72}     #U404.2i {176,148}

DT1-10.sil+1: <102> (28)
    #U404.13i {188,148}   #U404.6o {176,164}

GND: <13> (10732)
    #U504.8i {352,172}    #U510.10i {336,180}   #U406.10i {320,180}   #U509.10i {304,180}
    #U502.10i {288,180}   #U508.10i {272,180}   #U503.7i {256,168}    #U407.8i {224,172}
    #U506.10i {192,180}   #U404.7i {176,168}    #U110.12i {92,188}    #U210.12i {64,188}
```

```
    #U106.10i {48,180}    #U107.10i {32,180}    #U207.10i {16,180}    #U206.10i {0,180}
    #U208.12i {884,108}   #U108.12i {856,108}   #U201.8i {840,92}     #U307.10i {740,100}
    #U306.8i {724,92}     #U304.8i {708,92}     #U305.8i {692,92}     #U111.8i {676,92}
    #U302.8i {660,92}     #U303.8i {644,92}     #U402.8i {628,92}     #U401.8i {612,92}
    #U101.8i {596,92}     #U405.7i {580,88}     #U301.10i {564,100}   #U403.8i {548,92}
    #U501.8i {532,92}     #U416.10i {516,100}   #U517.7i {500,88}     #U316.8i {484,92}
    #U417.10i {468,100}   #U116.10i {452,100}   #U216.8i {436,92}     #U317.7i {420,88}
    #U516.8i {404,92}     #U117.8i {388,92}     #U217.7i {372,88}     #U214.10i {356,100}
    #U314.10i {340,100}   #U313.10i {324,100}   #U213.10i {308,100}   #U511.7i {292,88}
    #U513.7i {276,88}     #U114.7i {260,88}     #U112.7i {244,88}     #U512.7i {228,88}
    #U113.7i {212,88}     #U411.8i {192,92}     #U211.10i {176,100}   #U311.10i {160,100}
    #U312.10i {144,100}   #U212.10i {128,100}   #U413.10i {112,100}   #U412.10i {96,100}
    #U515.7i {80,88}      #U414.10i {64,100}    #U514.8i {48,92}      #U415.10i {32,100}
    #U315.10i {16,100}    #U215.10i {0,100}     C505 {484,44}         C511 {508,44}
    C514 {8,48}           C520 {32,48}          C524 {48,48}          E185 {228,4}
    E186 {232,4}          E176 {192,4}          E175 {188,4}          E112 {448,0}
    E111 {444,0}          E102 {408,0}          E101 {404,0}          #c316.2o {776,144}
    #c317.2o {760,144}    #c313.2o {408,144}    #c315.2o {424,144}    #c215.2o {456,144}
    #c211.2o {440,144}    #c217.2o {520,144}    #c213.2o {504,144}    #c301.2o {472,144}
    #c304.2o {488,144}    #c306.2o {552,144}    #c101.2o {536,144}    #c417.2o {568,144}
    #c517.2o {584,144}    #c515.2o {616,144}    #c513.2o {600,144}    #c511.2o {664,144}
    #c509.2o {632,144}    #c505.2o {648,144}    #c503.2o {744,144}    #c502.2o {728,144}
    #c501.2o {696,144}    #c401.2o {712,144}    #c302.2o {680,144}    #U118.12i {368,188}
    #U118.13i {392,188}   #U118.15o {392,180}   #U118.10o {368,180}   #R115.13o {804,156}
    #R115.15o {804,148}   #U502.19i {300,148}   #U502.1i {288,144}    #U507.1i {240,144}
    #U507.2i {240,148}    #U507.3i {240,152}    #U507.4i {240,156}    #U507.5i {240,160}
    #U507.6i {240,164}    #U507.7i {240,168}    #U507.8i {240,172}    #U407.5i {224,160}
    #U505.1i {208,144}    #U505.2i {208,148}    #U505.3i {208,152}    #U505.4i {208,156}
    #U505.5i {208,160}    #U505.6i {208,164}    #U505.7i {208,168}    #U505.8i {208,172}
    #U310.22i {172,168}   #U308.22i {144,168}   #U310.23i {172,164}   #U308.23i {144,164}
    #U107.1i {32,144}     #U106.1i {48,144}     #U105.40i {836,64}    #U103.40i {808,64}
    #U102.40i {780,64}    #U102.30o {780,104}   #U103.30o {808,104}   #U105.30o {836,104}
    #U307.1i {740,64}     #U302.15i {672,68}    #U306.15i {736,68}    #U305.15i {704,68}
    #U304.15i {720,68}    #U303.15i {656,68}    #U403.15i {660,68}    #U301.1i {564,64}
    #U401.5i {612,80}     #U501.7i {532,88}     #U501.12i {544,80}    #U301.18i {576,72}
    #U416.15i {528,84}    #U116.19i {464,68}    #U116.1i {452,64}     #U517.5i {500,80}
    #U517.8i {512,88}     #U417.1i {468,64}     #U216.15i {448,68}    #U316.7i {484,88}
    #U517.3i {500,72}     #U416.16i {528,80}    #U216.2i {436,68}     #U213.1i {308,64}
    #U313.1i {324,64}     #U512.2i {228,68}     #U311.19i {172,68}    #U311.2i {160,68}
    #U311.18i {172,72}    #U211.19i {188,68}    #U211.2i {176,68}     #U211.18i {188,72}
    #U411.12i {208,104}   #U411.13i {208,100}   #U413.1i {112,64}     #U412.16i {108,80}
    #U412.15i {108,84}    #U515.8i {92,88}      #U515.5i {80,80}      #U515.3i {80,72}
    #U414.16i {76,80}     #U315.1i {16,64}      #U415.1i {32,64}      #U414.15i {76,84}
    #U216.1i {0,64}

Init': <327> (696)
    #U301.17i {576,76}    #U510.19o {348,148}   #U315.18i {28,72}

INIT/: <317> (264)
    E114 {456,0}          #U510.1i {336,144}

Int: <206> (184)
    #U406.11i {332,180}   #U502.15i {300,164}   #U404.3o {176,152}

Int': <253> (76)
    #U504.12i {364,160}   #U502.5o {288,160}

Int0: <101> (28)
    #U504.15i {364,148}   #U510.2o {336,148}

INT0/: <344> (440)
    E141 {52,4}           #U504.1o {352,144}

Int1: <164> (36)
    #U504.14i {364,152}   #U510.5o {336,160}

INT1/: <343> (440)
    E142 {56,4}           #U504.2o {352,148}

Int2: <163> (36)
    #U504.13i {364,156}   #U510.6o {336,164}

INT2/: <348> (456)
    E139 {44,4}           #U504.3o {352,152}

INT3/: <347> (456)
    E140 {48,4}           #U504.4o {352,156}

INT4/: <352> (472)
    E137 {36,4}           #U504.5o {352,160}

INT5/: <351> (472)
    E138 {40,4}           #U504.6o {352,164}

INT6/: <354> (488)
    E135 {28,4}           #U504.7o {352,168}

INT7/: <356> (500)
    E136 {32,4}           #U504.9o {364,172}

IORC/: <340> (360)
    E121 {484,0}          #U502.6i {288,164}

IOWC/: <341> (372)
    E122 {488,0}          #U502.8i {288,172}

LoopBack': <295> (184)
    #U510.16o {348,160}   #U216.1i {436,64}

P.Read': <6> (704)
    #U308.4i {120,156}    #U308.25i {144,156}   #U310.4i {148,156}    #U310.25i {172,156}
```

```
    #U307.15o {752,84}

P.ReadReq': <260> (552)
    #U308.11o {120,184}   #U404.5i {176,160}    #U301.14i {676,88}

P.Write': <130> (684)
    #U308.21i {144,172}   #U310.21i {172,172}   #U307.12o {752,96}

P.WriteReq: <291> (172)
    #U502.4i {288,156}    #U308.5o {120,160}

P.WriteReq': <277> (460)
    #U404.9i {188,164}    #U502.16o {300,160}   #U301.13i {576,92}

Pd.Carrier: <221> (460)
    #U414.1i {64,64}      #U413.2o {112,68}     #U416.1i {516,64}

Pd.Coll: <334> (340)
    #U317.11i {432,76}    #U413.9o {112,96}

Pd.Data: <87> (156)
    #U414.2i {64,68}      #U515.11i {92,76}     #U413.5o {112,80}     #U211.11i {188,100}

Pd.Data0: <69> (104)
    #U315.7i {16,88}      #U315.2o {16,68}      #U412.1i {96,64}

Pd.Data1: <28> (104)
    #U315.8i {16,92}      #U315.5o {16,80}      #U412.2i {96,68}

Pd.Data2: <268> (92)
    #U412.3i {96,72}      #U315.6o {16,84}

Pd.Data3: <270> (100)
    #U412.4i {96,76}      #U315.9o {16,96}

Pd.Shift: <44> (192)
    #U211.1i {176,64}     #U311.1i {160,64}     #U413.6o {112,84}     #U515.1i {80,64}
    #U414.3i {64,72}      #U514.7i {48,88}

PU.00: <162> (36)
    #U506.3i {192,152}    #U505.16o {220,144}

PU.01: <186> (612)
    #U506.5i {192,160}    #U505.15o {220,148}   #R505.3i {788,152}

PU.02: <198> (616)
    #U506.7i {192,168}    #U505.14o {220,152}   #R505.4i {788,156}

PU.03: <209> (620)
    #U506.9i {192,176}    #U505.13o {220,156}   #R505.5i {788,160}

PU.04: <152> (604)
    #U506.12i {204,176}   #U505.12o {220,160}   #R505.6i {788,164}

PU.05: <73> (592)
    #U506.14i {204,168}   #U505.11o {220,164}   #R505.7i {788,168}

PU.06: <5> (600)
    #U506.16i {204,160}   #U505.10o {220,168}   #R505.8i {788,172}    #R505.9i {788,176}

PU.07: <176> (612)
    #U506.18i {204,152}   #U505.9o {220,172}    #R505.10i {788,180}

PU.08: <128> (536)
    #U507.16o {252,144}   #U508.3i {272,152}    #R507.3i {780,152}

PU.09: <127> (536)
    #U507.15o {252,148}   #U508.4i {272,156}    #R507.4i {780,156}

PU.10: <175> (552)
    #U507.14o {252,152}   #U508.7i {272,168}    #R507.5i {780,160}

PU.11: <174> (552)
    #U507.13o {252,156}   #U508.8i {272,172}    #R507.6i {780,164}

PU.12: <196> (544)
    #U507.12o {252,160}   #U508.13i {284,172}   #R507.7i {780,168}

PU.13: <173> (536)
    #U507.11o {252,164}   #U508.14i {284,168}   #R507.8i {780,172}

PU.14: <197> (560)
    #U507.10o {252,168}   #U508.17i {284,156}   #R507.9i {780,176}

PU.15: <222> (576)
    #U507.9o {252,172}    #U508.18i {284,152}   #R507.10i {780,180}

R.Abort: <321> (288)
    #U207.14i {28,168}    #U512.5o {228,80}

R.ClrInterrupt: <325> (300)
    #U107.15o {44,164}    #U112.11i {256,76}

R.CrcErr: <324> (300)
    #U207.13i {28,172}    #U512.9o {240,84}

R.EndAck': <126> (468)
    #U112.1i {244,64}     #U112.10i {256,80}    #U111.14o {688,72}

R.EndReq': <332> (328)
    #U301.4i {564,76}     #U112.6o {244,84}
```

```
R.FdIn: <304> (212)
    #U510.15o {348,164}   #U411.15i {208,92}

R.IntEn: <336> (344)
    #U510.9o {336,176}    #U405.4i {580,76}

R.Interrupt: <288> (492)
    #U405.5i {580,80}     #U112.9o {256,84}     #U406.13i {332,172}

R.Overflow: <314> (256)
    #U207.17i {28,156}    #U113.6o {212,84}

R.OverFlow': <35> (36)
    #U113.1i {212,64}     #U113.5o {212,80}     #U113.12i {224,72}

R.Read': <53> (628)
    #U212.1i {128,64}     #U312.1i {144,64}     #U307.19o {752,68}

R.ReadyAck': <349> (464)
    #U111.15o {688,68}    #U113.13i {224,68}

R.ReadyReq': <339> (356)
    #U301.3i {564,72}     #U113.8o {224,88}

R.SetOverflow: <307> (244)
    #U107.19o {44,148}    #U113.3i {212,72}

Rx.A0: <149> (276)
    #U311.7o {160,88}     #U312.3i {144,72}     #U411.2i {192,68}     #U509.2o {304,148}

Rx.A1: <184> (284)
    #U312.4i {144,76}     #U311.13o {172,92}    #U411.3i {192,72}     #U509.5o {304,160}

Rx.A2: <72> (260)
    #U312.7i {144,88}     #U311.6o {160,84}     #U411.4i {192,76}     #U509.6o {304,164}

Rx.A3: <119> (268)
    #U312.8i {144,92}     #U311.14o {172,88}    #U411.5i {192,80}     #U509.9o {304,176}

Rx.A4: <48> (268)
    #U312.13i {156,92}    #U311.5o {160,80}     #U411.6i {192,84}     #U509.12o {316,176}

Rx.A5: <71> (244)
    #U312.14i {156,88}    #U311.15o {172,84}    #U411.9i {192,96}     #U509.15o {316,164}

Rx.A6: <3> (244)
    #U312.17i {156,76}    #U311.4o {160,76}     #U411.10i {192,100}   #U509.16o {316,160}

Rx.A7: <88> (236)
    #U312.18i {156,72}    #U311.16o {172,80}    #U411.11i {192,104}   #U509.19o {316,148}

Rx.Abort': <300> (204)
    #U512.4i {228,76}     #U415.6o {32,84}

Rx.Adrs: <211> (52)
    #U414.5i {64,80}      #U315.12o {28,96}

Rx.Clear': <143> (32)
    #U514.9i {60,92}      #U415.9o {32,96}

Rx.CrcClr: <223> (56)
    #U515.4i {80,76}      #U415.12o {44,96}

Rx.CrcErr: <286> (152)
    #U512.12i {240,72}    #U515.13o {92,68}

Rx.Data: <346> (452)
    #U216.7o {436,88}     #U215.3i {0,72}

Rx.Data0: <18> (8)
    #U215.2o {0,68}       #U215.4i {0,76}

Rx.Data1: <17> (8)
    #U215.5o {0,80}       #U215.7i {0,88}

Rx.Data2: <20> (36)
    #U215.8i {0,92}       #U215.6o {0,84}       #U315.3i {16,72}

Rx.Data3: <154> (36)
    #U315.4i {16,76}      #U215.9o {0,96}

Rx.Enable: <50> (368)
    #U315.19o {28,68}     #U414.17i {76,76}     #U509.1i {304,144}    #U502.17i {300,156}

Rx.Enable': <45> (208)
    #U311.3i {160,72}     #U211.3i {176,72}     #U502.3o {288,152}

Rx.End: <23> (228)
    #U112.3i {244,72}     #U512.11i {240,76}    #U512.3i {228,72}     #U415.5o {32,80}

Rx.FCE': <289> (168)
    #U411.1i {192,64}     #U415.15o {44,84}

Rx.FdOut: <290> (824)
    #U315.13i {28,92}     #U411.7o {192,88}     #R502.3i {784,152}

Rx.PU: <10> (944)
    #U514.10i {60,88}     #U514.6i {48,84}      #U514.5i {48,80}      #U514.4i {48,76}
    #U514.3i {48,72}      #U514.1i {48,64}      #U515.2i {80,68}      #U515.10i {92,80}
    #U311.9i {160,96}     #U211.9i {176,96}     #U113.10i {224,80}    #U512.10i {240,80}
```

```
    #U112.4i {244,76}     #U112.2i {244,68}     #U112.13i {256,68}    #U511.1i {292,64}
    #R115.6i {792,164}

Rx.Word: <212> (52)
    #U514.15o {60,68}     #U315.14i {28,88}

Rx.Word0: <187> (44)
    #U414.4i {64,76}      #U315.15o {28,84}

Rx.Write: <47> (248)
    #U415.2o {32,68}      #U212.11i {140,100}   #U312.11i {156,100}   #U113.11i {224,76}

RxBuf.CE': <113> (176)
    #U307.5o {740,80}     #U108.18i {880,88}    #U208.18i {908,88}

Status.OE': <276> (116)
    #U406.19i {332,148}   #U407.10o {236,168}

Status.WE': <284> (140)
    #U510.11i {348,180}   #U407.14o {236,152}

T.AbortAck': <125> (428)
    #U114.13i {272,68}    #U511.4i {292,76}     #U111.12o {688,80}

T.AbortReq': <323> (296)
    #U301.8i {564,92}     #U114.8o {272,88}

T.IntEn: <335> (344)
    #U510.12o {348,176}   #U405.1i {580,64}

T.Interrupt: <281> (448)
    #U405.2i {580,68}     #U513.6o {276,84}     #U406.17i {332,156}

T.ReadyAck': <185> (440)
    #U114.1i {260,64}     #U511.3i {292,72}     #U111.13o {688,76}

T.SetTimeOut: <333> (328)
    #U107.16o {44,160}    #U513.11i {288,76}

T.Write': <51> (452)
    #U213.11i {320,100}   #U313.11i {336,100}   #U307.16o {752,80}

TD.00: <241> (68)
    #U214.7o {356,88}     #U213.2o {308,68}

TD.01: <248> (72)
    #U214.13o {368,92}    #U213.5o {308,80}

TD.02: <203> (48)
    #U214.6o {356,84}     #U213.6o {308,84}

TD.03: <240> (68)
    #U214.14o {368,88}    #U213.9o {308,96}

TD.04: <215> (52)
    #U214.5o {356,80}     #U213.12o {320,96}

TD.05: <202> (48)
    #U214.15o {368,84}    #U213.15o {320,84}

TD.06: <181> (40)
    #U214.4o {356,76}     #U213.16o {320,80}

TD.07: <230> (60)
    #U214.16o {368,80}    #U213.19o {320,68}

TD.08: <159> (36)
    #U313.2o {324,68}     #U314.7o {340,88}

TD.09: <182> (40)
    #U313.5o {324,80}     #U314.13o {352,92}

TD.10: <33> (16)
    #U313.6o {324,84}     #U314.6o {340,84}

TD.11: <158> (36)
    #U313.9o {324,96}     #U314.14o {352,88}

TD.12: <62> (20)
    #U313.12o {336,96}    #U314.5o {340,80}

TD.13: <32> (16)
    #U313.15o {336,84}    #U314.15o {352,84}

TD.14: <19> (8)
    #U313.16o {336,80}    #U314.4o {340,76}

TD.15: <95> (28)
    #U313.19o {336,68}    #U314.16o {352,80}

Tx.Coll': <96> (28)
    #U216.9o {448,92}     #U317.10i {432,80}

Tx.CrcIn: <146> (32)
    #U517.11i {512,76}    #U316.5o {484,80}

Tx.CrcOut: <145> (32)
    #U316.4i {484,76}     #U517.12o {512,72}

Tx.Data: <2> (100)
    #U317.5o {420,80}     #U216.5i {436,80}     #U216.3i {436,72}     #U316.15i {496,68}
```

```
    #U316.14i {496,72}    #U316.13i {496,76}    #U316.12i {496,80}

Tx.Go: <37> (52)
    #U317.1i {420,64}     #U317.13i {432,68}    #U417.2o {468,68}

Tx.Go': <22> (208)
    #U513.3i {276,72}     #U114.11i {272,76}    #U417.5o {468,80}

Tx.Idle: <36> (40)
    #U517.4i {500,76}     #U316.10i {496,88}    #U417.12o {480,96}

Tx.Idle': <249> (72)
    #U516.9i {416,92}     #U417.15o {480,84}

Tx.Inhibit: <305> (224)
    #U416.5i {516,80}     #U511.5o {292,80}

Tx.Jam: <24> (460)
    #U215.13i {12,92}     #U114.12i {272,72}    #U513.2i {276,68}     #U317.9o {432,84}

Tx.Jam': <84> (24)
    #U317.8o {432,88}     #U317.4i {420,76}

Tx.Jam0: <16> (8)
    #U215.12o {12,96}     #U215.14i {12,88}

Tx.Jam1: <15> (8)
    #U215.15o {12,84}     #U215.17i {12,76}

Tx.Jam2: <14> (8)
    #U215.16o {12,80}     #U215.18i {12,72}

Tx.Jam3: <77> (24)
    #U315.17i {28,76}     #U215.19o {12,68}

Tx.Jam4: <355> (500)
    #U416.2i {516,68}     #U315.16o {28,80}

Tx.Load: <46> (228)
    #U114.3i {260,72}     #U314.19i {352,68}    #U214.19i {368,68}    #U417.6o {468,84}

Tx.PU: <11> (1024)
    #U216.14i {448,72}    #U216.13i {448,76}    #U317.12i {432,72}    #U516.3i {404,72}
    #U516.4i {404,76}     #U516.5i {404,80}     #U516.6i {404,84}     #U516.7i {404,88}
    #U117.10i {400,88}    #U117.9i {400,92}     #U117.7i {388,88}     #U117.6i {388,84}
    #U117.5i {388,80}     #U117.4i {388,76}     #U117.3i {388,72}     #U117.1i {388,64}
    #U214.18i {368,72}    #U214.3i {356,72}     #U214.2i {356,68}     #U214.1i {356,64}
    #U314.18i {352,72}    #U314.3i {340,72}     #U114.10i {272,80}    #U114.4i {260,76}
    #U114.2i {260,68}     #U314.2i {340,68}     #U314.1i {340,64}     #U314.9i {340,96}
    #U314.11i {352,100}   #U214.9i {356,96}     #U214.11i {368,100}   #U516.10i {416,88}
    #U516.1i {404,64}     #U316.1i {484,64}     #U316.2i {484,68}     #U517.2i {500,68}
    #R115.5i {792,160}

Tx.Ready: <233> (324)
    #U114.6o {260,84}     #U416.4i {516,76}     #U301.7i {564,88}

Tx.SRData: <282> (136)
    #U316.3i {484,72}     #U314.17o {352,76}

Tx.State0: <68> (64)
    #U417.16o {480,80}    #U316.11i {496,84}    #U517.10i {512,80}    #U416.18i {528,72}

Tx.State1: <204> (48)
    #U417.19o {480,68}    #U416.19i {528,68}

Tx.Timeout: <278> (372)
    #U416.17i {528,76}    #U513.9o {288,84}     #U406.15i {332,164}

Tx.Word: <272> (104)
    #U516.15o {416,68}    #U416.3i {516,72}

TxBuf.CE': <131> (736)
    #U307.6o {740,84}     #U110.18i {116,168}   #U210.18i {88,168}

VCC: <12> (5988)
    #U504.16i {364,144}   #U510.20i {348,144}   #U406.20i {332,144}   #U509.20i {316,144}
    #U502.20i {300,144}   #U508.20i {284,144}   #U503.14i {268,144}   #U407.16i {236,144}
    #U506.20i {204,144}   #U404.14i {188,144}   #U110.24i {116,144}   #U210.24i {88,144}
    #U106.20i {60,144}    #U107.20i {44,144}    #U207.20i {28,144}    #U206.20i {12,144}
    #U208.24i {908,64}    #U108.24i {880,64}    #U201.16i {852,64}    #U307.20i {752,64}
    #U306.16i {736,64}    #U304.16i {720,64}    #U305.16i {704,64}    #U111.16i {688,64}
    #U302.16i {672,64}    #U303.16i {656,64}    #U402.16i {640,64}    #U401.16i {624,64}
    #U101.16i {608,64}    #U405.14i {592,64}    #U301.20i {576,64}    #U403.16i {560,64}
    #U501.16i {544,64}    #U416.20i {528,64}    #U517.14i {512,64}    #U316.16i {496,64}
    #U417.20i {480,64}    #U116.20i {464,64}    #U216.16i {448,64}    #U317.14i {432,64}
    #U516.16i {416,64}    #U117.16i {400,64}    #U217.14i {384,64}    #U214.20i {368,64}
    #U314.20i {352,64}    #U313.20i {336,64}    #U213.20i {320,64}    #U511.14i {304,64}
    #U513.14i {288,64}    #U114.14i {272,64}    #U112.14i {256,64}    #U512.14i {240,64}
    #U113.14i {224,64}    #U411.22i {208,64}    #U211.20i {188,64}    #U311.20i {172,64}
    #U312.20i {156,64}    #U212.20i {140,64}    #U413.20i {124,64}    #U412.20i {108,64}
    #U515.14i {92,64}     #U414.20i {76,64}     #U514.16i {60,64}     #U415.20i {44,64}
    #U315.20i {28,64}     #U215.20i {12,64}     C521 {36,48}          E184 {224,4}
    E182 {216,4}          E181 {212,4}          E183 {220,4}          E105 {420,0}
    E106 {424,0}          E104 {416,0}          E103 {412,0}          #R115.11o {804,164}
    #R115.12o {804,160}   #R115.14o {804,152}   #R115.16o {804,144}   #R505.1i {788,144}
    #R502.1i {784,144}    #R507.1i {780,144}    #c101.1i {524,144}    #c306.1i {540,144}
    #c304.1i {476,144}    #c301.1i {460,144}    #c213.1i {492,144}    #c217.1i {508,144}
    #c211.1i {428,144}    #c215.1i {444,144}    #c315.1i {412,144}    #c313.1i {396,144}
    #c317.1i {748,144}    #c316.1i {764,144}    #c302.1i {668,144}    #c401.1i {700,144}
    #c501.1i {684,144}    #c502.1i {716,144}    #c503.1i {732,144}    #c505.1i {636,144}
    #c509.1i {620,144}    #c511.1i {652,144}    #c513.1i {588,144}    #c515.1i {604,144}
```

```
    #c517.1i {572,144}    #c417.1i {556,144}    #U118.1i {368,144}    #U118.24i {392,144}
    #U310.8i {148,172}    #U308.8i {120,172}    #U102.10o {756,100}   #U103.10o {784,100}
    #U105.10o {812,100}

Write': <38> (52)
    #U407.3i {224,152}    #U404.12i {188,152}   #U404.8o {188,168}

X.15V: <89> (528)
    #U118.14o {392,184}   #U118.11o {368,184}   C512 {0,48}

X.Collision: <9> (888)
    #R115.4i {792,156}    #R115.3i {792,152}    #U116.8i {452,92}     C515 {12,48}

X.Collision': <82> (24)
    #U216.10i {448,88}    #U116.12o {464,96}

X.RCVData: <4> (476)
    #R115.2i {792,148}    #R115.1i {792,144}    C506 {488,44}         #U116.4i {452,76}

X.RCVData1': <34> (16)
    #U116.16o {464,80}    #U116.6i {452,84}

X.RCVData2: <144> (32)
    #U116.14o {464,88}    #U216.6i {436,84}

X.XMTData': <342> (436)
    C525 {52,48}          #U116.18o {464,72}

X.XMTData1: <83> (24)
    #U116.2i {452,68}     #U216.4o {436,76}

XACK/: <331> (312)
    E123 {492,0}          #U406.18o {332,152}
```

```
// Sun-Proms.bcpl -- Sun 3 MB Ethernet board Proms
// Last modified February 10, 1984  4:00 PM by Boggs
// Sun-Rev-B & CadLink-Rev-0 boards require a hardware change: (TX
Multibus/Fifo interlock)
//  isolate U308 pin 4; connect it to U308 pin 25 (P.Read/)
// Other known hardware fixes:
//  isolate U511 pin 4; connect it to U111 pin 12 (T.AbortAck/)
//  isolate U513 pin 2; connect it to U317 pin 9 (TX.Jam)

external [ Ws; OpenFile; Puts; Closes; Allocate; Free; sysZone ]

static [ memory; mbFile ]

structure String [ length byte; char↑1,1 byte ]

manifest [ high = 1; low = 0 ]

//---------------------------------------------------------------------------
let SunProms() be
//---------------------------------------------------------------------------
[
mbFile = OpenFile("Sun-Proms.mb")

DoMemory("TX", 256, 8, TX)
DoMemory("NewTX", 256, 8, NewTX)
DoMemory("Ctrl", 32, 40, Ctrl)

Puts(mbFile, 0)  //0 = end of file
Closes(mbFile)
]

//---------------------------------------------------------------------------
and DoMemory(name, nAddr, nData, Proc) be
//---------------------------------------------------------------------------
// nAddr is number of addresses
// nData is number of output bits
[
Ws("*N"); Ws(name)

Puts(mbFile, 4)  //4 = define memory
memory = memory +1
Puts(mbFile, memory)
Puts(mbFile, nData)
if name>>String.length gr 1 then
   for i = 1 to name>>String.length-1 by 2 do
      Puts(mbFile, name>>String.char↑i lshift 8 + name>>String.char↑(i+1))
Puts(mbFile, (name>>String.length & 1) eq 0? 0,
 name>>String.char↑(name>>String.length) lshift 8)

Puts(mbFile, 2)  //2 = set current memory
Puts(mbFile, memory)
Puts(mbFile, 0)  //location counter
```

```
let data = Allocate(sysZone, (nData+15)/16)
for addr = 0 to nAddr-1 do
  [
  Puts(mbFile, 1)  //1 = memory contents
  Puts(mbFile, 0)  //source line number
  Proc(addr, data)
  for i = 0 to (nData+15)/16 -1 do Puts(mbFile, data!i)
  ]
Free(sysZone, data)
]

//---------------------------------------------------------------------------------------
and TX(addr, data) be
//---------------------------------------------------------------------------------------
[
structure Addr:
  [
  blank bit 8
  state bit 2
  timeout bit
  inhibit bit
  ready bit
  wrd bit
  jam bit
  carrier bit
  ]

structure Data:
  [
  nextState bit 2
  notIdle bit
  idle bit
  blank bit
  load bit
  notGo bit
  go bit
  blank bit 8
  ]

manifest
  [
  stateIdle = 0
  stateData = 1
  stateCRC = 2
  ]

let state = addr<<Addr.state
let timeout = addr<<Addr.timeout eq high
let inhibit = addr<<Addr.inhibit eq high
let ready = addr<<Addr.ready eq high
let wrd = addr<<Addr.wrd eq high
let jam = addr<<Addr.jam eq high
```

```
let carrier = addr<<Addr.carrier eq high

let nextState = state
let idle, load, go = false, false, false

switchon state into
   [
   case stateIdle:
      [
      if not ready % carrier then idle = true
      if ready & not carrier then nextState = stateData //aquire Ether
      endcase
      ]
   case stateData:
      [
      go = not jam
      if not jam & wrd & ready then load = true
      if wrd & inhibit then nextState = stateCRC  //end of data
      if wrd & not ready then nextState = stateIdle    //data late
      if jam % timeout then nextState = stateIdle  //catastrophe
      endcase
      ]
   case stateCRC:
      [
      go = not jam
      if wrd then nextState = stateIdle       //end of CRC
      if jam % timeout then nextState = stateIdle  //catastrophe
      endcase
      ]
   default: nextState = stateIdle
   ]

data>>Data.nextState = nextState
data>>Data.notIdle = idle? low, high
data>>Data.idle = idle? high, low
data>>Data.load = load? high, low
data>>Data.notGo = go? low, high
data>>Data.go = go? high, low
]

//-------------------------------------------------------------------------------
and NewTX(addr, data) be
//-------------------------------------------------------------------------------
[
structure Addr:
   [
   blank bit 8
   state bit 2
   timeout bit
   inhibit bit
   ready bit
   wrd bit
```

```
  jam bit
  carrier bit
  ]

structure Data:
  [
  nextState bit 2
  notIdle bit
  idle bit
  done bit      //low true
  load bit
  abrt bit      //low true
  go bit
  blank bit 8
  ]

manifest
  [
  stateIdle = 0
  stateData = 1
  stateCRC = 2
  ]

let state = addr<<Addr.state
let timeout = addr<<Addr.timeout eq high
let inhibit = addr<<Addr.inhibit eq high
let ready = addr<<Addr.ready eq high
let wrd = addr<<Addr.wrd eq high
let jam = addr<<Addr.jam eq high
let carrier = addr<<Addr.carrier eq high

let nextState = state
let idle, load, go = false, false, false

switchon state into
  [
  case stateIdle:
    [
    if ready & not carrier & not inhibit then nextState = stateData //aquire
Ether
    endcase
    ]
  case stateData:
    [
    go = not jam
    if not jam & not inhibit & wrd & ready then load = true
    if wrd & inhibit then nextState = stateCRC  //end of data
    if wrd & not ready then nextState = stateIdle    //data late
    if jam % timeout then nextState = stateIdle  //catastrophe
    endcase
    ]
  case stateCRC:
```

```
      [
      go = not jam
      if wrd then nextState = stateIdle       //end of CRC
      if jam % timeout then nextState = stateIdle  //catastrophe
      endcase
      ]
   default: nextState = stateIdle
   ]

data>>Data.nextState = nextState
data>>Data.notIdle = nextState ne stateIdle? low, high
data>>Data.idle = nextState eq stateIdle? high, low
data>>Data.done = (nextState eq stateIdle & not jam)? low, high
data>>Data.load = load? high, low
data>>Data.abrt = jam? low, high
data>>Data.go = go? high, low
]

//-------------------------------------------------------------------------------
and Ctrl(addr, data) be
//-------------------------------------------------------------------------------
[
structure Addr:
   [
   blank bit 11
   Instr bit 5
   ]

structure Data:
   [
   BufWE bit
   RBufCE bit       //low true
   TBufCE bit       //low true
   CRead bit        //low true
   PWrite bit       //low true
   PRead bit     //low true
   TWrite bit       //low true
   RRead bit        //low true
   RxOverflow bit
   TxTimeout bit
   RxInterrupt bit
   QEmpty bit
   Ack bit       //low true
   Resume bit
   CarryIn bit
   DestHigh bit
   DestLow bit 2
   Function bit 3
   Source bit 3
   BReg bit 4
   AReg bit 4
   Branch bit 3
```

```
    Next bit 5          //msb is low true
    blank bit 8
    ]

manifest
    [
    // instruction addresses
    Init1 = 0
    Init2 = 1
    Init3 = 2
    RxEnd1 = 3
    RxEnd2 = 4
    RxEnd3 = 5
    RxEnd4 = 6
    RxReady1 = 7
    RxReady2 = 10b
    PortReadReq1 = 11b
    PortReadReq2 = 12b
    PortWriteReq1 = 13b
    PortStart = 20b
    PortStart1 = 14b
    PortStart2 = 15b
    PortStart3 = 21b
    PortStart4 = 16b
    TxStart = 17b
    TxAbort1 = 22b
    TxTimer = 23b
    TxTimer1 = 24b
    TxTimer2 = 25b
    TxTimer3 = 26b
    TxTimer4 = 27b

    // Startup addresses
    RxReady = 30b
    RxEnd = 31b
    TxReady = 32b
    TxAbort = 33b
    PortWriteReq = 34b
    PortReadReq = 35b
    Init = 36b
    Idle = 37b

    // Register names
    spare = 0
    rBase = 1
    rGet = 2
    rPut = 3
    count = 4
    tBase = 5
    tGet = 6
    tPut = 7
    retry = 8
```

```
timer = 9
random = 10

// Branch Condition Codes (CC)
Never = 0
NonZero = 1
Zero = 2
NoCarry8 = 3
Positive = 4
Negative = 5
Equal = 6
Always = 7

// 2901 Functions
RplusS = 0
SminusR = 1
RminusS = 2
RorS = 3
RandS = 4
NotRandS = 5
RxorS = 6
RxnorS = 7

// 2901 Sources
AQ = 0
AB = 1
ZQ = 2
ZB = 3
ZA = 4
DA = 5
DQ = 6
DZ = 7

// 2901 Destinations
QReg = 0
Nop = 1
RamA = 2
RamF = 3
RamQD = 4
RamD = 5
RamQU = 6
RamU = 7
]

let Next, Branch = 0, Never
let CarryIn, Function, Source = nil, nil, nil
let AReg, BReg, Destination = nil, nil, nil
let Resume, Ack, QEmpty = false, false, false
let RxInterrupt, TxTimeout, RxOverflow = false, false, false
let RRead, TWrite, PRead, PWrite, CRead = false, false, false, false, false
let TBufCE, RBufCE, BufWE = false, false, false
```

```
switchon addr<<Addr.Instr into
  [
  case Init:      //tGet ← -1
    [
    CarryIn = low; Function = RxnorS; Source = AB
    AReg = tGet; BReg = tGet; Destination = RamF
    Next = Init1
    endcase
    ]
  case Init1:       //tPut ← 0
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = spare; BReg = tPut; Destination = RamF
    Next = Init2
    endcase
    ]
  case Init2:       //rGet ← 0
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = spare; BReg = rGet; Destination = RamF
    Next = Init3
    endcase
    ]
  case Init3:       //rPut ← 0; Goto(RxEnd1)
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = spare; BReg = rPut; Destination = RamF
    Next = RxEnd1
    endcase
    ]

  case RxEnd:      //Test(rPut-rGet) mod 2↑11; SetRxOverflow(EQ);
Return(EQ); Ack
    [
    CarryIn = low; Function = RminusS; Source = AB
    AReg = rPut; BReg = rGet; Destination = Nop
    RxOverflow, Ack = true, true
    Branch = Equal
    Next = RxEnd1
    endcase
    ]
  case RxEnd1:        //Latch ← Count; Count ← 0
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = count; BReg = count; Destination = RamA
    Next = RxEnd2
    endcase
    ]
  case RxEnd2:        //RxBuf[rBase] ← Latch
    [
    CarryIn = low; Function = RorS; Source = ZB
    AReg = spare; BReg = rBase; Destination = Nop
```

```
    RBufCE, BufWE, CRead = true, true, true
    Next = RxEnd3
    endcase
    ]
  case RxEnd3:        //rBase ← rPut; RxBuf[rPut] ← Latch; QEmpty
    [
    CarryIn = low; Function = RorS; Source = ZA
    AReg = rPut; BReg = rBase; Destination = RamF
    RBufCE, BufWE, CRead = true, true, true
    QEmpty = true
    Next = RxEnd4
    endcase
    ]
  case RxEnd4:        //rPut ← rPut+1; Return
    [
    CarryIn = high; Function = RplusS; Source = ZB
    AReg = spare; BReg = rPut; Destination = RamF
    Branch = Always
    endcase
    ]

  case RxReady:   //Test(rPut-rGet) mod 2↑11; SetRxOverflow(EQ);
Return(EQ); Ack
    [
    CarryIn = low; Function = RminusS; Source = AB
    AReg = rPut; BReg = rGet; Destination = Nop
    RxOverflow, Ack = true, true
    Branch = Equal
    Next = RxReady1
    endcase
    ]
  case RxReady1:  //count ← count+1
    [
    CarryIn = high; Function = RplusS; Source = ZB
    AReg = spare; BReg = count; Destination = RamF
    Next = RxReady2
    endcase
    ]
  case RxReady2:  //RxBuf[rPut] ← Rx; rPut ← rPut+1; Return
    [
    CarryIn = high; Function = RplusS; Source = ZA
    AReg = rPut; BReg = rPut; Destination = RamA
    RBufCE, BufWE, RRead = true, true, true
    Branch = Always
    endcase
    ]

  case PortReadReq:  //Port ← RxBuf[rGet]
    [
    CarryIn = low; Function = RorS; Source = ZB
    AReg = spare; BReg = rGet; Destination = Nop
    RBufCE, PWrite = true, true
```

```
    Next = PortReadReq1
    endcase
    ]
  case PortReadReq1: //Test(rGet-Rbase) mod 2↑11; ClearRxInterrupt(EQ);
Return(EQ)
    [
    CarryIn = low; Function = RminusS; Source = AB
    AReg = rGet; BReg = rBase; Destination = Nop
    RxInterrupt = true
    Branch = Equal
    Next = PortReadReq2
    endcase
    ]
  case PortReadReq2: //rGet ← rGet+1; Goto(Idle)
    [
    CarryIn = high; Function = RplusS; Source = ZB
    AReg = spare; BReg = rGet; Destination = RamF
    Next = Idle
    endcase
    ]

  case PortWriteReq: //Test(tPut); TxBuf[tPut] ← Port; Return(Z);
Resume(PortStart)
    [
    CarryIn = low; Function = RorS; Source = ZB
    AReg = PortStart; BReg = tPut; Destination = Nop
    TBufCE, BufWE, PRead = true, true, true
    Resume = true
    Branch = Zero
    Next = PortWriteReq1
    endcase
    ]
  case PortWriteReq1:    //tPut ← tPut-1; Return(NZ); Goto(TxStart);
Resume(PortStart3)
    [
    CarryIn = low; Function = SminusR; Source = ZB
    AReg = PortStart3; BReg = tPut; Destination = RamF
    Resume = true
    Branch = NonZero
    Next = TxStart
    endcase
    ]

  case PortStart:    //tBase ← DataBus
    [
    CarryIn = low; Function = RorS; Source = DZ
    AReg = spare; BReg = tBase; Destination = RamF
    Next = PortStart1
    endcase
    ]
  case PortStart1:  //tPut ← tBase
    [
```

```
    CarryIn = low; Function = RorS; Source = ZA
    AReg = tBase; BReg = tPut; Destination = RamF
    Next = PortStart2
    endcase
    ]
  case PortStart2:   //mask ← 0  (mask is in Q register)
    [
    CarryIn = low; Function = RandS; Source = ZQ
    AReg = spare; BReg = spare; Destination = QReg
    Next = PortStart3
    endcase
    ]
  case PortStart3:   //retry ← 0
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = spare; BReg = retry; Destination = RamF
    Next = PortStart4
    endcase
    ]
  case PortStart4:   //timer ← 0; Return
    [
    CarryIn = low; Function = RandS; Source = ZB
    AReg = spare; BReg = timer; Destination = RamF
    Branch = Always
    endcase
    ]

  case TxStart:  //tGet ← tBase; Goto(TxReady)
    [
    CarryIn = low; Function = RorS; Source = ZA
    AReg = tBase; BReg = tGet; Destination = RamF
    Next = TxReady
    endcase
    ]

  case TxReady:    //Tx ← TxBuf[tGet]; tGet ← tGet-1; Ack; Goto(Idle)
    [
    CarryIn = low; Function = SminusR; Source = ZA
    AReg = tGet; BReg = tGet; Destination = RamA
    TBufCE, TWrite = true, true
    Ack = true
    Next = Idle
    endcase
    ]

  case TxAbort:    //mask ← ShiftLeft(mask); Ack
    [
    CarryIn = low; Function = RorS; Source = ZQ
    AReg = spare; BReg = spare; Destination = RamQU
    Ack = true
    Next = TxAbort1
    endcase
```

```
    ]
  case TxAbort1:   //retry ← random & mask; Return(NZ); Goto(TxStart)
    [
    CarryIn = low; Function = RandS; Source = AQ
    AReg = random; BReg = retry; Destination = RamF
    Branch = NonZero
    Next = TxStart
    endcase
    ]

  case Idle:      //random ← random+1; Return(NCY8); Goto(TxTimer)
    [
    CarryIn = high; Function = RplusS; Source = ZB
    AReg = spare; BReg = random; Destination = RamF
    Branch = NoCarry8
    Next = TxTimer
    endcase
    ]

  case TxTimer:    //Test(tGet); Return(Neg)
    [
    CarryIn = low; Function = RorS; Source = ZB
    AReg = spare; BReg = tGet; Destination = Nop
    Branch = Negative
    Next = TxTimer1
    endcase
    ]
  case TxTimer1:   //timer ← timer-1; Return(Z); SetTxTimeout(Z);
Resume(TxTimer4)
    [
    CarryIn = low; Function = SminusR; Source = ZB
    AReg = TxTimer4; BReg = timer; Destination = RamF
    Resume, TxTimeout = true, true
    Branch = Zero
    Next = TxTimer2
    endcase
    ]
  case TxTimer2:   //Test(retry); Return(Z)
    [
    CarryIn = low; Function = RorS; Source = ZB
    AReg = spare; BReg = retry; Destination = Nop
    Branch = Zero
    Next = TxTimer3
    endcase
    ]
  case TxTimer3:   //Retry ← Retry-1; Return(NZ); Goto(TxStart)
    [
    CarryIn = low; Function = SminusR; Source = ZB
    AReg = spare; BReg = retry; Destination = RamF
    Branch = NonZero
    Next = TxStart
    endcase
```

```
    ]
  case TxTimer4:   //tGet ← -1; Return
    [
    CarryIn = low; Function = RxnorS; Source = AB
    AReg = tGet; BReg = tGet; Destination = RamF
    Branch = Always
    endcase
    ]
  ]

data>>Data.BufWE = BufWE? high, low
data>>Data.RBufCE = RBufCE? low, high
data>>Data.TBufCE = TBufCE? low, high
data>>Data.CRead = CRead? low, high
data>>Data.PWrite = PWrite? low, high
data>>Data.PRead = PRead? low, high
data>>Data.TWrite = TWrite? low, high
data>>Data.RRead = RRead? low, high
data>>Data.RxOverflow = RxOverflow? high, low
data>>Data.TxTimeout = TxTimeout? high, low
data>>Data.RxInterrupt = RxInterrupt? high, low
data>>Data.QEmpty = QEmpty? high, low
data>>Data.Ack = Ack? low, high
data>>Data.Resume = Resume? high, low
data>>Data.CarryIn = CarryIn
data>>Data.DestHigh = Destination rshift 2
data>>Data.DestLow = Destination
data>>Data.Function = Function
data>>Data.Source = Source
data>>Data.BReg = BReg
data>>Data.AReg = AReg
data>>Data.Branch = Branch
data>>Data.Next = Next xor 20b
]
```

```
begin "epd"
 require "prom.sai" sourcelfile;
 $256;

 define

 data0  =[a0], data1  =[a1], data2  =[a2], data3  =[a3],
 state0 =[a4], state1 =[a5], state2 =[a6], state3 =[a7],

 d(x3,x2,x1,x0)   =[((data0 div d0 = x0) ∧ (data1 div d1 = x1)
       ∧ (data2 div d2 = x2) ∧ (data3 div d3 = x3))],
 onetransition  =[(d(0,0,0,1) ∨ d(0,0,1,1) ∨ d(1,0,0,1))],
 zerotransition   =[(d(0,1,1,0) ∨ d(1,1,0,0) ∨ d(1,1,1,0))],
 notransition   =[(d(0,0,0,0) ∨ d(1,0,0,0) ∨ d(0,1,1,1) ∨
 d(1,1,1,1))],
 idletransition   =[(d(0,0,0,0))],
 goodtransition   =[(onetransition ∨ zerotransition)],
 badtransition  =[(¬goodtransition ∧ ¬notransition)],  comment all
 others;
 _85_transition   =[(data0 ∧ data1 ∨ ¬data0 ∧ ¬data1)],  comment in
 sync with 85;

 state     =[((state0 + state1 + state2 + state3) div d4)],
 active    =[(state ~ 0)],
 duration  =[(if _85_transition then state else (state+1))],

 idle      =[(¬active ∧ idletransition)],
 startbit  =[(¬active ∧ onetransition)],
 lostsync  =[(¬active ∧ ¬(idletransition ∨ onetransition))],
 toomany     =[(active ∧ badtransition)],
 setup     =[(active ∧ goodtransition ∧ (2≤duration≤5))],
 datatrans   =[(active ∧ goodtransition ∧ (6≤duration≤10))],
 toofew    =[(active ∧ (goodtransition ∨ badtransition) ∧
 (11≤duration≤15))],
 timeout     =[(active ∧ notransition ∧ (13≤state≤15))],
 jam    =[(timeout ∧ data0)],
 eop    =[(timeout ∧ ¬data0)],

 data_zero   =[(zerotransition ∧ datatrans)],
 data_one  =[((onetransition ∧ datatrans) ∨ startbit)],
 collision   =[(lostsync ∨ jam ∨ toomany ∨ toofew)],
 start     =[(startbit ∨ lostsync ∨ jam ∨ datatrans ∨ toofew)],
 carrier     =[(nextstate ~ 0)],
 data      =[(collision ∨ data_one)],
 shift     =[(data_zero ∨ data_one)],
 nextstate   =[(if (idle ∨ eop) then 0
       else if jam then 15
       else if (start ∧ ¬_85_transition) then 1
       else if (start ∧ _85_transition) then 2
       else (state+2))];
 prombegin
```

```
prom(0,d0,   carrier);
prom(0,d1,   data);
prom(0,d2,   shift);
prom(0,d3,   collision);
prom(0,d4,   nextstate land d0);
prom(0,d5,   nextstate land d1);
prom(0,d6,   nextstate land d2);
prom(0,d7,   nextstate land d3);

promend;
writeprom("epd",0);
end;
```

```
begin "erx"
 require "prom.sai" sourcefile;
 $256;

 define

 carrier      =[a0],
 data       =[a1],
 shift      =[a2],
 word       =[a3],
 adrs       =[a4],
 enable     =[a5],
 state0     =[a6],
 state1     =[a7],

 init       =[(¬enable)],
 state      =[((state1 + state0) div d6)],
 idle       =[(state=0)],
 first_word   =[(state=1)],
 other_words  =[(state=2)],
 flush      =[(state=3)],
 event      =[((shift + data) div d1)],
 nil     =[(event=0)],
 collision    =[(event=1)],
 d_zero     =[(event=2)],
 d_one      =[(event=3)],
 datatr     =[(carrier ∧ (d_zero ∨ d_one ∨ nil))],
 visible      =[(other_words ∧ ((¬carrier ∧ ¬word) ∨
 (carrier ∧ collision)))],
 invisible    =[(first_word ∧ ((¬carrier) ∨ (carrier ∧
 collision) ∨
        (datatr ∧ word ∧ ¬adrs)))],
 end_idle   =[(idle ∧ carrier ∧ ¬word)],
 lostsync   =[(idle ∧ carrier ∧ collision)],
 write      =[(¬init ∧ ((first_word ∧ datatr ∧ word ∧ adrs) ∨
      (other_words ∧ datatr ∧ word)))],
 endbit     =[(¬init ∧ (visible ∨ (other_words ∧ ¬carrier ∧
 word)))],
 abort      =[(visible)],
 clear      =[(init ∨ idle ∧ ¬carrier)],
 crcclr     =[(init ∨ flush ∧ ¬carrier)],
 fce     =[(init ∨ first_word ∧ carrier ∧ (d_zero ∨
 d_one))],

 nextstate    =[(if init then 3 else
      if (       ! idle;
      (idle ∧ ¬carrier) ∨
      (idle ∧ carrier ∧ ¬(collision ∨ end_idle)) ∨
      (flush ∧ ¬carrier)
      ) then 0 else
      if (     ! first_word;
      (first_word ∧ datatr ∧ ¬word) ∨
```

```
      (end_idle)
      ) then 1 else
      if (    ! other_words;
      (first_word ∧ datatr ∧ word ∧ adrs) ∨
      (other_words ∧ datatr)
      ) then 2 else
      if (    ! flush;
      (flush ∧ carrier) ∨
      (lostsync) ∨
      (visible) ∨
      (invisible) ∨
      (other_words ∧ ¬carrier ∧ word)
      ) then 3 else
      error(cvs($$adrs)&": didn't assign any state!")
      )];

prombegin

prom(0,d0,  write);
prom(0,d1,  endbit);
prom(0,d2,  ¬abort);
prom(0,d3,  ¬clear);
prom(0,d4,  crcclr);
prom(0,d5,  ¬fce);
prom(0,d6,  nextstate land d0);
prom(0,d7,  nextstate land d1);

promend;
writeprom("erx",0);
end;
```

```
begin "etx"
 require "prom.sai" sourcelfile;
 $256;

 define

 carrier      =[a0],
 jam     =[a1],
 word       =[a2],
 ready      =[a3],
 inhibit       =[a4],
 timeout       =[a5],
 state0     =[a6],
 state1     =[a7],

 state      =[((state1 + state0) div d6)],
 idle       =[(state=0)],
 idlebit       =[(nextstate=0)],
 send       =[(state=1)],
 sendcrc       =[(state=2)],
 go      =[((send v sendcrc) ∧ ¬jam)],
 reload     =[(send ∧ ready ∧ ¬inhibit ∧ ¬jam ∧ word)],
 start      =[(idle ∧ ready ∧ ¬inhibit ∧ ¬carrier)],
 nextstate    =[(if (state=3) then 0     comment unused
 state;
      else if (       ! idle;
      timeout v
      jam v
      (idle ∧ ¬start) v
      (send ∧ word ∧ ¬ready) v   comment abort if data
 underflow;
      (sendcrc ∧ word)    comment return to idle;
      ) then 0 else
      if (     ! send;
      (start) v
      (reload) v
      (send ∧ ¬word)
      ) then 1 else
      if (     ! sendcrc;
      (send ∧ word ∧ inhibit) v     comment all data has
 been sent;
      (sendcrc ∧ ¬word)
      ) then 2 else
      error(cvs($$adrs)&": didn't assign any state!")
      )];

 prombegin

 prom(0,d0,   go);
 prom(0,d1,   ¬go);
 prom(0,d2,   reload);
 prom(0,d3,   0);
```

```
prom(0,d4,  idlebit);
prom(0,d5,  ¬idlebit);
prom(0,d6,  nextstate land d0);
prom(0,d7,  nextstate land d1);

promend;
writeprom("etx",0);
end;
```