DEFINITION OF 8086 PORTS
June 5, 1979

IOP PORTS

Address	R/W	Bits	Description
0002	R/W	8-15	Interrupt Control Register
		8	Select 60 Hz Interrupt
		9	Select KeyBoard Interrupt
		10	Select A/D Converter Interrupt
		11	Select 30 Hz Display Interrupt
		12	Select EIA Interrupt
		13	Select Disk Controller Interrupt
		14	Select System Interrupt
		15	Select Main Memory Parity Interrupt
0020	W	8-15	Processor Control Register
		8	Boot Sequence Done
		9	Processor Lock
		10	Battery Charger On
		11	Disable ROM(Enable Main Memory)
		12	Correction Off & CR4 Off(msb)
		13	CR3 Off
		14	CR2 Off
		15	CR1 Off(lsb)
0042	R	8-15	Read KeyBoard Data
0044	R	12-15	Read KeyBoard/FIFO Status
		12	FIFO Out Ready
		13	FIFO In Ready
		14	Data Received
		15	Data Sent
0048	W	8-15	UART←KBD Control Register
004A	W	8-15	UART←KBD Data(Turn KBD On)
004C	W		KBD Data Reset
004E	W		KBD Chip Reset
0060	W	0	Set D/A FIFO Sample & Hold
		1	Select D/A Sample & Hold Channel A
		2	Select D/A Sample & Hold Channel B
		3	Select D/A FIFO Frequency 0
		4	Select D/A FIFO Frequency 1
		5	Select D/A FIFO Frequency 2
		6	Tablet X On
		7	Tablet Y On

Address	R/W	Bits	Description
00A0	W	8-15	DataBus to PPI Interface PortA
00A0	R	8-15	PPI Interface PortA to DataBus
00A2	W	8-15	DataBus to PPI Interface PortB
00A2	R	8-15	PPI Interface PortB to DataBus
00A4	W	8-15	DataBus to PPI Interface PortC
00A4	R	8-15	PPI Interface PortC to DataBus
		8	Bit Set/Reset Flag(0=active)
		9-11	Dont Care
		12-14	Bit Select(0-7)
		15	Bit Set/Reset(0=reset;1=set)
00A6	W	8-15	Load PPI Control Register with Mode Def.
		8	Mode Set Flag(1=active)
		9-10	Group A-Mode Selection 00=Mode 0;01=Mode 1;1x=Mode 2
		11	Group A-Port A(0=output;1=input)
		12	Group A-Port C-Upper(0=output;1=input)
		13	Group B-Mode Selection 0=Mode 0;1=Mode 1
		14	Group B-Port B(0=output;1=input)
		15	Group B-Port C-Lower(0=output;1=input)
00C0	W	0-11	Load D/A Converter
0100	W		Input/Output Control Register
		0-1	A/D Converter Speed 0=3 KHz 1=4 KHz 2=6 KHz 3=12 KHz
		2	CRT Timing Control(0=stop;1=go)
		3	Disk Master Reset(0=reset)
		4-6	Bit Clock Speed 0=4.5 MHz 1=5.14 MHz 2=6.0 MHz 3=7.2 MHz 4=9.0 MHz 5=12 MHz 6=18 MHz 7=24 MHz
		7-9	A/D Source 0=Tablet X 1=Tablet Y 2=+5 Voltage 3=+12 Voltage 4=Battery Output Voltage 5=External Analog 0 6=External Analog 1 7=External Analog 2
		10	Select Drive 0(1=select)
		11	Select Drive 1(1=select)
		12	Select Drive 2(1=select)
		13	Select Side(0=side 0;1=side 1)
		14	+5 Voltage Control(0=off;1=on)
		15	+12 Voltage Control(0=off;1=on)

Address	R/W	Bits	Description
0120	W	8-15	Disk Command Register(low true logic)
		0X	Restore(type 1)
		1X	Seek(type 1)
		2X	Step(type 1)
		4X-5X	Step In(type 1)
		6X-7X	Step Out(type 1)
		8X-9X	Read Command(type 2)
		AX-BX	Write Command(type 2)
		C4	Read Address(type 2)
		DF	Force Interrupt(type 4)
		E4-E5	Read Track(type 3)
		F4	Write Track(type 3)
	R	8-15	Read Disk Status(low true logic)
		8	Disk Not Ready
		9	Write Protected
		10	Head Loaded(type 1 commands)
			Write Fault(write commands)
		11	Seek Error
		12	CRC Error
		13	Track 0(type 1 commands)
			Lost Data(type 2 & 3 commands)
		14	Index(type 1 commands)
			DR Full(read commands)
			DR Empty(write commands)
0122	R/W	8-15	Disk Track(0 to 34[22H])(low true logic)
0124	R/W	8-15	Disk Sector(1 to 9)(low true logic)
0126	R/W	8-15	Data Register(low true logic)
0140	W	8-15	Load CRT Control Register 0
0142	W	8-15	Load CRT Control Register 1
0144	W	8-15	Load CRT Control Register 2
0146	W	8-15	Load CRT Control Register 3
0148	W	8-15	Load CRT Control Register 4
014A	W	8-15	Load CRT Control Register 5
014C	W	8-15	Load CRT Control Register 6
0150	R	8-15	Read CRT Cursor Line Address
0152	R	8-15	Read CRT Cursor Character Address
0154	W		Reset Chip
0156	W		Scroll Up
0158	W	8-15	Load CRT Cursor Character Address
015A	W	8-15	Load CRT Cursor Line Address
015C	W		Start Timing Chain
0160	W	0-15	Load (Display Starting Address)/8
01A0	R	8-15	Read EIA Status
01A2	R	8-15	Read EIA Data
01A8	W	8-15	Load EIA Control Register
01AA	W	8-15	Load EIA Data
01AC	W		Reset EIA Data
01AE	W		Reset EIA Chip
01C0	R	8-15	Read A/D Converter
01E0	W	15	Select CRT(0=internal;1=external)

EP PORTS

Address	R/W	Bits	Description
0800	R/W	0-4	Interrupt Control Register
		0	Select Local Memory Parity Interrupt
		1	Select Main Memory Parity Interrupt
		2	Select System Interrupt
		3	Select 60 Hz Interrupt
		4	Select Illegal Address Interrupt Interrupt on FFFC0 thru FFFDF
1000	R/W	8-15	PPI Interface(Same as 00A0)
2000	W	8-15	Processor Control Register
		8	LED1 Local RAM Parity
		9	LED2
		10	LED3
		11	LED4
		12	LED5 Select ROM
		13	LED6 Select Processor Lock
		14	LED7 Enable Local RAM Parity
		15	LED8 Disable Local RAM
4000	W		Clear Parity on Local RAM

SPECIAL MEMORY LOCATIONS

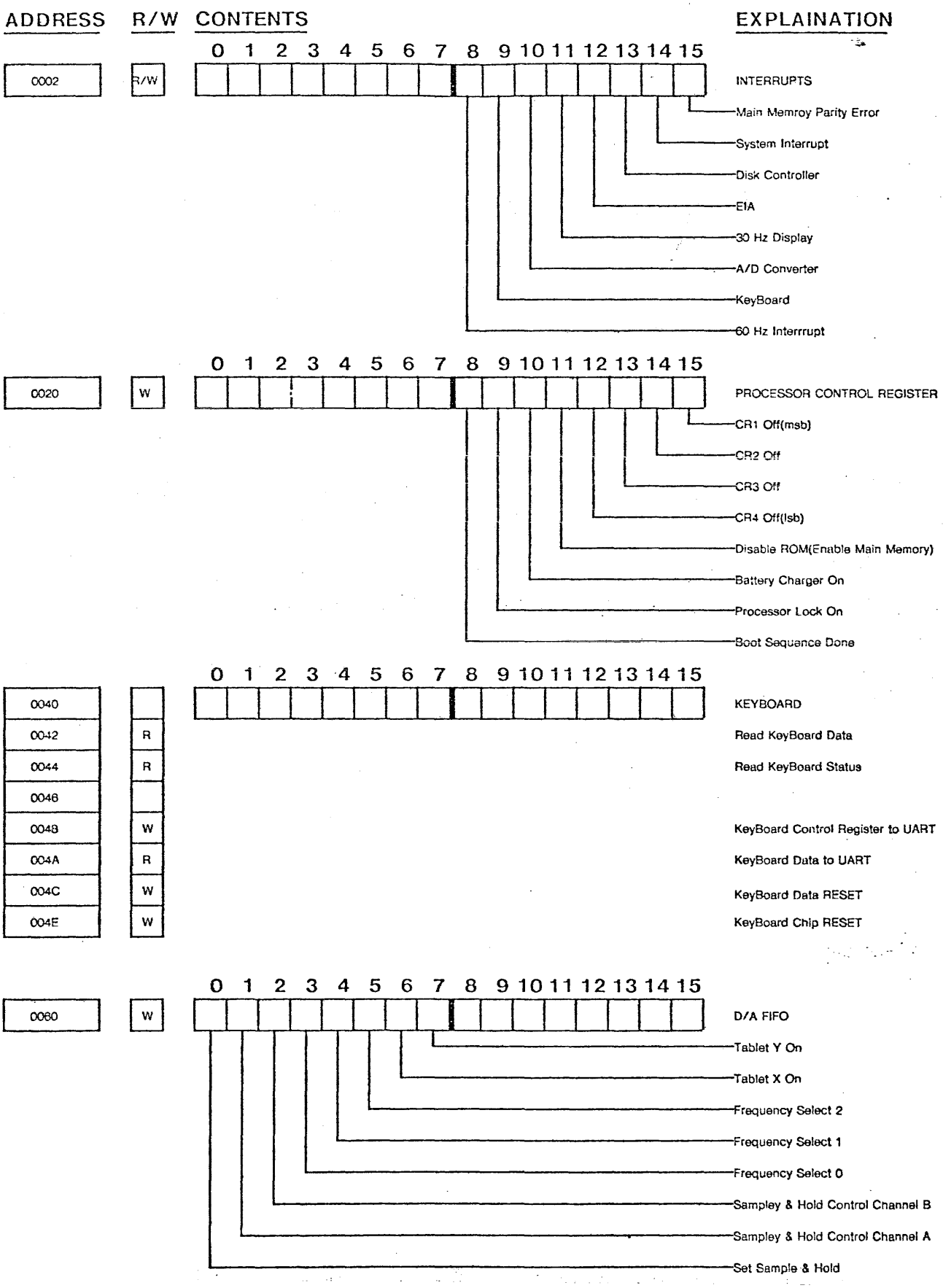
Address	R/W	Bits	Description
FFFEA	W	9	Processor Reset
		10	Processor Boot
		11	Processor Interrupt
		12-15	Processor Address(2=IOP;7=EP)
FFFEC	R	1	Parity Error Report Parity Bit
		2-7	Parity Error Report Syndrome Bits
		8-15	Parity Error Report High Order Address
FFFEE	R	0-15	Parity Error Report Low Order Address

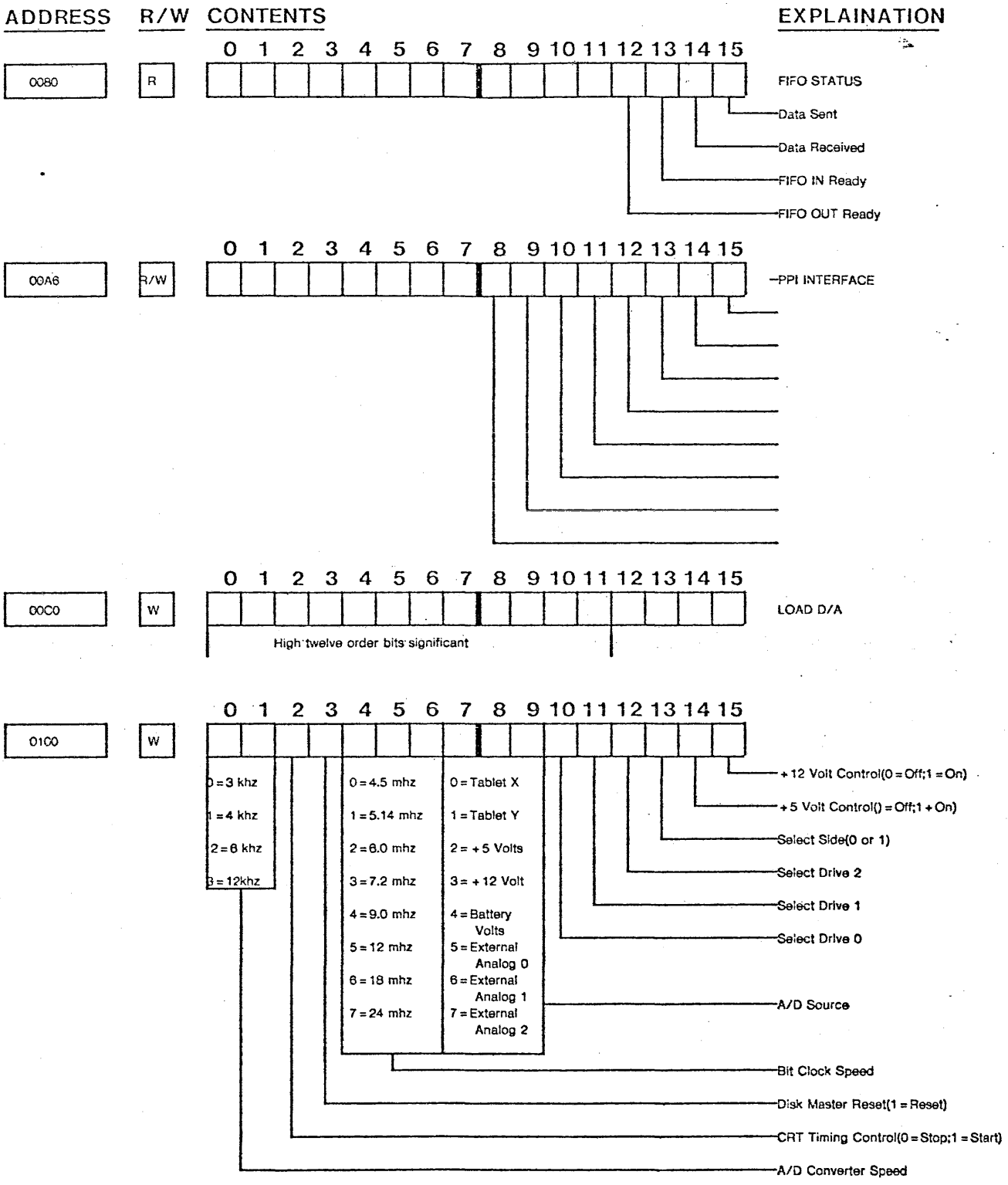
Address	Standard 8086 Interrupt Locations
00000	Divide by 0 Interrupt
00004	Single Step Interrupt
00008	None Masked Interrupt
0000C	Break Point Interrupt
00010	Over Flow Interrupt
00014	INT 05 Interrupt
⋮	
003FC	INT FF Interrupt

Address	IOP Interrupt Locations
00080	Main Memory Parity Interrupt
00084	System Interrupt
00088	Disk Interrupt
0008C	EIA Interrupt
00090	30 Hz (OddInt) Interrupt
00094	A/D Interrupt
00098	KeyBoard Interrupt
0009C	60 Hz Interrupt

Address	EP Interrupt Locations
00080	Local Memeory Parity Interrupt
00084	Main Memory Parity Interrupt
00088	System Interrupt
0008C	60 Hz Interrupt
00090	Illegal Address Interrupt

IOP PORTS


ADDRESS
R/W
CONTENTS
EXPLANATION
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0002
R/W
INTERRUPTS
Main Memroy Parity Error
System Interrupt
Disk Controller
EIA
30 Hz Display
A/D Converter
KeyBoard
60 Hz Interrrupt
0020
W
PROCESSOR CONTROL REGISTER
CR1 Off(msb)
CR2 Off
CR3 Off
CR4 Off(lsb)
Disable ROM(Enable Main Memory)
Battery Charger On
Processor Lock On
Boot Sequence Done
0040
KEYBOARD
0042
R
Read KeyBoard Data
0044
R
Read KeyBoard Status
0046
0048
W
KeyBoard Control Register to UART
004A
R
KeyBoard Data to UART
004C
W
KeyBoard Data RESET
004E
W
KeyBoard Chip RESET
0060
W
D/A FIFO
Tablet Y On
Tablet X On
Frequency Select 2
Frequency Select 1
Frequency Select 0
Sampley & Hold Control Channel B
Sampley & Hold Control Channel A
Set Sample & Hold

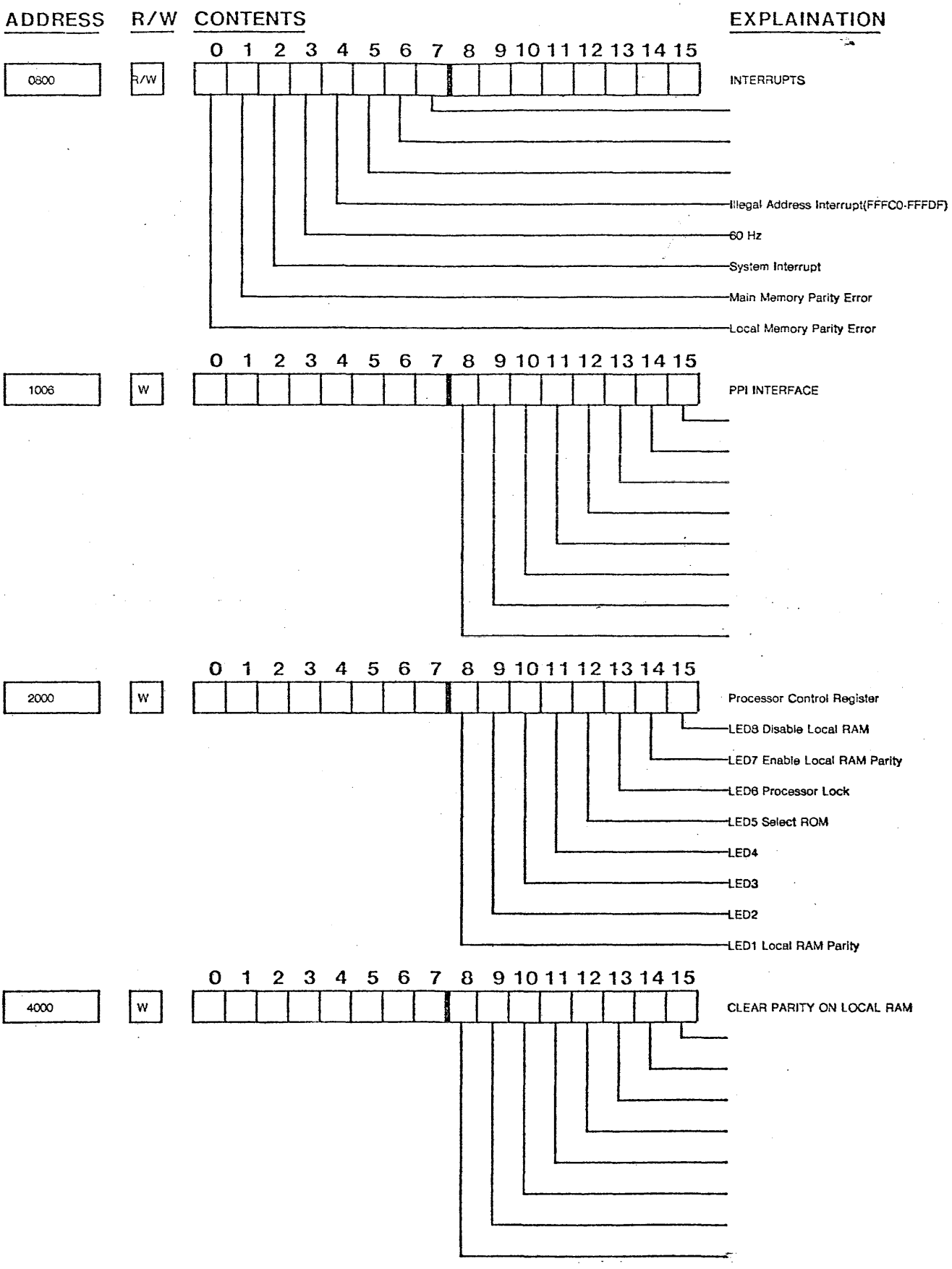

ADDRESS
R/W
CONTENTS
EXPLAINATION
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0080
R
FIFO STATUS
Data Sent
Data Received
FIFO IN Ready
FIFO OUT Ready
00A6
R/W
PPI INTERFACE
00C0
W
LOAD D/A
High twelve order bits significant
01C0
W
0 = 3 khz
1 = 4 khz
2 = 6 khz
3 = 12khz
0 = 4.5 mhz
1 = 5.14 mhz
2 = 6.0 mhz
3 = 7.2 mhz
4 = 9.0 mhz
5 = 12 mhz
6 = 18 mhz
7 = 24 mhz
0 = Tablet X
1 = Tablet Y
2 = +5 Volts
3 = +12 Volt
4 = Battery Volts
5 = External Analog 0
6 = External Analog 1
7 = External Analog 2
+12 Volt Control(0 = Off;1 = On)
+5 Volt Control() = Off;1 + On)
Select Side(0 or 1)
Select Drive 2
Select Drive 1
Select Drive 0
A/D Source
Bit Clock Speed
Disk Master Reset(1 = Reset)
CRT Timing Control(0 = Stop;1 = Start)
A/D Converter Speed

PORT 2

ADDRESS	R/W	CONTENTS	EXPLANATION
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
0120	R/W		DISK INTERFACE
0120	R		Read Status Register
0120	W		Set Command Register
0122	R/W		Track Register(0 to 34[22H])
0124	R/W		Sector Register(0 to 8)
0126	R/W		Data Register
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
0140	R/W		CRT INTERFACE
0140	W		Load Control Register 0
0142	W		Load Control Register 1
0144	W		Load Control Register 2
0146	W		Load Control Register 3
0148	W		Load Control Register 4
014A	W		Load Control Register 5
014C	W		Load Control Register 6
014E	W		Processor Self Load
0150	R		Read Cursor Line Address
0152	R		Read Cursor Charaqcter Address
0154	W		Reset Chip
0156	W		Scroll Up
0158	W		Load Cursor Character Address
015A	W		Load Cursor Line Address
015C	W		Start Timeing Chain
015E	W		Non-Processor Self Load
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
0160	W		Load Display Starting Address 19 Bits(Least Significant 3 Implied 000)
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
01A0	R/W		EIA INTERFACE
01A0	R		Read EIA Status
01A2	R		Read EIA Data
01A4			
01A6			
01A8	W		Load EIA Control Register
01AA	W		Load EIA Data
01AC	W		Reset EIA Data
01AE	W		Reset EIA Chip
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
01Co	R		READ A/D CONVERTER

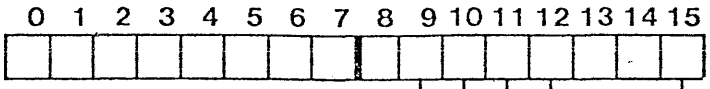
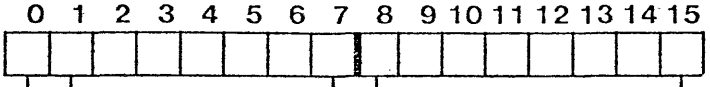
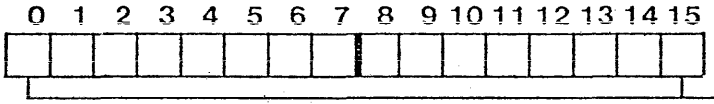
Pg 3

EP PORTS



Port 4

SPECIAL MEMORY LOCATIONS

ADDRESS	R/W	CONTENTS	EXPLANATION
FFFEA	W		SYSTEM CONTROL REGISTER
			Porcessor Address(2 = IOP; 7 = EP)
			Processor Interrupt
			Processor Boot
			Processor Reset
FFFEC	R		MAIN MEMORY PARITY REPORT
			High Order Address
			Syndrome Bits
			Parity Bit
FFFEE	R		MAIN MEMORY PARITY REPORT
			Low Order Address

00000	Divide By Zero	8086 INTERRUPTS
00004	Single Step Interrupt	
00008	Non Masked Interrupt(NMI)	
0000C	Break Point Interrupt	
00010	OverFlow Interrupt	
00014-003FC	INT05 - INTFF Interrupts	

00080	Main Memory Parity	8259 IOP INTERRUPTS
00084	System Interrupt	
00088	Disk Interrupt	
0008C	EIA Interrupt	
00090	30 Hz Interrupt	
00094	A/D Converter Interrupt	
00098	Key Board Interrupt	
0009C	60 Hz Interrupt	

00080	Local Memory Parity Interrupt	8259 EP INTERRUPTS
00084	Main Memory Parity Interrupt	
00088	System Interrupt	
0008C	60 Hz Interrupt	
00090	Illegal Address Interrupt	