CodeICE Emulator

for Intel i960® RP Microprocessor

Highlights

- Powerful multi-windowed MWX-ICE C/C++ debugger interface runs on Sun4, HP 9000/700, and PC hosts
- integrated interactive kernel support option for VxWorks™
- Intuitive CPU Browser™ interface to fully configure, visualize, and change internal 960 RP register states (MBCR, BPCON, PMCONs, etc.)
- Performance Plus tools provide:
  - Convenient profiling and code coverage support for Intel's optimizing compilers
  - Performance analysis for profiling real-time execution of unlimited system functions
- Unique Source-Level Trace capability automatically correlates execution history with source code
- Seamless networking support for workstations and PCs
- Real-time trace with timestamp captures 224 bits x 32K frames of information at full speed with cache enabled
- IDP mode services target interrupts while the emulator is paused
- Diagnostic functions, and scope loops help verify hardware design and diagnose problems
- 26 hardware access, 2 hardware execution breakpoints and virtually unlimited software breakpoints
- Flexible, powerful event system is easily configured to detect even the most isolated real-time system events
- Specific PCI support:
  - Low-level (clock-by-clock) PCI bus trace and event system
  - High-level display of PCI bus activity
  - Flexible, powerful event system triggered by PCI bus events
  - CPU Browser™ configuration of PCI registers

Companion Products

- CodeTEST™ embedded software verification tools for the 960 RP offer developers and testers comprehensive software performance analysis, code coverage analysis, memory allocation analysis and software trace

Applied Microsystems Corporation

CodeICE for 80960 RP—Serious speed puts the fun back in embedded development.

Tick, tick, tick . . .

Faster servers, better networking, cheaper add-in cards. Develop the products quicker. And do it for less. You face this kind of pressure every day, but now Applied Microsystems gives you some breathing room. The new CodeICE emulator for 960 RP is designed to accelerate development over the entire life cycle of your project. And CodeICE uses the latest in innovative emulation technology to give you a rich feature set and keep your costs down at the same time.

Beat the Clock

CodeICE 960 RP turns what used to take too much time and effort into just one more milestone you can check off. Features that help make your job easier include the new, graphical CPU Browser™ register configuration interface, a self-configuring performance optimization tool set, Applied's unique Source-Level Trace capability, and integrated RTOS support.

The intuitive MWX-ICE debugger interface makes it easy to organize your approach to development for the way you work best. The graphical debugger offers point-and-click access to even the most powerful emulator features. It also features seamless integration with a graphical source explorer, editors, language tools and configuration management tools. With tools this powerful and this easy to use, you have a development environment that can really stop the clock.

We also offer tools to support these Intel products:
80960 CA/CF/Jx/Hx; 80C186/188 XL, EA, EB, EC; 80L186/188 XL, EA, EB, EC; 80286; 80386 SX/DX; 386EX

A Winning Combination

Meeting today's aggressive schedules and budgets takes affordable tools that offer both robust power and ease of use. CodeICE emulators represent a new approach to emulator technology that meets each of these equirements.

Just for RP

Each CodeICE emulator is engineered for a single processor architecture. This processor-specific design makes it possible to reduce the number of components needed to build an emulator, yet significantly increase feature breadth and depth and achieve unmatched precision. As a result, the CodeICE emulator for 960 RP delivers affordable no-compromise performance—such as a PCI bus trace and event system integrated with the i960 trace and event system.

Power You Can Use

CodeICE features are designed to help you work more quickly and easily. Debugging embedded designs can actually be fun with tools like the CPU Browser graphical register configuration interface and interactive RTOS support. And with the intuitive MWX-ICE debugger interface you may even be home in time for dinner.

What's more, as the chart below shows, you can use the power of the emulator over the entire development cycle, which makes CodeICE an even better investment. Each team member, from software and hardware engineers to manufacturing and support technicians, can get information about your product they can't get as easily—or at all—with any other tool. And because each CodeICE can be installed on your workstation or PC network as its own node, everyone can have seamless access to the emulator.

Graphical Debugging Speeds Development

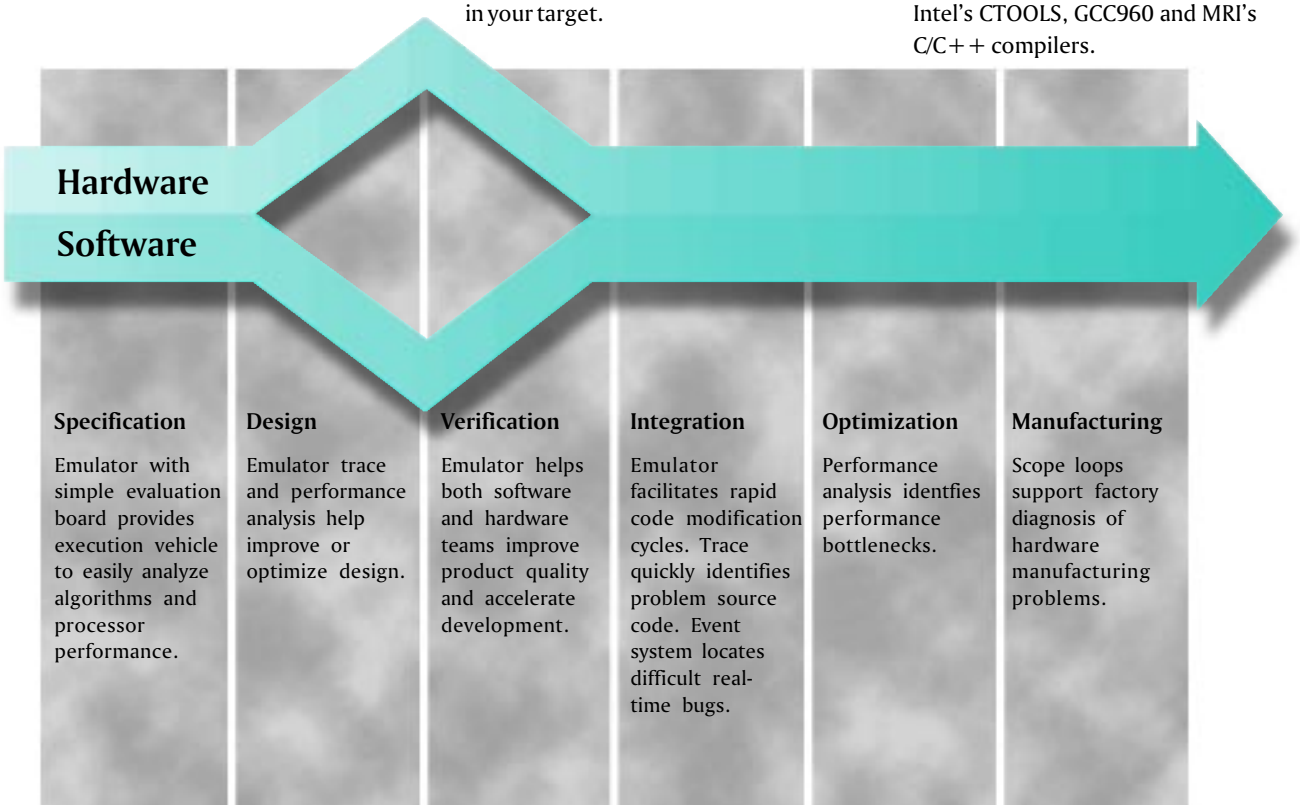
MWX-ICE is a function-rich C/C++, source- and assembly-level debugger. Available for PC , Sun4, or HP hosts, MWX-ICE gives you quick and easy visibility and control of code execution in your target.

This intuitive debugger combines a point-and-click windowed interface, extensive macro capabilities, and a comprehensive hypertext on-line help system with Applied's specially engineered support for all the features of the CodeICE emulator for 80960 RP. It gives you simple, straightforward control of your target and the emulator, whether you prefer to work with a mouse or from the command line.

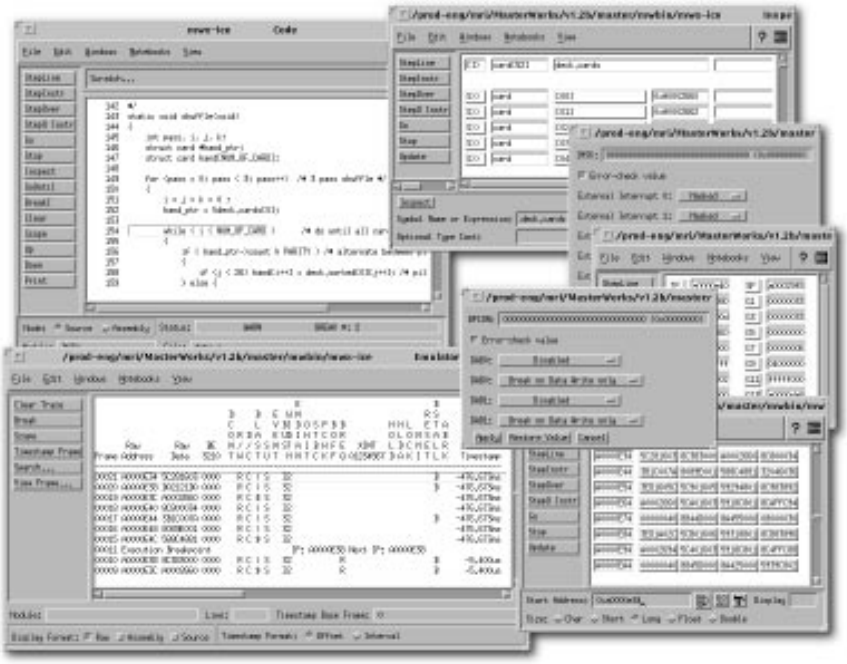
With the notebook feature, you don't have to remember debugger command language. Instead, you can build even complex command sequences just by pointing and clicking. And the context-sensitive hypertext help system means you don't waste time hunting through manuals.

The multi-windowed graphical interface lets you visually organize your debug environment for a more natural approach. For example, you can display source code with corresponding assembly language in separate windows to clarify the relationship between them and verify compiler performance.

MWX-ICE accepts executables from popular tool chains, including Intel's CTOOLS, GCC960 and MRI's C/C++ compilers.



The utility of the CodeICE emulator spans the entire development cycle.



The multi-windowed debugger speeds development with simultaneous display including (clockwise from upper left): source code, symbolic representation of structure elements, register values, stack values, call tracing, CPU Browser register-configuration utility, memory, and interleaved trace.

Source Level Trace Simplifies Debugging

To see what's really going on in your target, you need to see the relationship between source code and the processor instructions that execute in the target. With Applied's unique Source-Level Trace capability, correlating execution history to source code has never been easier.

When viewing trace at source-level, you can also display the associated source modules and line numbers for quick and easy reference. For complete capture of execution history, the Trace system provides 224 bits of information about each cycle to a depth of 32K frames. Register tracking, a pioneering technology in CodeICE emulators, records the state of processor registers during execution and aligns data movement to executed instructions. This unique capability helps boost productivity by providing accurate information about internal processor operations.

Trace With Cache Enabled

To debug code that makes the most of heavily cached processors, such as the RP, you need a means of seeing the instructions that were executed out of cache. Applied's trace system not only does that, but also disassembles cached instructions. You can then display them at source level, assembly level, bus/clock cycle level, or in mixed levels.

Easy Breakpoints

With the Scope feature, you don't need to search back and forth among source modules to determine where to set breakpoints or to find the source code corresponding to your current trace. Choosing the Scope button brings the current line of trace into scope for both symbol accesses and the source window. Then, to set a breakpoint in your application at the highlighted line of trace, simply choose the Break button.

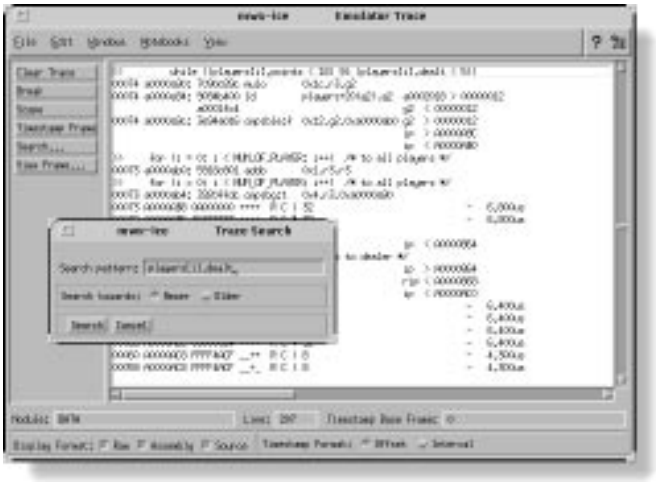
And when you need to locate a particular text string in the trace buffer, a menu-driven search capability finds any text, whether it's data, an address, or even a function name.

Event Systems Pinpoint Problems

The CodeICE emulator is tailored for the 80960 RP with two complete event systems. One monitors core bus activity; the other monitors PCI bus activity using an optional PCI bus probe. For example, you can configure the systems so that a particular 80860 core memory access will turn Trace ON and another special PCI transaction will turn Trace OFF.

The event systems let you readily determine the execution trail of your code without having to modify it with printf statements or semaphores. The systems can be used to qualify trace so you can capture the specific context of a problem, not just the effect. And you can quickly and transparently place breakpoints anywhere, even for functions executed out of cache.

It's easy to configure the event systems using familiar names and



Source-level trace reveals relationships between source code and processor instructions.

symbolic references. The systems support a variety of qualifications in any combination. The When Event / Then Action statement format is both simple to understand and powerful. The full complement of event system actions furnishes a complete tool kit for isolating problems. Available actions include stop emulation, turn-on trace, turn-off trace, change state or group, increment counters, and generate an external trigger for operations such as synching an oscilloscope. The Logic State Analysis Probe option allows you to bring an additional 16 external signals in from your target to further qualify events.

In most targets, when you're using breakpoints to help pin down a problem you can't always afford to stop your application's whole world when you hit a breakpoint. The target still needs to service interrupts driven from other tasks while you determine where to set your next breakpoint. That's why the CodeICE emulator provides a capability called Interrupts During Pause (IDP). When this feature is enabled, the emulator services interrupts even when you have suspended emulation.

RTOS Support Offers System-Level Visualization

CodeICE engineers work closely with industry-leading commercial kernel developers to provide comprehensive support packages for Real-Time Operating Systems (RTOS). RTOS visibility at the CodeICE level shows how the target, application, and RTOS interact with one another during execution in a thoroughly integrated, real-time environment.

Several broad categories of support are provided, including: real-time trace of RTOS activity, display of individual task context and other system structures, task-qualified breakpoints, task stack overflow detection, and task profiling support. The benefit of integrated RTOS support is a substantial reduction in the time required to debug and optimize your application as it runs in your target.

RTOS support reveals target, application, and RTOS interaction.

CPU Browser Speeds Register Configuration

Nobody enjoys poring through data books full of register bit settings. The CPU Browser™ register configuration utility makes your life easier with an error-proof means to configure and visualize the states and meanings of internal 80960 RP registers, such as the PMCONs, MBCR, timer, and interrupt registers. Its graphical display shows current or proposed register configuration information, with point-and-click access to all configurable bit fields.

Pre-set hex and binary values for bit configuration prevent mis-keying, and error checking is performed on all changes before they are applied. The CPU Browser window includes clear descriptions of individual bit fields, and the register bit configuration display immediately previews the effects of enabling and disabling each bit state.

CPU Browser lets you keep the data books on the shelf.

Performance Plus Tools Go Beyond Analysis

It takes more than just analysis to optimize performance. That's why the CodeICE system for the 80960 RP includes a suite of tools to help you streamline your embedded design.

Applied teamed with Intel to offer convenient profiling and code coverage support for Intel's optimizing compilers. The result is a set of seamless, easy-to-use commands that automate the process of locating, extracting, formatting and uploading real-time profile data from memory back to your file system in a ready-to-go image.

Automated performance improvement may be all you need in many situations. But for critical applications you can make additional system performance measurements with an easy to use Performance

Analysis tool. Because it places no demands on target operation or resources, the tool delivers an accurate view of where your code spends its time. It monitors an unlimited number of modules, gathering data to describe execution activity, code timing, interrupt timing and fault detection. Data is presented in an easily understood histogram format, and the tool generates reports to help document software and product performance.

Product validation is also an important component of every product life cycle. The CodeICE system includes an extensive macro language that lets you build automated test suites using emulator commands.

Once you've fine-tuned target performance and built up an arsenal of comprehensive test cases, you can use CodeICE profile support commands to gather test coverage information. Used together with Intel's coverage analyzer, CodeICE performance tools tailor the output of the code coverage report to your requirements, such as call graph listings, combinations of program-, module-, function-, and source-level coverage reports, hit or miss source line execution, and two-profile comparisons.

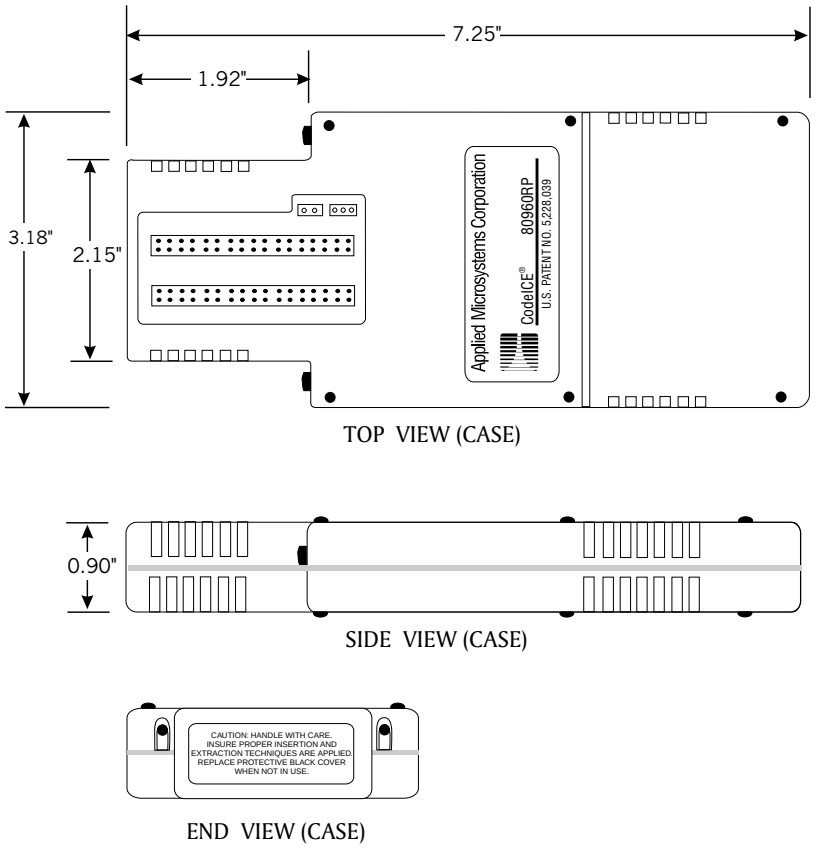
Helping You Succeed

Because our success depends on your success, we take product support very seriously. In fact, at Applied Microsystems we call our program Customer Satisfaction. Keeping you satisfied means more than just answering your questions. The leader in embedded development tools and the most experienced 960 market driver, Applied has the qualified and committed people it takes to provide thorough on-site training and superior engineering assistance, technical guidance on emulation issues, and expedited product service.

Our Applications Engineering Group is backed by a network of experienced Field Application Engineers, our own design teams, and the commitment of the entire company. And with over 16,000 installed solutions and more than fifteen years of leadership in embedded hardware and software development tools, our team is an important asset to have on your team.

Take the Time to Call Now

To see how the new CodeICE 960 RP emulator can help you beat the clock, call 1-800-426-3925 for information or a product demonstration. And breathe easier—with the CodeICE emulator you can develop your 960 RP product on time and in budget. And maybe even have a little time for yourself.



Dimensions of the CodeICE 960 RP emulator probe tip.

CodeICE Emulator for Intel i960® RP Microprocessors

Microprocessors Supported
Intel 80960RP at 16–33 MHz

Packages Supported
SBGA or BGA
Supports both the Intel connector specification (272812-001) and the Applied Microsystems standard connector (926-07959-00))

Minimum Host Requirements
PC 386 or better
Microsoft Windows 3.1 or higher, 12 MB RAM minimum, 16 MB recommended (1 vacant ISA or EISA slot for Ethernet)
Sun SPARC
16 MB RAM minimum, 20 MB swap, Sun OS 4.1.x, Solaris 2.2/2.3, Ethernet port
HP 9000/700
16 MB RAM minimum, 20 MB Swap, HP/UX 9.0 or later, Ethernet port

Communications
PC Environment:
Ethernet (Winsock 1.1, TCP/IP (incl. Novell)), IEEE 802.3 10base2, 10base5, 10baseT
Sun / HP Environment:
IEEE 802.3 10base2, 10base5, 10baseT

User Interface
Integrated Source Level Debugger
Multi-Windowed interface (X-windows/ Motif on workstations, Windows on PC)
Support for Intel, GNU, and MRI C / C++ and assembly language
Access to all global, local, stack-based and register-based symbols with full data typing features
Debug code without stopping the target system with Dynamic Run, Stop and Update
Execution breakpoints can be set on line numbers, source statements, program labels and memory addresses
High-level control of all emulation subsystems
Performance Optimizing Tools
Profile support for Intel's optimizing C compilers and code coverage utilities
Integrated Performance Analysis
View statistics based upon the number of occurrences of functions and/or actual time spent in functions in a convenient histogram format
Real-Time Operating System Support Option
Integrated support for Wind River Systems VxWorks RTOS
Display status of RTOS structures, profile tasks in real-time, trace the flow of RTOS activity, isolate defects based on RTOS activity, and more
Flash Programming
CPU Browser
Graphical interface allows display and modification of internal memory, breakpoint, interrupt controller and timer unit, PCI to PCI bridge, address translation unit, message, and DMA register values

Trace System
Hardware
Trace depth 32K x 224 bits wide with programmable 24-bit timestamp
Intelligent Trace Disassembler
Display instructions and register contents correlated with data
Trace Windows
Choose between bus cycle, assembly, and source trace display, on-the-fly, in any combination
Scrollable forward and backwards
Search trace for specified patterns
Connected to the event system to allow qualified tracing
Source-Level Trace
Unique capability displays which source lines were executed and correlated values while executing out of cache
PCI Trace
Low-level, by clock information
High-level transaction information
Protocol violation display
Event Systems (One CPU Core; One PCI)
Define external signals from your target to qualify events
4 independent groups; 4 independent, configurable states; 4 PCI
2 32-bit counters and 2 PCI counters
4 BNC connectors: one i960 trigger out, one PCI trigger out, one i960 trigger in, one PCI trigger in
i960 trace supports qualification of event by value of variable, LSA input, address, data, CPU signal status, trigger in, trace full or counter
PCI trace supports qualification of event by value of start address, data, status, trigger-in, and counter
Event Actions:
Break — Trace on/off/one
Activate state/group — Trigger out
Increment/reset counter

Breakpoint System
Up to 26 hardware access breakpoints and an additional 2 hardware execution breakpoints for ROM or RAM
Virtually unlimited software execution breakpoints for code located in RAM
1 asynchronous breakpoint from keyboard
Access to on-chip breakpoints

Target Hardware Debug Support
Fully buffered probe tip allows debug of dysfunctional target hardware
Predefined diagnostic routines and scope loops offer a suite of tools to quickly isolate defective hardware
Integrate up to 16 external signal lines from your target hardware into the CodeICE break, event and trace systems with optional Logic Analysis Probe

Advanced Testing and Validation
C-like macro extension language allows you to construct and save target regression tests
Record and playback debugging sessions

Physical Specifications
Chassis: 16" X 13" X 5" (40.6 cm X 33 cm X 12.7 cm) [L x W x H]
Chassis weight: 14 lb.s. (6.35 kg)
Probe Tip: 7.25" X 3.18" X 0.81" (18.41 cm X 8.07 cm X 2.05 cm) [L x W x H]
Probe Tip cable length: 24" (60.96 cm)

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