

# EL 3200 Emulator

## for Motorola 68360, 68EN360 and 68MH360 Microcontrollers

### Highlights

- Full-featured in-circuit emulator supporting all 3- and 5-volt family members to 33 MHz
- Powerful, multi-windowed debugger with C and C++ support on Sun4, HP9000 and PC hosts
- Compiler support for MRI, DIAB Data, GNU, Intermetrics and Greenhills
- RTOS Kernel support with real-time task and kernel profiling, system error detection and unique system visibility
- Register-tracking trace disassembler provides code execution history including register state and data accesses
- Register-decoder provides English-language description of processor and SIM60 register configurations
- Non-intrusive, crash-proof emulation:
  - Complete electrical and logical isolation for debugging dysfunctional targets
  - Uses no target memory space
  - Automatic recovery from hung bus-cycle conditions
  - Runs in-target at up to 33 MHz without wait states
- Sophisticated breakpoint and event systems provide precise debugging control and make it possible to trap time-sensitive, deeply nested and elusive bugs

### Companion Products

- CodeTAP®-BDM provides a robust BDM-style tool supported by the same user interface as the EL 3200 68360
- CodeTEST™ for 68360 provides a suite of tools for software developers and testers, including memory allocation analysis, performance analysis, code coverage analysis and trace analysis

*Technical advances tailored to the 68360 family of microprocessors.*



### Transparent 68360 Emulation

The EL 3200 emulator offers embedded systems developers a powerful, complete set of real-time emulation and debugging tools for both the 68360 family of processors. Engineers designing these processors into their products can take full advantage of all chip features and do so without burden or modification to the target hardware or software design. The emulator provides complete electrical and logical isolation, runs in-target at full speed, and consumes no target resources.

The emulator probe tip physically replaces the target system's microprocessor, and communicates with the advanced C/C++ source-level debugger through a high-speed serial, parallel or Ethernet link to Sun SPARCstations or PCs. From the windowed interface, EL 3200 users can control the entire debugging process: downloading software, controlling target operations, modifying memory and registers, and acquiring execution trace history. Optional language tools include an ANSI C/C++ optimizing compiler, assembler, and an instruction set simulator. This fully integrated development system boosts productivity and reduces time-to-market by getting your target running sooner and more reliably.



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*We also offer tools to support these Motorola products:  
68000, 68EC/HC000, 68020/EC020, 68030/EC030, 68040/040V,  
ColdFire MCF5102, 68302, 68330/340, 68331/332*

### **Advanced Features Mean Faster Debugging**

For efficient and accurate debugging, the EL 3200 for the 68360 incorporates advanced features including a powerful debugger, automatic pin tracking, an extremely capable event system, an intelligent trace disassembler, and high-speed communications.

The windowed source-level debugger provides multiple ways to view your code and data. Pin tracking automatically reconfigures the emulator to follow your definition of processor pins. The ground-breaking intelligent trace disassembler increases debugging efficiency by displaying instructions correlated with register values and data accesses. Event and breakpoint systems help find deeply nested bugs more quickly. The event system supports up to eight event statements in each of four groups. The breakpoint system includes ample hardware access, hardware

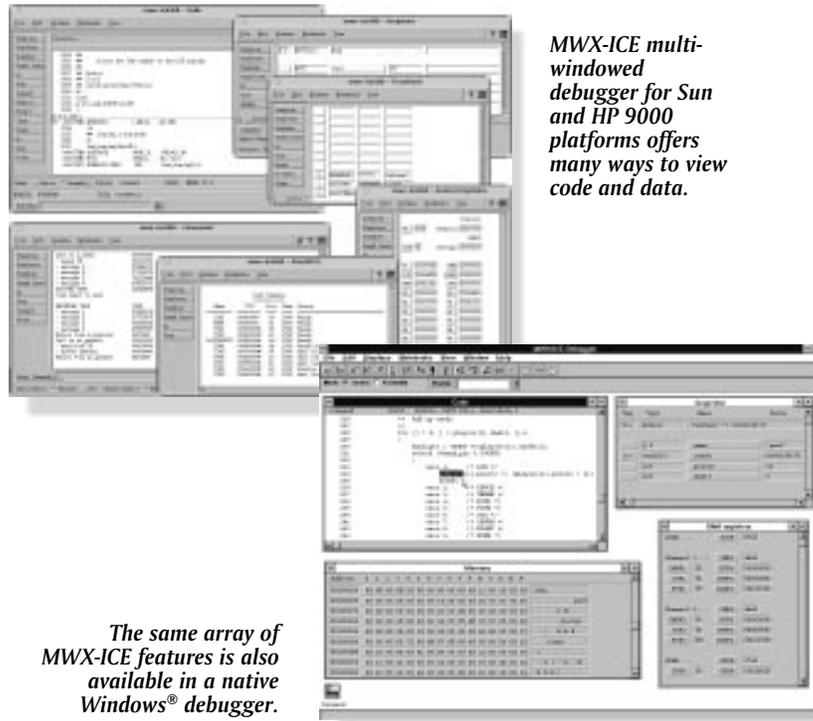
execution, and software execution breakpoints. For maximum productivity, the EL 3200 leads the industry with very high speed downloading. Combined with up to 4 MB of optional overlay memory, this eliminates the need to re-program EPROMs and makes debugging boot code faster and easier. And the Ethernet communication capability provides shared network access to the emulator for increased cost-effectiveness and efficiency.

### **Source-Level Debugger Combines Power and Ease of Use**

A function-rich Sun 4, HP9000 or PC-hosted C/C++ source- and assembly-level symbolic debugger supports the EL 3200. It provides access to high-level data structures and dynamic variables. The windowed interface smoothly implements complete control over all emulator functions. Users can: selectively start and stop

execution; display and modify CPU registers, stacks and memory; and collect and display program execution trace history. In addition, the debugger makes it easy to control the event system, set breakpoints, and create macros that can execute automatically when a breakpoint is encountered. Supported tool chains include MRI and GNU. A built-in assembler permits the user to assemble code in target memory using Motorola mnemonics.

Symbolic debugging is an integral part of the debugger. Symbols include arrays, structures, static variables, and register- and stack-based variables. Symbols can be displayed or changed by name, as declared in the program. The type and scope of each symbol, and its value in binary, hex, ASCII, or decimal format, can be displayed. Users can reference structure members, de-reference pointers, and apply type overrides. Memory contents with absolute references or register-relative references can also be displayed.



*MWX-ICE multi-windowed debugger for Sun and HP 9000 platforms offers many ways to view code and data.*

*The same array of MWX-ICE features is also available in a native Windows® debugger.*

## Real-Time Kernel Visibility and Performance Measurements

EL 3200 engineers work closely with industry-leading commercial kernel developers to provide comprehensive support packages for Real-Time Operating Systems (RTOS). RTOS visibility at the CodeICE level shows how the target, application, and RTOS interact with one another during execution in a thoroughly integrated, real-time environment.

Applied's RTOS-Link™ feature provides several broad categories of support, including: real-time trace of RTOS activity, display of individual task context and other system structures, task-qualified breakpoints, task stack overflow detection, and task profiling support. The benefit of integrated RTOS support is a substantial reduction in the time required to debug and optimize your application as it runs in your target.

## Trace History Shows Problem Causes

Trace history allows users to capture and record processor execution history, in real-time, while the emulator executes the target program. With trace history, users can verify software operation and find errors that may occur during execution of the program. Intelligent trace disassembly—an industry first—dramatically increases productivity by displaying instructions correlated with register values and bus cycles. And because IPIPE and IFETCH signals are monitored, trace disassembly is extremely accurate. By combining event system conditions with trace control actions, a “qualified” trace captures only bus cycles of interest and eliminates unwanted information.

The EL 3200's trace buffer is 32K bus cycles deep by 144 bits wide.

Trace history can be displayed in raw bus cycles, C/C++ source-level, assembly-level, or mixed C/C++ source and assembly. Trace history can also be stored in a file for later analysis, along with comments to aid in documenting failure conditions and other items of interest. Trace commands permit paging backward or forward through trace history, displaying a particular line or range of trace history, and searching trace for a particular bus cycle.



*RTOS-Link provides visibility of configuration and activities in kernel-based systems. Views such as task execution trace, task profiling, and configuration detail help you quickly isolate even subtle system problems.*

## Full Breakpoint System Offers Choices

With a generous selection of breakpoints, debugging is easier and less intrusive. The EL 3200 emulator provides three types of breakpoints to best serve your needs:

- hardware execution breakpoints
- software execution breakpoints
- external asynchronous breakpoints

Hardware breakpoints can be qualified with bus cycle status, and can be set over target RAM or ROM. For precise control without code modification or RAM usage, hardware breakpoints allow breaking from emulation before instruction execution.

Software execution breakpoints are useful for code held in RAM. The EL 3200 provides 1024 software execution breakpoints which are managed so as to be transparent to the user. The display of code is not affected even though it may be riddled with breakpoints in target memory.

The EL 3200 also supports asynchronous breakpoints from the keyboard or another instrument such as a logic analyzer.

## Event System Monitors Complex Conditions

The advanced event system is particularly well-suited to debugging nested or sequential problems. With it, users can set up complex conditional events that trigger various emulator actions. Such actions include break emulation, switch between event system groups, turn trace on or off, control a counter, force special interrupt or trigger another instrument. The EL 3200 supports four independent groups of address, data, status, and logic state comparators. The comparators monitor program events, a timer, two counter values, logic state information, and the CPU bus state.

The EL 3200 also provides both BNC input and output to cross-trigger laboratory instruments. When the EL 3200 event system receives an external trigger-in signal from the target or from a piece of test equipment, such as a logic analyzer, it can cause the EL 3200 to break emulation or initiate any function available to the event system.

## Overlay Memory Saves Time and Effort While Developing Boot Code

The EL 3200 contains overlay memory that can replace target RAM, ROM or EPROM memory or be used where target memory resources do not exist. Using overlay memory eliminates the need to burn PROMs and makes immediate code patches possible.

Up to 4 MB of high-speed overlay can be mapped in 4K segments anywhere in memory, including ROM addresses (except space used by 68360 SIM registers). Because the overlay supports the processor's dynamic bus resizing capability, memory can be mapped using either addresses or chip selects and can be either 8-, 16-, or 32-bit based. Each segment of overlay memory can be mapped as read-only or read/write. During emulation, if a write cycle attempts to use a read-only segment, the EL 3200 can be set to issue a violation message. Overlay memory operates to 20 MHz with zero wait states during three-clock bus cycles with no performance impact on the target; one wait state is required between 20.1 and 33 MHz.

## Physical Specifications

Chassis: 17.5"W x 14.75"D x 6.50"H

(44.45cm x 37.46cm x 16.51cm)

Chassis weight: 25 lbs. (11.3 Kg)

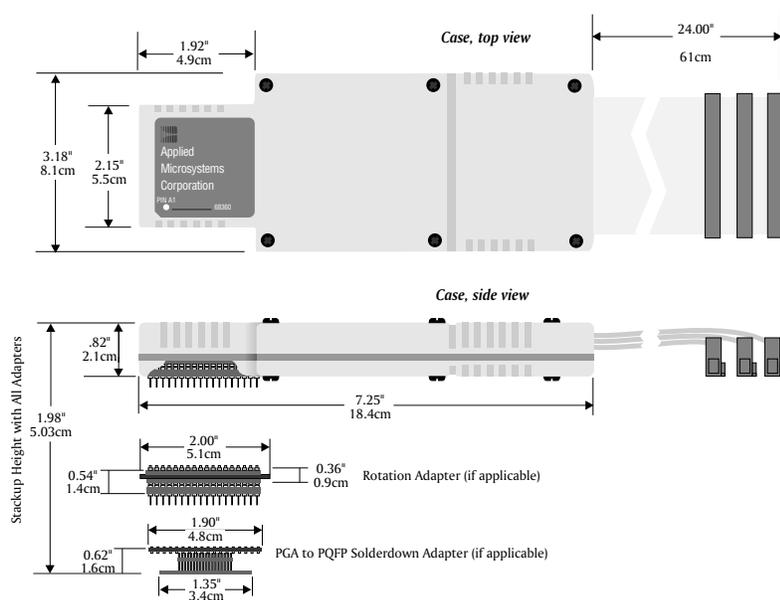
Probe tip: 3.18"W x 7.25"L x .82"H

(8.1cm x 18.4cm x 2.1cm)

Probe tip cable length: 24" (61cm)

Ambient humidity: 0–90% non-condensing

Operating temperature: 32–104°F (0–40°C)



EL 3200 68360 Probe Tip and Adapter Dimensions

### ***Rich Macro Language Provides Custom Features***

Users can construct complex macros containing ANSI C statements, expressions, and debugger commands for regression testing, code patching, and hardware simulation. Macros can be invoked from the keyboard, buttons on the user interface or some system event. For convenience and for documenting procedures, debugging sessions can be recorded and played back.

### ***Pin Tracking Lets You Debug Your Software Instead of Your Debug Tool***

A hallmark and highly useful feature of the 68360 is the ability to reprogram pins on-the-fly to perform different functions. While this feature offers developers valuable flexibility, it can create obstacles to accurate emulation.

An emulator that doesn't account for reprogramming can miss critical signal information. A cumbersome work-around is to program the emulator for a single assumed state of the processor, then stop execution and re-configure the emulator whenever the processor state changes.

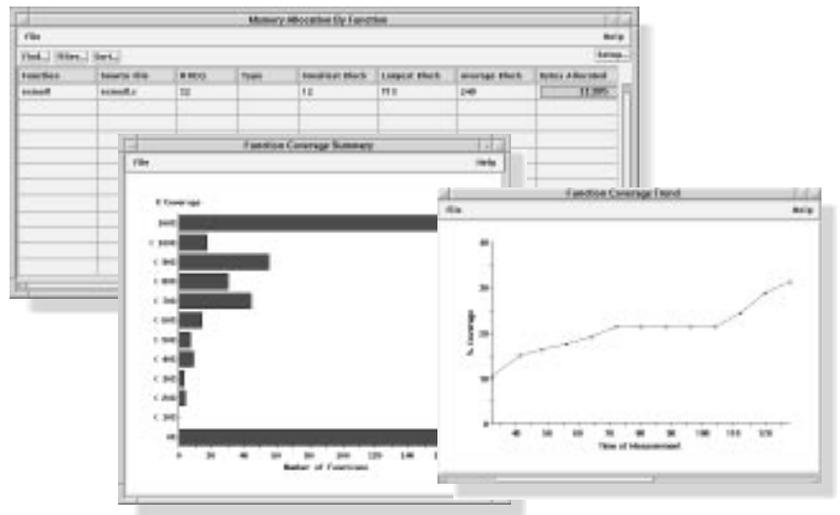
The EL 3200 conveniently solves the problem with unique pin tracking circuitry. Pin tracking transparently responds to changes in pin functions. This allows trace memory, trace disassembly, overlay address mapping, event system operations, and breakpoints to function accurately at all times—even while pin functions are being reprogrammed—all without user intervention.

### ***Companion CodeTAP-BDM Provides Low-Cost, Crash-Proof Replacement For ROM Monitor***

The CodeTAP-BDM exploits the background debug mode of the 360 to offer a low-cost, crash-proof emulation tool for the software developer. This particularly robust BDM tool helps the developer accelerate the debugging process with an Ethernet connection for downloading code to RAM or Flash, controlling target operation and perusing memory and register information. The CodeTAP-BDM employs the same MWX-ICE interface as the EL 3200 to provide symbolic debugging on Sun4, HP9000 and PC-Windows. It also provides a simple target connection for rack mounted systems and offers a viable mobile debugging tool when attached to a portable PC and the Windows version of MWX-ICE.

### ***CodeTEST Companion Tools Test, Analyze and Measure Code Performance***

Software development is made from equal parts of debugging and testing code. The CodeICE provides an exceptional set of tools to debug code; CodeTEST offers the same for testing code. In fact, CodeTEST is the first software verification tool suite crafted specifically for embedded software. It offers memory allocation analysis to help you locate memory leaks and detect improper uses of malloc() and free(). Performance analysis provides real-time module duration and call-pair linkages for up to 32,000 functions. The coverage analysis package clarifies the effectiveness of your test suite to help you develop higher quality code. Finally, the trace analysis package offers multiple ways to view the execution history of your program and, thereby, see the “big picture” about the operation of your software.



***CodeTEST™ Embedded Software Verification Tools for 68360 offer developers and testers comprehensive software performance analysis, code coverage analysis, memory allocation analysis, and software trace.***

# EL 3200 Emulator for Motorola 68360, 68EN360 and 68MH360

## Microprocessors Supported

68360 to 33 MHz; 68EN360 to 33 MHz; 68MH360 to 33 MHz

## Packages Supported

241-pin PGA; 240-pin PQFP (via solder-down or clip-over adaptor)

## Minimum Host Requirements

PC386, Microsoft Windows 3.0 or higher, 16 MB RAM, ISA or EISA slot  
Sun SPARC, Sun OS 4.1, 20 MB swap  
Solaris 2.2 or above  
HP 9000, HP-UX 9.0 or above, 20 MB swap

## Communications

### PC Environment

IEEE 802.3 10base2, 10base5, 10baseT (effective download speed 4.0 MB/min)  
High-speed parallel (ISA or EISA bus required, effective download speed 5.0 MB/min)

### Sun and HP9000 Environment

IEEE 802.3 10base2, 10base5, 10baseT (effective download speed 4.0 MB/min)

## Optional Code Generation Tools

ANSI C / C++ cross-compiler  
Cross-assembler  
Embedded linking loader  
Object module librarian

## Optional Instruction Set Simulator

Interprets user programs and processes code identically to the microprocessor  
View code execution in high-level or assembly-level

## Source-Level Debugger

### Integrated source level debugger

Window-oriented interface (X-Window support on SUN)  
Support for C, C++ and assembler  
Access to source code variables  
Disassembled source view for machine-level debug and patch  
Access to all global, local, stack-based and register-based symbols  
Full C-typing features

### Execution control and full access to the emulator

Soft switches provide interactive instrument control  
Execution breakpoints can be set on line numbers, C statements, program labels and memory addresses  
Display trace in raw, assembly, and high-level formats or disassembled  
Monitor real and simulated I/O  
High-level control of event system set-up and operation  
Perform emulator operations while the target is running

### In-line assembler/memory functions

Assemble code in target memory using Motorola mnemonics  
Display and modify memory

### Performance analysis

Display relative time spent in functions or groups of functions  
**Advanced testing and set-up capabilities**  
Construct complex macros containing C-like statements and debugger commands

Record and play back debugging sessions  
EXPLODE command displays register contents with explanations

### File format compatibility

IEEE 695, A.OUT, COFF, S-record

## RTOS Support

ISI pSOS+ via Applied's RTOS-Link™

## Advanced Trace and Event System

### Trace System:

32K deep x 144 bit wide trace buffer records data in real time  
Display CPU bus cycle information, including address, data and control lines with symbols  
Display and save disassembled code execution, assembly- and C source-level, with symbols  
Search for trace frames containing any combination of address, data, and status information  
Record timestamp information (50 ns to 10 ms resolution)  
Record DMA cycles

Record external 16-bit logic state inputs (with optional Logic State Analysis Probe)

### Event System:

4 independent groups (address, data, bus status, and logic state comparators)  
Up to 8 conditional statements per group  
Multiple address, data and status conditions per statement  
1 BNC trigger in/out  
20 MHz timestamp timer; 2 event counters  
8 Event Actions

## Intelligent Trace Disassembler

Displays instructions and register contents correlated to data

## Target Diagnostics

Built-in diagnostic routines to debug target hardware before running code

## Breakpoint System

1024 software execution breakpoints  
16 hardware execution breakpoints  
16 single access breakpoints or 8 range access breakpoints  
1 asynchronous breakpoint via keyboard  
1 BNC input and one BNC output support external breakpoints

## Overlay memory

1MB or 4MB  
Zero wait state during three clock bus cycles to 20 MHz; one wait state 20–33 MHz  
Supports pin re-programming and dynamic bus sizing  
Set read/write protection including read-only during run  
Map anywhere, with minimum resolution of 4K bytes  
Map as 8-, 16-, or 32-bit port or as chip select

## Pin Tracking

Basic Breakpoint, Overlay, and Trace and Event Systems transparently track the processor's dynamic reprogramming of pin assignments and chip select registers

## IPIPE/IFETCH Decoder

Decodes IPIPE/IFETCH pins for trace disassembly

## Power Requirements

Emulator, AC: 250 W, 115Vac, 47–63 Hz, or 230Vac, 47–63 Hz  
Probe tip, from target: 5mA from CPU socket



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