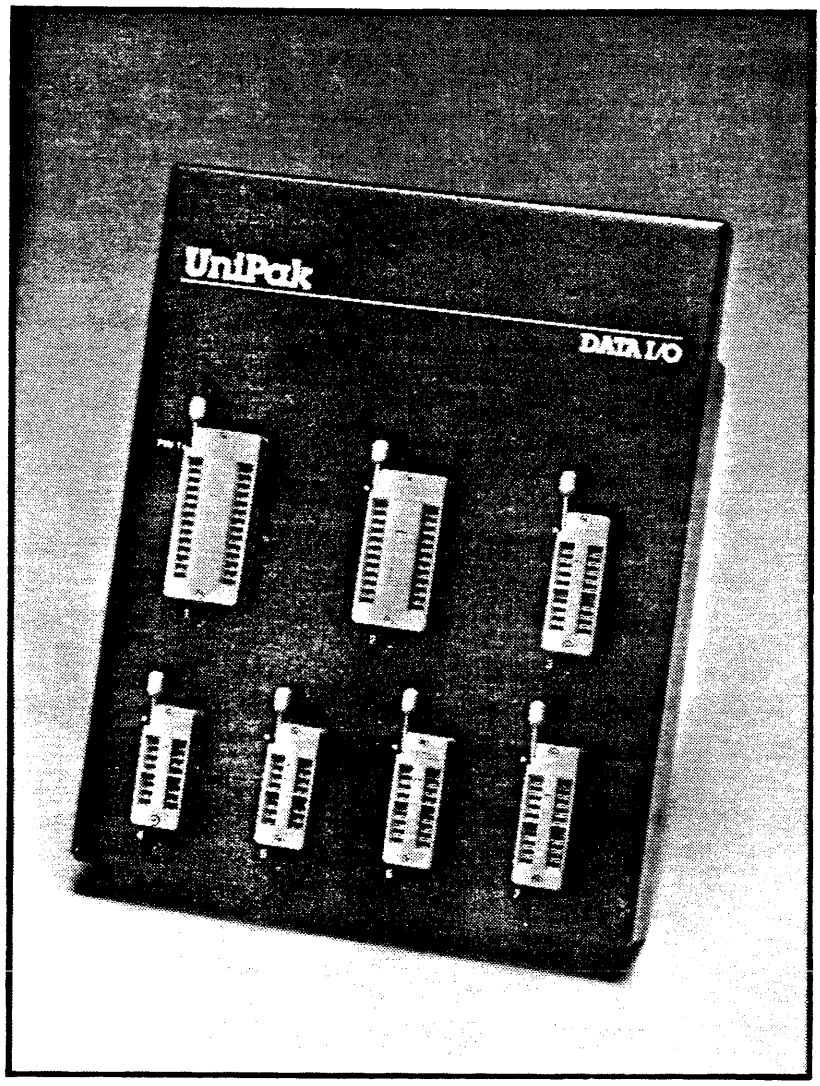


UniPak
950-0099-005

REV N MAY 83 **10-950-0099**

FOREWORD

Before using the -005 version of the UniPak, read the information in this section to be sure your programmer does not require a modification. Either or both of two modifications to your System 17 or 19 may be required for compatibility with the -005 or later version of the UniPak:

A. It may be necessary to make a small hardware modification to the System 17/19 Controller (702-1520).

B. A firmware update may be necessary.

29A Universal Programmers and 100A Production Programmers may need a firmware update.

A. HARDWARE MODIFICATION

System 19s with serial numbers below 1516 and System 17s with serial numbers below 219 will require a small modification for use with the UniPak. The UniPak may cause invalid error messages if the modification is not made. No other programmer functions are affected, nor will attempting an operation harm the programmer, the UniPak, or a device in the socket.

CAUTION

The following hardware modification to the System 19 and 17 should be performed by a qualified technician only. If the facilities are not available to perform the modification, contact your local Data I/O Service Center listed below to arrange for return of the programmer to Data I/O for modification.

Data I/O Corporation
10525 Willows Road N.E.
C-46
Redmond, WA 98052
(206) 881-6445
Telex 15-2167

Data I/O Corporation
2770 South Harbor Blvd.
Suite K
Santa Ana, CA 92704
(714) 662-1182
Telex 910-595-1562

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511
(603) 889-8513 (Applications & Service)
Telex 943431

DATA I/O EUROPE
Vondelstraat 50-52
NL-1054 GE Amsterdam
The Netherlands
(20) 186855
Telex 16616 DATIO NL

Data I/O Corporation
473 Sapena Court
Suite 4
Santa Clara, CA 95050
(408) 727-0641
Telex 352054

Allan Crawford Associates, Ltd.
6503 Northam Drive
Mississauga, Ontario L4V IJ2
(416) 678-1500
Telex 06 968769

Data I/O Corporation
1810 N. Glenville Drive
Suite 108
Richardson, TX 75081
(214) 235-0044
Telex 792474

DATA I/O JAPAN
Data I/O Japan Company, Ltd.
Sankei Building
1-8, Sarugaku-cho 2-Chome
Chiyoda-Ku, Tokyo 101
Japan
(03) 295-2656
Telex 2225391 DATAIO J

MODIFICATION INSTRUCTIONS

1. Unplug power cord.

2. Remove Programming Pak.

3. Remove protection shield.

   a. Pull the two snap-lock connectors and lift them gently.
   b. Lift the back edge of the plate first and pull it up slightly and turn it to the left until it is clear.

4. Remove top cover.

   a. Turn the programmer on its top.
   b. Remove the 4 cover screws.
   c. Turn the programmer upright and lift the cover off.

5. Remove display panel.

   a. Remove 4 screws located at the corner of the display panel.
   b. Remove the screw fastening the support bracket to the power supply assembly.
   c. Remove the screw fastening the support bracket to the front of the base.
   d. If there is a screw fastening the support bracket to the bottom plate, remove it.

6. Refer to Figure 1. Sever the trace connecting R66 to U41 pin 1 just above R66 (left side).

7. Install an insulated wire from the top side of R58 (just *left* of C29, in front of the Programming Pak connector) to U41 pin 1. To connect to U41 pin 1, use the feed-through hole on the trace tying R66 to U41. (See Figure 1.)

8. Reinstall the display panel top cover and protective shield by reversing the removal procedures.

PROGRAMMER CHECK

9. Install a Programming Pak.

   a. Check the programmer for proper initialization.
   b. Load a device with a known data pattern and perform a verify to confirm proper operation.

B. SOFTWARE UPDATE

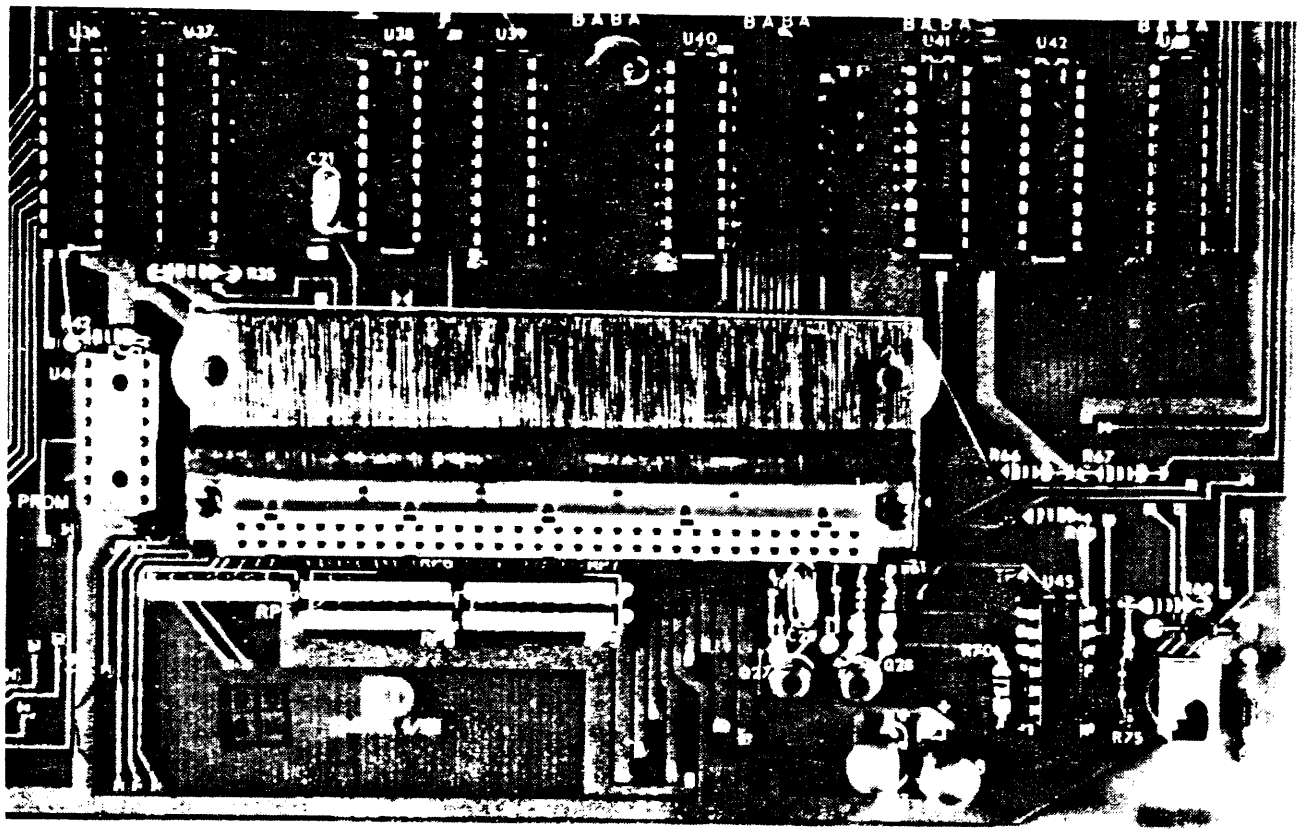
Some programmers require a software update for compatibility with the -004 or later version of the UniPak. Table 1 shows the revisions and software-configuration-check numbers for each programmer configuration requiring a software update. If your System 17 or 19, 29A or 100A is of one of these revisions, contact a Data I/O Sales Representative to order the appropriate update kit.

To determine the revision level of a programmer, use the procedure below to display the software configuration-check number and compare it to Table 1.

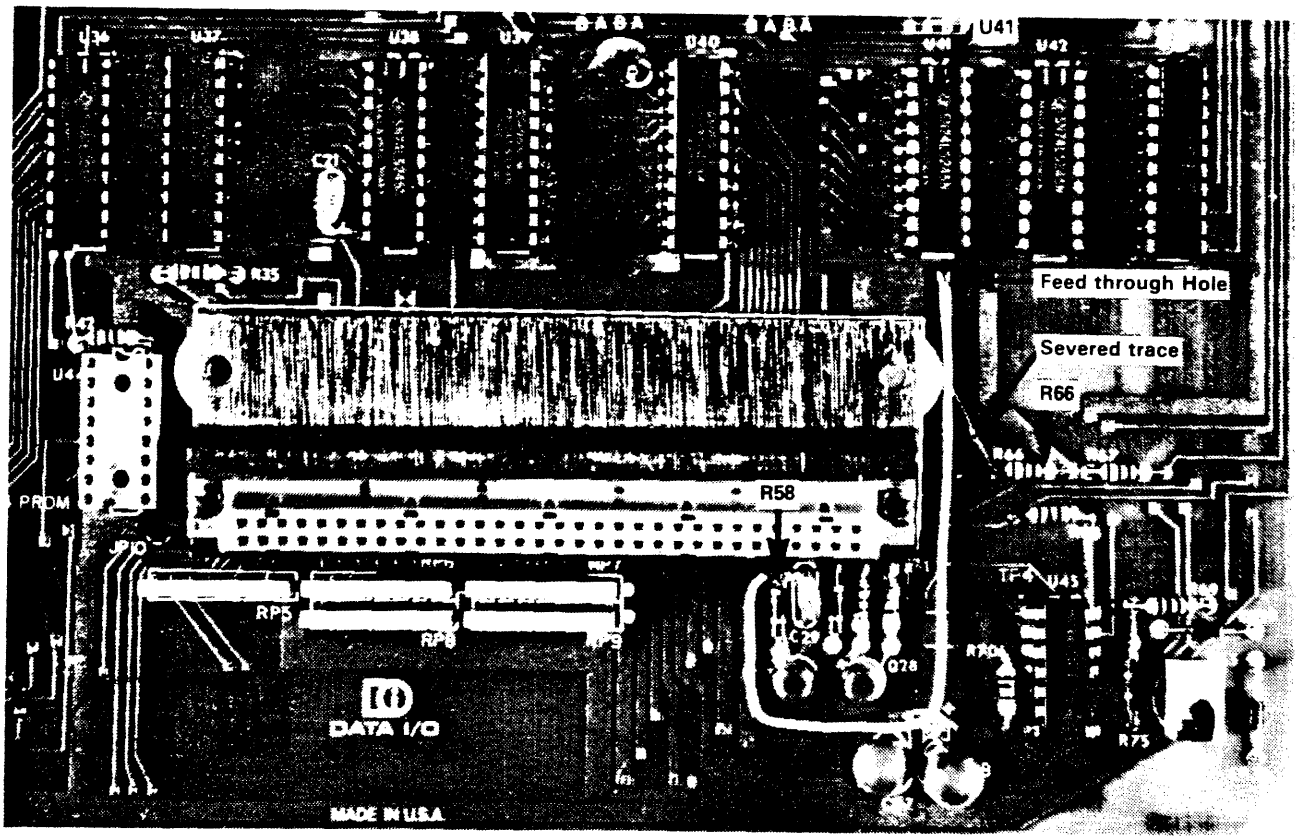
- **System 19 and 29A, all configurations.** Key in Select Code B2-START.
- **100A Production Programmer.** Key in Select Code 10.
- **System 1730.** Enter remote control and use the G command.
- **System 1731.** Enter remote control and use the CN command.

Table 1. Programmers Requiring Updates

System	Revision	Software configuration check number
990-1900	A	F9CF
	B	ØØAC
	C	Ø7CD
	D	ØB11
	E	FC6A
	F	B16C
990-1901	A	89CC
	B	CC89
	C	6BCD
990-1902	A	C56C
	B	8B82
	C	9141
	D	9ØØ2
	E	2Ø68
	F	29CE
	G	3868
	H	3599
990-1903	A	2C23
	B	6A9B
	C	3A33
990-1730	A	6D7B
	B	ADF5
	C	35EE
	D	4180
	E	44F8
990-1731	A	93AA
	B	3A3A
29A	A	1ECA
	B	20A4
29A w/computer remote control	A	BB41
	B	CØØB
100A	A	917F
	B	9405
	C	9DEE
	D	9BED



a. Before Modification.



b. After Modification

Note: Your Controller may appear slightly different. Be sure connections are made tc the components designated in this bulletin.

Figure 1. Jumper-Wire Location on Programmer Controller, 702-1520.

NOTE

This configuration of the UniPak varies from previous configurations in that it uses some hexadecimal family codes. No decimal family numbers have been changed. While this configuration will work with any Data I/O Universal Programmer (see Section 1.1), to use hexadecimal families it may be necessary to update your programmer. Refer to the foreword section of this manual for maintenance compatibility requirements. Model 1730's cannot handle hexadecimal families at this time. Some of the new larger devices will require that the programmer RAM be expanded. Consult your nearest Data I/O representative for update availability.

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SECTION 4. CALIBRATION

SECTION 5. MAINTENANCE

SECTION 6. TROUBLESHOOTING

SECTION 7. CIRCUIT DESCRIPTION

APPENDIX 1. ERROR CODES

SECTION 8. SCHEMATICS

LIST OF FIGURES

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SECTION 1
INTRODUCTION

1.1 GENERAL INFORMATION

Data I/O's UniPak reliably programs over 400 different popular MOS and bipolar devices. By generating programming signals under software timing and routing control, the UniPak eliminates the need to change hardware for different devices.* A 2-digit Family Code and a 2-digit Pinout Code select all the necessary conditions for each device within the UniPak's repertoire. With codes selected, the UniPak illuminates the LED of the appropriate socket.

The UniPak can be used in System 19s, 29A Universal Programmers, and Model 100A Production Programmers of any configuration and in System 17s with remote control (see note page i).

1.2 APPLICATIONS

Table 1-1 is a complete list of devices within the capability of the UniPak at the time this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the UniPak will not require any revision. For some new applications, such as to accommodate a new device family, a software update of the UniPak may be required. The revision letter is stamped after the part number (950-0099) along the underside of the top edge of the UniPak socket assembly. Data I/O Field Bulletins give information on updating equipment.

1.3 SPECIFICATIONS

The UniPak receives its power from the programmer. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling software is located on a separate circuit card within the UniPak.

Table 1-2 lists the physical and environmental specifications of the UniPak.

1.4 ORGANIZATION OF THE PROGRAMMING ELECTRONICS

The UniPak is designed to adapt to the programming requirements of several device families.

Pinout variations are handled by the 7 device sockets on the UniPak; specially designed electronic switches allow programming of both bipolar and MOS devices in the 24-pin socket (number 2).

In order to maximize control speed during programming, the UniPak makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by software.

Values for programming variables, including pinouts, voltage levels and timing, are stored in software tables. When the operator chooses the Family and Pinout Codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum software.

1.5 CALIBRATION

The need for calibration varies with the amount of use. Generally, we suggest calibration whenever programming yields fall below the manufacturer's recommended minimums.

The UniPak can be calibrated only on a programmer that has an address and data display; UniPaks used with a System 17 programmer must either be calibrated on another programmer or sent to a Data I/O Service Center.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of 90 days begins when you receive the equipment.

The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

1.7 SERVICE

Data I/O maintains Service Centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products are calibrated. A list of all Data I/O Service Centers is located in the back of this manual.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative. Orders for shipment must contain the following information:

- Description of the equipment (See the latest Data I/O Price List or contact your sales representative for equipment and part numbers.)
- Quantity of each item ordered
- Shipping and billing address of firm, including zip code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment.

* As of the -004 version, several adapters will be available to program several nonstandard pinout devices.

Table 1-1. UniPak Family and Pinout Codes

KEY TO HEADINGS

1. Device Part Number. The part number assigned by the device manufacturer.
2. Family Code. A 2-digit number that designates the programming algorithm.
3. Pinout Code. A 2-digit number used to differentiate device types based on pin assignment and array size.
4. UniPak Revision. A number in this column specifies the earliest software version of the UniPak that will program the device to the manufacturer's latest specifications.
5. Socket Adapter. Model number of the socket adapter that programs the device. If a number does not appear in this column, use the fixed 28-pin front panel socket to program your device.
6. Socket Adapter Revision. Indicates the earliest revision of the socket adapter that will program the device.
7. Notes. The following is an explanation of the letters that appear in the Notes column.
   - O - This device is obsolete and no longer in production
   - P - This device is currently in production. Data I/O has a written manufacturer approval for this device's programming algorithm.
   - I - Programming algorithm for this device is installed within the programmer; manufacturer approval has been requested.

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Advanced Micro Devices						
27LS18	16	02	A	-	-	P
27LS19	16	02	A	-	-	P
27S08	15	02	A	-	-	O
27S09	15	02	A	-	-	O
27S18	16	02	A	-	-	P
27S19	16	02	A	-	-	P
29750A	16	02	A	-	-	P
29751A	16	02	A	-	-	P
27S10	15	01	A	-	-	O
27S11	15	01	A	-	-	O
27S20	16	01	A	-	-	P
27S21	16	01	A	-	-	P
29760A	16	01	A	-	-	P
29761A	16	01	A	-	-	P
27S12	16	03	A	-	-	P
27S13	16	03	A	-	-	P
29770	16	03	A	-	-	P
29771	16	03	A	-	-	P
27S15	16	79	005	351A-068	A	P
27S24	16	65	003	-	-	P
27S25	16	65	003	-	-	P
27S26	16	85	005	351A-067	A	P
27S27	16	85	005	351A-067	A	P
27S28	16	09	E	-	-	P
27S29	16	09	A	-	-	P
27S30	16	36	A	-	-	P
27S31	16	36	A	-	-	P
29774	16	85	005	351A-067	A	I
29775	16	85	005	351A-067	A	I
27S32	16	38	E	-	-	P
27S33	16	38	E	-	-	P
27PS181	16	37	A	-	-	P
27PS281	16	37	003	-	-	P
27S180	16	37	A	-	-	P
27S181	16	37	A	-	-	P
27S280	16	37	003	-	-	P
27S281	16	37	003	-	-	P
27S35	16	66	004	-	-	P
27S37	16	66	004	-	-	P
27LS185	16	06	E	-	-	P
27PS184	16	06	A	-	-	P
27PS185	16	06	E	-	-	P
27S184	16	06	E	-	-	P
27S185	16	06	E	-	-	P
27PS191	16	68	H	-	-	P
27PS291	16	68	003	-	-	P
27S190	16	68	H	-	-	P
27S191	16	68	H	-	-	P
27S290	16	68	003	-	-	P
27S291	16	68	003	-	-	P
27S45	16	77	004	351A-066	A	P
27S47	16	77	004	351A-066	A	P
27PS41	16	53	005	351A-065	A	P
27S40	16	53	004	351A-065	A	P
27S41	16	53	004	351A-065	A	P
27PS43	16	63	004	-	-	P

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Advanced Micro Devices (continued)						
27S43	16	63	004	-	-	P
27PS49	16	67	003	-	-	P
27S49	16	67	003	-	-	P
2708	21	27	A	-	-	P
AM9708	21	27	A	-	-	P
2716	19	23	A	-	-	P
AM9716	19	23	A	-	-	P
2732	19	24	A	-	-	P
2732A	27	24	005	-	-	P
AM9732	19	24	A	-	-	P
2764	AF	33	005	-	-	P
AM9764	AF	33	005	-	-	P
27128	AF	51	005	-	-	P
27256	93	32	005	-	-	I
Electronic Arrays						
2708	21	27	A	-	-	P
2716	19	23	A	-	-	P
Fairchild						
93417	01	01	A	-	-	P
93427	01	01	A	-	-	P
93436	01	03	A	-	-	P
93446	01	03	A	-	-	P
93438	01	15	A	-	-	P
93448	01	15	A	-	-	P
93452	01	05	A	-	-	P
93453	01	05	A	-	-	P
93450	01	16	A	-	-	P
93451	01	16	A	-	-	P
93460	01	16	A	-	-	P
93461	01	16	A	-	-	P
93L450	01	16	A	-	-	P
93L451	01	16	A	-	-	P
93514	01	06	A	-	-	P
93515	01	06	A	-	-	P
93510	01	21	004	-	-	P
93511	01	21	004	-	-	P
2708	21	27	A	-	-	P
Fujitsu						
27C32A	27	24	A	-	-	P
27C64	45	33	005	-	-	P
27C128	45	51	005	-	-	I
8518	21	27	A	-	-	P
8516	19	23	A	-	-	P
8742	50	57	005	351A-070	A	I
8749H	50	57	005	351A-070	A	I
2732A	27	24	A	-	-	P
2732A-35	27	24	A	-	-	P
8532	19	24	F	-	-	P
2764	45	33	005	-	-	P
27128	45	51	005	-	-	I
General Instruments						
5716	83	23	003	-	-	P
5816	37	23	003	-	-	P

Table 1-1. Continued

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Harris						
6641	40	47	F	-		
7610	05	01	A	-	-	P
7611	05	01	A	-	-	P
7629	05	43	A	-	-	O
7620	05	03	A	-	-	P
7621	05	03	A	-	-	P
7640	05	15	A	-	-	P
7641	05	15	A	-	-	P
7648	05	09	A	-	-	P
7649	05	09	A	-	-	P
7642	05	05	A	-	-	P
7642P	05	38	H	-	-	O
7643	05	05	A	-	-	P
7643P	05	38	H	-	-	O
7644	05	04	A	-	-	O
7608	05	16	A	-	-	P
7680	05	16	A	-	-	P
7680RP	05	16	H	-	-	O
7681	05	16	A	-	-	P
7681RP	05	16	H	-	-	O
7684	05	06	A	-	-	P
7684P	05	06	H	-	-	O
7685	05	06	A	-	-	P
7685P	05	06	H	-	-	O
7616	05	42	A	-	-	P
76160	05	21	A	-	-	O
76161	05	21	A	-	-	P
76165	05	53	004	351A-065	A	P
76320	05	63	H	-	-	O
76321	05	63	H	-	-	P
76641	05	67	H	-	-	P
Hitachi						
27C64	79	33	004	-	-	P
462716	19	23	F	-	-	P
48016	33	23	E	-	-	P
462532	19	25	E	-	-	P
462732	19	24	A	-	-	P
462732P	19	24	A	-	-	P
482732A	27	24	A	-	-	P
482764	79	33	004	-	-	P
4827128	79	51	004	-	-	P
Hughes						
3004-1	58	62	004	-	-	P
3004-2	58	61	004	-	-	P
3704-1	58	62	004	-	-	P
3704-2	58	61	004	-	-	P
3008	58	60	004	-	-	P
3708	58	60	004	-	-	P
Intel						
2704	21	26	A	-	-	O
8704	21	26	A	-	-	P
2708	21	27	A	-	-	O
2758	19	22	A	-	-	P
8708	21	27	A	-	-	P
8741	56	59	005	351A-070	A	I
8741A	56	59	005	351A-070	A	I
8748	52	56	005	351A-070	A	I
8748H	50	56	005	351A-070	A	I
2716	19	23	A	-	-	P
2815	85	23	005	-	-	P
2816	37	23	H	-	-	P
8742	50	57	005	351A-070	A	I
8749H	50	57	005	351A-070	A	I
8755A	47	55	005	351A-072	A	I
2732	19	24	A	-	-	P
2732A	27	24	A	-	-	P
8751	53	58	005	351A-071	A	I
2764	79	33	004	-	-	P
2764A	93	33	005	-	-	P
27128	79	51	004	-	-	P
27128A	93	51	005	-	-	P
27256	93	32	005	-	-	P
Intersil						
6716	59	64	004	-	-	P
Mitsubishi						
2708	21	27	A	-	-	P
8748	52	56	005	351A-070	A	I
2716	19	23	A	-	-	P
2732	19	24	A	-	-	P
2732A	27	24	A	-	-	P
2764	79	33	004	-	-	P
27128	79	51	004	-	-	I

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Monolithic Memories						
5330	29	02	A	-	-	P
5331	29	02	A	-	-	P
53LS080	18	02	004	-	-	O
53LS081	18	02	004	-	-	O
53S080	18	02	004	-	-	O
53S081	18	02	004	-	-	O
6330	29	02	A	-	-	P
6331	29	02	A	-	-	P
63LS080	18	02	004	-	-	P
63LS081	18	02	004	-	-	P
63S080	18	02	004	-	-	P
63S081	18	02	004	-	-	P
5300	11	01	D	-	-	P
5301	11	01	D	-	-	P
6300	11	01	D	-	-	P
6301	11	01	D	-	-	P
63LS140	18	01	004	-	-	P
63LS141	18	01	004	-	-	P
63S140	18	01	004	-	-	P
63S141	18	01	004	-	-	P
5308	11	08	D	-	-	P
5309	11	08	D	-	-	P
5335	11	14	D	-	-	P
5336	11	14	D	-	-	P
6308	11	08	D	-	-	P
6309	11	08	D	-	-	P
6335	11	14	D	-	-	P
6336	11	14	D	-	-	P
5305	11	03	D	-	-	P
5306	11	03	D	-	-	P
6305	11	03	D	-	-	P
6306	11	03	D	-	-	P
63LS240	18	03	004	-	-	P
63LS241	18	03	004	-	-	P
63S240	18	03	004	-	-	P
63S241	18	03	004	-	-	P
5340	11	15	D	-	-	P
5340JS	11	15	003	-	-	P
5341	11	15	D	-	-	P
5341JS	11	15	003	-	-	P
5348	11	09	D	-	-	P
5349	11	09	D	-	-	P
6340	11	15	D	-	-	P
6340JS	11	15	003	-	-	P
6341	11	15	D	-	-	P
6341JS	11	15	003	-	-	P
6348	11	09	D	-	-	P
6349	11	09	D	-	-	P
63S480	18	09	004	-	-	P
63S481	18	09	004	-	-	P
5352	11	05	D	-	-	P
5353	11	05	D	-	-	P
6352	11	05	D	-	-	P
6353	11	05	D	-	-	P
63RA441	18	07	004	-	-	P
63RS441	18	07	005	-	-	P
63S440	18	05	004	-	-	P
63S441	18	05	004	-	-	P
5380	11	16	D	-	-	P
5380JS	11	16	D	-	-	P
5381	11	16	D	-	-	P
5381JS	11	16	D	-	-	P
6380	11	16	D	-	-	P
6380JS	11	16	D	-	-	P
6381	11	16	D	-	-	P
6381JS	11	16	D	-	-	P
63RS881	18	86	005	-	-	P
5388	11	06	D	-	-	P
5389	11	06	D	-	-	P
6388	11	06	D	-	-	P
6389	11	06	D	-	-	P
63RA841	18	11	004	-	-	P
63S840	18	06	004	-	-	P
63S841	18	06	004	-	-	P
1681JS	18	21	004	-	-	P
63S1680	18	21	004	-	-	P
63S1681	18	21	004	-	-	P
63S1640	18	53	004	351A-065	A	P
63S1641	18	53	004	351A-065	A	P
63S3281	18	63	005	-	-	P
Mostek						
2716	19	23	A	-	-	P
Motorola						
7620	05	03	A	-	-	P
7621	05	03	A	-	-	P

Table 1-1. Continued

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Motorola (continued)						
7640	05	15	A	-	-	P
7641	05	15	A	-	-	P
7649	05	09	A	-	-	P
7642	05	05	A	-	-	P
7643	05	05	A	-	-	P
7680	05	16	A	-	-	P
7681	05	16	A	-	-	P
7684	05	06	A	-	-	P
7685	05	06	A	-	-	P
76161	05	21	A	-	-	P
76165	05	53	003	351A-065	A	I
MCM2708P	21	27	A	-	-	O
MCM2808	81	72	003	-	-	P
MCM68708	21	27	A	-	P	
MCM2716	19	23	B	-	-	P
MCM2816	43	23	003	-	-	P
MCM2817	81	71	003	-	-	P
TMS2716	23	28	A	-	-	P
68732-0	25	44	A	-	-	O
68732-1	25	46	A	-	-	O
MCM2532	19	25	B	-	-	P
MCM2832	81	70	003	-	-	P
MCM68764	25	29	F	-	-	P
MCM68766	25	29	F	-	-	P
27C16	19	23	E	-	-	P
25C32	19	25	A	-	-	P
27C32	19	24	A	-	-	P
54S188	08	02	A	-	-	O
54S288	08	02	A	-	-	O
74S188	08	02	A	-	-	P
74S288	08	02	A	-	-	P
54S287	08	01	A	-	-	O
54S387	08	01	A	-	-	O
74S287	08	01	A	-	-	P
74S387	08	01	A	-	-	P
54LS471	08	08	A	-	-	O
54S471	08	08	A	-	-	O
74LS471	08	08	A	-	-	P
74S471	08	08	A	-	-	P
54S570	08	03	A	-	-	O
54S571	08	03	A	-	-	O
74S570	08	03	A	-	-	P
74S571	08	03	A	-	-	P
54S472	08	09	A	-	-	O
54S473	08	09	A	-	-	O
74S472	08	09	A	-	-	P
74S473	08	09	A	-	-	P
74S474	08	15	A	-	-	P
74S475	08	15	A	-	-	P
87S295	08	15	A	-	-	P
87S296	08	15	A	-	-	P
87SR25	08	81	005	-	-	P
54S572	08	05	A	-	-	P
54S573	08	05	A	-	-	P
74S572	08	05	A	-	-	P
74S573	08	05	A	-	-	P
74S574	08	34	A	-	-	P
87LS181	08	16	A	-	-	P
87S180	08	16	A	-	-	P
87S181	08	16	A	-	-	P
87S280	08	16	003	-	-	P
87S281	08	16	003	-	-	P
87S184	08	06	A	-	-	P
87S185	08	06	A	-	-	P
87S190	08	21	A	-	-	P
87S191	08	21	A	-	-	P
87S290	08	21	003	-	-	P
87S291	08	21	003	-	-	P
87S195	08	53	004	-	-	P
87S321	08	63	004	-	-	P
2708	21	27	A	-	-	P
2758A	19	22	A	-	-	P
2758B	19	35	A	-	-	P
2716	19	23	A	-	-	P
2816	37	23	003	-	-	P
9716	83	23	005	-	-	P
2532	19	25	A	-	-	P
2732	19	24	A	-	-	P
2764	36	33	F	-	-	I
Nippon Electronic Company, Ltd.						
8741AD	56	59	005	351A-070	A	I
8748AD	52	56	005	351A-070	A	I
2716	19	23	F	-	-	P
8755A	47	55	005	351A-072	A	I
2732	19	24	F	-	-	P

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Nippon Electronic Company, Ltd. (continued)						
2732A	27	24	A	-	-	P
2764	79	33	004	-	-	I
27128	79	51	004	-	-	I
Oki						
2708	21	27	A	-	-	P
2758	19	22	A	-	-	P
2716	19	23	A	-	-	P
8755A	47	55	005	351A-072	A	I
2532	19	25	A	-	-	P
2732	19	24	A	-	-	P
2732A	27	24	A	-	-	P
2764	79	33	004	-	-	I
27128	79	51	004	-	-	I
Raytheon						
29660	11	01	D	-	-	P
29661	11	01	D	-	-	P
29662	11	01	D	-	-	P
29663	11	01	D	-	-	P
29600	11	08	D	-	-	P
29601	11	08	D	-	-	P
29602	11	08	D	-	-	P
29603	11	08	D	-	-	P
29610	11	03	D	-	-	P
29611	11	03	D	-	-	P
29612	11	03	D	-	-	P
29613	11	03	D	-	-	P
29620	11	09	D	-	-	P
29621	11	09	D	-	-	P
29622	11	09	D	-	-	P
29623	11	09	D	-	-	P
29624	11	15	D	-	-	P
29625	11	15	D	-	-	P
29626	11	15	D	-	-	P
29627	11	15	D	-	-	P
29630	11	16	D	-	-	P
29630SM	11	16	003	-	-	P
29631	11	16	D	-	-	P
29631SM	11	16	003	-	-	P
29632	11	16	D	-	-	P
29632SM	11	16	003	-	-	P
29633	11	16	D	-	-	P
29633SM	11	16	003	-	-	P
29634	11	16	D	-	-	P
29635	11	16	D	-	-	P
29636	11	16	D	-	-	P
29637	11	16	D	-	-	P
29650	11	06	D	-	-	P
29651	11	06	D	-	-	P
29652	11	06	D	-	-	P
29653	11	06	D	-	-	P
29680	11	21	D	-	-	P
29680SM	11	21	003	-	-	P
29681	11	21	D	-	-	P
29681SM	11	21	003	-	-	P
29682	11	21	D	-	-	P
29682SM	11	21	003	-	-	P
29683	11	21	D	-	-	P
29683SM	11	21	003	-	-	P
29640	11	53	004	351A-065	A	P
29641	11	53	004	351A-065	A	P
29642	11	53	004	351A-065	A	P
29643	11	53	004	351A-065	A	P
29671	11	63	H	-	-	P
29673	11	63	H	-	-	P
Ricoh						
RD5H32	27	24	F	-	-	P
Seeq						
5133	35	33	005	-	-	P
5133H	79	33	005	-	-	P
5143	79	51	005	-	-	I
SGS Technology						
2716	19	23	A	-	-	P
2732	19	24	F	-	-	P
Signetics						
82123	10	02	A	-	-	P
82S123	10	02	A	-	-	P
82S23	10	02	A	-	-	P
82S126	10	01	A	-	-	P
82S129	10	01	A	-	-	P
82LS136	10	08	A	-	-	P

Table 1-1. Continued

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Signetics (continued)						
82S114	AE	84	005	351A-068	A	I
82S135	10	08	A	-	-	P
82S130	10	03	A	-	-	P
82S131	10	03	A	-	-	P
82S115	AE	83	005	351A-068	A	I
82S140	10	15	A	-	-	P
82S141	10	15	A	-	-	P
82S146	10	09	A	-	-	P
82S147	10	09	A	-	-	P
82LS137	10	05	A	-	-	P
82S136	10	05	A	-	-	P
82S137	10	05	A	-	-	P
82LS180	10	16	A	-	-	P
82LS181	10	16	003	-	-	P
82PS180	10	16	A	-	-	P
82PS181	10	16	003	-	-	P
82S180	10	16	A	-	-	P
82S181	10	16	A	-	-	P
82S182	10	16	A	-	-	P
82S183	10	16	A	-	-	P
82S2708	10	16	A	-	-	P
82S184	10	06	A	-	-	P
82S185	10	06	A	-	-	P
82S190	10	21	A	-	-	P
82S191	10	21	A	-	-	P
82S195	10	53	004	351A-065	A	P
82S321	10	63	004	-	-	P
2708	21	27	A	-	-	P
Synertek						
2716	19	23	A	-	-	P
Thompson						
71190	92	21	004	-	-	P
71191	92	21	004	-	-	P
Texas Instruments						
18S030	04	02	A	-	-	P
18SA030	04	02	A	-	-	P
74188A	04	02	A	-	-	O
74S188	04	02	A	-	-	O
74S288	04	02	A	-	-	O
14S10	03	01	A	-	-	P
14SA10	03	01	A	-	-	P
24S10	13	01	A	-	-	P
24SA10	13	01	A	-	-	P
74S287	03	01	A	-	-	O
74S387	03	01	A	-	-	O
18S22	04	08	A	-	-	P
18SA22	04	08	A	-	-	P
28L22	13	46	G	-	-	P
28LA22	13	46	G	-	-	P
74S470	04	08	A	-	-	O
74S471	04	08	A	-	-	O
18S42	04	09	A	-	-	P
18S46	04	15	A	-	-	P
18SA42	04	09	A	-	-	P
18SA46	04	15	A	-	-	P
28L42	13	09	G	-	-	P
28L45	13	15	G	-	-	I
28P42	13	09	G	-	-	I
28P45	13	15	G	-	-	I

Device Part No.	Family Code	Pinout Code	Software Version	Socket Adapter	Socket Adapter Revision	Notes
Texas Instruments (continued)						
→ 28S42	13	09	A	-	-	P
28S45	13	15	G	-	-	P
28S46	13	15	G	-	-	P
28SA42	13	09	G	-	-	P
28SA46	13	15	G	-	-	P
74S472	04	09	A	-	-	O
74S473	04	09	A	-	-	O
74S474	04	15	A	-	-	O
74S475	04	15	A	-	-	O
24S41	13	38	A	-	-	P
24SA41	13	38	A	-	-	P
74S476	13	38	A	-	-	O
74S477	13	38	A	-	-	O
28L85	13	16	G	-	-	I
28L86	13	16	A	-	-	P
28P85	13	16	G	-	-	I
28S2708	13	16	A	-	-	P
28S85	13	16	G	-	-	I
28S86	13	16	A	-	-	P
28SA86	13	16	A	-	-	P
54LS478	13	16	A	-	-	O
74S2708	13	16	A	-	-	O
74S478	13	16	A	-	-	O
74S479	13	16	A	-	-	O
24S81	13	06	A	-	-	P
24SA81	13	06	A	-	-	P
74S454	13	06	A	-	-	O
74S455	13	06	A	-	-	O
28L166	13	21	G	-	-	P
28P166	13	21	G	-	-	I
28S166	13	21	G	-	-	P
28SA166	13	21	G	-	-	I
24S166	13	53	005	351A-065	A	I
24SA166	13	53	005	351A-065	A	I
2508	19	22	A	-	-	P
2708	21	27	A	-	-	P
27L08	21	27	A	-	-	P
2516	31	23	005	-	-	P
TMS2716	23	28	A	-	-	P
2532	31	25	005	-	-	P
25L32	19	25	A	-	-	P
2732	31	24	005	-	-	P
2732A	27	24	A	-	-	P
2564	31	30	G	-	-	P
2764	35	33	F	-	-	P
27128	31	51	005	-	-	I
Toshiba						
321	21	26	A	-	-	P
322	21	27	A	-	-	P
323	19	23	A	-	-	P
8755AC	47	55	005	351A-072	A	I
2732	19	24	A	-	-	P
2732A	27	24	A	-	-	P
2732D	19	24	A	-	-	P
2764	79	33	004	-	-	I
27128	79	51	004	-	-	I
Xicor						
2804	37	82	005	-	-	P
2816	37	23	005	-	-	P

Table 1-2. Specifications

Weight	1.38 kg (3 lb. .5 oz.)	**Operating-Temperature Range**	0 to 40°C (32 to 104°F)
Dimensions	20.9 cm x 17.0 cm x 10.5 cm (8.2″ x 6.7″ x 4.2″)	**Storage-Temperature Range**	−40 to 55°C (−40 to 131°F)

SECTION 2
INSTALLATION

2.1 INSPECTION

The UniPak was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should therefore arrive free of any defect, without marks or scratches, and in perfect operating condition. Carefully inspect the instrument for any damage that may have occurred in transit; if you note any damage, file a claim with the carrier and notify Data I/O.

2.2 ASSEMBLY AND DISASSEMBLY

The top cover and card carrier normally remain attached, but for calibration they detach as shown in Figure 2-1. To reattach them, insert the flanges on the upper edges of the top cover and card carrier into each other. Then press them together and tighten the captive fasteners.

The UniPak is mounted on the programmer in the same way as a standard Programming Pak. If a Programming Pak is installed, remove it by pulling the handle to separate the mating connectors and then lifting it out.

Figure 2-1. Interconnection of the Top Cover and Card Carrier

2.3 INSTALLING THE UniPak

CAUTION

Be sure that all sockets are empty when installing or removing the UniPak.

Install the UniPak by inserting the flange on the top edge of the UniPak around the top edge of the opening and pressing firmly to ensure mating of the connectors on the two units.

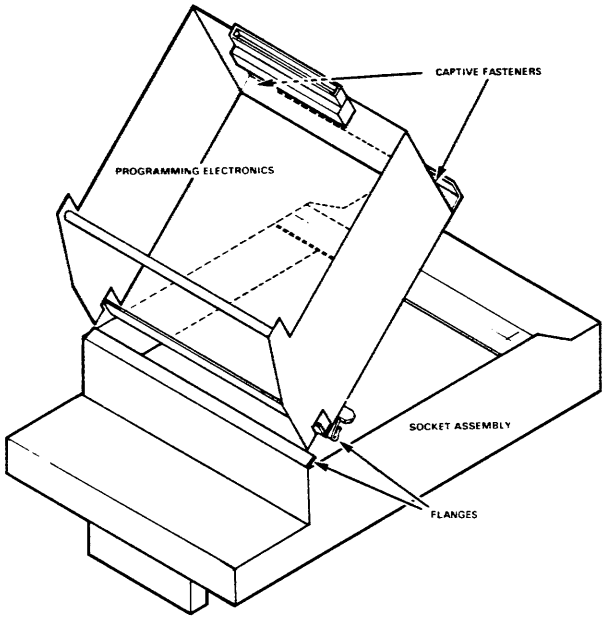


Figure 2-1. Interconnection of the Top Cover and Card Carrier

2.4 REPACKAGING FOR SHIPMENT

If the UniPak is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by serial number, model number, and name.

If the original shipping container is to be used, place the UniPak in the container with appropriate packing material and seal the container well with strong tape. If some other container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 INTRODUCTION

This section explains steps in preparing the UniPak for operations with a particular device.

CAUTION

Follow the procedures in this section carefully to avoid damage to the programmer, the UniPak, or devices to be programmed.

3.2 POWER-UP

Install the UniPak according to the procedure in section 2.3. On power-up, the programmer performs an automatic self-test routine, signalling you when it is functional. Each programmer signals readiness in a different way; consult your programmer manual.

The UniPak may be installed and removed with the programmer's power on. This feature allows you to retain data in RAM during equipment changes.

CAUTION

Voltage transients can cause damage. Be sure that all sockets are empty when:

1. **switching power on or off**
   or
2. **installing or removing the UniPak**

3.3 DEVICE SELECTION

With the UniPak, device selection must always precede device-related operations. Any device in the UniPak's repertoire is specified by a unique combination of a 2-digit Family Code and a 2-digit Pinout Code. Once the codes are entered for a particular device, the UniPak remains adapted for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the Family and Pinout Codes should be entered. If unacceptable Family and Pinout Codes are entered, a beep will sound as either START or ENTER is pressed; the operation will be stopped.

3.4 SELECT FUNCTIONS

Extended Select Functions CE and CF are used to set the reject count — the number of programming pulses applied to a fuse before it is rejected.

- **CE** sets the commercial reject count. This is the default value.

- **CF** sets the single pulse reject count.

NOTE

This feature was accomplished in previous configurations of the UniPak by adding 50 to the commercial Family Code.

- **EF** displays the configuration number of the UniPak software.

Consult your programmer manual for the key sequences for entering Select Functions.

3.5 DEVICE INSERTION

Once the appropriate Family and Pinout Codes have been chosen, the UniPak is ready to accept a device in the socket indicated by the illuminated LED.

CAUTION

1. **Do not insert a device into a socket if the socket LED is not illuminated.**

2. **Never insert more than one device in the UniPak.**

A good electrical connection between the device and socket is essential. Insert the device in the socket with the lever in the upright position, ensuring that pin 1 is aligned with pin 1 of the socket. Lock the device in the socket by pushing the lever down.

CAUTION

Never insert or extract a device when the START light is on.

3.6 LOAD, PROGRAM AND VERIFY

Once the Family and Pinout Codes have been entered, the UniPak is ready for device-related operations. The codes remain in effect until they are changed or until power is removed. Load, Program, and Verify operations may be executed normally.

During each operation, the UniPak performs automatic parametric tests of the device. Tests, consisting of comparisons of the device data and RAM data, are performed at various Vcc levels, output-sink currents, and output-level-sense voltages, according to specific manufacturers' requirements.

In the Load mode, the nominal Vcc level, with a 1.6 mA current source on each output, is applied to the device. The sense threshold is 1.6 volts.

In the Program mode, illegal bit tests and blank checks are performed at nominal Vcc and with nominal output loading. Programming is done according to manufacturer's specifications. The first- and second-pass verifies are

performed at parametric levels indicated in steps 15 and 16 of the Measurement Chart, respectively.

In the Verify mode, the two verify passes are done in the same way.

NOTE

Valid Family and Pinout Codes must be in effect to use the System 19 DEVICE DATA key. When the DEVICE DATA key is pressed, either nominal, first-pass, or second-pass verify levels are applied to the device. The level applied depends on the 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration of the UniPak is recommended whenever programming yields fall below the device manufacturers' minimum specifications.

Calibration consists of 3 parts:

1. **Power Supply Calibration.** These are measurements of the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part must be done first.

2. **DC Calibration.** This consists of measuring and adjusting other critical DC voltage levels generated by the UniPak.

3. **Waveform Observation.** Programming waveforms can be observed on an oscilloscope for compliance with the device manufacturers' critical voltage and timing specifications.

A performance check can be done to determine if your UniPak requires a complete, three-part calibration. The performance check consists of performing the tests noted on the Measurement Chart in order. Some tests, as noted on the chart may be skipped. If the performance check yields voltages within the specified range, all supplies and drivers will have been tested and the UniPak is ready for programming. During a performance check, the UniPak can remain installed as for normal operation.

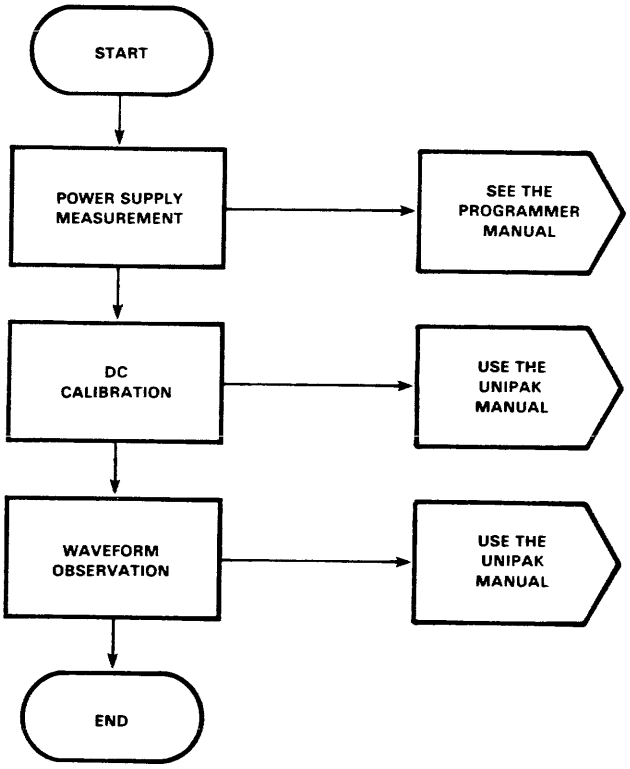


Figure 4-1. Calibration

4.1.1 USE OF THE MANUAL IN CALIBRATION

Because of the different possible combinations of programmers and programming modules, this manual does not attempt to cover all areas of calibration. Instead, it lists the steps necessary to calibrate the UniPak. For information on how to carry out these steps on various programmers, consult the programmer's O & M manual. The programmer manual will be used for Part 1 of calibration, and this manual for Parts 2 and 3. See Figure 4-1.

4.1.2 REQUIRED EQUIPMENT

The following equipment is necessary to calibrate the UniPak.

- Data I/O Calibration Extender, part number 910-1521
- Digital Voltmeter (Fluke 8000A or equivalent)
- Dual-trace Oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that may be necessary to calibrate the programmer.

4.2 THE MEASUREMENT CHART

The Measurement Chart contains the information necessary for all DC calibration tests. The information is presented as follows:

- The **STEP NO.** column tells which step to use for each test. Step numbers are set at the programmer keyboard.
- The **TEST NO.** column identifies individual tests.
- The **TEST DESCRIPTION** column identifies the functions being tested.
- The **TEST LOCATION** column tells which socket pins or test points to probe for measuring voltages.
- **The VOLTAGE** columns specify allowable voltage ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak until the problem is corrected.
- The **ADJUSTMENT LOCATION** column tells which potentiometer to adjust if a voltage is out of range.
- The **COMMENTS** column gives special instructions for particular tests.

4.3 CALIBRATION PROCEDURE

The following paragraphs describe how to calibrate the UniPak.

4.3.1 POWER SUPPLY MEASUREMENTS

Follow the procedures for power supply measurements in the appropriate programmer manual.

4.3.2 EQUIPMENT SET-UP

Set-up the equipment according to the following procedures. Figure 4-2 shows the calibration set-up.

1. Turn power off.

2. Remove the UniPak from the programmer by lifting the handle gently, separating the mating connectors, and then lifting it out.

3. Unscrew the 2 captive fasteners located on the underside of the top cover; they connect the UniPak to the top cover. Separate the 2 parts of the assembly.

CAUTION

Do not let the fasteners short to the Motherboard. (part number 702-1999)

4. Insert the Calibration Extender the same way as the UniPak, being sure to seat it properly in the programmer's mating connector.

5. Insert the 64-pin connector of the UniPak into the mating connector on the Calibration Extender.

4.3.3 DC CALIBRATION

DC calibration procedures are as follows:

1. Install the UniPak as described in section 4.3.2 and power up.

2. Put the programmer into the calibration mode as described in the programmer manual.

3. Follow the steps on the Measurement Chart in order. Voltage readings are made at the device sockets. Figure 4-3 shows pin numbers for these sockets.

4. Adjustment pots are located on the Waveform Generator and Address Cards. These pots are accessible when the UniPak is installed in the Calibration Extender. Figure 4-4 shows the location of these adjustment points.

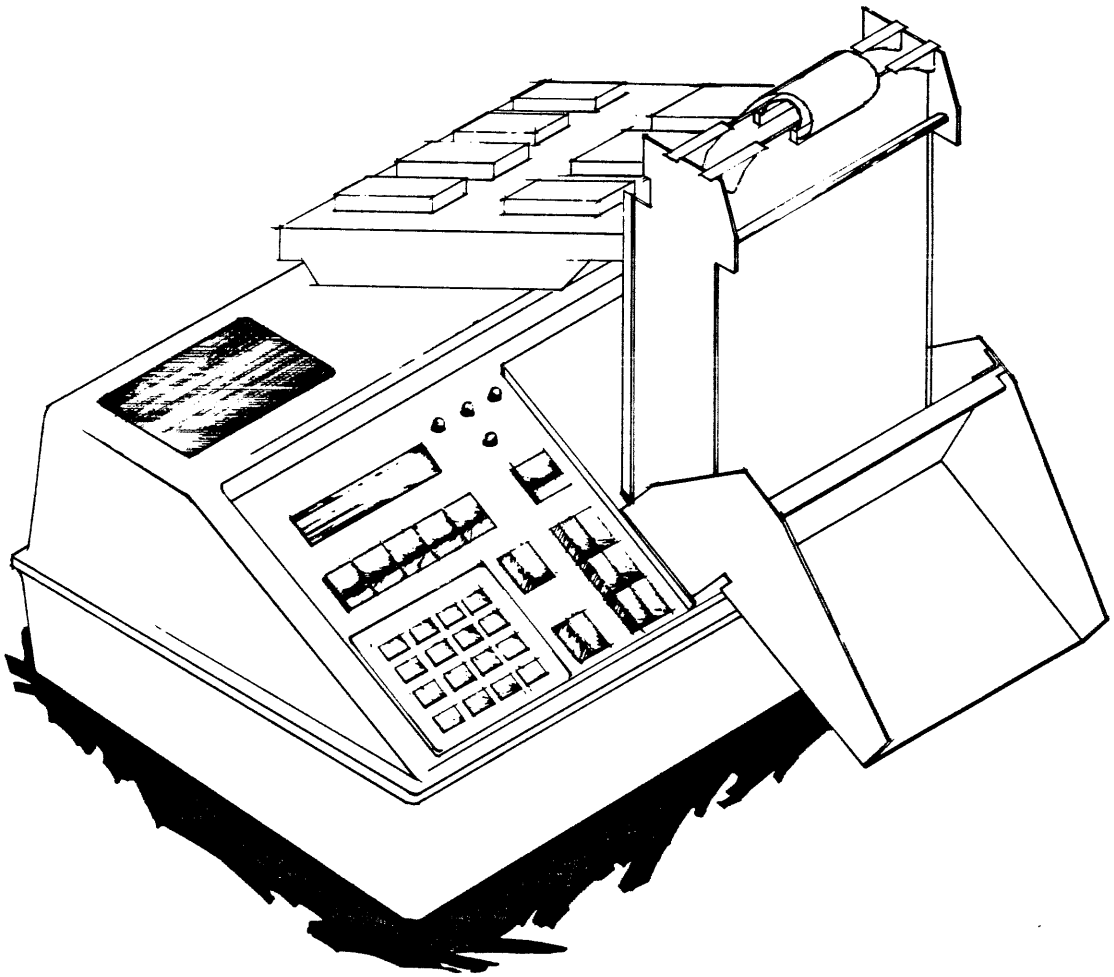


Figure 4-2. Calibration Set-up

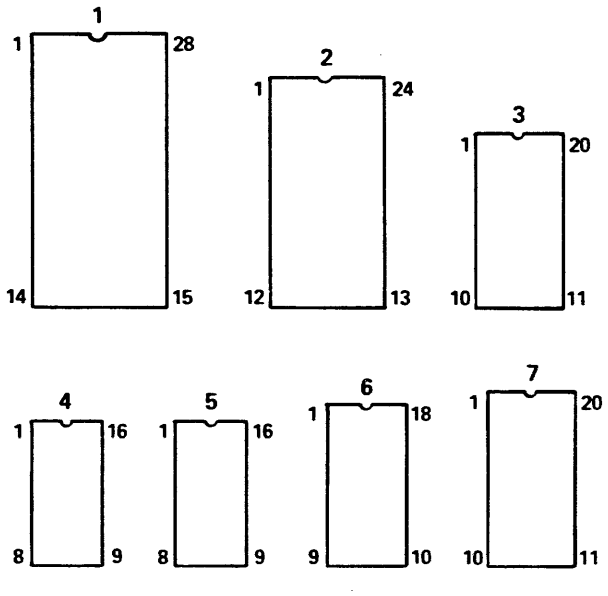


Figure 4-3. Pin Numbers of Device Sockets

4.3.4 OPTIONAL VERIFY-VOLTAGE CHECKS

Two calibration steps, 15 and 16, have been provided for the measurement of first and second pass verify voltages. The Measurement Chart defines the levels for first and second pass verifications for each family. These are provided for the investigation of yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

4.4 WAVEFORM OBSERVATION

Programming waveforms can be observed with an oscilloscope and compared with the Timing Diagrams. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the UniPak is performing to the device manufacturers' standards.

Since the UniPak generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, it is only necessary to observe waveforms for commonly used devices or those that are presenting yield problems.

4.4.1 THE TIMING SEQUENCE

Waveform observation uses a software routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated every address increment. This occurs after the reject pulse count has been reached for all the bits being programmed in the previous data word. The address is automatically reset to Ø when the maximum PROM address is reached, and incrementing continues.

The waveform observation procedure, paragraph 4.4.3, calls for filling RAM with data such that it is possible to observe address-change waveforms and bit-to-program waveforms. The procedure takes into account the device type (VOL or VOH) so that for either type of PROM a bit-to-program will appear on the same socket contact.

4.4.2 THE TIMING DIAGRAMS

This manual contains a Timing Diagram for each device family programmed by the UniPak. Each Timing Diagram contains a set of waveform photographs that show critical programming parameters. The minimum and maximum parameter values are listed in the waveform variables tables on the diagrams. Other voltage and timing parameters are to be considered noncritical, with a tolerance of 10%.

Horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. It can be adjusted on the oscilloscope to set convenient reference points; by taking into account any time-base variance, time comparisons can be made between photographs. (The time base is always the same for different waveforms in the same photograph.) Time-base and volts-per-division settings are printed on each photograph.

The waveform names are called out along the left edge of each photograph. Waveform names correspond to the pin names on the Pinout Charts, Figure 4-5. These charts tell which socket contacts to probe when observing the waveforms for a particular device pinout within a family.

The bit-to-program and $A_Ø$ waveforms shown are usually for 4-bit-devices. If an 8-bit pinout is chosen for observation, the time between $A_Ø$ transitions should be doubled to account for the 4 additional bits programmed at each word. Using the oscilloscope's single sweep mode is recommended for address observation, since one trigger pulse is generated for each address change.

NOTE

When RAM is filled with the data in Table 4-1 according to the procedure in the programmer manual, a bit-to-program may be observed on output O_4 (4-bit device) or O_8 (8-bit device), and a no-bit-to-program may be observed on output O_3 (4-bit device) or O_7 (8-bit device).

Detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train. The delay time is printed at the bottom right of each detailed photograph.

4.4.3 OBSERVATION PROCEDURE

This procedure, when used with a Timing Diagram, allows you to compare waveforms on the oscilloscope with the waveform photographs on the Timing Diagram for any type of device. The procedure is as follows:

1. Refer to Table 1-1 to determine the Family and Pinout Codes, polarity, and technology of the selected device

NOTE

Polarity is indicated in the Family Code. Odd numbered families are VOL and even numbered families are VOH.

2. Initiate a Load operation.

3. Key in the Family and Pinout Codes.

4. Fill the programmer's RAM with programming data according to procedures given in the Operation section of the appropriate programmer manual. The correct data depends on the polarity and technology of the device. This data is listed in Table 4-1.

CAUTION

Remove all devices before entering calibration. Waveform generation may damage any device in the UniPak.

5. Enter Waveform generation at step 17. Refer to the programmer manual for the procedure.

6. Prepare the oscilloscope by connecting TP1 on the Address and Data Driver board to the trigger input.

7. Ground the scope to the GND contact of the socket with its LED illuminated (Refer to Figure 4-5.)

8. To observe individual waveforms, refer to Figure 4-5 under the Pinout Code number entered in step 3. The charts give the numbers of the socket contacts to probe when observing the waveforms on the Timing Diagram.

NOTE

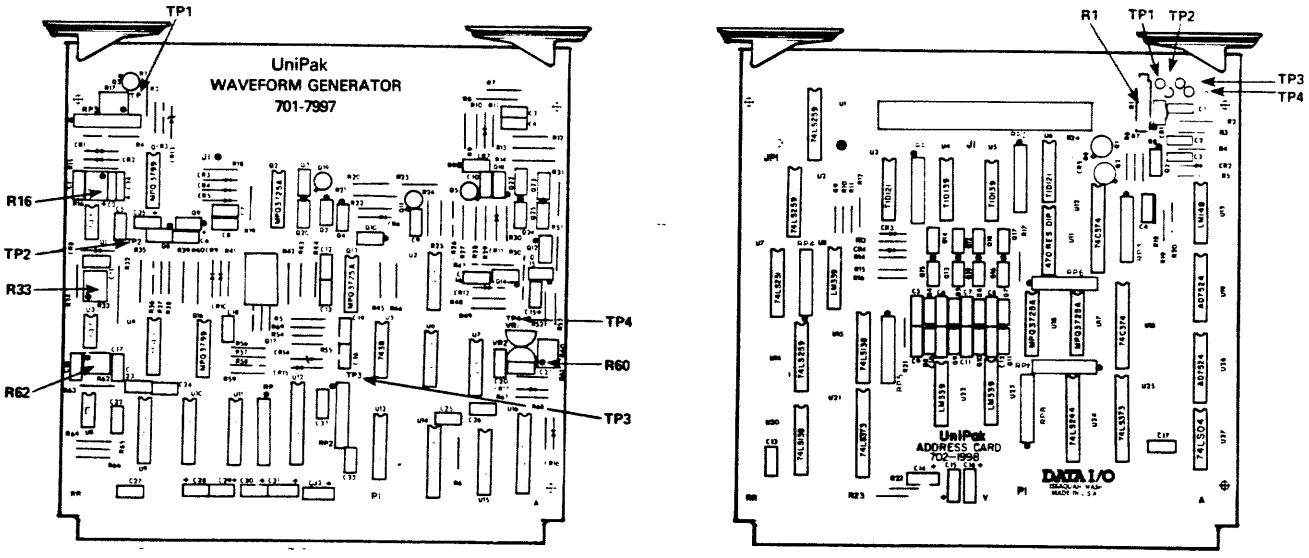
Paragraph 4.4.2 explains considerations helpful in setting up and interpreting the waveform displays.

Table 4-1. RAM Data for Waveform Observation

TYPE OF DEVICE	POLARITY	DATA IN EVERY ADDRESS
MOS PROMs	VOL	Hex 55
MOS PROMs	VOH	Hex AA
Bipolar PROMs	VOL	Hex 00
Bipolar PROMs	VOH	Hex FF

4.4.4 ERASE WAVEFORMS

The UniPak generates waveforms to erase many Electrically Erasable or Alterable PROMs. These waveforms may be observed by following the procedure in section 4.4.3 for programming waveform observations. Chip-erase waveforms can be viewed by entering calibration step 19, and byte-erase waveforms can be viewed in step 21. If step 19 is entered with other than an EEPROM family selected, it will result in an invalid family/pinout error (Error 30). If a family is selected that cannot be byte-erased, the UniPak will respond with Error B0.



a. Waveform Generator, 701-7997

b. Address Card, 702-1998

Figure 4-4. Adjustment Locations

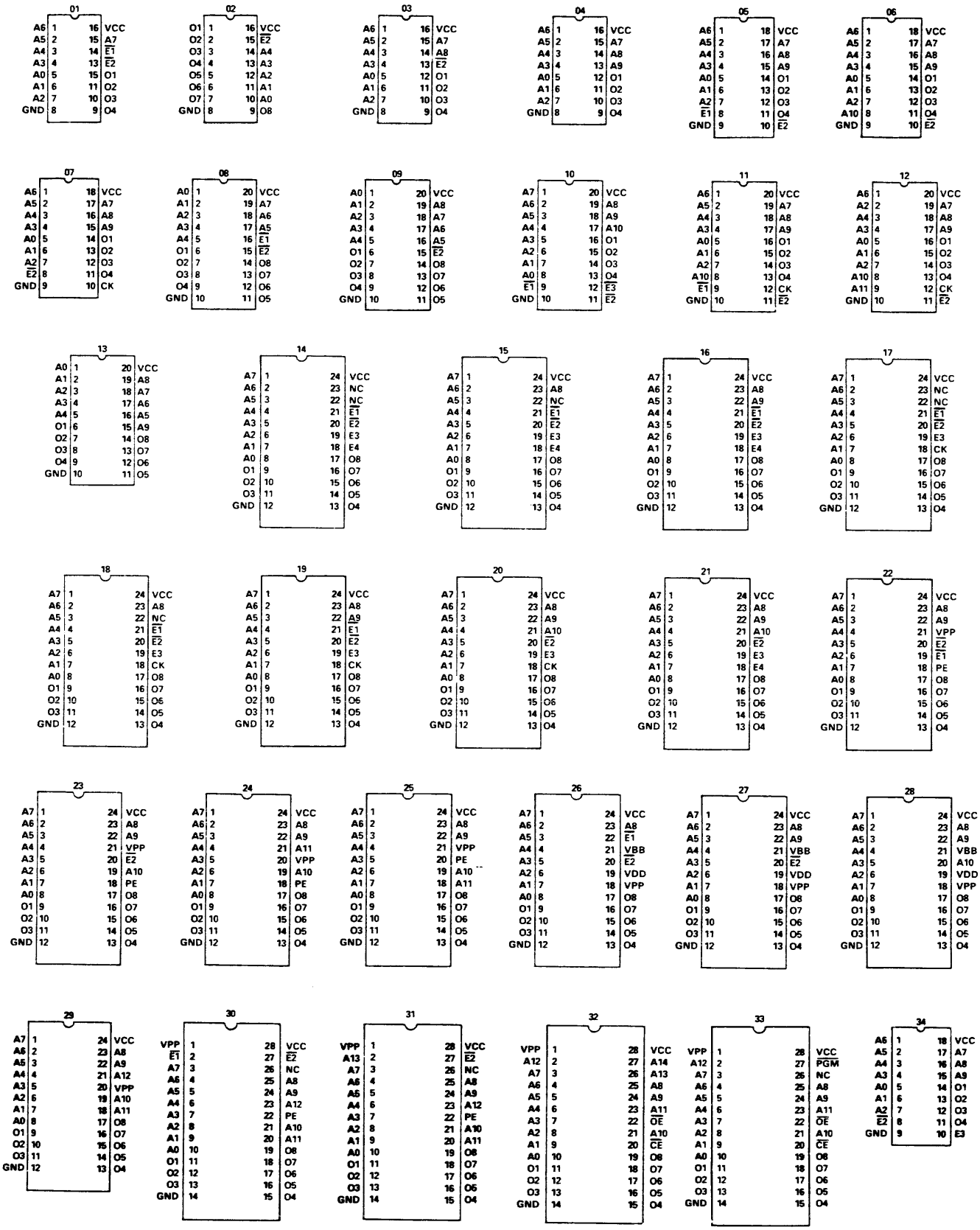


Figure 4-5. Pin Names by Pinout Code Numbers

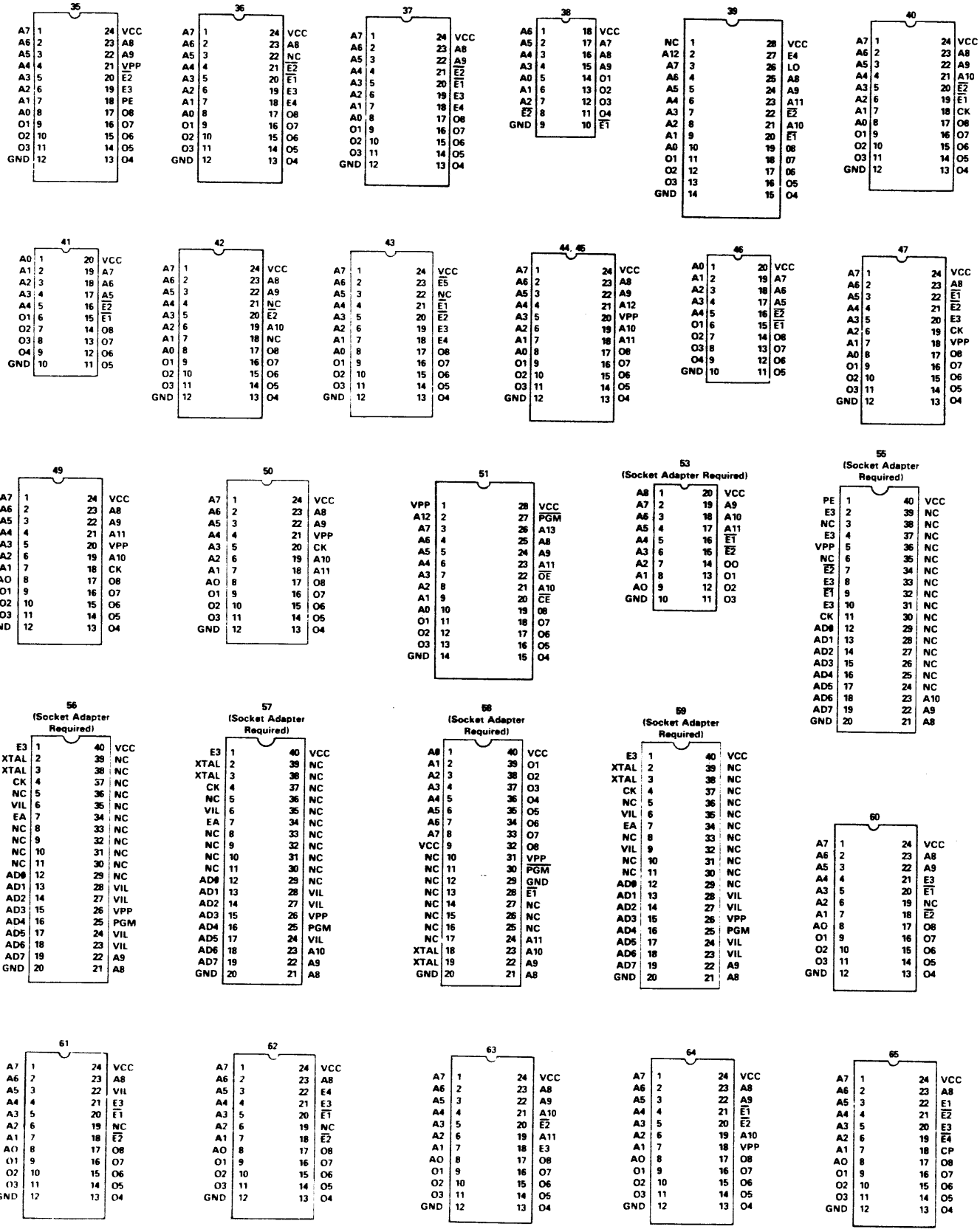


Figure 4-5. Continued

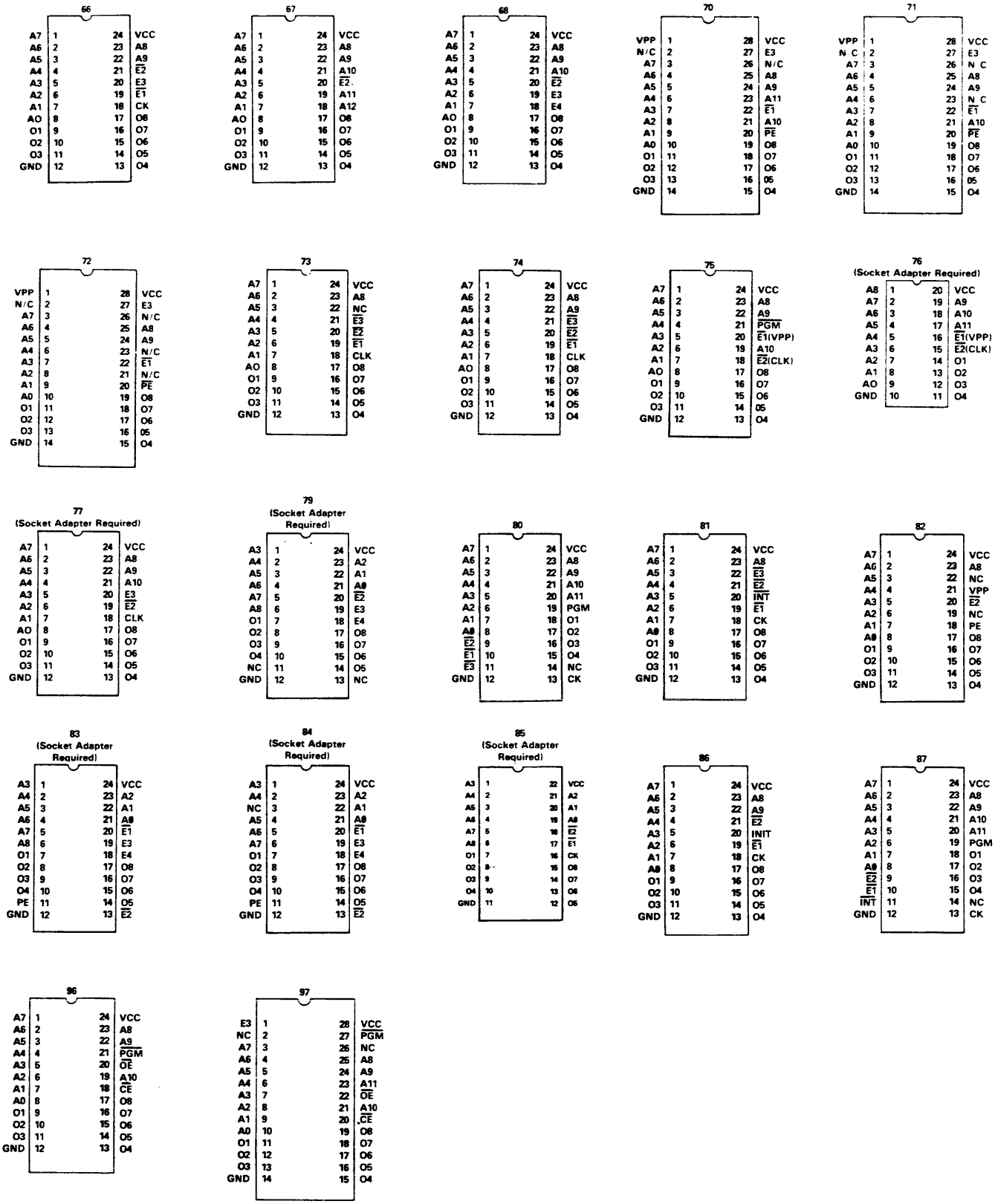


Figure 4-5. Continued

Figure 4-3. Measurement Chart

DATE	REV	REVISION RECORD	DR	CK
6-2-82	A	RELEASE PER ECN #4564	EF	GB
7-21-82	B	ECN #4667	EF	
12-22-82	C	ECN #4728	CH	
5-83		ECN 4803		

UNIPAK MEASUREMENT CHART
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
1	1	All Voltages Off	All/All	-0.1		-0.4		
	2	Socket 2 LED	2 /NA					Confirm that Socket 2 LED is on.[a]
2	3	V Reference DAC	701-1998/ TP4	10.20	10.24	10.28	R1,701-1998	Skip this test for performance
								check.
	4	Supply Reference	701-7997/ TP4	4.98	5.00	5.02	R60,701-7997	Skip this test for performance
								check.
	5	Current Source 1 Supply	701-1998/ TP3	24.35		25.7		Skip this test for performance
								check.
	6	Current Source 2 Supply	701-1998/ TP2	24.3		25.7		Skip this test for performance
								check.
	7	VCC Voltage	2 /24	11.95	12.00	12.05	R62,701-7997	
	8	CE Voltage	2 /20	32.7	33.0	33.2	R16,701-7997	
	9	CE Load	2 /20	32.5		33.2		Load with 100 ohm 5 W resistor
								between pin 20 and pin 12,
								socket 2.
								CAUTION[b]
								Skip this test for performance
								check.
	10	CE Voltage Switch	2 /18	32.7	33.0	33.2		
	11	CE Voltage Switch	2 /21, 1 /26	32.7	33.0	33.2		

[a]Do not leave programmer unattended in calibration mode Step 1.
[b]Remove load immediately after making reading, or return to Step 1.

Figure 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
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UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	12	Bit Supply & Data Switch	2 /9, 11, 14, 16	25.9	26.0	26.1	R33,701-7997	
	13	Bit Load	2 /11	25.5		26.1		Load with 100 ohm 5 W resistor
								between pin 11 and pin 12,
								socket 2.
								CAUTION[a]
								Skip this test for performance
								check.
	14	Bit Supply & Data Switch	2 /10, 13, 15, 17	4.6		5.9		
3	15	Socket 4 LED	4 /NA					Confirm that Socket 4 LED is on.
	16	VCC Voltage	4 /16	11.9		12.1		
	17	Bit Supply & Data Switch	4 /1,3,5,7	4.6		5.9		
	18	Bit Supply & Data Switch	4 /2,4,6,9	25.6		26.2		
4	19	Socket 5 LED	5 /NA					Confirm that Socket 5 LED is on.
	20	VCC Voltage	5 /16	11.9		12.1		
5	21	Socket 6 LED	6 /NA					Confirm that Socket 6 LED is on.
	22	VCC Voltage	6 /18	11.9		12.1		
6	23	Socket 7 LED	7 /NA					Confirm that Socket 7 LED is on.
	24	VCC Voltage	7 /20	11.9		12.1		
	25	I Source & Pulldowns	7 /6,7,8,9,11	2.0		2.6		

[a]Remove load immediately after making reading, or return to Step 1.

Figure 4-3. Measurement Chart (Continued)

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LTR	DESCRIPTION	P.E.	DATE
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UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
7	26	Socket 3 LED	3 /NA					Confirm that Socket 3 is on.
	27	VCC Voltage	3/ 20	11.9		12.1		
8	28	Socket 1 LED	1/ NA					Confirm that Socket 1 is on.
	29	VCC Voltage	1/ 28	11.9		12.1		
	30	I Source & Pulldowns	1/ 11,12, 13,15,16,17,18,19	2.0		2.6		
	31	VCC Load	1/ 28	11.8		12.1		Load with a 20 ohm 2 watt resistor
								between pin 28 and pin 14,
								socket 1.
								CAUTION [a]
								Skip this test for performance
								check.
9	32	V Reference Linearity	701-1998 /TP4	6.75		6.85		Skip this test for performance
								check.
	33	I Source Linearity	701-1998 /TP2,3	22.5		24.0		Skip this test for performance
								check.
	34	VCC Voltage Linearity	2/ 24	9.95		10.05		Skip this test for performance
								check.
	35	CE Voltage Linearity	2/ 20	23.00		23.50		Load 2.2K ohm, 1/2W resistor, pin
								12 to 20, socket 2.

[a]Remove load immediately after making reading, or return to Step 1.

Figure 4-3. Measurement Chart (Continued)

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LTR	DESCRIPTION	P.E	DATE
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UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
	36	Bit Supply Linearity	2/ 9	23.2		23.6		Ground DVM to Socket 7, Pin 10.
	37	-5 Volt Supply	2/ 21, 1/26	-5.2		-4.8		
	38	Pin 18 Switch	2/ 18	-0.1		0.4		
	39	Pin 19 Switch Off	2/ 19	-0.1		0.4		
10	40	VCC Voltage Linearity	2/ 24	4.95		5.05		
	41	CE Voltage Linearity	2/ 20	11.40		12.00		Load 2.2K ohm, socket 2 pin 12
								to 20.
	42	Bit Supply Linearity	2/ 9	11.50		11.80		
	43	Pin 19 Switch On	2/ 19	11.0		11.4		
	44	V Reference Linearity	701-1998 /TP4	3.35		3.45		Skip this test for performance
								check.
	45	I Source Linearity	701-1998/ TP2,3	11.2		12.0		Skip this test for performance
11	46	12 Volt Supply	2/ 20	11.4		12.6		check.
12	47	Odd Address, Controls,	1/ 1,2,3,5,7,9,12,15,	3.0		5.9		
		& Data High	17,19,20,22,24,26					
	48	Even Address & Data Low	1/ 4,6, 8,10,11, 13,16	-0.1		0.4		
			18,21,23,25,27					
13	49	Odd Address, Controls,	1/ 1,2,3,5,7,9,12,15,	-0.1		0.4		
		& Data Low	17, 19, 20, 22, 24, 26					

Figure 4-3. Measurement Chart (Continued)

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LTR	DESCRIPTION	P.E.	DATE
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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM Socket 7, Pin 10.
	50	Even Address & Data High	1 /4,6,8,10,11,13	3.0		5.9		
			16,18,21,23,25,27					
14	51	VCC Pullups On	1 /28	4.0		5.2		
	52	VCC Pullups On	2 /24	4.0		5.2		
	53	VCC Pullups On	3 /20	4.0		5.2		
	54	VCC Pullups On	7 /20	4.0		5.2		
	55	VCC Pullups On	6 /18	4.0		5.2		
	56	VCC Pullups On	5 /16	4.0		5.2		
	57	VCC Pullups On	4 /16	4.0		5.2		
			Steps 15 and 16 are optional parametric tests. For each pair of steps, select valid					
			Family and Pinout Codes. There are no adjustments and the tests may be skipped					in calibration.
15	58	Family 01,02 Ver., 1st	* /VCC	4.4		4.6		* Use socket with LED on.
		Pass						
	59	V Ref.	701-1998 / TP4	0.8		1.0		
	60	I Source 1	701-1998 / TP2	6.9		7.9		Nominal currents (I Source 1 plus
								I Source 2) is 3.5 mA.
	61	I Source 2	701-1998 / TP3	6.9		7.9		
	64	I Source 1	701-1998 / TP2	6.9		7.9		Nominal current (I Source 1 plus
								I Source 2) is 3.5mA.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM Socket 7, Pin 10.
	65	I Source 2	701-1998 / TP3	6.9		7.9		
15	66	Family 03,04 Ver., 1st	* /VCC	4.4		4.6		*Use socket with LED on.
		Pass						
	67	V Ref.	701-1998 / TP4	0.8		1.0		
	68	I Source 1	701-1998 / TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 1.0 mA.
	69	I Source 2	701-1998 / TP3	11.2		12.2		
16	70	Family 03,04 Ver., 2nd	* /VCC	5.4		5.6		*Use socket with LED on.
		Pass						
	71	V Ref.	701-1998 / TP4	1.6		1.8		
	72	I Source 1	701-1998 / TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.7 mA.
	73	I Source 2	701-1998 / TP3	8.9		9.9		
15	74	Family 05,06 Ver., 1st	* /VCC	4.4		4.6		*Use socket with LED on.
		Pass						
	75	V Ref.	701-1998 / TP4	0.8		1.0		
	76	I Source 1	701-1998 / TP2	15.5		16.5		Nominal current (I Source 1 plus
								I Source 2) is 8.6 mA.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
	77	I Source 2	701-1998/ TP3	15.5		16.5		Ground DVM to Socket 7, Pin 10.
16	78	Family 05, 06 Ver., 2nd	* /VCC	5.4		5.5		*Use socket with LED on.
		Pass						
	79	V Ref.	701-1998/ TP4	1.6		1.8		
	80	I Source I	701-1998/ TP2	12.4		13.4		Nominal current (I Source 1 plus
								I Source 2) is 6.3 mA.
	81	I Source 2	701-1998/ TP3	12.4		13.4		
15	82	Family 07,08 Ver., 1st	* /VCC	3.9		4.1		*Use socket with LED on.
		Pass						
	83	V Ref.	701-1998/ TP4	0.8		1.0		
	84	I Source 1	701-1998/ TP2	6.8		7.8		Nominal current (I Source 1 plus
								I Source 2) is 3.4 mA.
	85	I Source 2	701-1998/ TP3	6.8		7.8		
16	86	Family 07, 08 Ver., 2nd	* /VCC	4.9		5.1		*Use socket with LED on.
		Pass						
	87	V Ref.	701-1998/ TP4	1.6		1.8		
	88	I Source 1	701-1998/ TP2	5.9		6.9		Nominal current (I Source 1 plus
								I Source 2) is 2.4 mA.
	89	I Source 2	701-1998/ TP3	5.9		6.9		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
15	90	Family 09, 10 Ver., 1st	* /VCC	4.4		4.6		*Use socket with LED on.
		Pass						
	91	V Ref.	701-1998/ TP4	1.4		1.6		
	92	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.3 mA.
	93	I Source 2	701-1998/ TP3	4.7		5.7		
16	94	Family 09, 10 Ver., 2nd	* /VCC	5.4		5.6		*Use socket with LED on.
		Pass						
	95	V Ref.	701-1998/ TP4	1.4		1.6		
	96	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.3mA.
	97	I Source 2	701-1998/ TP3	4.7		5.7		
15	98	Family 11, 12 Ver., 1st	* /VCC	4.1		4.3		*Use Socekt with LED on.
		Pass						
	99	V Ref.	701-1998/ TP4	0.8		1.0		
	100	I Source 1	701-1998/ TP2	17.9		18.9		Nominal current (I Source 1 plus
								I Source 2) is 10.0mA.
	101	I Source 2	701-1998/ TP3	17.9		18.9		
16	102	Family 11, 12 Ver., 2nd	* /VCC	5.9		6.1		*Use socket with LED on.
		Pass						

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	103	V Ref.	701-1998 /TP4	3.4		3.6		
	104	I Source 1	701-1998 /TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 10.2 mA.
	105	I Source 2	701-1998 /TP3	5.7		6.7		
15	106	Family 13, 14 Ver., 1st	* /VCC	4.4		4.6		*Use socket with LED on.
		Pass						
	107	V Ref.	701-1998 /TP4	0.9		1.1		
	108	I Source 1	701-1998 /TP2	16.3		17.3		Nominal current (I Source 1 plus
								I Source 2) is 9.0 mA.
	109	I Source 2	701-1998 /TP3	16.3		17.3		
16		Pass						
16	110	Family 13, 14 Ver., 2nd	* /VCC	5.4		5.6		*Use socket with LED on.
		Pass						
	111	V Ref.	701-1998/ TP4	2.9		3.1		
	112	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 1.0 mA.
	113	I Source 2	701-1998/ TP3	13.2		14.2		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10
15	114	Family 15, 16 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	115	V Ref.	701-1998/ TP4	0.6		0.8		
	116	I Source 1	701-1998/ TP2	24.8		25.8		Nominal current (I Source 1 plus
								I Source 2) is 14.0 mA.
	117	I Source 2	701-1998/ TP3	24.8		25.8		
16	118	Family 15, 16 Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	119	V Ref.	701-1998/ TP4	2.3		2.5		
	120	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 1.6 mA.
	121	I Source 2	701-1998/ TP3	18.6		19.6		
15	122	Family 17, 18 Ver., 1st	* /VCC	4.2		4.4		*Use socket with LED on.
		Pass						
	123	V Ref.	701-1998/ TP4	0.8		1.0		
	124	I Source 1	701-1998/ TP2	7.0		8.0		Nominal current (I Source 1 plus
								I Source 2) is 3.5 mA.

Figure 4-3. Measurement Chart (Continued)

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LTR	DESCRIPTION	P.E.	DATE
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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	125	I Source 2	701-1998/ TP3	7.0		8.0		
16	126	Family 17, 18 Ver., 2nd	* /VCC	5.9		6.1		*Use socket with LED on.
		Pass						
	127	V Ref.	701-1998/ TP4	3.4		3.6		
	128	I Source 1	701-1998/ TP2	8.2		9.2		Nominal current (I Source 1 plus
								I Source 2) is 2.7 mA.
	129	I Source 2	701-1998/ TP3	8.2		9.2		
15	130	Family 19, 20 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	131	V. Ref.	701-1998/ TP4	0.6		0.8		
	132	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 2.0 mA.
	133	I Source 2	701-1998/ TP3	20.9		21.9		
16	134	Family 19, 20 Ver., 2nd	* /VCC	4.9		5.1		*Use socket with LED on.
		Pass						
	135	V Ref.	701-1998/ TP4	2.3		2.5		
	136	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	137	I Source 2	701-1998/ TP3	4.6		5.6		
15	138	Family 21, 22 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	139	V Ref.	701-1998/ TP4	0.6		0.8		
	140	I Source I	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 1.6 mA.
	141	I Source 2	701-1998/ TP3	16.9		17.9		
16	142	Family 21, 22 Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	143	V Ref.	701-1998/ TP4	2.1		2.3		
	144	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	145	I Source 2	701-1998/ TP3	4.4		5.4		
15	146	Family 23, 24 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	147	V Ref.	701-1998/ TP4	0.6		0.8		
	148	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 1.6 mA.
	149	I Source 2	701-1998/ TP3	16.9		17.9		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10
16	150	Family 23, 24 Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	151	V Ref.	701-1998/ TP4	2.1		2.3		
	152	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	153	I Source 2	701-1998/ TP3	4.4		5.4		
15	154	Family 25, 26 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	155	V Ref.	701-1998/ TP4	0.6		0.8		
	156	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 2.0 mA.
	157	I Source 2	701-1998/ TP3	20.9		21.9		
16	158	Family 25, 26 Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	159	V Ref.	701-1998/ TP4	2.3		2.5		
	160	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	161	I Source 2	701-1998/ TP3	4.6		5.6		
15	162	Family 27, 28 Ver., 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DVM to Socket 7, Pin 10.
	163	V Ref.	701-1998/ TP4	0.6		0.8		
	164	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 2.0 mA.
	165	I Source 2	701-1998/ TP3	20.9		21.9		
16	166	Family 27, 28 Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	167	V Ref.	701-1998/ TP4	2.3		2.5		
	168	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	169	I Source 2	701-1998/ TP3	4.6		5.6		
15	170	Family 29, 30 Ver., 1st	* /VCC	4.1		4.2		Use socket with LED on.
		Pass						
	171	V Ref.	701-1998/ TP4	0.8		1.0		
	172	I Source 1	701-1998/ TP2	17.9		18.9		Nominal current (I Source 1 plus
								I Source 2) is 10.0 mA.
	173	I Source 2	701-1998/ TP3	17.9		18.9		
16	174	Family 29, 30 Ver., 2nd	* /VCC	5.9		6.1		*Use socket with LED on.
		Pass						
	175	V Ref.	701-1998/ TP4	3.4		3.6		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10
	176	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus I
								I Source 2) is 0.2 mA.
	177	I Source 2	701-1998/ TP3	5.7		6.7		
15	178	Family 31, Ver. 1st	* /VCC	4.7		4.9		*Use socket with LED on.
		Pass						
	179	V Ref.	701-1998/ TP4	0.6		0.8		
	180	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus I
								I Source 2) is 2.0 mA.
	181	I Source 2	701-1998/ TP3	20.9		21.9		
	182	Family 31, Ver., 2nd	* /VCC	5.1		5.3		*Use socket with LED on.
		Pass						
	183	V Ref.	701-1998/ TP4	2.3		2.5		
	184	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus I
								I Source 2) is 0.2 mA.
	185	I Source 2	701-1998/ TP3	4.6		5.6		
15	186	Family 33 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	187	V Ref.	701-1998/ TP4	0.6		0.8		
	188	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus I
								I Source 2) is 2.0 mA.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	189	I Source 2	701-1998/ TP3	20.9		21.9		
16	190	Family 33 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	191	V Ref.	701-1998/ TP4	2.3		2.5		
	192	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	193	I Source 2	701-1998/ TP3	4.6		5.6		
15	194	Family 35 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	195	V Ref.	701-1998/ TP4	0.6		0.8		
	196	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 2.0 mA.
	197	I Source 2	701-1998/ TP3	20.8		21.8		
16	198	Family 35 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	199	V Ref.	701-1998/ TP4	2.1		2.3		
	200	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	201	I Source 2	701-1998/ TP3	4.4		5.4		
15	202	Family 37 Ver., 1st Pass	* /VCC	4.7		4.7		*Use socket with LED on.
	203	V Ref.	701-1998/ TP4	0.6		0.8		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	204	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 2.0 mA.
	205	I Source 2	701-1998/ TP3	20.8		21.8		
16	206	Family 37 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	207	V Ref.	701-1998/ TP4	2.1		2.3		
	208	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.2 mA.
	209	I Source 2	701-1998/ TP3	4.4		5.4		
15	210	Family 39 Ver., 1st Pass	* /VCC	3.9		4.1		*Use socket with LED on.
	211	V Ref.	701-1998/ TP4	0.7		0.9		
	212	I Source 1	701-1998/ TP2	6.0		7.0		Nominal current (I Source 1 plus
								I Source 2) is 3 mA.
	213	I Source 2	701-1998/ TP3	6.0		7.0		
16	214	Family 39 Ver., 2nd Pass	* /VCC	5.9		6.1		*Use socket with LED on.
	215	V Ref.	701-1998/ TP4	4.0		4.2		
	216	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current (I Source 1 plus
								I Source 2) is 0.5 mA.
	217	I Source 2	701-1998/ TP3	9.3		10.3		
15	218	Family 43 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	219	V Ref.	701-1998/ TP4	0.6		0.8		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	220	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	221	I Source 2	701-1998/ TP3	20.8		21.8		
16	222	Family 43 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	223	V Ref.	701-1998/ TP4	2.1		2.3		
	224	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	225	I Source 2	701-1998/ TP3	4.4		5.4		
15	226	Family 45 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	227	V Ref.	701-1998/ TP4	0.6		0.8		
	228	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	229	I Source 2	701-1998/ TP3	21.0		22.0		
16	230	Family 45 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	231	V Ref.	701-1998/ TP4	2.1		2.3		
	232	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	233	I Source 2	701-1998/ TP3	4.4		5.4		
15	234	Family 47, 48, 1st Pass	* / VCC 701-1998	4.7		4.9		*Use socket with LED on.
	235	V Ref.	701-1998/ TP4	0.4		0.6		
	236	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 20 mA.
	237	I Source 2	701-1998/ TP3	20.7		21.7		
16	238	Family 47, 48, 2nd Pass	* /VCC 701-1998	5.1		5.3		*Use socket with LED on.
	239	V Ref.	701-1998/ TP4	2.3		2.5		

Figure 4-3. Measurement Chart (Continued)

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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
	240	I Source 1	701-1998/ TP2	-0.4		0.4		Ground DVM to Socket 7, Pin 10. Nominal current = 0.2 mA.
	241	I Source 2	701-1998/ TP3	4.6		5.6		
15	242	Family 49, 50, 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	243	V Ref.	701-1998/ TP4	0.4		0.6		
	244	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	245	I Source 2	701-1998/ TP3	20.8		21.8		
16	246	Family 49, 50, 2nd Pass	* /VCC 701-1998	5.1		5.3		*Use socket with LED on.
	247	V Ref.	701-1998/ TP4	2.3		2.5		
	248	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	249	I Source 2	701-1998/ TP3	4.6		5.6		
15	250	Family 51, 52, 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	251	V Ref.	701-1998/ TP4	0.4		0.6		
	252	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	253	I Source 2	701-1998/ TP3	20.8		21.8		
16	254	Family 51, 52, 2nd Pass	* /VCC 701-1998	5.1		5.3		*Use socket with LED on.
	255	V Ref.	701-1998/ TP4	2.3		2.5		
	256	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	257	I Source 2	701-1998/ TP3	4.6		5.6		
15	258	Family 53, 54, 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	259	V Ref.	701-1998/ TP4	0.4		0.6		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	260	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current - 2.0 mA.
	261	I Source 2	701-1998/ TP3	20.8		21.8		
16	262	Family 53, 54, 2nd Pass	* /VCC 701-1998	5.1		5.3		*Use socket with LED on.
	263	V Ref.	701-1998/ TP4	2.3		2.5		
	264	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	265	I Source 2	701-1998/ TP3	4.6		5.6		
15	266	Family 55, 56, 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	267	V Ref.	701-1998/ TP4	0.4		0.6		
	268	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	269	I Source 2	701-1998/ TP3	20.8		21.8		
16	270	Family 55, 56, 2nd Pass	* /VCC 701-1998	5.1		5.3		*Use socket with LED on.
	271	V Ref.	701-1998/ TP4	2.3		2.5		
	272	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	273	I Source 2	701-1998/ TP3	4.6		5.6		
	274	Family 57, 58, 1st Pass	* /VCC	4.7		4.9		
	275	V Ref.	701-1998/ TP4	0.6		0.8		
	276	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	277	I Source 2	701-1998/ TP3	20.8		21.8		
16	278	Family 57, 58, 2nd Pass	* /VCC	5.1		5.3		

Figure 4-3. Measurement Chart (Continued)

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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
	279	V Ref.	701-1998/ TP4	2.1		2.3		Ground DVM to Socket 7, Pin 10.
	280	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	281	I Source 2	701-1998/ TP3	4.4		5.4		
15	282	Family 59, 60, 1st Pass	* /VCC 701-1998	4.8		5.0		
	283	V Ref.	701-1998/ TP4	0.7		0.9		
	284	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 1.6 mA.
	285	I Source 2	701-1998/ TP3	17.0		18.0		
16	286	Family 59, 60, 2nd Pass	* /VCC 701-1998	5.4		5.6		
	287	V Ref.	701-1998/ TP4	3.4		3.6		Nominal current = 1.6 mA.
	288	I Source 1	701-1998/ TP2	-0.4		0.4		
	289	I Source 2	701-1998/ TP3	19.7		20.7		
15	290	Family 61 Ver., 1st Pass	* /VCC	4.6		4.8		*Use socket with LED on.
	291	V Ref.	701-1998/ TP4	0.6		0.8		
	292	I Source 1	701-1998/ TP2	24.5		25.5		Nominal current - 14.0 mA.
	293	I Source 2	701-1998/ TP3	24.5		25.5		
16	294	Family 61, Ver., 2nd pass	* /VCC	5.1		5.3		*Use socket with LED on.
	295	V Ref.	701-1998/ TP4	2.3		2.5		
	296	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 1.6 mA.
	297	I Source 2	701-1998/ TP3	18.6		19.6		
15	298	Family 79 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	299	V Ref.	701-1998/ TP4	0.6		0.8		
	300	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	301	I Source 2	701-1998/ TP3	20.8		21.8		
16	302	Family 79 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	303	V Ref.	701-1998/ TP4	2.1		2.3		
	304	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2mA.
	305	I Source 2	701-1998/ TP3	4.4		5.4		
	306	Family 81 Veer., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	307	V Ref.	701-1998/ TP4	0.6		0.8		
	308	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0mA.
	309	I source 2	701-1998/ TP3	20.8		21.8		
16	310	Family 81 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	311	V Ref.	701-1998/ TP4	2.1		2.3		
	312	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2mA.
	313	I Source 2	701-1998/ TP3	4.4		5.4		
15	314	Family 83 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	315	V Ref.	701-1998/ TP4	0.6		0.8		
	316	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0mA.
	317	I Source 2	701-1998/ TP3	20.8		21.8		
16	318	Family 83 Ver., 2nd pass	* /VCC	5.1		5.3		*Use socket with LED on.

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	319	V Ref.	701-1998/ TP4	2.1		2.3		
	320	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	321	I Source 2	701-1998/ TP3	4.4		5.4		
15	322	Family 85 Ver., 1st Pass	* /VCC	4.7		4.9		*Use socket with LED on.
	323	V Ref.	701-1998/ TP4	0.6		0.8		
	324	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	325	I Source 2	701-1998/ TP3	20.8		21.8		
16	326	Family 85 Ver., 2nd Pass	* /VCC	5.1		5.3		*Use socket with LED on.
	327	V Ref.	701-1998/ TP4	2.1		2.3		
	328	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	329	I Source 2	701-1998/ TP3	4.4		5.4		
15	330	Family 87, 88, 1st Pass	* /VCC	2.9		3.1		
	331	V Ref.	701-1998/ TP4	0.4		0.5		
	332	I Source 1	701-1998/ TP2	6.0		7.0		Nominal current = 3.2 mA.
	333	I Source 2	701-1998/ TP3	6.0		7.0		
16	334	Family 87, 88, 2nd Pass	* /VCC	6.9		7.1		
	335	V Ref.	701-1998/ TP4	2.2		2.4		
	336	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.5 mA.
	337	I Source 2	701-1998/ TP3	7.5		8.5		

Figure 4-3. Measurement Chart (Continued)

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UniPak Measurement Chart
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STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	338	Family 89, 90, 1st Pass	* /VCC 701-1998	3.9		4.1		
	339	V Ref.	701-1998/ TP4	0.3		0.5		
	340	I Source 1	701-1998/ TP2	6.0		7.0		Nominal current = 3.2 mA.
	341	I Source 2	701-1998/ TP3	6.0		7.0		
16	342	Family 89, 90, 2nd Pass	* /VCC 701-1998	5.9		6.1		
	343	V Ref.	/ TP4	2.3		2.5		
	344	I Source 1	/ TP2	-0.4		0.4		Nominal current = 1.0 mA.
	345	I Source 2	/ TP3	3.6		4.6		
	346	Family 91, 92., 1st Pass	* /VCC 701-1998	4.4		4.6		
	347	V Ref.	/ TP4	0.4		0.6		
	348	I Source 1	/ TP2	17.5		18.5		
	349	I Source 2	/ TP3	17.5		18.5		
16	350	Family 91, 92., 2nd Pass	* /VCC 701-1998	5.4		5.6		
	351	V Ref.	/ TP4	2.3		2.5		
	352	I Source 1	/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	353	I Source 2	/ TP3	22.6		23.6		
15	354	Family 93, 94., 1st Pass	* /VCC 701-1998	4.7		4.9		

Figure 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See page 1		

UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, pin 10
	355	V Ref.	/ TP4	0.6		0.8		
	356	I Source 1	/ TP2	-0.4		0.4		Nominal current - 2.0 mA.
	357	I Source 2	/ TP3	20.9		21.9		
16	358	Family 93, 94, 2nd Pass	* /VCC 701-1998	5.1		5.3		
	359	V Ref.	/ TP4	2.1		2.3		
	360	I Source 1	/ TP2	-0.4		0.4		Nominal current - 0.2 mA.
	361	I Source 2	/ TP3	4.4		5.4		
15	362	Family A5, A6, 1st Pass	701-1998	4.6		4.8		
	363	V Ref.	/ TP4	0.4		0.6		
	364	I Source 1	/ TP2	-0.4		0.4		Nominal current = 2.1 mA.
	365	I Source 2	/ TP3	21.9		22.9		
16	366	Family A5, A6, 2nd Pass	* /VCC 701-1998	5.4		5.6		
	367	V Ref.	/ TP4	2.1		2.3		
	368	I Source 1	/ TP2	-0.4		0.4		Nominal current = 0.5 mA.
	369	I Source 2	/ TP3	7.4		8.4		
15	370	Family A9, AA. 1st Pass	* /VCC 701-1998	3.9		4.1		*Use socket with LED on.
	371	V Ref.	701-1998/ TP4	0.8		1.0		
	372	I Source 1	701-1998/ TP2	6.9		7.9		Nominal current = 3.5 mA.

Figure 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
	See page 1		

UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points		MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	373	I Source 2		701-1998/ TP3	6.9		7.9		
16	374	Family A9, AA, 2nd Pass	* /VCC	701-1998	5.9		6.1		*Use socket with LED on.
	375	V Ref.		701-1998	3.4		3.6		
	376	I Source 1		701-1998/ TP2	8.2		9.2		Nominal current = 2.7mA
	377	I Source 2		701-1998/ TP3	8.2		9.2		
15	378	Family AB, AC, 1st Pass	* /VCC	701-1998	4.7		4.9		*Use socket with LED on.
	379	V Ref.		701-1998/ TP4	0.4		0.6		
	380	I Source 1		701-1998/ TP2	-0.4		0.4		Nominal current = 2.0mA
	381	I Source 2		701-1998/ TP3	20.7		21.7		
16	382	Family AB, AC, 2nd Pass	* /VCC	701-1998	5.1		5.3		*Use socket with LED on.
	383	V Ref.		701-1998/ TP4	2.3		2.5		
	384	I Source 1		701-1998/ TP2	-0.4		0.4		Nominal current = 0.2mA
	385	I Source 2		701-1998/ TP3	4.6		5.6		
15	386	Family AD, AE, 1st Pass	* /VCC	701-1998	4.4		4.6		*Use socket with LED on.
	387	V Ref.		701-1998/ TP4	1.4		1.6		
	388	I Source 1		701-1998/ TP2	-0.4		0.4		Nominal current = 0.3mA
	389	I Source 2		701-1998/ TP3	4.6		5.6		

Figure 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
	See page 1		

UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
16	390	Family AD, AE, 2nd Pass	* /VCC 701-1998	5.4		5.6		*Use socket with LED on.
	391	V Ref.	701-1998/ TP4	1.4		1.6		
	392	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.3mA
	393	I Source 2	701-1998/ TP3	4.6		5.6		
15	394	Family AF, BØ, 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	395	V Ref.	701-1998/ TP4	.6		.8		
	396	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0mA
	397	I Source 2	701-1998/ TP3	20.8		21.8		
16	398	Family AF, BØ, 2nd Pass	* /VCC 701-1998	5.5		5.7		*Use socket with LED on.
	399	V Ref.	701-1998 TP4	2.1		2.3		
	400	I Source 1	701-1998 TP2	-0.4		0.4		Nominal current = 0.2 mA.
	401	I Source 2	701-1998/ TP3	4.6		5.6		
15	402	Family B1, B2, 1st Pass	* /VCC 701-1998	3.9		4.1		*Use socket with LED on.
	403	V Ref.	701-1998/ TP4	0.8		1.0		
	404	I Source 1	701-1998/ TP2	6.9		7.9		Nominal current = 3.5 mA.
	405	I Source 2	701-1998/ TP3	6.9		7.9		
16	406	Family B1, B2, 2nd Pass	* /VCC 701-1998	5.9		6.1		*Use socket with LED on.

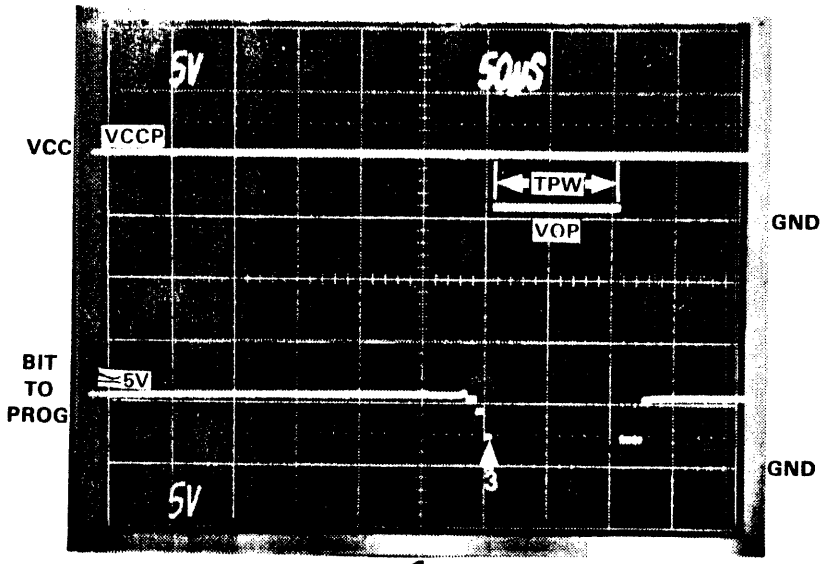
Figure 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See page 1		

UniPak Measurement Chart
34-950-0099

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit boards/test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DVM to Socket 7, Pin 10.
	407	V Ref.	701-1998/ TP4	3.4		3.6		
	408	I Source 1	701-1998/ TP2	8.2		9.2		Nominal current = 2.7 mA.
	409	I Source 2	701-1998/ TP3	8.2		9.2		
15	410	Family, B3, B4 1st Pass	* /VCC 701-1998	4.7		4.9		*Use socket with LED on.
	411	V Ref.	701-1998/ TP4	0.5		0.7		
	412	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 2.0 mA.
	413	I Source 2	701-1998/ TP3	20.8		21.8		
16	414	Family B3, B4, 2nd Pass	*,/VCC 701-1998	5.1		5.3		*Use socket with LED on.
	415	V Ref.	701-1998/ TP4	2.2		2.4		
	416	I Source 1	701-1998/ TP2	-0.4		0.4		Nominal current = 0.2 mA.
	417	I Source 2	701-1998/ TP3	4.5		5.0		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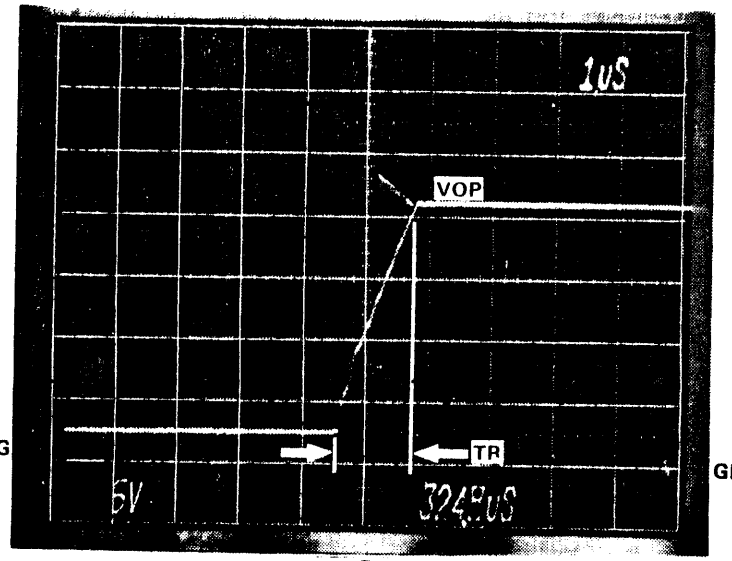
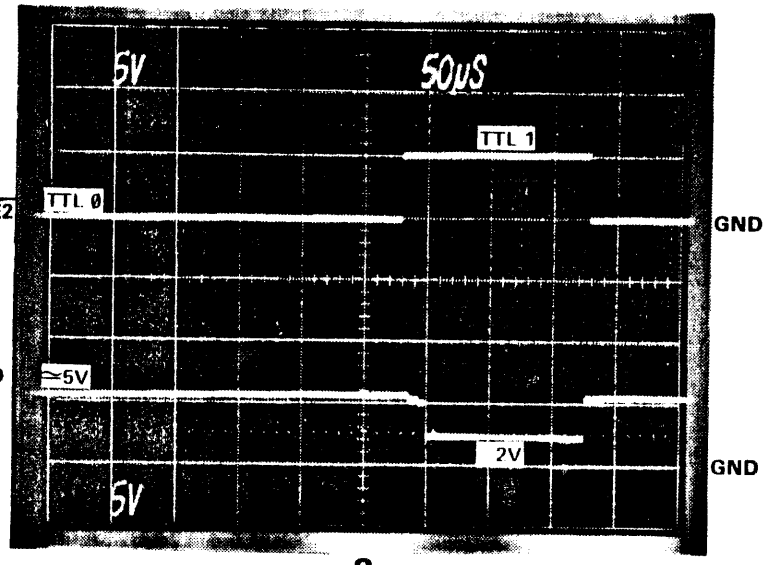
50uS
VCC
VCCP
TPW
VOP
GND
BIT
TO
PROG
≈5V
GND
5V

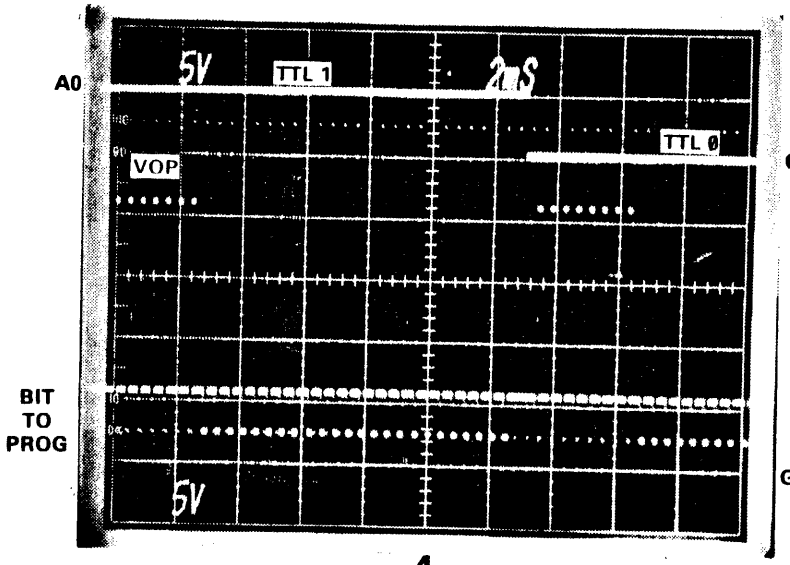
1


1uS
VOP
BIT
TO
PROG
TR
GND
5V
324.0uS

3


5V
50uS
TTL 1
E2
TTL 0
GND
BIT NO
PROG
≈5V
2V
GND
5V

2


A0
5V
TTL 1
2mS
TTL 0
VOP
GND
BIT
TO
PROG
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_0 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	
VOP	20		21	V	
TPW	90	100	110	µs	
TR	.8	1.2	1.6	µs	
REJECT		8		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	P.K.A	TEB	3-20-84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

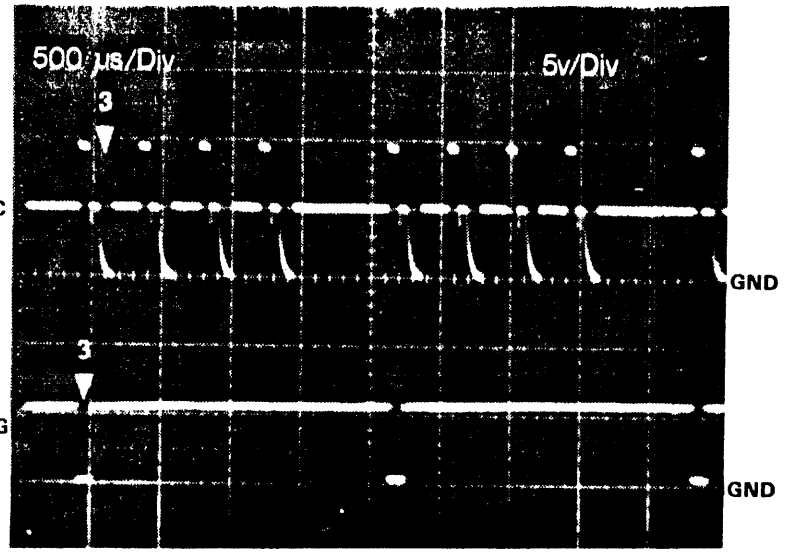
FAMILY CODES 01, 02

DRAWN BY: K.A

CHECKED BY: JS

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0001

SCALE | SHEET 1/1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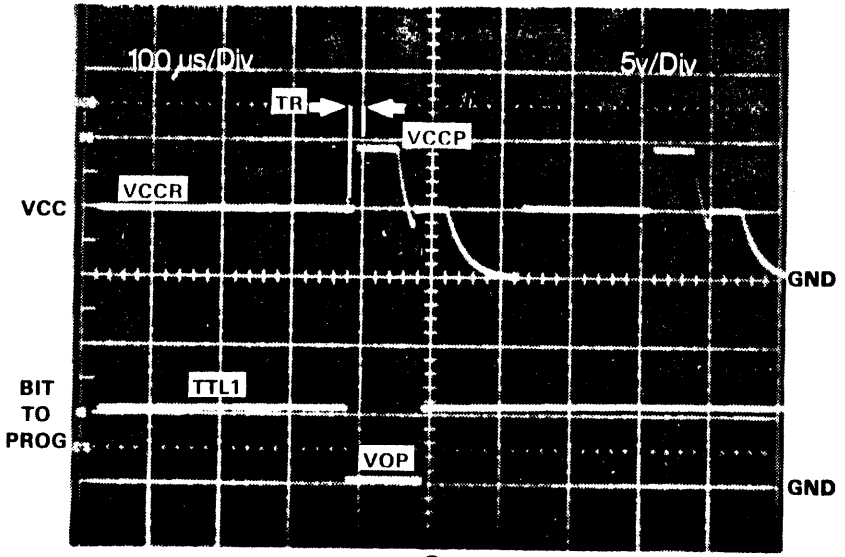
5v/Div
3
VCC
GND
3
BIT
TO
PROG
GND

1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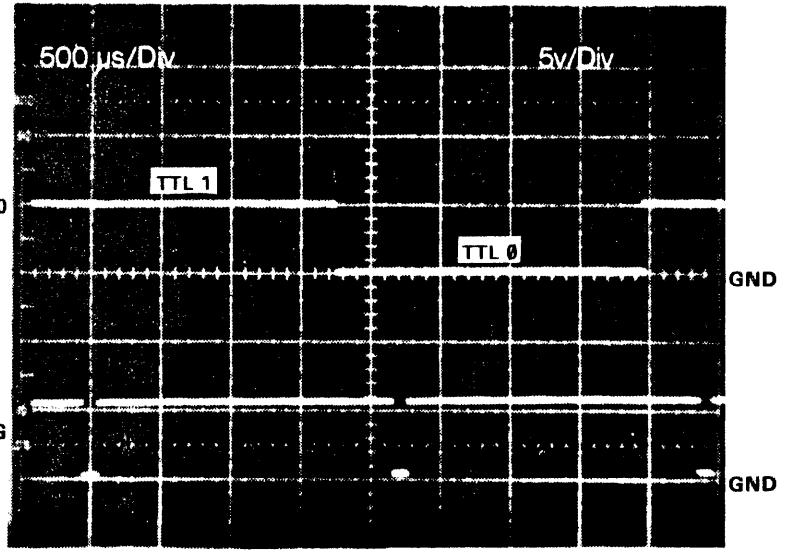
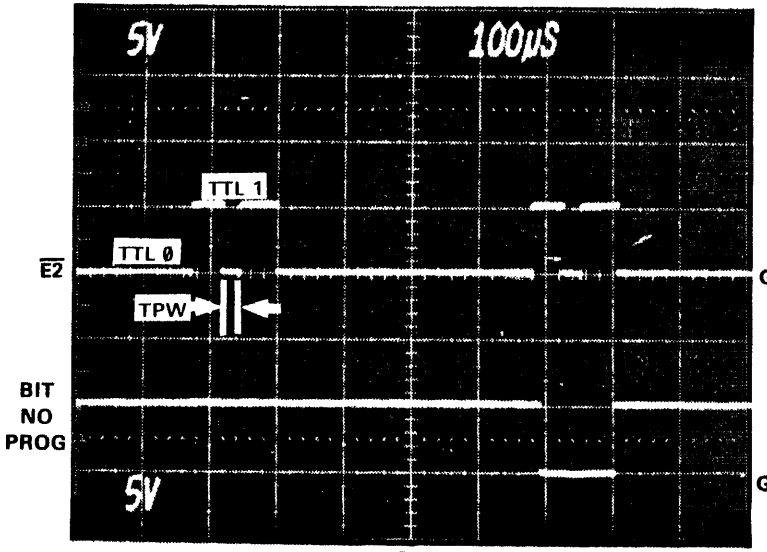
VCCP
VCCR
VCC
GND
BIT
TO
PROG
TTL1
VOP
GND

3


500 µs/Div
5v/Div
TTL 1
A0
TTL 0
GND
BIT
TO
PROG
GND

2


5V
100µS
TTL 1
TTL 0
E2
GND
TPW
BIT
NO
PROG
5V
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.0	5.25	V	
VCCP	9.0	9.25	9.50	V	
VOP	0		.3	V	
TPW	15	25	100	µs	
TR	5		20	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	[illegible]	[illegible]	3-20-82
	B	ECN #4630		[illegible]	7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 03, 04

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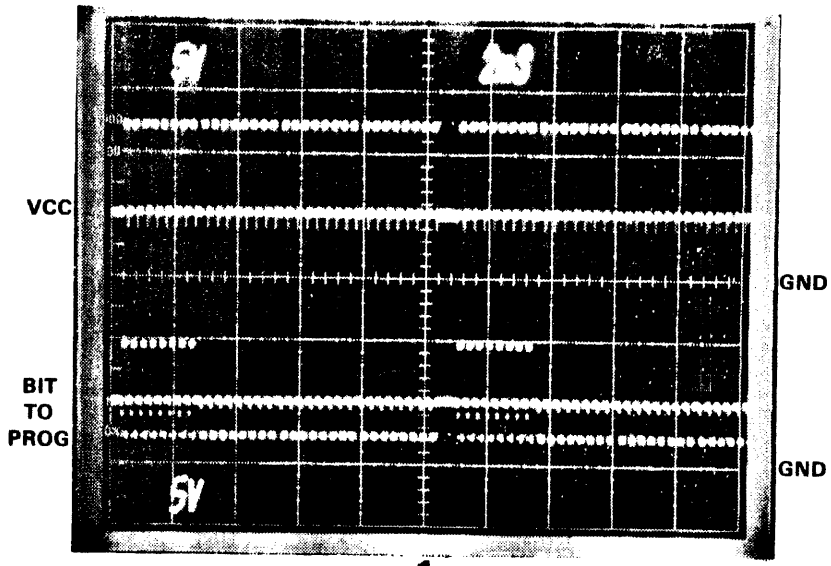
CHECKED BY: [illegible]

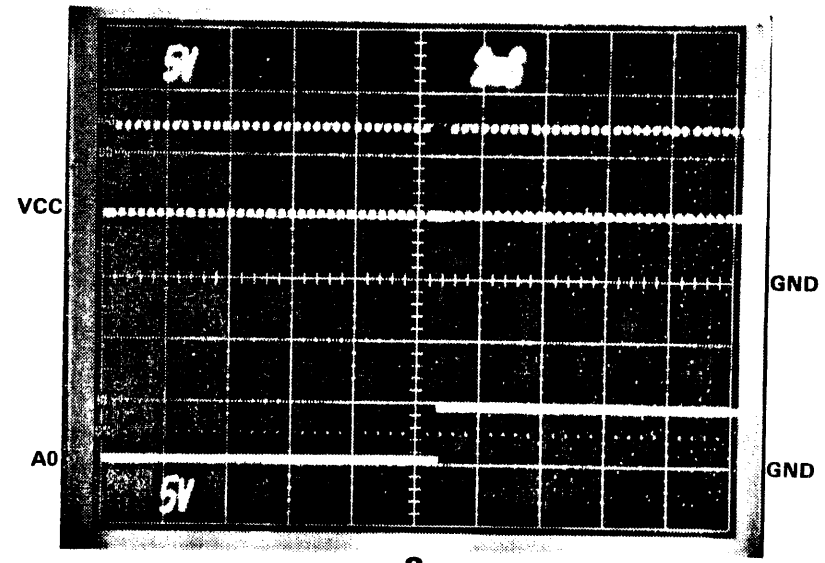
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0003

SCALE

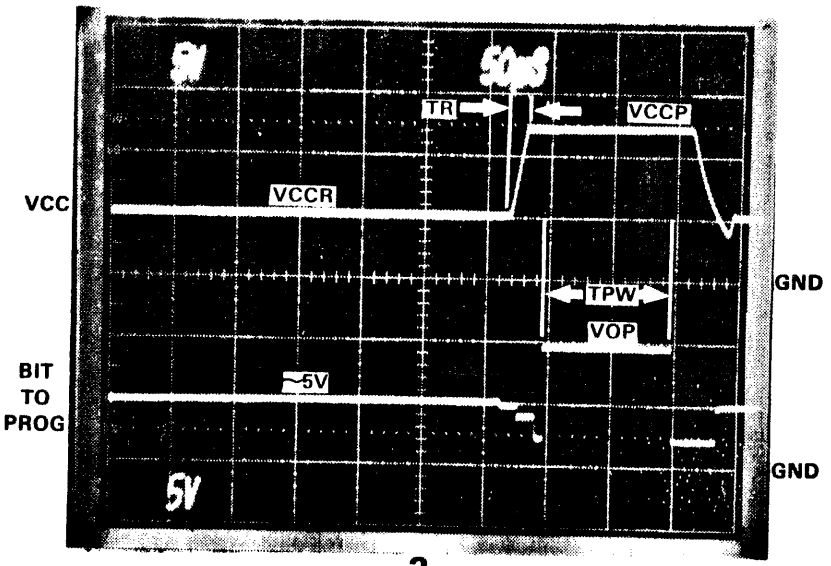
SHEET 1/1


VCC
GND
BIT
TO
PROG
GND

1


VCC
GND
A0
GND

2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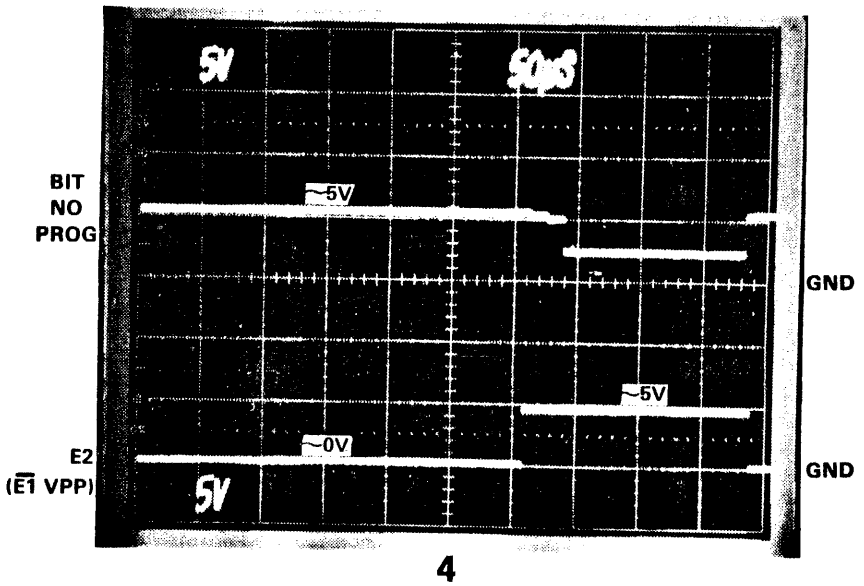
VCCP
VCCR
VCC
TPW
VOP
GND
BIT
TO
PROG
~5V
GND

3


BIT
NO
PROG
~5V
GND
~5V
E2
(E1 VPP)
~0V
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.0	5.25	V	
VCCP	12.0	12.25	12.5	V	
VOP	10.5	10.75	11.0	V	
TPW	90	100	110	µs	
TR	1		15	µs	
REJECT		8		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	[illegible]	[illegible]	[illegible]

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 05, 06

DRAWN BY: [illegible]

CHECKED BY: [illegible]

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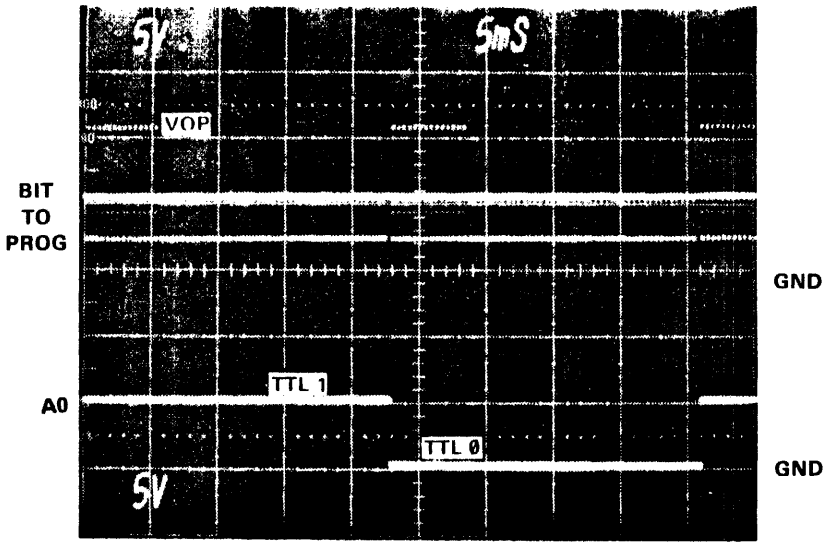
B	54193	007-0005

SCALE: | SHEET 1/1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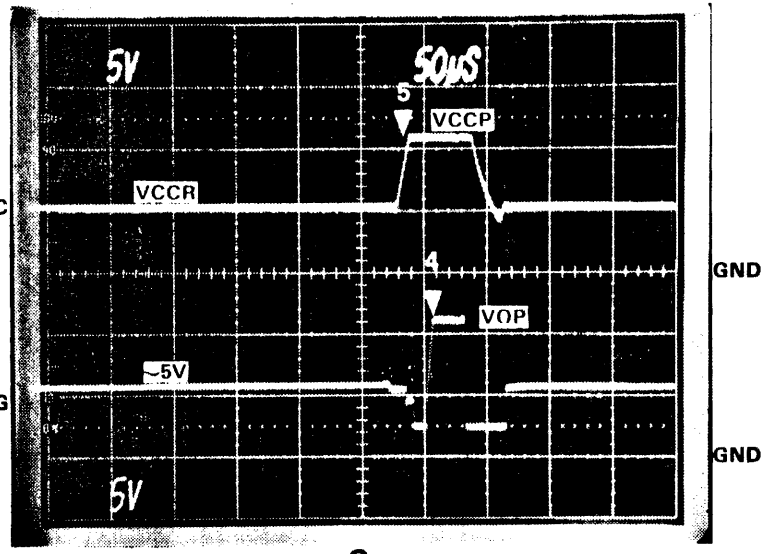
5mS
VOP
BIT
TO
PROG
GND
A0
TTL 1
TTL 0
GND
5V

1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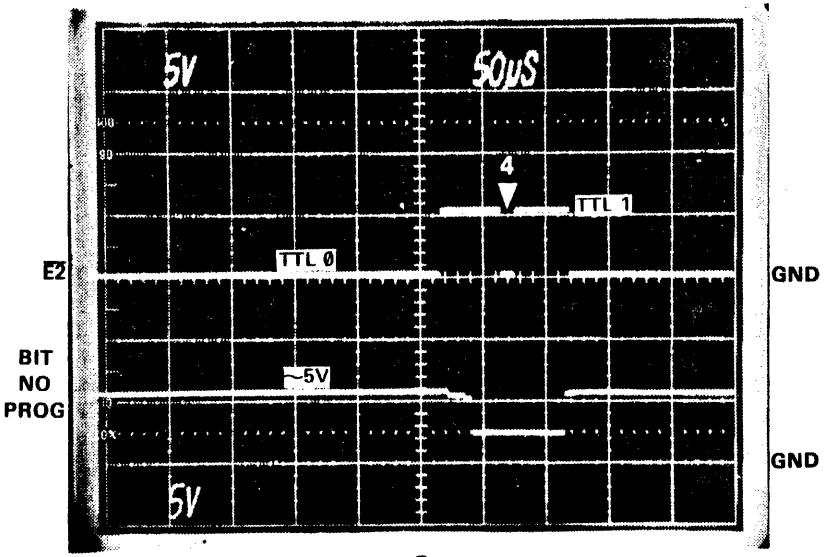
5
VCCP
VCC
VCCR
4
VOP
GND
BIT
TO
PROG
~5V
GND
5V

2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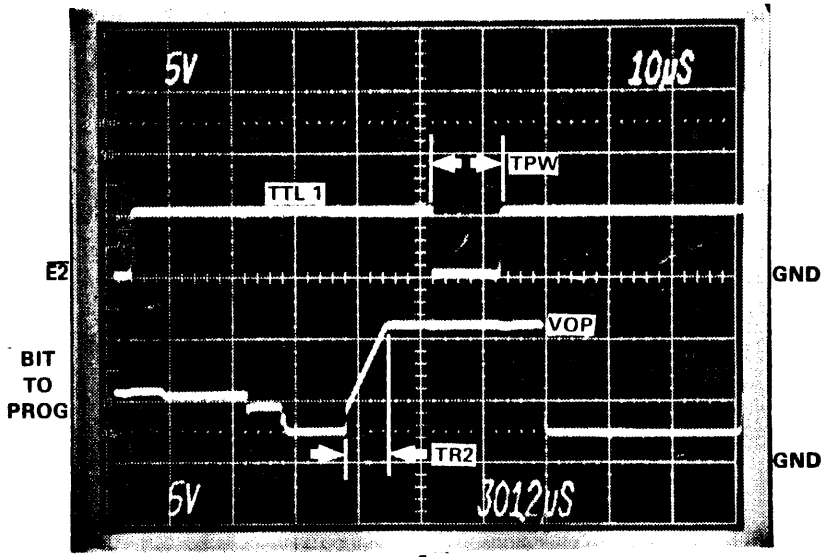
50µS
4
TTL 1
E2
TTL 0
GND
BIT
NO
PROG
~5V
GND
5V

3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10µS
TPW
TTL 1
E2
GND
VOP
BIT
TO
PROG
TR2
GND
5V
3012µS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	10.0	10.5	11.0	V	
VCCR	4.75	5.0	5.25	V	
VOP	10.0	10.5	11.0	V	
TPW	9	10	11	µs	
TR1	1		15	µs	
TR2	1		10	µs	
REJECT		14		PULSES	
OVERPROGRAM		5		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		TED	3-20-81
	B	ECN #4376		EJC	1-14-82
	C	ECN #4630		UBS	7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 07, 08

DRAWN BY: XJ

CHECKED BY: BS

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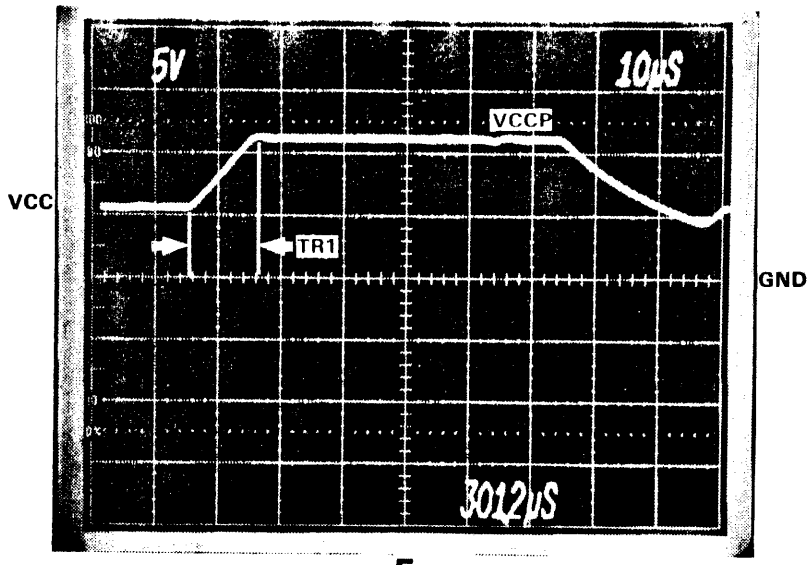
B	54193	007-0007

SCALE

SHEET 1/2



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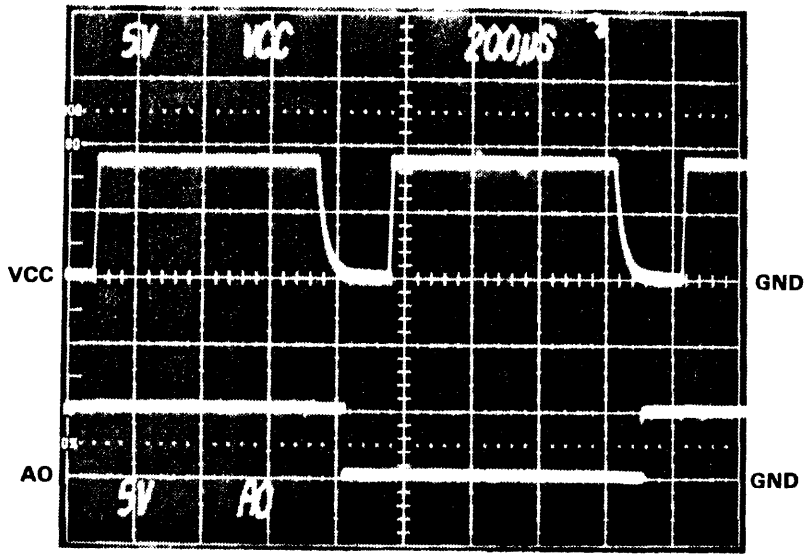
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 07, 08		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 007-0007
SCALE		SHEET 2/2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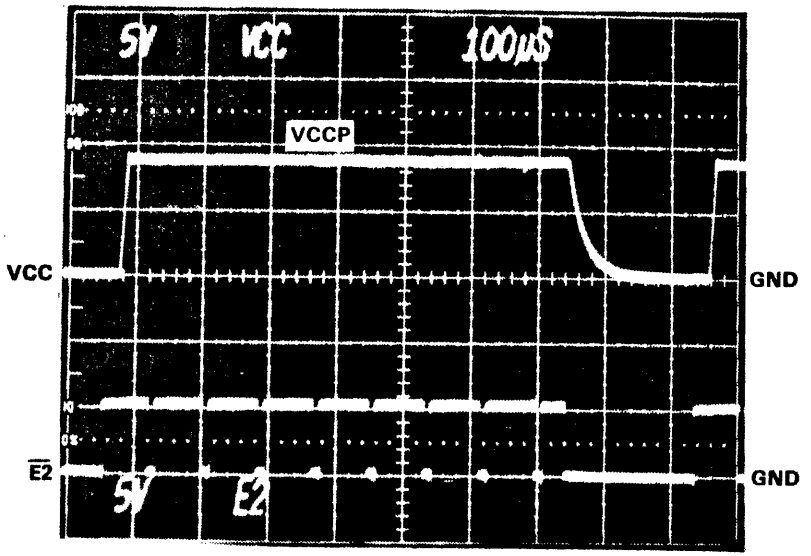
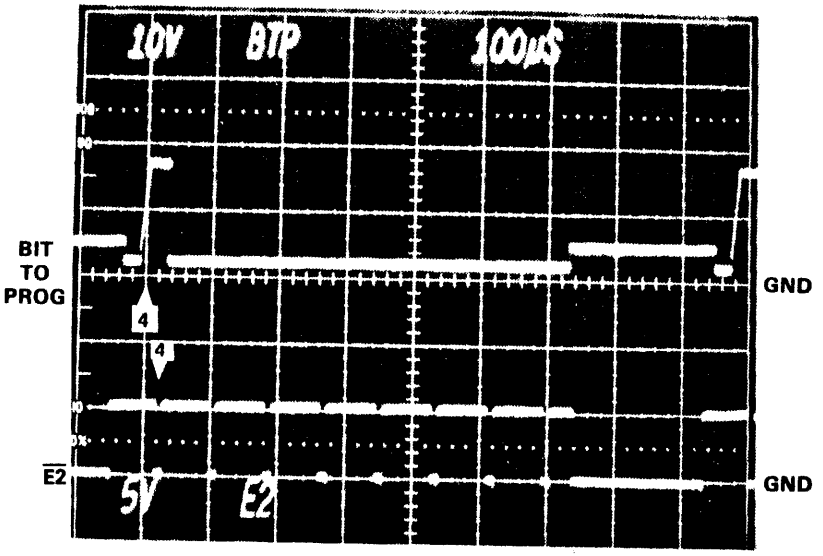
VCC
GND
AO
GND
5V AO

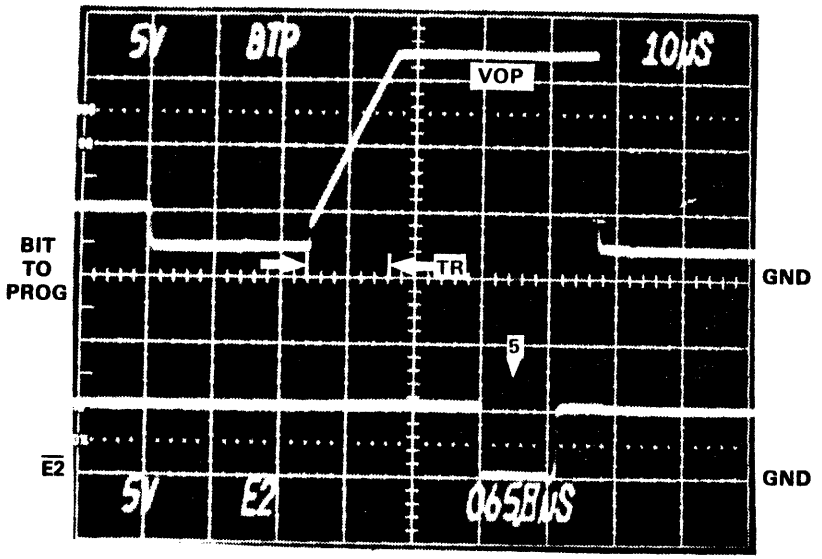
1


5V VCC 100µS
VCCP
VCC
GND
E2
GND
5V E2

2


10V BTP 100µS
BIT TO PROG
GND
4
4
E2
GND
5V E2

3


5V BTP 10µS
VOP
BIT TO PROG
TR
GND
5
E2
GND
5V E2 0658µS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.5	8.75	9.0	V	
	VOP	16.5	17.0	17.5	V	
	TPW	10		15	µs	
	TR	10		20	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	

10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		ZH	11/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 09, 10

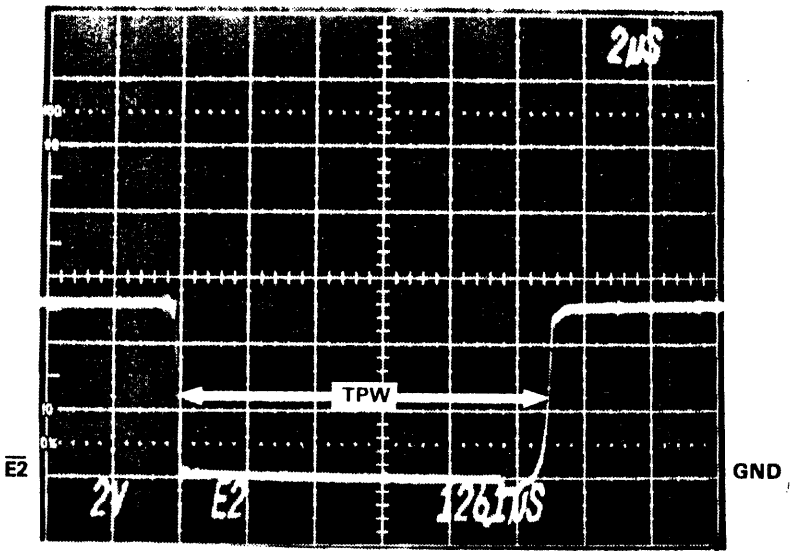
DRAWN BY: BG (EE)

CHECKED BY: ZH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

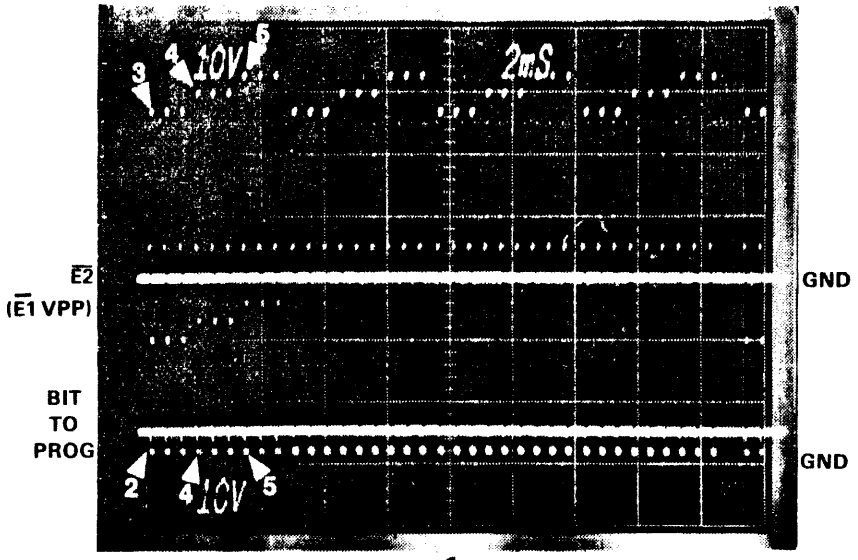
4-49
10-950-0099

REVISIONS

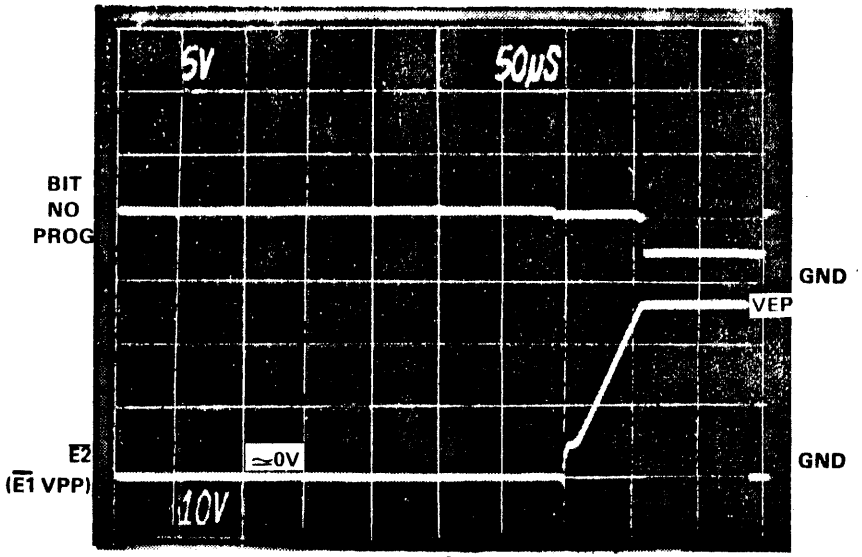
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

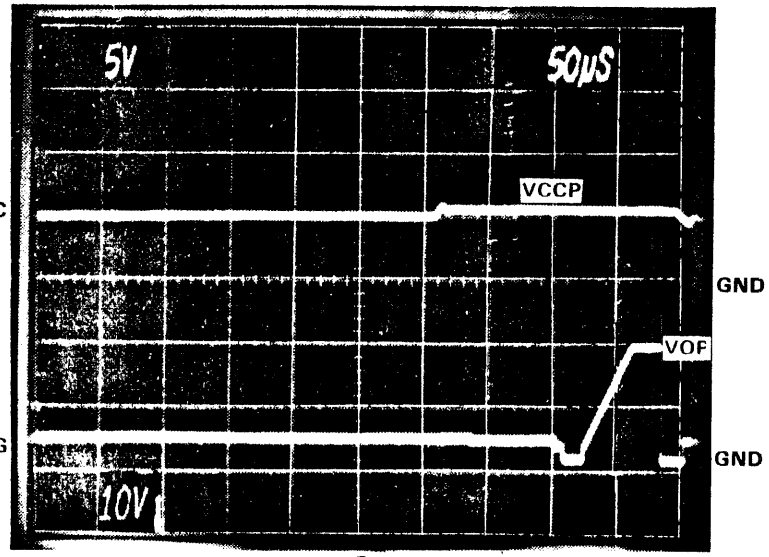
TITLE: TIMING DIAGRAM FAMILY CODES 09, 10	DRAWN BY: BG (FE) CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0099	
SCALE	SHEET 2/2


3
4
10V
5
2m.S.
E2
(E1 VPP)
GND
BIT
TO
PROG
GND
2
4
10V
5

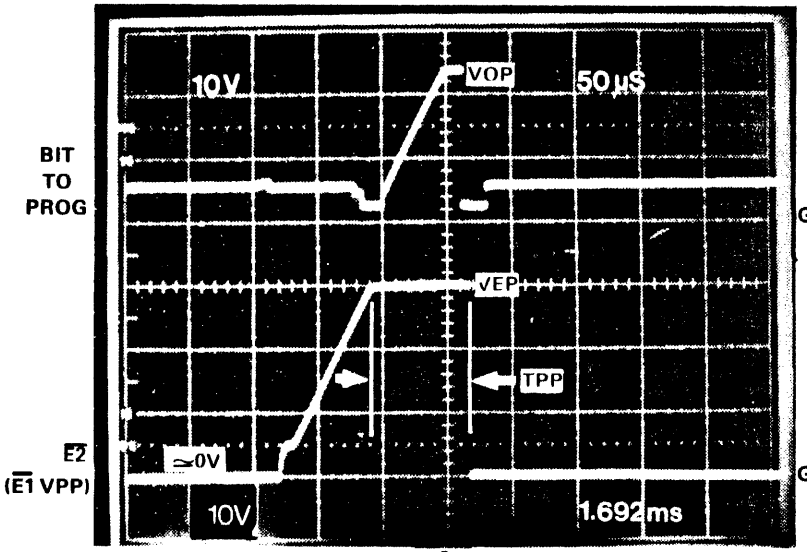
1


5V
50µS
BIT
NO
PROG
GND
VEP
E2
(E1 VPP)
≃0V
GND
10V

3


5V
50µS
VCC
VCCP
GND
VOP
BIT
TO
PROG
GND
10V

2


10V
VOP
50 µS
BIT
TO
PROG
GND
VEP
TPP
E2
(E1 VPP)
≃0V
GND
10V
1.692ms

4

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.0	5.25	V	
VCCP	4.75	5.5	5.75	V	
VEP	26	27	28	V	PULSE #1-3
	29	30	31	V	PULSE #4-6
	32	33	34	V	PULSE #7-9
VOP	19	20	21	V	PULSE #1-3
	22	23	24	V	PULSE #4-6
	25	26	27	V	PULSE #7-9
TPW	10		40	µs	
TPP	30		100	µs	
TR	0.34	0.4	0.46	V/µs	
REJECT		9		PULSES	
OVERPROGRAM		0		PULSES	

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			
	B	ECN # 3729	KB	DEB	7-11-80
	C	ECN #4376		FJC	1-14-82
	D	ECN #4630		WJB	7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

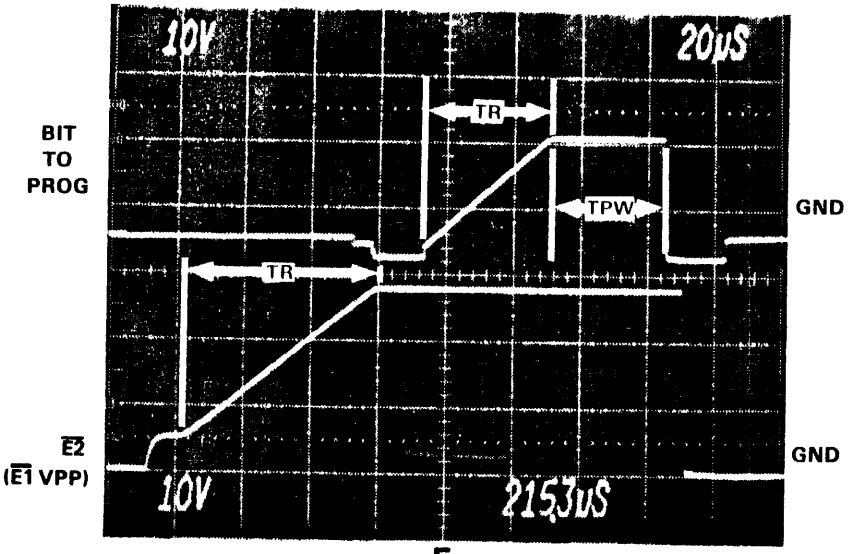
FAMILY CODES 11, 12

DRAWN BY:

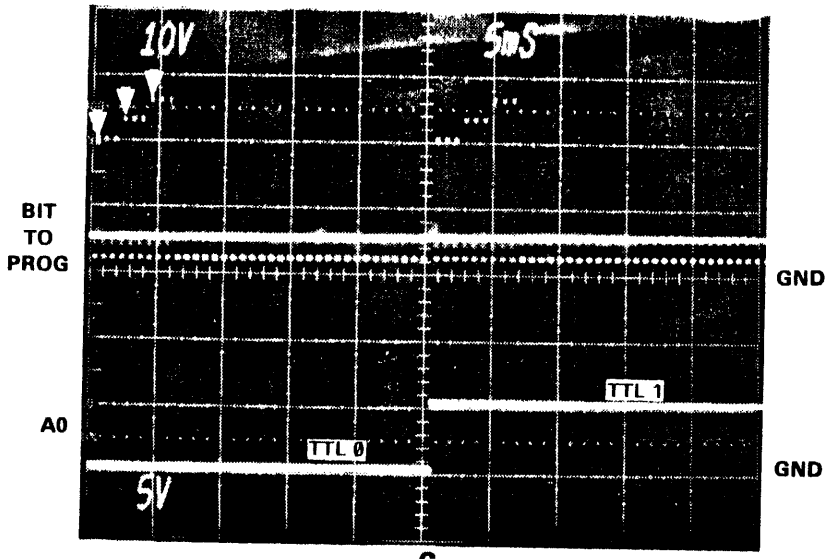
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0011

SCALE | SHEET 1/2


10V
20uS
BIT
TO
PROG
TR
TPW
GND
TR
E2
(E1 VPP)
GND
10V
215,3uS

5


10V
5mS
BIT
TO
PROG
GND
TTL 1
A0
TTL 0
GND
5V

6

4-53
10-950-0069

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 11, 12

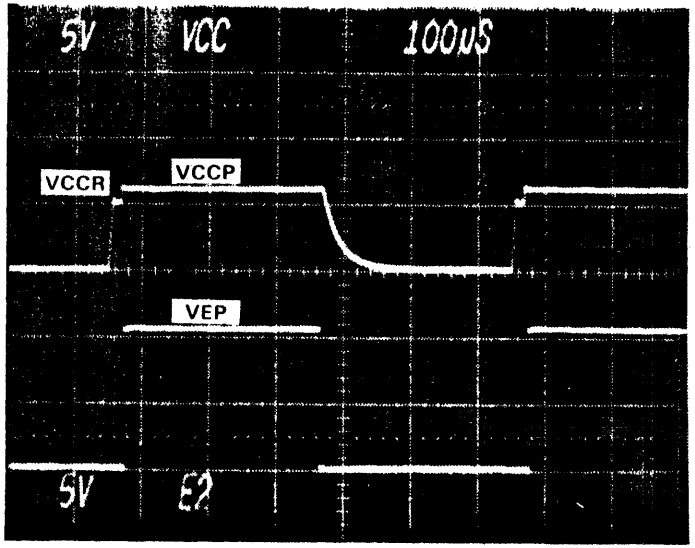
DRAWN BY:

CHECKED BY:

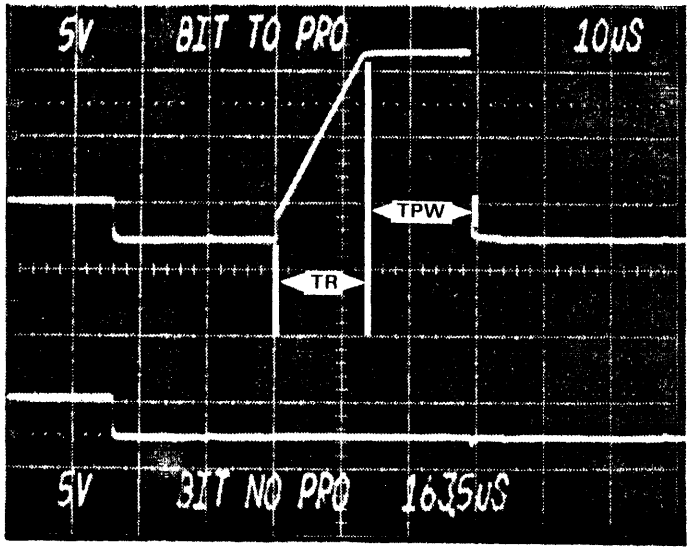
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0011

SCALE

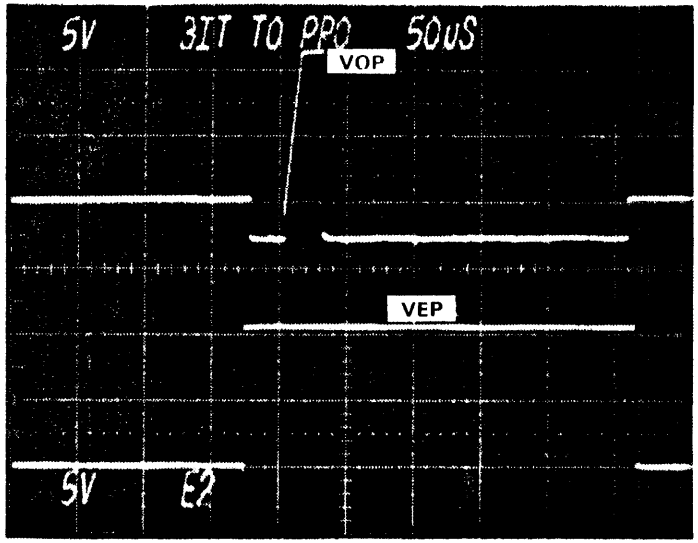
SHEET 2/2


5V VCC 100uS
VCCR
VCCP
VCCP
VCCR
VCC
GND
VEP
E2
GND
5V E2

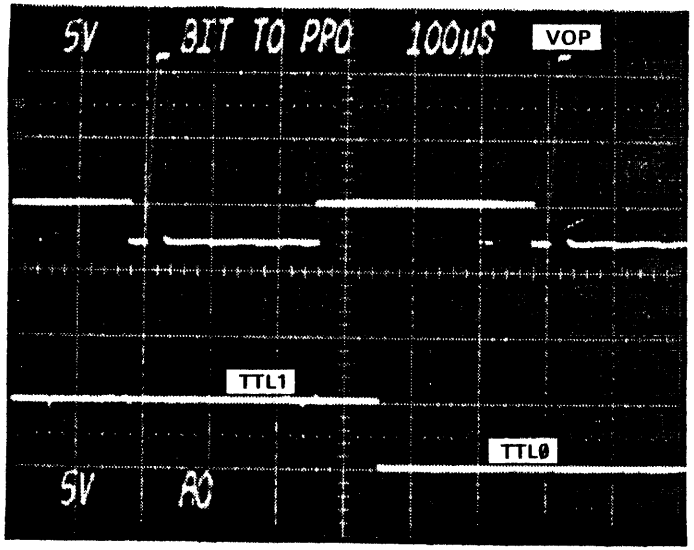
1


5V BIT TO PPO 10uS
BIT
TO
PGM
TPW
TR
GND
BIT
NO
PGM
GND
5V BIT NO PPO 16.35uS

3


5V BIT TO PPO 50uS
VOP
BIT
TO
PGM
GND
VEP
E2
GND
5V E2

2


5V BIT TO PPO 100uS
VOP
BIT
TO
PGM
GND
TTL1
A0
TTL0
GND
5V A0

4

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.0	5.25	V	
VCCP	5.8		6.2	V	
VOP	15.75	16.0	16.25	V	
VEP	9.75	10.0	11.0	V	
TPW	12	17	22	µs	
TR	10		25	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the Textool socket.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			
	B	ECN #4139			8-2581
	C	ECN #4376		FJC	1-14-82
	D	ECN #4630			7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 13, 14

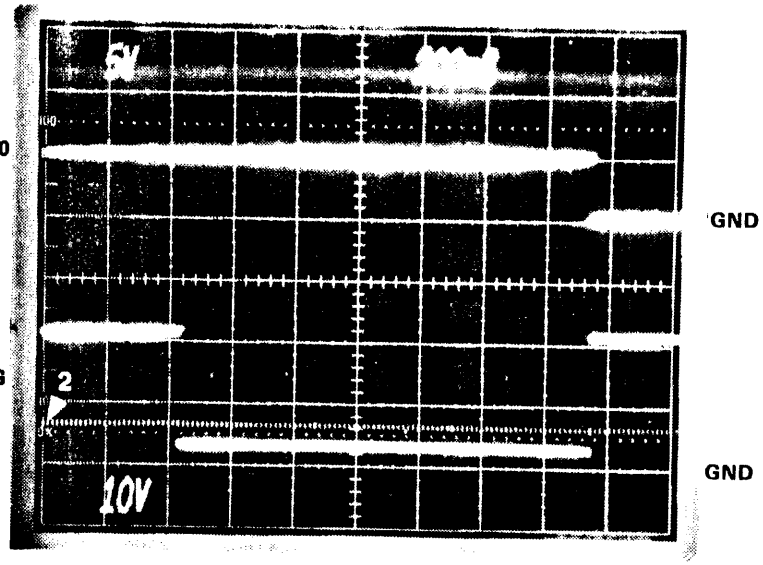
DRAWN BY:

CHECKED BY:

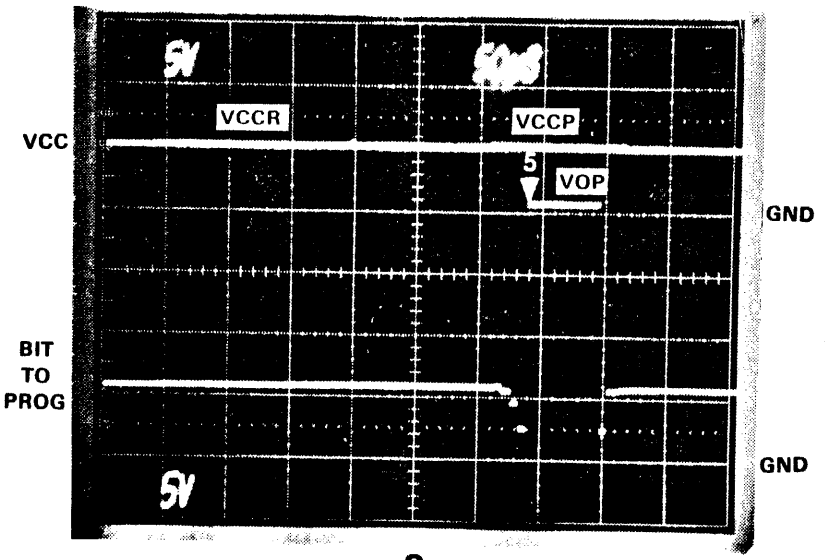
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0013

SCALE

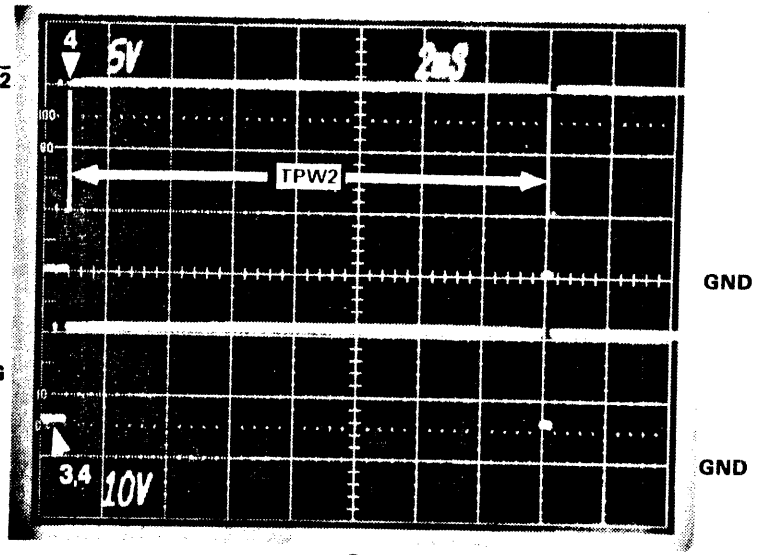
SHEET 1/1


5V
A0
GND
BIT
TO
PROG
2
10V
GND

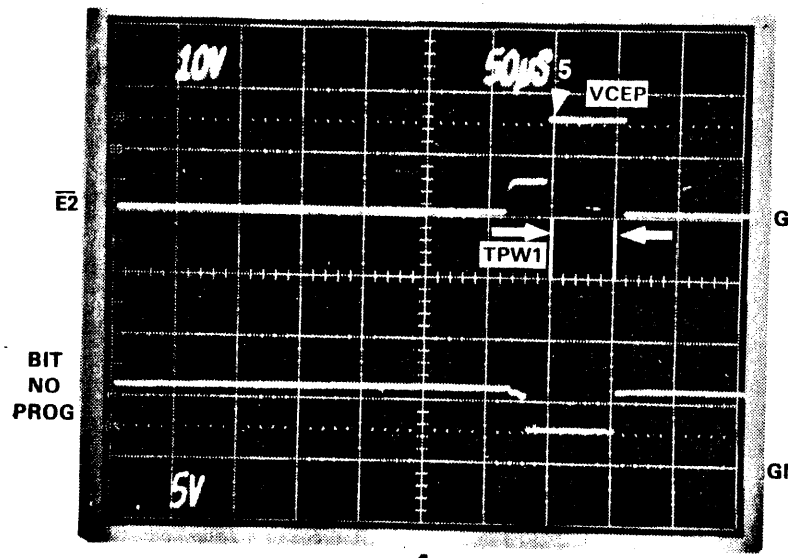
1


5V
VCCR
VCCP
VCC
5
VOP
GND
BIT
TO
PROG
5V
GND

3


4
5V
2mS
E2
TPW2
GND
BIT
TO
PROG
3,4
10V
GND

2


10V
50μS
5
VCEP
E2
GND
TPW1
BIT
NO
PROG
5V
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75		5.25	V	
VCCP	5.0		5.5	V	
VOP	19.5		20.5	V	
VCEP	14.5		15.5	V	
TPW1	50		100	µs	PULSE #1
TPW2	5.0		15.0	ms	PULSE #2-29
TR1	.2		.7	µs	
TR2	.6		1.4	µs	
REJECT		29		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RAT	MEB	3-20-80
	B	ECN #4376	X	FTC	1-14-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 15, 16

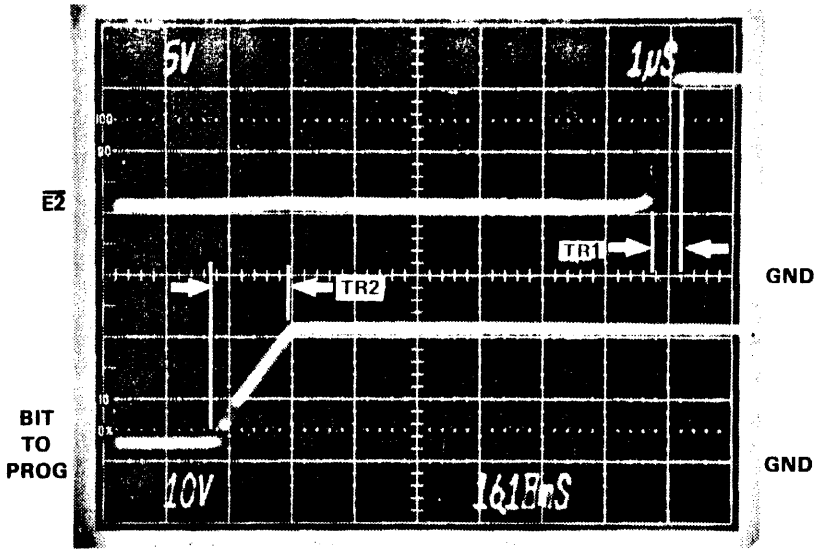
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0015

SCALE

SHEET 1/2



5

10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 15, 16

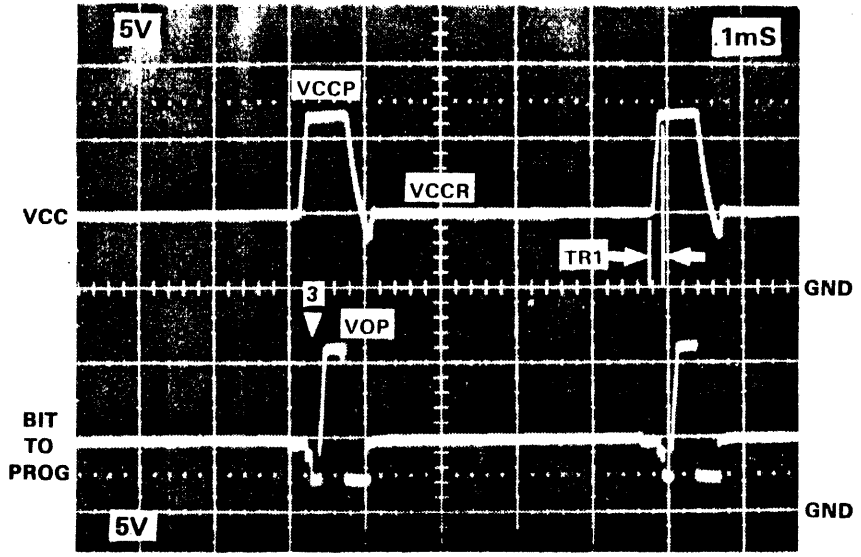
DRAWN BY:

CHECKED BY:

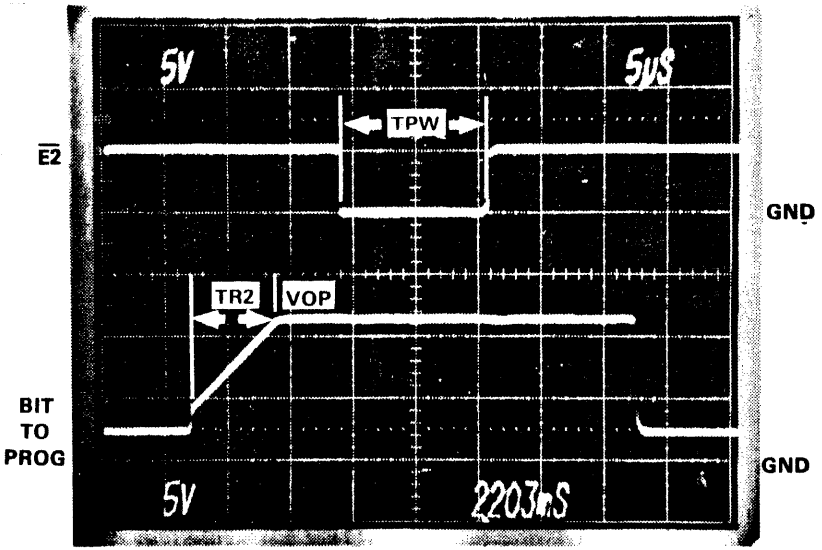
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0015

SCALE

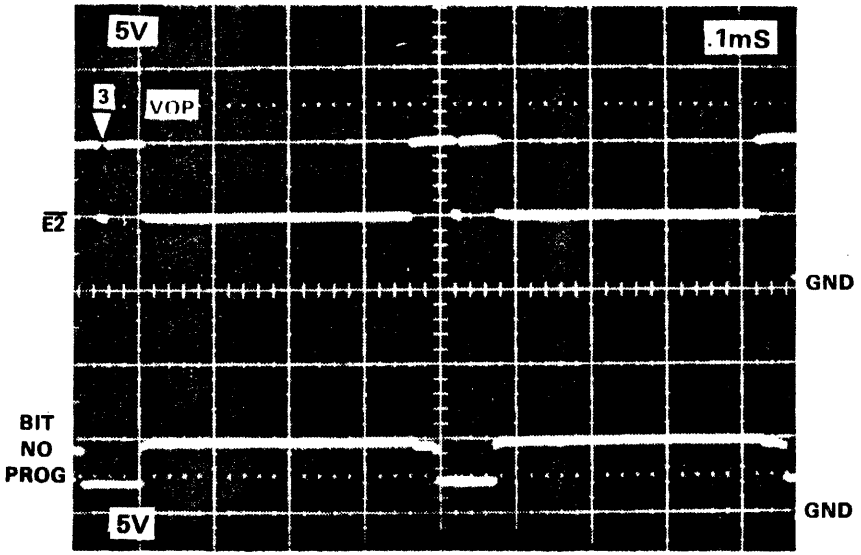
SHEET 2/2


5V
.1mS
VCCP
VCCR
VCC
TR1
GND
3
VOP
BIT
TO
PROG
5V
GND

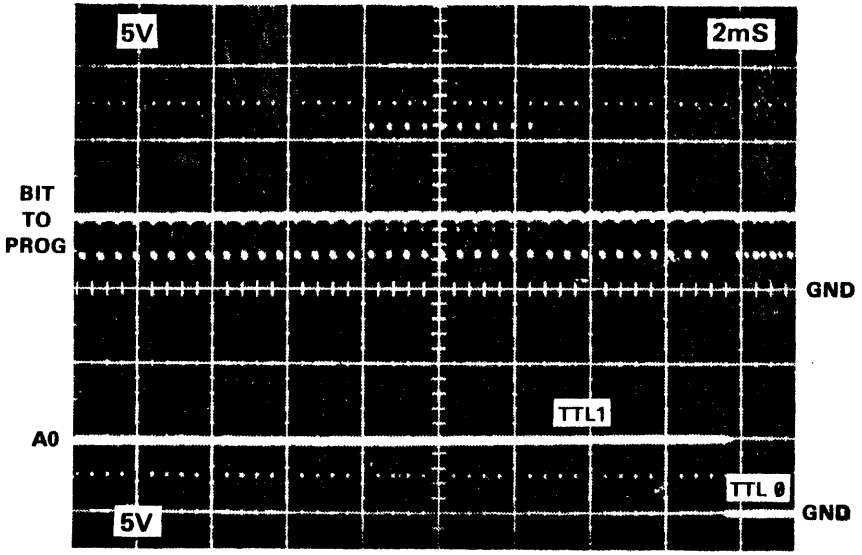
1


5V
5μS
TPW
E2
GND
TR2
VOP
BIT
TO
PROG
GND
5V
2203mS

3


5V
.1mS
3
VOP
E2
GND
BIT
NO
PROG
5V
GND

2


5V
2mS
BIT
TO
PROG
GND
TTL1
A0
TTL 0
5V
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.00	5.25	V	
VCCP	10.5	11.0	11.5	V	
VOP	10.5	11	11.5	V	
TPW	9	10	13	µs	
TR1	1		15	µs	
TR2	2		10	µs	
REJECT		14		PULSES	
OVERPROGRAM		5		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RAM	[illegible]	5-26-88
	C	ECN #4803		[illegible]	5/17/89

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 17, 18

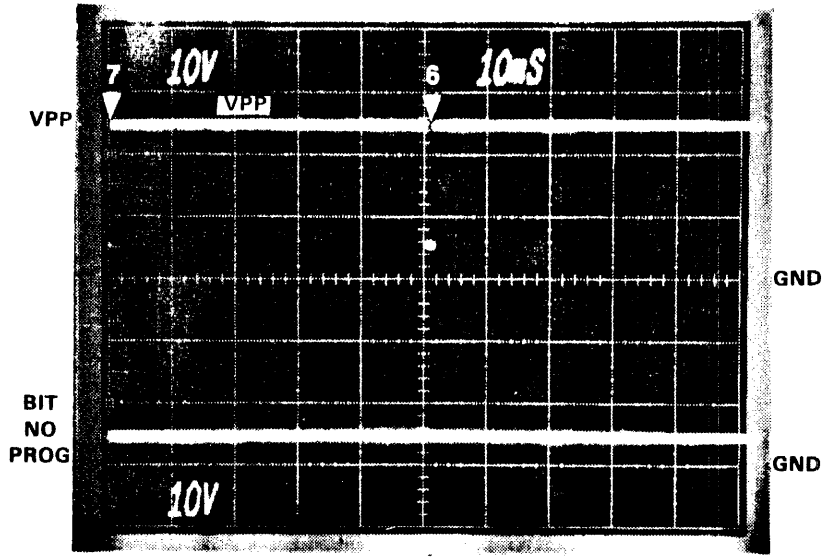
DRAWN BY: [illegible]

CHECKED BY: [illegible]

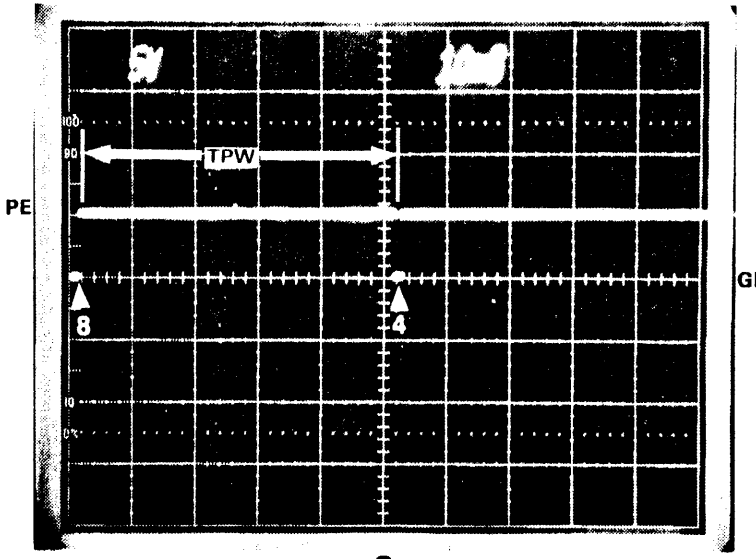
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0017

SCALE

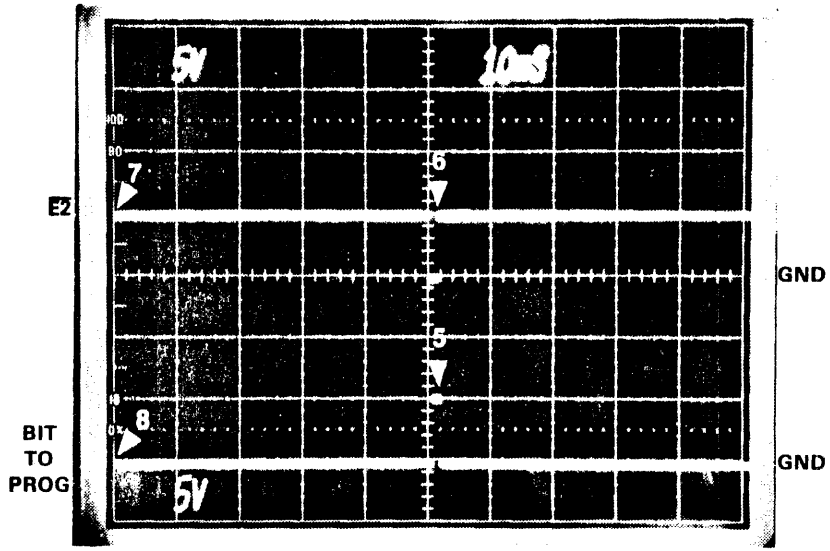
SHEET 1/1


7
10V
VPP
6
10mS
VPP
GND
BIT
NO
PROG
GND
10V

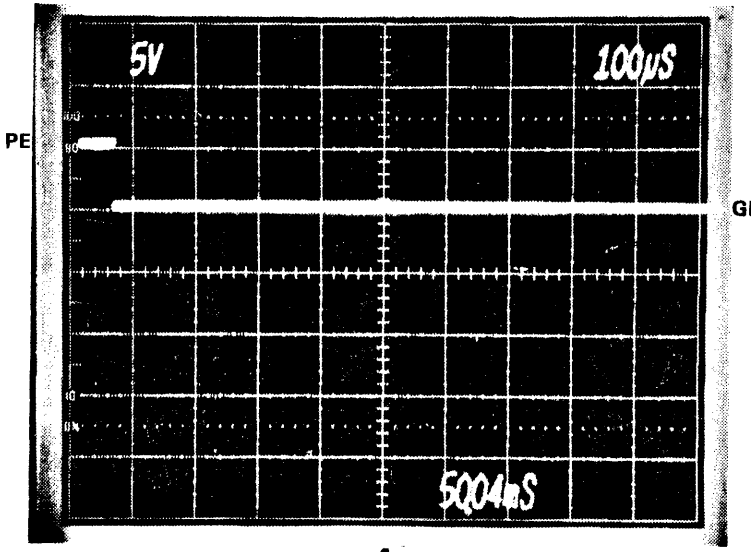
1


5V
TPW
PE
GND
8
4

3


5V
10mS
E2
7
6
GND
5
BIT
TO
PROG
8
GND
5V

2


5V
100µS
PE
GND
500µS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Use pinout 23 to observe these waveforms.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	48	50	52	ms	
TD	2	—	—	µs	
TR	.05	—	—	µs	
TF	.05	—	—	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

10-0500-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RLA	TEB	3-20-82
	B	ECN 3812	EF	MMR	9-26-80
	C	ECN #4376		FJC	1-14-82
	D	ECN #4630		WJB	7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 19, 20

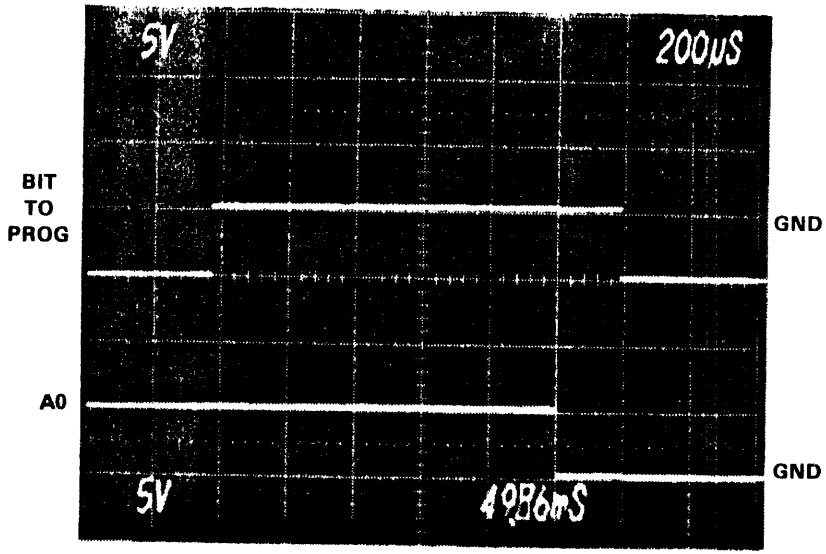
DRAWN BY:

CHECKED BY:

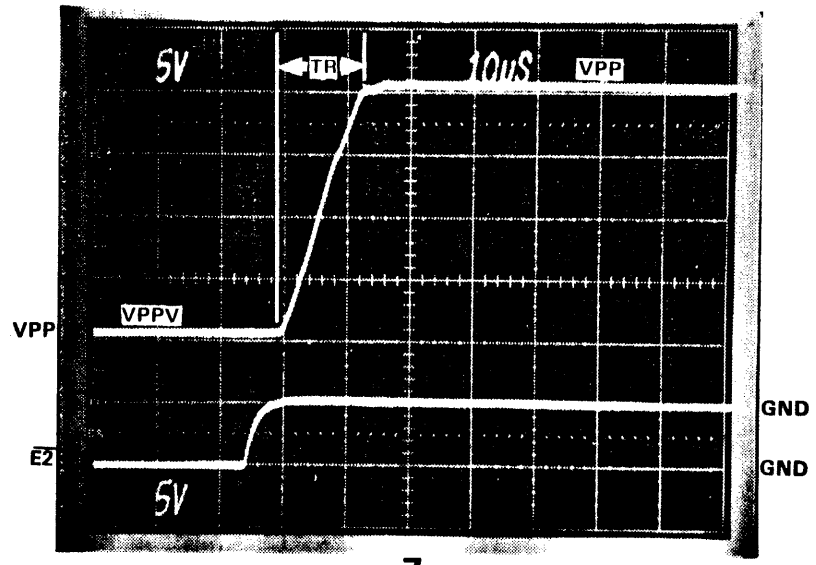
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0019

SCALE

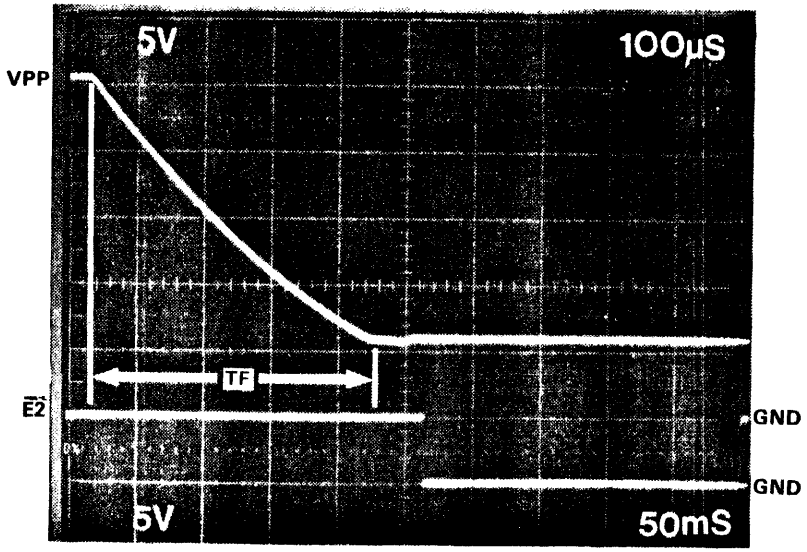
SHEET 1/2


5V
200µS
BIT
TO
PROG
GND
A0
GND
5V
4.986mS

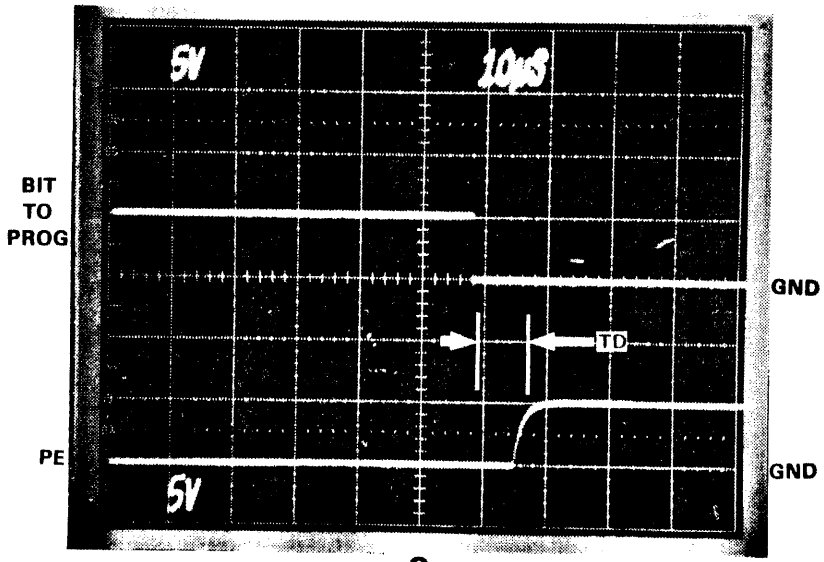
5


5V
TR
10µS
VPP
VPP
VPPV
GND
E2
GND
5V

7


5V
100µS
VPP
TF
E2
GND
GND
5V
50mS

6


5V
10µS
BIT
TO
PROG
GND
TD
PE
GND
5V

8

4-65
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 19, 20

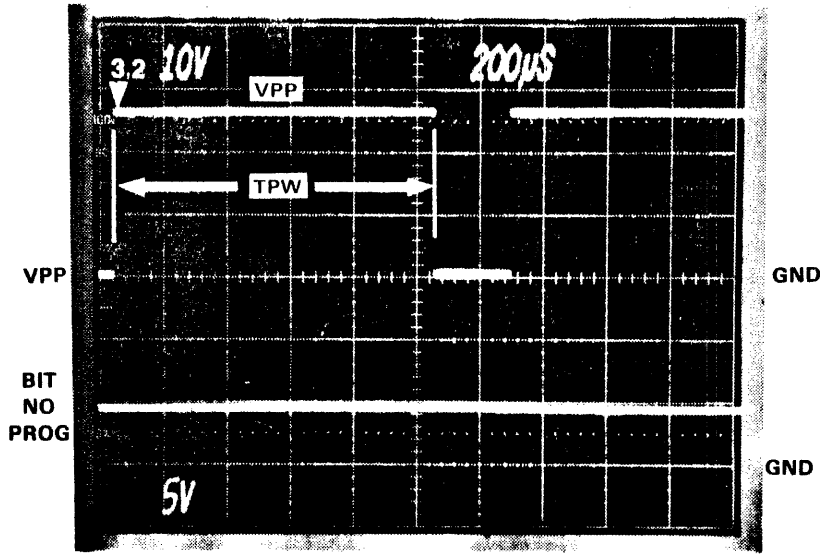
DRAWN BY:

CHECKED BY:

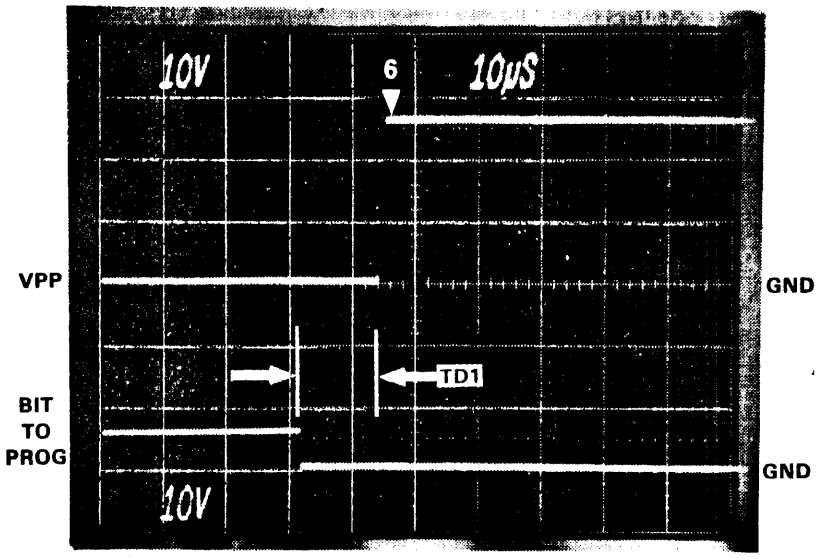
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0019

SCALE

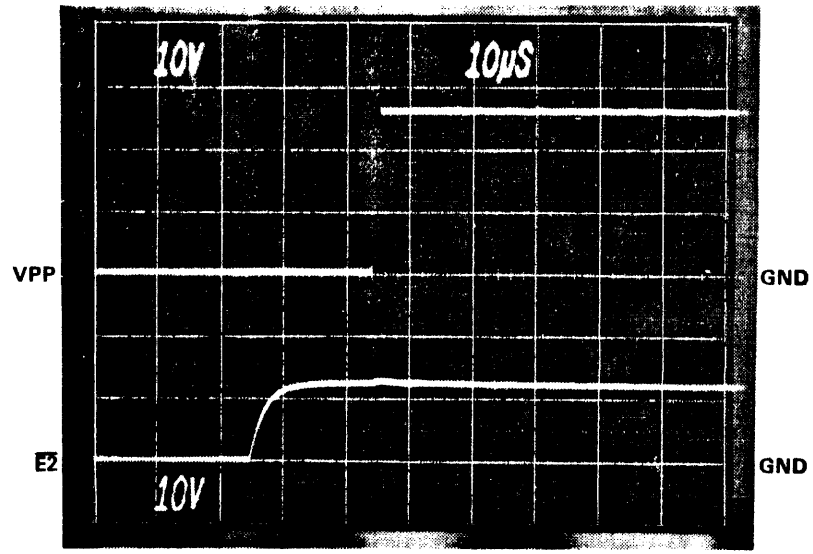
SHEET 2/2


3.2
10V
VPP
200µS
TPW
VPP
GND
BIT
NO
PROG
GND
5V

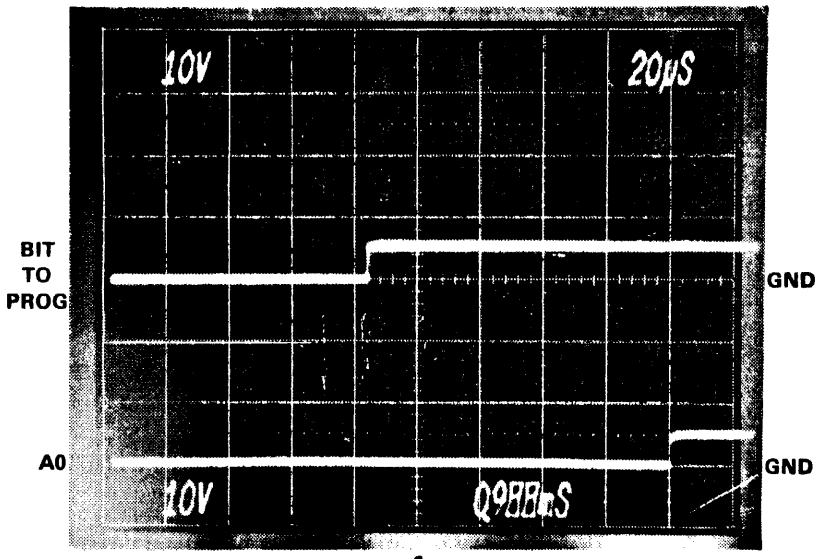
1


10V
6
10µS
VPP
GND
TD1
BIT
TO
PROG
GND
10V

2


10V
10µS
VPP
GND
E2
GND
10V

3


10V
20µS
BIT
TO
PROG
GND
A0
GND
10V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VBB	−5.25	−5.0	−4.75	V	Not Shown
VDD	11.4	12.0	12.6	V	Not Shown
VPP	25.0	26.0	27.0	V	
VEP	11.4	12.0	12.6	V	
TPW	.8	1.0	1.2	ms	
TR	.5	1.0	2.0	µs	
TF	.5	1.0	2.0	µs	
TD1	10	—	—	µs	
TD2	1	—	—	µs	
REJECT		100		LOOPS*	* Loop is defined as complete pass from address 0 to max device address applying 1 pulse at each address.
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			
	B	ECN #4376		FJC	1-18-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 21, 22

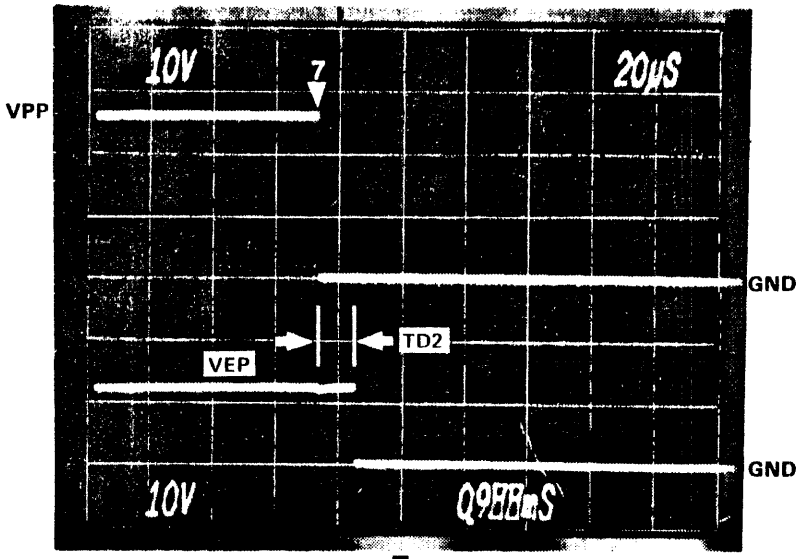
DRAWN BY:

CHECKED BY:

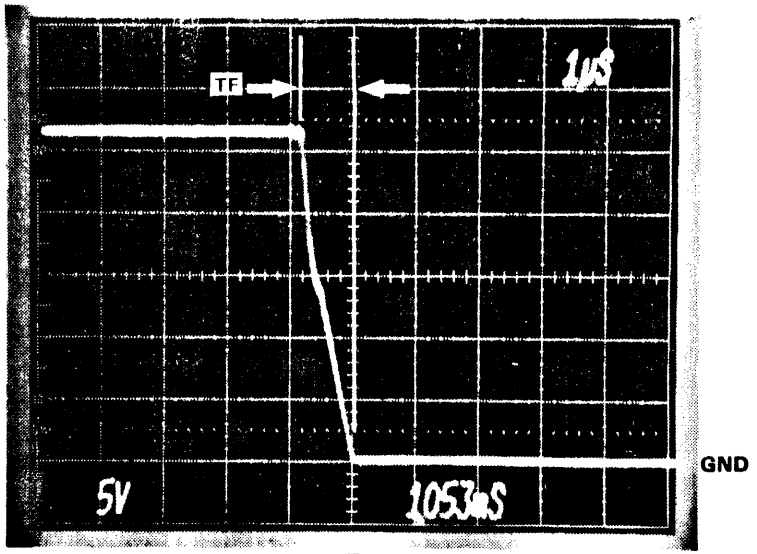
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0021

SCALE

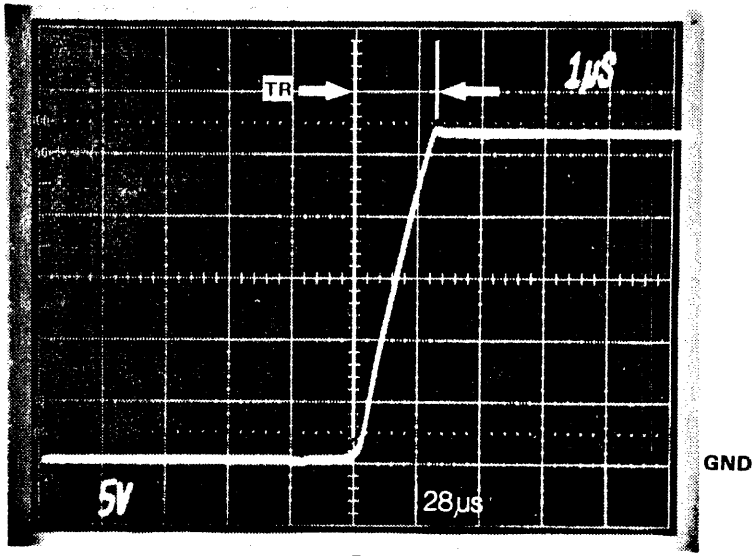
SHEET 1/2


10V
7
20µS
VPP
GND
VEP
TD2
GND
10V

5


TF
1µS
VPP
GND
5V

7


TR
1µS
VPP
GND
5V
28µs

6

4-69
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 21, 22

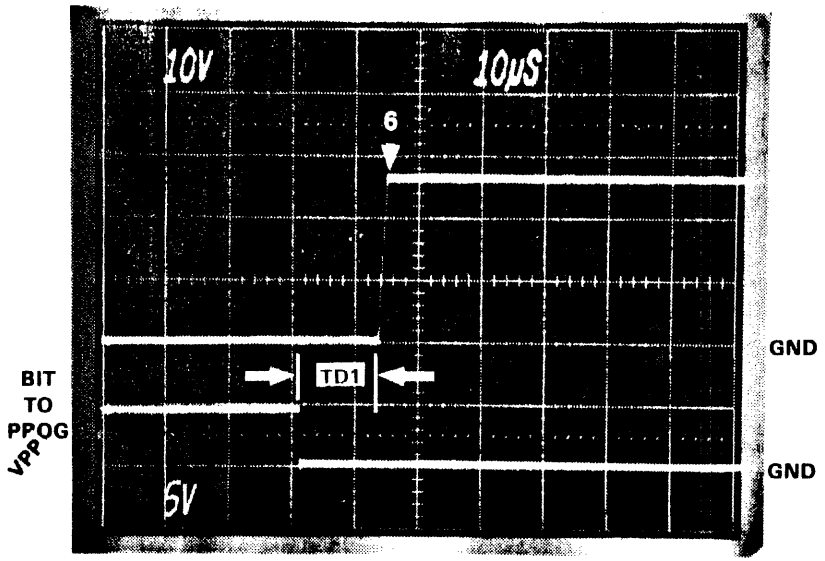
DRAWN BY:

CHECKED BY:

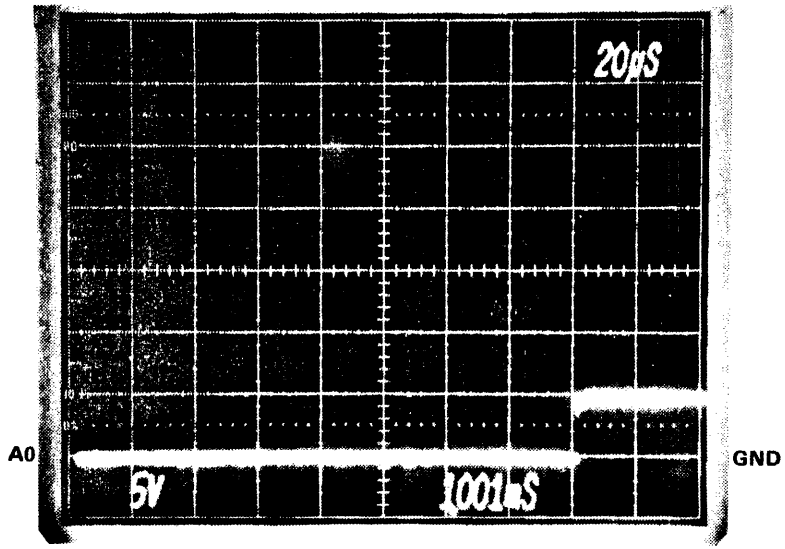
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0021

SCALE

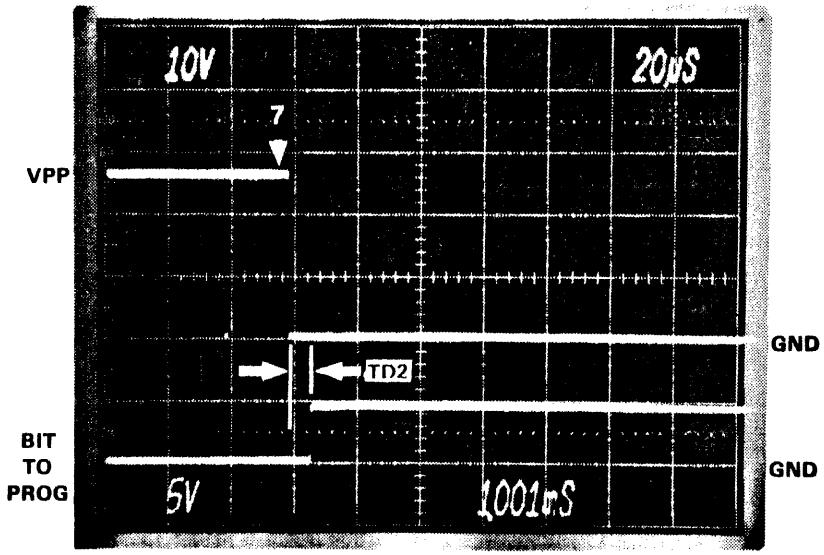
SHEET 2/2


10V
10µS
6
BIT
TO
PPOG
VPP
TD1
GND
GND
5V

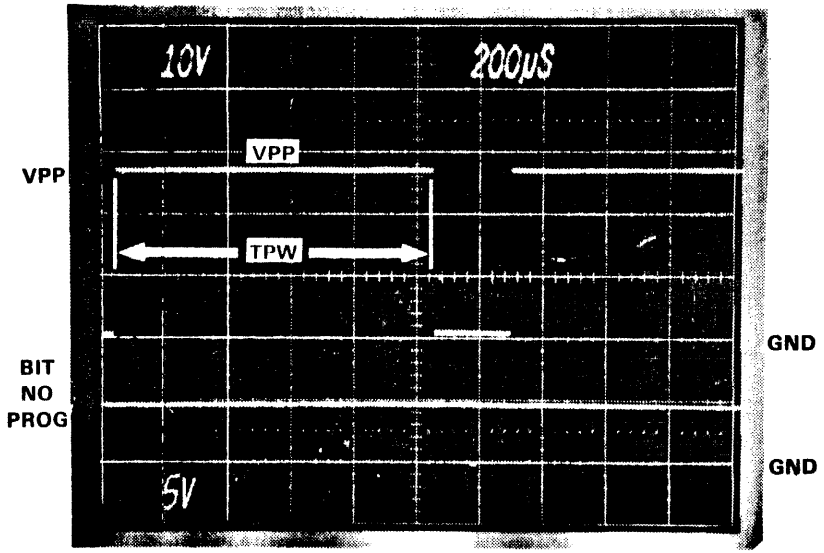
1


20µS
A0
GND
5V
1001mS

2


10V
20µS
7
VPP
GND
TD2
BIT
TO
PROG
GND
5V
1001mS

3


10V
200µS
VPP
VPP
TPW
GND
BIT
NO
PROG
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	11.4	12.0	12.6	V	
VBB	−5.25	−5.0	−4.75	V	
VDD	11.4	12.0	12.6	V	
VPP	25.0	26.0	27.0	V	
TPW	.8	1	1.2	ms	
TR	.5	1.0	2.0	µs	
TF	.5	1.0	2.0	µs	
TD1	10	—	—	µs	
TD2	1	—	—	µs	
REJECT		100		LOOPS*	* = loop is defined as a complete pass from address 0 to max device address, applying 1 pulse at each address.
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 23, 24

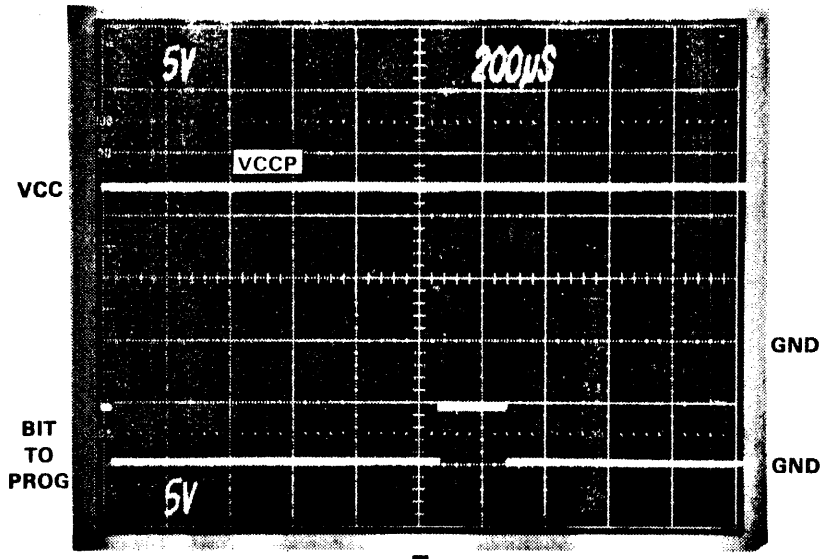
DRAWN BY:

CHECKED BY:

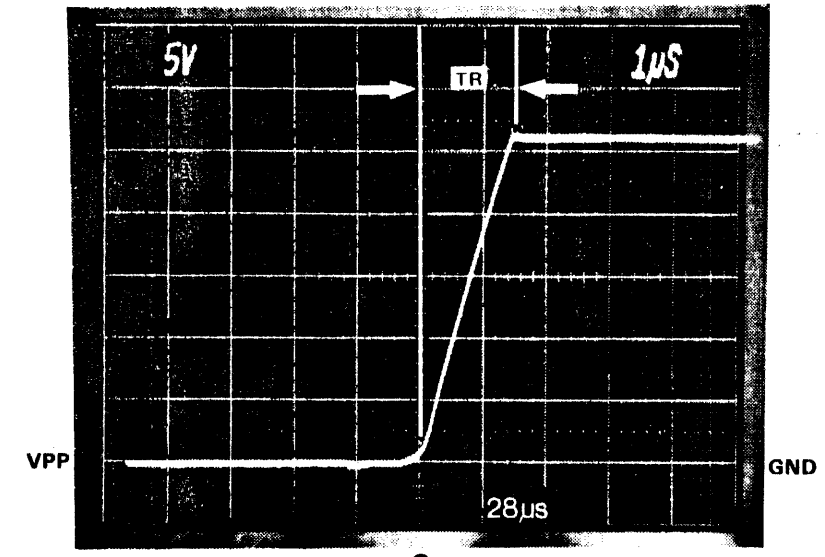
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0023

SCALE

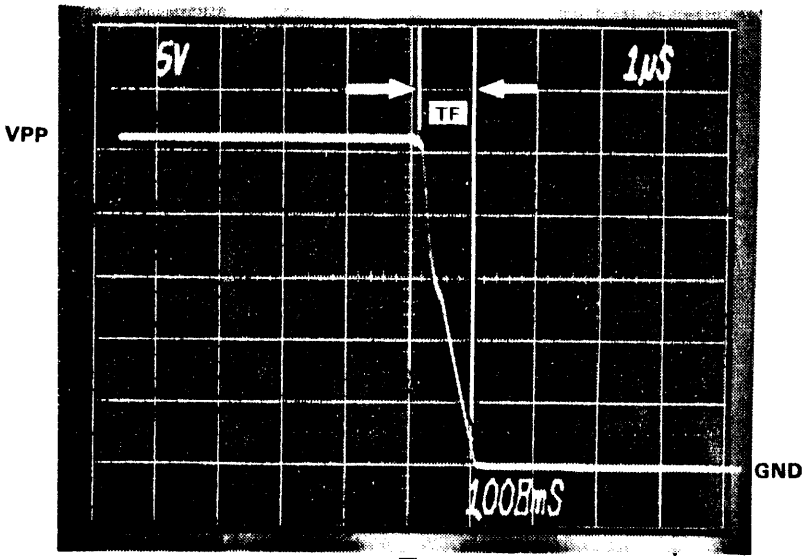
SHEET 1/2


5V
200µS
VCCP
VCC
GND
BIT
TO
PROG
GND
5V

5


5V
TR
1µS
VPP
GND
28µs

6


5V
TF
1µS
VPP
GND
100mS

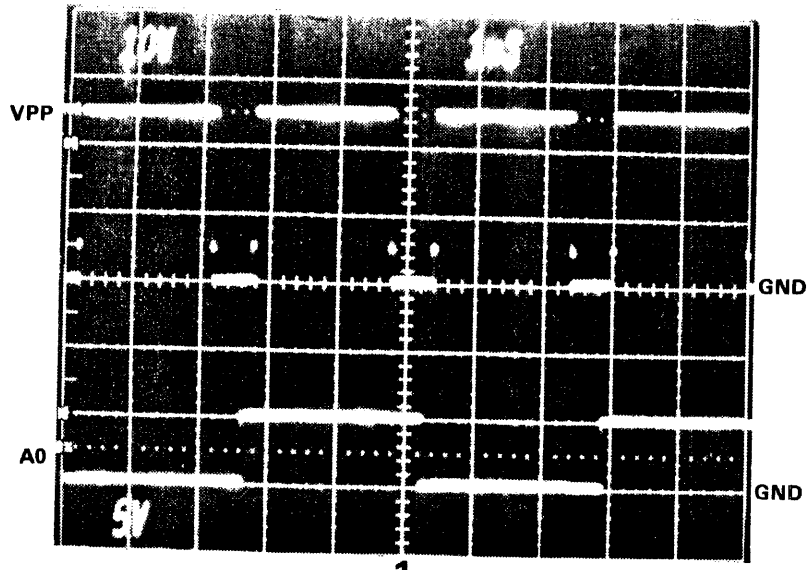
7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

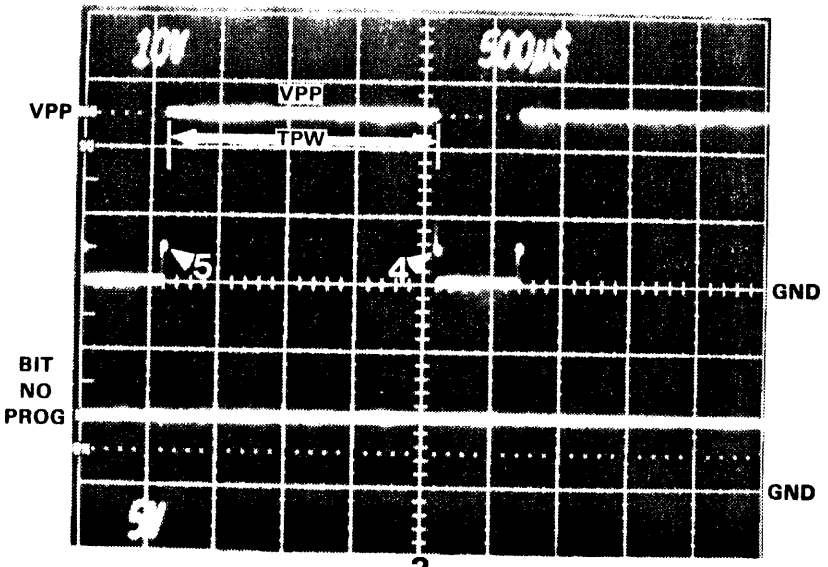
DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 23, 24		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 007-0023
SCALE		SHEET 2/2

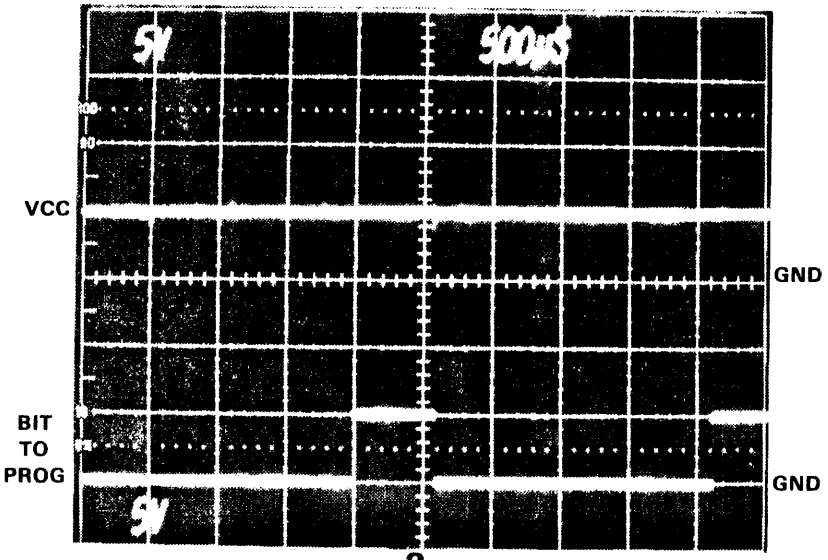
10-960-0099 4-73


10V
1mS
VPP
GND
A0
GND
5V

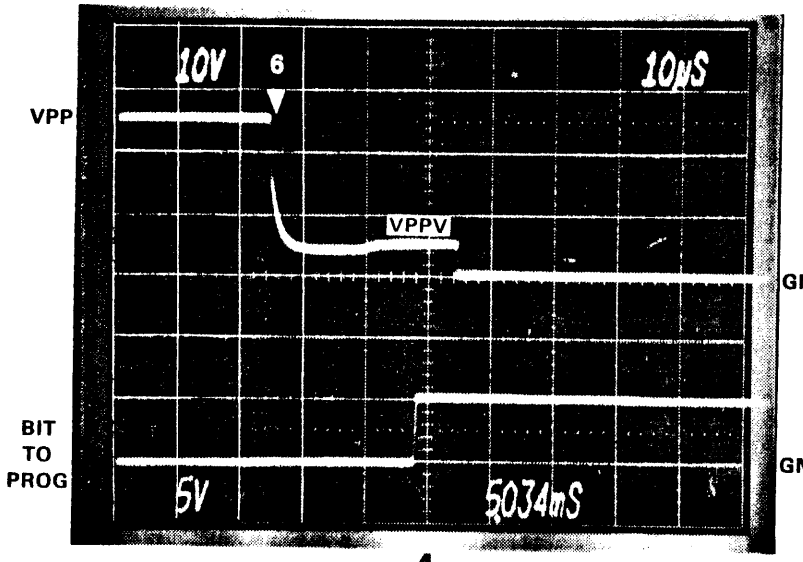
1


10V
500mS
VPP
VPP
TPW
5
4
GND
BIT
NO
PROG
GND
5V

3


5V
900mS
VCC
GND
BIT
TO
PROG
GND
5V

2


10V
6
10μS
VPP
VPPV
GND
BIT
TO
PROG
GND
5V
5.034mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	
VPP	24	25	26	V	
VPPV	4.6	5.0	5.4	V	
TPW	1.8	2.0	2.2	ms	
TR	0.5	1.0	2.0	µs	
TF	0.5	1.0	5.0	µs	
REJECT		10		PULSES	
OVERPROGRAM		X		PULSES	X = maximum number of pulses applied to any address for first verify.

10-950-0069

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			
	B	ECN #3880		FJC	2-10-81
	C	ECN #4376		FJC	1-14-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 25, 26

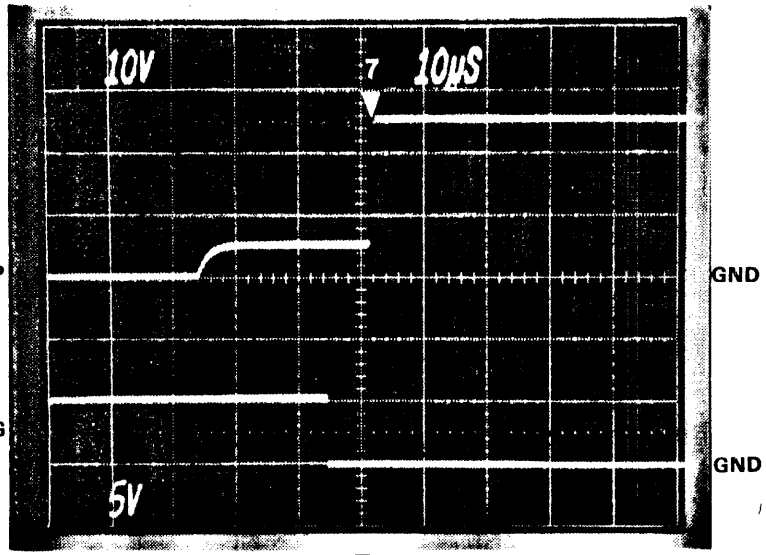
DRAWN BY: KJ

CHECKED BY:

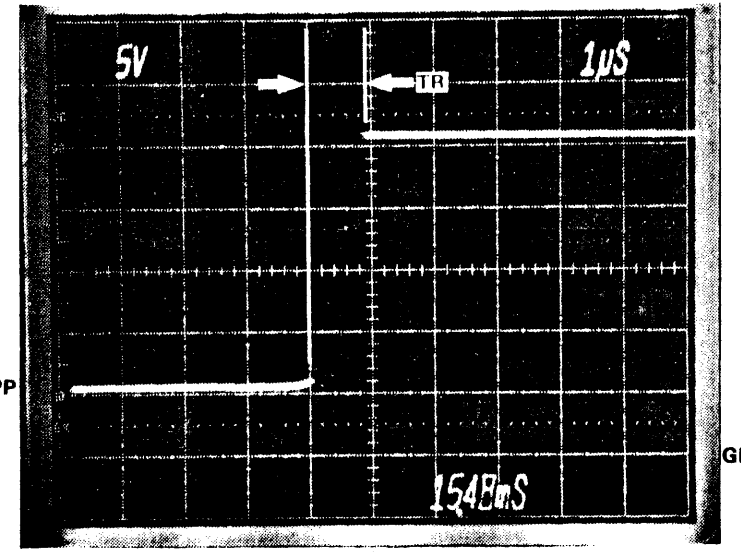
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0025

SCALE

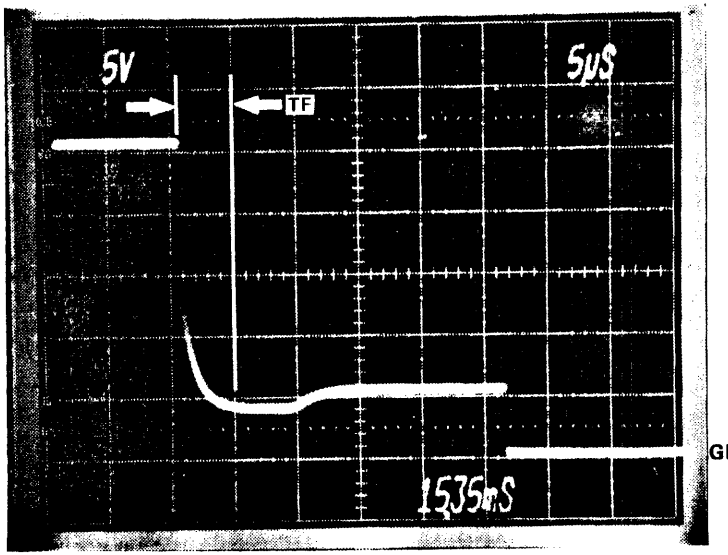
SHEET 1/2


10V
7
10µS
VPP
GND
BIT
TO
PROG
GND
5V

5


5V
TR
1µS
VPP
GND
154mS

7


5V
TF
5µS
VPP
GND
153.5mS

6

4-77
10-950-0069

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 25, 26

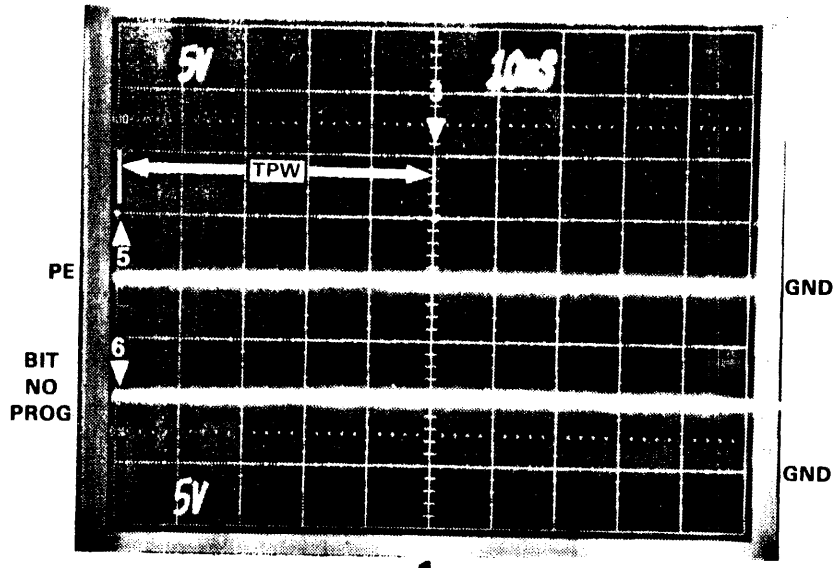
DRAWN BY:

CHECKED BY:

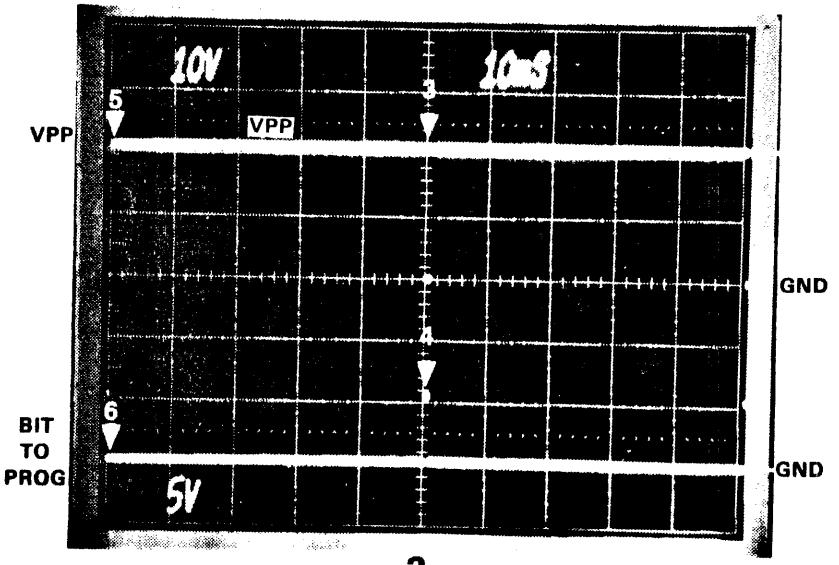
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0025

SCALE

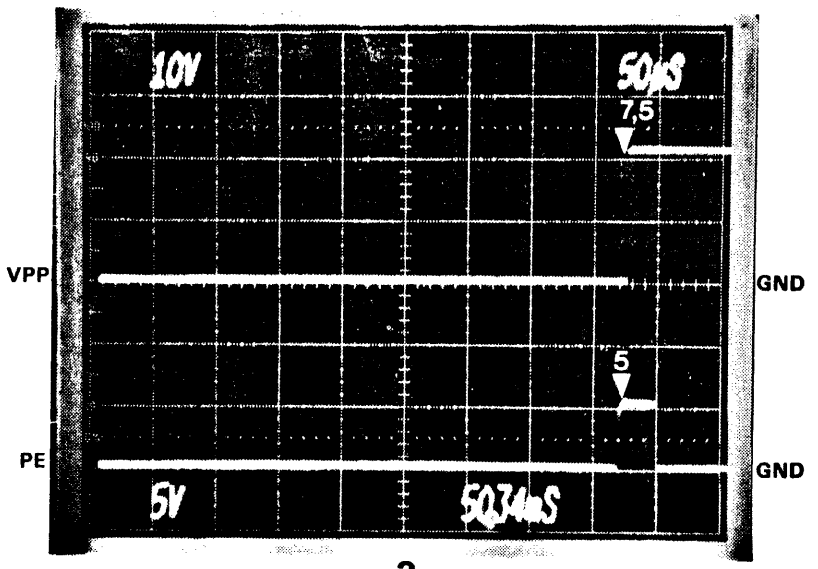
SHEET 2/2


5V
10mS
TPW
PE
BIT
NO
PROG
GND
GND
5V

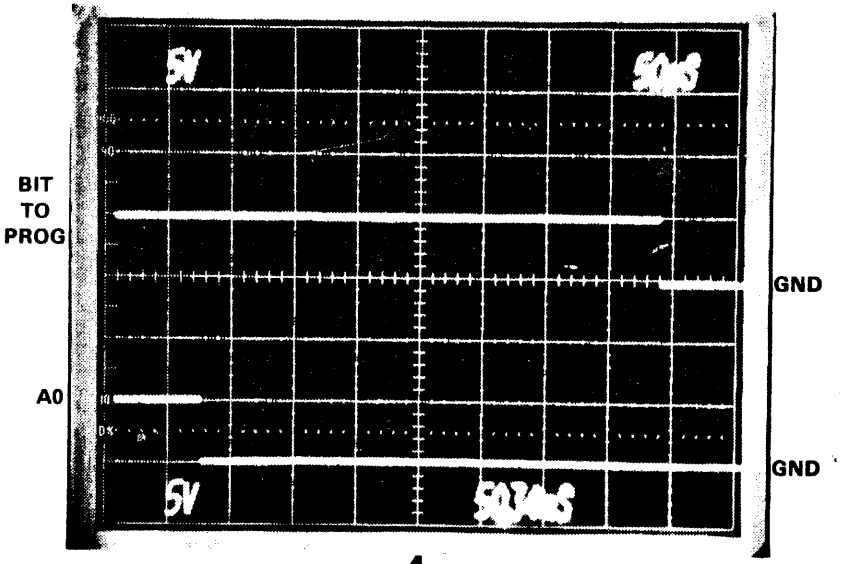
1


10V
10mS
VPP
VPP
BIT
TO
PROG
GND
GND
5V

2


10V
50µS
7,5
VPP
5
PE
GND
GND
5V
50µS

3


5V
50µS
BIT
TO
PROG
A0
GND
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.00	5.25	V	Not Shown
VPP	20.5	21.0	21.5	V	
TOES	2	—	—	µs	
TPW	48	50	52	ms	
TR	50	—	—	ns	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			3-20-81
	B	ECN #4376		FJC	1-14-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 27, 28

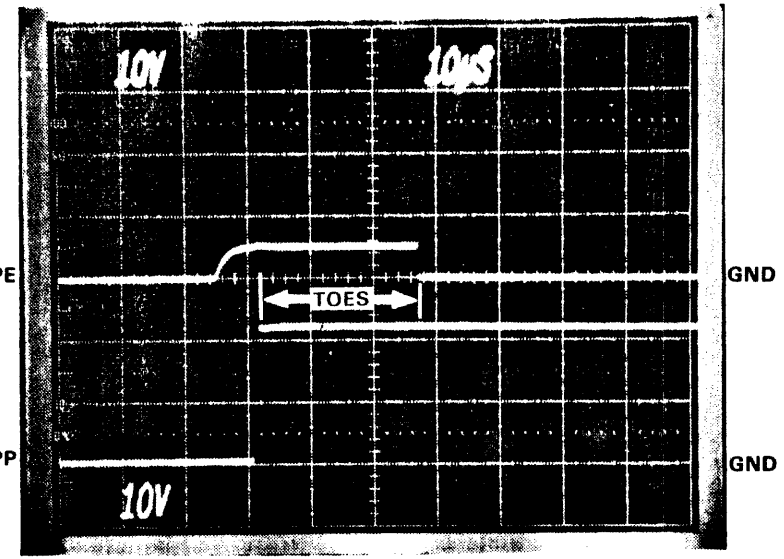
DRAWN BY:

CHECKED BY:

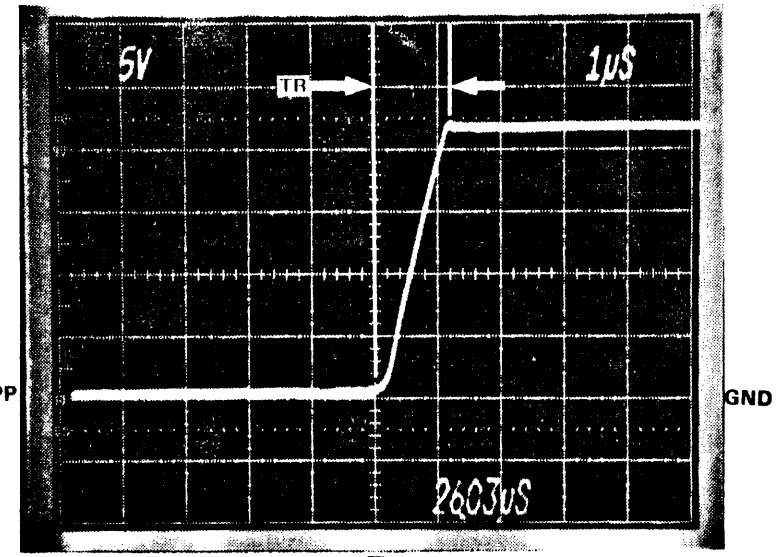
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0027

SCALE

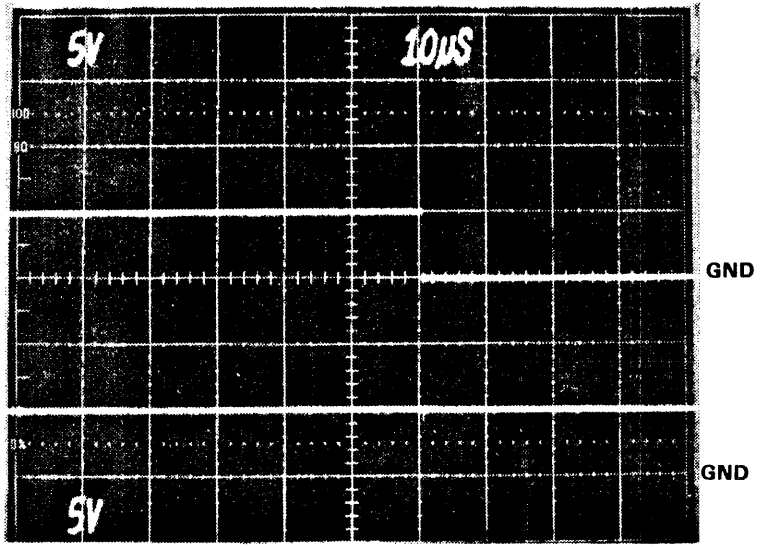
SHEET 1/2


10V
10µS
PE
TOES
GND
VPP
GND
10V

5


5V
TR
1µS
VPP
GND
2603µS

7


5V
10µS
BIT
TO
PROG
GND
BIT
NO
PROG
GND
5V

6

4-81
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 27, 28

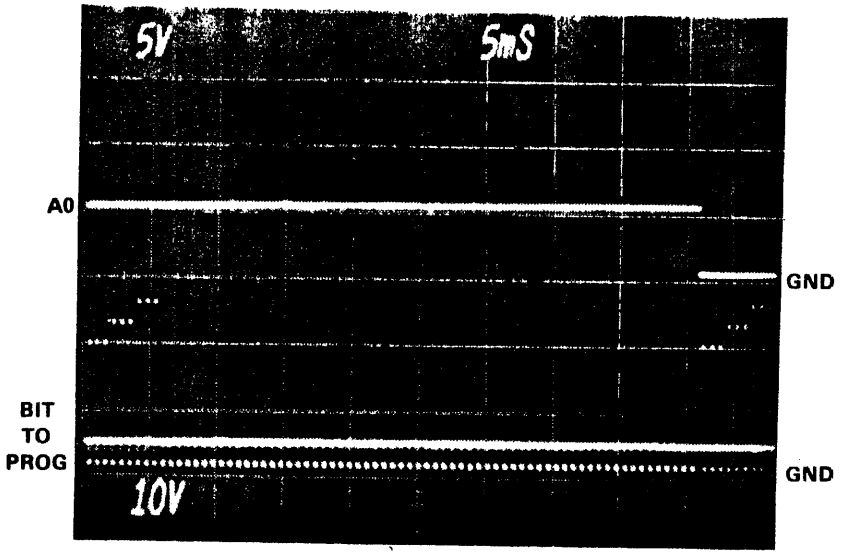
DRAWN BY:

CHECKED BY:

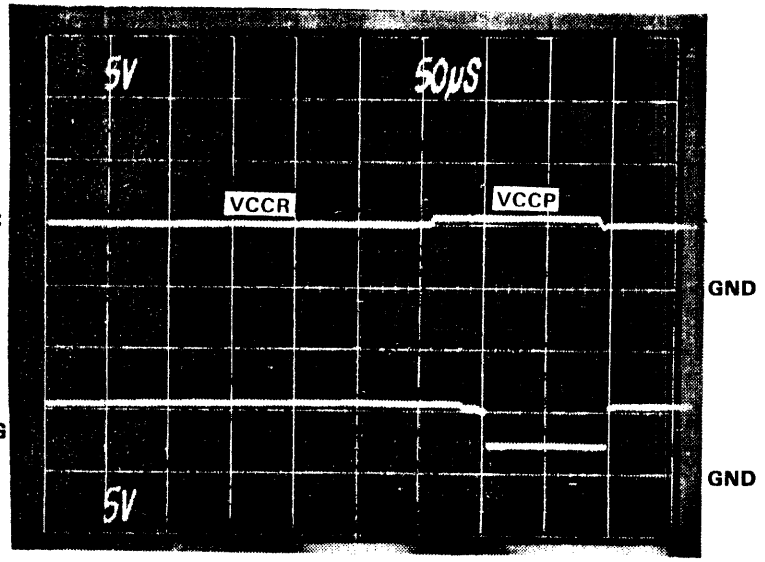
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0027

SCALE

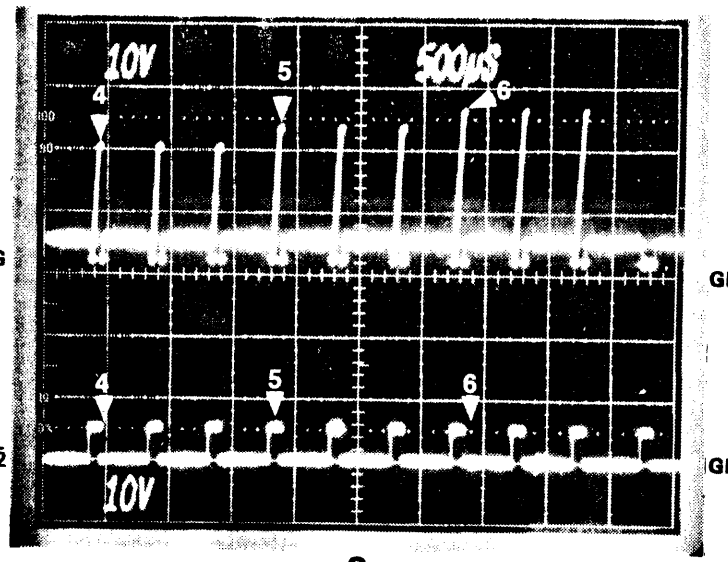
SHEET 2/2


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

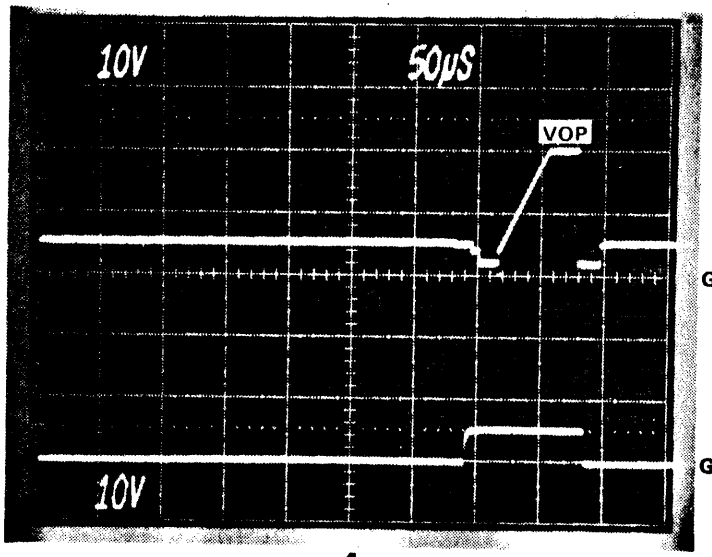
1


5V
50µS
VCC
VCCR
VCCP
GND
BIT
NO
PROG
GND
5V

2


10V
500µS
4
5
6
BIT
TO
PROG
GND
4
5
6
E2
GND
10V

3


10V
50µS
VOP
BIT
TO
PROG
GND
E2
GND
10V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

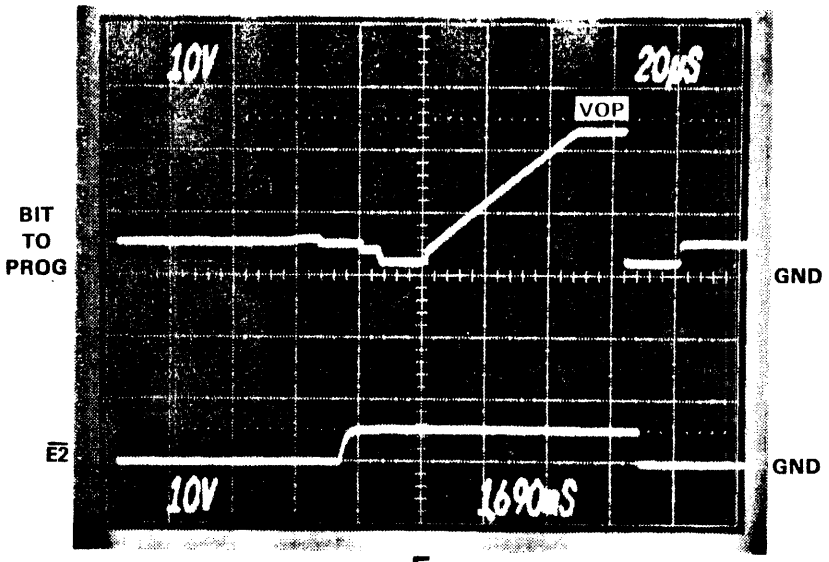
VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCR	4.75	5.0	5.25	V	
VCCP	4.75	5.5	5.25	V	
VOP	19	20	21	V	PULSE # 1-3
	22	23	24	V	PULSE # 4-6
	25	26	27	V	PULSE # 7-9
TPW	10		40	µs	
TR	.34	.4	.46	V/µs	
REJECT		9		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

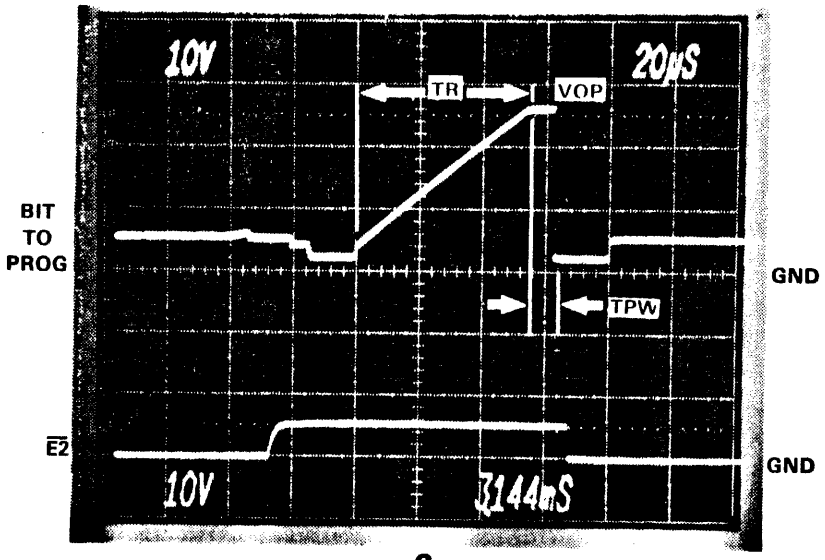
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE			3-20-82
	B	ECN #4376		FJC	1-14-82
	C	ECN #4630			7-20-82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 29, 30	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 007-0029	
SCALE	SHEET 1/2


10V
20µS
VOP
BIT
TO
PROG
GND
E2
GND
10V
1690mS

5


10V
20µS
TR
VOP
BIT
TO
PROG
GND
TPW
E2
GND
10V
3144mS

6

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10-950-0069

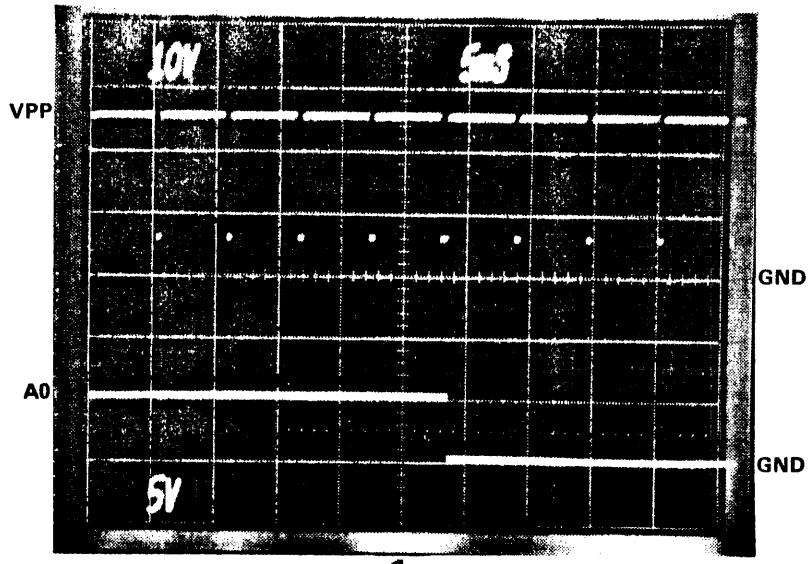
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.			

DATA I/O ISSAQUAH, WA

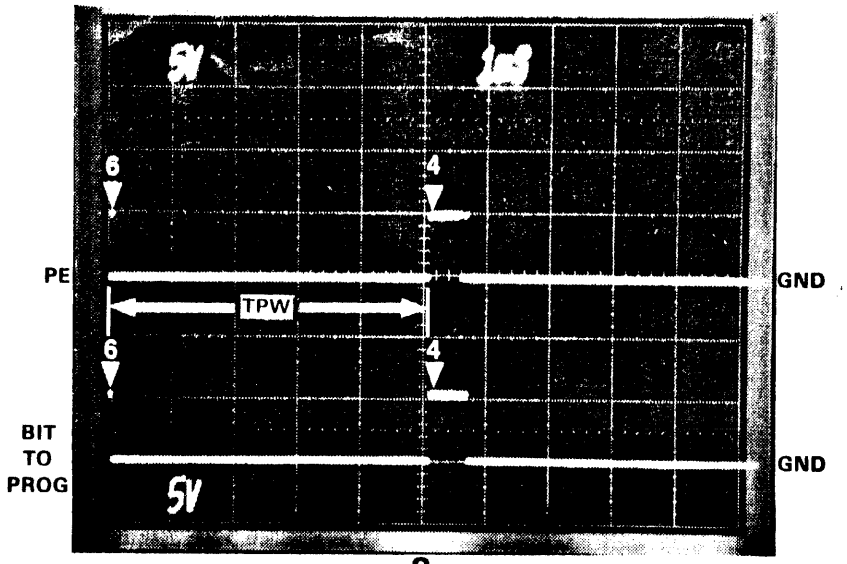
TITLE: TIMING DIAGRAM FAMILY CODES 29, 30	DRAWN BY: CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0029

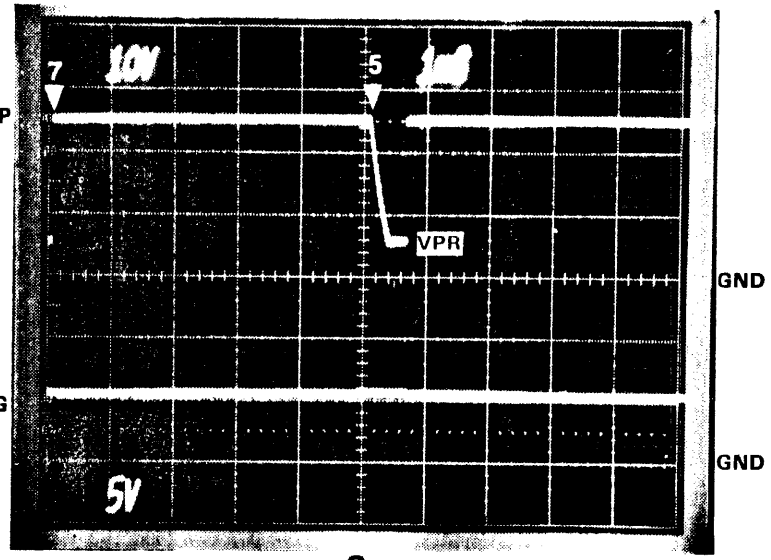
SCALE | SHEET 2/2


10V
5mS
VPP
GND
A0
GND
5V

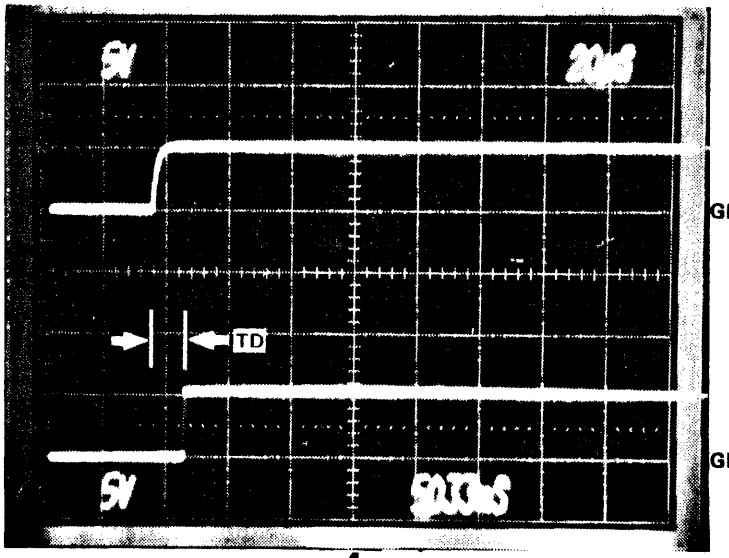
1


5V
1mS
6
4
PE
GND
TPW
6
4
BIT
TO
PROG
GND
5V

3


7
10V
5
1mS
VPP
VPR
GND
BIT
NO
PROG
GND
5V

2


5V
20mS
PE
GND
TD
BIT
TO
PROG
GND
5V
50mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	Not Shown
VPP	24	25	26	V	
VPR	4.75	5	5.25	V	
TPW	4.9	5	5.1	ms	
TD	2			µs	
REJECT		10		PULSES	
OVERPROGRAM		X		PULSES	X = maximum number of pulses applied to any address for first verify.

10-960-0099
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REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RAH	DEB	3-20-9

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 31, 32

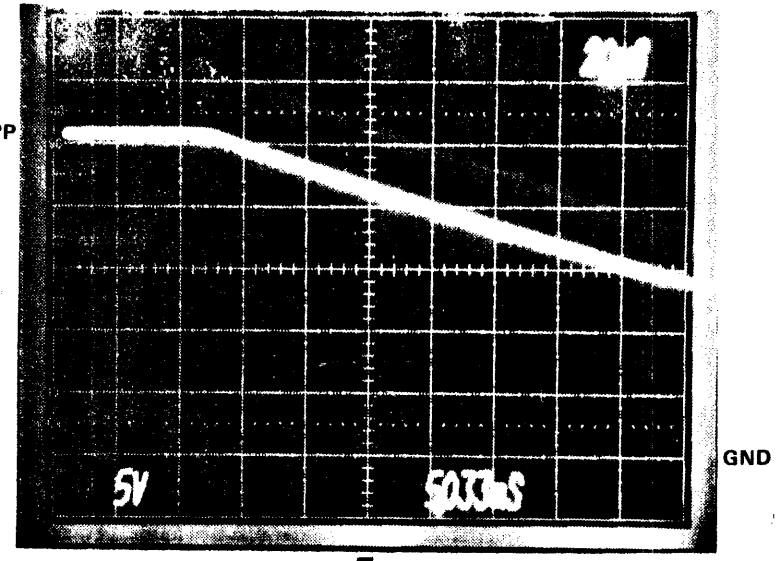
DRAWN BY:

CHECKED BY:

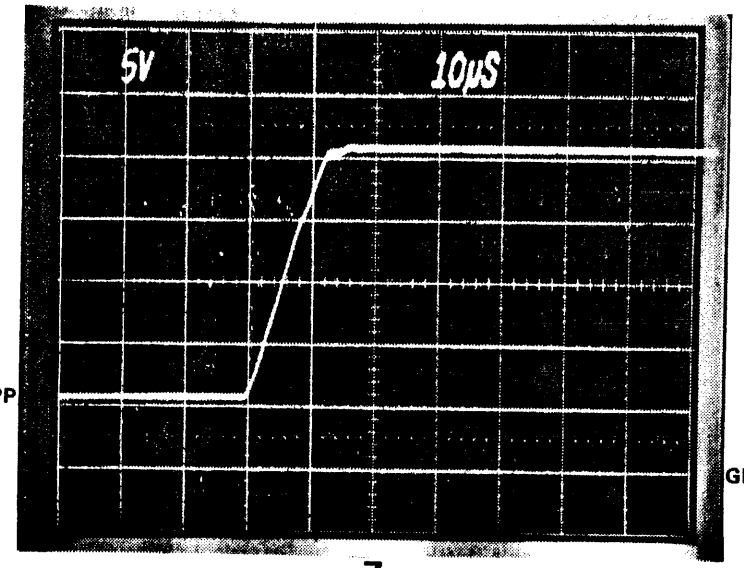
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0031

SCALE

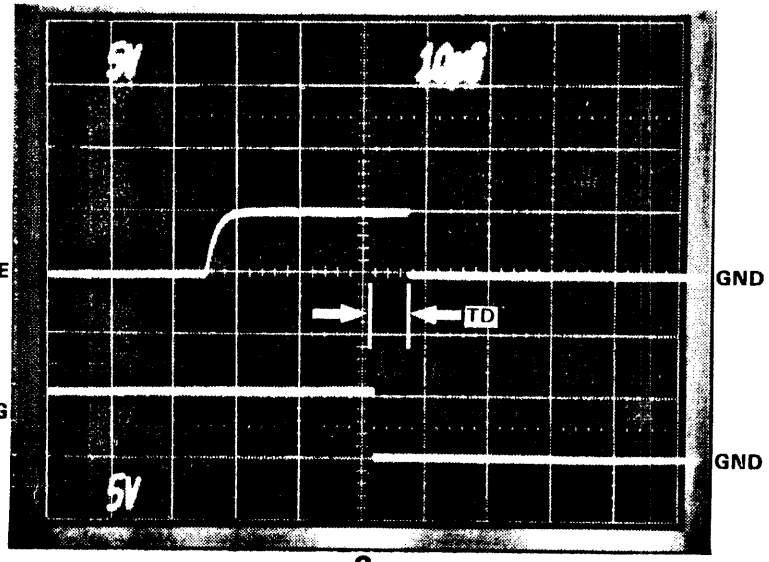
SHEET 1/2



5



7



6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 31, 32

DRAWN BY:

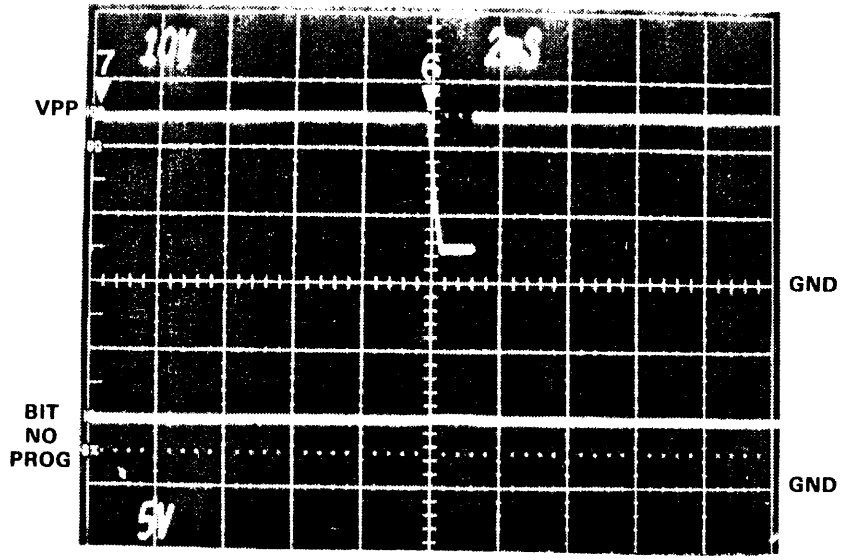
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0031

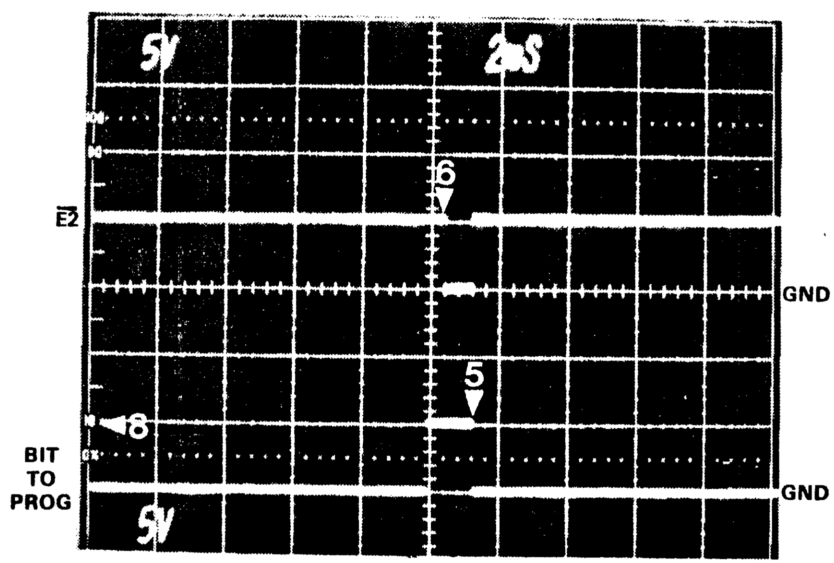
SCALE

SHEET 2/2

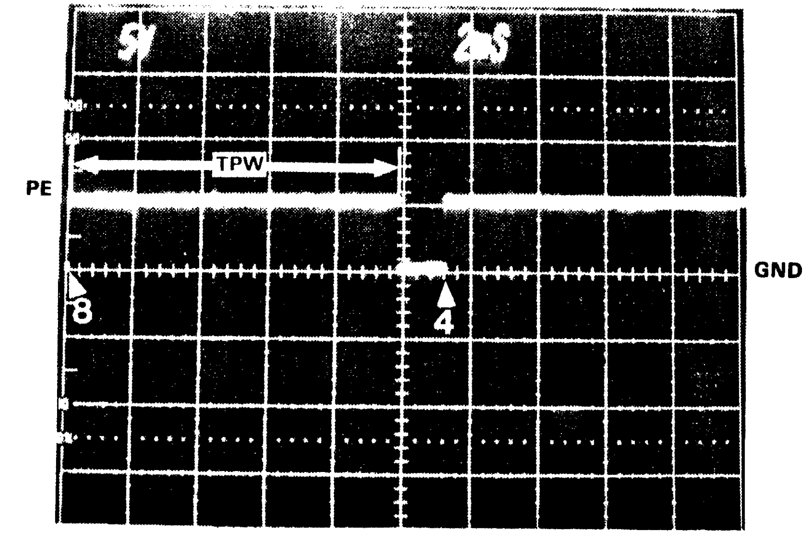
10-960-0099 4-89


10V
2mS
7
6
VPP
GND
BIT
NO
PROG
GND
5V

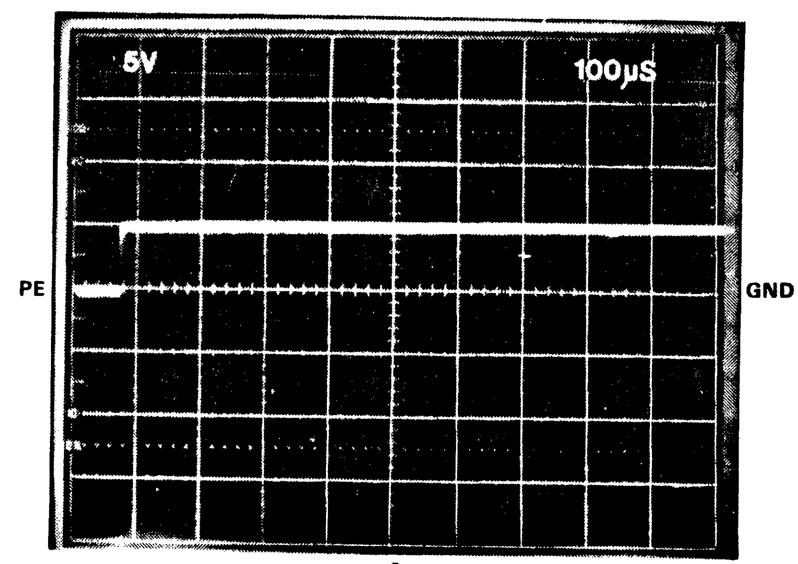
1


5V
2mS
6
E2
GND
5
8
BIT
TO
PROG
GND
5V

2


5V
2mS
TPW
PE
GND
8
4

3


5V
100μS
PE
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

6. *To observe this level, adjust time base.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	9.8	10	10.2	ms	
TD	2	—	—	µs	
TR	.05	—	—	µs	
TF	.05	—	—	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

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10-950-0069

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		EJC	2-10-81
	B	ECN #4376		EJC	1-14-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 33, 34

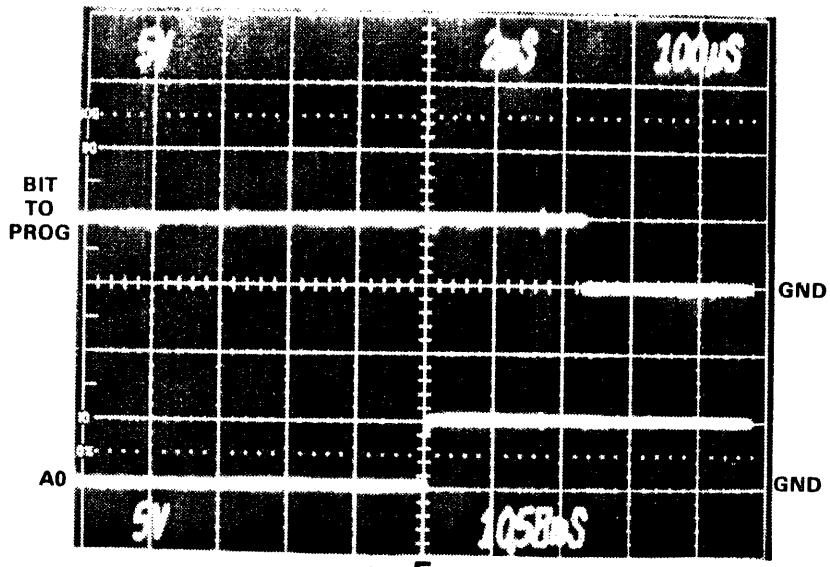
DRAWN BY: KJ

CHECKED BY:

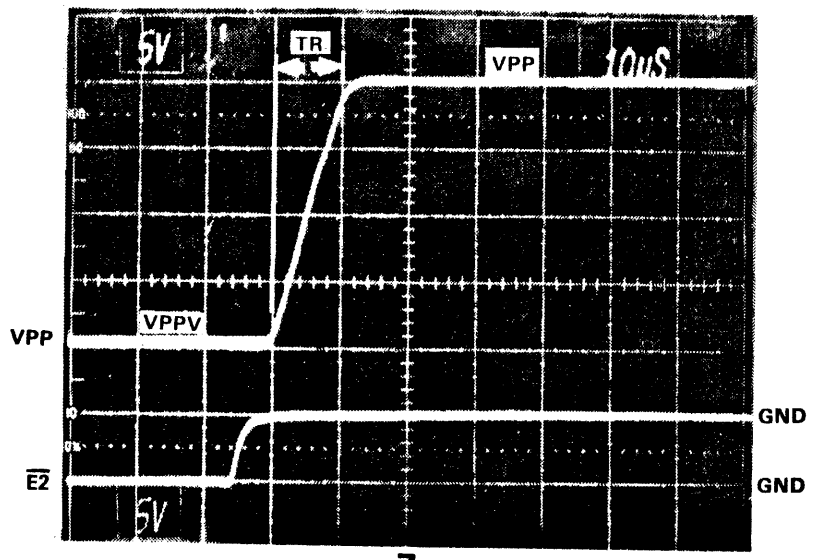
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0033

SCALE

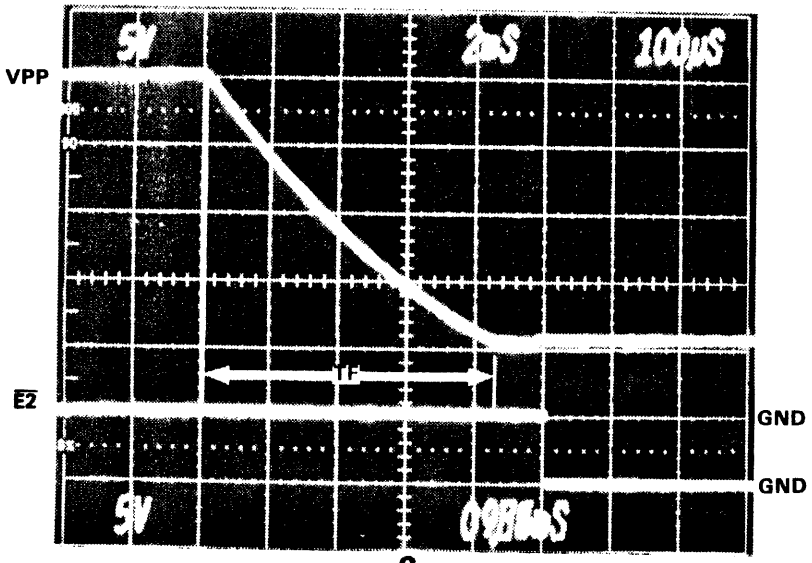
SHEET 1/2


5V
2mS
100µS
BIT
TO
PROG
GND
A0
GND
5V
105mS

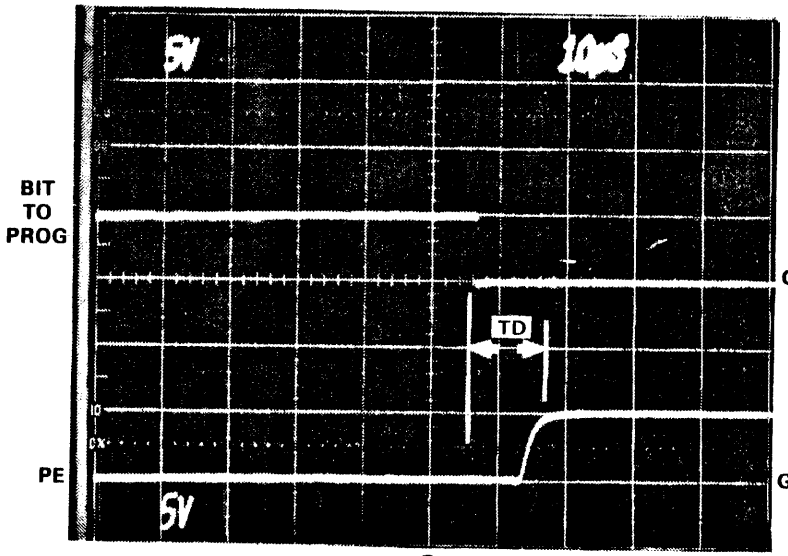
5


5V
TR
VPP
10uS
VPPV
VPP
GND
E2
GND
5V

7


5V
2mS
100µS
VPP
E2
TF
GND
GND
5V

6


5V
10mS
BIT
TO
PROG
GND
TD
PE
GND
5V

8

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10-950-0009

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.		RJC	2-10-81

DATA I/O ISSAQUAH, WA

TITLE

TIMING DIAGRAM
FAMILY CODES 33, 34

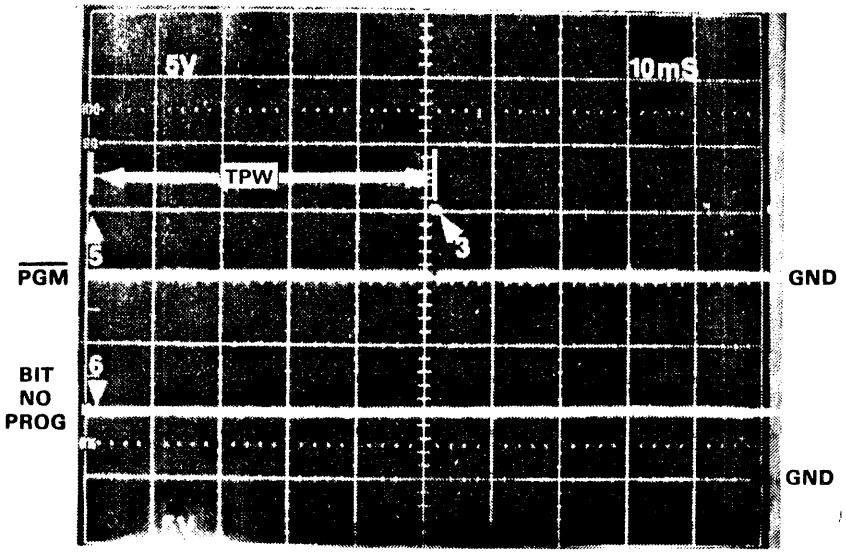
DRAWN BY: KJ

CHECKED BY: [illegible]

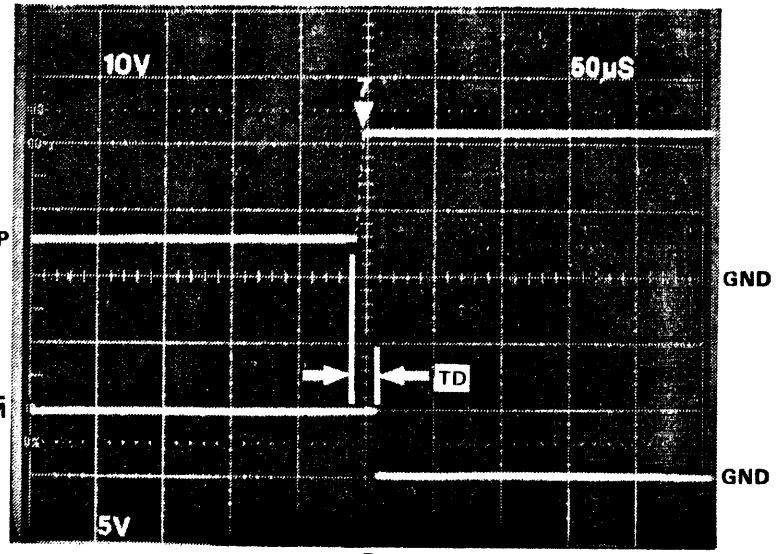
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0033

SCALE

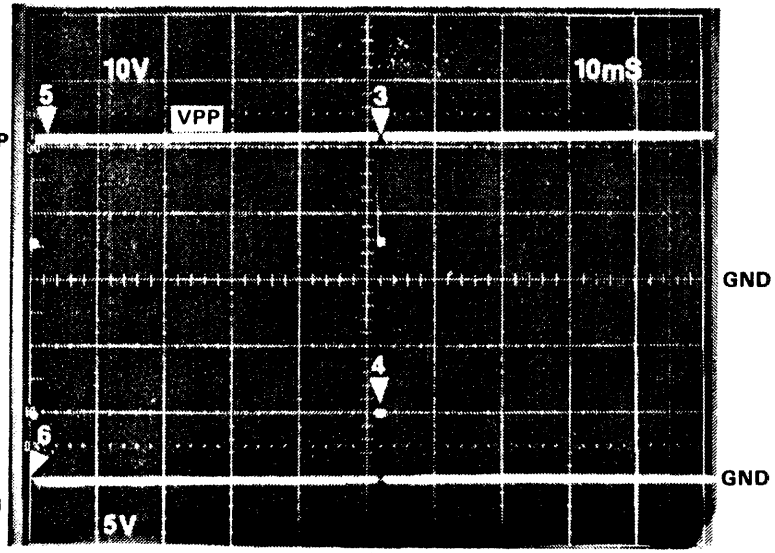
SHEET 2/2


5V
10mS
TPW
5
3
PGM
GND
6
BIT
NO
PROG
GND
5V

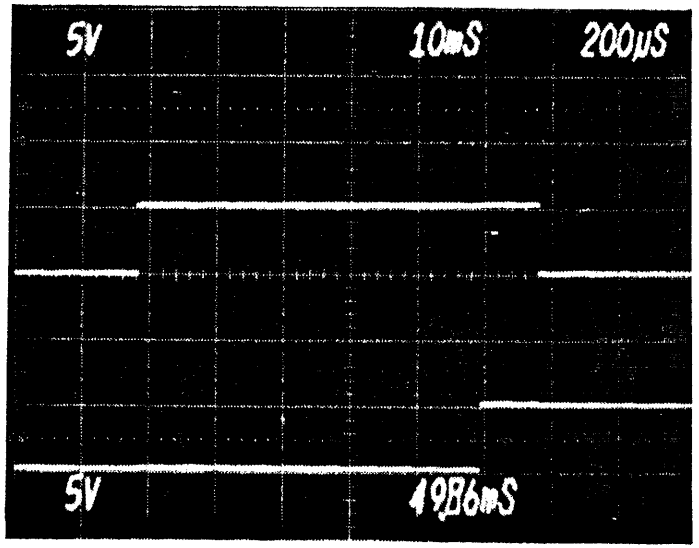
1


10V
50µS
VPP
GND
TD
PGM
GND
5V

3


10V
10mS
5
VPP
3
VPP
GND
4
6
BIT
TO
PROG
GND
5V

2


5V
10mS
200µS
BIT
TO
PROG
GND
A0
GND
5V
19.86mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.00	5.25	V	Not Shown
VPP	20.5	21.0	21.5	V	
TD	2	–	–	µs	
TPW	48	50	52	ms	
TR	50	–	–	ns	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		FJC	2-10-81
	B	ECN #4630		WBS	7-20-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 35, 36

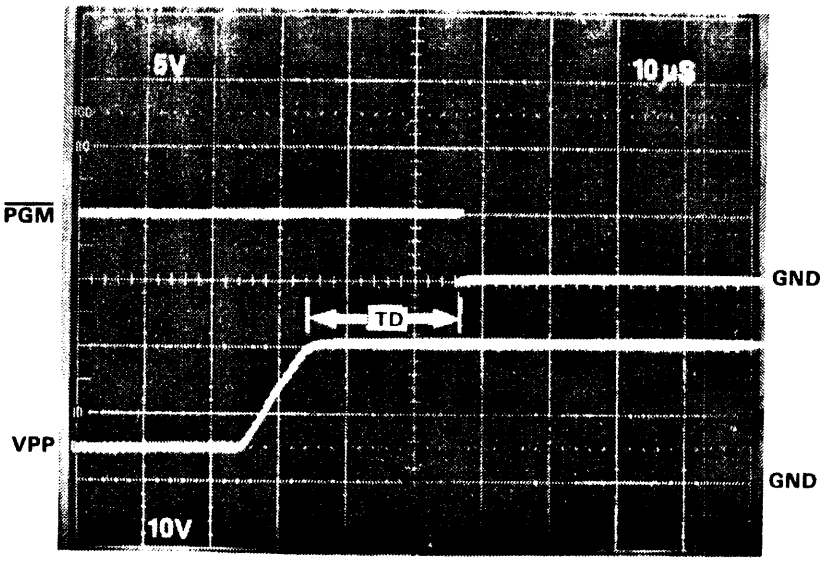
DRAWN BY: KJ.

CHECKED BY:

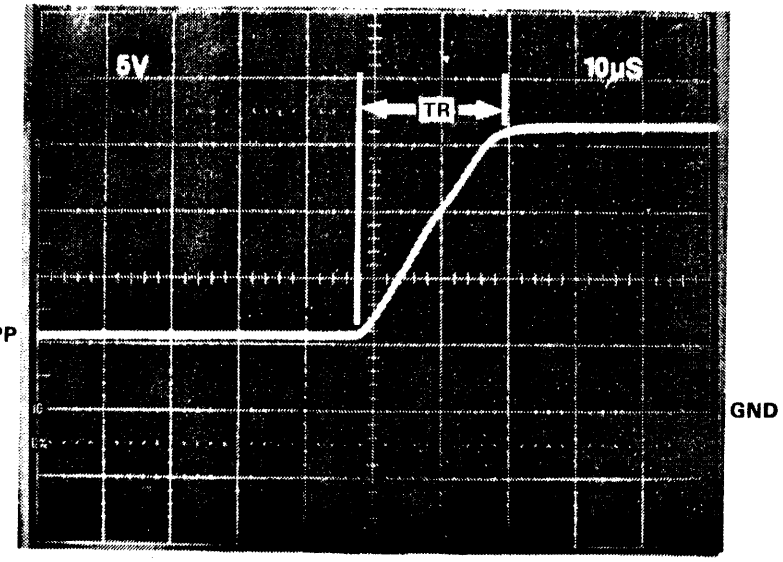
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0035

SCALE

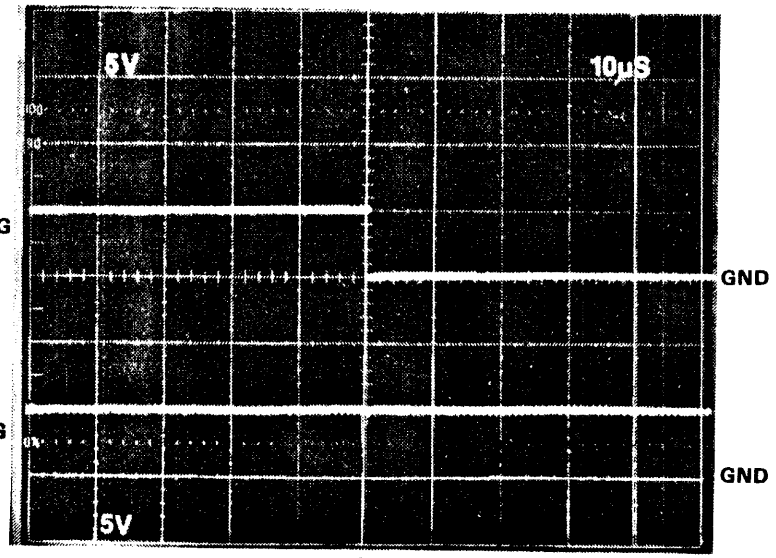
SHEET 1/2


5V
10µS
PGM
GND
TD
VPP
GND
10V

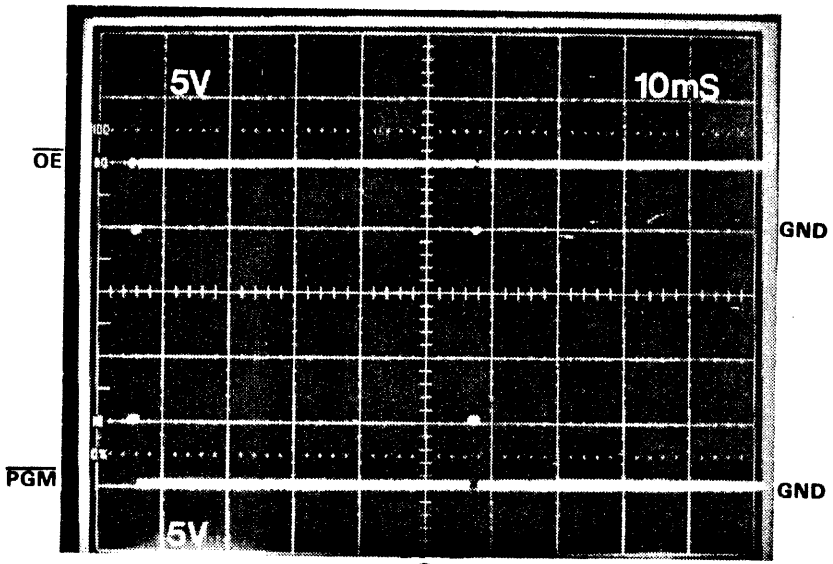
5


5V
10µS
TR
VPP
GND

7


5V
10µS
BIT
TO
PROG
GND
BIT
NO
PROG
GND
5V

6


5V
10mS
OE
GND
PGM
GND
5V

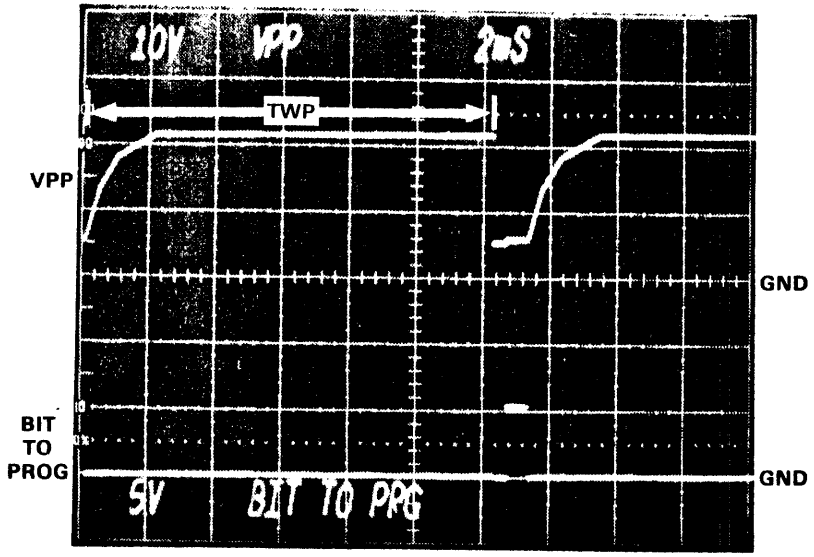
8

10-960-0099
4-87

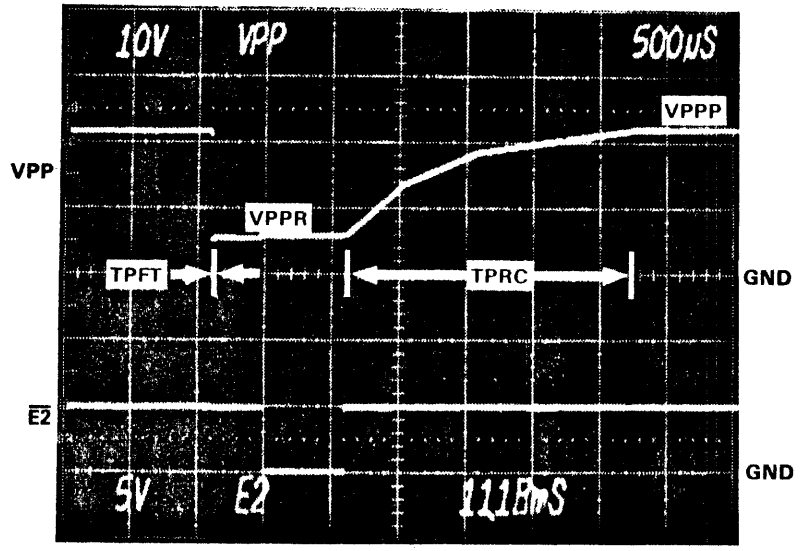
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1.		FJC	

DATA I/O ISSAQUAH, WA

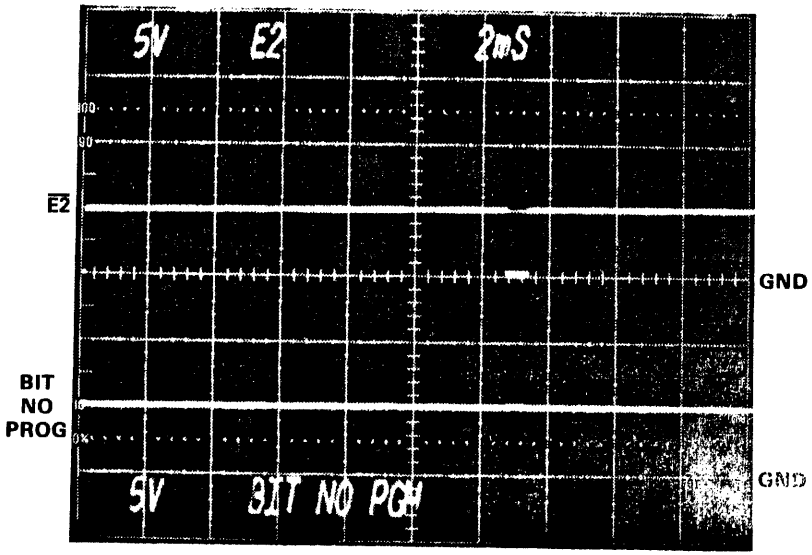
TITLE: TIMING DIAGRAM FAMILY CODES 35, 36		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 007-0035
SCALE		SHEET 2/2



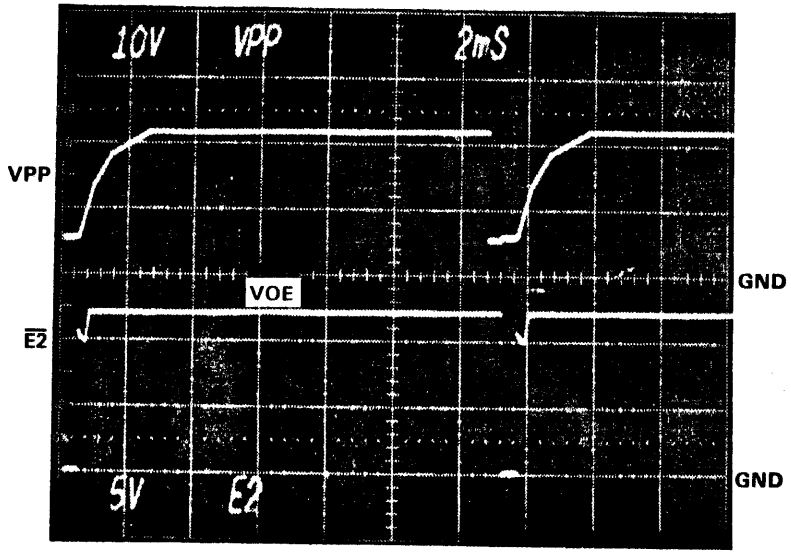
1



2



3



4
(ERASE CYCLE)

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact or a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no- bit-to-program, use O_3 for a 4-bit PROM Or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VPPP	20.0	21.0	22.0	V	
VPPR	4.0	4.6	6.0	V	
VCC	4.75	5.0	5.25	V	
VOE	9.0	12.0	15.0	V	
TWP	9.0	12.0	15.0	ms	
TPFT	—	—	100	µs	
TPRC	450	600	750	µs	effective time constant
OVERPROGRAM	—	0	—	PULSES	
REJECT	—	0	—	PULSES	

4-99
10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		MR	9/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODE 37, 38

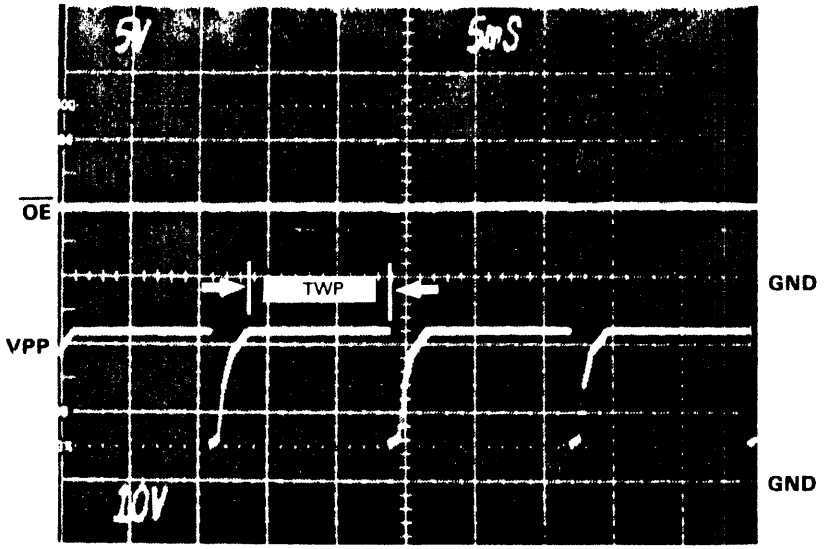
DRAWN BY:

CHECKED BY:

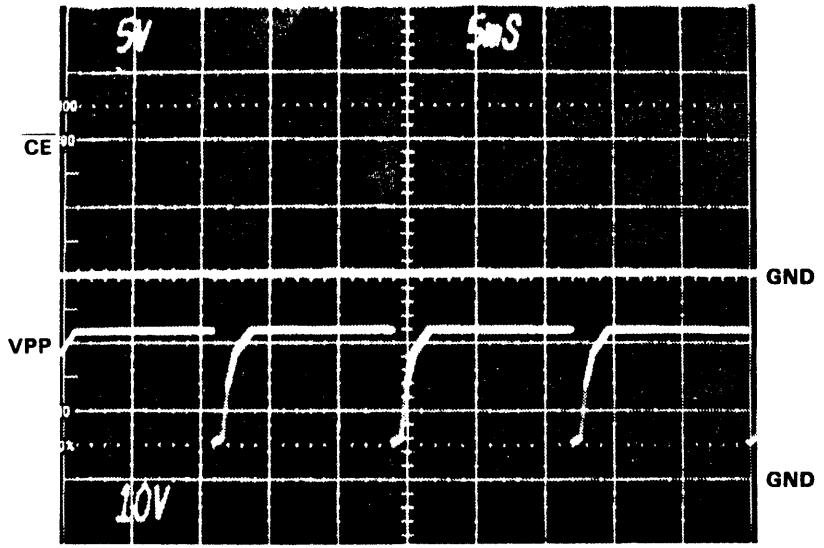
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

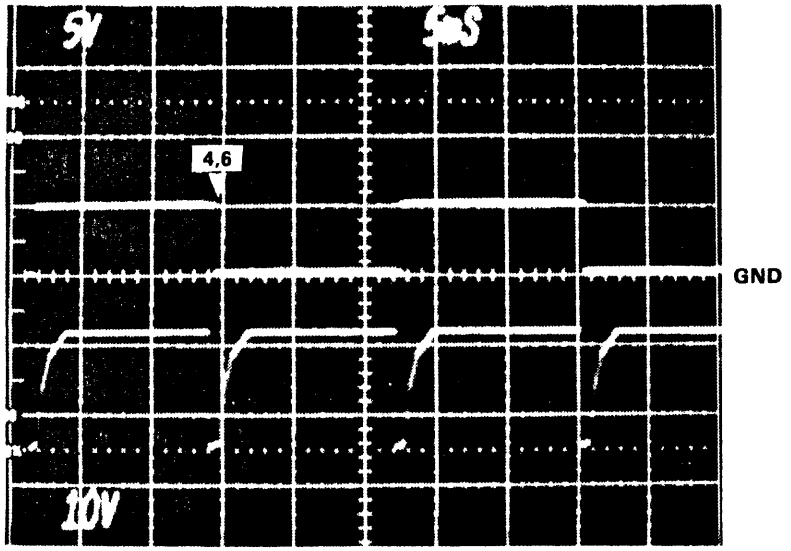
SHEET 1/1


5V
5mS
OE
TWP
VPP
GND
GND
10V

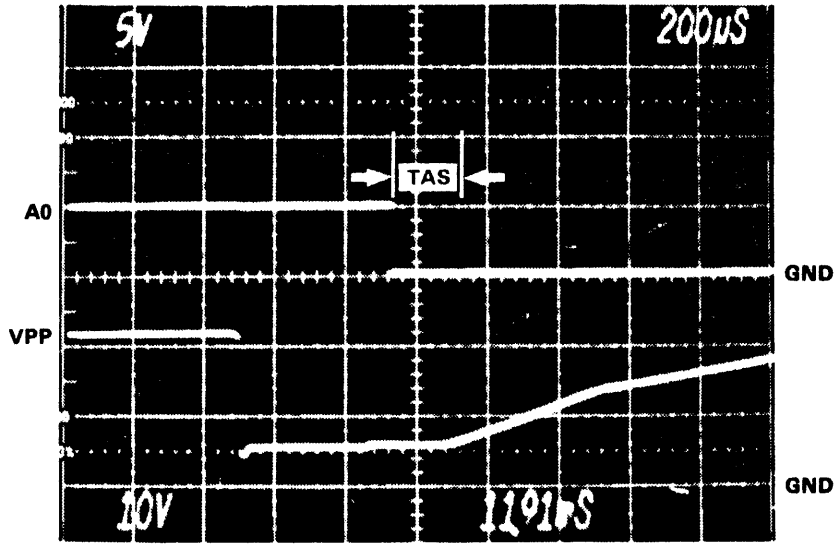
1


5V
5mS
CE
GND
VPP
GND
10V

2


5V
5mS
4,6
A0
GND
VPP
10V

3


5V
200uS
TAS
A0
GND
VPP
GND
10V
1191uS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
BYTE ERASE					
VPP	20.0	21.0	22.0	V	
TWP	9	10	15	ms	
TAS	150			ns	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

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10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			5/17/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 37,38, BYTE ERASE

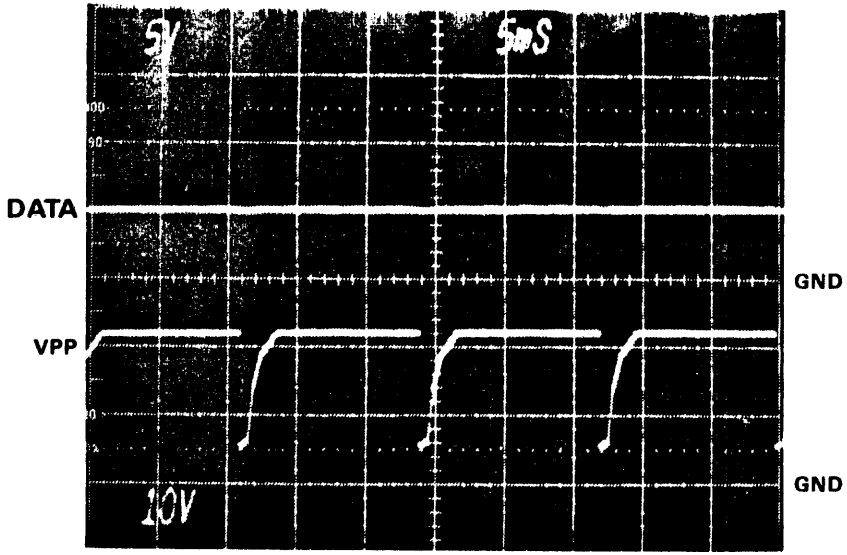
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

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10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 37, 38,
BYTE ERASE

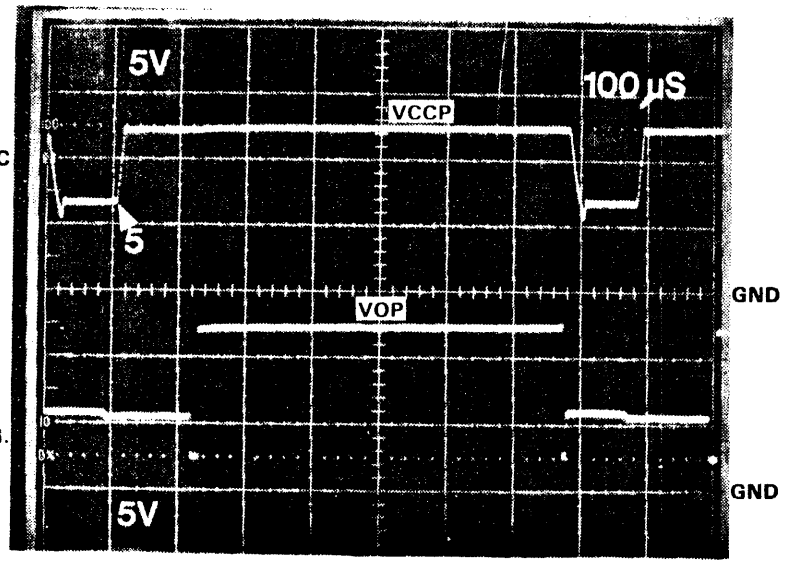
DRAWN BY:

CHECKED BY:

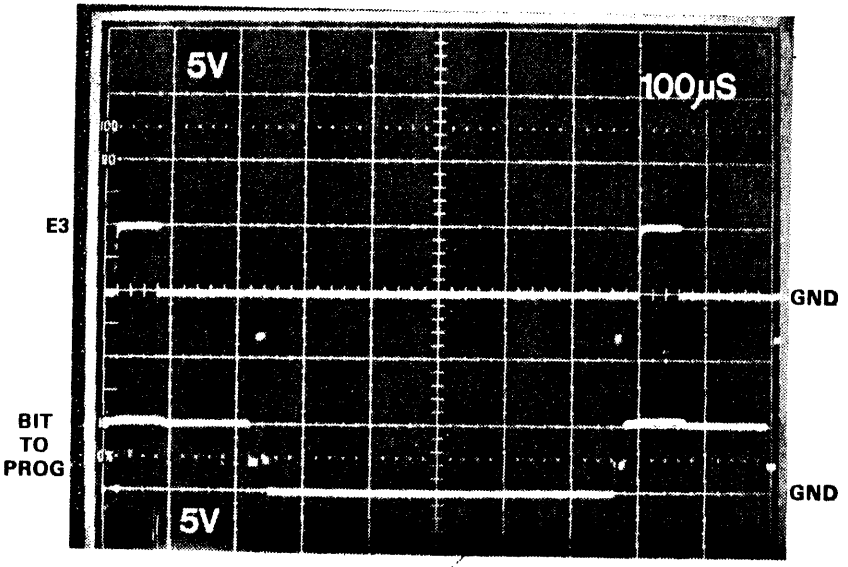
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

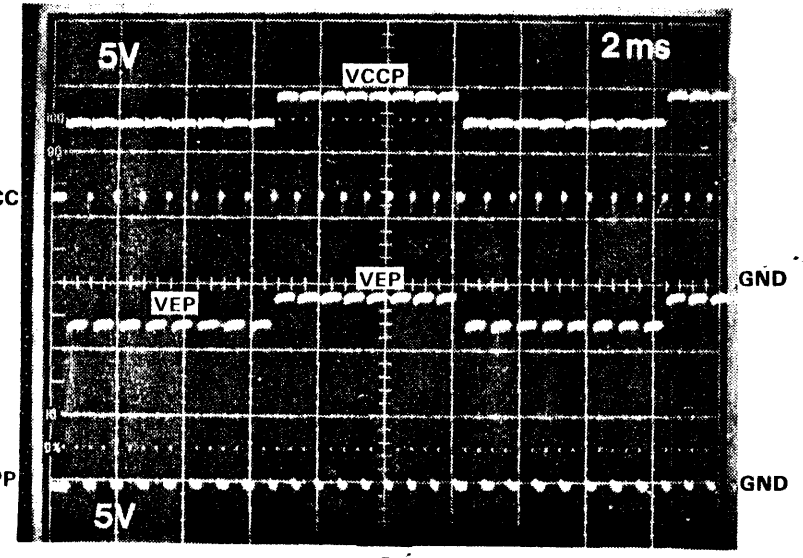
SHEET 2/2


5V
100 µS
VCCP
VCC
5
GND
VOP
BIT
NO
PROG.
GND
5V

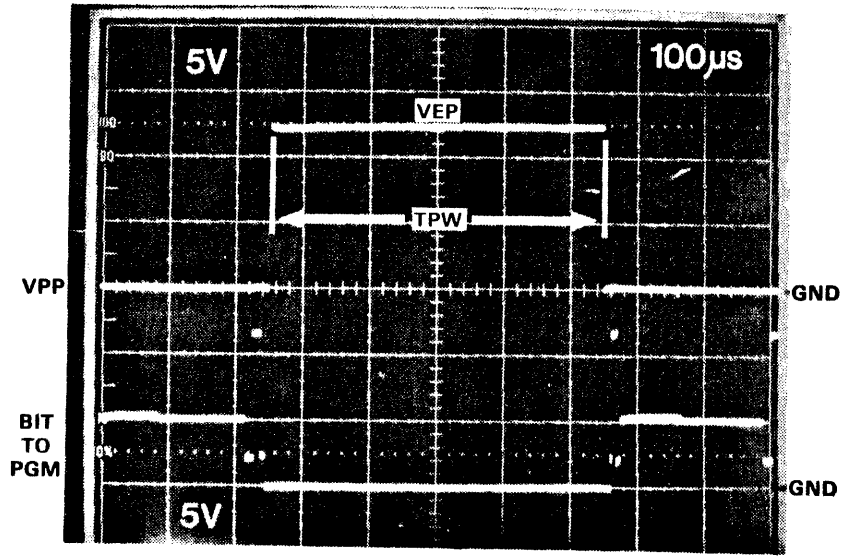
1


5V
100µS
E3
GND
BIT
TO
PROG
GND
5V

3


5V
2 ms
VCCP
VCC
VEP
VEP
GND
VPP
GND
5V

2


5V
100µs
VEP
TPW
VPP
GND
BIT
TO
PGM
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *To observe this level, adjust time base.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	11.5		12.5	V	PULSES 1-8
	13.5		14.5	V	PULSES 9-16
VEP	11.5		12.5	V	PULSES 1-8
	13.5		14.5	V	PULSES 9-16
VOP	11.5		12.5	V	PULSES 1-8
	13.5[6]		14.5	V	PULSES 9-16
TPW	450		550	usec	
TR	1			usec	
REJECT		16			PULSES
OVERPRO-GRAM		2			PULSES

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		BWR	9/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 39, 40

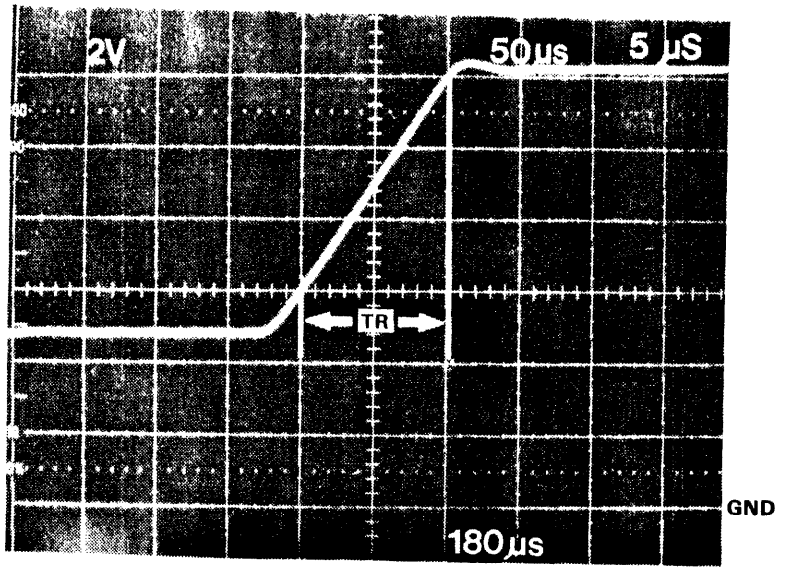
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 39, 40

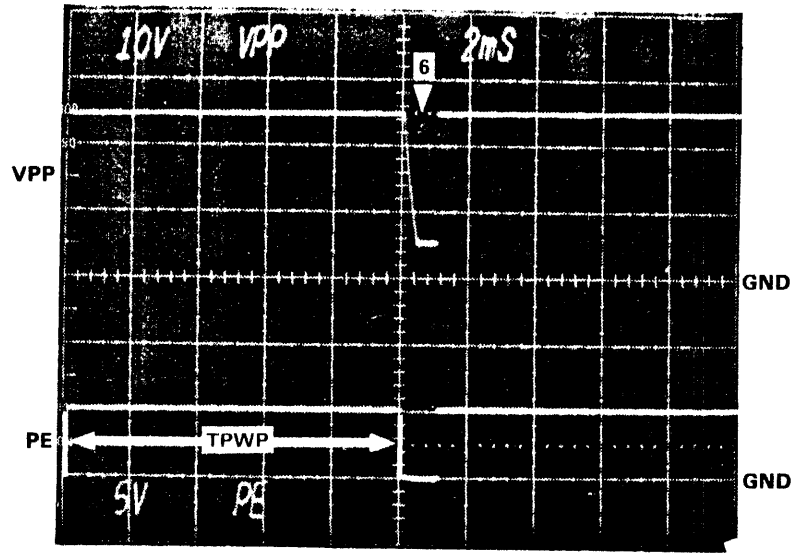
DRAWN BY:

CHECKED BY:

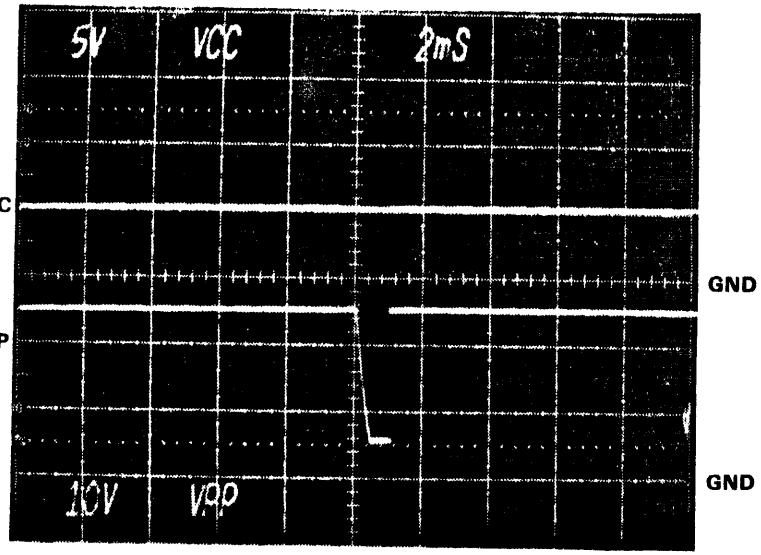
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

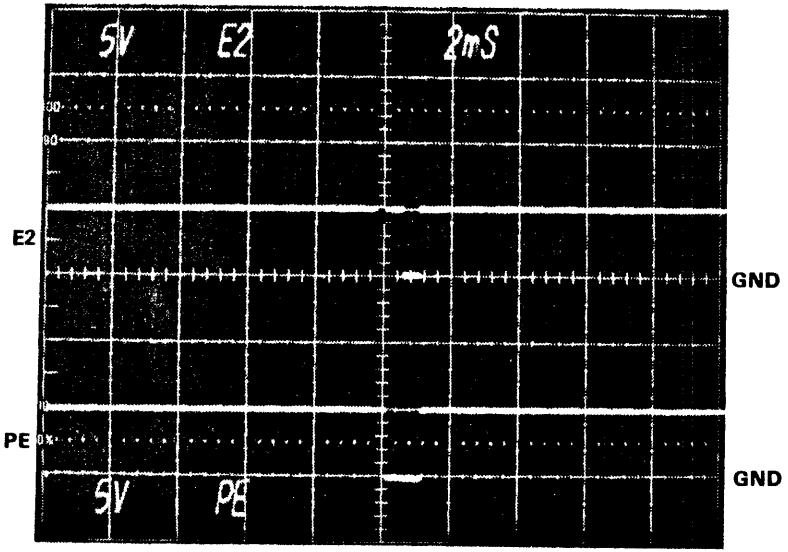
SHEET 2/2


10V VPP 2mS
6
VPP
GND
PE
TPWP
GND
5V PE

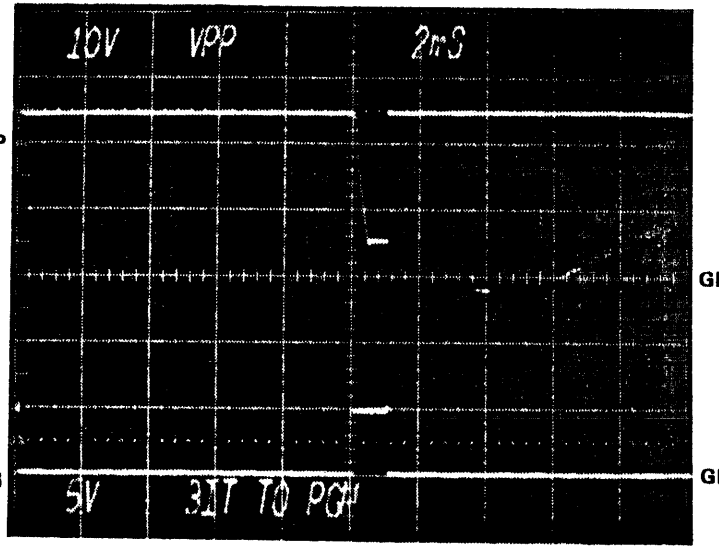
1


5V VCC 2mS
VCC
GND
VPP
GND
10V VPP

3


5V E2 2mS
E2
GND
PE
GND
5V PE

2


10V VPP 2mS
VPP
GND
BIT TO PROG
GND
5V BIT TO PGM

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact or a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no- bit-to-program, use O_3 for a 4-bit PROM Or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.50	5.00	5.50	V	
VPP	24.0	25.0	26.0	V	
TPWP	9.9	10	10.1	msec	PROGRAM PW
TPWE	—	100	—	msec	ERASE PW
REJECT	—	0	—	PULSES	
OVERPROGRAM	—	0	—	PULSES	

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10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		JM	9/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODE 43, 44

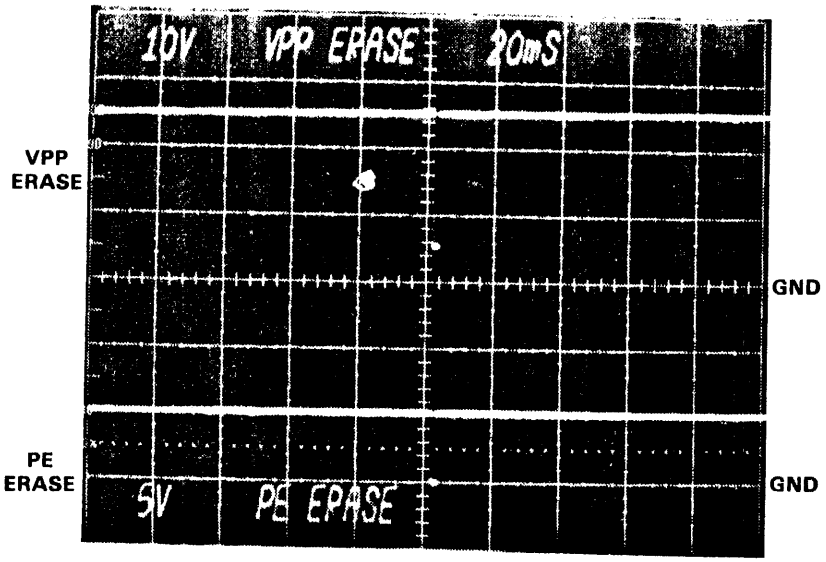
DRAWN BY:

CHECKED BY:

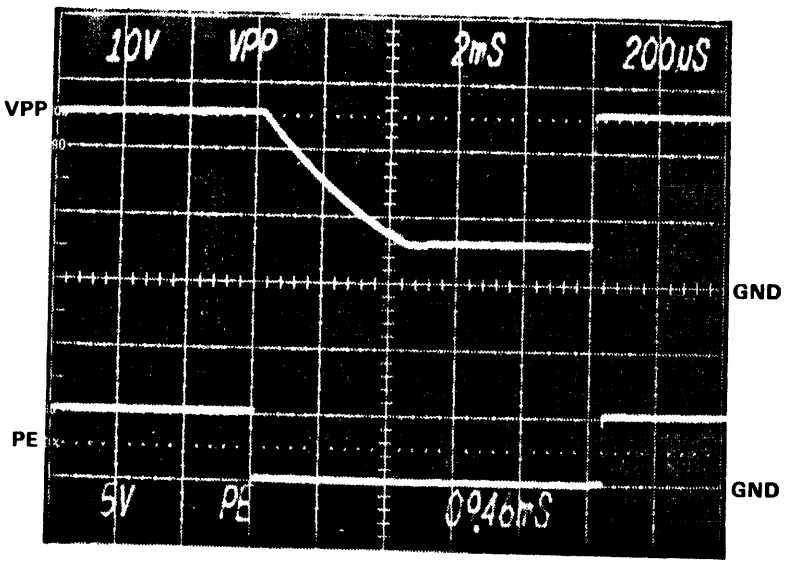
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2


10V
VPP ERASE
20mS
VPP
ERASE
GND
PE
ERASE
GND
5V
PE ERASE

5


10V
VPP
2mS
200uS
VPP
GND
PE
GND
5V
PE
0.46mS

6

4-111
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 43, 44

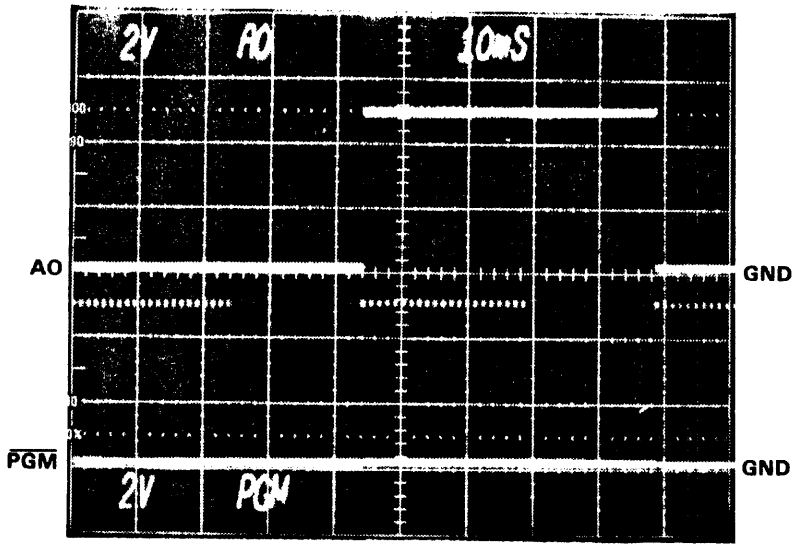
DRAWN BY:

CHECKED BY:

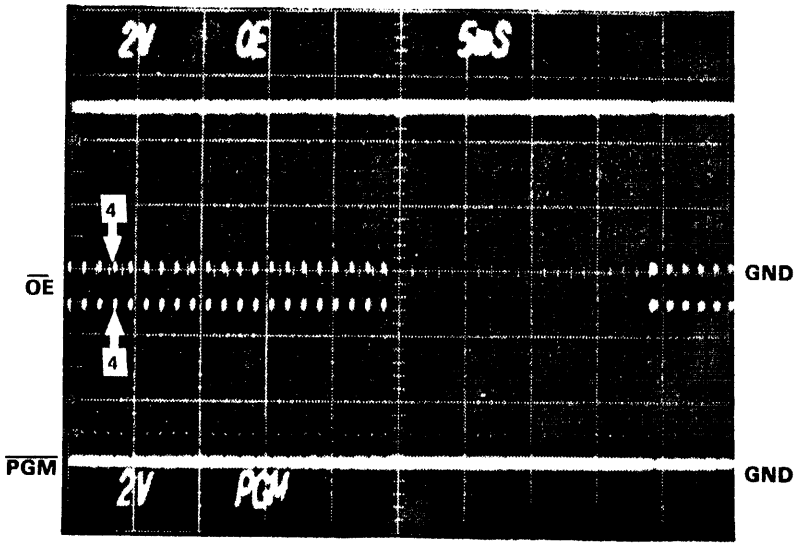
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

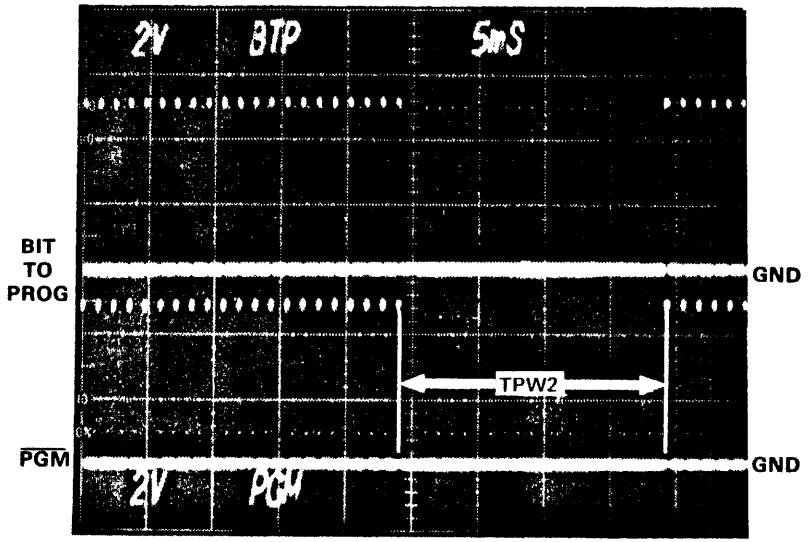
SHEET 2/2


2V
AO
10mS
AO
GND
PGM
GND
2V
PGM

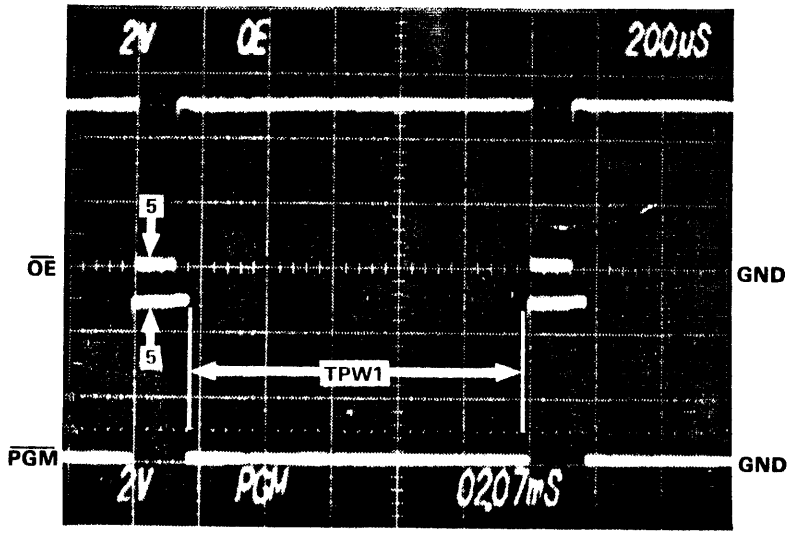
1


2V
OE
5mS
4
OE
4
GND
PGM
GND
2V
PGM

3


2V
BTP
5mS
BIT
TO
PROG
GND
TPW2
PGM
GND
2V
PGM

2


2V
OE
200uS
5
OE
5
GND
TPW1
PGM
GND
2V
PGM
0207mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	Not shown
	VPP	20.5	21.0	21.5	V	Not shown
	TPW1	.95	1.0	1.05	ms	
	Reject		20		Pulses	
	Overprogram		1		Pulses	
	TPW2	.95	1X	21	ms	x = number of pulses applied to that byte prior to it verifying

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XX	11/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 45, 46

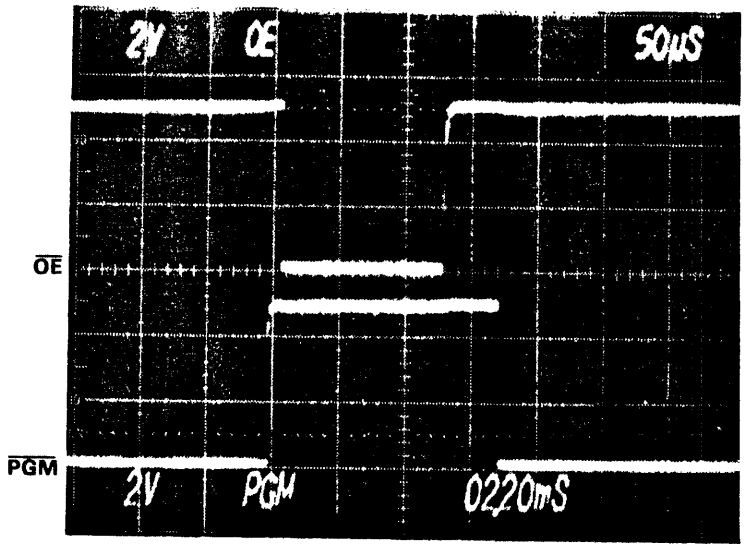
DRAWN BY: EE

CHECKED BY: XX

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

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10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 45, 46

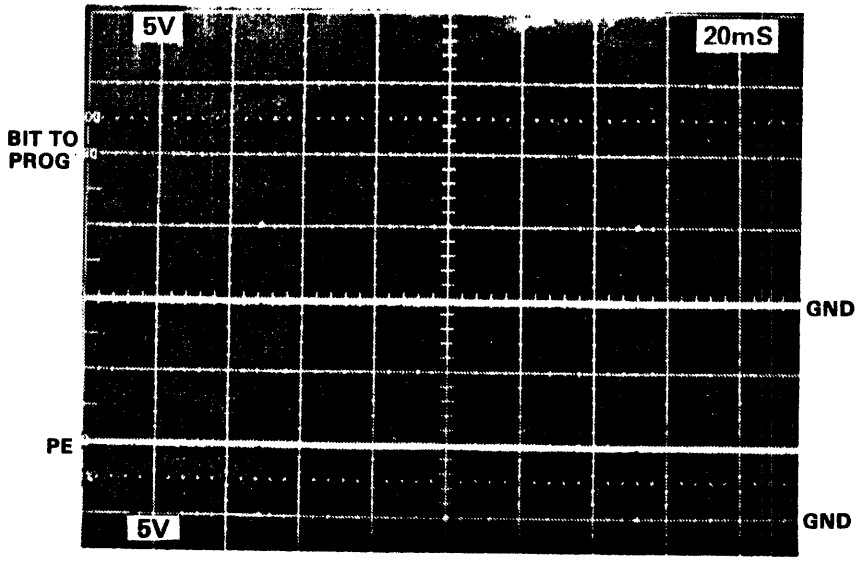
DRAWN BY:

CHECKED BY: XH

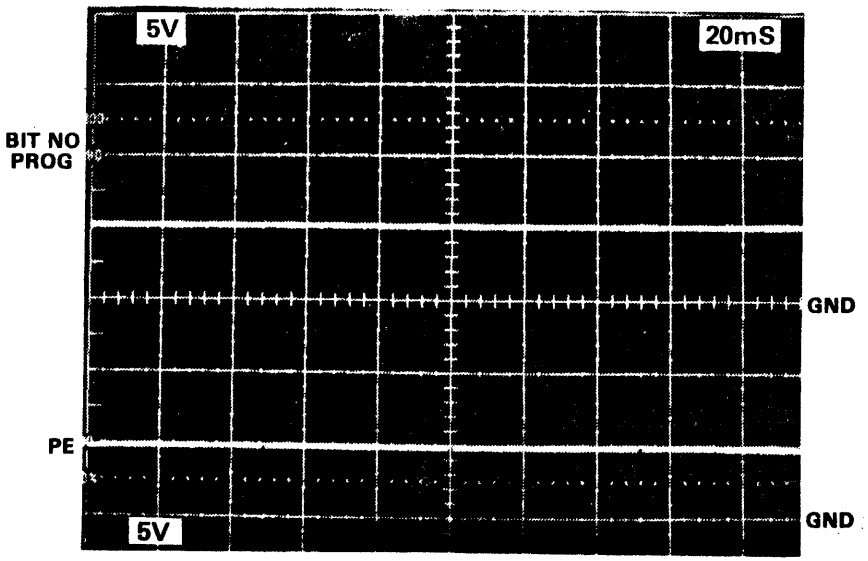
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

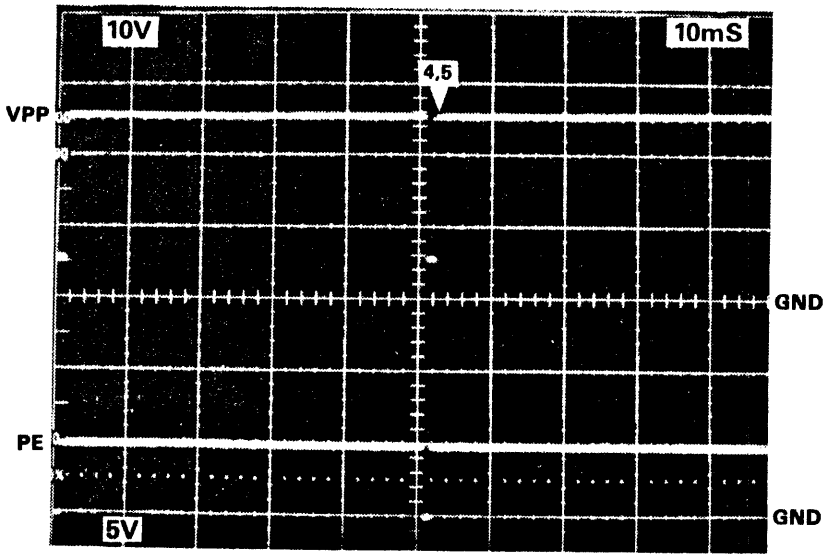
SHEET 2/2


5V
20mS
BIT TO PROG
GND
PE
5V
GND

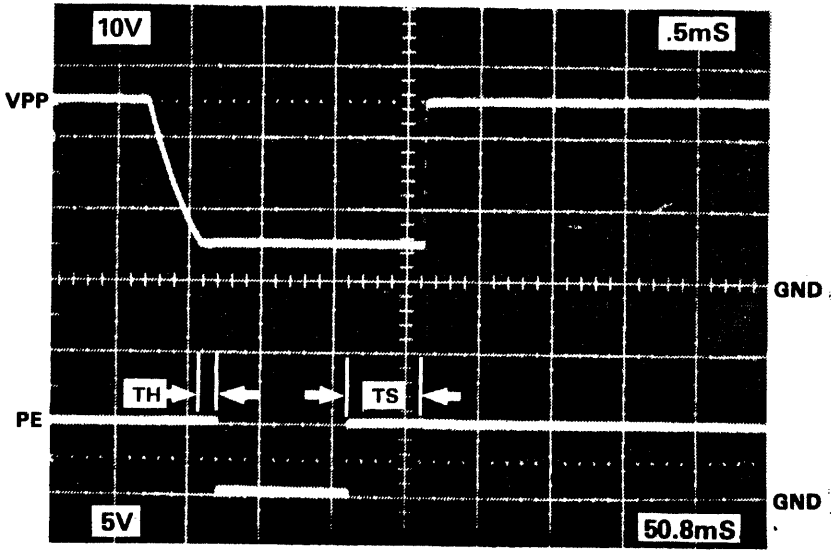
1


5V
20mS
BIT NO PROG
GND
PE
5V
GND

2


10V
10mS
4.5
VPP
GND
PE
5V
GND

3


10V
.5mS
VPP
GND
TH
TS
PE
5V
GND
50.8mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VPP	24.0	25.0	26.0	V	
VCC	4.75	5.0	5.25	V	
TPR	.01	2.0		µs	
TH	2			µs	
TS	2			µs	
REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		BS	5/17/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM
FAMILY CODES 47, 48

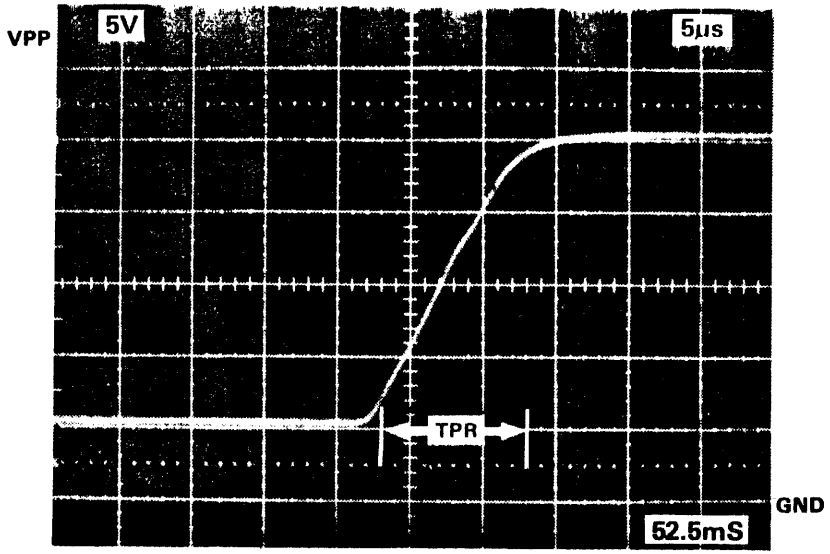
DRAWN BY:

CHECKED BY:

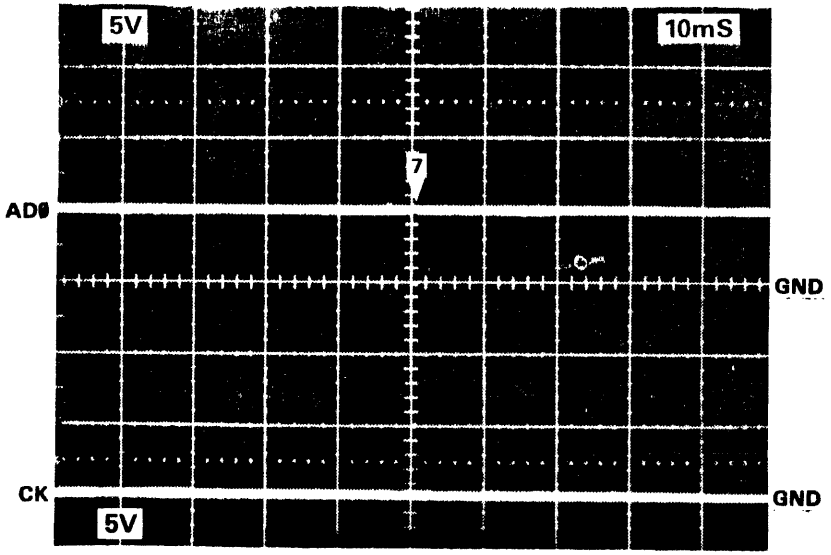
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

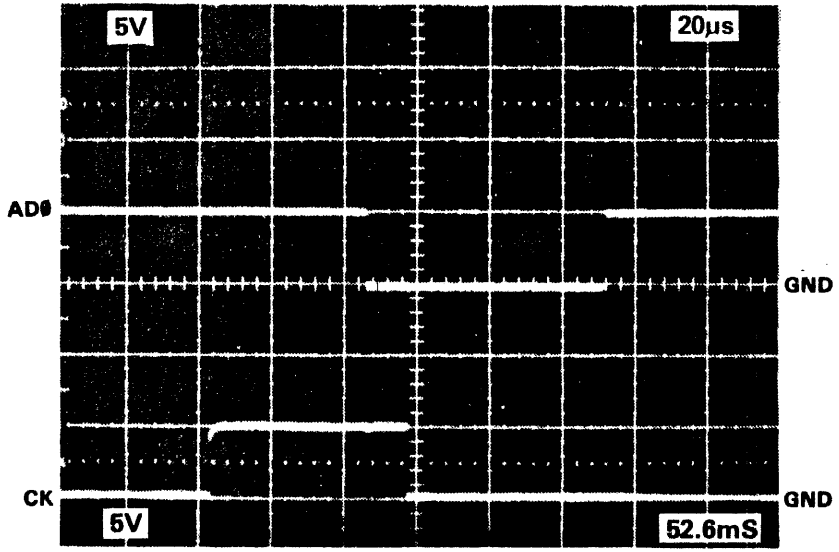
SHEET 1/2


VPP
5V
5µs
TPR
GND
52.5mS

5


5V
10mS
7
AD0
GND
CK
GND
5V

6


5V
20µs
AD0
GND
CK
GND
5V
52.6mS

7

4-119
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 47, 48

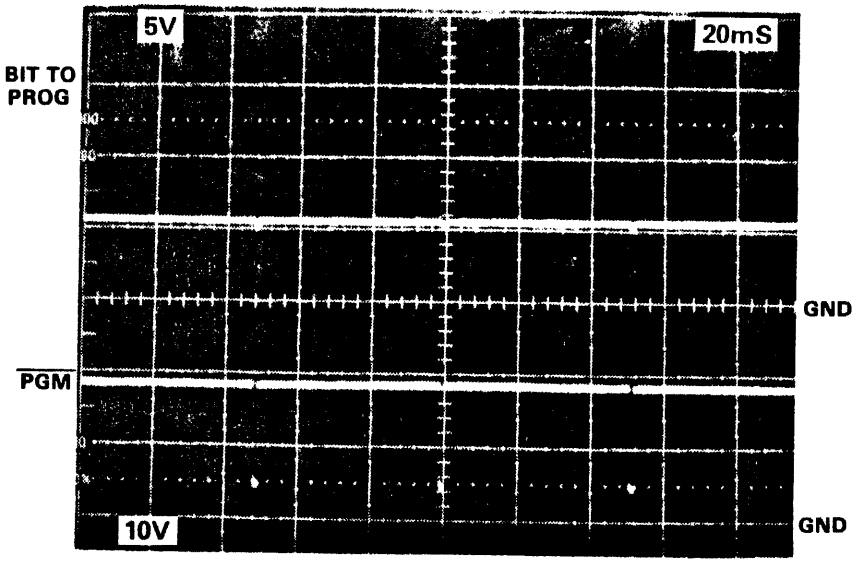
DRAWN BY:

CHECKED BY:

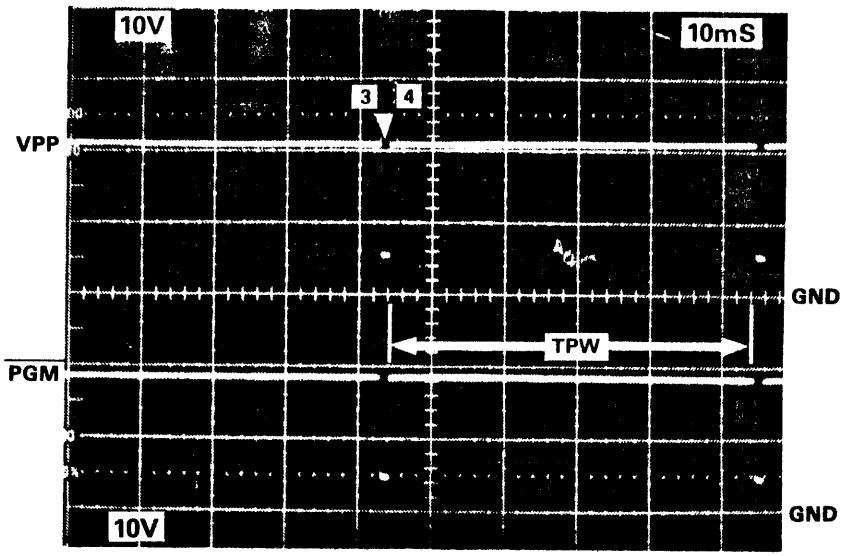
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54103	33-950-0099

SCALE

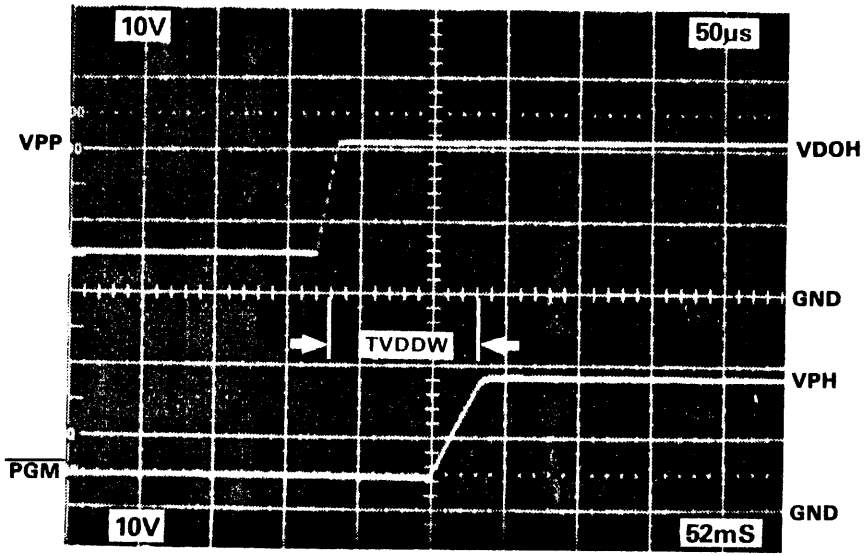
SHEET 2/2


5V
20mS
BIT TO PROG
GND
PGM
10V
GND

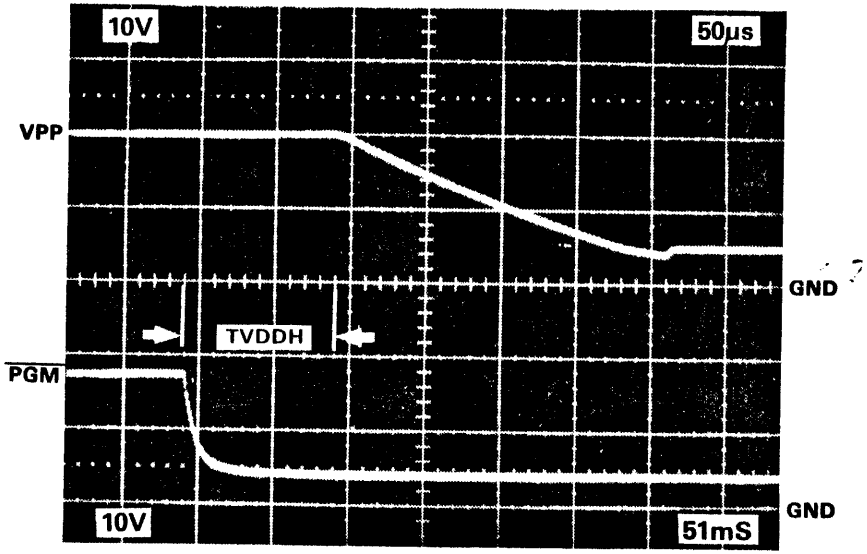
1


10V
10mS
3
4
VPP
GND
TPW
PGM
10V
GND

2


10V
50µs
VPP
VDOH
GND
TVDDW
VPH
PGM
10V
52mS
GND

3


10V
50µs
VPP
GND
TVDDH
PGM
10V
51mS
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VDOH	20.5	21.0	21.5	V	
VPH	17.5	18.0	18.5	V	
TPW	50		60	ms	
TWW	20			µs	
TVDDW	20			µs	
TVDDH	0				
TWT	20			µs	
.REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		TJ	5/17/83

DATA I/O ISSAQUAH, WA

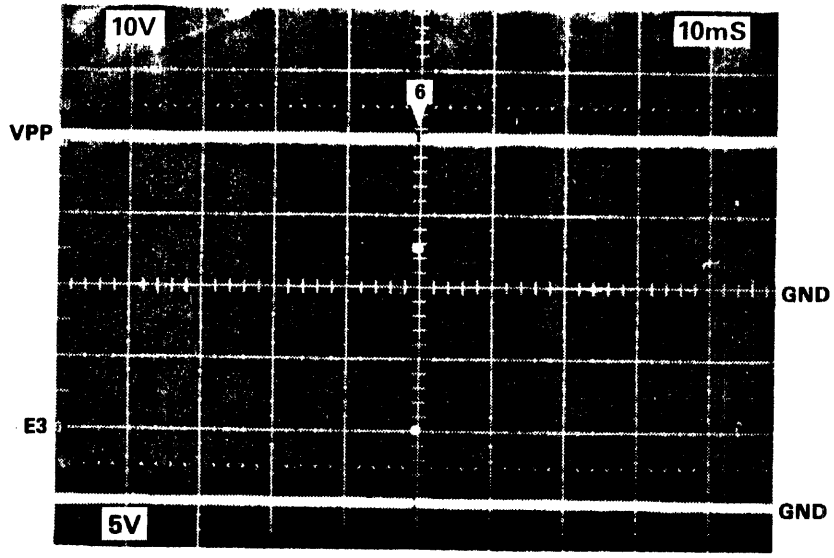
TITLE
TIMING DIAGRAM
FAMILY CODES 49, 50

DRAWN BY: JP

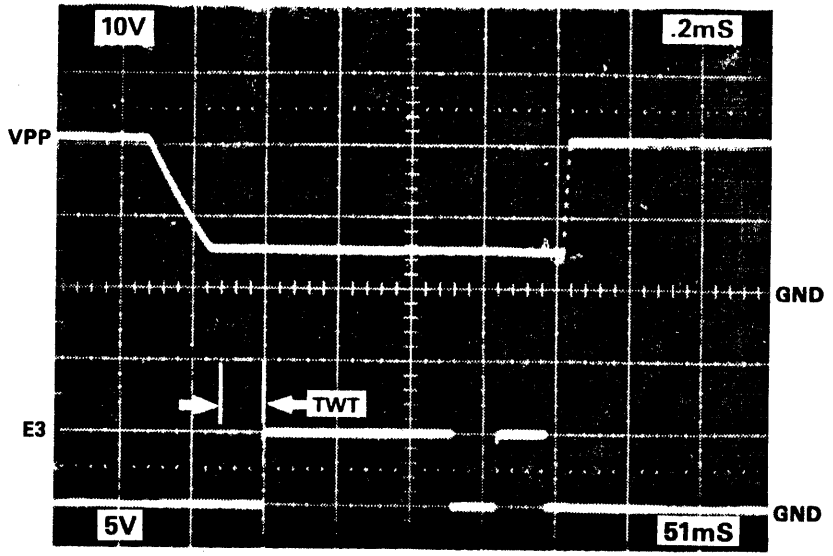
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

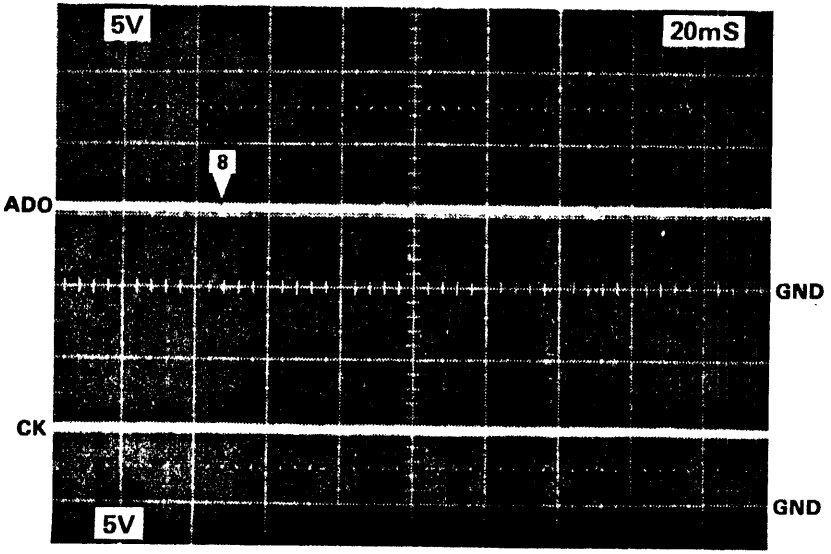
SCALE | SHEET 1/2


10V
10mS
6
VPP
GND
E3
GND
5V

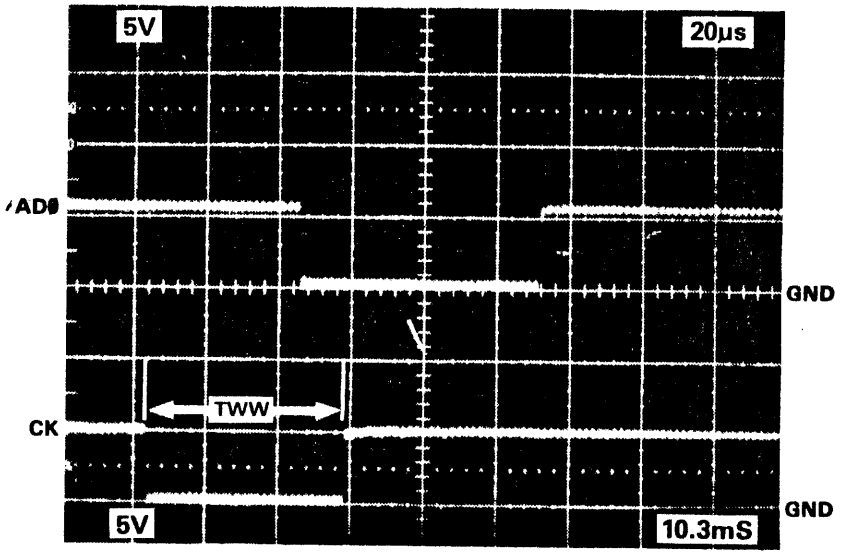
5


10V
.2mS
VPP
GND
TWT
E3
5V
51mS
GND

6


5V
20mS
8
ADO
GND
CK
5V
GND

7


5V
20µs
ADO
GND
TWW
CK
5V
10.3mS
GND

8

4-123
10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 49, 50

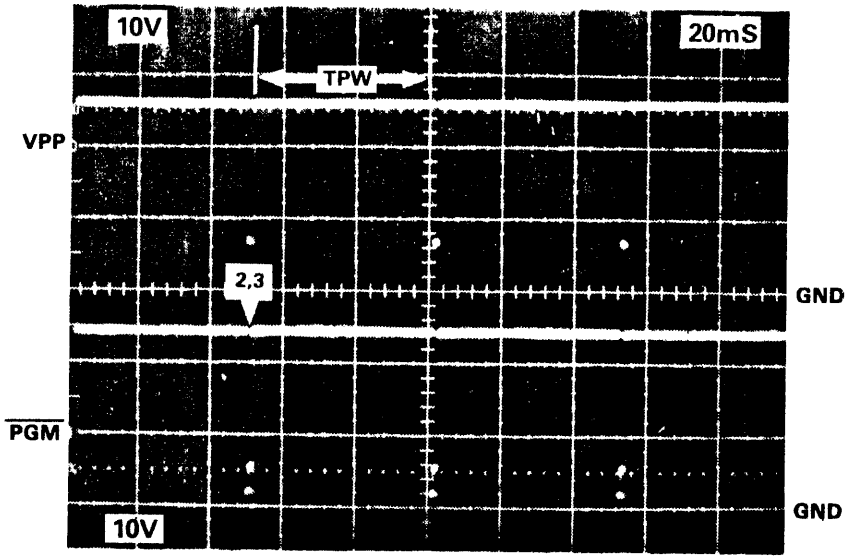
DRAWN BY:

CHECKED BY:

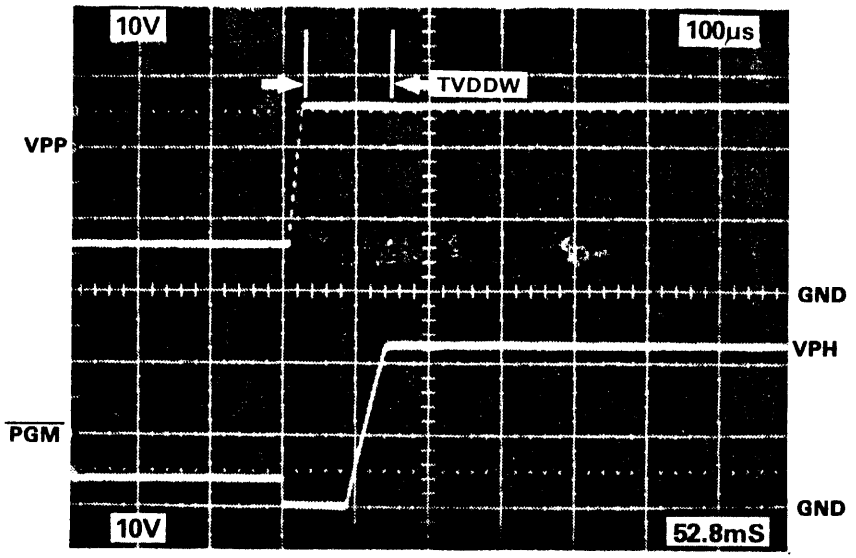
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

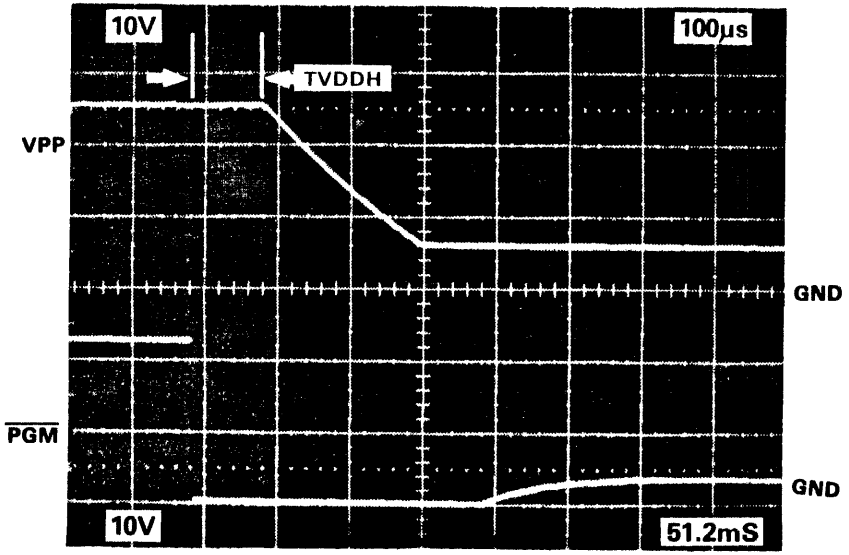
SHEET 2/2


10V
20mS
TPW
VPP
2,3
GND
PGM
GND
10V

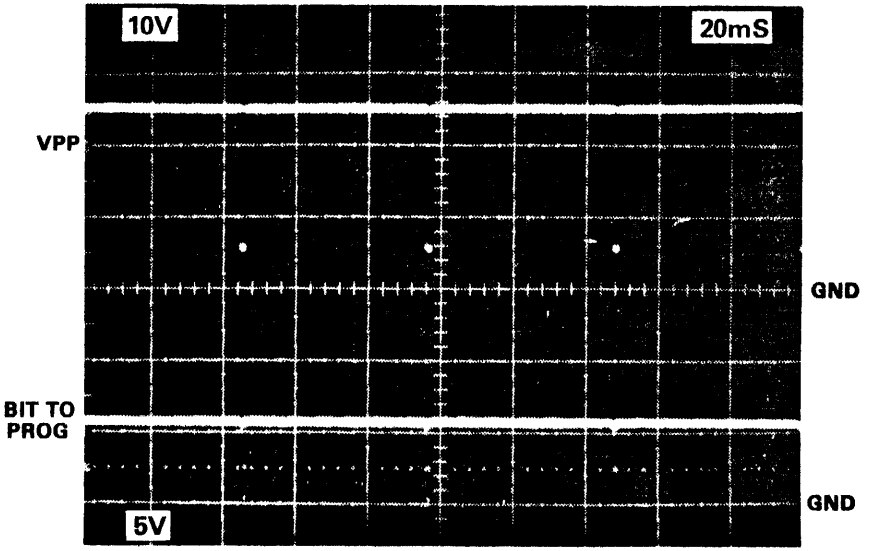
1


10V
100µs
TVDDW
VPP
GND
VPH
PGM
GND
10V
52.8mS

2


10V
100µs
TVDDH
VPP
GND
PGM
GND
10V
51.2mS

3


10V
20mS
VPP
GND
BIT TO
PROG
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▌ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *This family has a multiplexed address bus. The A0 line is shown in diagram 8 as CK goes high.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VPP	24.0		26.0	V	
TPW	50.0		60.0	ms	
TVDDW	20			µs	
VPH	21.5		24.5	V	
TVDDH	0				
TWW	20			µs	
REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		RS	5/10/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 51, 52

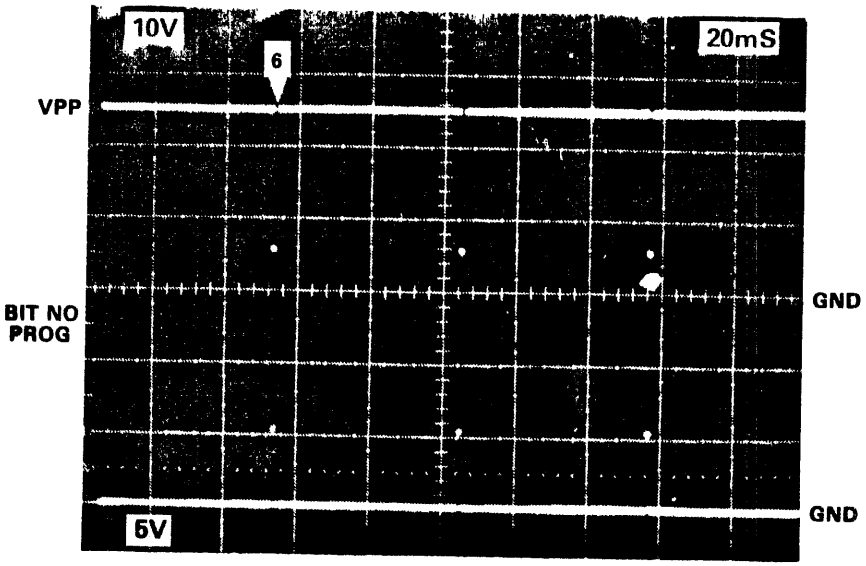
DRAWN BY:

CHECKED BY:

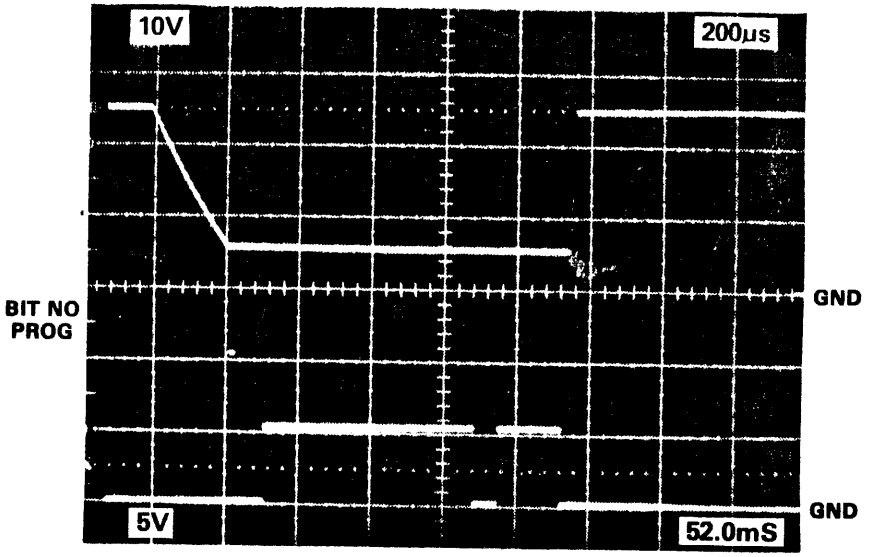
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

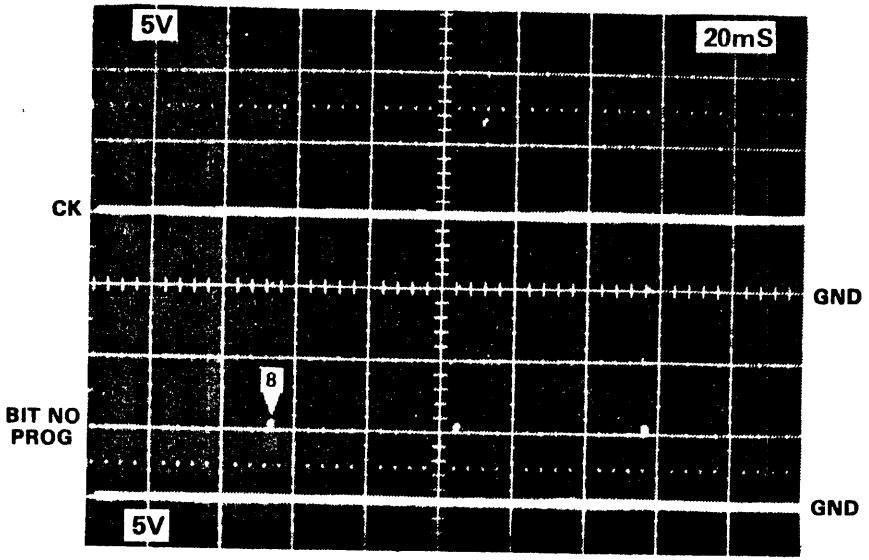
SHEET 1/2


10V
20mS
6
VPP
BIT NO PROG
GND
GND
5V

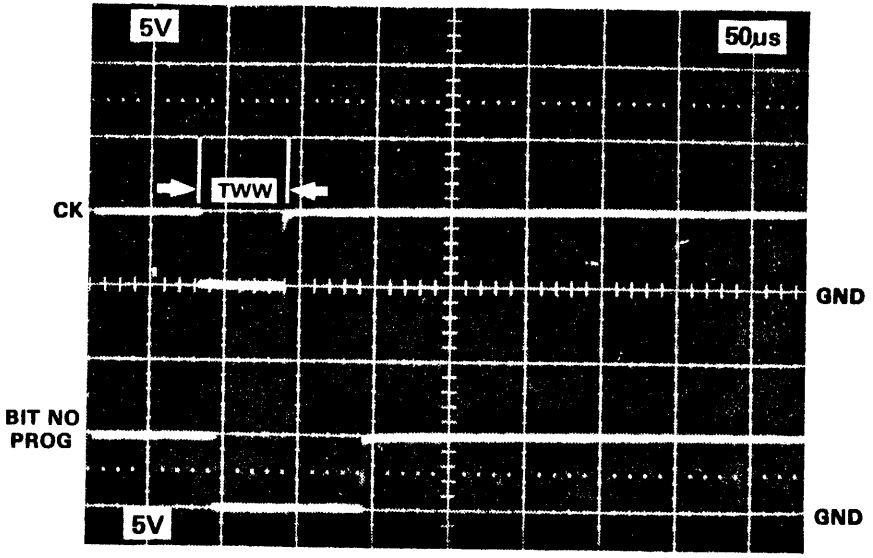
5


10V
200µs
BIT NO PROG
GND
5V
52.0mS
GND

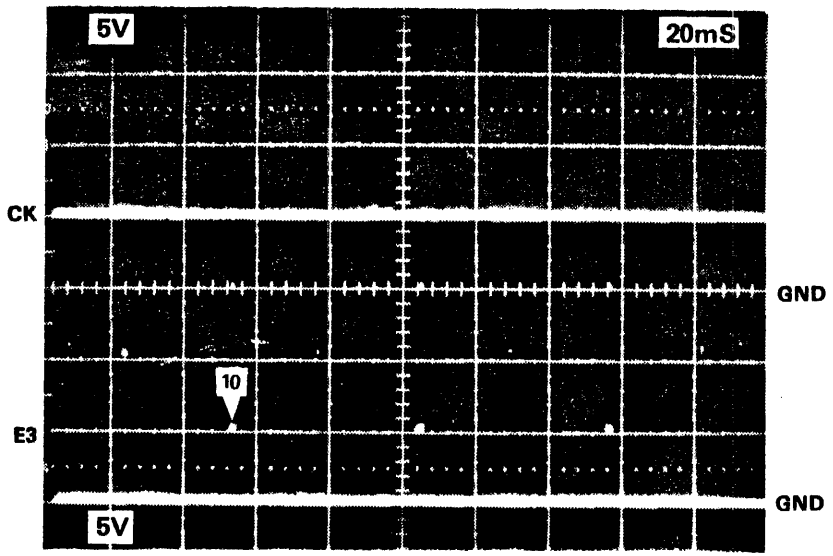
6


5V
20mS
CK
GND
8
BIT NO PROG
5V
GND

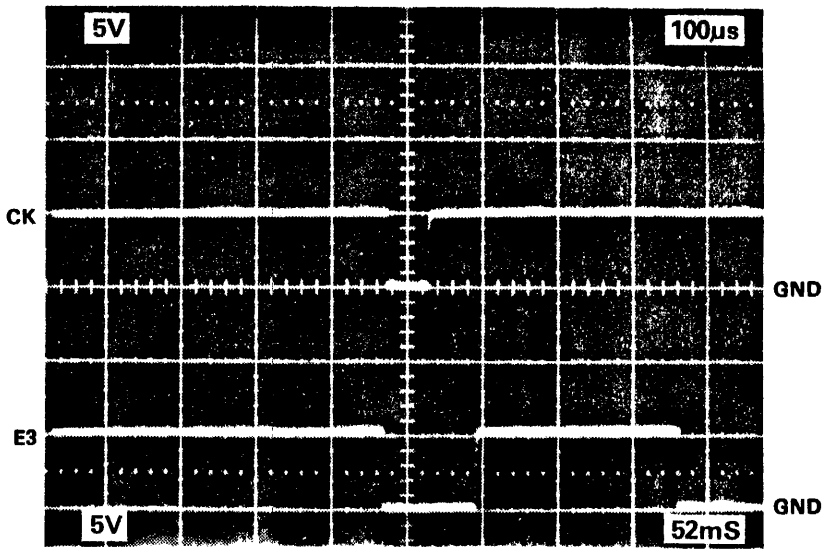
7


5V
50µs
TWW
CK
GND
BIT NO PROG
5V
GND

8



9



10

4-127
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 51, 52

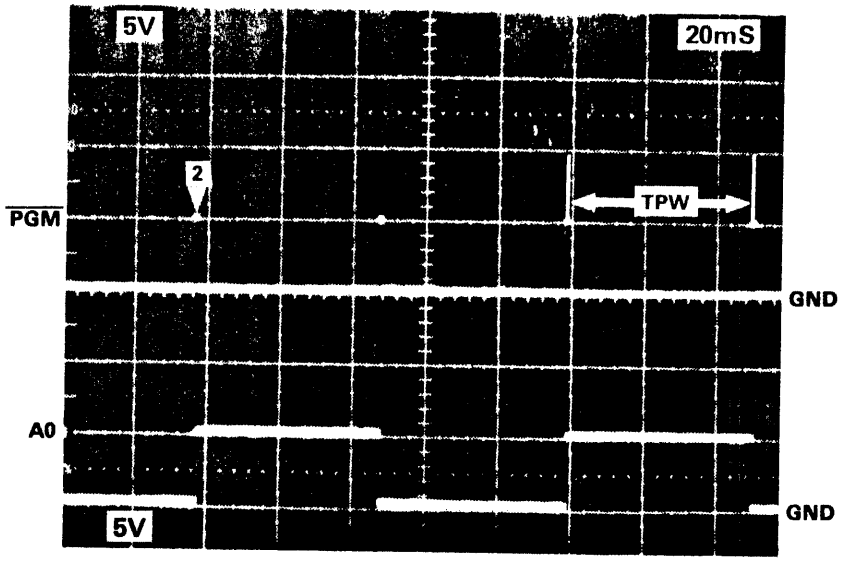
DRAWN BY:

CHECKED BY:

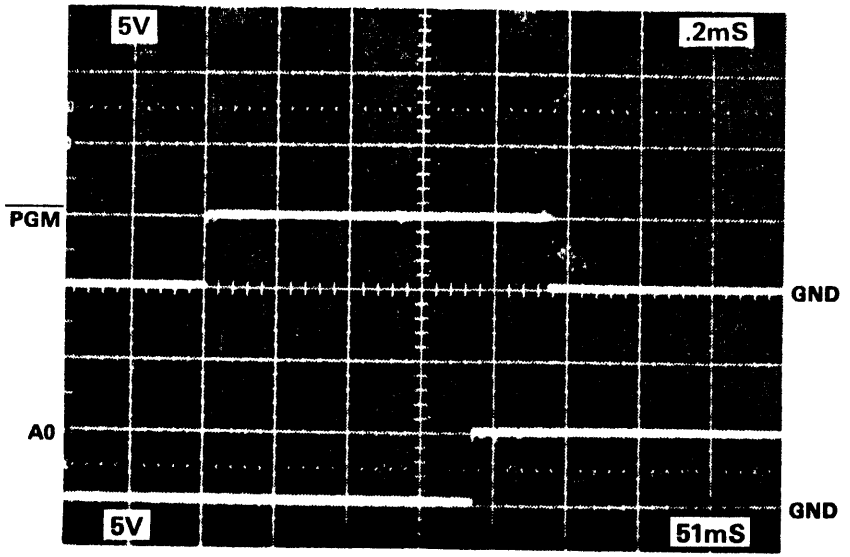
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

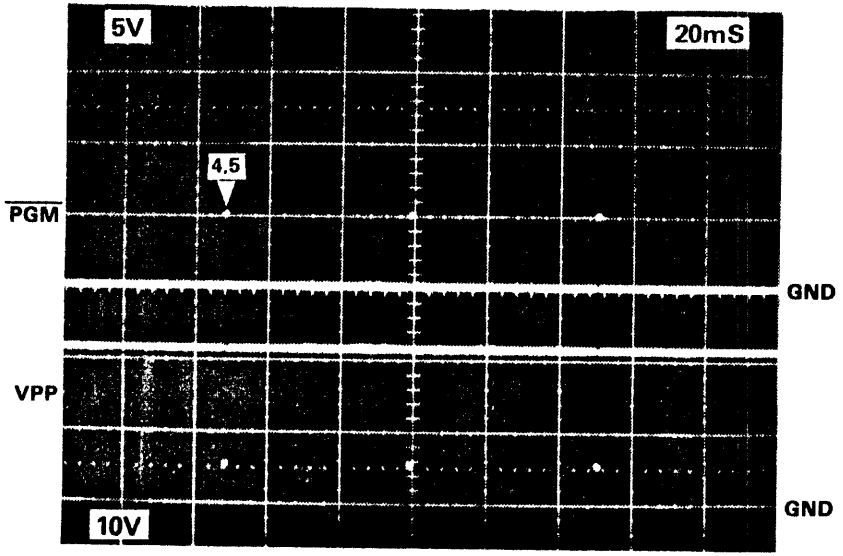
SHEET 2/2


5V
20mS
2
TPW
PGM
GND
A0
GND
5V

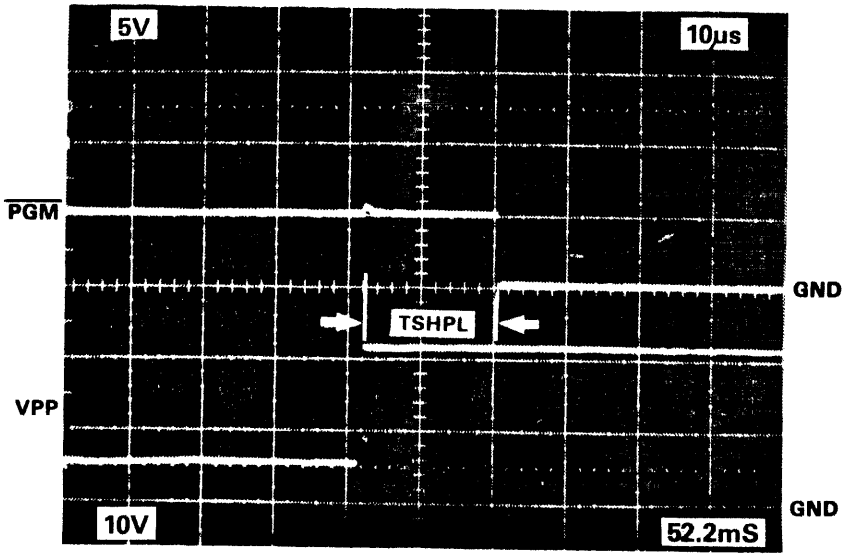
1


5V
.2mS
PGM
GND
A0
GND
5V
51mS

2


5V
20mS
4.5
PGM
GND
VPP
GND
10V

3


5V
10µs
PGM
GND
TSHPL
VPP
GND
10V
52.2mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the 0_4 contact for a 4-bit PROM or 0_3 for an 8-bit PROM. To observe a no-bit-to-program, use 0_3 for a 4-bit PROM or 0_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VPP	20.5	21.0	21.5	V	
VCC	4.75	5.0	5.25	V	
TSHPL	10			µs	
TPW	49	50	51	ms	
TPHSL	10			µs	
REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			5/17/85

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 53, 54

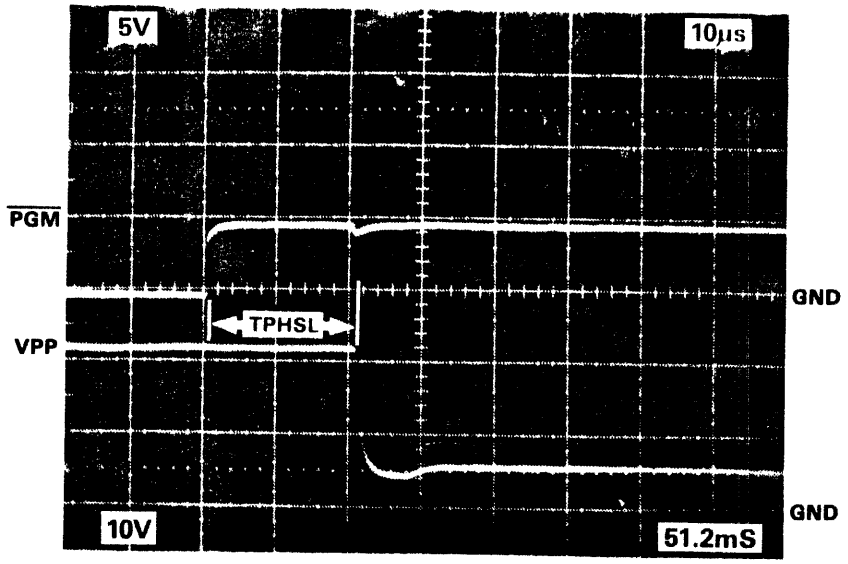
DRAWN BY:

CHECKED BY:

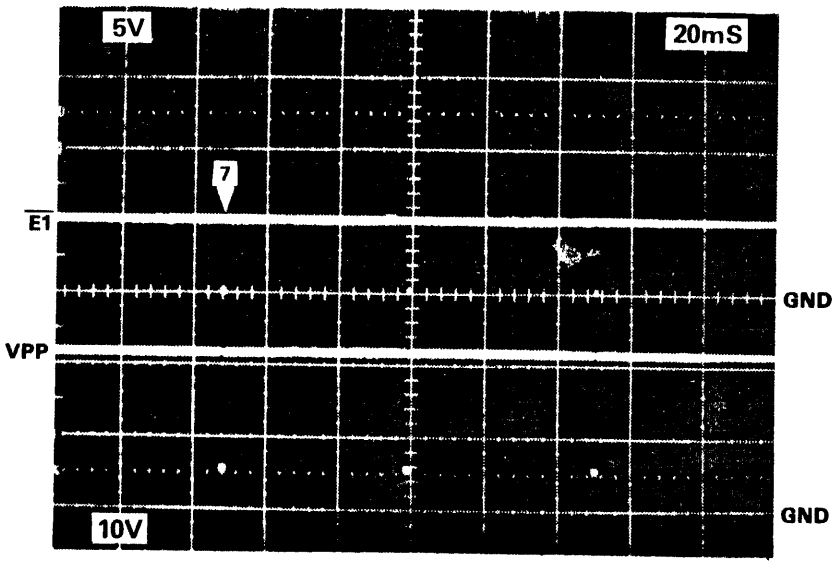
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

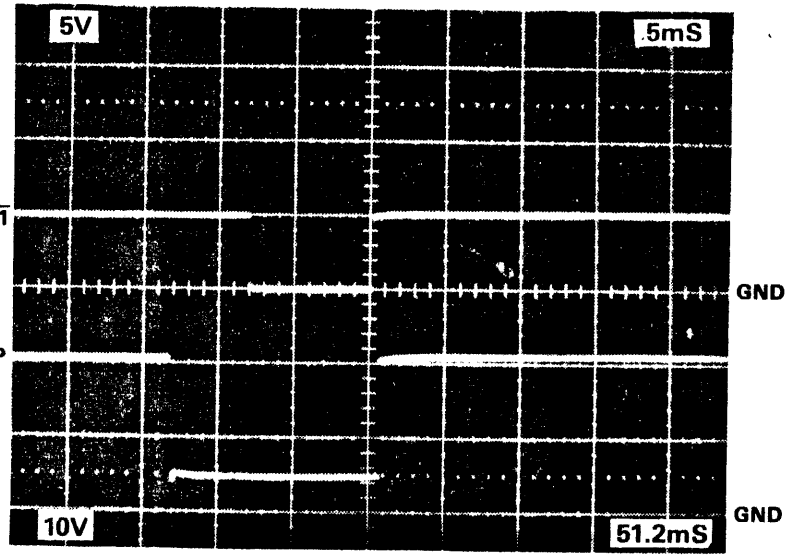
SHEET 1/2


5V
10µs
PGM
GND
VPP
TPHSL
GND
10V
51.2mS

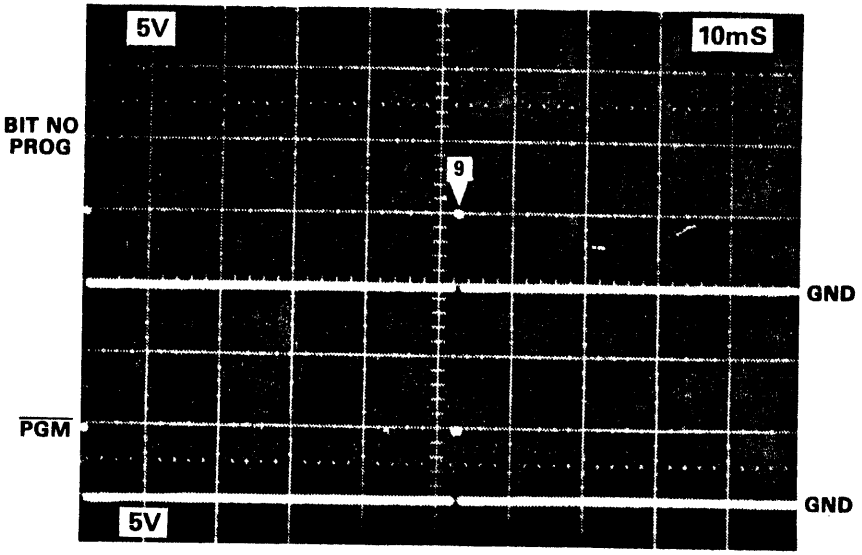
5


5V
20mS
7
E1
GND
VPP
10V
GND

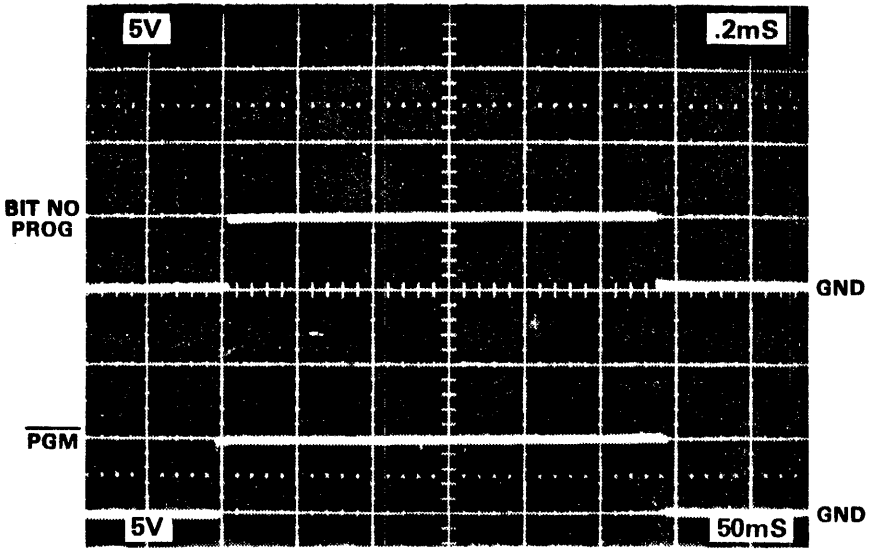
6


5V
5mS
E1
GND
VPP
10V
51.2mS
GND

7


5V
10mS
BIT NO
PROG
9
GND
PGM
5V
GND

8



9

4-131
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 53, 54

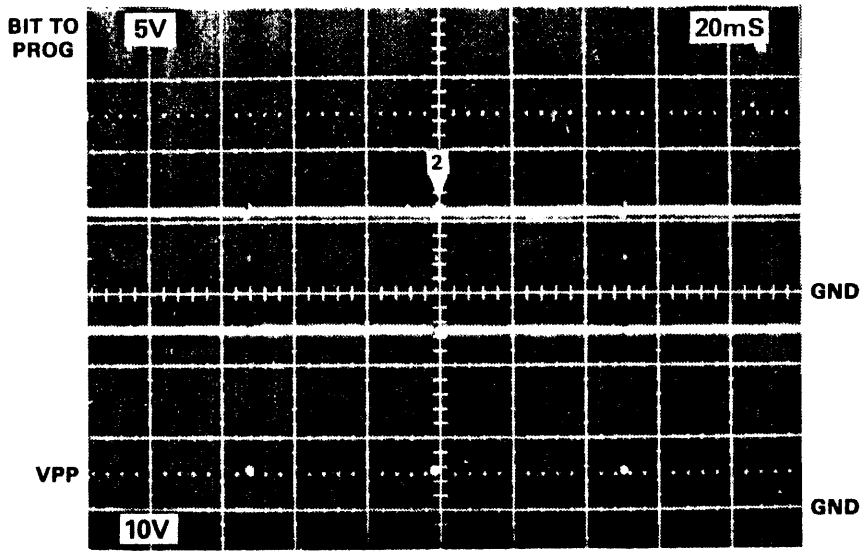
DRAWN BY:

CHECKED BY:

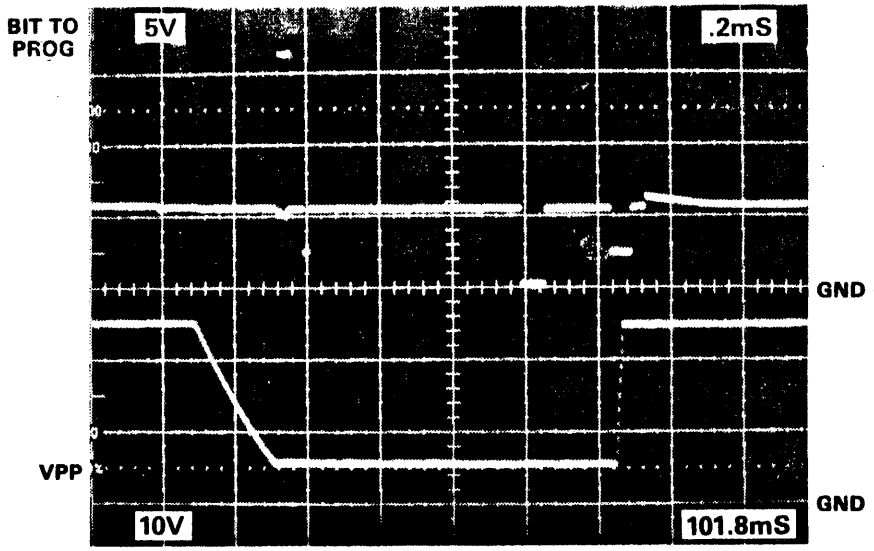
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

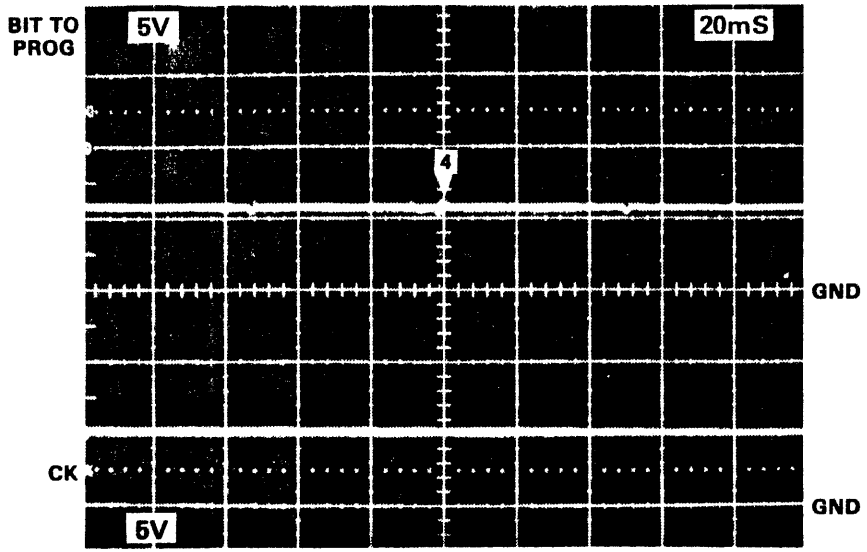
SHEET 2/2


BIT TO PROG
5V
20mS
2
GND
VPP
GND
10V

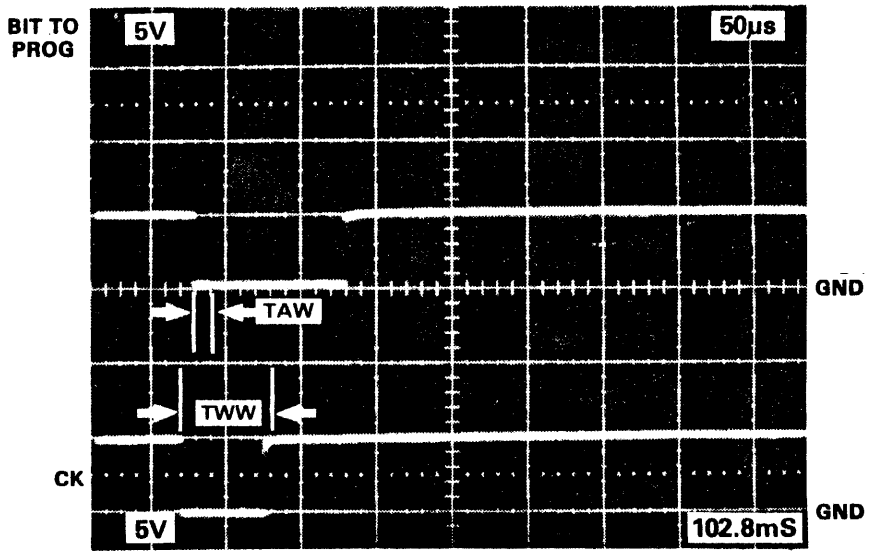
1


BIT TO PROG
5V
.2mS
GND
VPP
GND
10V
101.8mS

2


BIT TO PROG
5V
20mS
4
GND
CK
GND
5V

3


BIT TO PROG
5V
50µs
GND
TAW
TWW
CK
GND
5V
102.8mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VPP	24.0	25.0	26.0	V	
PROG	21.5	23.0	24.5	V	
TWW	20			µs	
TPW	50	55	60	ms	
TVDDW	20.0			µs	
TVDDH	0				
TWT	20			µs	
TAW	20			µs	
EA	21.5	23.0	24.5	V	
REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		TG	5/17/85

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 55, 56

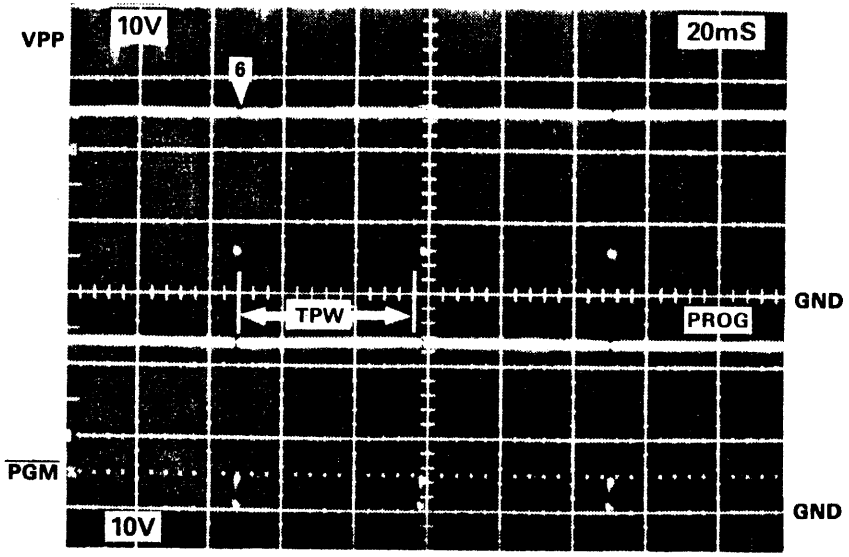
DRAWN BY:

CHECKED BY:

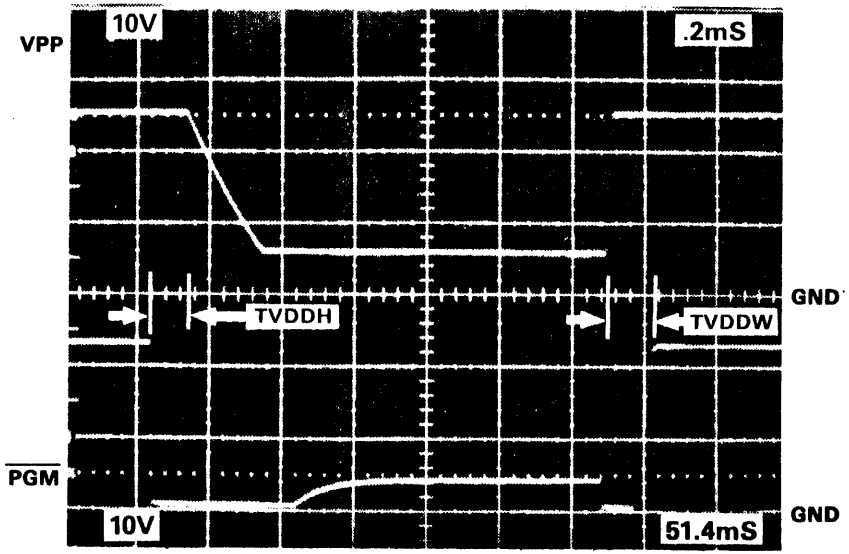
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

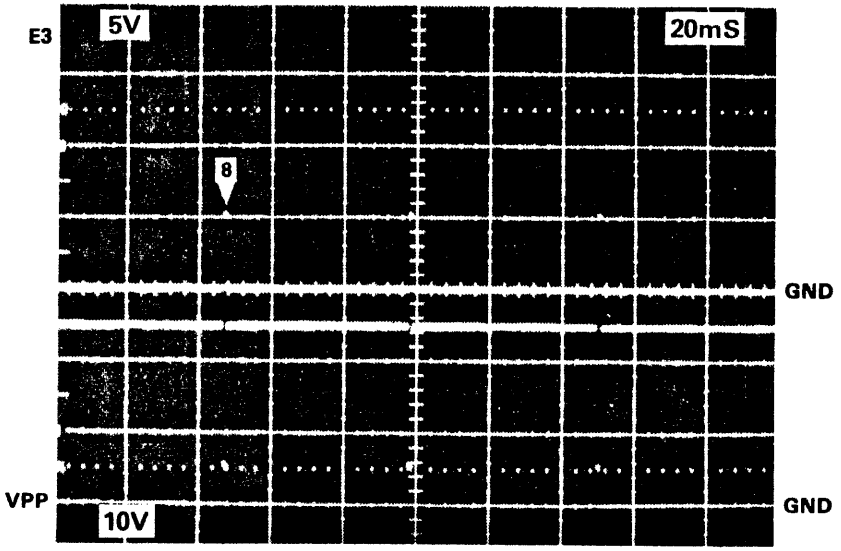
SHEET 1/2


VPP
10V
20mS
6
TPW
PROG
GND
PGM
GND
10V

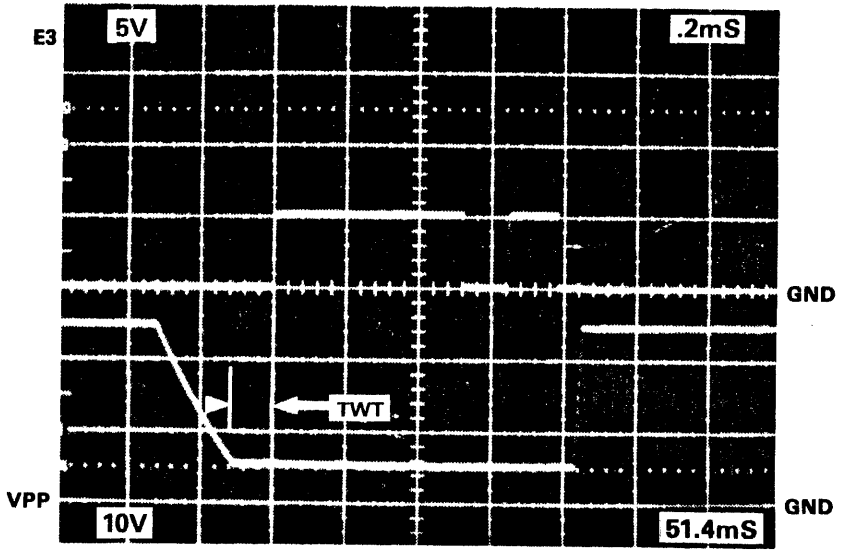
5


VPP
10V
.2mS
TVDDH
TVDDW
GND
PGM
GND
10V
51.4mS

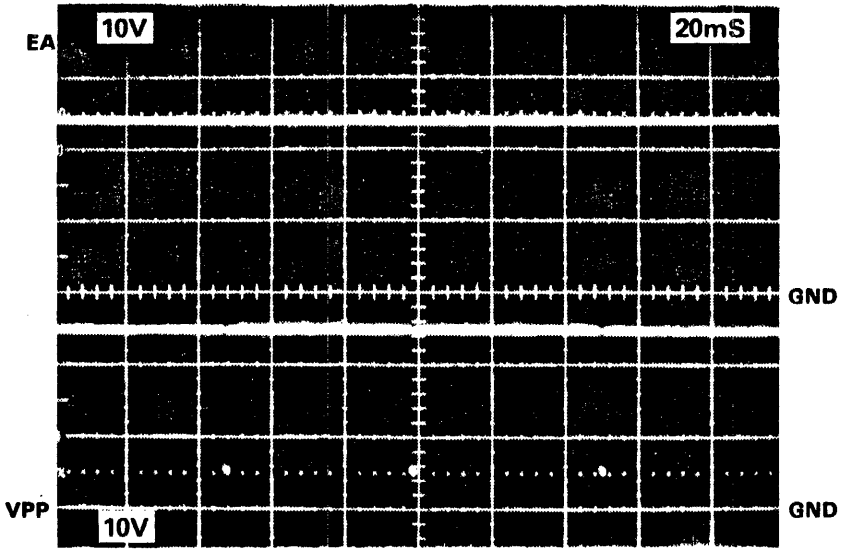
6


E3
5V
20mS
8
GND
VPP
10V
GND

7


E3
5V
.2mS
GND
TWT
VPP
10V
51.4mS
GND

8



9

4-135
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 55, 56

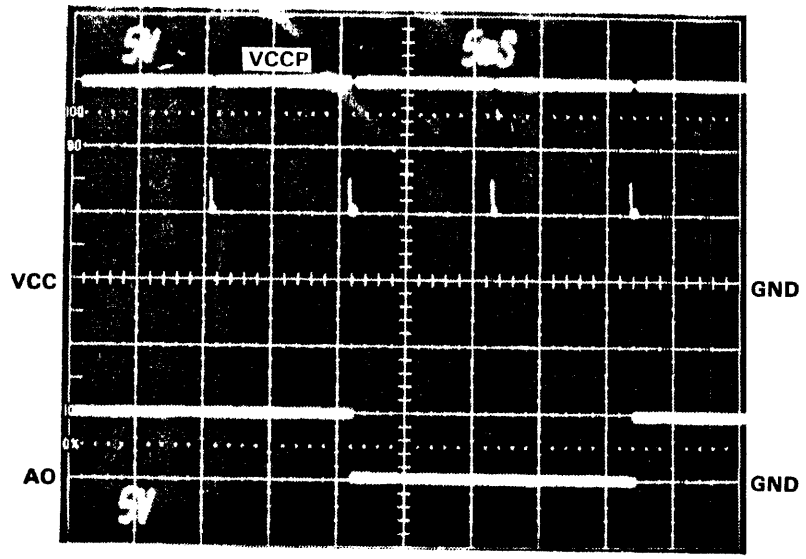
DRAWN BY:

CHECKED BY:

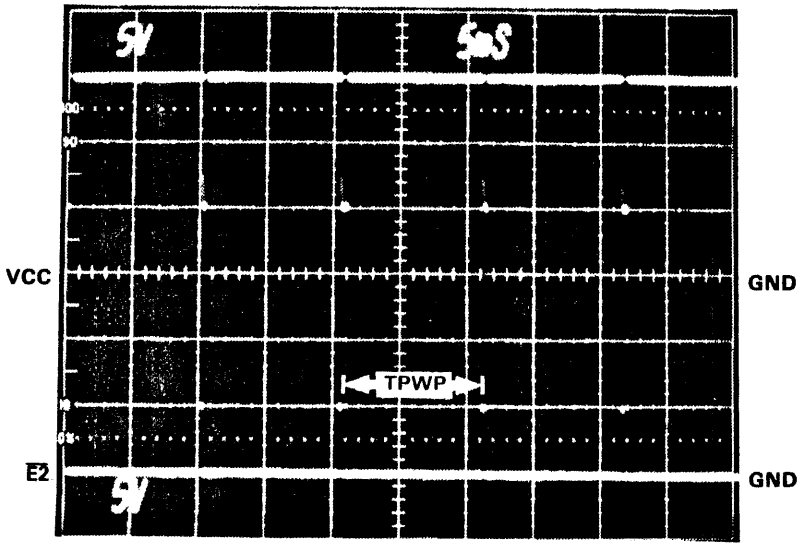
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

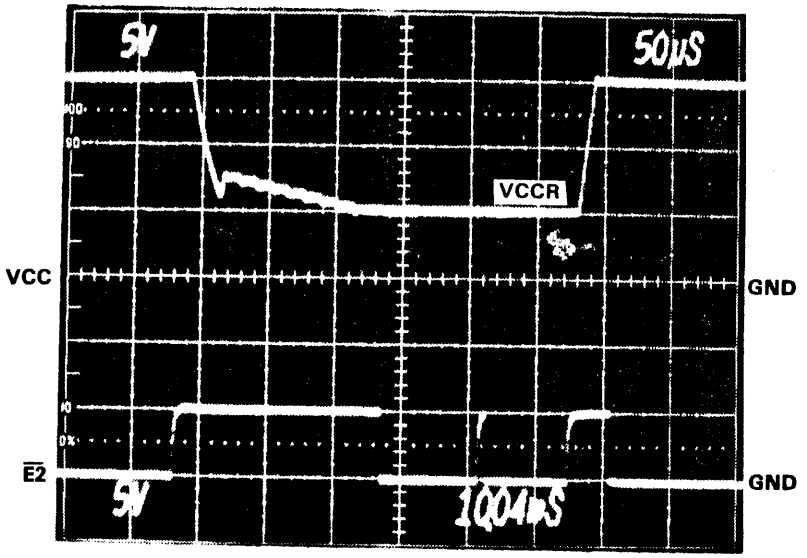
SHEET 2/2


5V
VCCP
5mS
VCC
GND
AO
GND
5V

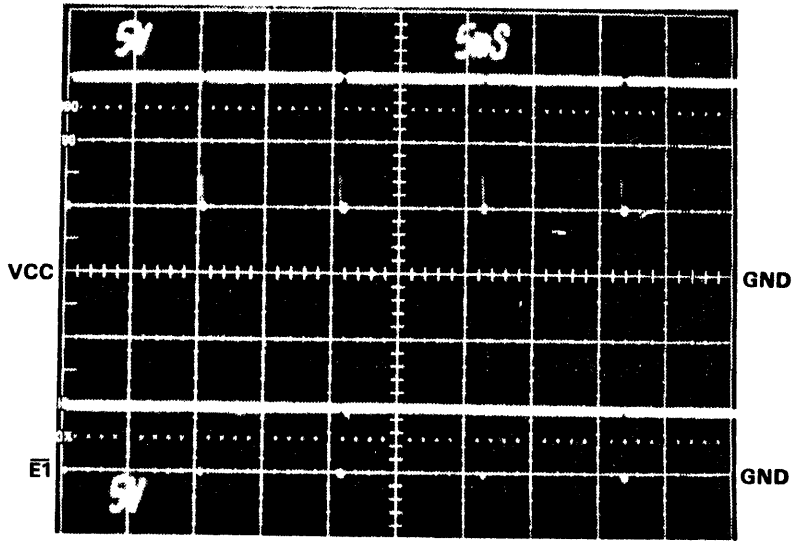
1


5V
5mS
VCC
GND
TPWP
E2
GND
5V

2


5V
50µS
VCCR
VCC
GND
E2
GND
5V
100µS

3


5V
5mS
VCC
GND
E1
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	14.9	15.0	15.1	V	
	VCCR	4.9	5.0	5.1	V	
	TPWE	9.9	10	10.1	ms	Erase pulse width
	TPWP	9.9	10	10.1	ms	Program pulse width
	Reject		2		Pulses	
	Overprogram		0		Pulses	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XX	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 57, 58

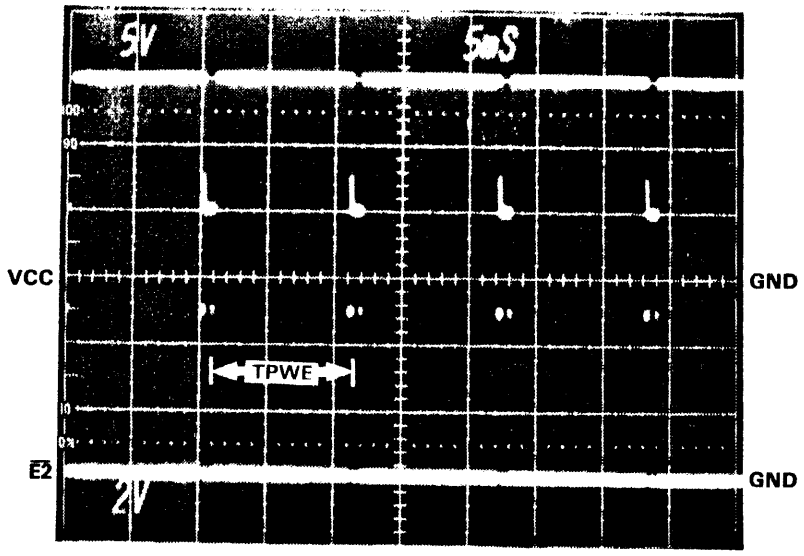
DRAWN BY: EE

CHECKED BY: XX

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

(Erase Waveforms)

4-139
10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XX	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 57, 58

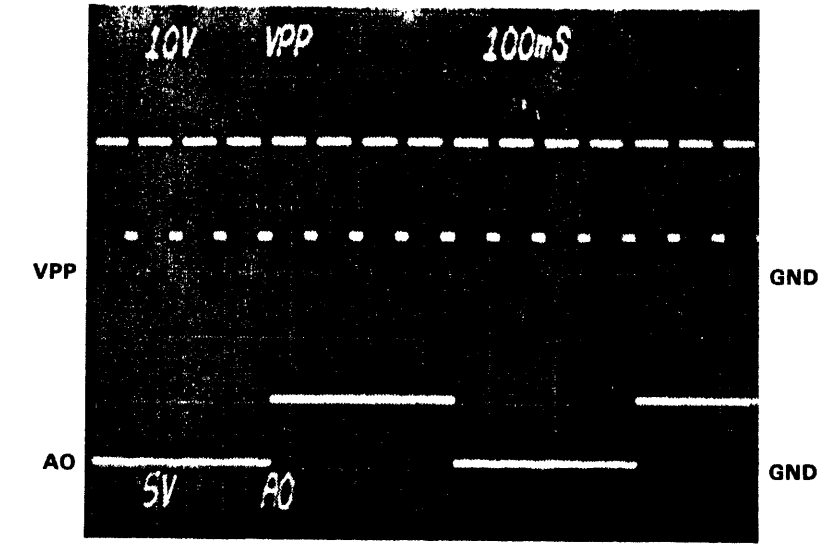
DRAWN BY: EE

CHECKED BY:

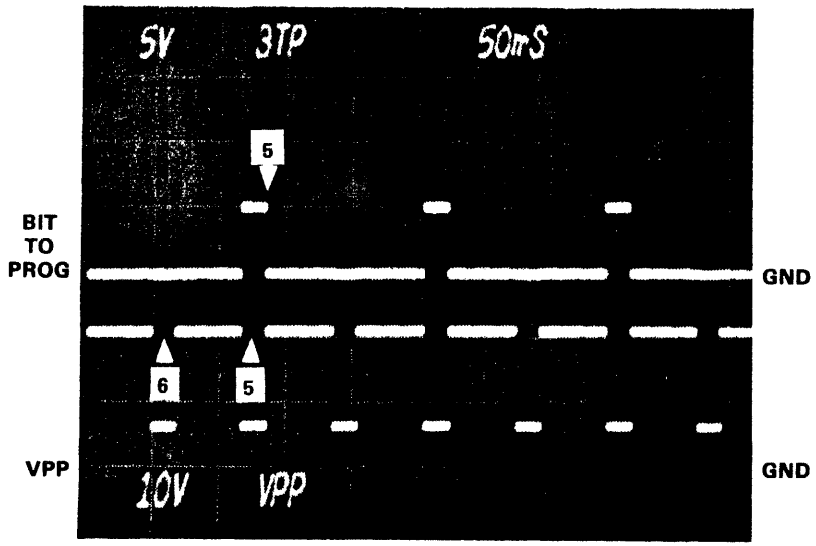
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

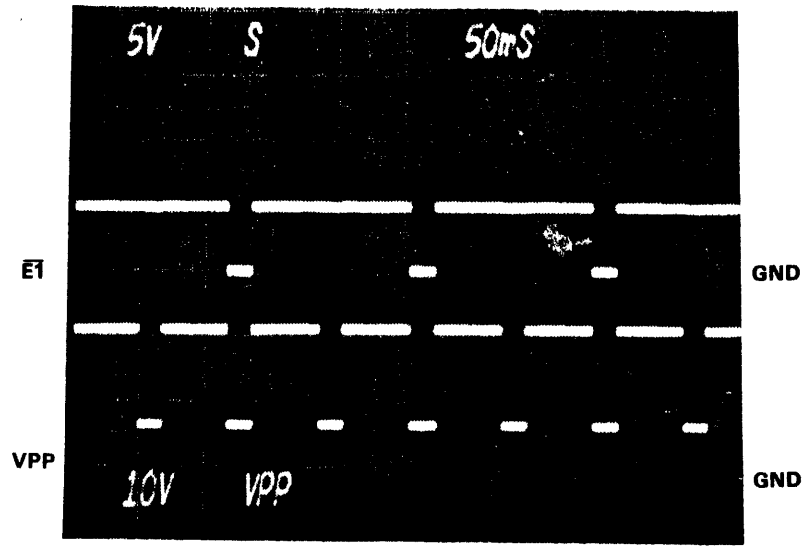
SHEET 2/2


10V VPP 100mS
VPP
GND
AO
GND
5V AO

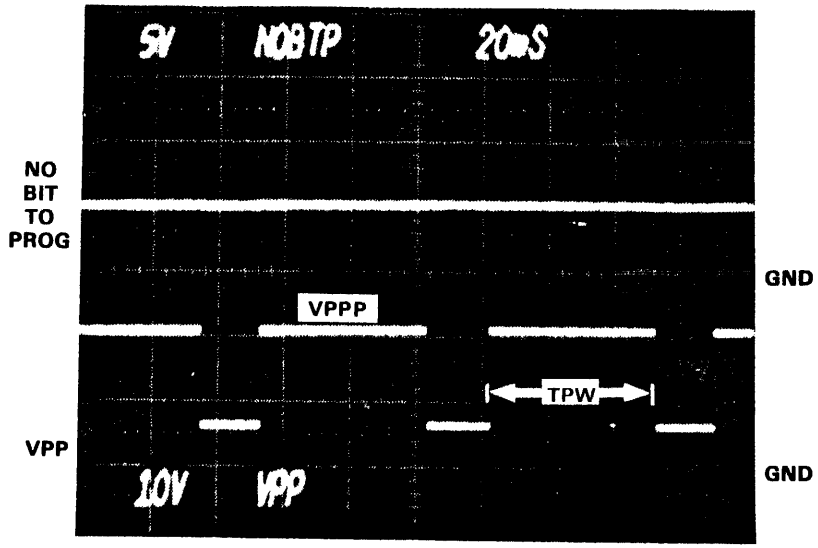
1


5V 3TP 50mS
5
BIT TO PROG
GND
6
5
VPP
GND
10V VPP

2


5V S 50mS
E1
GND
VPP
GND
10V VPP

3


5V NOBTP 20mS
NO BIT TO PROG
GND
VPPP
TPW
VPP
GND
10V VPP

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	Not shown
	VPPP	20.0	20.5	21.0	V	
	TPW	45	50	55	ms	
	Reject		2		Pulses	
	Overprogram		2		Pulses	
	Passes		3		Loops	This algorithm makes 3 passes through the entire range to be programmed.

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		KH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 59, 60

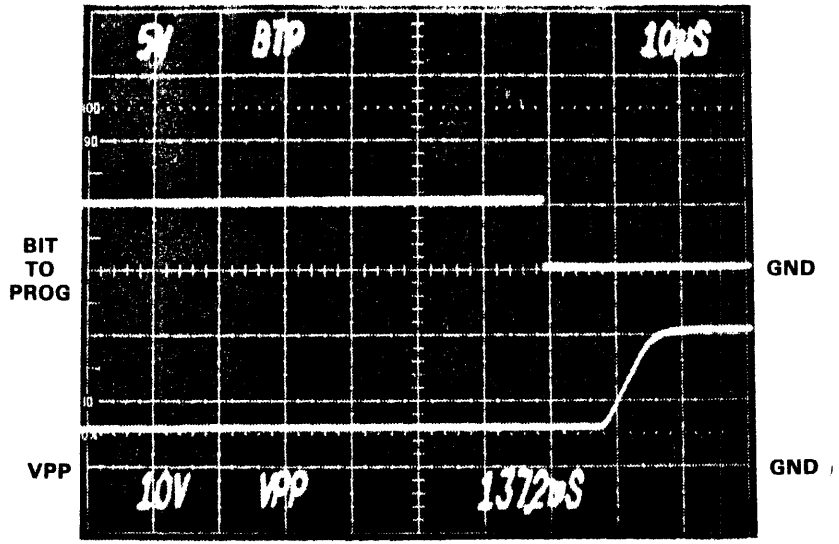
DRAWN BY:

CHECKED BY: KH

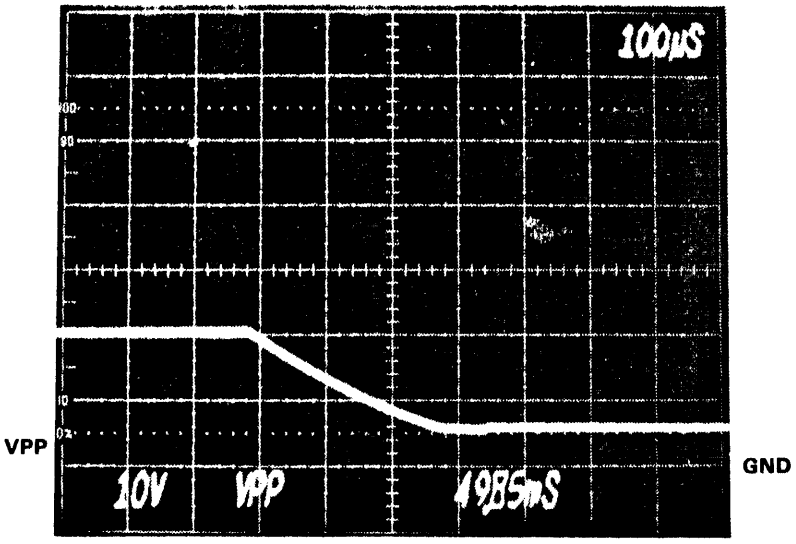
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2


5V
BTP
10µS
BIT
TO
PROG
GND
VPP
GND
10V
VPP
1372µS

5


100µS
VPP
GND
10V
VPP
4985µS

6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		KH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 59, 60

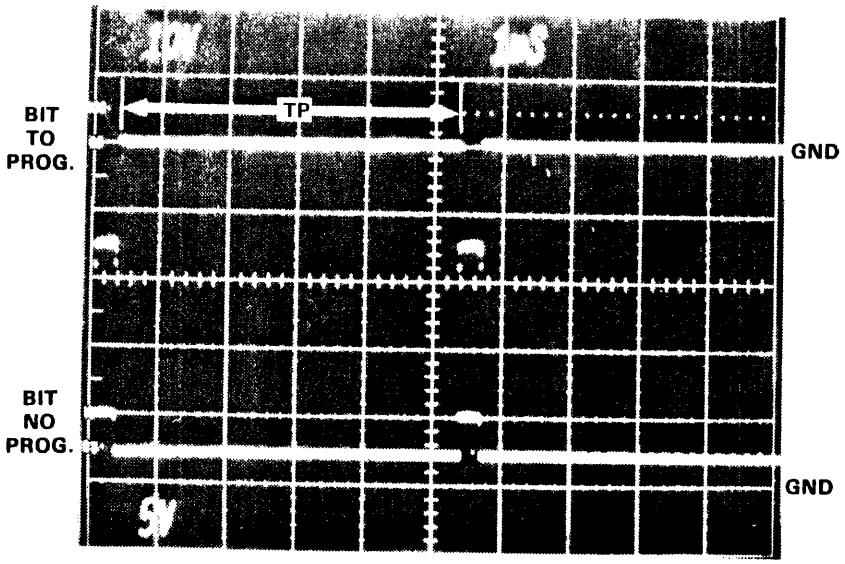
DRAWN BY:

CHECKED BY: KH

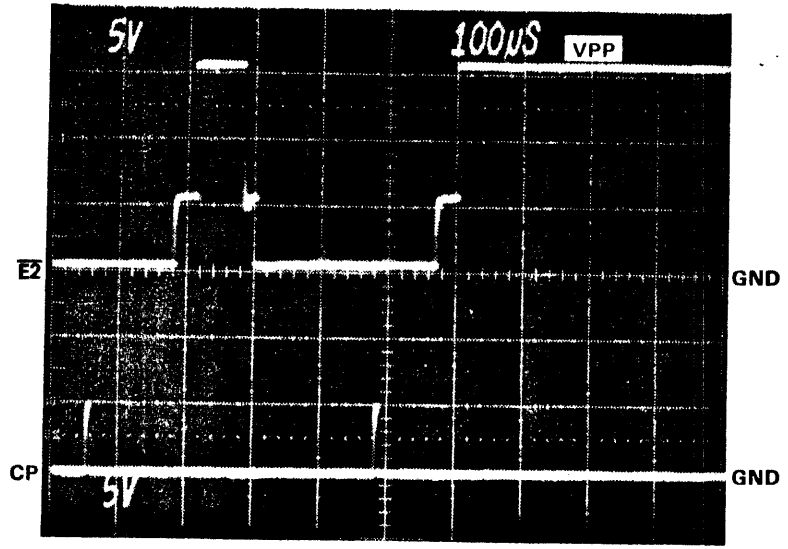
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

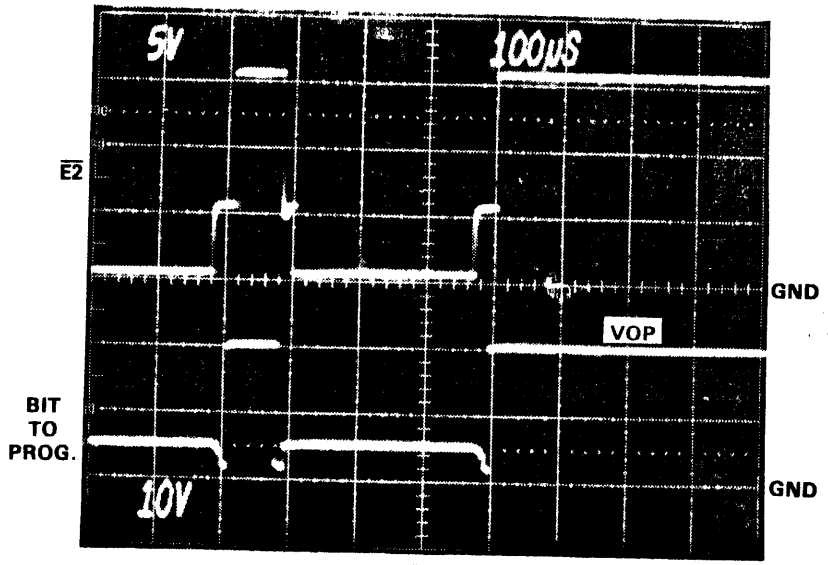
SHEET 2/2


BIT
TO
PROG.
TP
GND
BIT
NO
PROG.
GND
5V

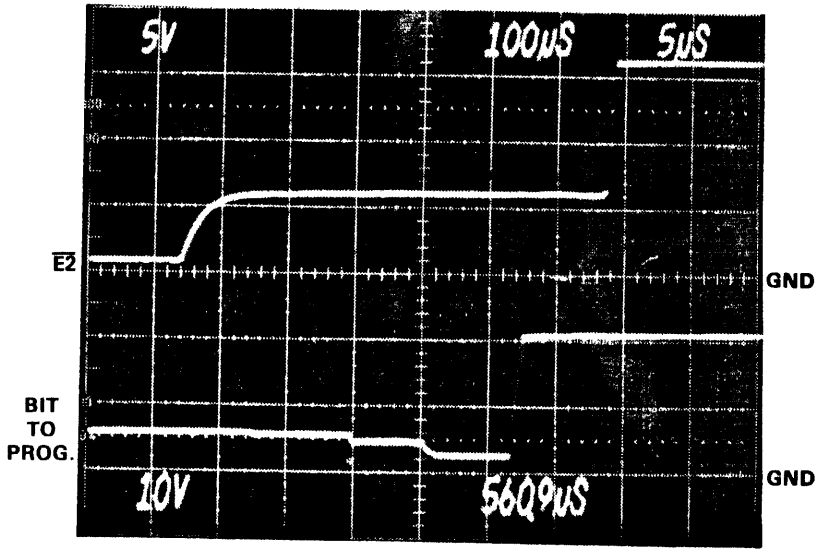
1


5V
100µS
VPP
E2
GND
CP
5V
GND

2


5V
100µS
E2
GND
VOP
BIT
TO
PROG.
10V
GND

3


5V
100µS
5µS
E2
GND
BIT
TO
PROG.
10V
5609µS
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_7 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	5.0	5.25	5.5	V	
VPP	14.5	15.0	15.5	V	
VOP	19.5	20.0	20.5	V	
TPW	5		15	ms	
Overprogram		0		pulses	
Reject		80		pulses	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		FJC	1-14-82
	B	ECN #4630		UJB	7-21-82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODE 61, 62

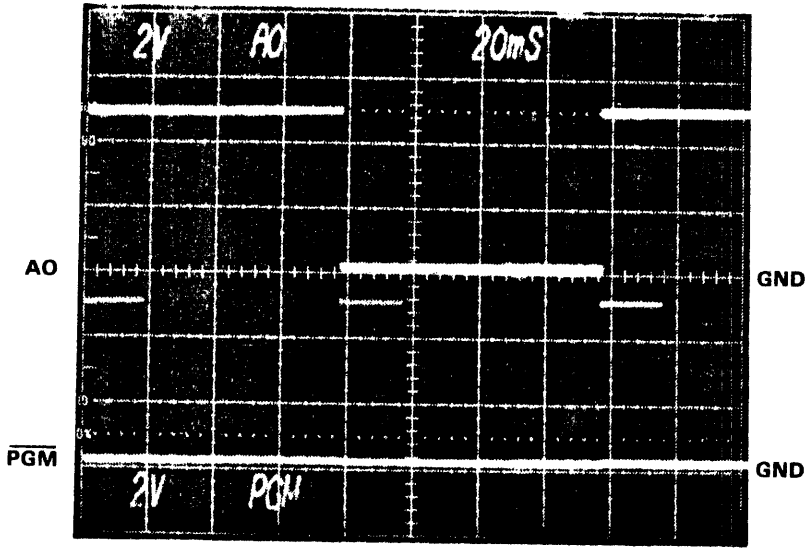
DRAWN BY: KJ

CHECKED BY: D.C.

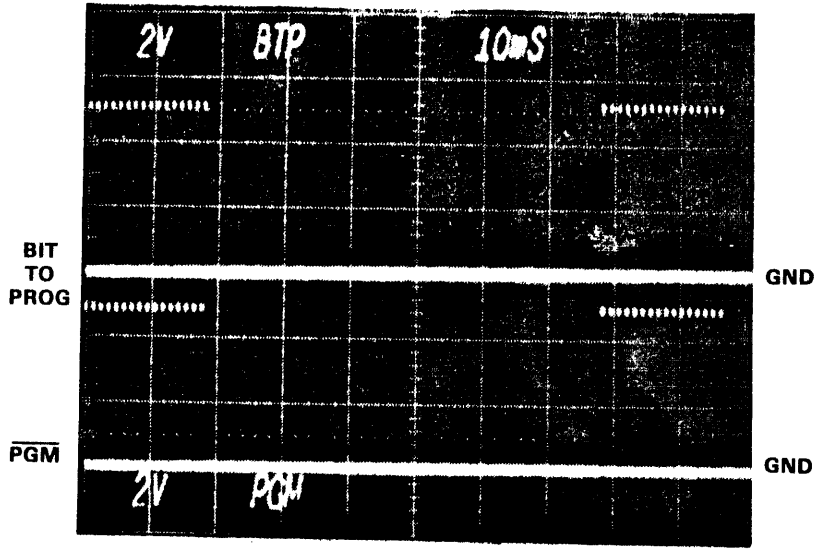
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	007-0061

SCALE

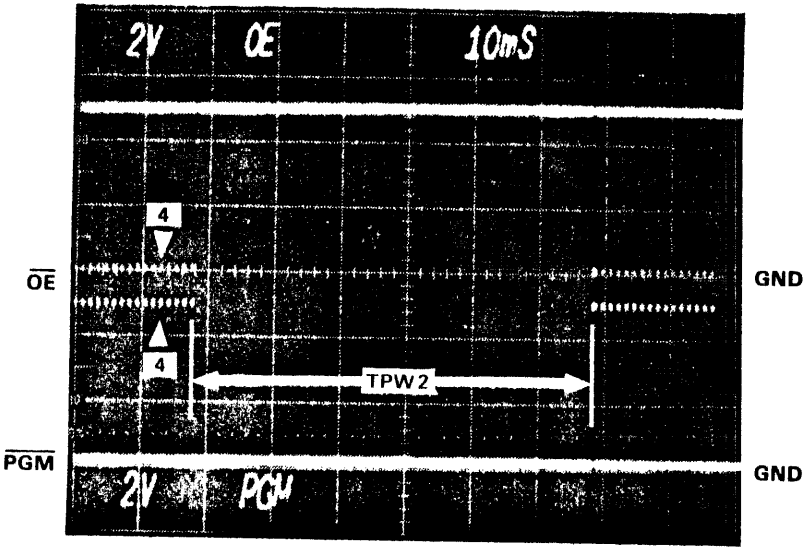
SHEET 1/1


2V
AO
20mS
AO
GND
PGM
GND
2V
PGM

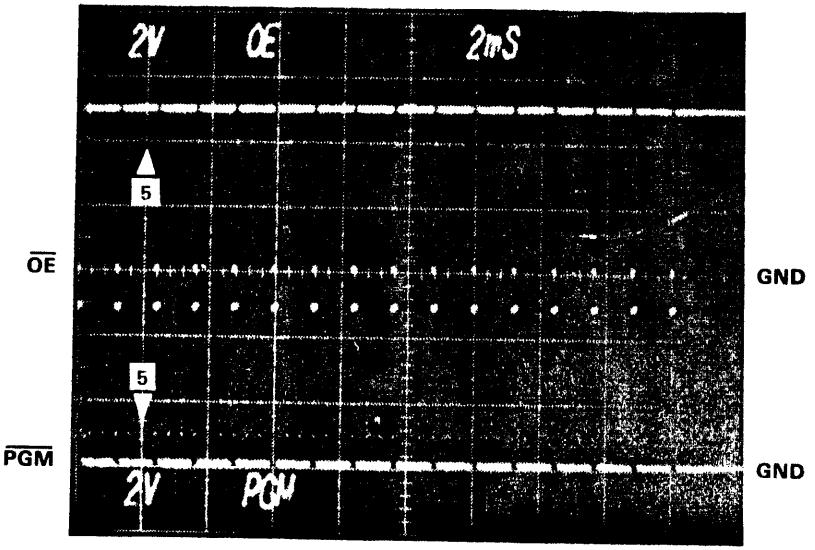
1


2V
BTP
10mS
BIT
TO
PROG
GND
PGM
GND
2V
PGM

3


2V
OE
10mS
4
OE
GND
4
TPW2
PGM
GND
2V
PGM

2


2V
OE
2mS
5
OE
GND
5
PGM
GND
2V
PGM

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	Not shown
	VPP	20.5	21.0	21.5	V	Not shown
	TPW1	.95	1.0	1.05	ms	
	Reject		15		Pulses	
	Overprogram		1		Pulses	
	TPW2	3.8	4X	63	ms	x = number of pulses applied to that byte prior to it verifying

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728			11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 79, 80

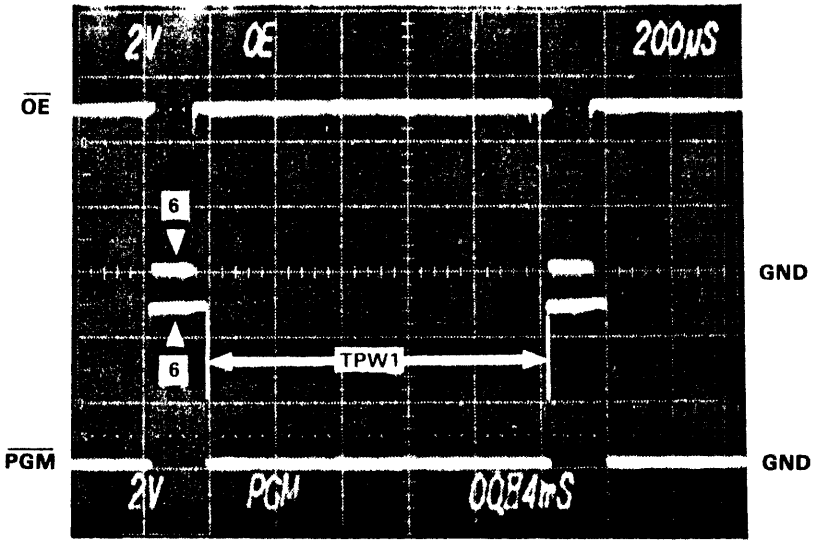
DRAWN BY: P.P.

CHECKED BY:

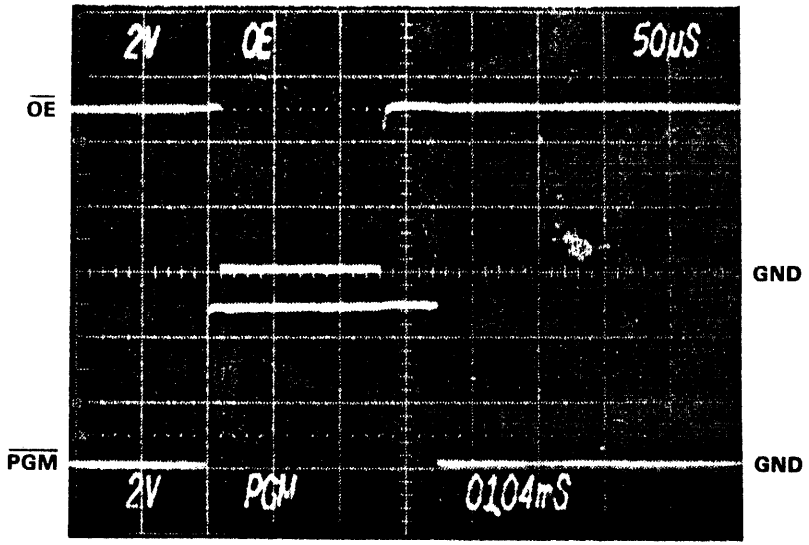
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2


2V
OE
200µS
OE
6
GND
6
TPW1
PGM
GND
2V
PGM
0Q84mS

5


2V
OE
50µS
OE
GND
PGM
GND
2V
PGM
0104mS

6

4-149
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 79, 80

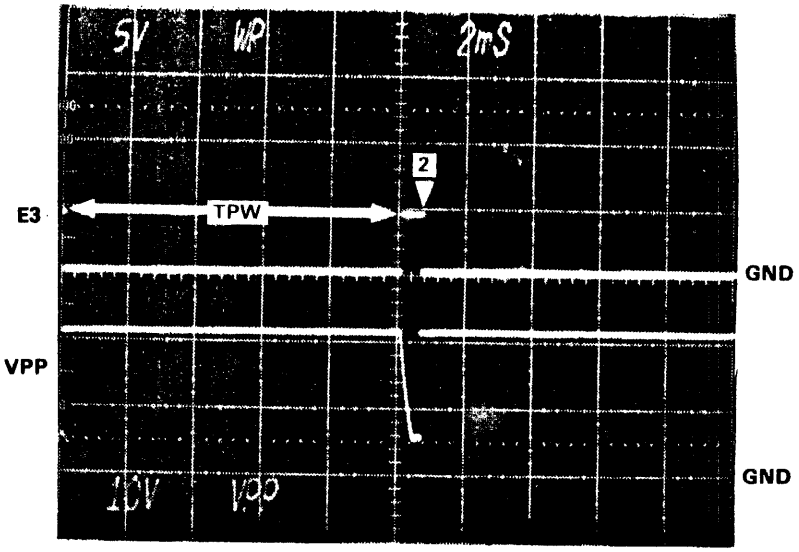
DRAWN BY: P.F.

CHECKED BY: XH

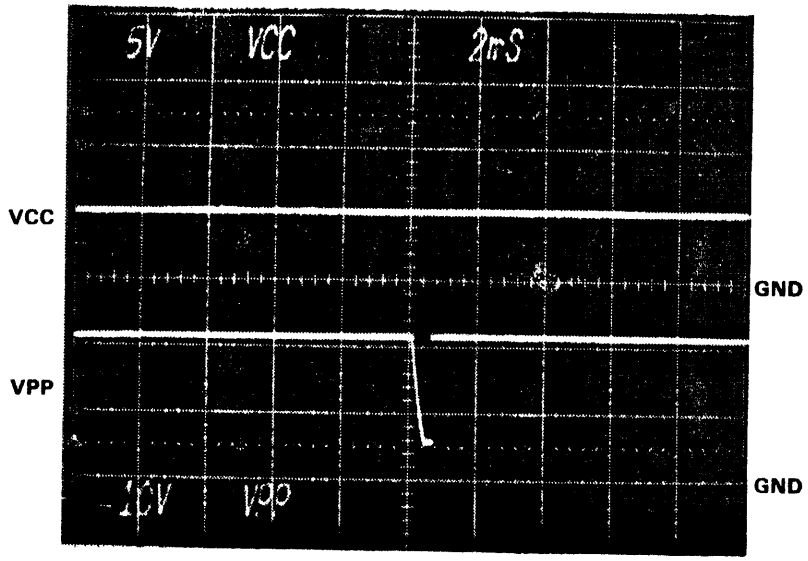
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

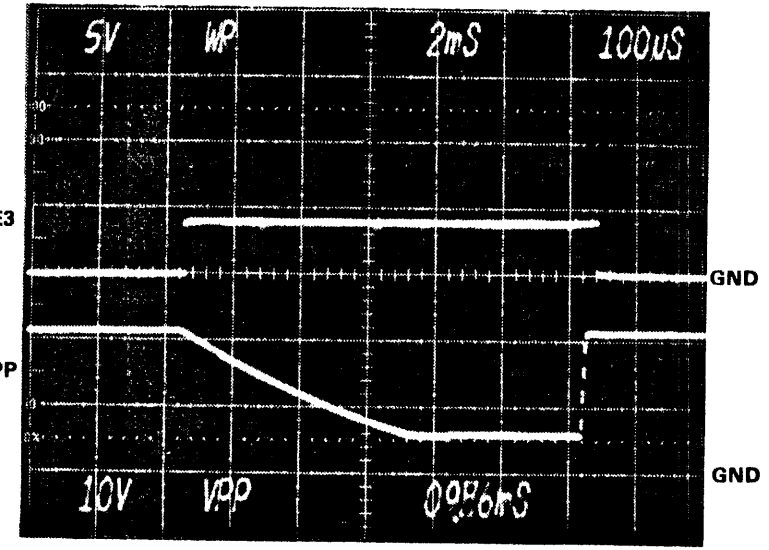
SHEET 2/2


5V
WP
2mS
2
E3
TPW
GND
VPP
GND
10V
Vpp

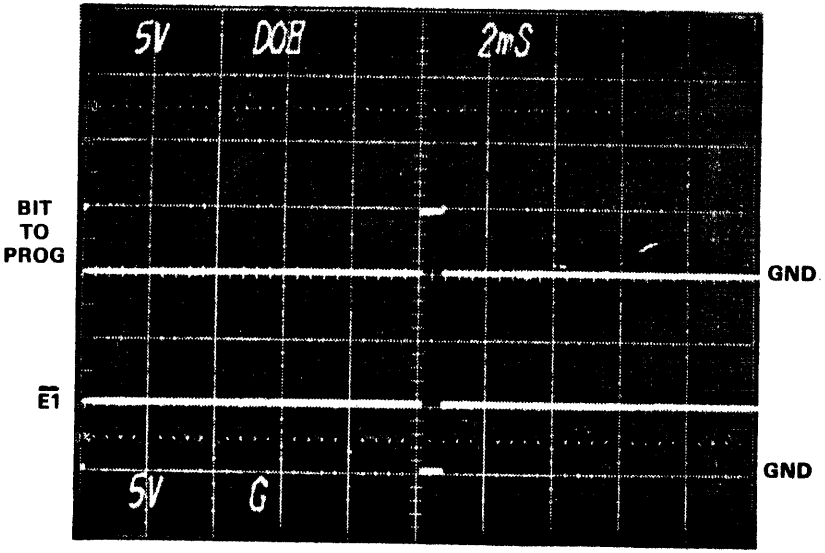
1


5V
VCC
2mS
VCC
GND
VPP
GND
10V
Vpp

3


5V
WP
2mS
100uS
E3
GND
VPP
GND
10V
Vpp

2


5V
DOB
2mS
BIT
TO
PROG
GND
E1
GND
5V
G

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact or a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no- bit-to-program, use O_3 for a 4-bit PROM Or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.50	5.00	5.50	V	
VPP	20	21	22	V	DURING PROG, ERASE
TPW	9.5	10.0	10.5	msec	
REJECT	–	1	–	PULSES	
OVERPROGRAM	–	0	–	PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		MR	9/8

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODE 81, 82

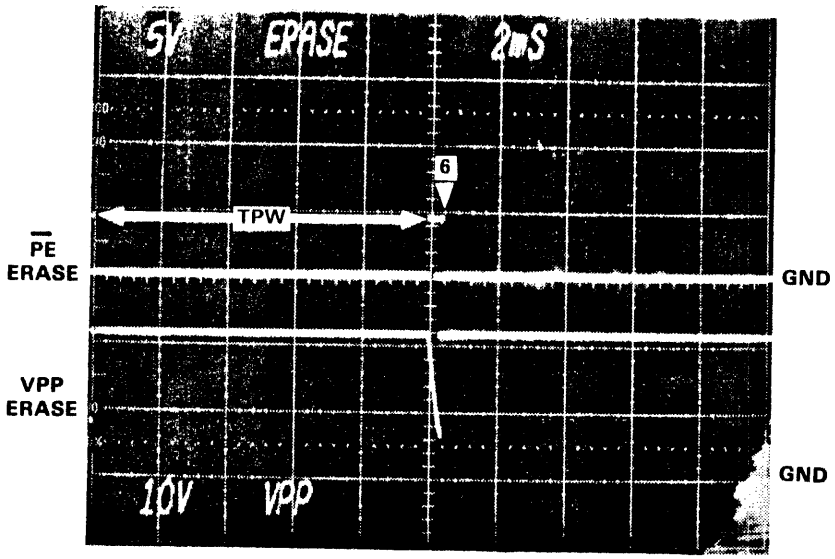
DRAWN BY:

CHECKED BY:

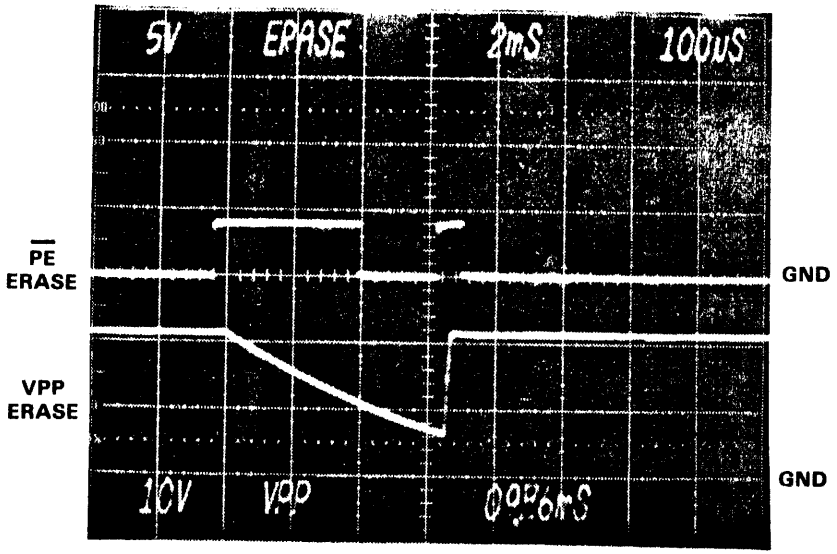
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0076

SCALE

SHEET 1/2


5V
ERASE
2mS
6
TPW
PE
ERASE
GND
VPP
ERASE
GND
10V
VPP

5


5V
ERASE
2mS
100uS
PE
ERASE
GND
VPP
ERASE
GND
10V
VPP

6

4-153
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 81, 82

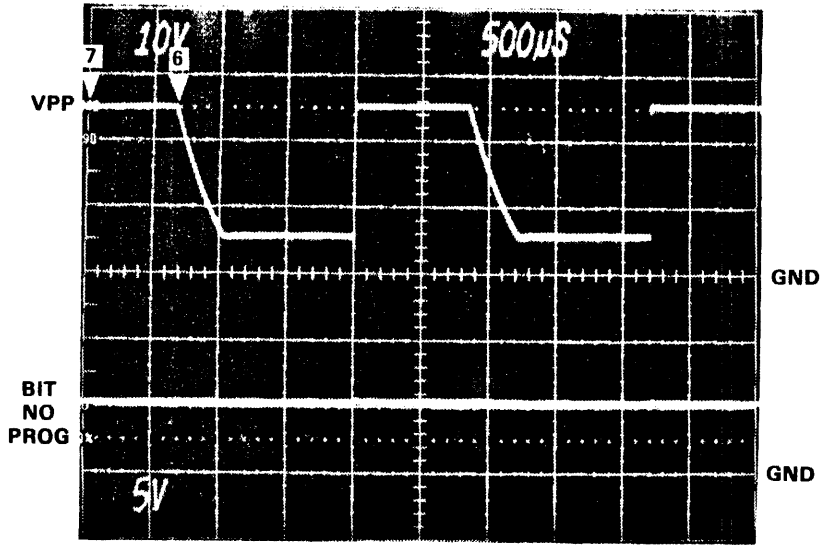
DRAWN BY:

CHECKED BY:

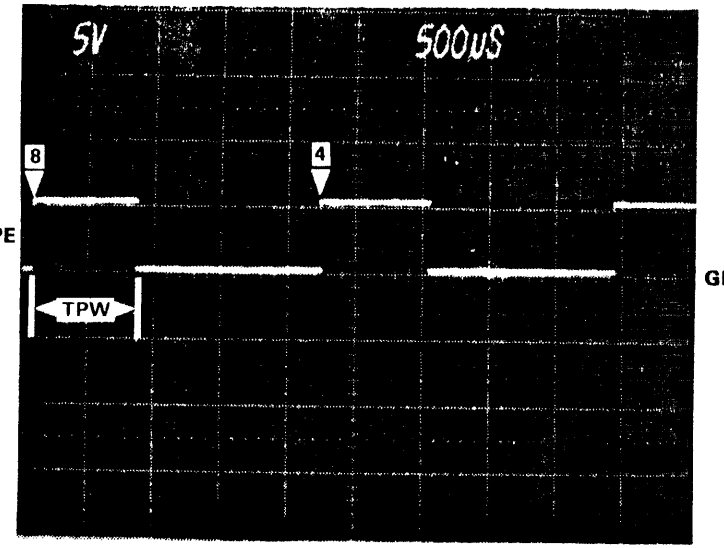
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0076

SCALE

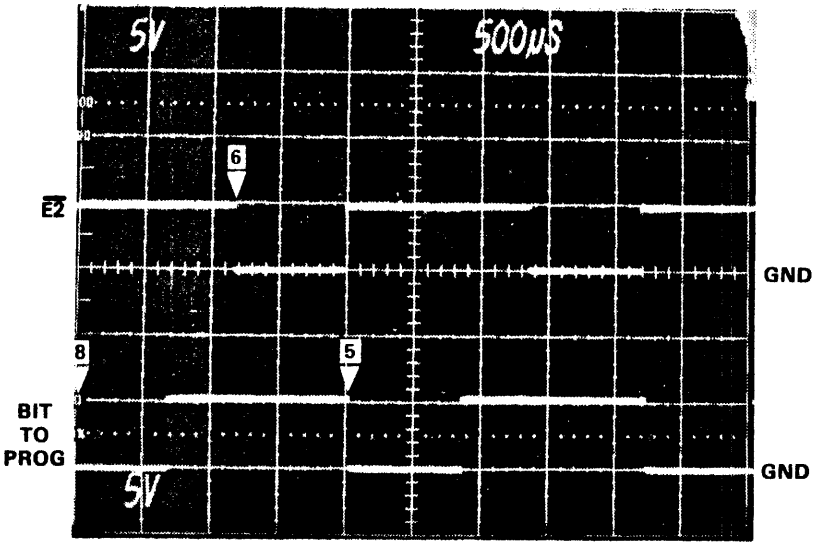
SHEET 2/2


10V
500µS
7
6
VPP
GND
BIT
NO
PROG
GND
5V

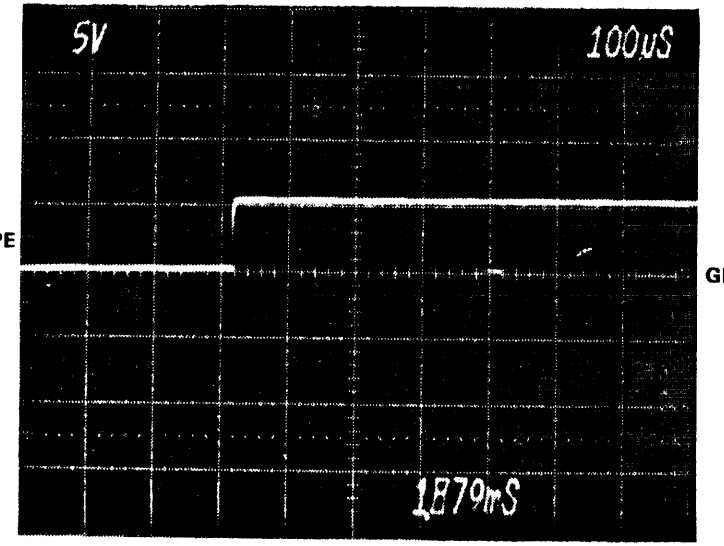
1


5V
500µS
8
4
PE
GND
TPW

3


5V
500µS
6
E2
GND
8
5
BIT
TO
PROG
GND
5V

2


5V
100µS
PE
GND
1.879mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*

2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*

3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact or a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no- bit-to-program, use O_3 for a 4-bit PROM Or O_1 for an 8-bit PROM.*

4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*

5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

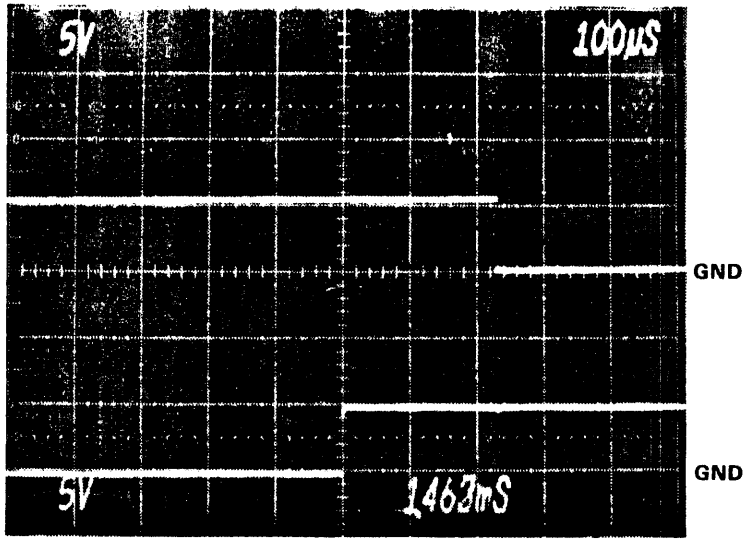
VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCP	4.75	5.0	5.25	V	
VPP	24	25	26	V	
VPPV	4.75	5.0	5.25	V	
TPW	800	—	—	µs	
TD	2	—	—	µs	
TR	.05	—	—	µs	
TF	.05	—	—	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	

REVISIONS

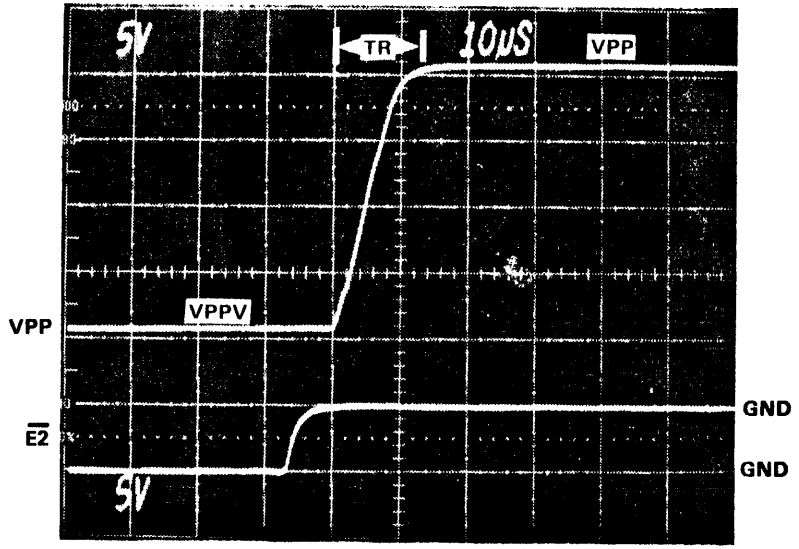
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		BWR	7/82

DATA I/O ISSAQUAH, WA

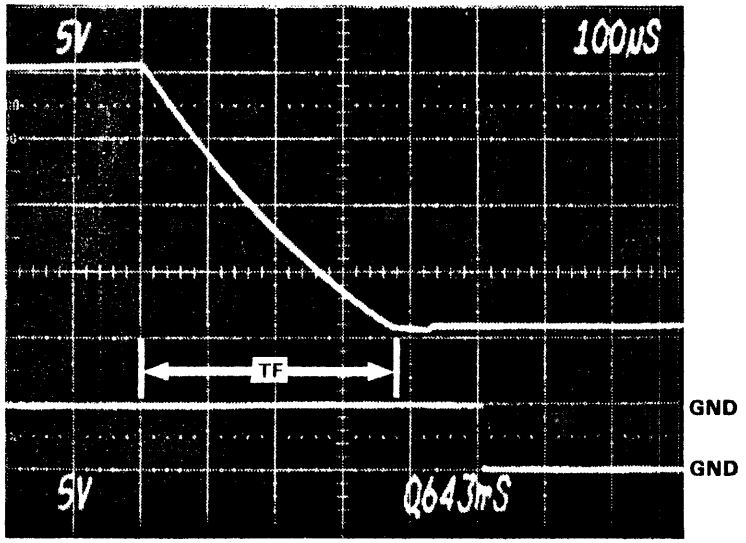
TITLE: TIMING DIAGRAM FAMILY CODE 83, 84	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0076	
SCALE	SHEET 1/2


5V
100µS
BIT
TO
PROG
GND
A0
GND
5V
1463mS

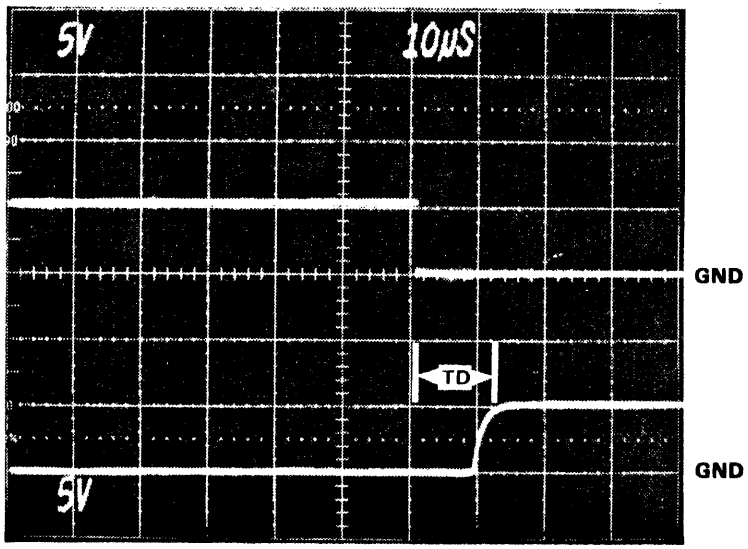
5


5V
TR
10µS
VPP
VPPV
VPP
E2
GND
GND
5V

6


5V
100µS
VPP
TF
GND
E2
GND
5V
Q643mS

7


5V
10µS
BIT
TO
PROG
GND
TD
PE
GND
5V

8

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 83, 84

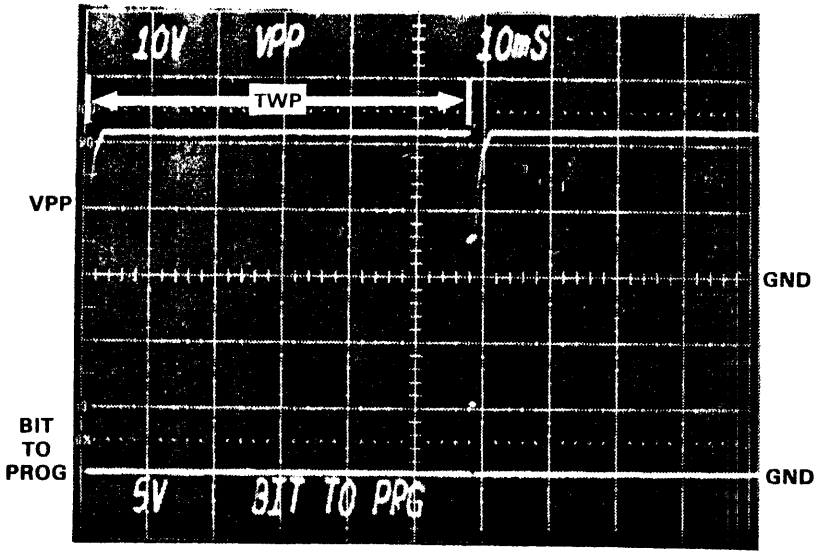
DRAWN BY:

CHECKED BY:

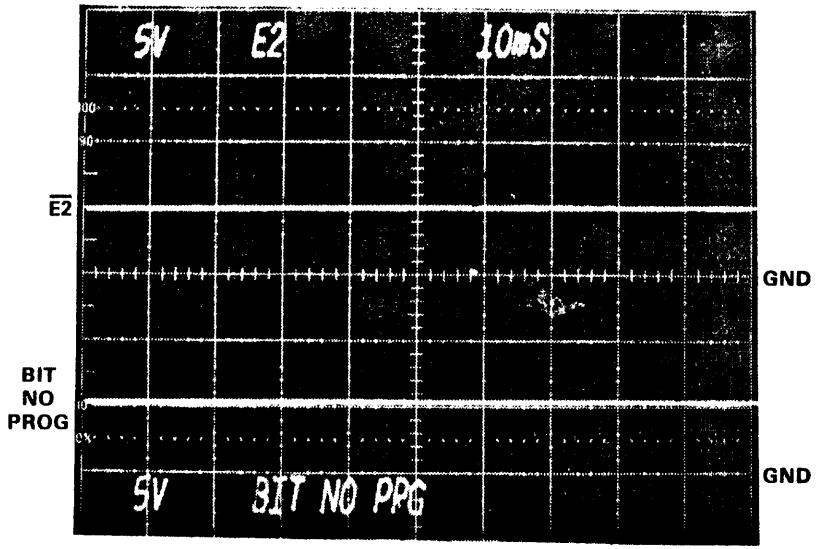
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0076

SCALE

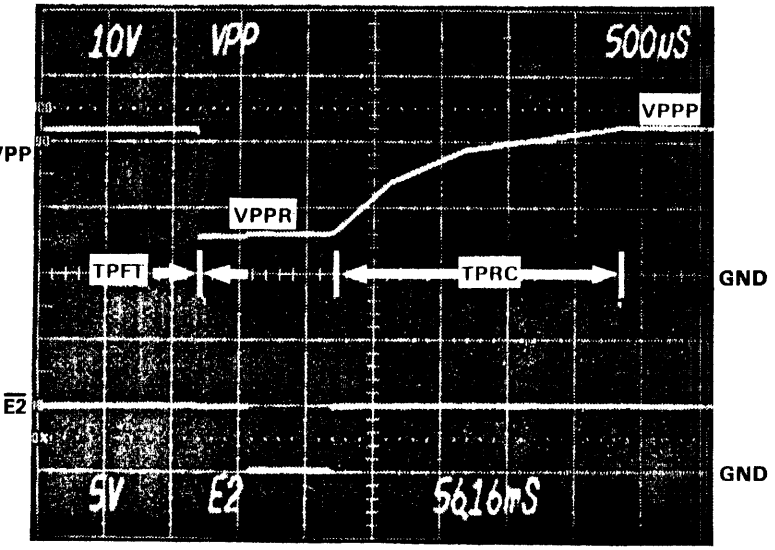
SHEET 2/2



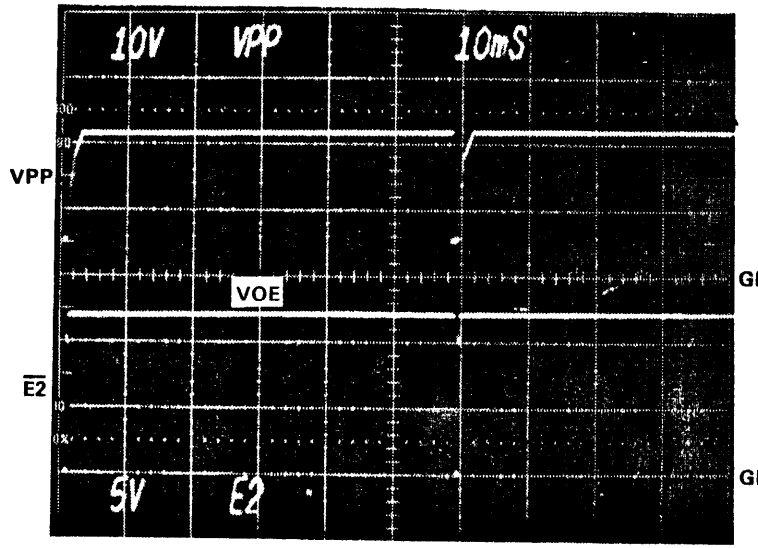
1



3



2



4
(ERASE CYCLE)

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact or a 4-bit PROM or O_8 for an 8-bit PROM. To observe a no- bit-to-program, use O_3 for a 4-bit PROM Or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VPPP	20.0	21.0	22.0	V	
VPPR	4.0	4.6	6.0	V	
VCC	4.75	5.0	5.25	V	
VOE	9.0	12.0	15.0	V	
TWP	50	58	70	ms	
TPFT	—	—	100	µs	
TPRC	450	600	750	µs	EFFECTIVE TIME CONSTANT
OVERPROGRAM		0		PULSES	
REJECT		2		PULSES	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	ECN #4516		MWR	9/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODE 85, 86

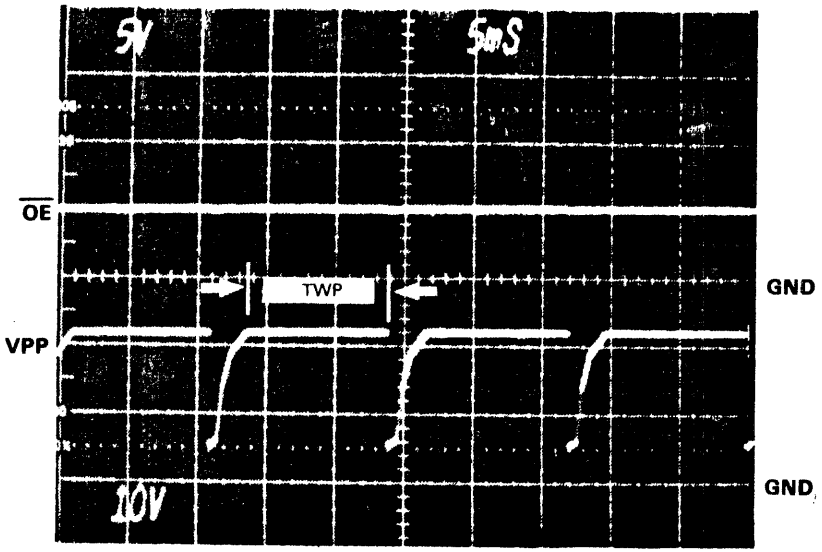
DRAWN BY:

CHECKED BY:

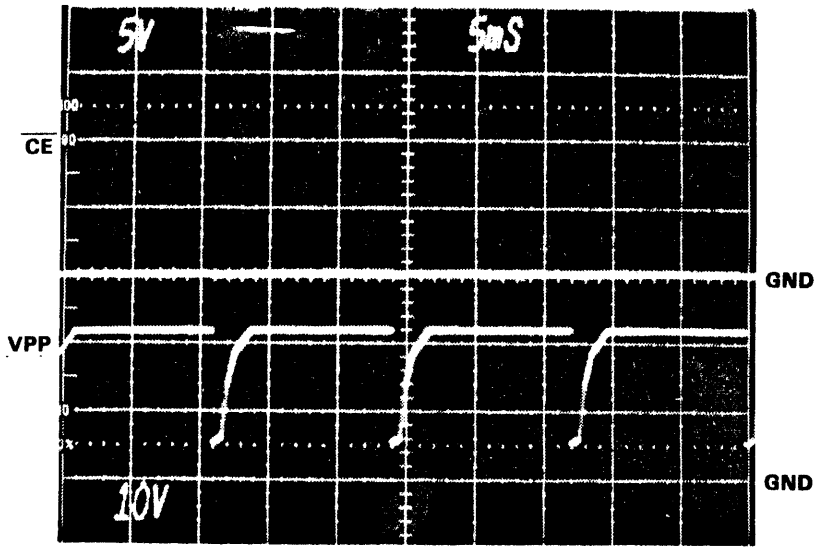
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0076

SCALE

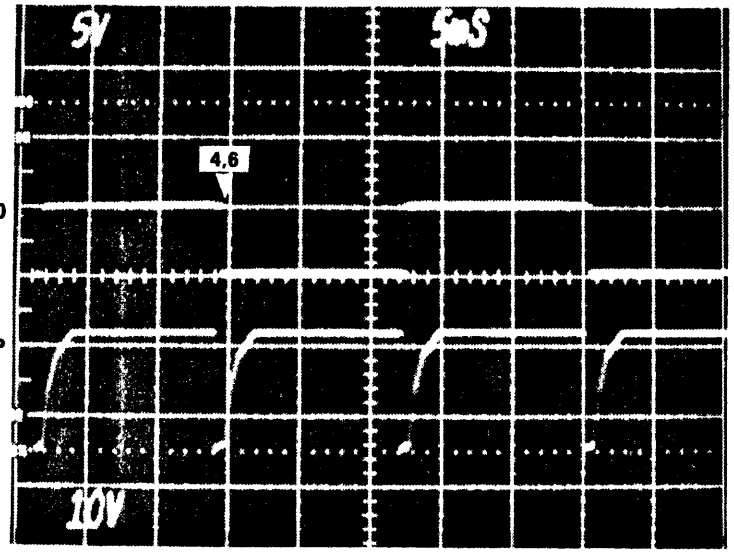
SHEET 1/1


5V
5mS
OE
TWP
GND
VPP
GND
10V

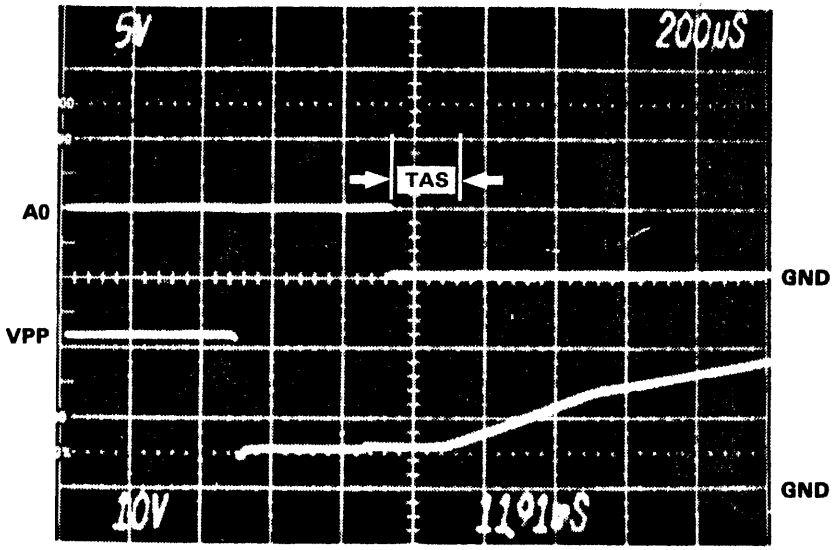
1


5V
5mS
CE
GND
VPP
GND
10V

2


5V
5mS
4,6
A0
GND
VPP
10V

3


5V
200uS
TAS
A0
GND
VPP
GND
10V
1191uS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
BYTE ERASE					
VPP	20.0	21.0	22.0	V	
TWP	9	10	15	ms	
TAS	150			ns	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

4-161
10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			5/17/85

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 85,86
BYTE ERASE

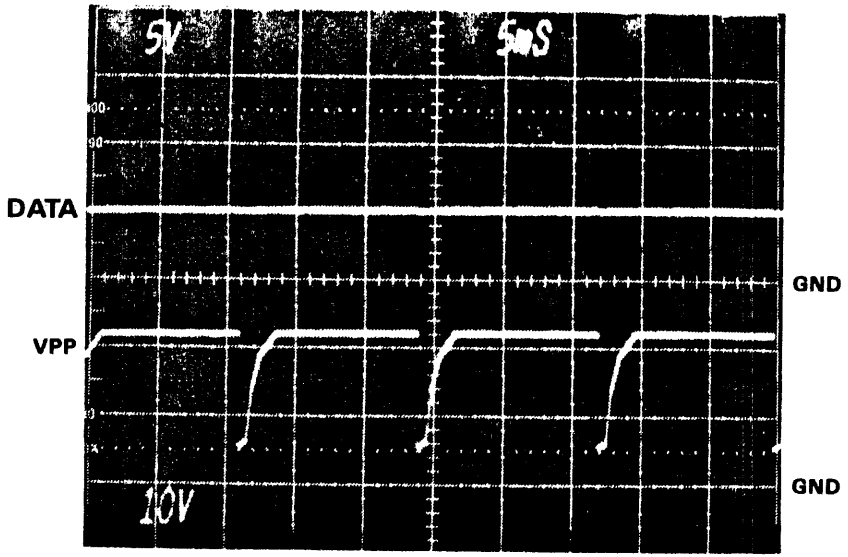
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 85, 86
BYTE ERASE

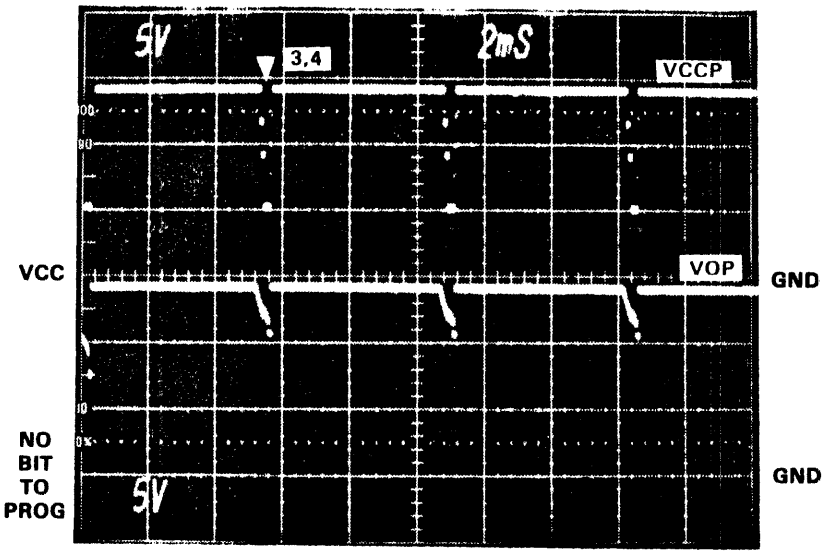
DRAWN BY:

CHECKED BY:

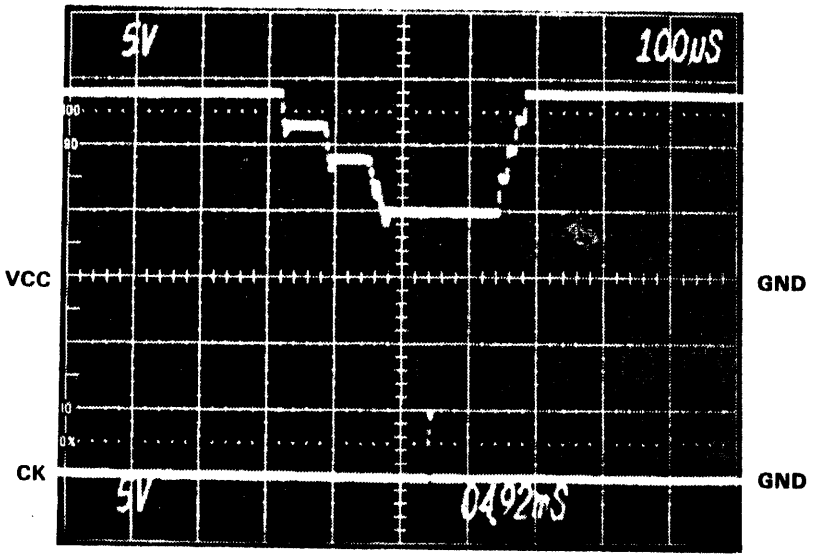
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

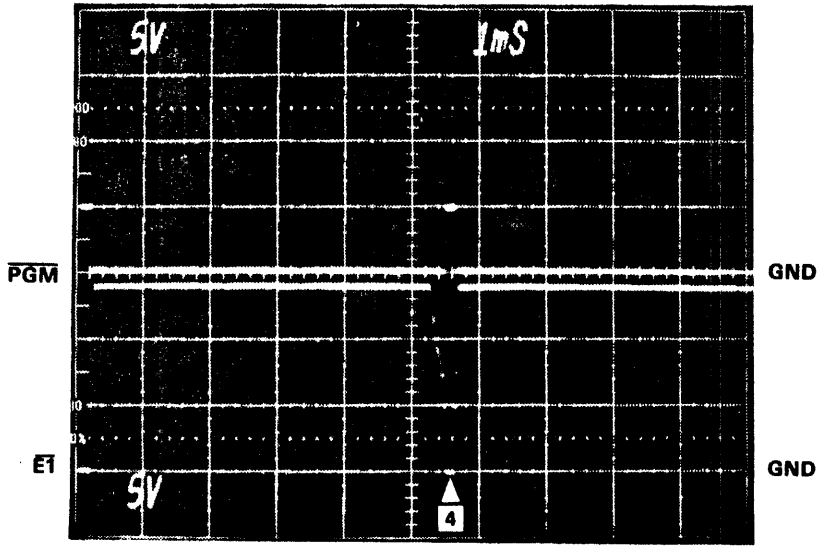
SHEET 2/2


5V
3.4
2mS
VCCP
VCC
VOP
GND
NO
BIT
TO
PROG
GND
5V

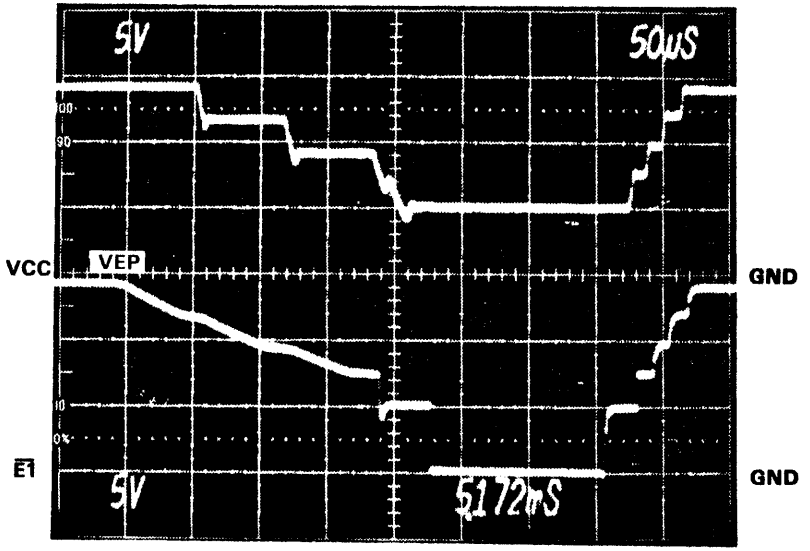
1


5V
100uS
VCC
GND
CK
GND
5V
0492mS

3


5V
1mS
PGM
GND
E1
GND
5V
4

2


5V
50uS
VCC
VEP
GND
E1
GND
5V
5172mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

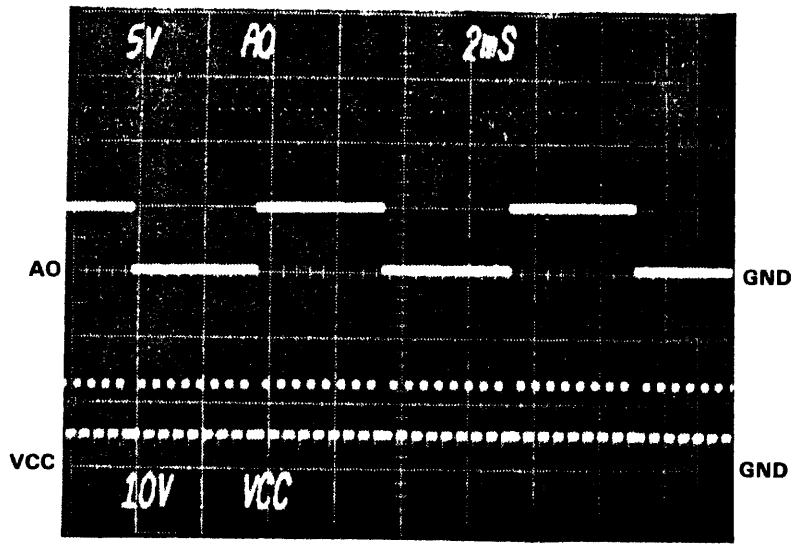
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	13.5	14.0	14.5	V	
	VEP	13.5	14.0	14.5	V	
	VOP	13.5	14.0	14.5	V	
	TPW	4.5		5.5	ms	
	Reject		8		Pulses	
	Overprogram		0		Pulses	

REVISIONS

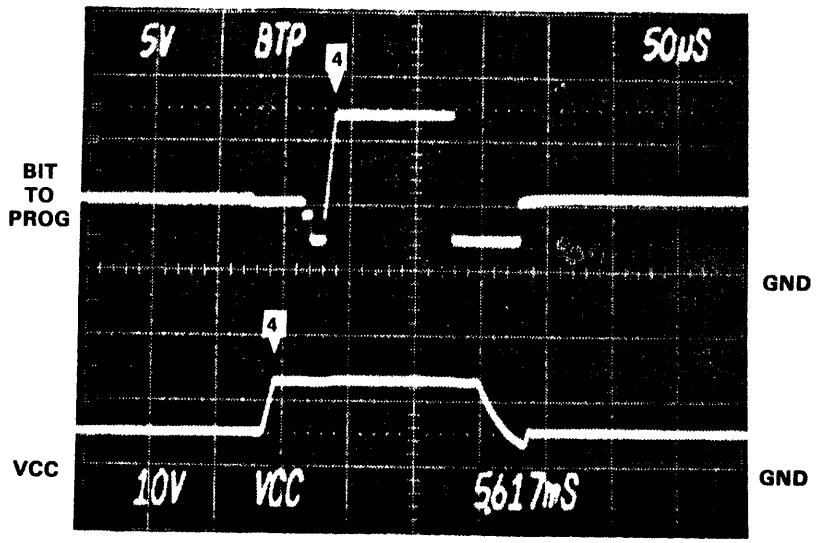
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

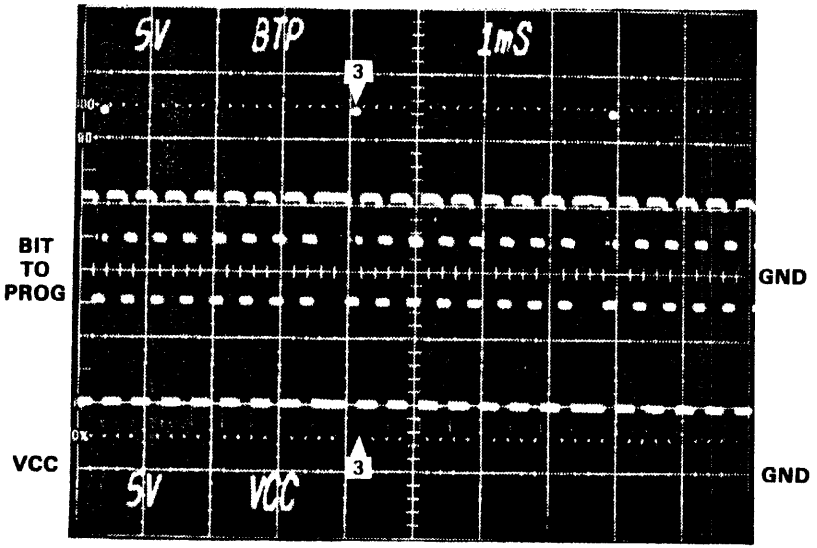
TITLE: TIMING DIAGRAM FAMILY CODES 87, 88	DRAWN BY: P.R	CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE		SHEET 1/1


5V
AO
2mS
AO
GND
VCC
GND
10V
VCC

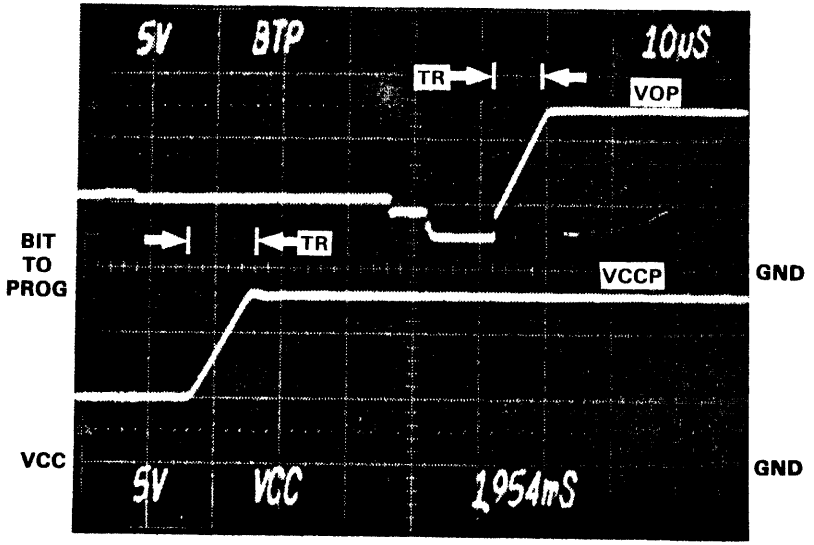
1


5V
BTP
4
50µS
BIT
TO
PROG
GND
4
VCC
GND
10V
VCC
5617mS

3


5V
BTP
3
1mS
BIT
TO
PROG
GND
VCC
3
GND
5V
VCC

2


5V
BTP
10µS
TR
VOP
BIT
TO
PROG
TR
VCCP
GND
VCC
GND
5V
VCC
1.954mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCR	4.5	5.0	5.5	V	
	VCCP	12.5	12.75	13.0	V	
	VOP	11.5	12.0	12.5	V	
	TPW	40	50	60	µs	
	TR	5		20	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XX	11/82

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

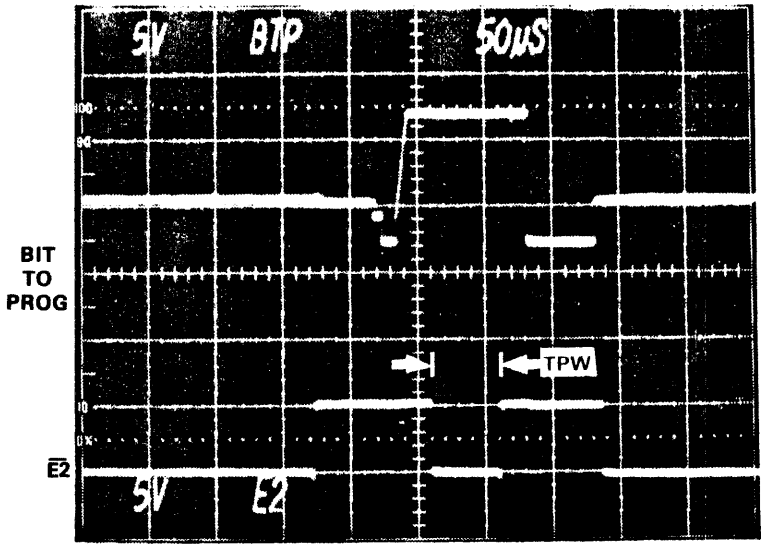
DRAWN BY: EE

CHECKED BY: XX

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



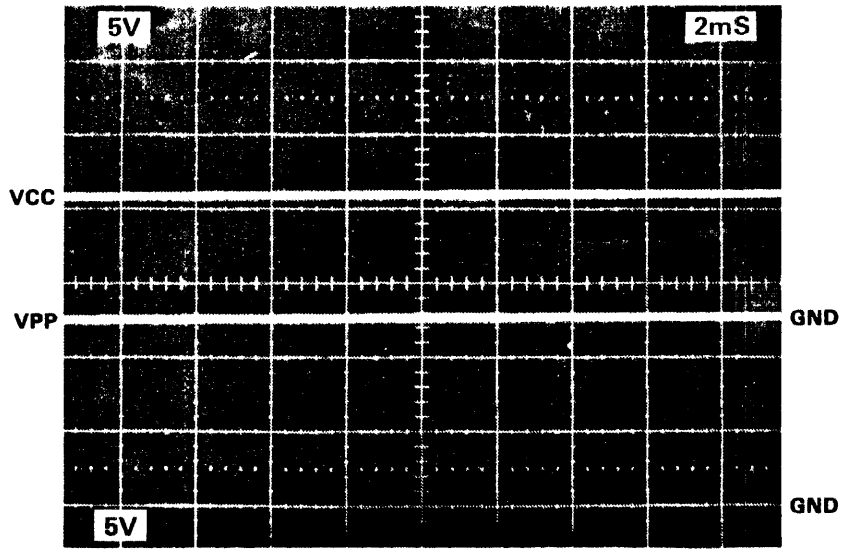
5

4-169
10-950-0099

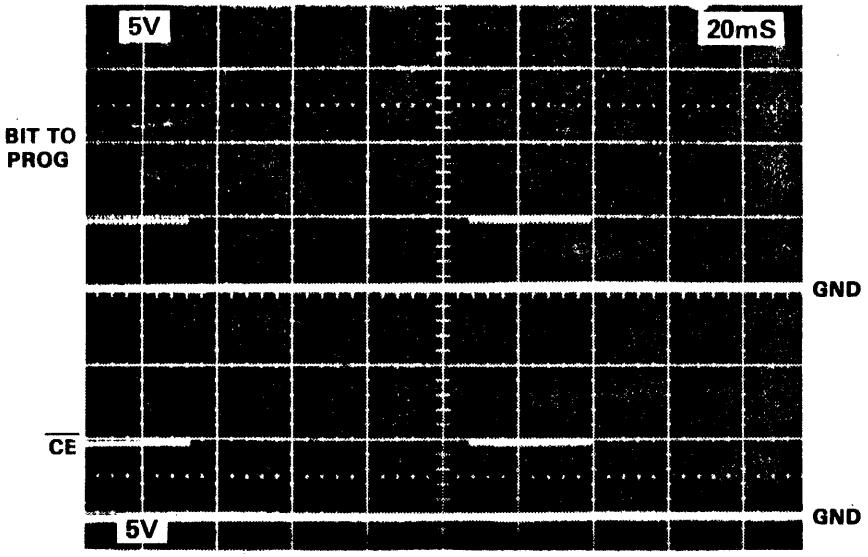
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		ZH	11/82

DATA I/O ISSAQUAH, WA

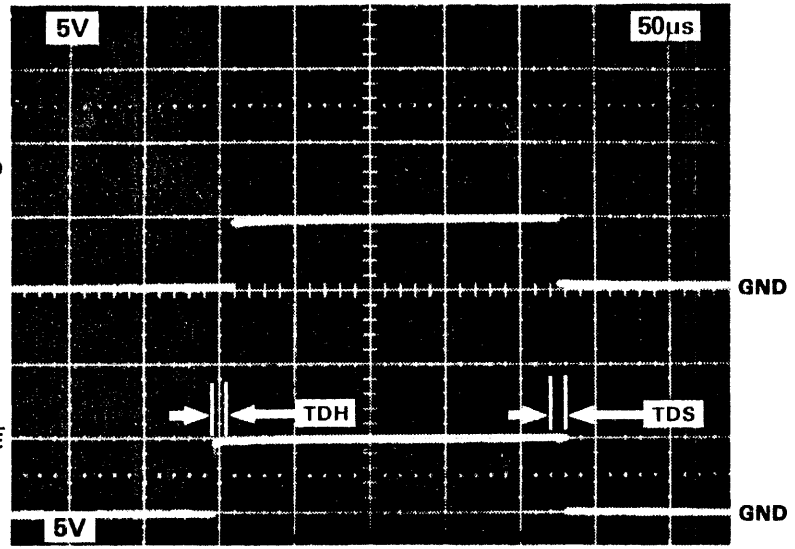
TITLE: TIMING DIAGRAM FAMILY CODES 91, 92			DRAWN BY: CHECKED BY: ZH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099	
SCALE			SHEET 2/2


5V
2mS
VCC
VPP
GND
GND
5V

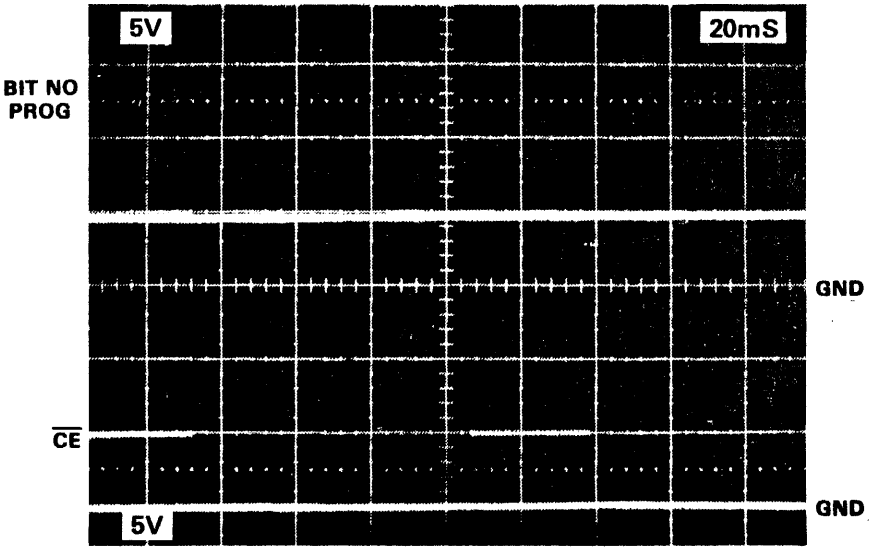
1


5V
20mS
BIT TO PROG
GND
CE
GND
5V

2


5V
50µs
BIT TO PROG
GND
CE
TDH
TDS
GND
5V

3


5V
20mS
BIT NO PROG
GND
CE
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_5 for an 8-bit PROM. To observe a no-bit-to-program, use O_5 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *The most significant address line will not toggle when viewing waveforms in the calibration mode.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VCC	5.75	6.0	6.25	V	
VPP		12.5		V	
TPW	0.95	1.0	1.05	ms	
TOES	2			µs	
REJECT		25		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 93, 94

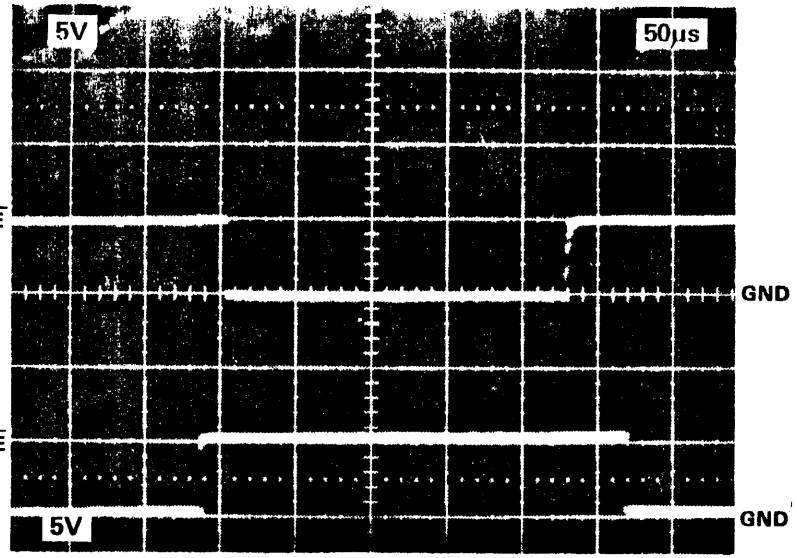
DRAWN BY:

CHECKED BY:

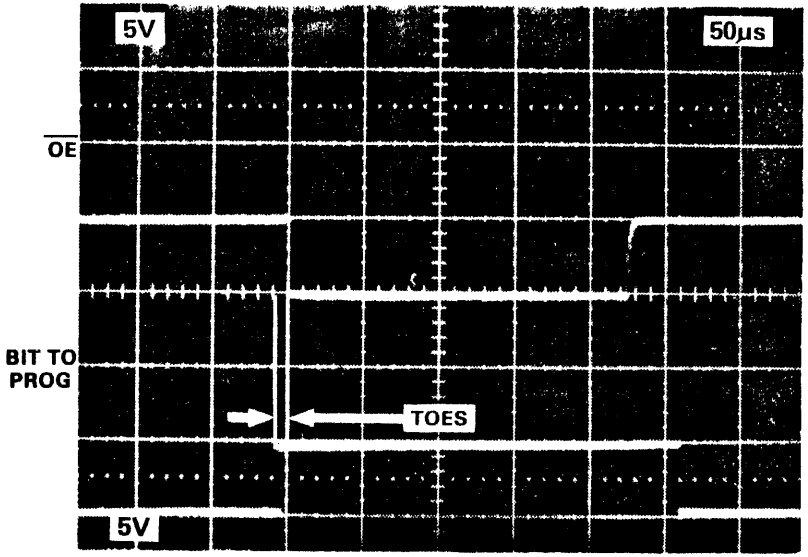
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

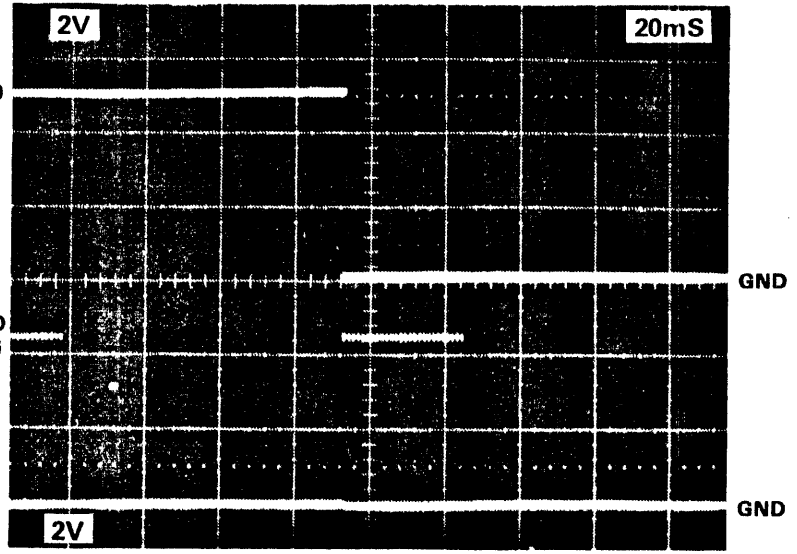
SHEET 1/2


5V
50µs
OE
GND
CE
GND
5V

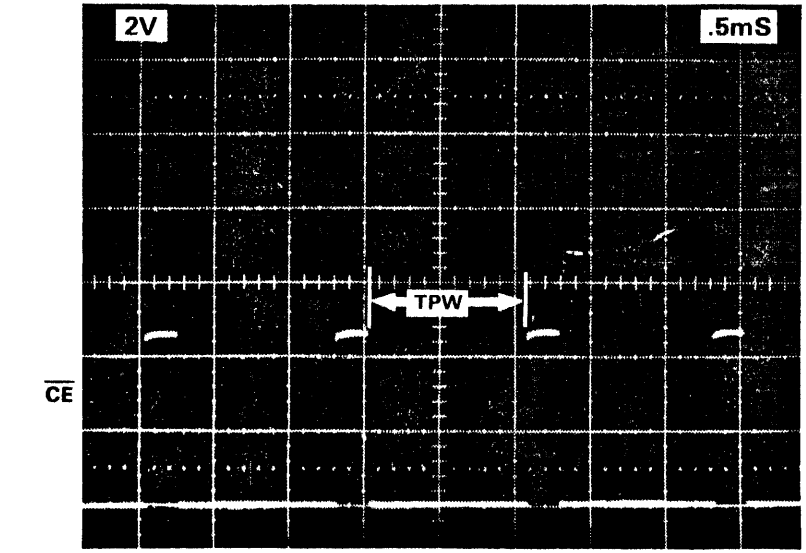
5


5V
50µs
OE
GND
BIT TO PROG
TOES
GND
5V

6


2V
20mS
A0
GND
BIT TO PROG
GND
2V

7


2V
.5mS
TPW
CE
GND

8

4-173
10-950-0099

REVISIONS

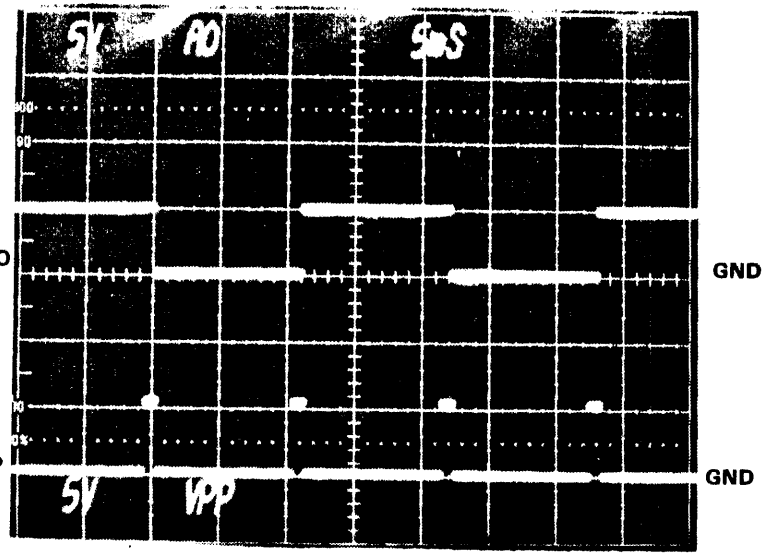
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		[illegible]	5/17/83

DATA I/O ISSAQUAH, WA

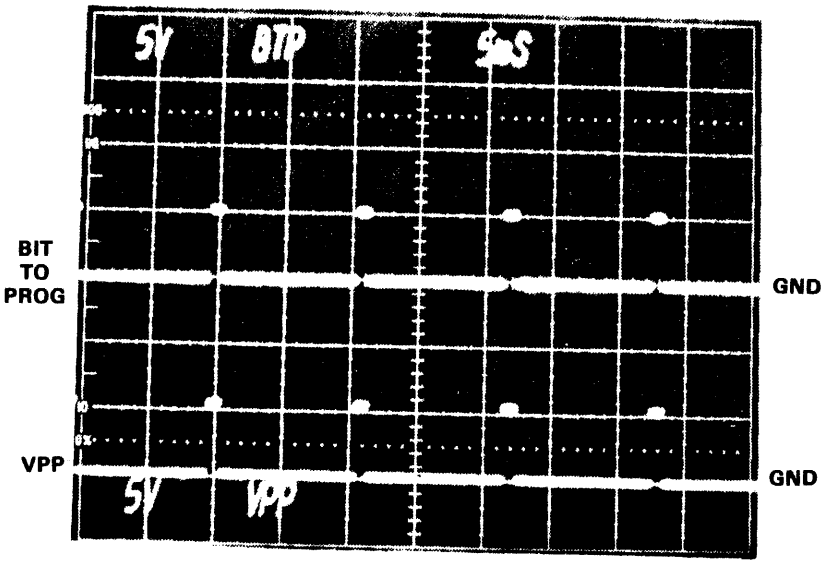
TITLE: TIMING DIAGRAM FAMILY CODES 93, 94	DRAWN BY: CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

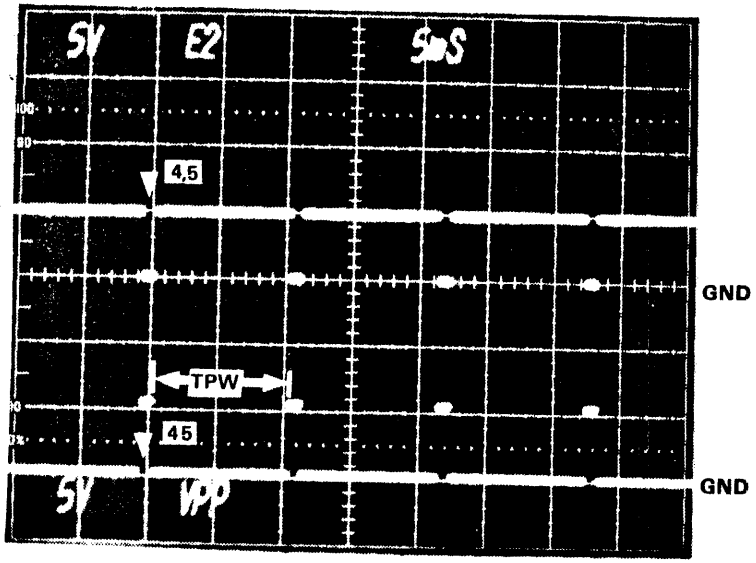
SCALE | SHEET 2/2


5V
AO
5mS
AO
GND
VPP
GND
5V
VPP

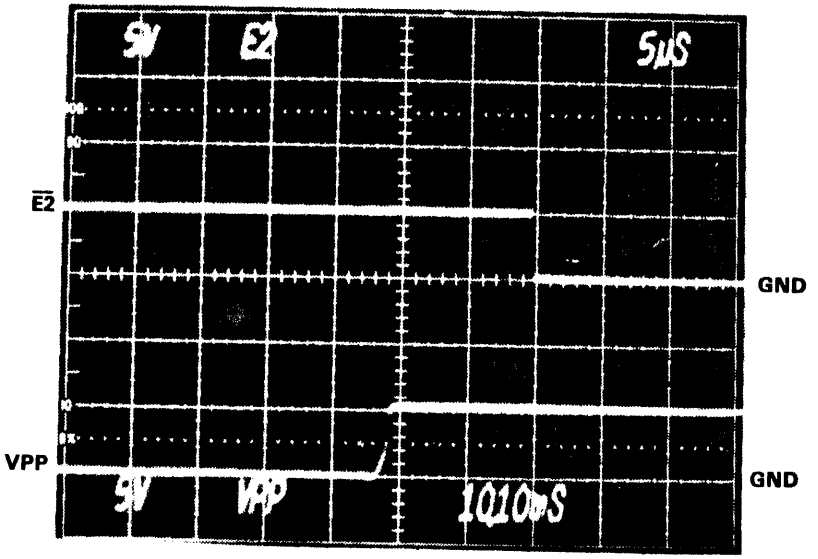
1


5V
BTP
5mS
BIT
TO
PROG
GND
VPP
GND
5V
VPP

3


5V
E2
5mS
4.5
E2
GND
TPW
4.5
VPP
GND
5V
VPP

2


5V
E2
5µS
E2
GND
VPP
GND
5V
VPP
1010mS

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card, 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-4, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	
	VOE	12.0	12.0	22.0	V	
	TPW	5	10	15	ms	
	Reject		1		Pulses	
	Overprogram		0		Pulses	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES A5, A6

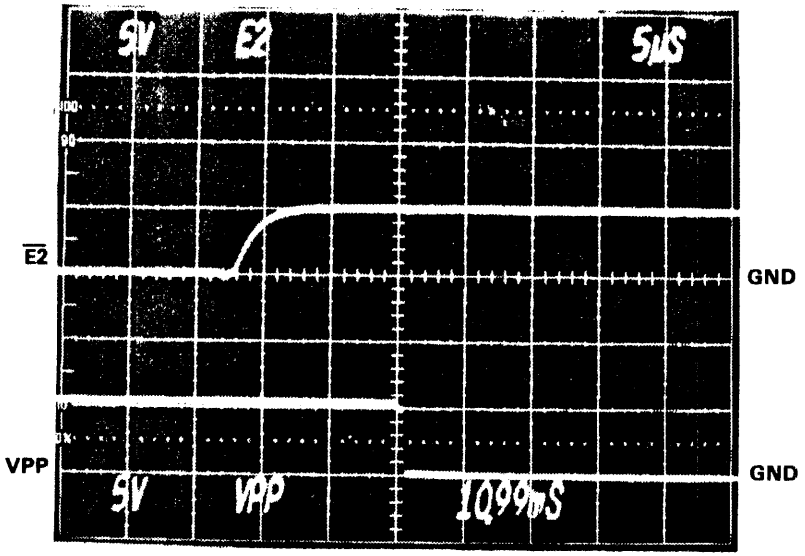
DRAWN BY: BG./PP

CHECKED BY: XH

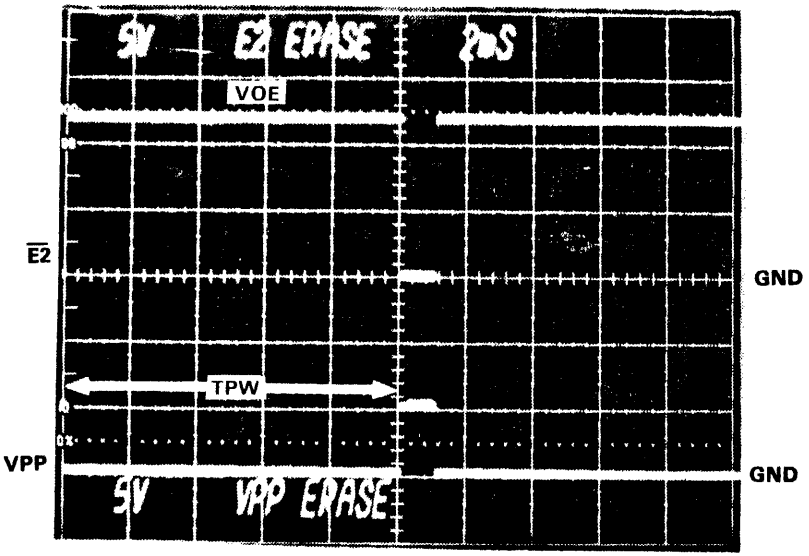
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5



6

(Erase Cycle)

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4728		XH	11/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES A5, A6

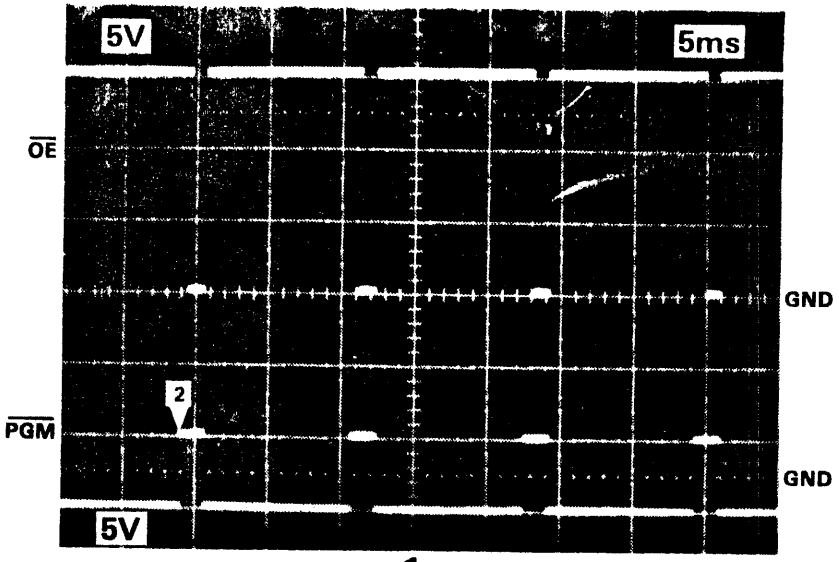
DRAWN BY: BG / PP

CHECKED BY: XH

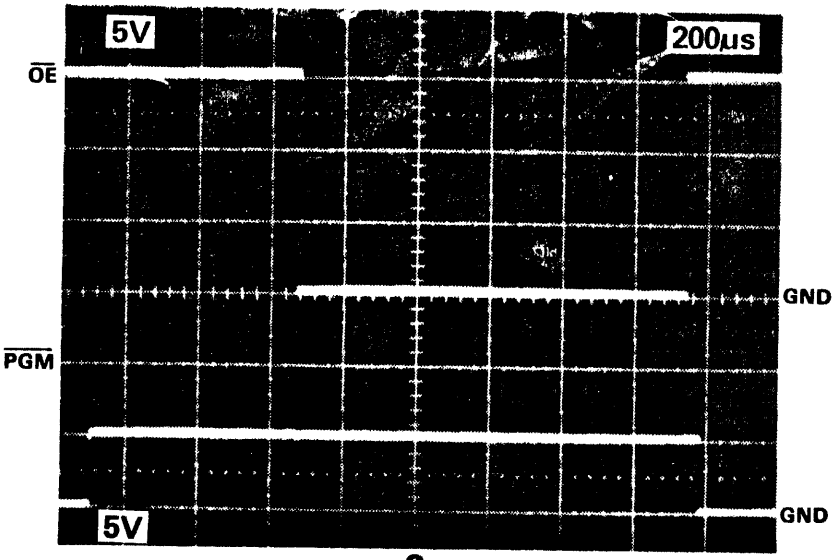
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

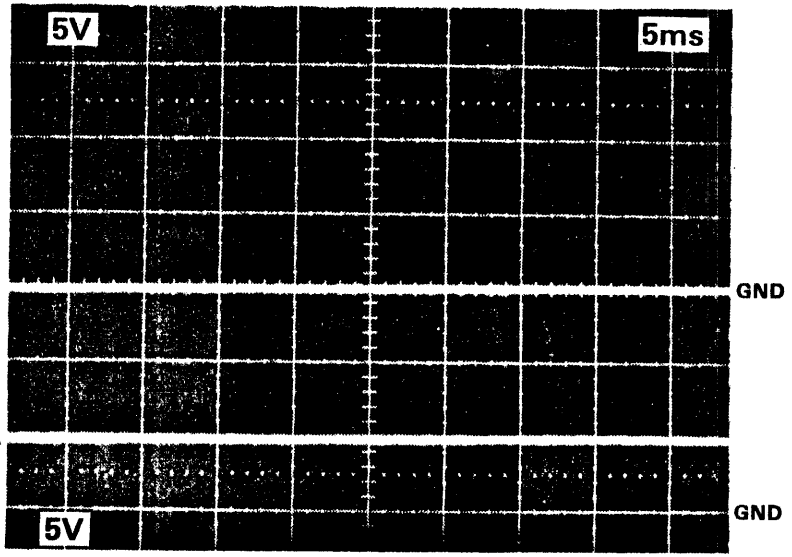
SHEET 2/2


5V
5ms
OE
GND
2
PGM
GND
5V

1


5V
200µs
OE
GND
PGM
GND
5V

2


5V
5ms
CE
GND
DATA
GND
5V

3

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
5. *Family AB/AC cannot be chip erased by UniPak™. Erasure of the whole device is performed on a byte-to-byte basis.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		TD	5/17/85

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES A5, A6
CHIP ERASE

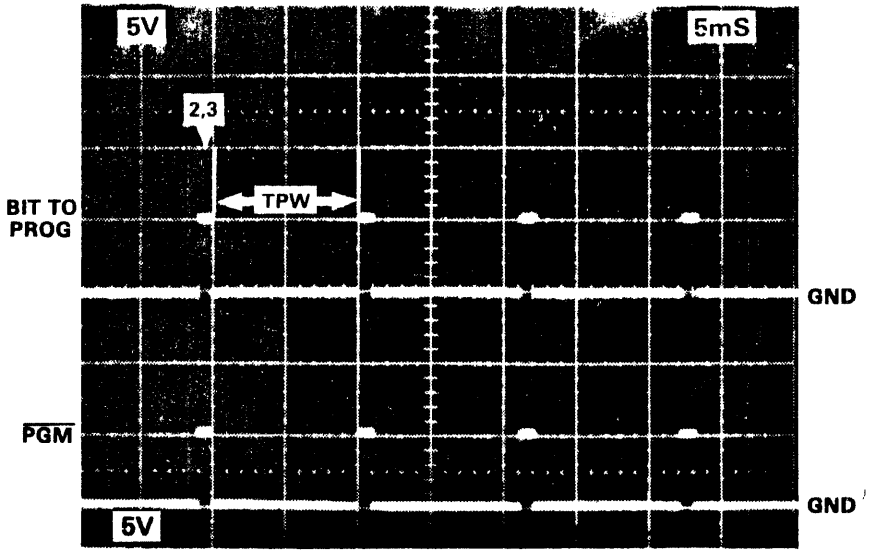
DRAWN BY:

CHECKED BY:

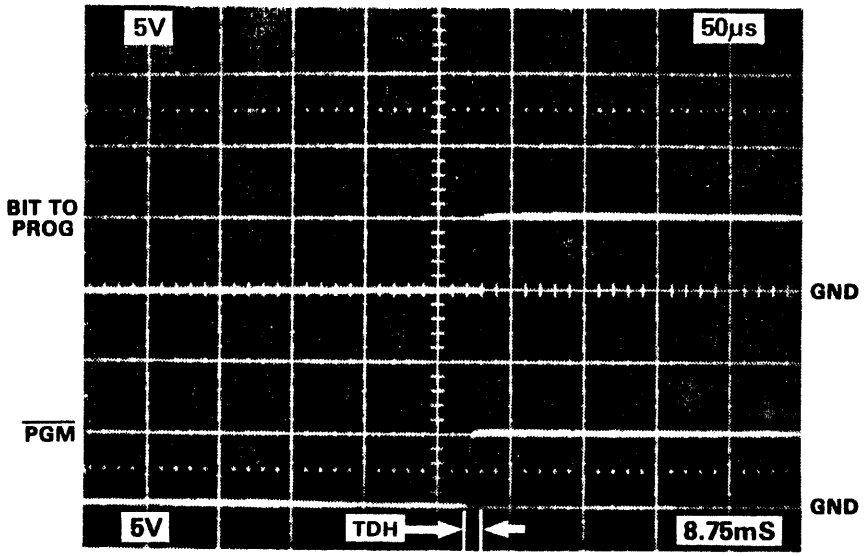
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

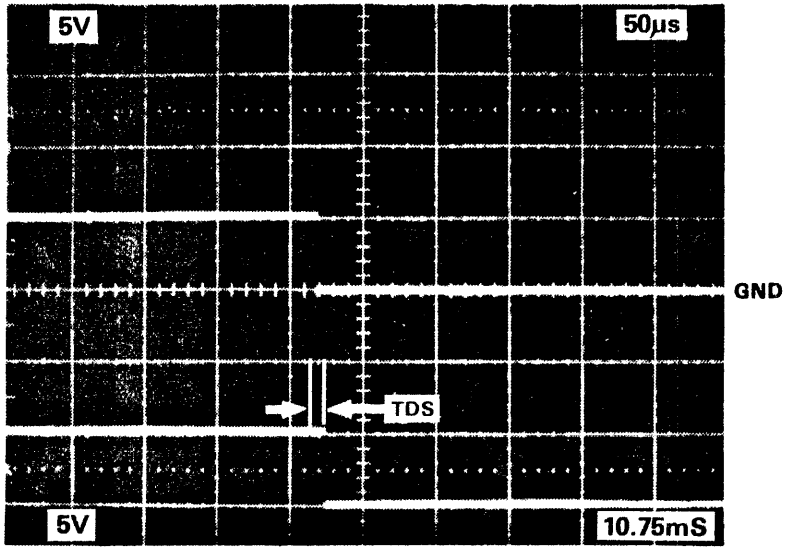
SHEET


5V
5mS
2,3
TPW
BIT TO PROG
GND
PGM
GND
5V

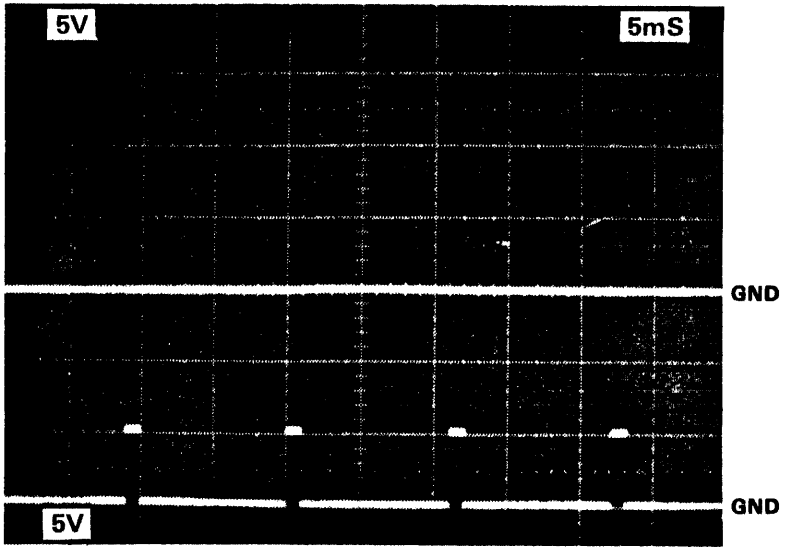
1


5V
50µs
BIT TO PROG
GND
PGM
GND
5V
TDH
8.75mS

2


5V
50µs
BIT TO PROG
GND
PGM
TDS
5V
10.75mS

3


5V
5mS
CE
GND
PGM
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the 0_4 contact for a 4-bit PROM or 0_3 for an 8-bit PROM. To observe a no-bit-to-program, use 0_3 for a 4-bit PROM or 0_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *The byte-erase waveforms look identical to the byte-write waveforms except that the data programmed are $FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
TPW	5	10	15	ms	
TDS	0				
TDH	50			ns	
TAS	150			ns	
TDS	0				
TDH	50			ns	
Reject		1		PULSES	
Overprogram		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		BJ	3/17/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES AB/AC
A5/A6

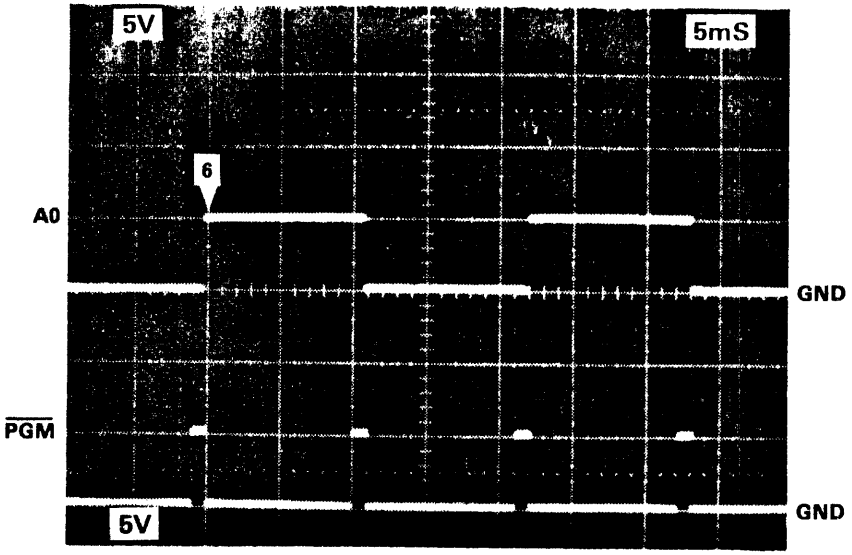
DRAWN BY:

CHECKED BY:

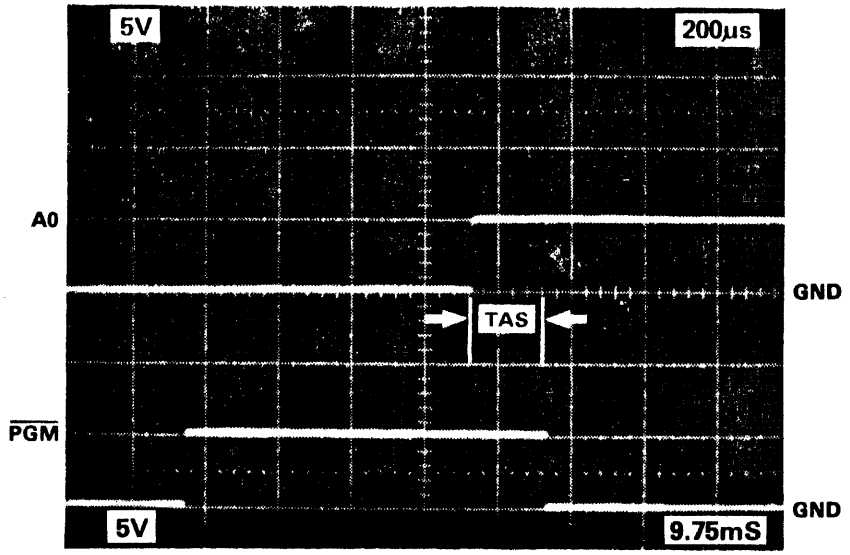
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2



5



6

4-183
10-950-0099

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES AB/AC
A5/A6

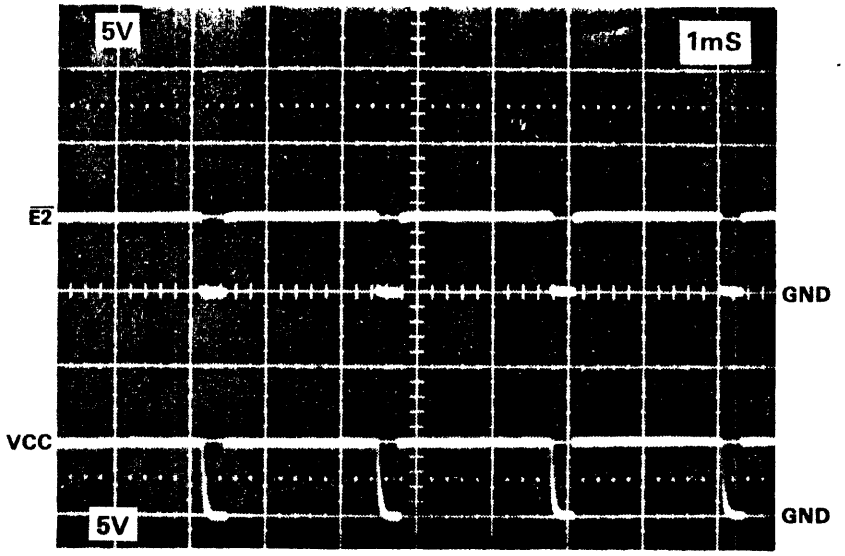
DRAWN BY:

CHECKED BY:

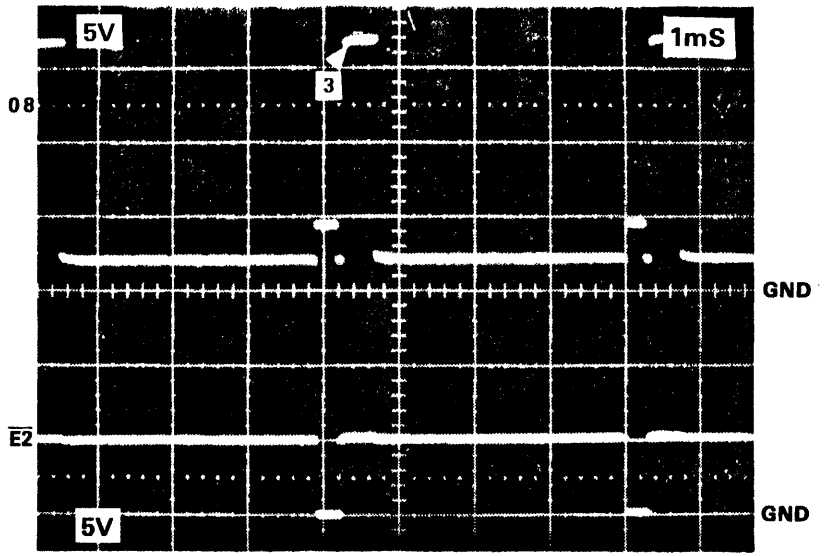
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

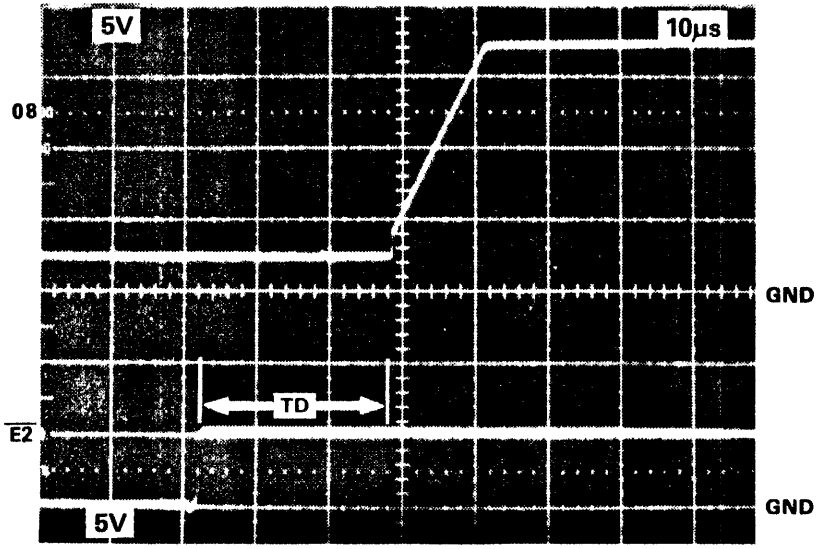
SHEET 2/2


5V
1mS
E2
GND
VCC
5V
GND

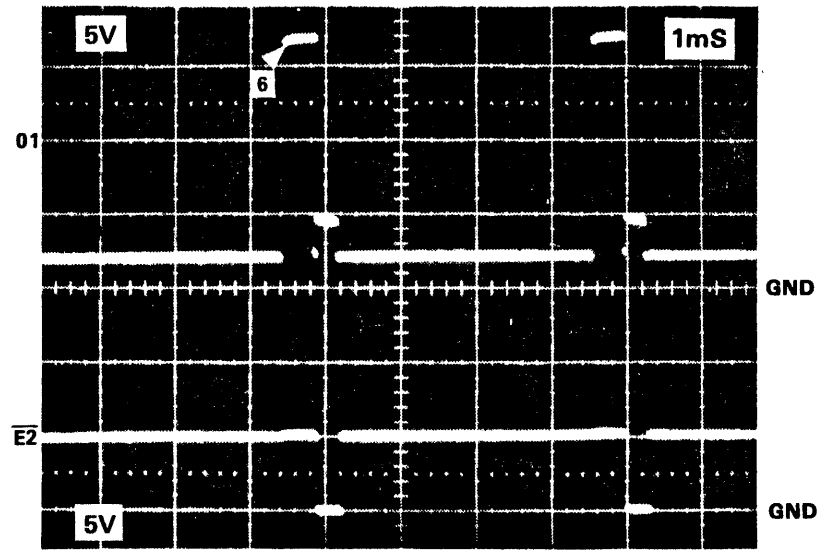
1


5V
1mS
3
08
GND
E2
5V
GND

2


5V
10µs
08
GND
TD
E2
5V
GND

3


5V
1mS
6
01
GND
E2
5V
GND

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
5. *Data = $FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VCC	4.75	5.0	5.25	V	
VOUT	16.0	17.0	18.0	V	
TPW	.3	.4	.5	ms	
TD	10			µs	
TR	10		50	µs	
REJECT		1		PULSES	
OVERPROGRAM		0		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

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10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		BS	5/12/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES AD, AE

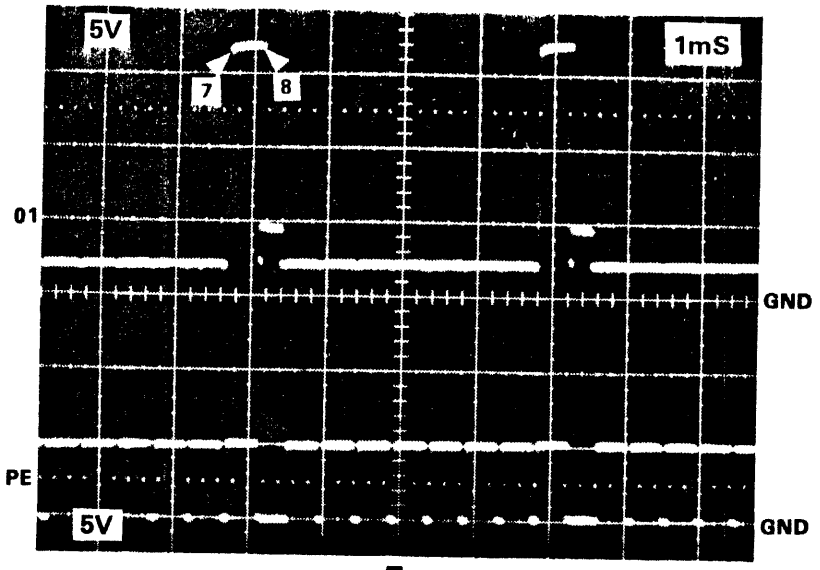
DRAWN BY:

CHECKED BY:

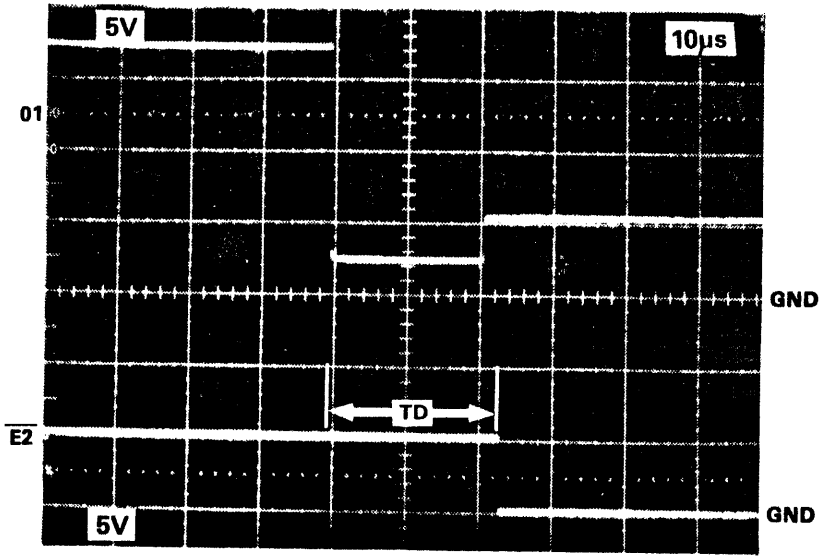
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

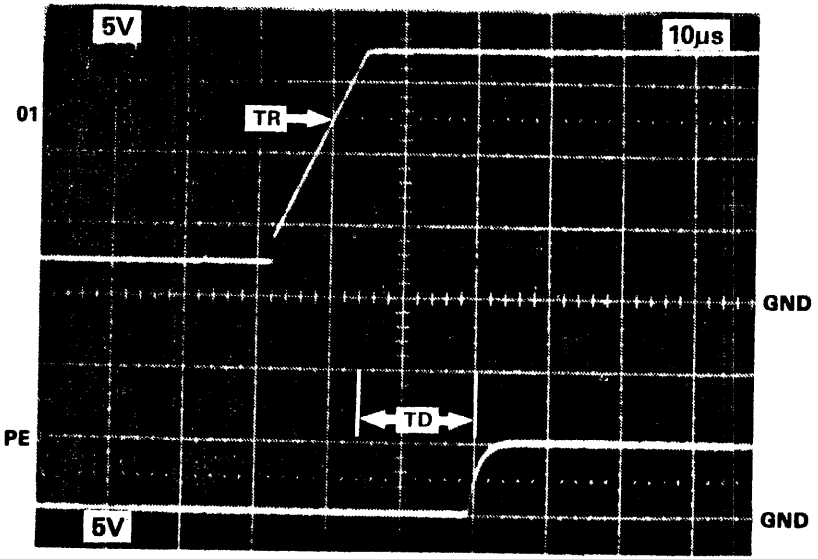
SHEET 1/2


5V
1mS
7
8
01
GND
PE
5V
GND

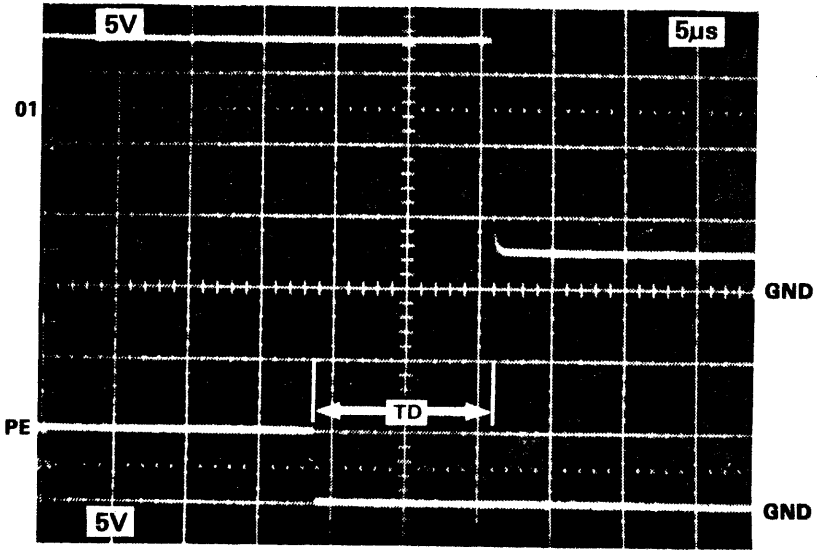
5


5V
10µs
01
GND
TD
E2
5V
GND

6


5V
10µs
01
TR
GND
TD
PE
5V
GND

7


5V
5µs
01
GND
TD
PE
5V
GND

8

4-187
10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES AD, AE

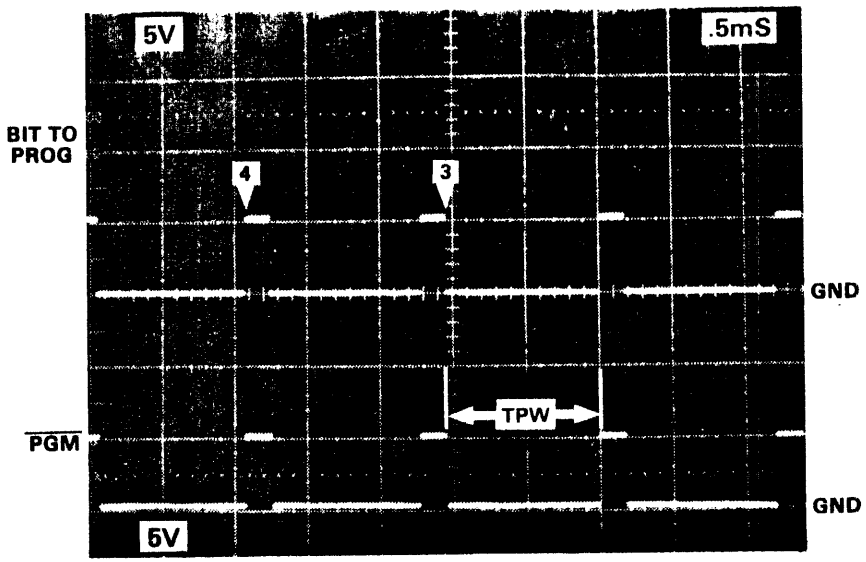
DRAWN BY:

CHECKED BY:

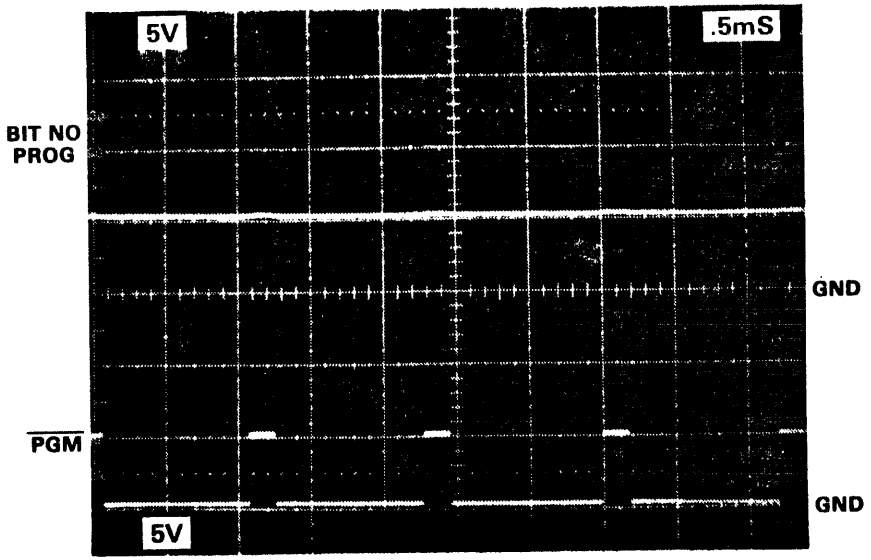
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

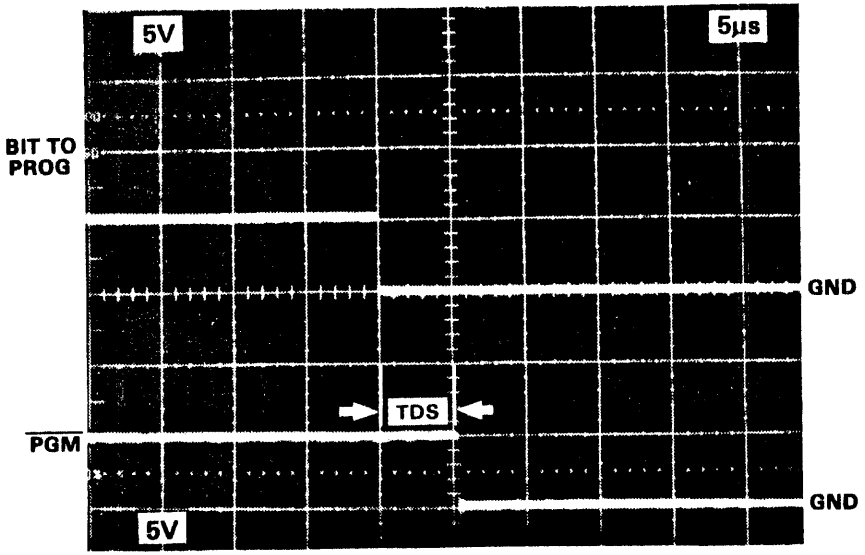
SHEET 2/2


5V
.5mS
BIT TO PROG
4
3
GND
TPW
PGM
GND
5V

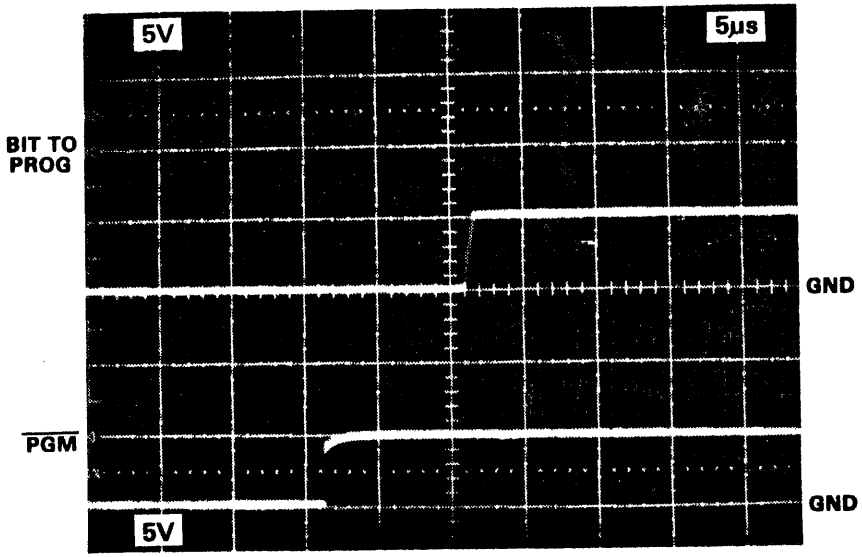
1


5V
.5mS
BIT NO PROG
GND
PGM
GND
5V

2


5V
5µs
BIT TO PROG
GND
TDS
PGM
GND
5V

3


5V
5µs
BIT TO PROG
GND
PGM
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *▼ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*
6. *Overprogram pulses can only be seen after 40 program pulses have been applied to each address; i.e., after address $0FFF has been programmed.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VCC		6.0		V	
VPP	21.0	21.5	22.0	V	Not Shown
TPW		1.0		ms	
TDS	2.0			µs	
TOES	2.0			µs	
OVERPROGRAM					
VCC		5.0		V	
VPP	21.0	21.5	22.0	V	
TPW		4.0		ms	
TDS	2.0			µs	
TOES	2.0			µs	
REJECT		40		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1998/TP4
High Load					701-1998/TP2
Low Load					701-1998/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			5/17/

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES AF, B0

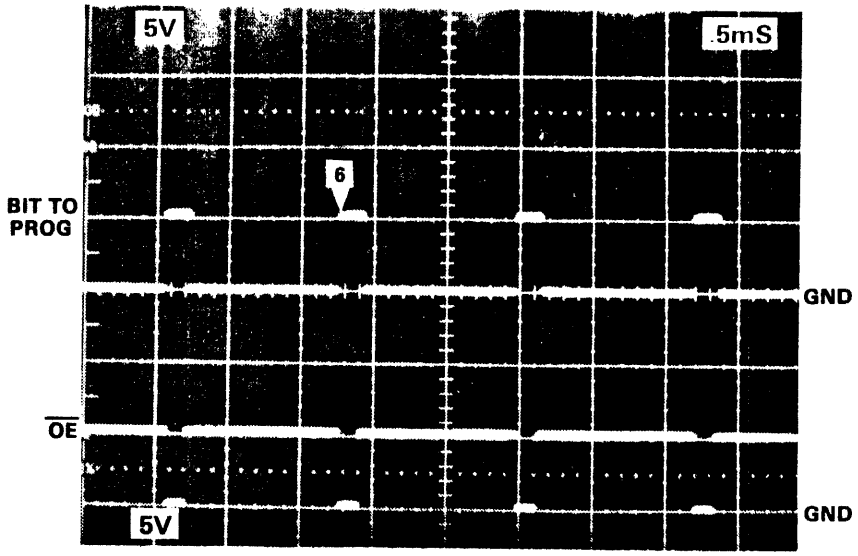
DRAWN BY:

CHECKED BY:

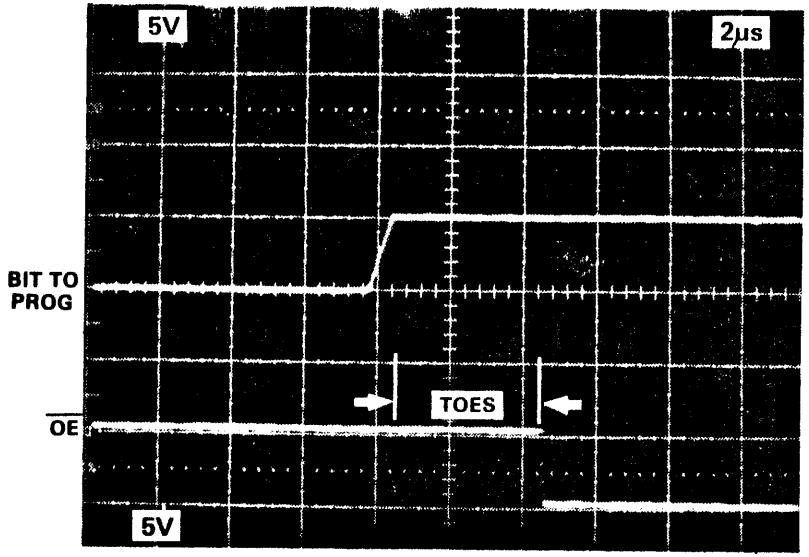
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

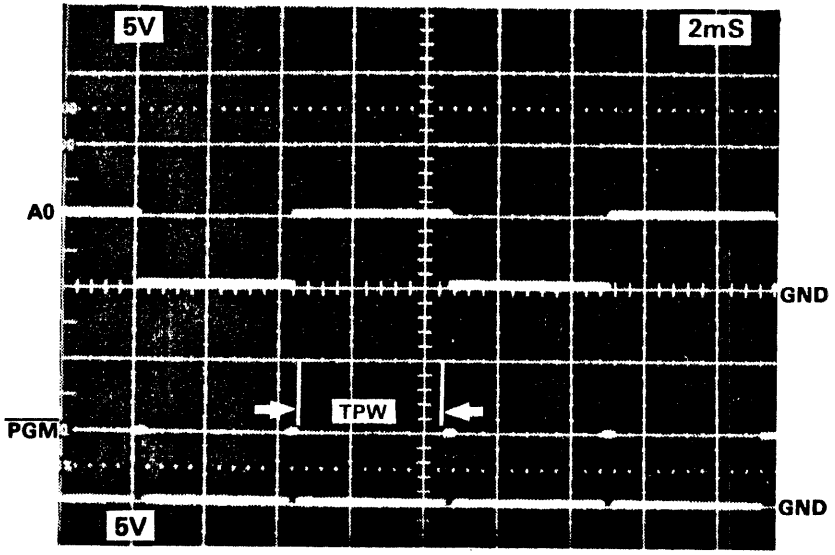
SHEET 1/2



5

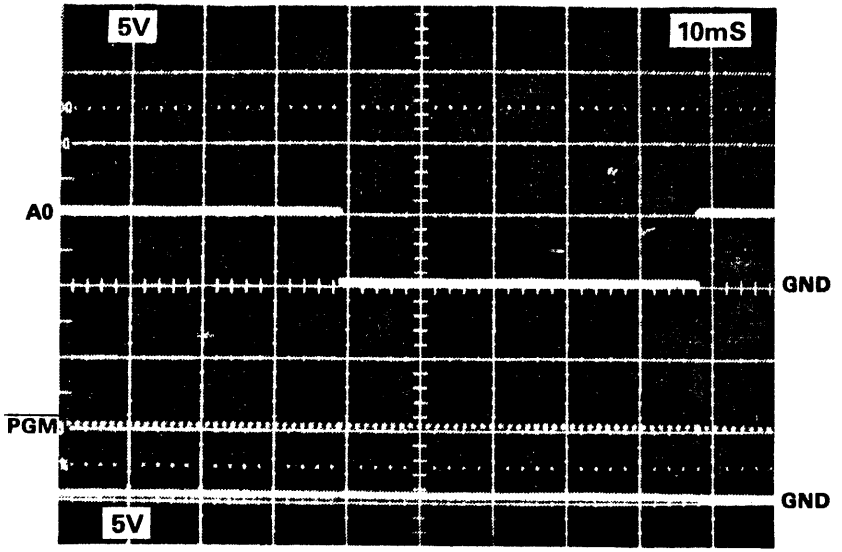


6



7

(OVERPROGRAM PULSES)



8

(PROGRAM PULSES)

PULSES)

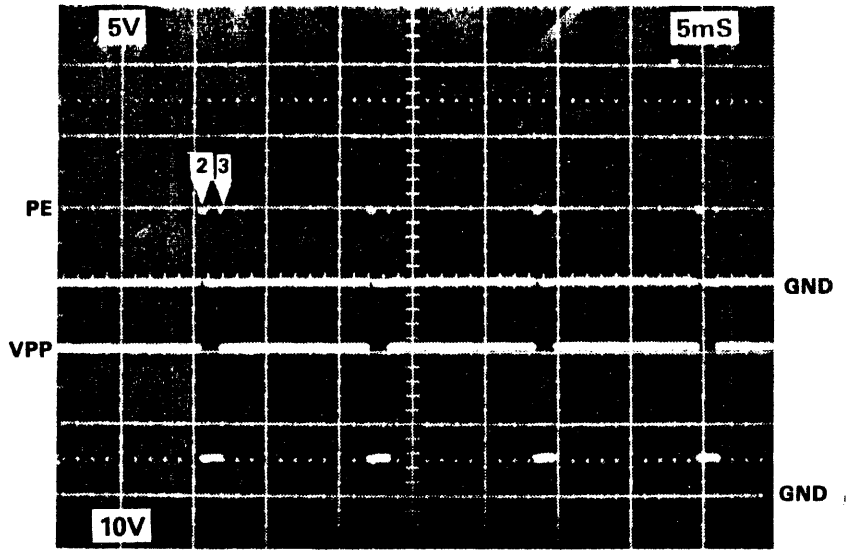
PULSES)

4-191
10-950-0099

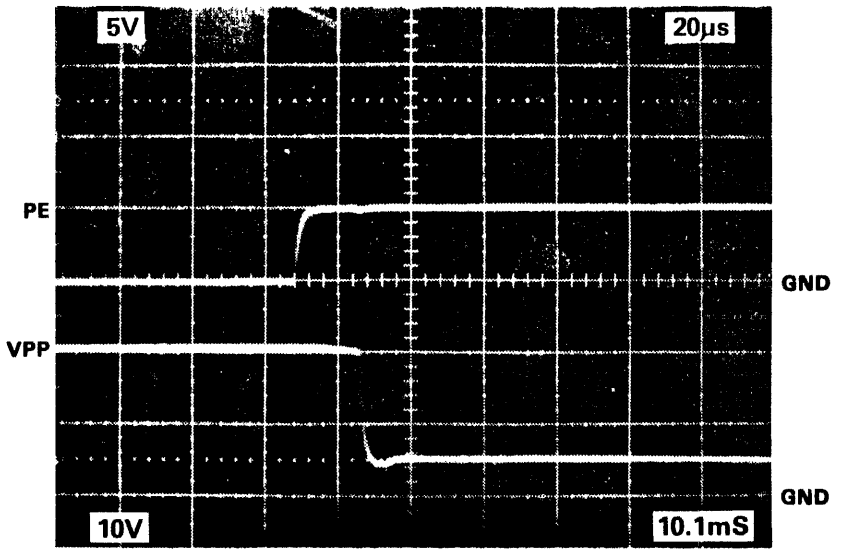
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

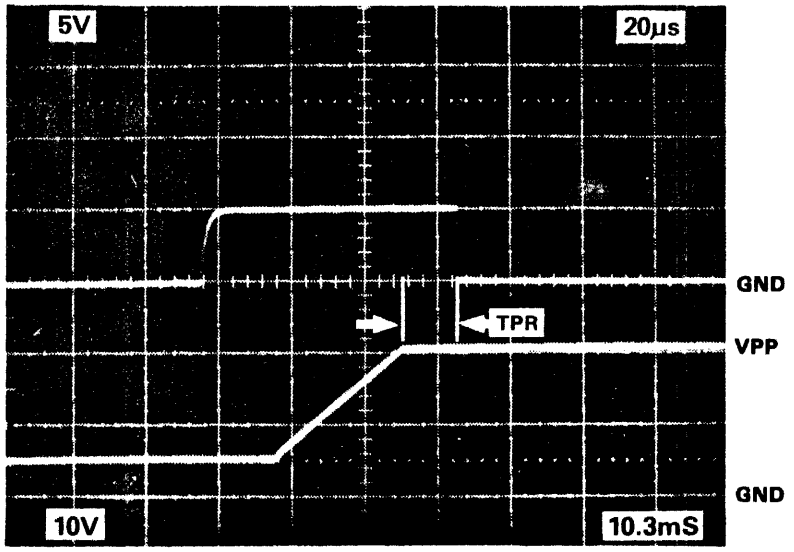
TITLE: TIMING DIAGRAM FAMILY CODES AF, BØ		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE:		SHEET 2/2


5V
5mS
2
3
PE
GND
VPP
GND
10V

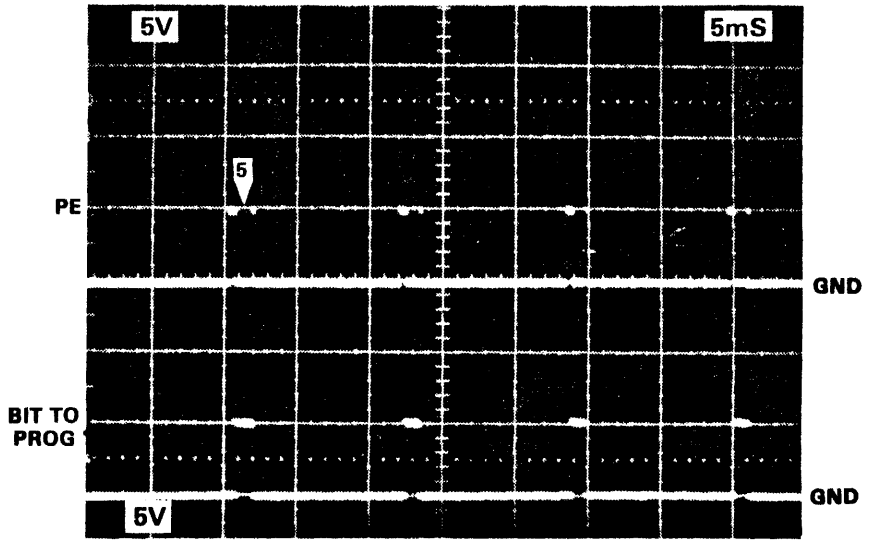
1


5V
20µs
PE
GND
VPP
GND
10V
10.1mS

2


5V
20µs
PE
GND
TPR
VPP
VPP
GND
10V
10.3mS

3


5V
5mS
5
PE
GND
BIT TO
PROG
GND
5V

4

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *The Pinout Charts, Figure 4-5, indicate which socket contact to probe to observe each waveform. Refer to the charts by Pinout Code. To observe a bit-to-program waveform, use the O_4 contact for a 4-bit PROM or O_3 for an 8-bit PROM. To observe a no-bit-to-program, use O_3 for a 4-bit PROM or O_1 for an 8-bit PROM.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM					
VPP	20		22	V	
TWP	9	10	15	ms	
TPR	0				
TDS	0				
VOE	9		15	V	
REJECT		1		PULSES	
OVERPROGRAM		1		PULSES	
1ST PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3
2ND PASS					
VERIFY					
VCC					
VREF					701-1655/TP2
High Load					701-1655/TP4
Low Load					701-1655/TP3

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		BS	5/17/85

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES B3, B4

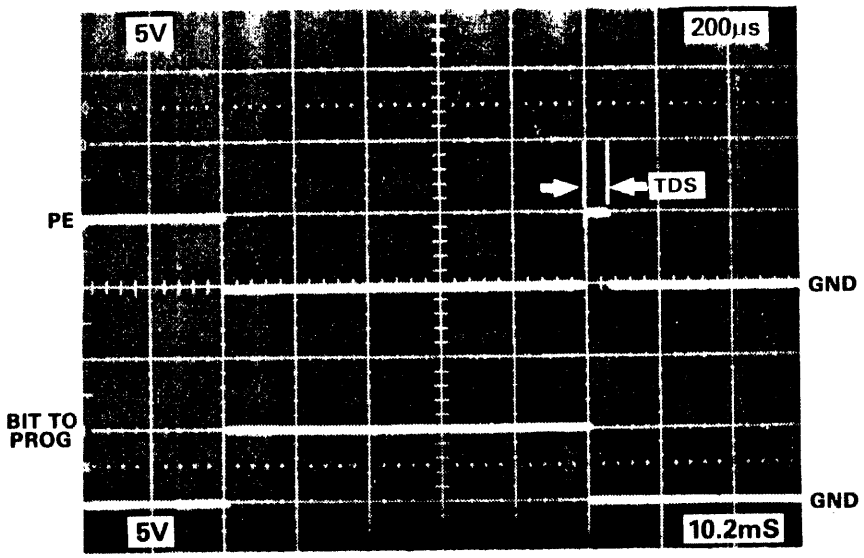
DRAWN BY:

CHECKED BY:

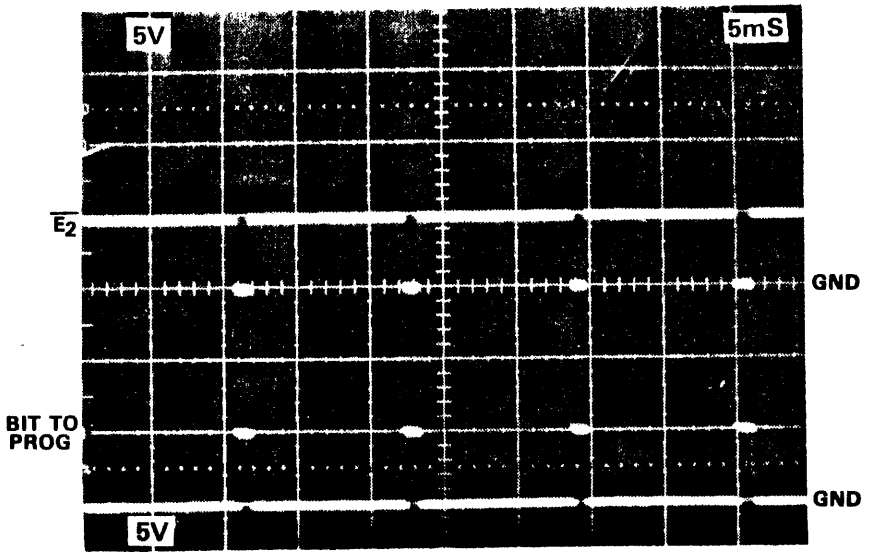
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

SHEET 1/2


5V
200µs
TDS
PE
GND
BIT TO PROG
GND
5V
10.2mS

5


5V
5mS
$\overline{E_2}$
GND
BIT TO PROG
GND
5V

6

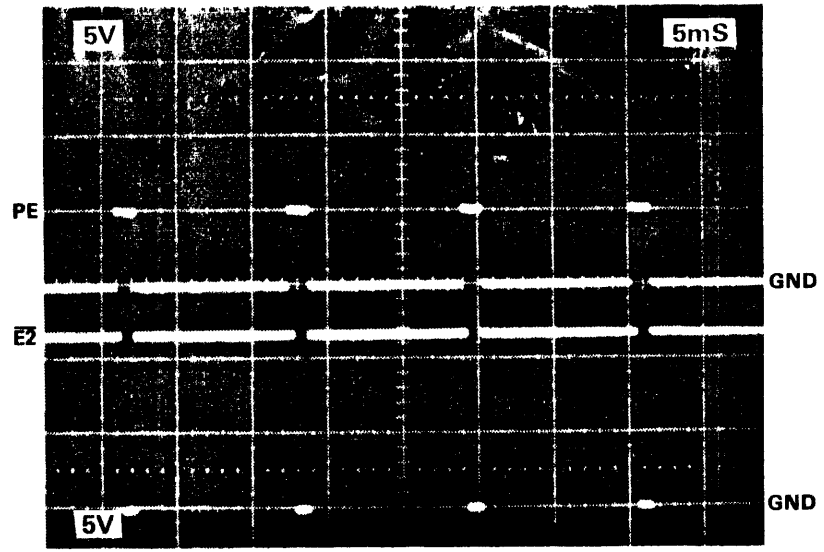
4-195
10-950-0099

REVISIONS

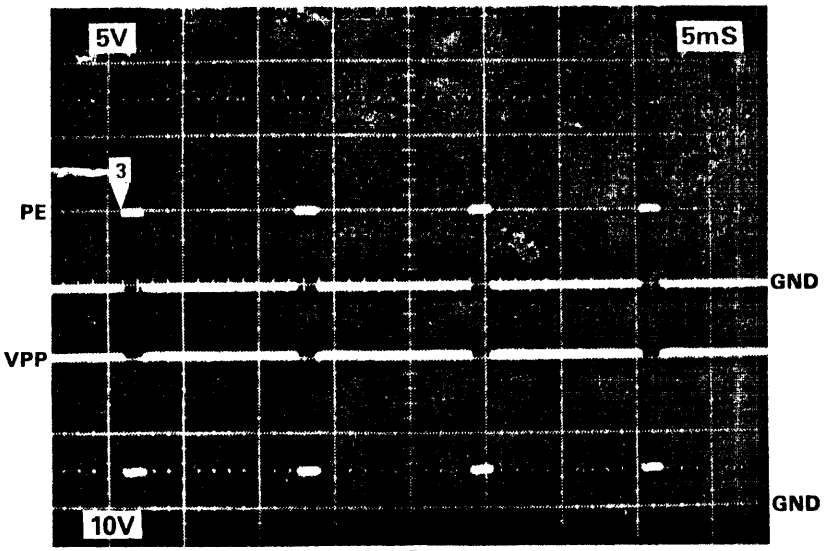
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803			

DATA I/O ISSAQUAH, WA

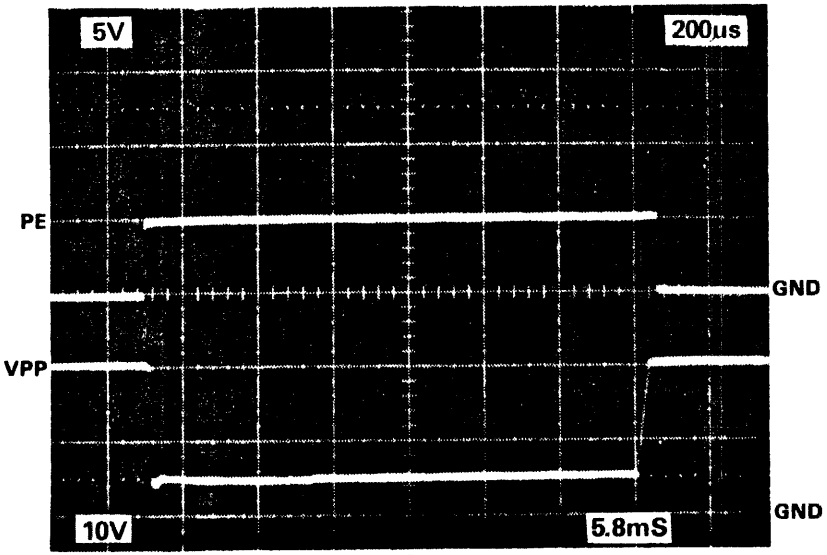
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE:		SHEET 2/2


5V
5mS
PE
GND
E2
GND
5V

1


5V
5mS
3
PE
GND
VPP
GND
10V

2


5V
200µs
PE
GND
VPP
GND
10V
5.8mS

3

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

10-950-0099

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		[illegible]	5/17/83

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES B3, B4
CHIP ERASE

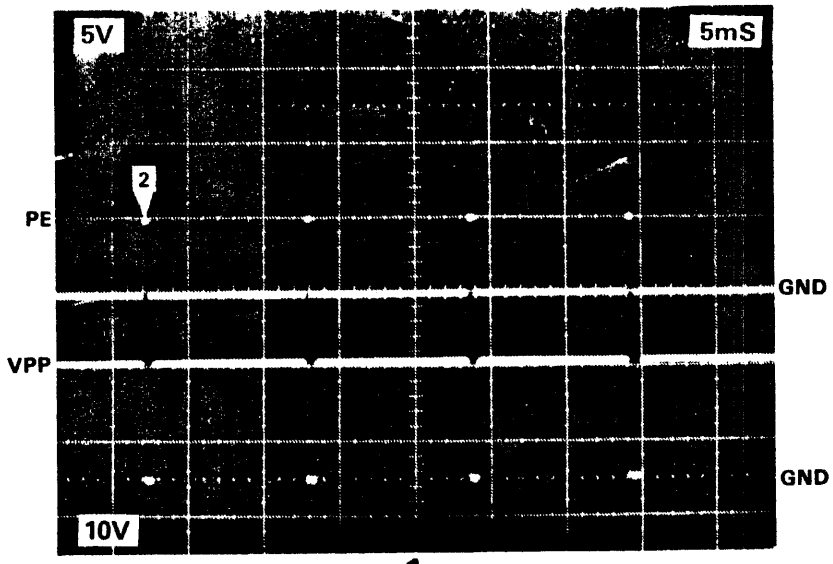
DRAWN BY:

CHECKED BY:

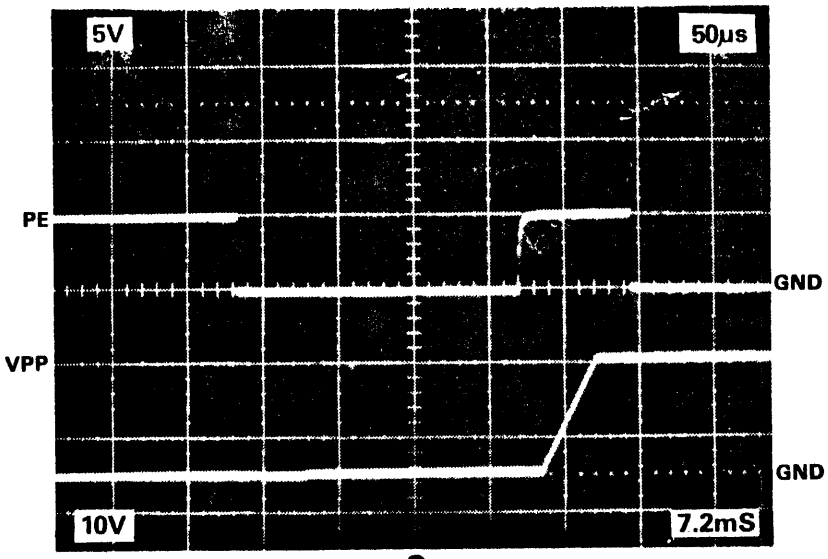
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0099

SCALE

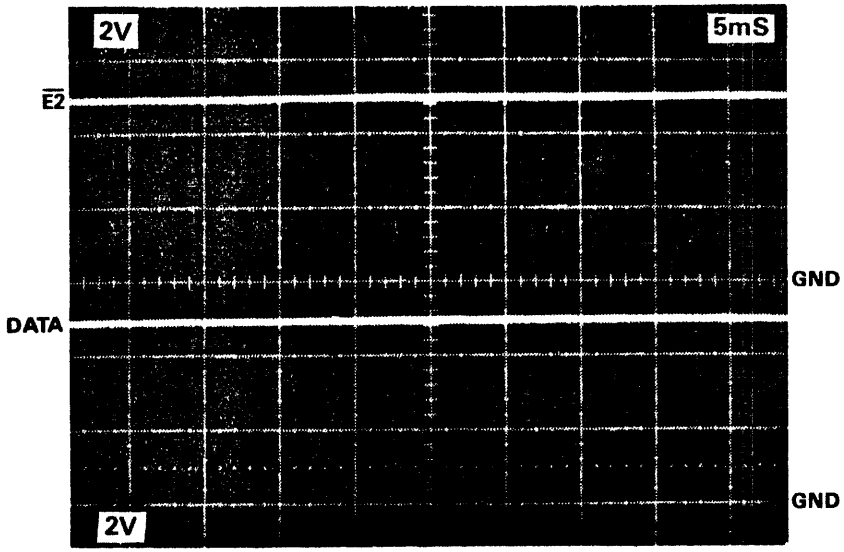
SHEET


5V
5mS
2
PE
GND
VPP
GND
10V

1


5V
50µs
PE
GND
VPP
GND
10V
7.2mS

2


2V
5mS
$\overline{E2}$
GND
DATA
GND
2V

3

NOTES

1. *Oscilloscope trigger point: TP1 on the Address Card 701-1998. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact on the socket with its LED illuminated.*
3. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
4. ▼ *with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	C	ECN #4803		[illegible]	5/17/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES B3, B4 BYTE ERASE	DRAWN BY:	
	CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE		SHEET

SECTION 5
MAINTENANCE

5.1 CLEANING

Inspect the UniPak regularly, inside and out, for accumulated dirt or dust. Dust on the circuit boards is most easily removed with a blast of compressed air. Dust and dirt can be wiped off the outside with a damp cloth. Do not use any abrasive cleaners!

5.2 INSPECTION

Periodic inspection of the UniPak can be a hedge against malfunction. A good time to schedule an inspection is before every calibration. Check cable connections, card seating, mounting of discrete components, etc., for shorts, opens or unstable continuity.

Particular care is required if heat-damaged components are found. It is important to find and correct the cause of overheating in order to prevent further damage.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

The following information is an aid to interpreting malfunctions and locating hardware failures in the UniPak. System failures can be divided into two categories:

- No system operation
- Persistent or intermittent test-stage errors (or poor yields)

These categories, covered in paragraphs 6.2 and 6.3, will direct the service technician to the portion of the circuitry implicated by test errors or unacceptable calibration results. Table 6-1 can be used to isolate the problem to a suspect board or component. Section 7, Circuit Description, and Section 8, Schematics, provide additional information useful in troubleshooting.

After successful troubleshooting, calibrate the UniPak, as described in Section 4.

6.2 NO SYSTEM OPERATION

Perform the following steps if the system will not operate after installation of the UniPak. After completing each step, determine whether the problem still exists.

1. Check for proper installation of the UniPak (refer to Section 2).
2. Check all cables for proper insertion and orientation. Check the UniPak-to-programmer connector for bent pins.
3. Check power supplies.
4. If steps 1 through 3 do not reveal the problem, contact your local Data I/O Service Center.

6.3 PERSISTENT OR INTERMITTENT TEST-STAGE ERRORS

Perform the following steps to isolate a system failure. After completing each step, determine whether the problem still exists.

1. Check that the Family and Pinout Codes are correct for the device being programmed and that the device is inserted in the proper socket. Refer to Section 3.
2. Substitute a good device to determine if a hardware problem exists.
3. Check for proper installation of the UniPak (refer to Section 2).
4. Check all cables for proper insertion and orientation. Check the UniPak-to-programmer connector for bent pins.
5. Perform a complete calibration. Note any voltages still falling outside the indicated limits, and then refer to the corresponding test number in Table 6-1 to locate the suspect board or component. Referring to the circuit description (Section 7) and the schematics (Section 8) may also prove helpful.
6. Perform waveform observation tests. Note any waveform irregularities. Referring to the circuit description (Section 7) and the Schematics (Section 8) may prove helpful in determining the cause of any irregularities.
7. Perform Measurement Chart Steps 15 and 16 for the device family presenting problems. (Refer to paragraph 4.3.4.)
8. If steps 1 through 7 do not reveal the problem, contact your local Data I/O Service Center.

Table 6-1. Troubleshooting Chart

TEST NUMBER	SUSPECT BOARDS	SUSPECT COMPONENTS
1	701-7997, 701-1998	
2	702-7995	DS2, U1
3	701-1998	U26, U13, CR1
4	701-7997	VR1, Q23, U6, U13
5	701-1998	U19, U13, Q3
6	701-1998	Q1, Q2, U14
7	701-7997	Q17, U8, U4, U11
	702-7995	U2, CR12
8	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
9	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
10	701-7997	Q1, Q4, Q2, Q20
11	701-7997	Q1, Q18, Q21
12	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-10, U16, U17
13	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-10, U16, U17
14	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-10, U16, U17
15	702-7995	DS4, U1
16	702-7995	U2, CR15
17	701-1998	Q4-10, U16, U17, U18
18	701-1998	Q4-10, U16, U17, U18
19	702-7995	DS5, U1
20	702-7995	U2, CR11
21	702-7995	DS6, U1
22	702-7995	U2, CR13
23	702-7995	DS7, U1
24	702-7995	U2, CR16
25	701-1998	RP1, RP2, U3-6
	702-7995	U9, U10, Q2
26	702-7995	DS3, U1
27	702-7995	U2, CR14
28	702-7995	DS1, U1
29	702-7995	U1, CR8
30	701-1998	RP1, RP2, U3-6
	702-7995	U9, U10, Q2
31	701-7997	U1, CR8, U6, Q16, R39
32	701-1998	U26
33	701-1998	U19
34	701-7997	U11
35	701-7997	U10
36	701-7997	U9
37	701-7997	Q15, U4, Q21
38	701-7997	U2, Q20
39	701-7997	U2, Q6, Q22
40	701-7997	U11
41	701-7997	U10
42	701-7997	U9
43	701-7997	Q6, Q12, CR7, Q22
44	701-1998	U26
45	701-1998	U19
46	701-7997	VR2, U7
47	701-1998	U1, U2, U12, Q12-19
48	701-1998	U1, U2, U12, Q12-19
49	701-1998	U1, U2, U12, Q12-19
50	701-1998	U1, U2, U12, Q12-19
51-58	702-7995	Q1, RP1, U3, CR17

SECTION 7
CIRCUIT DESCRIPTION

7.1 INTRODUCTION

This section defines the functions of the UniPak's principle hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

7.2 GENERAL ARCHITECTURE

7.2.1 THE LINK BETWEEN THE UniPak AND THE PROGRAMMER

The UniPak is controlled by the programmer's extended processor bus (J6), through the UniPak's mating connector. Pin functions of the extended processor bus are shown in Table 7-1.

The control software for the UniPak is located in PROM on the Memory Card (702-0045).

7.2.2 THE BUSES

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the Memory Card and control the gates and registers on the Waveform Generator (701-7997) and Address and Data Driver (701-1998) Cards. The UniPak's device bus gathers the programming waveforms produced by these cards and transmits them to the Socket Card (702-7995). Figure 7-1 shows the relationship among the buses.

Table 7-1. Pin Functions, Programmer's Extended Processor Bus (at J1-J3)

Pin	Function	Pin	Function
1	A_0	A	A_5
2	A_1	B	A_6
3	A_2	C	A_7
4	A_3	D	A_8
5	A_4	E	A_9
6	A_{10}	F	A_{11}
7	A_{12}	H	A_{13}
8	A_{14}	J	A_{15}
9	DO_1	K	DI_1
10	DO_2	L	DI_2
11	DO_3	M	DI_3
12	DO_4	N	DI_4
13	DO_5	P	DI_5
14	DO_6	R	DI_6
15	DO_7	S	DI_7
16	DO_8	T	DI_8
17	Ver. A	U	Ver. B
18	Start	V	Clk. Inh.
19	W/L	W	"26"
20	VOL/VOH	X	"36"
21	+5 V	Y	−9 V
22	+Prog.	Z	+24 V
23	GND	AA	−5 V
24	Sense	BB	Operate
25	+48 V	CC	Unreg. H.V.
26	GND	DD	Gnd.
27	C1	EE	C4
28	C2	FF	C5
29	C3	HH	C6
30	IRQ	JJ	Gate Enable
31	R/W	KK	Extend
32	V•Ø2	LL	+18 V Raw
33	Interlock	MM	PP
34	+10 V Raw	NN	RR
35	Write	PP	Read
36	Reset	RR	Fwd.

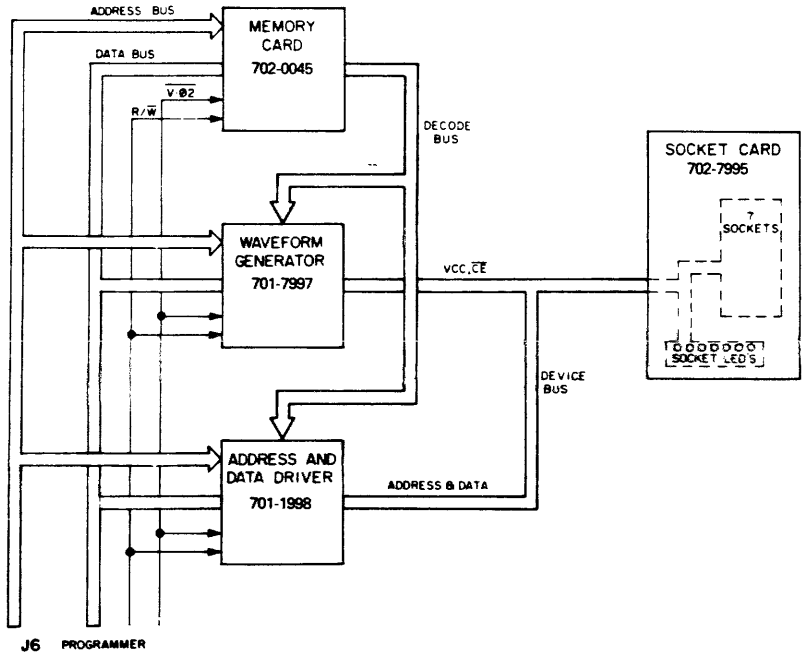


Figure 7-1. Block Diagram, UniPak Electronics

7.3 COMPONENT LAYOUT

Figure 7-2 shows the component layout of the UniPak. The principal components are described in paragraphs 7.3.1–7.3.5.

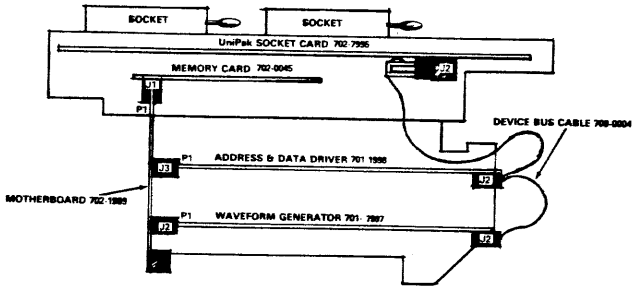


Figure 7-2. Principal Components of the UniPak

7.3.1 MOTHERBOARD

The motherboard accepts the signals and power supplies from J6 of the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector. See Figure 7-3 and schematic 008-1999.

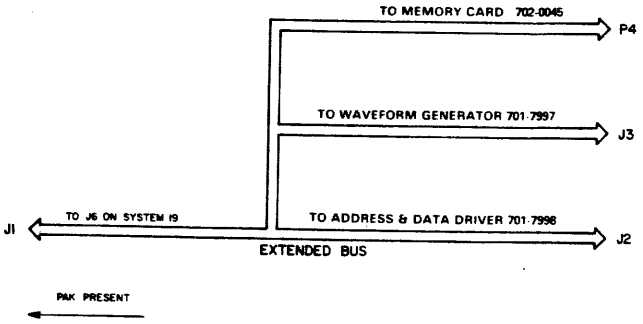


Figure 7-3. Block Diagram, UniPak Motherboard

7.3.2 WAVEFORM GENERATOR

The Waveform Generator provides all signals, including addresses and data, required for programming devices. These signals are generated by the blocks shown in Figure 7-4.

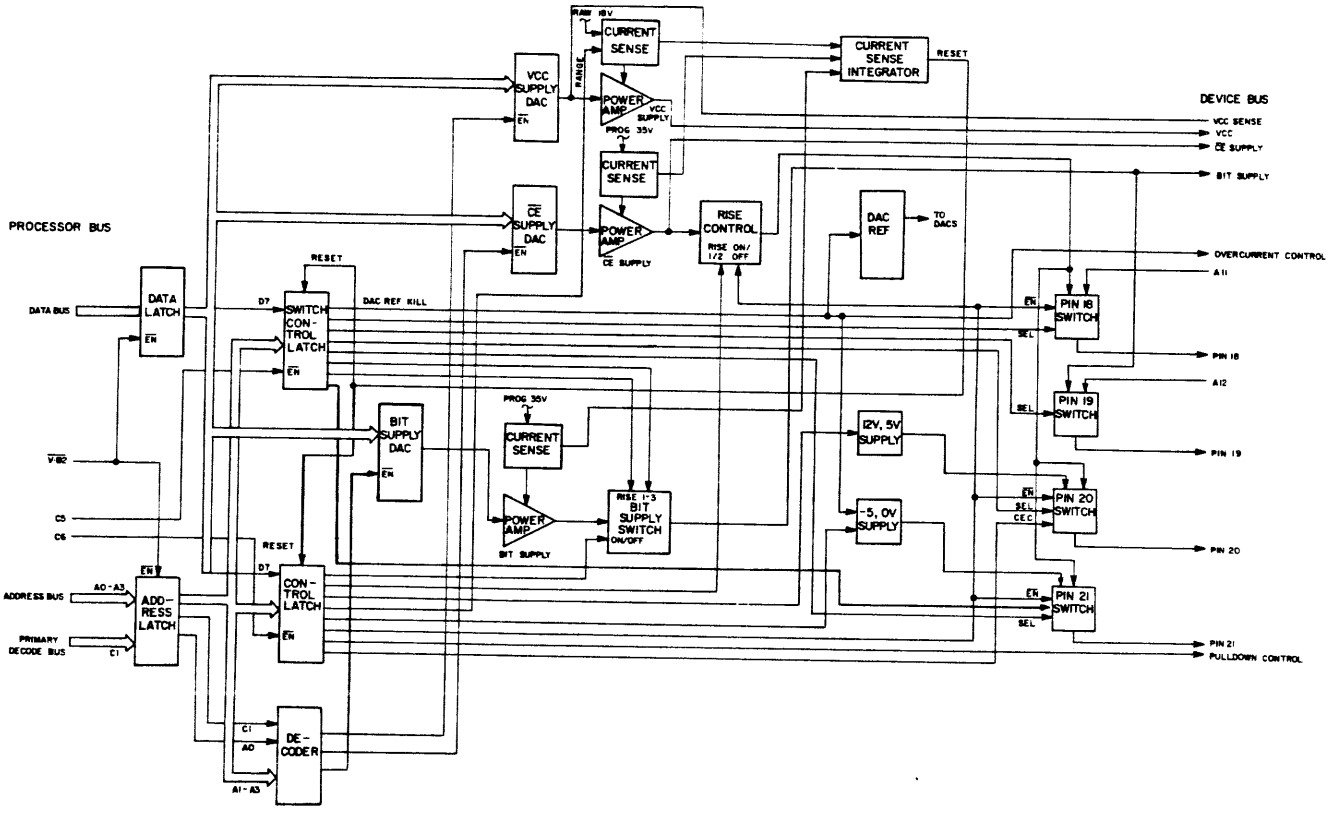


Figure 7-4. Block Diagram, Waveform Generator

Three major supplies are the Vcc Supply, the $\overline{CE}$ Supply and the Bit Supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All D/A converters obtain their reference voltage from the DAC Reference.

The Vcc waveforms are generated by writing appropriate DAC values from the software. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1 A). If a detector is activated, the control latch is reset; the DAC-Reference Kill output then causes the DAC Reference to go to zero, in turn causing all supplies to return to zero.

The Vcc Supply senses the Vcc voltage at the PROM socket via the Vcc-Sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ Supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the Control Latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the Switch-Control Latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ Supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$-supply level. An NPN-transistor pulldown is included in the switch to provide a 20 V/µs controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

The Pin 21 Switch uses the same principles as the Pin 18 and Pin 20 Switches. However, a power amplifier output (-5/0 supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5 V.

The Pin 20 Switch includes a pullup that is connected to the +12/+5 V Supply, thus allowing the switch in the TTL mode to switch from 0 to 12 V as well as from 0 to 5 V. The +12/+5 V Supply consists of a monolithic regulator and a 5.1 V zener diode controlled by the Switch-Control Latch.

Signals to be applied to the data lines of a device are generated with the Bit-Supply signals and controlled by the Bit-Supply Switch. The Bit Supply is nearly identical to the $\overline{CE}$ Supply but has one less diode in the feedback path compensating for one less drop in the switch paths. The Bit-Supply Switch consists of an emitter follower, a current source and three rise-time-control capacitors. The collector of the emitter follower is connected to the Bit Supply; the base is connected to the current source and timing capacitor. The Control Latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the Bit-Supply switch is sent to the Address and Data Driver Card and to the Pin 19 Switch.

Unlike the Pin 20, 21 and 18 Switches, the Pin 19 Switch consists of a simple PNP-saturating switch controlled by the Switch-Control Latch.

The Current-Sense Integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the Vcc, $\overline{CE}$, Bit or (0/-5 V) Supply exists for sufficient time, the Control Latch is reset, in turn causing the DAC Reference and the supplies to go to zero. The state of the Overcurrent-Control line can be read by the Address and Data Driver Card and used by the programmer to detect shorted devices. Table 7-2 gives the functions of the device-bus pins. The Data Latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The Address Latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the Decoder and the Address Latches. The Decoder provides decode signals to the DACs for the Vcc, $\overline{CE}$ and Bit Supplies. The Switch-Control Latch and the Control Latch receive their clocks from a decoder on the Address and Data Driver Card.

Table 7-2. Pin Functions, Device Bus (at J1)

1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	VCC
10	VCC Sense	35	GND
11	CE Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9	41	PD_2
17	+24	42	PD_3
18	Overcurrent	43	PD_4
19	Pull Down Control	44	S1
20	VCC Pull Up	45	S2
21	VREF	46	S3
22	PD_8	47	Spare
23	PD_7	48	Spare
24	PD_6	49	+5
25	PD_5	50	GND

7.3.3 ADDRESS AND DATA DRIVER

The Address and Data Driver, diagrammed in Figure 7-5, provides the device address, device data, data loads and supply measurement capability of the UniPak.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The Data-Switch Register drives PNP Data Switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant base drive at all bit-switch voltages.

The Data Sink Register drives the NPN Data Sinks directly. These data sinks are used to shunt to ground large programming currents. Device data is read via the Data Comparators and strobed to the processor bus via the Data Gate. The Comparators receive their reference voltage from

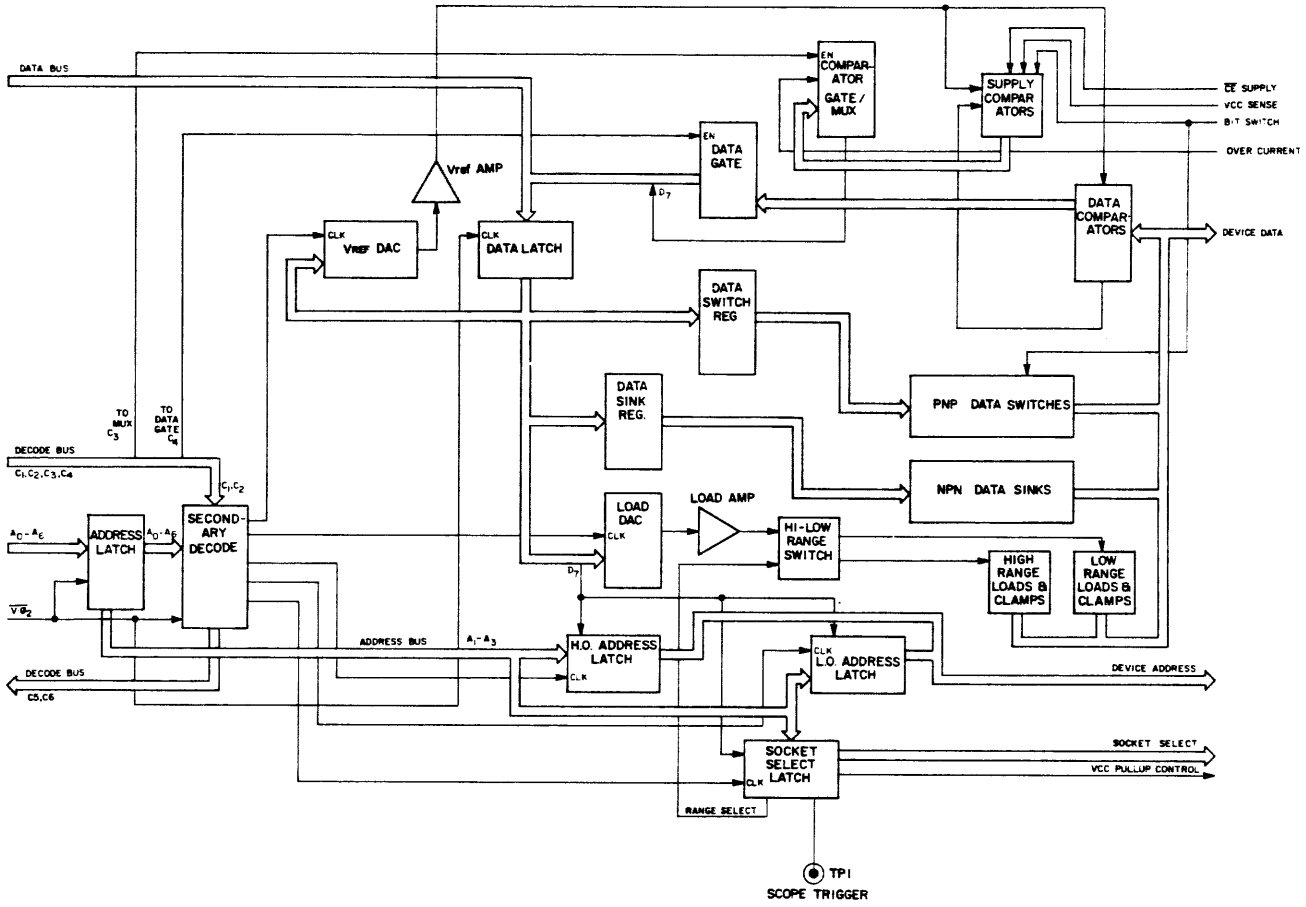


Figure 7-5. Block Diagram, Address and Data Driver Card

the VREF amplifier which is controlled by the VREF DAC. Loading of the device data bus can be controlled by the Load DAC, the Load Amplifier and the Hi/Low Range Switch. A voltage is developed by the Load Amp and applied to either the high-range or low-range resistor banks. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5 V.

The Supply Comparators read the Vcc-Sense line, the $\overline{CE}$ supply and the Bit-Switch line. The comparator Gate/Mux strobes the data from the Supply Comparators or Overcurrent-Read line to the most-significant-bit line of the data bus.

The Socket-Select Latch provides a control line for the Hi/Low Range Switch and control lines for the Socket Card.

The Data Latch buffers the data bus and holds data to satisfy the DAC requirements.

The Address Latch buffers low-order addresses for the Secondary Decoder. The decoder provides the appropriate signals for the DACs and registers as well as the latches on this card and on the Waveform Generator. The $V \bullet \emptyset_2$ signal controls the timing of the various clock signals developed by the decoder.

7.3.4 UniPak SOCKET CARD

The UniPak Socket Card distributes to the device sockets the signals developed on the Address and Data Driver Card and the Waveform Generator. Refer to the block diagram, Figure 7-6. The device address lines connect directly to the device sockets; larger devices connect to more device addresses than smaller devices; diode-overvoltage protection on these lines prevents damage to the drivers on the Address and Data Driver Card.

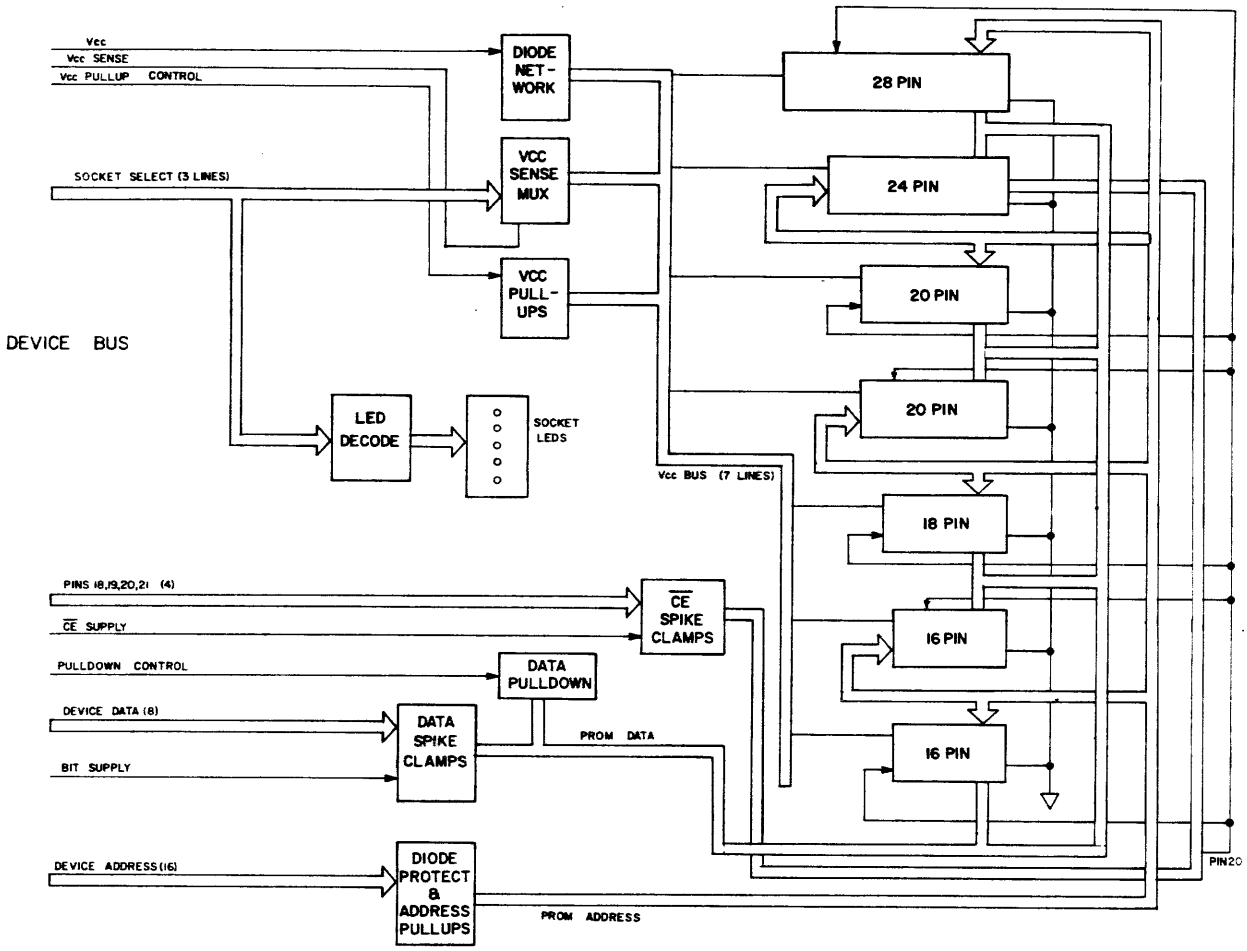


Figure 7-6. Block Diagram, UniPak Socket Card

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD_1-PD_4. The data pulldowns consist of 1 kΩ resistors and a diode network. Data-Spike Clamps consist of diode networks and capacitor-resistor networks. The diode networks are used to clip overshoot on the data-line programming pulses. The capacitor network is charged by the Bit Supply so that the network does not absorb energy from the actual data-line programming pulses.

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the Waveform Generator via the corresponding pin switches. A spike-suppression network similar to that used on the data lines is provided where the $\overline{CE}$ Supply charges the R-C network. Vcc is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the Vcc-Sense Mux. When Vcc is brought to zero, the device's Vcc lines can be pulled up by the Vcc pullups. The Vcc-Sense Mux and a comparator on the Address and Data Driver Card are then used to read the Vcc voltage. If a device is in a socket the Vcc voltage will be above 2 V. If it is in backwards it will be below 1 V, and if no device is in the socket the voltage will approach 4 V.

The LED Decoder is used to light the LED below the selected socket.

7.3.5 UniPak MEMORY CARD

The UniPak Memory Card is shown in block-diagram form in Figure 7-7. PROMs which store the UniPak software are contained on the Memory Card. These PROMs connect to the address bus directly, and to the data bus through data buffers.

Two PROMs and a latch comprise the Primary Decoder. The PROMs connect to 12 higher-order address lines and the R/$\overline{W}$ line. Outputs from the Primary-Decoder Latch connect to the Secondary Decoder and also to secondary decoders on the Address and Data Driver Card and the Waveform Generator. A 1-of-8 decoder timed with $\overline{V \bullet \emptyset_2}$ provides the secondary decoding for the software PROMs. Two additional lines from this decoder connect to the Address and Data Driver Card to provide the decode signals for the Data Gate and Comparator Gate/Mux. Additional outputs from the Primary Decoder enable the Data Buffer during all software-read operations and lower the Data-Gate-Enable line during any access of the UniPak.

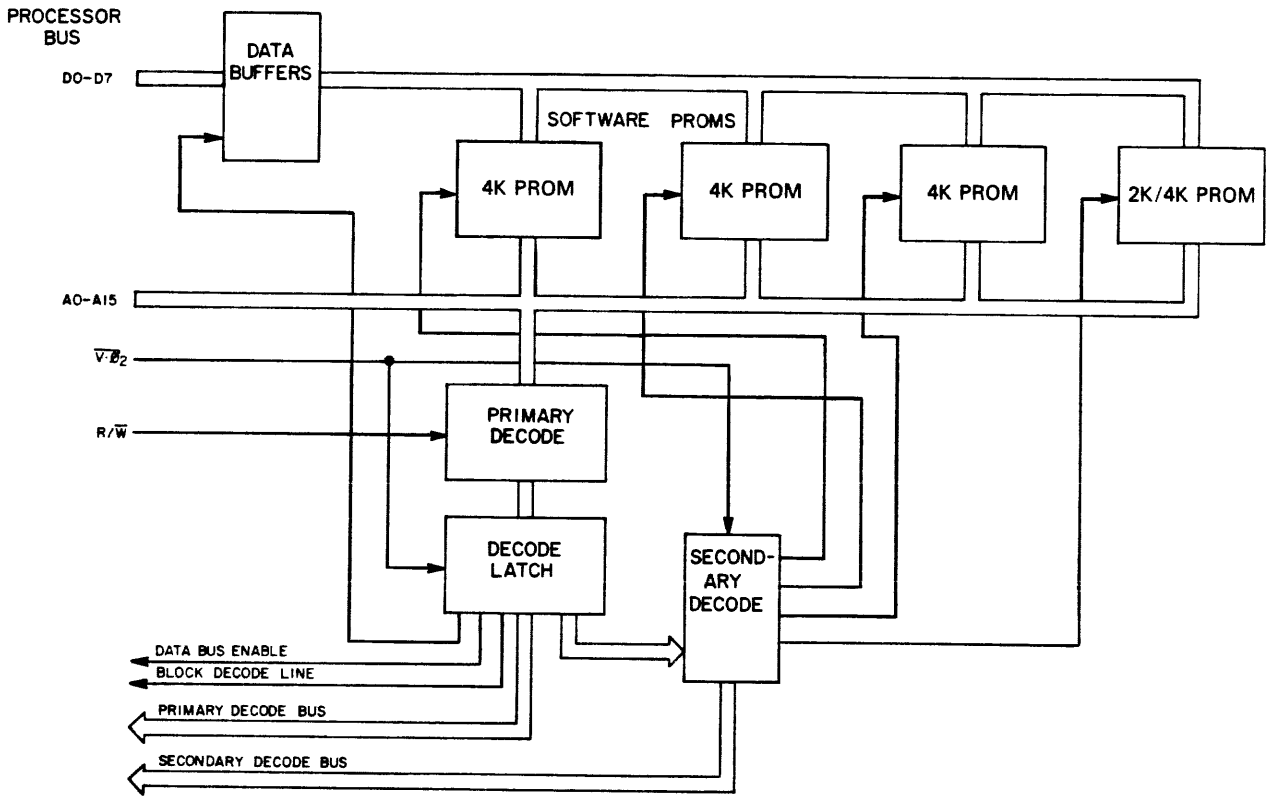


Figure 7-7. Block Diagram, UniPak Memory Card

SECTION 8
SCHEMATICS

30-702-7995	Socket Assembly
30-702-0045	UniPak Memory
30-701-7997	Waveform Generator
008-1998	Address Card
008-1999	Motherboard

REVISIONS				
ZONE	LTR	DESCRIPTION	ECN	DATE
	A	RELEASE PER ECN 4564	[illegible]	6/82
	B	ECN 4728	[illegible]	1/83

VPUP 20
S1 44
S2 45
S3 46
SOCKET SELE
VCC SENSE
VCC 34
CE SUPPLY 11
PIN 18 38
PIN 19 39
PIN 20 13
.N21 14
J1
O.C. 18
BIT SPLY. 37
BIT SW 12
VREF 21
VCC SENSE 10
SP 47
SP 48
SCOPE TRIGGER 15
GND 9 35 36 50
+5V 49
+24 VOLTS 17
J2

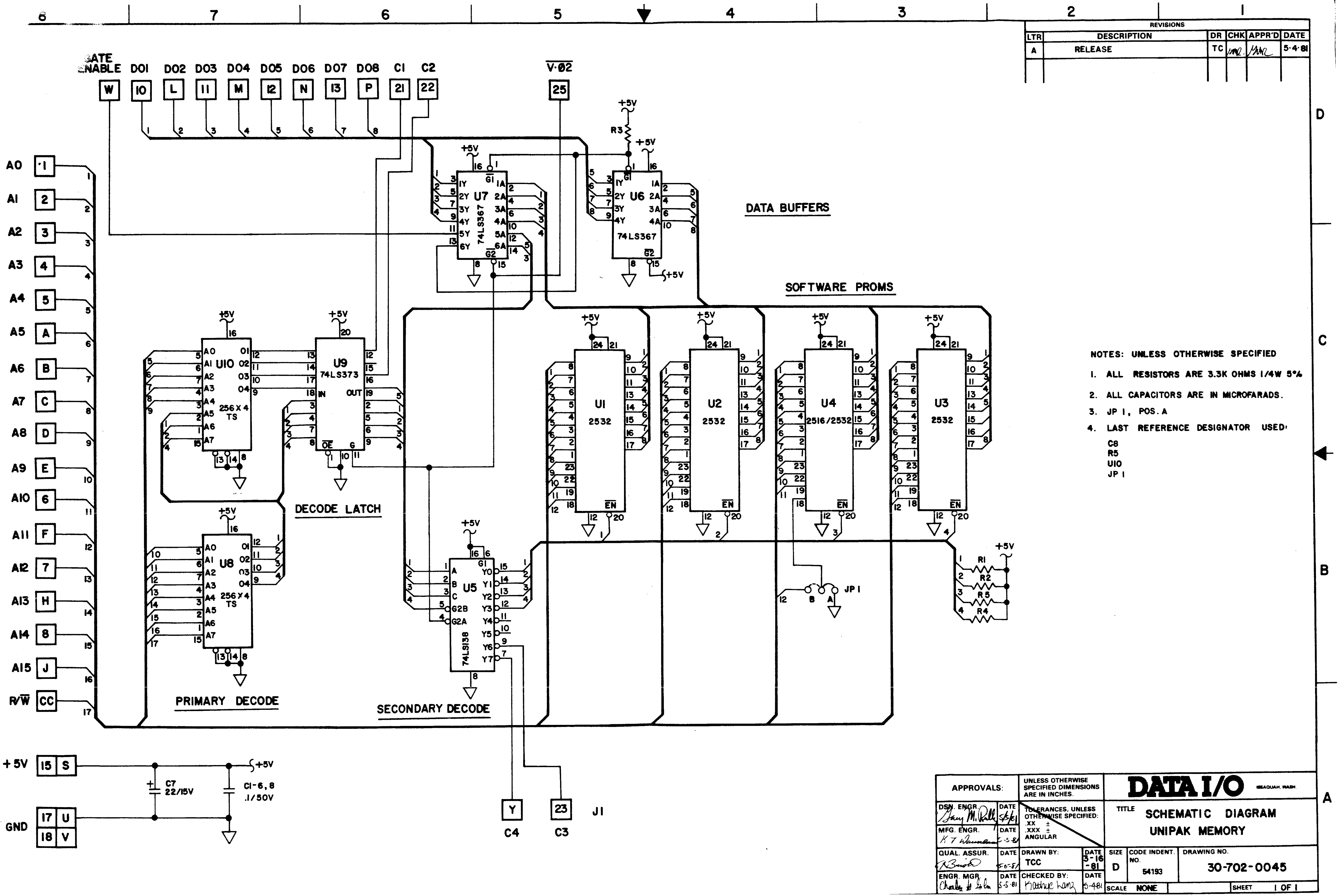
+15V +5V -9V
U2 6108
R4 R5 R6 3.3K (3 PLACES)
R7 2.2K
R8 2.2K
Q1 2N2907
CR17 IN4148
R9 300 1/2W
VCC SENSE MUX
CR15 CR11 CR13 CR16 CR14 CR12 CR8 IN4003 (7 PLACES)
U1 74LS138 L.E.D. DECODE
SOCKET LED'S DS4 DS5 DS6 DS7 DS8 DS3 DS2 DS1
R15 R16 R17 R18 R14 R12 R11 470 (7PLACES)
CR10 IN4148
CR9 IN4148
R10 10K C7 .1/50V
CR5 CR6 CR7 1N5819 (3 PLACES) CE
SPIKE CLAMPS
BIT SPLY
CE SPLY
VCC SENSE
VCC
VCC PULLUPS
RP1 330
U3 TID121
VCC PROTECTION
CR4 IN4745
ADDRESS PULLUPS
R2 10K
RP3 10K
R1 10K
RP2 10K
DEVICE SOCKETS
C6 .01 50V
U5 SOCKET 1
C8 .01/50V
U6 SOCKET 2
C9 .01/50V
U8 2K X 4 SOCKET 3
DIODE PROTECTION
U4 TID121
U17 TID121
C1,C4 .1/50V
R3 1K
C2 .1/50V
CR3 IN4745
-9V 16
C3 .1/50V
-9V J2
DEVICE SOCKETS
C5 .01 50V
U16 SOCKET 7
C13 .01 50V
U14 SOCKET 6
C12 .01 50V
U13 SOCKET 5
C10 .01 50V
U11 SOCKET 4
DATA SPIKE CLAMPS
U12 TID121
C11 .1/50V
DATA SPIKE CLAMPS
U15 TID121
C14 .1/50V
DATA PULLDOWNS
U9 1K
U10 TID121
Q2 2N2222
PULL DOWN CONTROL 19
J2
DATA SPIKE CLAMPS
U7 TID121
CR2 IN4148
CR1 IN4148
C5 .1/50V
R13 4.7K
BIT SUPPLY

PA15 8
PA14 7
PA13 6
PA12 5
PA11 4
PA10 3
PA9 2
PA8 1
PA7 26
PA6 27
PA5 28
PA4 29
PA3 30
PA2 31
PA1 32
PA0 33
J2

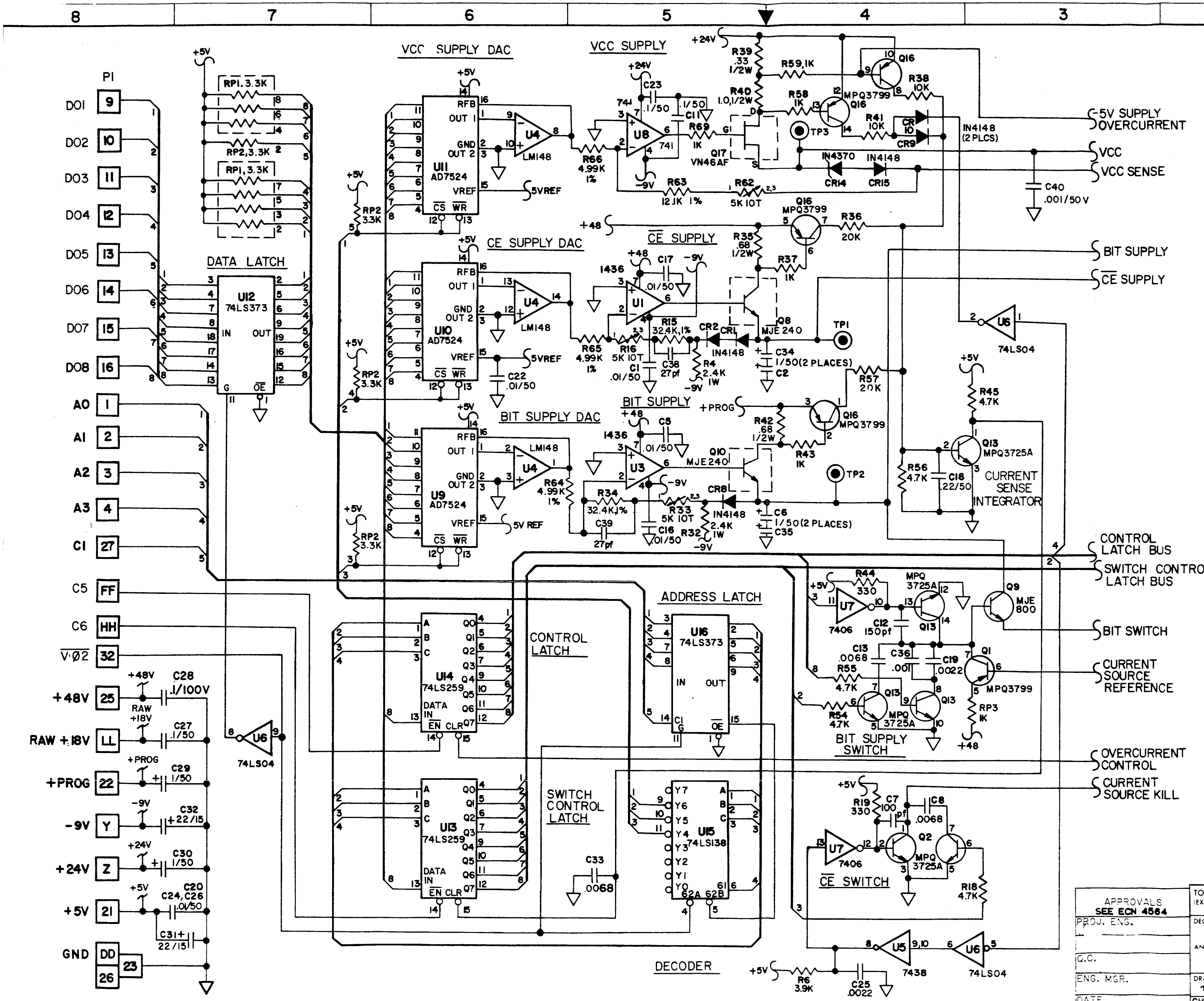
PD1 40
PD2 41
PD3 42
PD4 43
PD5 25
PD6 24
PD7 23
PD8 22
J2

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3 LAST REFERENCE DESIGNATOR USED:
U17 CR17
RP3 C15
R18 J2
DS7 Q2

APPROVALS SEE ECN 4564	TOLERANCES (EXCEPT AS NOTED)	DATA I/O
PROJ ENG	DECIMAL ±	TITLE SCHEMATIC DIAGRAM UniPak SOCKET ASSEMBLY
D.C.	ANGULAR ±	
MFG MGR	DRAWN BY: G. RYDER	SIZE D; CODE IDENT NO; DRAWING NO. 30-702-7995
DATE	CHECKED BY:	SHEET 1 OF 1



REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
A RELEASE TC 5-4-81
DATA BUFFERS
SOFTWARE PROMS
DECODE LATCH
PRIMARY DECODE
SECONDARY DECODE
U7 74LS367
U6 74LS367
U9 74LS373
U10 256 X 4 TS
U8 256 X 4 TS
U5 74LS138
U1 2532
U2 2532
U4 2516/2532
U3 2532
JP1
R1 R2 R3 R4 R5
C7 22/15V
C1-6, 8 .1/50V
+5V
GND
J1
C4
C3
V·Ø2
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8 C1 C2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 R/W
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 3.3K OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. JP 1, POS. A
4. LAST REFERENCE DESIGNATOR USED:
C8
R5
U10
JP 1
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES, UNLESS OTHERWISE SPECIFIED:
DATA I/O
TITLE SCHEMATIC DIAGRAM UNIPAK MEMORY
DRAWN BY: TCC
DATE 3-16-81
SIZE D
CODE INDENT. NO. 54193
DRAWING NO. 30-702-0045
SCALE NONE
SHEET 1 OF 1



REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE.	APP	DATE
	A	RELEASE PER ECN 4564				5/81

NOTES:

UNLESS OTHERWISE NOTED:

1. RESISTORS ARE 1/4W AND IN OHMS.
2. CAPACITORS ARE IN MICROFARADS.
3. U2,U5,U6,U7 - PIN 7=GND, PIN 14=+5V
   U12,U16 - PINS 1 & 10 = GND, PIN 20=+5V
   U13,U14,U15 - PIN 8=GND, 16=+5V
   U4 PIN 4= +24, PIN 11= -9
4. LAST REF. DES. USED:
   RP3
   C40
   Q25
   U16
   CR17
   R70
   TP4
   VR2

APPROVALS SEE ECN 4564	TOLERANCES (EXCEPT AS NOTED)	DATA I/O	
PROJ. ENG.	DECIMAL ±	TITLE SCHEMATIC DIAGRAM UniPak WAVEFORM GENERATOR	
Q.C.	ANGULAR ±		
ENG. MGR.	DRAWN BY T. CONNERTON	SIZE D	DRAWING NO 30-701-7997
DATE 1-17-80	CHECKED BY:	SCALE	SHEET 1 OF 2

REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE	APP	DATE
		SEE SHEET ONE				3/82

J1 (34) (10) (11) (37) (12) (18)

C40 .001

VCC
VCC SENSE
$\overline{CE}$ SUPPLY
BIT SUPPLY
CURRENT SOURCE REFERENCE
CURRENT SOURCE KILL
OVERCURRENT CONTROL
CONTROL LATCH BUS
SWITCH CONTROL LATCH BUS

+5V RP2 3.3K U2 7406 U6 74LS04 C37 200PF

+48 RP3 IK Q1 MPQ3799 CR4 IN4003 CR5 IN4003 CR3 IN4003 R17 5K 10T R2 32.4K 1%

Q3 2N2484 CR13 IN4370 R3 4.7K R1 IK $\overline{CE}$ PIN 18 SWITCH

MJE 800 Q4 R21 2.2K 1/2W J1 (38) PIN 18

Q2 MPQ3725A R49 3.3K CR6 IN4003 C9 470pf Q20 MJE240

U7 7406 U5 7438 +12, +5 SUPPLY

+24 VR2 78L12 C21 .1/50 R22 330 U2 7406 (4) PA 11

R61 1.2K CR17 IN751 R47 2.2K 1/2W U7 7406 (13) PIN 20

R68 3.3K Q2 MPQ3725A U7 7406 U5 7438 U7 7406

$\overline{CE}$ Q14 MJE800 CR12 IN4003 R48 330 C14 470pf Q24 MJE240 $\overline{CE}$ PIN 20 SWITCH

Q18 MJE800 CR11 IN4003 R13 2.2K 1/2W (14) PIN 21

+18V R50 IK 1/2W TP4 5VREF R60 5K 10T VR1 TL430 Q23 MJE240 R9 3.3K DAC REF

74LS04 U6 U2 7406

R25 3.3K R24 3.3K Q11 2N2907 R23 3.3K R20 3.3K +5V

R27 IK R28 IK R29 470 C10 470pf Q21 MJE240 2N2907 Q5 Q19 2N2222 R26 IK R30 IK Q7 MJE240

-9V R70 300K R51 10K 1% PIN 21 SWITCH

5VREF R52 4.42K 1% R53 4.99K 1% U6 74LS04 U2 7406 U4 LM148 R5 IK CR16 IN4003 C15 .1/50 Q15 MJE251

+24V (17)
-9V (16)
+5V (49)
GND (9) (35) (36) (50)

-5V SUPPLY OVERCURRENT R12 4.7K Q25 MJE240 R31 IK R14 5.1 1/2W -9V

-5V, 0V SUPPLY

J1 (3) PA 10

BIT SWITCH

C3 470pf R11 2.2K Q6 MJE251 R46 470 Q12 MJE240 R7 220 CR7 IN4003 Q22 MJE240 R10 330 C4 470pf R8 2.2K 1/2W (39) PIN 19 (5) PA 12

R67 4.7K (19) PULL DOWN CONTROL

PIN 19 SWITCH

APPROVALS: SEE ECN 4564	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
PROJ. ENG.		TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM UniPak WAVEFORM GENERATOR
Q.C.		DRAWN BY: T. CONNERTON	DATE 10/79
ENG.		CHECKED BY:	DATE
		SIZE D	CODE IDENT NO. DRAWING NO. 30-701-7997
		SCALE	SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	CM	PE	DATE
	A				1-17-80
	B	ECN 3742			7-80

ADDRESS LATCH

PI
A0 1
A1 2
A2 3
A3 4
A4 5
A5 A 6
A6 B 7

+5V
U21 74LS373 IN OUT OE

L.O. ADDRESS LATCH
U1 74LS259 DATA IN CL EN

H.O. ADDRESS LATCH
U2 74LS259 DATA CL EN

SOCKET SELECT LATCH
U14 74LS259 DATA CL EN
TO RANGE SWITCH

PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11 PA12 PA13 PA14 PA15
33 32 31 30 29 28 27 26 1 2 3 4 5 6 7 8

JI
S1 44
S2 45
S3 46
VPUP 20
SCOPE TRIGGER 15
TPI

+5V 49

JI
ENABLES
OVER CURRENT 18

GND 9 35 36 50

SECONDARY DECODE
+5V
U15 LSI38 A B C G1 G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

PI
CI 27
V-Ø2 32

U20 LSI38 A B C G1 G2A G2B Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

PI
C2 28
C3 29
C4 EE
C5 FF
C6 HH

U27 74LS04

GND
23 26 DD

RAW 18V LL → RAW 18V

OPER-ATE BB
R22 10

SENSE 24
R23 10K 1%

PI

+5V DATA GATE
U24 74LS244 OUT IN 2G

PI
DO1 9
DO2 10
DO3 11
DO4 12
DO5 13
DO6 14
DO7 15
DO8 16

GATED DATA
RP8 3.3K
+5V +5V RP5 3.3K

+5V
U25 74LS373 IN OUT G OE

LATCHED DATA
RP3 3.3K
+5V +5V RP4 3.3K

DATA LATCH

+5V 21 .1/50V C13 C17 +5V C15 22/15V
+PROG 22 1/50V C14 +PROG .1/50V C3 +VP
R25 10K
-9V Y C4 .1/50V -9V C16 22/15V

PI

CR2 IN751

UNUSED GATES
U27 74LS04
U27 74LS04
U27 74LS04
U27 74LS04
U8 LM339

+5V
U7 74LS251 A B C CLK D0 D1 D2 D3 D4 Y

RP4 3.3K +5V

COMPARATOR GATE/MUX
JPI

U8 1/4 LM339
R9 100K 1%
R11 100K 1%
R16 100K 1%
R15 33.2K 1%
R10 100K 1%
R12 33.2K 1%
VREF

JI
10 VCC SENSE
13 PIN 20
BIT SW.

SUPPLY COMPARATORS

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS IN MICROFARADS.
3. LAST REF. DES. USED:
   U27 R25 TP4
   CR5 C17 JI
   RP8 Q19 JPI

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ± / ANGULAR ±	TITLE SCHEMATIC DIAGRAM UniPak ADDRESS CARD		
APPROVALS			
PROJ. ENG.			
ENG. MGR.	DRAWN BY	SIZE D	CODE IDENT NO.	DRAWING NO. 008-1998
DATE 1-4-80	CHECKED BY	SCALE NONE	SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE	1-17-85	J.B.

DATA SINKS

DATA SWITCHES

ATCHED DATA

GATED DATA

ENABLES

DATA COMPARATORS

1/4 LM339 +PROG U22 U23

RP5 3.3K +5V

VREF

DATA SINK REGISTER

U12 74C374 IN OUT CLK OE +5V

Q12 MJE240 Q13 MJE240 Q14 MJE240 Q15 MJE240 Q16 MJE240 Q17 MJE240 Q18 MJE240 Q19 MJE240

470

U11

DATA SWITCH REGISTER

U18 74C374 IN OUT CLK OE +5V

RP7 220

U16 U17

C10 C6 C9 C5 C12 C8 C11 C7 250pf

RP6 330

Q9 Q5 Q8 Q4 Q11 Q7 Q10 Q6 MJE251

R21 R17 220

U16, U17, MPQ3725A

J1

21 VREF

40 PD1

41 PD2

42 PD3

43 PD4

25 PD5

24 PD6

23 PD7

22 PD8

12 BIT SWITCH

BIT SW

U26 AD7524 LSB MSB CS WR GND RFB OUT1 OUT2 VREF +5V

U19 AD7524

VREF DAC

LOAD SUPPLY DAC

C1 .1/50

R1 5K 15T

CR1 TL430

R2 2.2K 1/2 W

RAW18V

+VP

U13 LM148 -9V

R19 4.99K 1%

R20 4.99K 1%

LOAD AMP

TP4

VREF.

R18 10K, 1%

LOAD SUPPLY

R8 34.8K 1%

C2 .1/50

+PROG

Q3 MJE240

R5 10K

R6 1K

Q1 2N2907

Q2 2N2484

R7 470

HI-LO RANGE SWITCH

TO RANGE SWITCH

R4 4.7K

R3 4.7K

LOW RANGE LOADS

HIGH RANGE LOADS

RP2 10K

U5 TID139

R13 10K

CR3 IN4148

RP1 2K

U4 TID 139

R14 2K

CR4 IN4148

J1 TP3 SP 48

SP 47 TP2

LOAD CLAMPS

U3 TID121

U6 TID121

+5V R24 470

CR5 IN4733

TOLERANCES (EXCEPT AS NOTED)

DECIMAL ±

ANGULAR ±

DRAWN BY

APPROVED BY

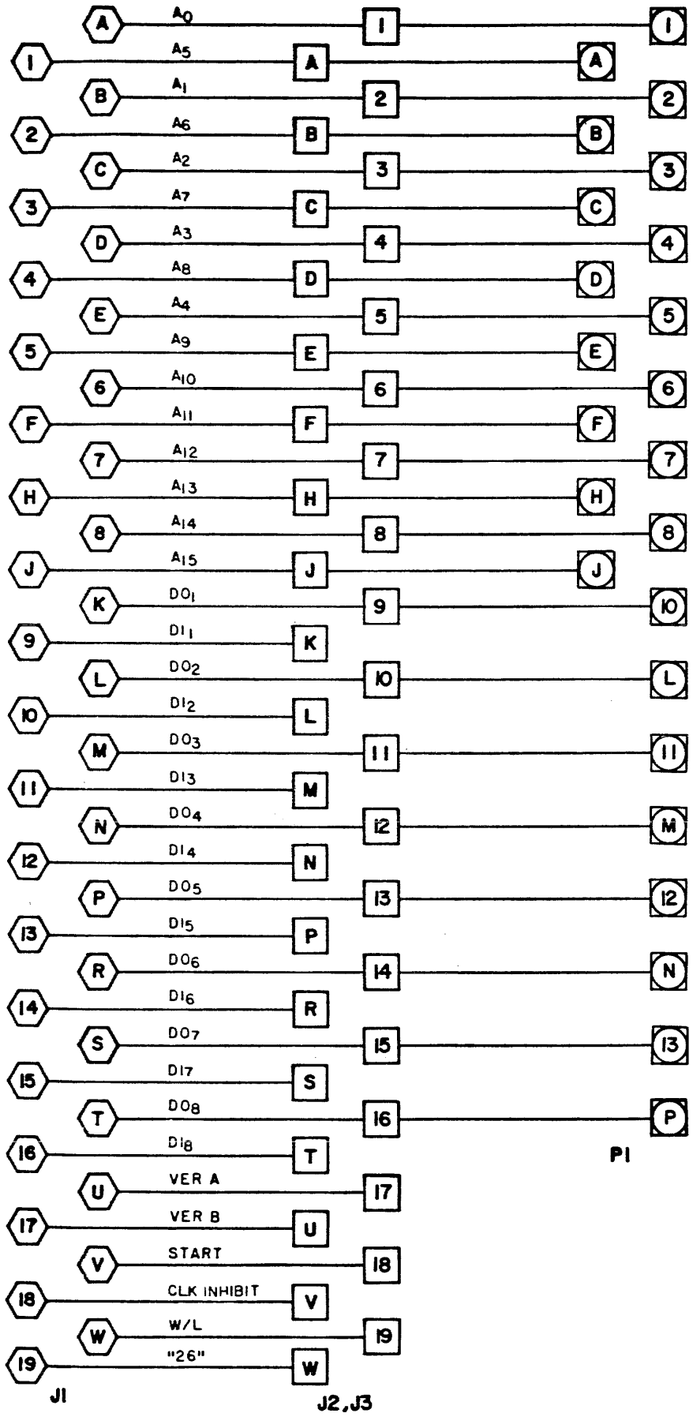
DATA I/O ISSAQUAH, WASH

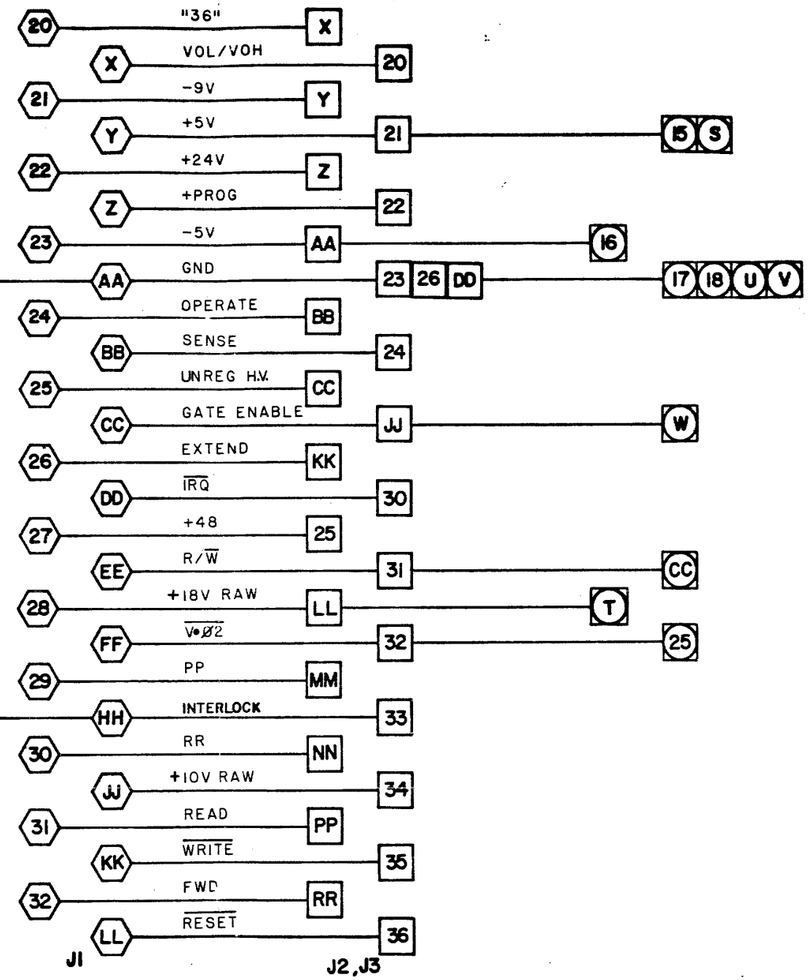
TITLE SCHEMATIC DIAGRAM UniPak ADDRESS CARD

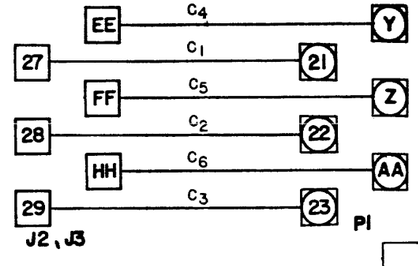
SIZE D | CODE IDENT NO | DRAWING NO. 008-1998

SCALE NONE | SHEET 2 OF 2

REVISIONS						
ZONE	LTR	DESCRIPTION	DWN	CK	PE	DATE
	A	RELEASE	BZ			1-80







APPROVALS	TOLERANCES (EXCEPT AS NOTED)	DATA I/O REDMOND WASH	
PROJ. ENG.	DECIMAL ±	TITLE	SCHEMATIC DIAGRAM UniPak MOTHERBOARD
PROD. ENG.	ANGULAR ±		
CONF. MANG.	DRAWN BY G. RYDER	SIZE D	CODE IDENT NO
ENG. MGR.	CHECK	DRAWING NO	008-1999
DATE 1-17-80		SCALE NA	SHEET 1 OF 1

APPENDIX 1

ERROR CODES

NOTE

In the case of an error condition, be sure that the Family and Pinout Codes are correct for the PROM installed.

CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data were incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data were incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid Family and Pinout Codes are not selected, or Family Code selection not followed by Pinout Code selection.
31	Excessive Current Drain	The operation stopped due to excessive current drain by a device.
32	Backwards Device	The operation stopped due to Vcc level test indicating a backwards device.
34		Number wrong/invalid family and pinout code in remote control.
35	Faulty Chip Select	The operation stopped due to data being present while a device is disabled.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
37	Socketing Error	Operation stopped due to a low Vcc level indication on sockets presumed to be empty. A device may be in the wrong socket, or 2 or more devices may be socketed simultaneously.
70	Faulty Bit Supply	The operation stopped due to a faulty bit supply. Do not use UniPak until repaired.
71	Faulty CS Supply	The operation stopped due to a faulty CS supply. Do not use UniPak until repaired.
72	Faulty Vcc Supply	The operation stopped due to a faulty Vcc. Do not use UniPak until repaired.
BØ	Illegal Erase Operation	The operation stopped because an attempt was made to perform a byte-erase operation that the UniPak cannot byte erase. This error may appear when block limits are set or when accessing calibration step 21.

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FIELD BULLETIN

To: All 29A Programmer Users
Subject: 64K x 8 Dynamic RAM

November, 1983
FB #021-0209

This Field Bulletin affects 29A Programmers with the following part numbers:

990-0029-065
990-0029-066
990-0029-067
990-0029-068

The part number is located on the serial number sticker on the bottom of the unit.

Some 64K x 8 Dynamic RAM Boards have exhibited a marginal timing problem in the RAM refresh circuitry. This timing problem results in an intermittent RAM data error "64". To correct this problem, a new refresh timing PAL has been developed.

If you have one of the units listed above and are experiencing the "error 64" problem, contact your local Data I/O Service Center for a free update kit.

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0683/1083

DATA I/O

FIELD BULLETIN

To: All 29A Programmer Users
Subject: 16-Bit Development System Data Formats

November, 1983
FB #021-0210

This Field Bulletin affects Model 29A Programmers with firmware configuration numbers "088A" or "86F1." To display the system's firmware configuration number, enter: SELECT-B2-START.

When receiving 16-bit Data Formats (Intel, Motorola, T.I. and H.P.), address fields outside the desired block of data are not being translated properly by the affected units. If you have one of the affected units, a firmware update can be obtained from your local Data I/O Service Center at no charge.

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FIELD BULLETIN

To: All PLDS Users
Subject: 1. LogicPak 303A
2. PALASM Design Adapter 303A-100
3. Signetics IFL Design Adapter 303A-101

November, 1983
FB #021-0211

---

1. LogicPak 303A V02.

   This Field Bulletin applies only to the V02 version of the LogicPak™. To determine the version number of the pak, check the label under the rear edge of the pak.

   When using the programmer serial port for control of the pak or for data transfer with odd or even polarity selected, the V02 version LogicPak™ would give invalid responses.

   If you have a V02 version LogicPak™, contact your local Data I/O Service Center for a firmware update at no charge.

2. PALASM Design Adapter 303A-100 V02

   This Field Bulletin applies only to the V02 version of the PALASM design adapter. To determine the version number of the adapter, check the label under the front edge or, with the adapter installed on the LogicPak™ in the programmer, enter SELECT CODE "EF" "START" and observe the programmer display. If it displays configuration number "EC4E," it is a V02 adapter.

   When using the programmer serial port for remote control or data transfer with odd or even parity selected, the V02 version PALASM design adapter would give invalid responses.

   If you have a V02 version PALASM design adapter, contact your local Data I/O Service Center for a firmware update at no charge.

3. Signetics IFL Design Adapter 303A-101 V02

   This Field Bulletin applies only to the V02 version of the Signetics IFL Design Adapter. To determine the version number of the adapter, check the label under the front edge or, with the adapter installed on the LogicPak™ in the programmer, enter SELECT CODE "EF" "START" and observe the programmer display. If it displays configuration number "3AD2," it is a V02 adapter.

   When using the 82S158/159 FPLS devices, the firmware in the V02 adapter did not properly generate or translate the Signetics ASCII Logic Format (the JEDEC format operates correctly). If you have a V02 IFL Design Adapter, contact your local Data I/O Service Center for a firmware update at no charge.

Attached is an updated copy of the logic diagram for the 82S158/159 FPLS devices. Use it to replace the one in your 303A-001 Signetics IFL P/T Adapter manual. The earlier one had the wrong fuse numbers assigned to the "EA" and "EB" fuses.

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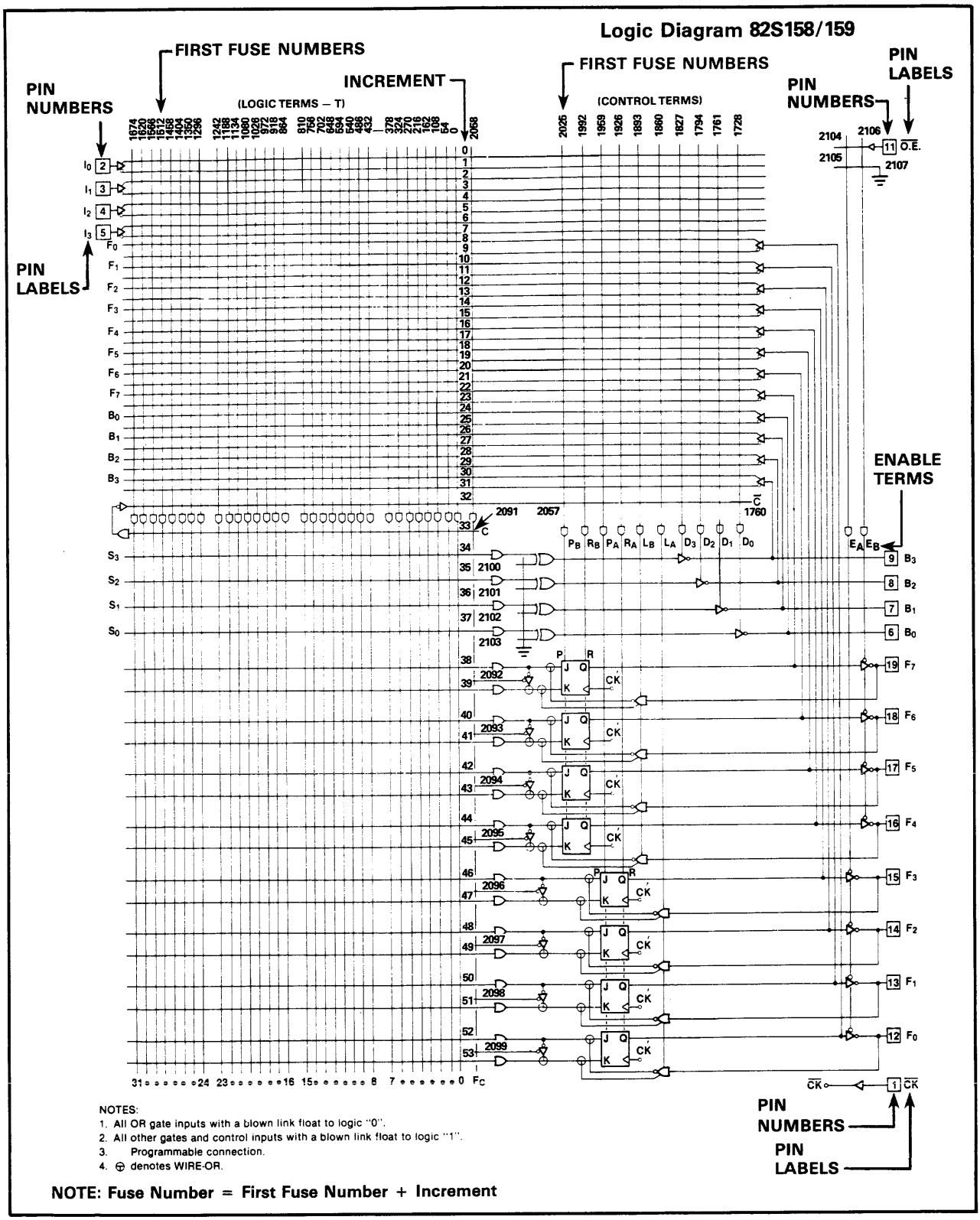

Figure A-6. Logic Diagram 82S158/159