

# DATA/CONTROL INTERFACE CARD

**05427-60001 or 05451-60025**

(FOR 2100, 2114, 2115, 2116, 21MX and 21MX-E COMPUTERS)

## OPERATING AND SERVICE MANUAL

### NOTE

Retain this manual with the applicable computer system documentation.

### Card Assemblies

05451-60025, Series 1440

05427-60001, Series 1440

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PACKARD**

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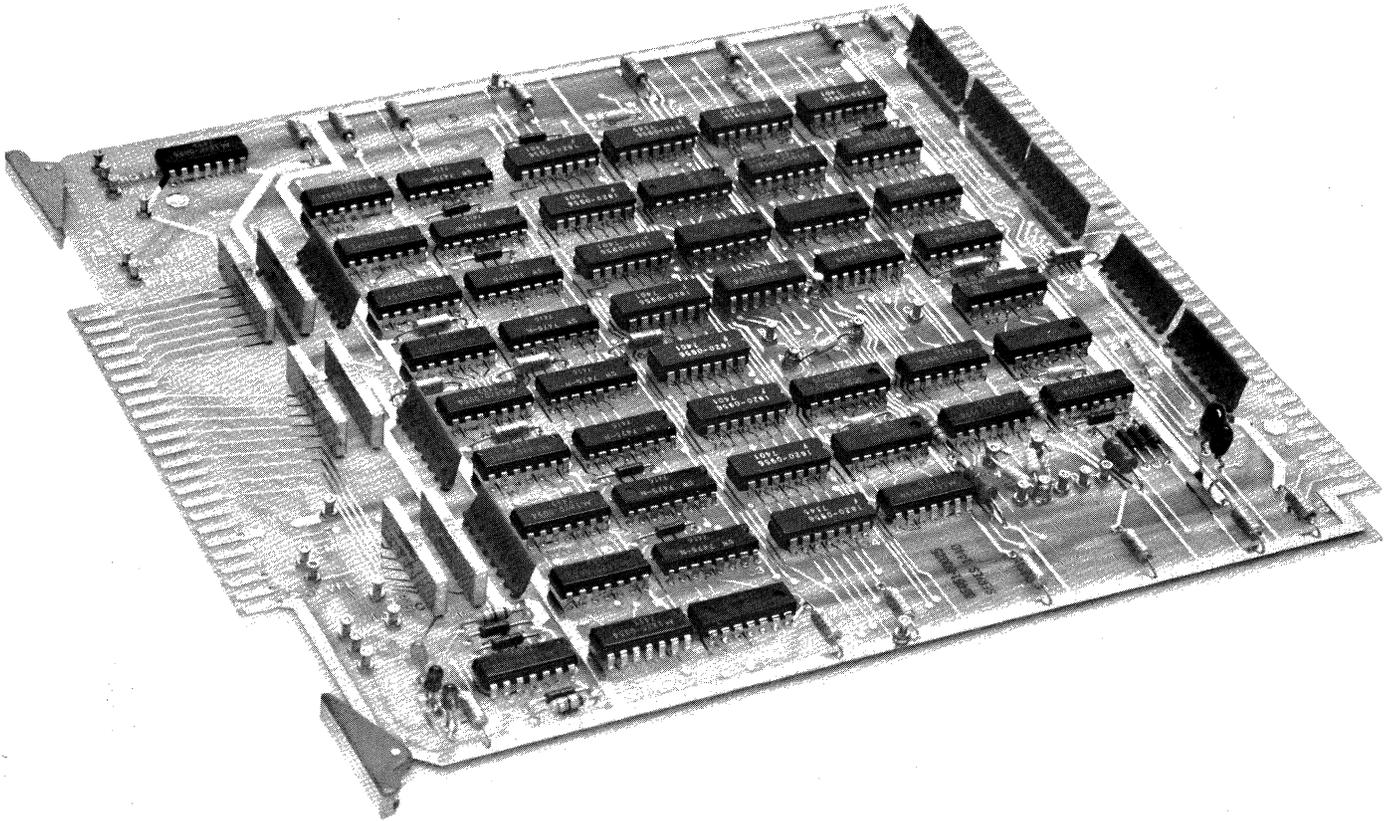
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Figure 1-1. Interface Card



(05451-60025 shown)

## SECTION I GENERAL INFORMATION

### 1-1. INTRODUCTION

This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, and replaceable parts information for the HP 05451-60025 and the HP 05427-60001 Data/Control Interface Card (see Figure 1-1).

### 1-2. DESCRIPTION

This interface card provides a means to transfer data, in either direction, between an HP computer and a peripheral device (or other computer), as shown in Figure 1-2. Separate 16-bit buffer registers are provided for input and output. Two sets of two-wire "handshake" lines are software-selectable to allow connection of the one interface card to two devices while using a single I/O select code. Many jumpering options are available to allow interfacing of existing devices and to allow full-speed DMA transfer rates.

All control signals and data lines are wire-ORable, ground-true, TTL logic levels.

### 1-3. COMPARISON WITH HP 12566

The 05451-60025 Data/Control Interface Card differs from the HP 12566-60024 option 001 (ground-true) Microcircuit Interface Card in the following ways —

- Increased output drive capability (43 mA vs 31 mA)
- Increased transfer rate (full 1 MHz DMA instead of every-other-cycle)
- Two sets of device command and device flag lines are provided (instead of one) to allow connection to two devices or bus's.
- Several new jumper options facilitate highspeed device interfacing by increasing the allowable command to flag turnaround time for every-cycle DMA transfers.
- Status lamps and test points are provided.

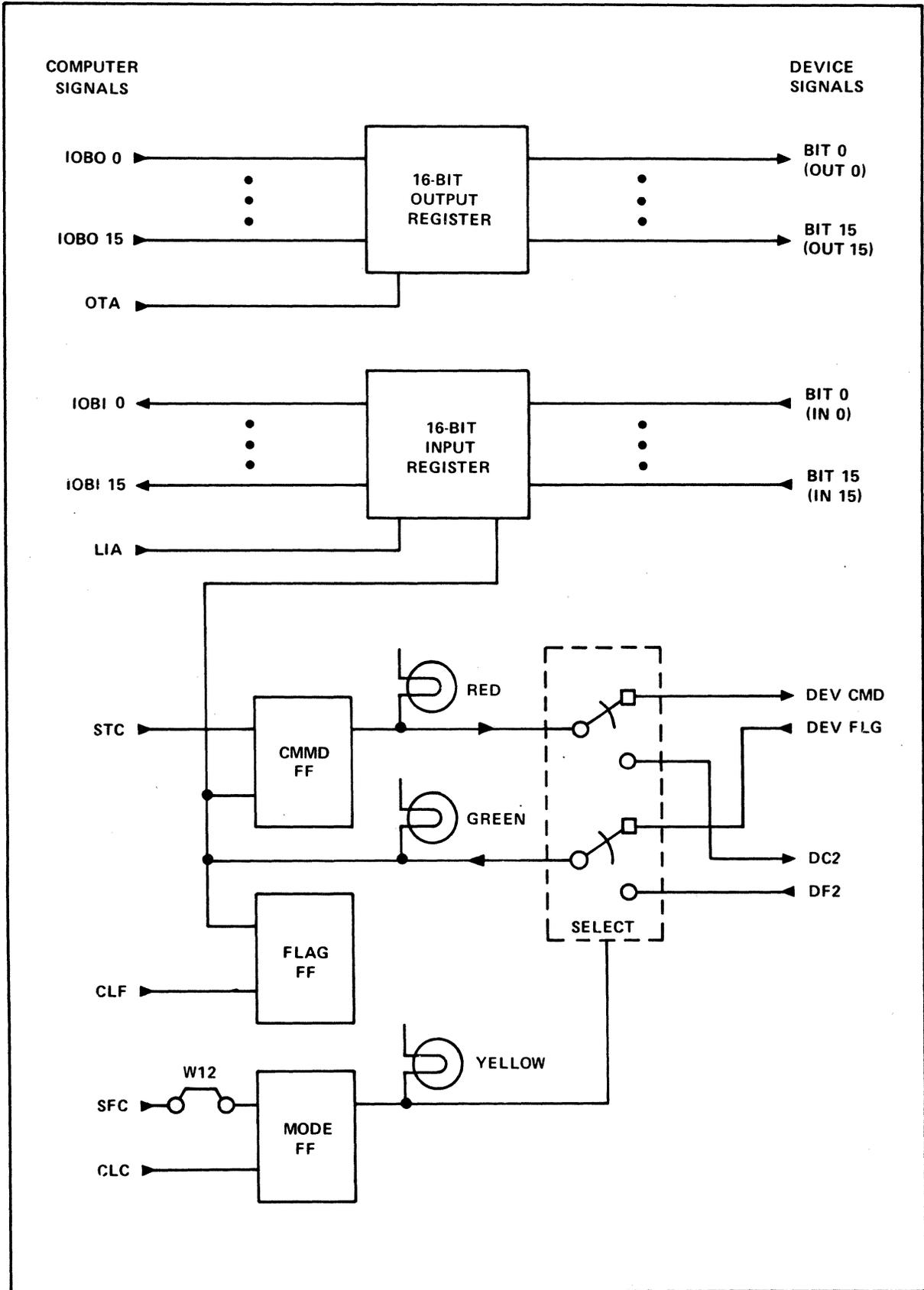
The 05451-60025 card is generally backward-compatible with the 12566 card and existing 12566-card-to-device cables as long as —

- The 05451-60025 jumpers W10-W13 (non-existent on 12566) are set as follows: W10A, W11A, W12 out, and W13 out.
- Card edge connector pins 19, 20, 31, W, and Y (unused on 12566) are unconnected.
- If jumper W1C ("party line command pulse" on 12566) is used, note that the pulse begins slightly earlier (T5 instead of T6).
- The additional current drawn from the Computer's +4.5V supply is acceptable (1.5 amps vs. 1.2 amps.)

The 05427-60001 Data/Control Interface Card differs from the 05451-60025 Data/Control Interface Card in two respects —

- U101 output device command IC
- Strapping of W10 jumper

Figure 1-2 Block Diagram



## 1-4. CHARACTERISTICS

Table 1-1 lists characteristics of the interface card.

*Table 1-1. Interface Card Characteristics*

Output Levels: Wire OR-able	
"1" state	0 to +.4 Vdc, 43 mA (sink)
"0" state	1000 $\Omega$ to + 5.0 Vdc
Inputs Levels:	
"1" state	0 to +.8 Vdc, 18 mA
"0" state	+2.0 to +5.0 Vdc
Current Requirements: (Supplied by computer)	
+4.5 Vdc Supply	1.5A typical (outputs connected to inputs, outputs all low)
-2 Vdc Supply	0.05 A
Card Dimensions:	
Width	7-3/4 inches (196,8 mm)
Height	8-11/16 inches (220,7 mm)
Weight	
Net	18 oz (544.8 gm)
Shipping	2 lb (908 gm)



## SECTION II INSTALLATION

### 2-1. INTRODUCTION

This section provides information on unpacking and inspection, preparation for use, installation, and reshipment of the interface card.

### 2-2. UNPACKING AND INSPECTION

If the shipping container is damaged upon receipt, request that the carrier's agent be present when the equipment is unpacked. Inspect the card for damage (scratches, cracks, loose components, etc.). If the card is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (HP Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged equipment without waiting for any claims against the carrier to be settled.

### 2-3. PREPARATION FOR USE

Because the interface card is designed for a variety of applications, an interconnecting cable must be either fabricated or otherwise available for the particular peripheral I/O device used, and jumpers on the printed circuit card must be placed in the positions that will effect desired operation.

### 2-4. CABLE FABRICATION

A 48-pin connector kit (Part Number HP 5060-8339) provides the connector required at the computer end of the interconnecting cable. The connector for the device end of the cable must be furnished by the user.

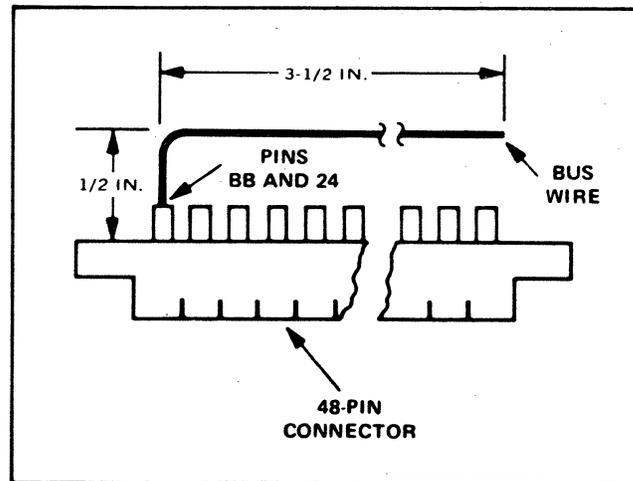
Due to the fast rise times and low voltage level outputs from the interface card, the interconnecting cable must be of the twisted-pair type. Some typical cables which can be used in this application are listed below.

Number of Twisted Pairs	HP Part Number
24 (unshielded)	8120-0957
36 (unshielded)	8120-1846
40 (unshielded)	8120-0924

Figures 2-1 and 2-2 show details of cable fabrication. The procedure for wiring the 48-pin connector is as follows:

- a. Insert approximately 10 inches of cable into the connector hood.
- b. Strip the outer jacket of the cable back 5 inches.
- c. Prepare a bus wire from 22-gauge bare-copper wire and solder it to pins BB and 24 of the connector as shown in Figure 2-1.
- d. Refer to Table 2-1, and select the signals to be used.

Figure 2-1. Bus Wire Details



- e. Divide the 36 twisted-pairs into groups of six pairs each.
- f. Starting at the end of the 48-pin connector nearest pins BB and 24, connect the first six pairs as follows:
  - (1) Solder each of the six colored signal wires to its selected pin on the connector and insulate each pin with tubing as shown in Figure 2-2.
  - (2) Solder the six white ground wires to the bus wire and insulate with shrink tubing as shown in Figure 2-2.
- g. Repeat substeps (1) and (2) with the remaining groups of wires until all wires are soldered to the connector and insulated.
- h. Trim off any excess bus wire and install the 48-pin connector in the connector hood using the two self-tapping screws.
- i. Install the cable clamp and tighten it in place with the setscrew.

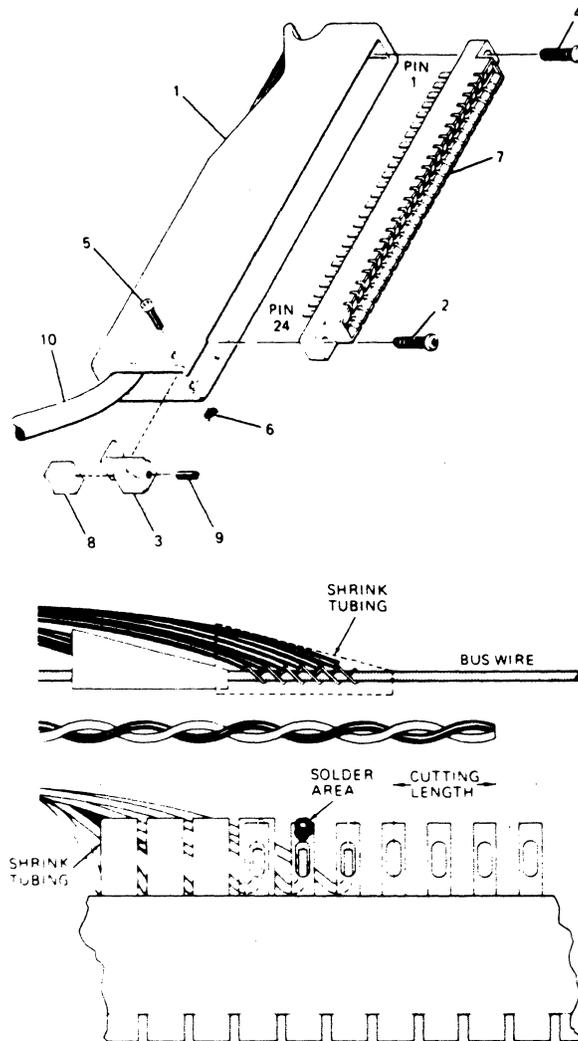
## 2.5. CIRCUIT CARD JUMPERS

Table 2-2 lists the jumper wires on the interface card and specifies the function associated with each jumper position. Figure 5-2 shows the location of each jumper on the circuit card. Use Table 2-2 to determine which jumper positions give the desired operating characteristics.

Standard positions for the 05451-60025 are marked with a **square**. Use of these positions provide a ground-true device command (DEVCMD), which is reset by the negative-going edge of the device flag (DEVFLG); strobed input data; continuously available output data; slow DMA; and disabled alternate hand-shake. Note that the I/O T-periods are approximately 200 ns long and occur in sequence 2-3-4-5-6-2. . .

Standard positions for the 05427-60001 are marked with a **circle**.

Figure 2-2. Cable Fabrication Diagram and Parts List



CONTAINED IN ITEM	DESCRIPTION	PART NO.
1*	CONNECTOR HOOD	5040-6071
2*	SELF-TAPPING SCREW (A)	0624-0098
3*	MOUNTING BLOCK	5040-6072
4*	SELF-TAPPING SCREW (B)	0624-0098
5*	PAN-HEAD SCREW (4-40 x .562")	.....
6*	HEX NUT (4-40 x .187")	.....
7*	CONNECTOR, 48 PIN	1251-0335
8*	CABLE CLAMP	5040-6003 OR 5040-6004
9*	SET SCREW	3030-0143
10	CABLE, TWISTED PAIR	See text

\* Items 1-9 contained in Connector Kit (HP Part No. 5060-8339)

Table 2-1. 48 Pin Device Interface Pin Assignments

FROM I/O DEVICE		TO I/O DEVICE	
PIN	SIGNAL	PIN	SIGNAL
1	IN 0	A	OUT 0
2	IN 1	B	OUT 1
3	IN 2	C	OUT 2
4	IN 3	D	OUT 3
5	IN 4	E	OUT 4
6	IN 5	F	OUT 5
7	IN 6	H	OUT 6
8	IN 7	J	OUT 7
9	IN 8	K	OUT 8
10	IN 9	L	OUT 9
11	IN 10	M	OUT 10
12	IN 11	N	OUT 11
13	IN 12	P	OUT 12
14	IN 13	R	OUT 13
15	IN 14	S	OUT 14
16	IN 15	T	OUT 15
17		U	
18		V	
		19,W	VCC*
20	RFD	X	
21	DF2	Y	DC2
		22,Z	DEVCMD
23,AA	DEVFLG		
24	GND	BB	GND

\*VCC is connected to pins 19 & W only if jumper W13 is inserted.

## 2-6. INSTALLATION

Before installing the interface card in the computer, determine that the additional power consumed by the card will not overload the computer power supply. Power requirements of the card are given in Table 1-1; instructions for calculating available power are given in the applicable computer manual. If sufficient power is available, and if the interconnecting cable has been fabricated and the jumper wires have been positioned for desired operation, install the interface kit as follows:

- a. Turn off power at the computer and at the I/O device.
- b. Gain access to the computer card cage and insert the interface card into the card slot corresponding to the desired I/O select code.
- c. Connect the 48-pin connector of the interconnecting cable to the 48-pin edge of the interface card.
- d. Connect the other end of the interconnecting cable to the proper connector on the I/O device.

## 2-7. RESHIPMENT

If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the number of the kit.

Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

### NOTE

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

Table 2-2. Interface Card Jumper Positions

JUMPER	POSITION	FUNCTION
W1	A	Ground-true device command signal starting at T3 (DMA) or T4 (software), reset as per W2.
	B	Positive-true version of W1A.
	C ○	Ground-true device command signal starting at T5, reset as per W10.
	D □ △	Ground-true device command signal starting at T3 (DMA) or T4 (software). Reset at first T5 following W2-specified condition.
W2	A	Resets device command signal on positive-going device flag edge.
	B □ △ ○	Reset device command signal on negative-going device flag edge.
	C	Reset device command signal on next T2.
W9	A □ △ ○	Allows CLC signal to reset device command signal. Does not apply if jumper W1C and W10B are used together.
	B	Does not allow CLC signal to reset device command signal.
W10	A □ △	Ignored unless W1C is used. Resets device command signal at next T3.
W10	W1-D ○	Ignored unless W1C is used. Resets device command signal at next T5 after device flag is received.

□ = Std Position for 05451-60025

△ = Std Position for 05451-60025 used with 5440 mainframe

○ = Std Position for 05427-60001

Table 2-2. Interface Card Jumper Positions (Continued)

JUMPER	POSITION	FUNCTION
W10	B	Ignored unless W1C is used. Resets device command signal as per W3-specified device flag edge. Note that the only way to reset a device command signal when W1C and W10B are used simultaneously is with a device flag edge.
W3	<p>NOTE:</p> <p>A</p> <p>B □ △ ○</p> <p>C</p> <p>D</p> <p>E</p> <p>NOTE:</p>	<p>Setting the Flag Buffer FF via W3 is inhibited if the Flag FF has not been cleared (by software or by DMA).</p> <p>Set the Flag Buffer FF on positive edge of the device flag signal.</p> <p>Sets the Flag Buffer FF on negative edge of the device flag signal (<math>\overline{\text{DEVFLG}}</math> or <math>\overline{\text{DF2}}</math>).</p> <p>Sets the Flag Buffer FF continuously, i.e., every T2.</p> <p>Sets the Flag Buffer FF on the positive-going edge of device RFD signals.</p> <p>Sets the Flag Buffer FF on the negative-going edge of device RFD signal.</p> <p>W3D or W3E allows the device to issue separate "data accepted" and "ready for data" messages on output.</p>
W11	<p>A □ ○</p> <p>B △</p> <p>C</p>	<p>Issues DMA service request SRQ signal when Flag FF is set. This limits DMA transfer rate to half-speed, i.e., every other cycle.</p> <p>Issues DMA service request SRQ signal when Flag Buffer FF is set. The SRQ signal must occur before T5 to allow every-cycle (i.e., full-speed) DMA transfers. This allows almost two T-periods for flag turnaround at the full rate.</p> <p>Issues DMA service request SRQ signal continuously. This is used by devices which can source or sink data at full DMA speed but which can not satisfy the T5 timing constraint of W11C. It may be used with non-handshake protocol (e.g., using W2C, so the device command is a strobe) or with handshake protocol (e.g., using W2B allows device flag to return as late as T2).</p>

Table 2-2. Interface Card Jumper Positions (Continued)

JUMPER	POSITION	FUNCTION
W4	A	Output data is gated on by device command signal and off by T5 following W2-specified condition.
	B □△○	Output data is continuously available.
W5	OUT	Input data bits 0-3 are continuously available in input register.
	IN □△○	Input data bits 0-3 are strobed into input register by W3-specified condition.
W6	IN □△○	Like W5, bits 4-7.
W7	IN □△○	Like W5, bits 8-11.
W8	IN □△○	Like W5, bits 12-15.
W12	IN △○	Enables programmer to switch device handshake modes. Following a CLC software instruction, $\overline{\text{DEVCM}}\overline{\text{D}}$ and $\overline{\text{DEVFLG}}$ are used for device command and device flag signals. Following a SFC software instruction, $\overline{\text{DC2}}$ and $\overline{\text{DF2}}$ are used. The handshake mode may be switched at any time to allow communication with two devices, a command bus and a data bus, etc.
	OUT □	Disables special processing associated with SFC software instruction.
W13	IN ○	Makes 5 volts available at card edge connector, to allow device to use computers power supply. W13, if used, should be an appropriate user-supplied fuse.
	OUT □△	Computer power is not available at the card edge connector.



## SECTION III PROGRAMMING

### 3-1. INTRODUCTION

This section provides assembly language programming information for the interface card.

For information concerning software systems used with the computer, software interfacing, and operating procedures, refer to the applicable software manuals provided with the computer documentation.

### 3-2. OPERATION AND TIMING

Section IV of this manual provides theory of operation for the circuits on the interface card. A flowchart, Figure 4-2, is provided to show the operating sequence of the interface card and, consequently, the time relationships of the individual operations.

### 3-3. GENERAL PROGRAM CONSIDERATIONS

A block diagram of the interface card is shown in Figure 1-2 (more detail is shown in Figure 4-1). All messages from the computer to a device are sent via the 16 output data lines and a single device command signal. All messages from the device to the computer are sent via the 16 input data lines and a single device flag signal. Jumper W12 allows the programmer to control two sets of device command and device flag signals, this is discussed later.

The device command signal is generated by the STC software instruction as specified by jumpers W1, W2, W9, and W10. This device command signal may be viewed by the device as a pulse (e.g., W2C), as the beginning of a command-flag handshake (e.g., W2B), or a level (to be later reset via a CLC instruction). The device flag signal (as selected by jumper W3) sets the Flag FF (flip-flop) on the interface card. This signal is always a change in logic level (e.g., high-to-low transition for W3B). The Flag FF may be sensed via the software SFS (or SFC) instructions, or it may be used to cause a computer interrupt, or it may be used to cause a DMA cycle-steal.

When the computer EXTERNAL PRESET switch is pushed, the device command signal is cleared and the Flag FF is set. This is the (conventional) idle state of an interface card. A "PRESET" may be programmed via a CLC and a STF instruction.

Some devices use a cable which jumpers the input and output data bits together. This reduces the cable size but requires a software CLA, OTA to reset the output register which will be wire-ORd with the device-generated data bits during input operations.

Tables 3-1 and 3-2 illustrate conventional skip-on-flag-set I/O software for an interface card plugged into select code 14. On output, the Flag FF means "device is ready for data" and the device command signal means "computer has loaded the output register". On input, the device command signal means "the device should get data" and the Flag FF means "the data is now available". Notice that the computer and device roles change on input and output — on input, the computer waits and the device controls the transfer, on output, the device waits and the computer controls the transfer.

Interrupt-I/O is programmed so that the device flag signal (which is not expected for a long time, e.g., 5 msec on 200 cps papertape reader) causes a CPU interrupt. When an interrupt occurs, the CPU "fetches" the instruction in the trapcell corresponding to the interrupting interface card and "executes" it. Normally, the trapcell contains a JSB instruction, but sometimes it contains a NOP, CLC, HLT or some other instruction. For an interrupt to occur, the interrupt system must be enabled via STF 0 instruction

Table 3-1. Sample Input Program

INPUT	STC 14B,C	send device command and clear FLAG.
	SFS 14B	is FLAG set yet?
	JMP *-1	no, wait.
	LIA 14B	read input register
	OTA 1	and display on front panel.
	JMP INPUT	repeat this forever.

Table 3-2. Sample Output Program

OUTPUT	LIA 1	read switch register
	OTA 14B	store in output register on interface card
	STC 14B,C	send device command and clear FLAG
	SFS 14B	is FLAG set yet?
	JMP *-1	no, wait.
	JMP OUTPUT	repeat this forever.

(generally executed at system level rather than driver level), the Control and Flag FF's must be set, and no higher priority device can have Flag & Control set. The Control FF is "owned" by software via the STC and CLC instructions. The Flag FF can be set by a device flag signal or by software STF instruction. See Figure 3-1.

DMA-I/O is programmed by issuing the appropriate instructions to DMA (via special select codes 2, 3, 6, and 7). Once turned on DMA will intercept all device flag signals (via W10-specified SRQ signal) at a "cost" of 1 cycle-steal per flag. This method of I/O is used when the data rates are very, very high (e.g., 100's of kHz of transfer rate would steal 10's of % of computational capability), when the device requires a synchronous data transfer (e.g., disc or ADC), or when interrupt latency can not be tolerated.

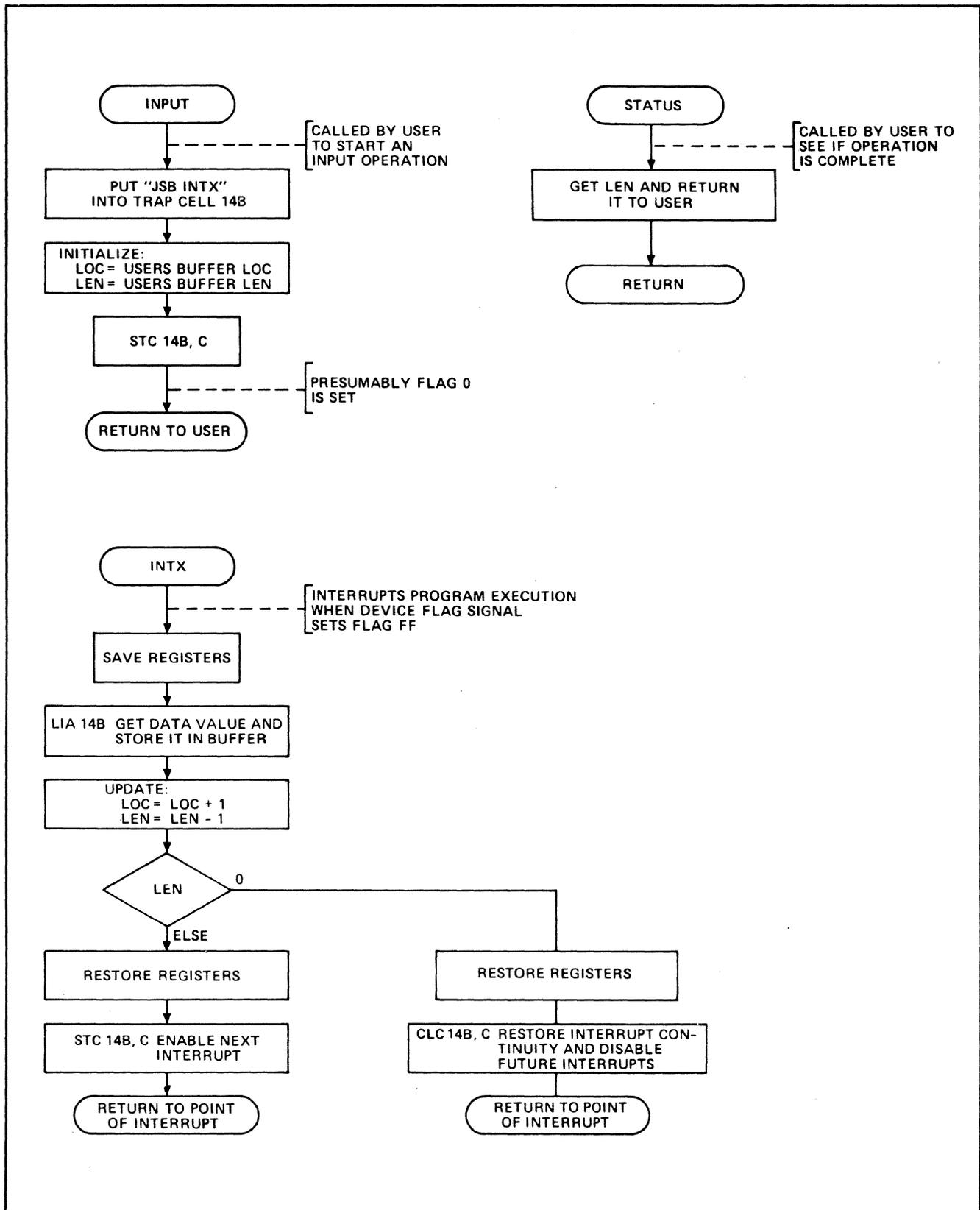
### 3-4. DUAL HANDSHAKE MODE

Two sets of device handshake lines are available on the interface card. Only one set is active at a time, this set is selected by the Mode FF. The Mode FF is reset by a CLC (or CLC 0) instruction; this enables the normal DEVCMO/DEVFLG lines and turns off the YELLOW Mode lite. (The DEVCMO and DEVFLG lines are present on a conventional 12566 microcircuit card.)

The Mode FF is set by a SFC instruction occurring when jumper W12 is used. This enables the DC2/DF2 lines and turns on the YELLOW Mode lite. The SFC instruction also performs the conventional skip-on-flag-clear task.

This selectable handshake capability might be used to handle two devices via one card (DEVCMO and DEVFLG to device 1, DC2 and DF2 to device 2, data lines to both). It might also be used to separate the "control" and "data transfer" functions of a single device (DEVCMO is used to signal "control" words on the data lines, DC2 is used to signal "data" words on the data lines) without reducing the data path to 15 bits or requiring a complicated hardware/software interface protocol. It might also be used in conjunction with the RFD input signal to talk to a device requiring a 3-wire handshake (e.g., using jumpers W2B and W3E).

Figure 3-1. Typical Software Structure for Interrupt Input  
(via select code 14B)





## SECTION IV THEORY OF OPERATION

### 4.1. INTRODUCTION

This section provides both general and detailed theory of operation for the interface. Block diagrams, Figures 1-2 and 4-1 are provided to describe the overall logic structure of the card. A flowchart, Figure 4-2, is provided to show the overall operating details of the card and the time relationships of the various signals.

### 4.2. OVERALL DESCRIPTION

The Data/Control Interface Card is used to provide a 16-bit bidirectional TTL interface between a device and a HP 21XX series Computer. It can handle transfer rates up to 1 million 16-bit words per second. Figure 1-2 shows how the Computer-generated STC instruction generates a device-visible command ( $\overline{\text{DEVCM}}\overline{\text{D}}$  or  $\overline{\text{DC}}\overline{2}$ , as selected by the MODE FF). The device perceives this signal as "output data ready" or a "request for input data", depending on its (the device's) state.

Figure 4-1 is a block diagram detailing all device interface signals, all jumper locations, all computer-generated instructions, all storage, and many test points. Each block in this diagram is characterized (roughly) by left-entry of important signals, bottom-entry of software or DMA-generated instructions, right-exit of important signals, and top-entry of timing (e.g., T2, T3, . . .) and occasional (e.g., power up POPIO) signals. The device-interface (i.e., the card's top-edge connector) comprises the 32 data lines, 2 pairs of handshake lines, and the RFD ("ready for data") and +5V lines at the left margin.

Figure 4-1 shows the general progression of the device's command signal from the STC instruction, through a W1-selected normal or delayed CMD FF into (via DCMD) the MODE-selected handshake selector and then to the device as either  $\overline{\text{DEVCM}}\overline{\text{D}}$  or  $\overline{\text{DC}}\overline{2}$ .

Figure 4-1 also shows the general progression of a MODE-selected device flag signal DFLG via W2 to clear the CMD FF and (via W3) to set the FLAGBUFFER FF and (at the next T2) to set the FLAG FF. These signals drive the three computer interfaces for DMA, interrupt, and skip-on-flag modes of transfer (the computer programmer selects one or a combination of transfer modes to suit his particular problem).

The device generally "handshakes" the command signal by returning a device flag signal ( $\overline{\text{DEVFLG}}$  for  $\overline{\text{DEVCM}}\overline{\text{D}}$  or  $\overline{\text{DF}}\overline{2}$  for  $\overline{\text{DC}}\overline{2}$ .) This resets the command FF. It also sets the FLAG FF; this act is what causes the computer (via IRQ interrupt request, via SRQ DMA request, or via SKF skip-on-flag software request) to detect completion of the handshake (and, normally, to proceed with the transfer of the next word of data).

This block diagram and the test points it suggests are the starting point to understanding the schematics and other details found in this operating and service manual.

### 4.3. FUNCTIONAL CIRCUIT DESCRIPTION

The following paragraphs describe operation of the various circuits contained on the interface card. A Mnemonics Signal Table is supplied in Section V, Table 5-3. For further information about the computer input/output system, refer to the instruction manuals supplied with the computer.

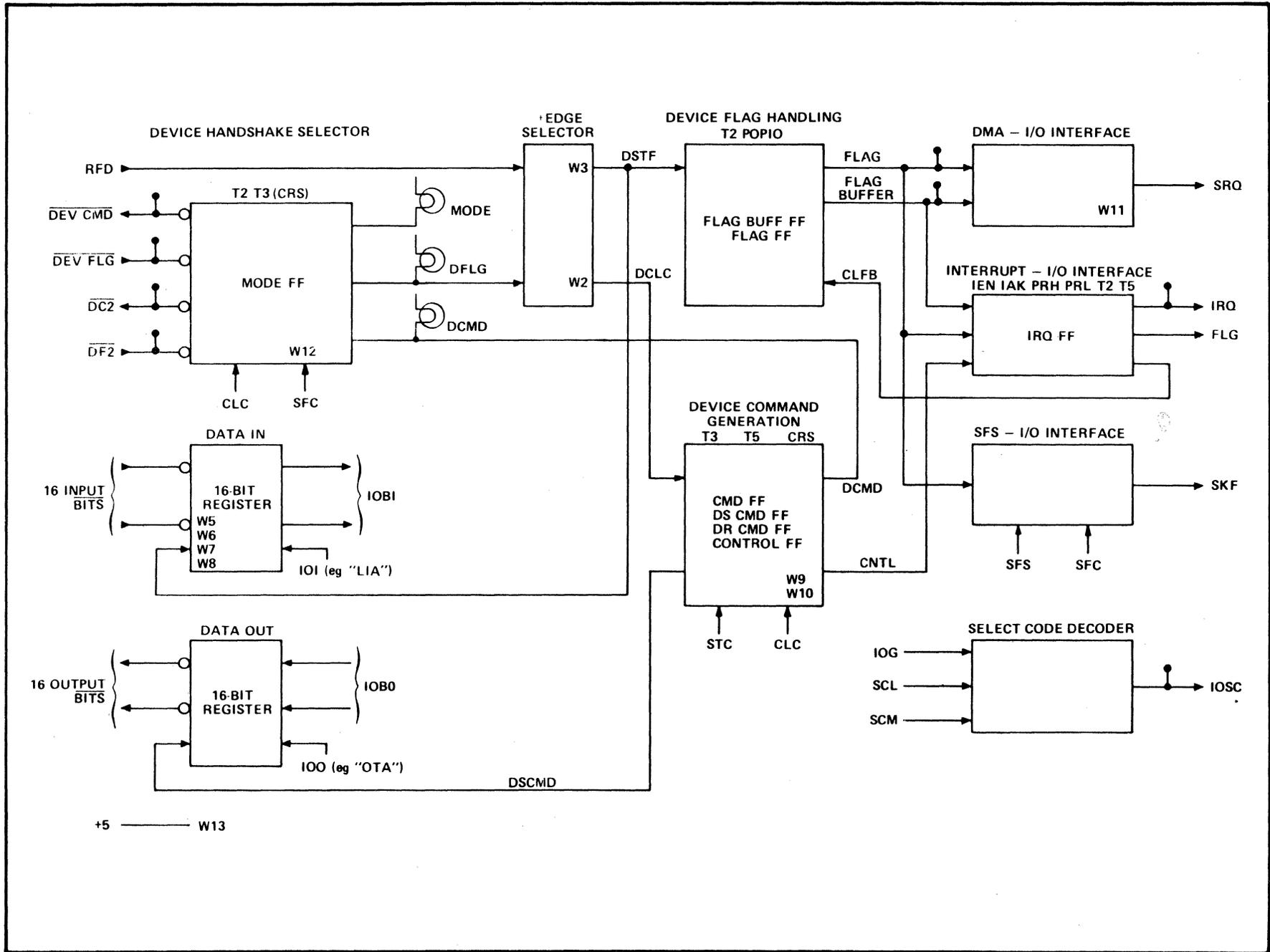


Figure 4-1. Block Diagram (Detailed)

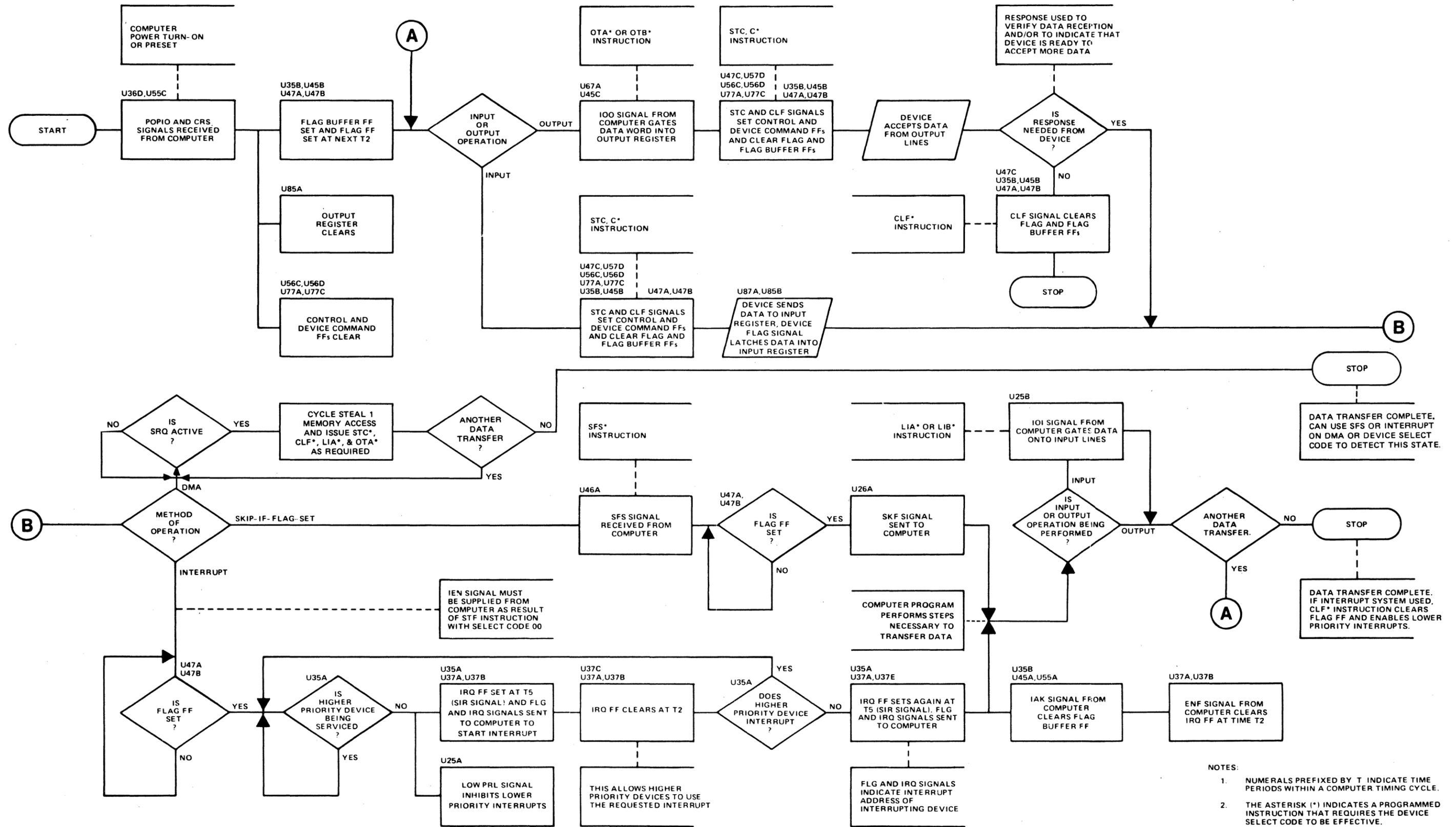


Figure 4-2. Flowchart of Operating Sequence

#### 4-4. POWER-ON AND PRESET CIRCUIT

When computer power is turned on or the PRESET switch is pressed (EXTERNAL PRESET, depending on computer model), the computer sends POPIO(B) and CRS signals to the interface card. The POPIO(B) signal is inverted and sets the Flag Buffer FF; the Flag Buffer FF sets the Flag FF at computer time T2. Inverted again to its original logic level by gate U85A, the POPIO(B) signal clocks the output register. Since the IOBO lines from the computer are low (false) during turn-on or preset, the POPIO(B) signal clears the output register. The inverted CRS signal clears both the Control and Device Command FFs.

The Mode FF, used by the device handshake selector circuit, is not reset by power-on or the PRESET switch. It requires a CLC signal supplied by software, typically a CLC 0 instruction is used when a program initially is started following power-on.

#### 4-5. DEVICE HANDSHAKE SELECTOR

The Mode FF (test point M2) is used to switch the device command and device flag signals to either the  $\overline{\text{DEVCM}}\overline{\text{D}}$  and  $\overline{\text{DEVFLG}}$  lines (when test point M2 is low), or to the  $\overline{\text{DC2}}$  and  $\overline{\text{DF2}}$  lines (when test point M2 is high). The unselected device command line is held high, the unselected device flag line is ignored.

Three lights are provided to indicate the status of the Mode FF and the enabled device command and device flag lines. The lights are "ON" when the corresponding signal is "active". Thus, red light DS1 indicates an active (low) device command; green light DS2 indicates an active (low) device flag signal, and yellow light DS3 indicates that the Mode FF is set.

The Mode FF is set by a SFC software instruction. The SFC signal is ANDed with T3 by gate U11C to avoid DMA-generated SFC glitches occurring during T6 when a cycle-steal immediately follows a SOC software instruction. The Mode FF is reset (only) by a CLC software instruction, see Paragraph 4-4. The CLC signal is delayed by U67B and U75A until T5, to insure that the device command resets before the Mode FF does.

#### 4-6. ± EDGE SELECTOR

This block accepts the DFLG signal from the device handshake selector and shapes it with a 30 ns low pass filter (comprising R61, C3, and R62, see LPFLG test point) and Schmitt Trigger U87CD.

Jumper W2 selects which edge of the device flag should trigger the DCLC one shot U86AC. Jumper W3 selects which edge of the device flag or which edge of the RFD signal should trigger the DSTF one shot.

Note that the edges sensed by this circuitry could be caused by the device (via  $\overline{\text{DEVFLG}}$ ,  $\overline{\text{DF2}}$ , or RFD) or by the software (via SFC and CLC instructions when  $\overline{\text{DEVFLG}}$  and  $\overline{\text{DF2}}$  are complementary levels). The software approach might be useful in a diagnostic program, to detect the illegal state wherein both  $\overline{\text{DEVCM}}\overline{\text{D}}$  and  $\overline{\text{DEVFLG}}$  are low (i.e., computer and device are deadlocked).

#### 4-7. DEVICE FLAG HANDLING

If the Flag FF is set when the W2-selected DSTF pulse arrives, the DSTF pulse is ignored. This could happen if the device generated a second device flag when the first had not been acknowledged by a software or DMA CLF instruction. If the Flag FF is clear, then the DSTF pulse sets the Flag Buffer FF, and, at the next T2, sets the Flag FF.

The Flag Buffer FF and Flag FF are used by the DMA, interrupt, and skip-on-flag methods of data transfer.

#### 4-8. DMA-I/O INTERFACE

Jumper W11 selects the Flag FF, Flag Buffer FF, or continuous generation of the SRQ signal. If DMA has been enabled (via the appropriate software instructions to the DMA select code), then it tests the SRQ line at the start of each T5. If SRQ is active, DMA begins a cycle-steal memory access at T6, and issues STC, CLF, instructions as appropriate.

Note that the STC is issued by DMA during T3. During an output operation however, the data is not available until T5. Thus, a device using DMA output must either delay a T3 referenced device command edge or use a T5-referenced device command edge for strobing the data into the device.

#### 4-9. INTERRUPT-I/O INTERFACE

A computer interrupt is requested by the interface card via IRQ whenever the Flag FF and Control FF are set, the interrupt system is enabled (IEN is high), and no interface card with lower select code (i.e., higher priority) is already requesting one (i.e., PRH is high). When the computer grants the interrupt, it sends IAK, which, via gate U55A, clears the Flag Buffer FF to prevent "interrupting an interrupt". Until a CLF instruction is issued by software or DMA, the Flag Buffer cannot be set again (see Paragraph 4-7), and another interrupt cannot occur.

The IRQ signal is issued at time T5. At the next T2, the IRQ FF is cleared, to allow higher-priority devices to request service. Lower priority devices are held off at this time by a low PRL signal generated by U25A. If no higher priority device requests service, PRH remains high, and, at T5, the IRQ FF sets a second time. The FLG and IRQ signals are then used to indicate the interrupt address. The PRL signal remains low until software issues a CLF signal or CLC signal; thus, lower priority device interrupts are prevented during the software interrupt subroutine.

#### 4-10. SFS-I/O INTERFACE

The computer software can test the Flag FF at any time, via the SFS and SFC instructions. They issue the SKF signal if the Flag FF is, respectively set or clear. The SFC instruction is also used, when jumper W12 is in, as described in Paragraph 4-5.

#### 4-11. DEVICE COMMAND GENERATOR

This circuitry generates the device command signal, which is selected via jumper W1 and routed to the  $\overline{\text{DEVCM}}\overline{\text{D}}$  or  $\overline{\text{DC}}\overline{2}$  lines via the device handshake selector gate U101AC. The STC signal (generated during T3 by DMA and T4 by software) sets the Command FF. The CRS signal (and if jumper W9A is used also the CLC signal) resets the Command FF. Also provided are a Delayed Set Command FF (sets at T5, resets as per jumper W10) and a Delayed Reset Command FF (resets at T5).

The Control FF is set via STC and reset via CRS or CLC. It is used only by the interrupt-I/O interface.

#### 4-12. SELECT CODE DECODER

Each I/O instruction comprises four signals — SCL and SCM select a particular interface card, IOG(B) specifies that the current instruction is an I/O instruction, and SFC, STC, CLF, etc. specify what the instruction is. Gate U54A generates the IOSC signal, which is used to qualify all the I/O instructions.

Test point IOG:SC is high whenever any I/O instruction is issued to this card by DMA or software.

#### **4-13. DATA I/O**

The two storage registers on the interface card contain 16 flip-flops each. Integrated circuits U33, U53, U73, and U93 form the output storage register; U23, U43, U63, and U83 form the input storage register.

The IOO signal from the computer, delayed by the IOO Delay FF, U67A, gates computer data from the IOBO lines into the output register. Register contents are present on the output lines to the device at all times, or gated onto the output lines, as determined by the position of jumper W4.

If jumpers W5 through W8 are disconnected, the input register always contains the data that is present on the input lines from the I/O device. If the four jumpers are connected, a Device Flag signal from the I/O device gates data into the input register. Data from the input register is gated onto the IOBI lines by an IOI signal from the computer.



## **SECTION V MAINTENANCE**

### **5-1. INTRODUCTION**

This section contains troubleshooting and diagnostic information for the interface card. Logic diagrams, component location diagrams, a list of testpoints and indicators, a mnemonic signal name table, typical waveforms, and a replaceable parts list are included.

### **5-2. PREVENTIVE MAINTENANCE**

Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no separate preventive maintenance schedules for the interface card; however, it is a good practice to remove dust and visually inspect the interface card whenever the card is removed from the computer.

### **5-3. DIAGNOSTIC TEST**

Use the General Purpose Register Diagnostic, P/N 24931-16001, to verify proper operation of the interface card. The Diagnostic Program Procedure in the Manual of Diagnostics gives operating information and jumper configuration for the diagnostic test. The flag, control, and interrupt circuits and the data storage registers are checked for proper operation when the diagnostic test is performed.

### **5-4. TROUBLESHOOTING**

Troubleshoot the interface card by performing the diagnostic test and analyzing any error halts that occur during the test. The repeat mode switch-option on the diagnostic test is particularly useful. To further isolate troubles, use the block diagram (Figure 4-1) and the list of test points and indicators (Table 5-1) in conjunction with a logic probe or oscilloscope. The edge connector pin assignments (given in Tables 2-2 and 5-2), the integrated circuit diagrams and characteristics (Figure 5-2), the parts locator (Figure 5-3) and the logic diagram (Figure 5-4) are useful, as are the theory of operation paragraphs (Section IV) associated with the malfunctioning block. Signal mneumonics are listed in Table 5-3.

Table 5-1. List of Test Points and Indicators

Yellow MODE Light	OFF indicates Mode FF is reset and the normal $\overline{\text{DEVCM}}\overline{\text{D}}$ and $\overline{\text{DEVFL}}\overline{\text{G}}$ handshake lines are being used. ON indicates the Mode FF is set and the auxiliary $\overline{\text{DC}}\overline{2}$ and $\overline{\text{DF}}\overline{2}$ handshake lines are being used.
Red CMD Light	ON indicates active (i.e., low) device command signal ( $\overline{\text{DEVCM}}\overline{\text{D}}$ or $\overline{\text{DC}}\overline{2}$ as determined by yellow MODE light). When red light is ON, the computer is waiting (for device flag).
Green FLG Light	ON indicates active (i.e., low) device flag signal ( $\overline{\text{DEVFL}}\overline{\text{G}}$ or $\overline{\text{DF}}\overline{2}$ as determined by yellow MODE light). When green light is ON, the device is waiting (for device command).
M2	Mode FF, like yellow MODE light.
$\overline{\text{DEVCM}}\overline{\text{D}}$ $\overline{\text{DEVFL}}\overline{\text{G}}$	Normal computer/device handshake signals.
$\overline{\text{DC}}\overline{2}$ $\overline{\text{DF}}\overline{2}$	Auxiliary computer/device handshake signals.
IOG·SC	High whenever any I/O instruction is issued to the interface card. Low indicates no software or DMA activity relative to the interface card.
LPFLG	Positive-true device flag signal after passing through low pass filter.
(W2)	Jumper carries ground-true $\overline{\text{DCLC}}$ signal, output from $\pm$ edge selector.
(W3)	Jumper carries ground-true $\overline{\text{DSTF}}$ signal, output from $\pm$ edge selector.
Flag Buffer FF	Flag Buffer FF.
Flag FF	Flag FF.
IEN	Interrupt System Enable signal. High unless interrupt system is disabled (via CLF 0 software instruction) or DMA is cycle-stealing.
IRQ FF	Interrupt Request FF.
IAK	Interrupt Acknowledge signal, occurs when interrupt trapcell instruction is Fetched.
T2	I/O timing periods are approximately 200 ns long and occur in T2-T3-T4-T5-T6-T2- . . . sequence whenever power is applied in the computer. The T2 signal is a good timing reference for the computer side of the computer/device interface.
Data	Input data bits (IN15-IN0) and output data bits (OUT15-OUT0) are available on labeled traces near the top card edge connector.

Figure 5-1. Typical waveforms for the 05451-60025 during dma input or output transfer. Jumpers W1A, W2B, W3B are assumed, also DEVFLG = 200 ns delayed DEVCMD.

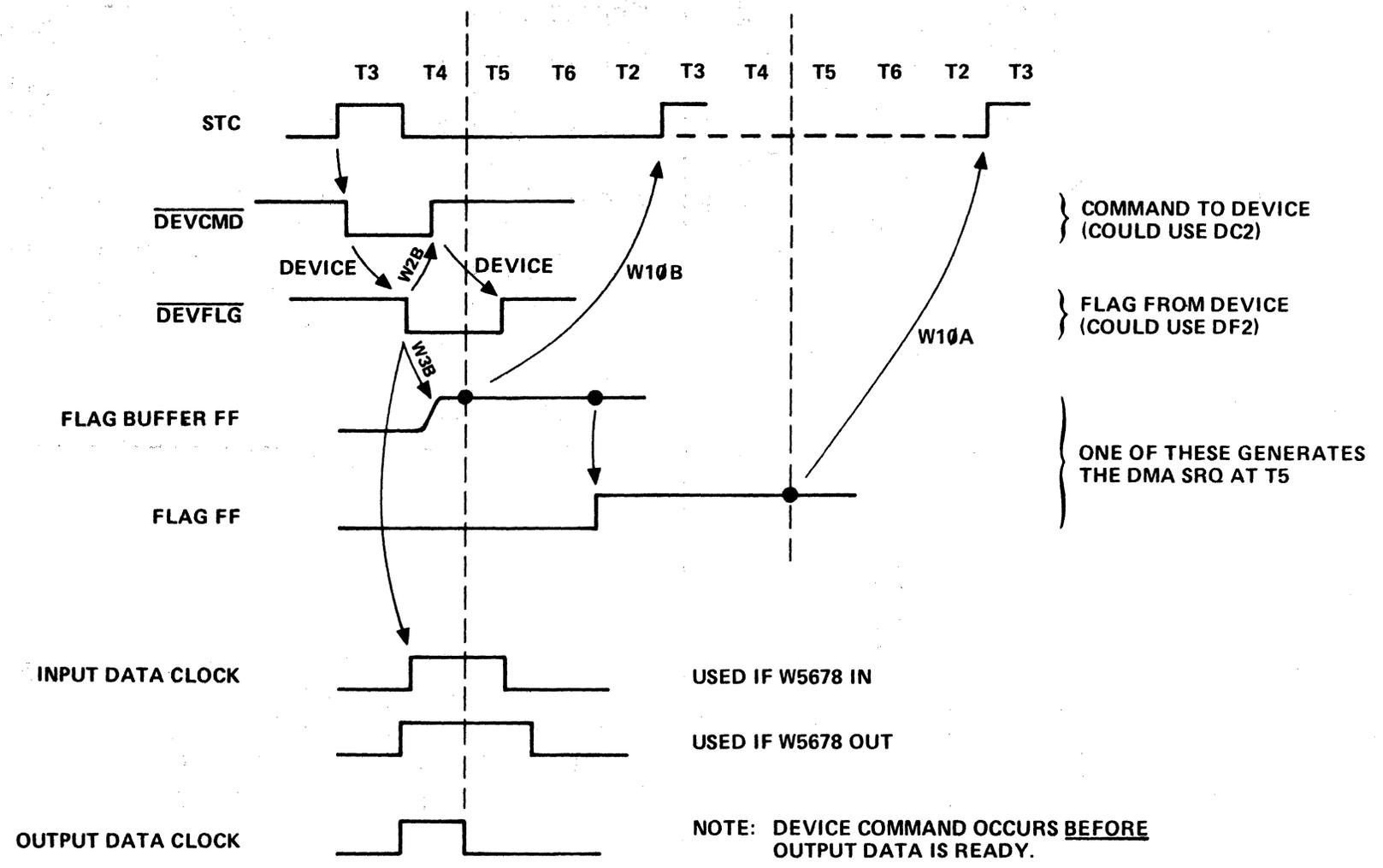
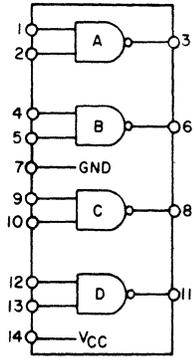
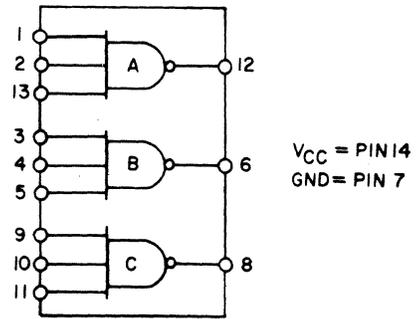


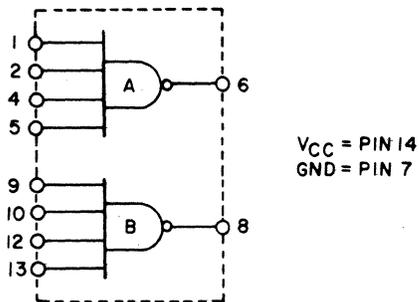
Figure 5-2. Integrated Circuit Diagrams and Characteristics



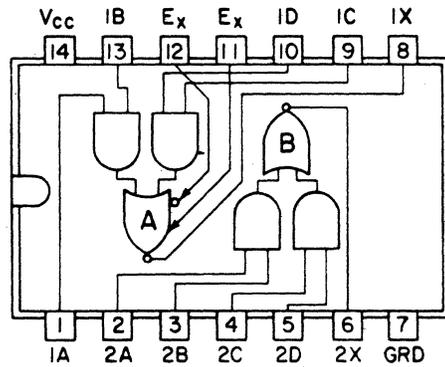
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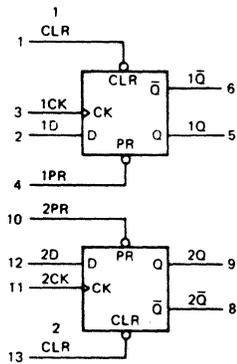
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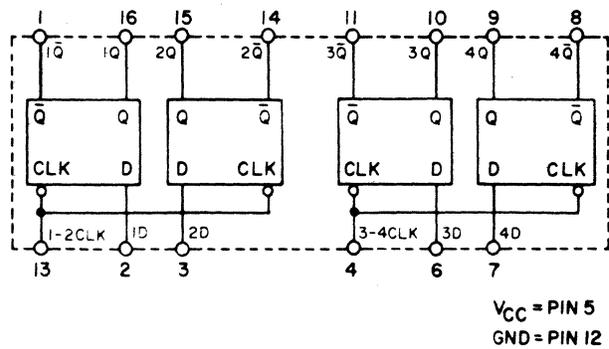
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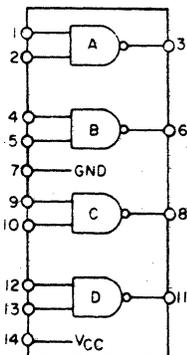
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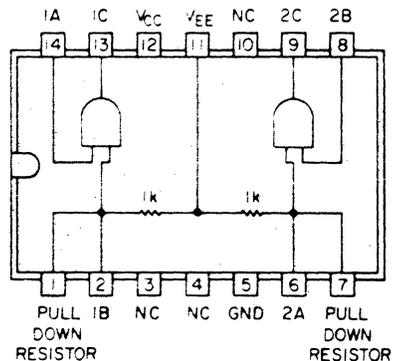
1820-0077



1820-0301



1820-0621 & 1820-0539



1820-0956

Table 5-2. 86 Pin Computer Interface Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	2	GROUND
3	PRL	4	FLG
5	SFC	6	IRQ
7	CLF	8	IEN
9	STF	10	IAK
11	T3	12	SKF
13	CRS	14	SCM
15	IOG(B)	16	SCL
17	POPIO	18	
19	SRQ	20	IOO
21	CLC	22	STC
23	PRH	24	IOI
25	SFS	26	IOB10
27	IOB18	28	IOB19
29	IOB11	30	IOB12
31	IOB110	32	T5(SIR)
33		34	
35	IOB00	36	
---		---	
37		38	IOB01
39	+4.85 V (VCC)	40	+4.85 V (VCC)
41	IOB02	42	IOB04
43		44	
45	IOB03	46	T2 (ENF)
47	-2 V (VEE)	48	-2 V (VEE)
49		50	
51	IOB05	52	IOB07
53	IOB06	54	IOB08
55	IOB011	56	IOB09
57	IOB012	58	IOB010
59		60	IOB11
61	IOB013	62	
63		64	IOB13
65	IOB114	66	
67		68	
69		70	
71		72	
73		74	IOB015
75		76	
77	IOB14	78	IOB112
79	IOB113	80	IOB115
81	IOB16	82	IOB114
83	IOB115	84	IOB17
85	GROUND	86	GROUND

Dashed line represents key slot in band.

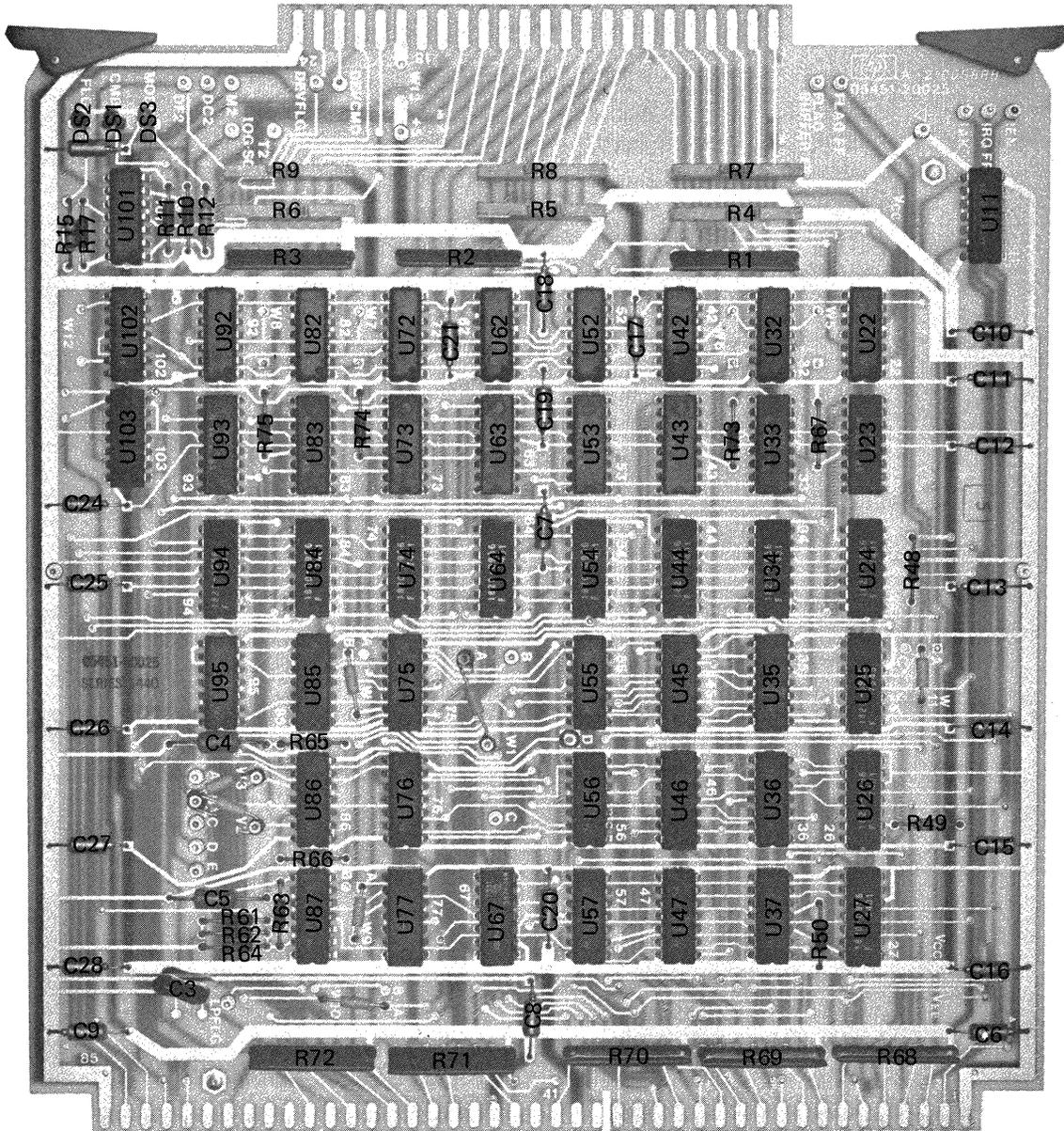
Table 5-3. Mnemonics Table (Signal Names)

<b>CLC</b>	clear control instruction
<b>CLF</b>	clear flag instruction
<b><math>\overline{\text{CLFB}}</math></b>	internal request to clear flag buffer FF generated by IAK at time of computer interrupt
<b>CRS</b>	control reset, T5 pulse train occurs while PRESET button is pushed
<b><math>\overline{\text{DC2}}</math></b>	device command (used if Mode FF is set)
<b><math>\overline{\text{DCLC}}</math></b>	internal 300ns pulse W2-jumper selects the DFLG edge to reset the command FF
<b>DCMD</b>	internal W1-jumper-selected device command which is routed to $\overline{\text{DEVCMDB}}$ or $\overline{\text{DC2}}$ as specified by Mode FF
<b>DFLG</b>	internal device flag signal, from $\overline{\text{DEVFLG}}$ or $\overline{\text{DF2}}$ as selected by Mode FF
<b><math>\overline{\text{DEVCMDB}}</math></b>	device command (used if Mode FF is clear)
<b><math>\overline{\text{DEVFLG}}</math></b>	device flag (used if Mode FF is clear)
<b><math>\overline{\text{DF2}}</math></b>	device flag (used if Mode FF is set)
<b>DRCMD</b>	delayed reset command, used with W4A
<b><math>\overline{\text{DSTF}}</math></b>	internal 300ns pulse, W3-jumper selects the DFLG edge which sets Flag Buffer FF (unless held off by Flag FF) and strobes input register via W5, 6, 7, 8-jumpers
<b>ENF(T2)</b>	enable flag (this is T2 timing signal, see T3)
<b>FLG</b>	flag (not associated with Flag FF, this signal is the same as IRQ)
<b>IAK</b>	interrupt acknowledge, occurs when trap cell instruction is 'Fetched' during interrupt
<b>IEN</b>	interrupt system enable (set by $\text{STF0}$ instruction, reset by $\text{CLF0}$ instruction)
<b><math>\overline{\text{IN0-15}}</math></b>	input data bit 0 to 15 from device
<b>IOBI0-IOBI15</b>	computer I/O bus inputs bits 0 to 15
<b>IOI</b>	I/O input strobe (caused by LIA, LIB, MIA, and MIB instructions)
<b>IOBO0-IOBO15</b>	computer I/O bus output bits 0 to 15
<b>IOO</b>	I/O output strobe (caused by OTA and OTB instructions)
<b>IOG(B)</b>	I/O group (caused by any I/O instruction to any select code)
<b>IOSC</b>	internal signal, true whenever an I/O instruction is directed to this card from any source (i.e., software or DMA)
<b>IRQ</b>	interrupt request, pulse train which occurs while card waits for computer interrupt to occur

Table 5-3. Mnemonics Table (Signal Names) (Cont.)

<b>LPFLG</b>	internal low pass filtered DFLG signal
<b>M2</b>	internal 'Q' output of Mode FF, associated with DC2 and DF2
<b>OUT<del>0</del>-15</b>	output data bits 0 to 15 to device
<b>PRH</b>	interrupt priority high, true when no higher priority (smaller select code) cards are interrupting
<b>PRL</b>	interrupt priority low, true when ok for lower priority (i.e., larger select code) I/O cards can interrupt
<b>POPIO</b>	power on preset I/O, occurs on Power-up
<b>RFD</b>	device ready for data, normally used only with devices requiring 3-wire handshake
<b>SCL</b>	select code least significant digit (IOG•SCL•SCM true only during I/O instruction to this card)
<b>SCM</b>	select code most significant digit (IOG•SCL•SCM true only during I/O instruction to this card)
<b>SFC</b>	skip if FLAG clear instruction
<b>SFS</b>	skip if FLAG set instruction
<b>SIR(T5)</b>	set interrupt request (this is timing signal T5, see T3)
<b>SKF</b>	skip flag signal to computer, response to SFS and SFC instruction
<b>SRQ</b>	service request to DMA
<b>STC</b>	set control instruction, sets Control FF and Device Command FF
<b>STF</b>	set flag instruction, sets Flag Buffer FF (which sets Flag FF)
<b>T3</b>	computer timing signal (pattern T2-T3-T4-T5-T6-T2, etc. occurs whenever computer is applied)

Figure 5-3. Data/Control Interface Card Component Locator



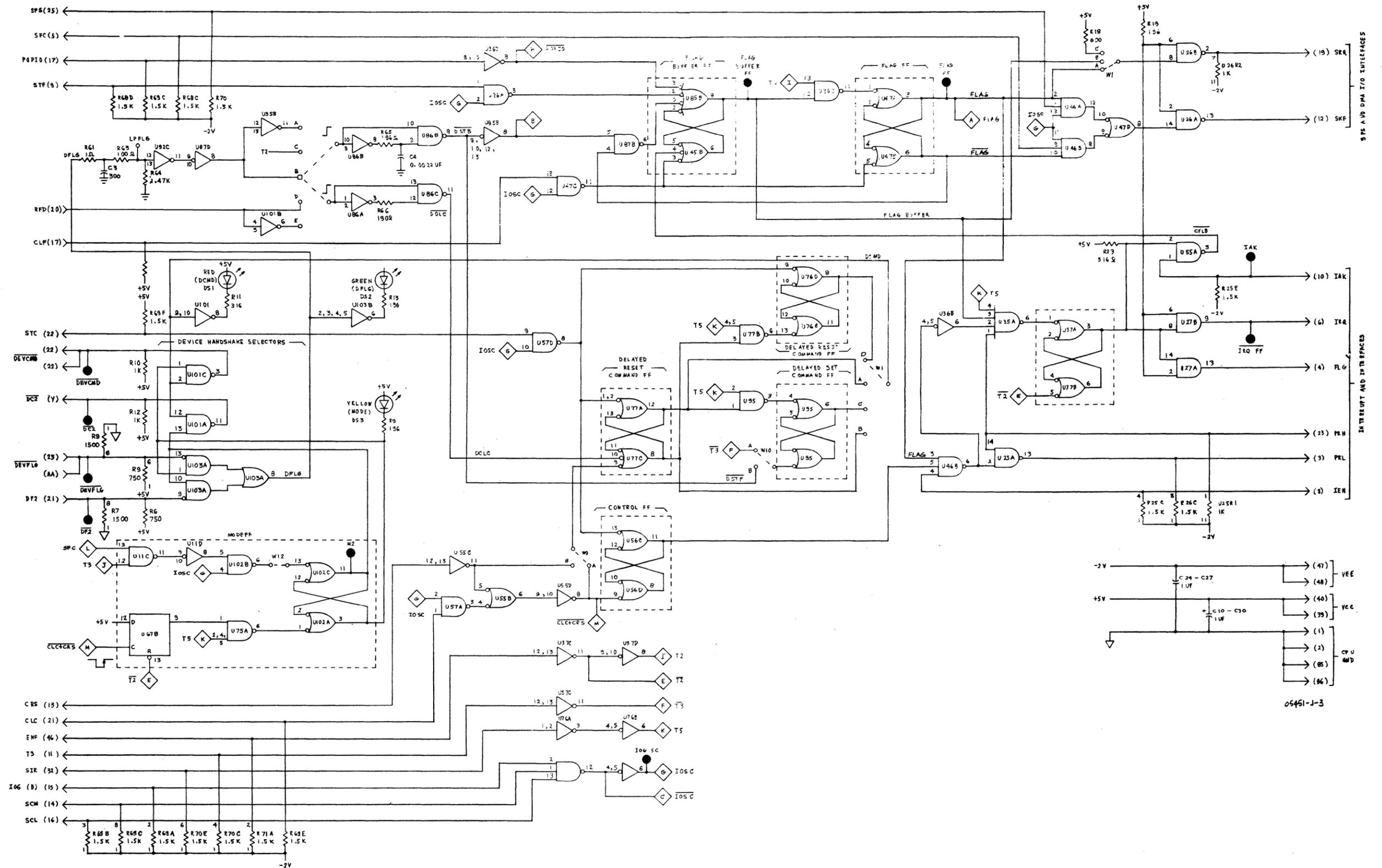


Figure 5-4. Data/Control Interface Card Logic Diagram (Sheet 1 of 2)



## **SECTION VI REPLACEABLE PARTS**

### **6-1. INTRODUCTION**

This section contains information for ordering replacement parts for both interface cards. Table 6-1 lists the following for each part.

- a. Description of the part. (Refer to Table 6-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)
- b. Typical manufacturer of the part in a five-digit code; refer to the list of manufacturers in Table 6-3.
- c. Manufacturer's part number.
- d. Reference designator used in the Component Locator and Schematic Diagram.

### **6-2. ORDERING INFORMATION**

To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the back of this manual for addresses.) Specify the following information for each part ordered:

- a. Interface card model number.
- b. Circuit card revision number.
- c. Hewlett-Packard part number.
- d. Description of each part.
- e. Circuit reference designation.

Table 6-1. Interface Card 05451-60025, Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR. CODE	MFR. PART NO.
C3	0140-0225	Capacitor, Fxd, My, 300 pF, 10%, 200 VDCW	28480	0140-0225
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
C6 thru C30	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X-9035A2
R1,R2,R3	1810-0030	Resistor Network, 7 x 1K	28480	1810-0030
R4,R5,R6	1810-0123	Resistor Network, 7 x 750	28480	1810-0123
R7,R8,R9	1810-0075	Resistor Network, 7 x 330	28480	1810-0075
R48	0757-1100	Resistor, Fxd, Flm, 600	24546	C4-1/8-TO-601-F
R46,47,63	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R11,50	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R49,65,66,12,13	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor, Network (7 fxd flm resistors)	28480	1810-0020
U22,36,37,42,47,55,56,57,62,76,82,86,87,96,102,11	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U23,33,43,53,63,73,83,93	1820-0301	Integrated Circuit, TTL	01295	SN7475N
U24 thru U27,34,44,54,64,74,84,94	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U32,52,72,92,101 (05451-60025)	1820-0621	Integrated Circuit, TTL	01295	SN7438N
U35	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U45,46,77	1820-0068	Integrated Circuit, TTL	12040	SN7410N
U67	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U75,85	1820-0071	Integrated Circuit, TTL	01295	SN7440N
U103	1820-0072	Integrated Circuit, TTL	01295	SN7450N
U101 (05427-60001)	1820-0539	Integrated Circuit, TTL	01295	SN7437N
DS1	1990-0486	Diode, Light-Emitting, Red	28480	1990-0486
DS2	1990-0485	Diode, Light-Emitting, Green	28480	1990-0485
DS3	1990-0487	Diode, Light-Emitting, Yellow	28480	1990-0487
W1 thru W13	8159-0005	Jumper Wire	28480	8159-0005

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS		
<p><b>A</b> = assembly  <b>B</b> = motor, synchro  <b>BT</b> = battery  <b>C</b> = capacitor  <b>CB</b> = circuit breaker  <b>CR</b> = diode  <b>DL</b> = delay line  <b>DS</b> = indicator  <b>E</b> = Misc electrical parts  <b>F</b> = fuse  <b>FL</b> = filter  <b>J</b> = receptacle connector</p>	<p><b>K</b> = relay  <b>L</b> = inductor  <b>M</b> = meter  <b>MC</b> = microcircuit  <b>P</b> = plug connector  <b>Q</b> = semiconductor device other than diode or microcircuit    <b>R</b> = resistor  <b>RT</b> = thermistor  <b>S</b> = switch  <b>T</b> = transformer</p>	<p><b>TB</b> = terminal board  <b>TP</b> = test point  <b>U</b> = integrated circuit, non-repairable assembly  <b>V</b> = vacuum tube, photocell, etc.  <b>VR</b> = voltage regulator  <b>W</b> = cable, jumper  <b>X</b> = socket  <b>Y</b> = crystal  <b>Z</b> = tuned cavity, network</p>
ABBREVIATIONS		
<p><b>A</b> = amperes  <b>ac</b> = alternating current  <b>ad</b> = anode  <b>Al</b> = aluminum  <b>AR</b> = as required  <b>adj</b> = adjust  <b>assy</b> = assembly    <b>B</b> = base  <b>bp</b> = bandpass  <b>blk</b> = black  <b>blu</b> = blue  <b>brn</b> = brown  <b>brs</b> = brass  <b>Btu</b> = British thermal unit  <b>Be Cu</b> = beryllium copper    <b>C</b> = collector  <b>cw</b> = clockwise  <b>ccw</b> = counterclockwise  <b>cer</b> = ceramic  <b>cmo</b> = cabinet mount only  <b>com</b> = common  <b>crt</b> = cathode-ray tube  <b>CTL</b> = complementary-transistor logic    <b>cath</b> = cathode  <b>cd pl</b> = cadmium plate  <b>Comp</b> = composition  <b>conn</b> = connector  <b>compl</b> = complete    <b>dc</b> = direct current  <b>dr</b> = drive  <b>DTL</b> = diode-transistor logic  <b>depc</b> = deposited carbon  <b>dpdt</b> = double-pole, double-throw  <b>dpst</b> = double-pole, single-throw    <b>E</b> = emitter  <b>ECL</b> = emitter-coupled logic  <b>ext</b> = external  <b>encap</b> = encapsulated  <b>elctlt</b> = electrolytic    <b>F</b> = farads  <b>FF</b> = flip-flop  <b>flh</b> = flat head  <b>Fim</b> = film  <b>Fxd</b> = fixed  <b>filh</b> = fillister head    <b>G</b> = giga (10<sup>9</sup>)  <b>Ge</b> = germanium  <b>gl</b> = glass  <b>gnd</b> = ground(ed)</p>	<p><b>gra</b> = gray  <b>grn</b> = green    <b>H</b> = henries  <b>Hg</b> = mercury  <b>hr</b> = hour(s)  <b>Hz</b> = hertz  <b>hdw</b> = hardware  <b>hex</b> = hexagon, hexagonal    <b>ID</b> = inside diameter  <b>IF</b> = intermediate frequency  <b>in.</b> = inch, inches  <b>I/O</b> = input/output  <b>int</b> = internal  <b>incl</b> = include(s)  <b>insul</b> = insulation, insulated  <b>impgrg</b> = impregnated  <b>incand</b> = incandescent    <b>k</b> = kilo (10<sup>3</sup>), kilohm    <b>lp</b> = low pass    <b>m</b> = milli (10<sup>-3</sup>)  <b>M</b> = mega (10<sup>6</sup>), megohm  <b>My</b> = Mylar  <b>mfr</b> = manufacturer  <b>mom</b> = momentary  <b>mtg</b> = mounting  <b>misc</b> = miscellaneous  <b>Met Ox</b> = metal oxide  <b>mintr</b> = miniature    <b>n</b> = nano (10<sup>-9</sup>)  <b>n.c.</b> = normally closed or no connection    <b>Ne</b> = neon  <b>no.</b> = number  <b>n.o.</b> = normally open  <b>np.</b> = nickel plated  <b>NPN</b> = negative-positive-negative  <b>NPO</b> = negative-positive zero (zero temperature coefficient)  <b>NSR</b> = not separately replaceable  <b>NRFR</b> = not recommended for field replacement    <b>OD</b> = outside diameter  <b>OBD</b> = order by description  <b>orn</b> = orange  <b>ovh</b> = oval head  <b>oxd</b> = oxide    <b>p</b> = pico (10<sup>-12</sup>)  <b>PC</b> = printed circuit</p>	<p><b>ph</b> = Phillips head  <b>pk</b> = peak  <b>p-p</b> = peak-to-peak  <b>pt</b> = point  <b>PIV</b> = peak inverse voltage  <b>PNP</b> = positive-negative-positive  <b>PWV</b> = peak working voltage  <b>porc</b> = porcelain  <b>posn</b> = position(s)  <b>pozi</b> = pozidrive    <b>rf</b> = radio frequency  <b>rdh</b> = round head  <b>rmo</b> = rack mount only  <b>rms</b> = root-mean-square  <b>RWV</b> = reverse working voltage  <b>rect</b> = rectifier  <b>r/min</b> = revolutions per minute  <b>RTL</b> = resistor-transistor logic    <b>s</b> = second  <b>SB</b> = slow blow  <b>Se</b> = selenium  <b>Si</b> = silicon  <b>scr</b> = silicon controlled rectifier  <b>sil</b> = silver  <b>sst</b> = stainless steel  <b>stl</b> = steel  <b>spcl</b> = special  <b>spdt</b> = single-pole, double throw  <b>spst</b> = single-pole, single-throw  <b>semicond</b> = semiconductor    <b>Ta</b> = tantalum  <b>td</b> = time delay  <b>Ti</b> = titanium  <b>tgl</b> = toggle  <b>thd</b> = thread  <b>tol</b> = tolerance  <b>TTL</b> = transistor transistor logic    <b>U(μ)</b> = micro (10<sup>-6</sup>)    <b>V</b> = volt(s)  <b>var</b> = variable  <b>vio</b> = violet  <b>VDCW</b> = direct current working volts    <b>W</b> = watts  <b>WW</b> = wirewound  <b>wht</b> = white  <b>WIV</b> = working inverse voltage    <b>yel</b> = yellow</p>

*Table 6-3. Code List of Manufacturers*

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2 and the latest supplements.					
Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
01295	Texas Instruments, Inc., Transistor Products Div. . . . .	Dallas, Texas	14674	Corning Glass Works . . . . .	Corning, N.Y.
04713	Motorola Inc., Semiconductor Products Div. . . . .	Phoenix, Arizona	19701	Electra Mfg. Co. . . . .	Independence, Kan.
07263	Fairchild Camera & Inst. Corp., Semiconductor Div. . . . .	Mountain View, Ca.	24546	Corning Glass Works . . . . .	Bradford, Pa.
			28480	Hewlett-Packard Co. . . . .	Palo Alto, Ca.
			56289	Sprague Electric Co. .	North Adams, Mass.