User's Guide

HP Debug User Interface

for SH7040/50 Series

Notice

Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Hewlett-Packard assumes no responsibility for the use or reliability of its software on equipment that is not furnished by Hewlett-Packard.

Hewlett-Packard
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901-2197, U.S.A.

Printing History

New editions are complete revisions of the manual. The date on the title page changes only when a new edition is published.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual was issued. Many product updates and fixes do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual revisions.

Edition 1 B3755-97000, November 1996

Edition 2 B3755-97001, March 1997

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Warranty

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round-trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country. HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environment specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

Exclusive Remedies

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific **WARNINGS** elsewhere in this manual may impair the protection provided by the equipment. In addition it violates safety standards of design, manufacture, and intended use of the instrument.
The Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

Do Not Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify Instrument

Because of the danger of introducing additional hazards, do not install substitute parts or perform unauthorized modifications to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting this instrument.

Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

Instruction manual symbol: The product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

Alternating current.

Direct current.

On (Supply).

Off (Supply).

Frame (or chassis) terminal. A connection to the frame (chassis) of the equipment which normally include all exposed metal structures.

Warning

This Warning sign denotes a hazard. It calls your attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution

This Caution sign denotes a hazard. It calls your attention to a operating procedure, practice, condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

Note denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

In This Book

The HP B3755A/56A Debug User Interface, which is used with the HP E3472/73A Emulator, is a high-level language debugger for the Hitachi SH7040 Series.

This book describes processor-specific functions and usage of the HP B3755A/56A Debug User Interface.

For common functions and usage of the HP Debug User Interface, refer to the *HP Debug User Interface User's Guide*.

For installation of the HP Debug User Interface, refer to the *HP Debug User Interface Installation Guide*.

For installation of the HP E3472/73A Emulator, refer to the *HP E3472/73A Emulator User's Guide*.

Note

Contents

1

Connecting the Target System

Connecting the Target System

This chapter shows you how to connect the emulator to your target system.

Overview

To connect the HP E3472/73A Emulator and the target system, the **QFP cable** and the **QFP socket/adapter** (attached to the QFP cable products) are used.

Caution

To prevent the emulator and the target system from being damaged, be sure to follow the cautions below when handling them.

- **To prevent damage by static discharge, use the emulator in a place resistant to static electricity.**
- **Be sure to turn off the emulator and the target system before connecting them.**
- **Be sure that orientation of each connector is right.**
- **Check that the ground line of the emulator and that of the target system are properly connected.**
- **When turning the system on, switch on the target system first and then the emulator.**
- **When turning the system off, switch off the emulator first then the target system.**

Note

Refer to "Logic Analyzer" in Chapter 5 for connecting the HP E3472/73A and the logic analyzer in detail.

The **QFP cable** is a cable assembly to connect the PGA adapter to the QFP socket/adapter on the target system. Use one of the following QFP cables.
For the HP E3472A SH7040 Emulator, use the QFP cable shown below.

Table 1-1. Supported Processors of Each QFP Cable (SH7040 Series)

Processor	Package (Pitch)	QFP Cable
SH7040/42/44	QFP-112 (.65 mm)	**HP E3472B**
SH7041/43/45	QFP-144 (.5 mm)	**HP E3472C**

For the HP E3473A SH7050 Emulator, use the QFP cable shown below.

Table 1-2. Supported Processors of Each QFP Cable (SH7050 Series)

Processor	Package (Pitch)	QFP Cable
SH7050/51	QFP-168 (.65 mm)	**HP E3473B**

The **QFP socket/adapter** is a part to adapt the the QFP cable to the target system. You must solder this part to your target system. The QFP socket/adapter can be used as a "socket" to mount a real processor. The following QFP socket/adapters are provided.

For the HP E3472A SH7040 Emulator, use the QFP socket/adapter shown below.

Table 1-3. QFP Socket/Adapters (SH7040 Series)

Processor	Package (Pitch)	QFP Socket/Adapter
SH7040/42/44	QFP-112 (.65 mm)	**HP E3472-61620**
SH7041/43/45	QFP-144 (.5 mm)	**HP E3472-61621**

Note

When mounting a real processor on the QFP socket/adapter **HP E3472-61621** , the socket cap **HP E3472-61631** is required.

For the HP E3473A SH7050 Emulator, use the QFP socket/adapter shown below.

Table 1-4. QFP Socket/Adapters (SH7050 Series)

Processor	Package (Pitch)	QFP Socket/Adapter
SH7050/51	QFP-168 (.65 mm)	**HP E3473-61620**

Note

When mounting a real processor on the QFP socket/adapter **HP E3473-61621**, the socket cap **HP E3473-61630** is required.

To connect the target system,

1. Verify both the emulator and the target system are turned off.
2. Solder the QFP socket/adapter to the target system.
3. Attach the QFP cable to the emulation probe.
4. Align pin #1 of the QFP cable and the QFP socket/adapter, then fix them with four screws.
5. Turn on the target system and then the emulator.

Caution

Do not apply excessive force to the QFP cable. It may cause damage to the QFP cable, the QFP socket/adapter and the target system.

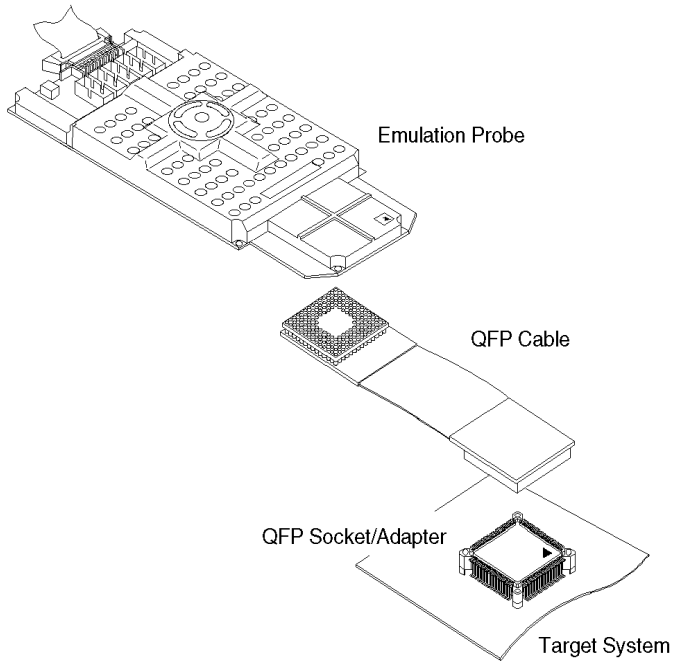

Figure 1-1. Connecting the Target System

2

Configuring the Emulator

Configuring the Emulator

This chapter shows you how to set the following items to configure the emulator.

- Hardware Options
- Memory Map

Hardware Options

The emulator can be configured to suit developments of various target systems and user programs by setting the hardware options.
The HP E3472/73A Emulator has the following hardware options.

- **Processor Clock Mode**
- **Restrict to Real Time**
- **Set Breakpoints at Delay Slot**
- **PE13/TIOC4B/MRES Pin Function** (SH7040)
- **Quick-Break Mode**
- **Processor Type**
- **Processor Operation Mode**
- **Stack Pointer Reset Value**

Setting the Hardware Options

To set the hardware options,

1. Choose **Settings→Configuration→Hardware...** (Alt, S, C, H) from the control menu of the Debug window.
2. Set the hardware options using the Emulator Configuration dialog box.
3. Click the OK button.

Note Set the hardware options prior to setting the memory map.

Note In the Emulator Configuration dialog box, the option button checked means **Yes**, the option button not checked means **No**.

Note Setting the hardware options will drive the emulator into a reset state.

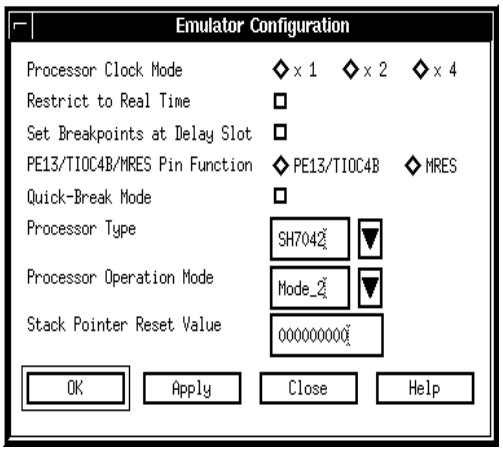

Figure 2-1. Emulator Configuration Dialog Box

Processor Clock Mode

This option allows you to select the clock mode of the emulation processor.

x1 Multiply the input clock frequency from the target system by one, and use it as the internal clock.

x2 Multiply the input clock frequency from the target system by two, and use it as the internal clock.

x4 Multiply the input clock frequency from the target system by four, and use it as the internal clock.

Note

The emulator ignores the MD3 to MD0 inputs, and uses this option setting instead.

Restrict to Real Time

The emulator has to break to the monitor to access processor registers and target memory. While running the user program, this break is done implicitly and called "temporary break".

With temporary breaks, the user program cannot be executed in real time. This may cause unexpected result if your target system circuitry is dependent on constant execution time of the program code.

This option allows you to select whether the emulator is restricted to real-time runs.

Yes The emulator is restricted to real-time runs.

While running the user program, all commands that cause a temporary break are refused. The user program is guaranteed to be executed in real time.

Commands to display/modify registers and target memory are not allowed when the emulator is running the user program. However, you can still execute the run control commands such as reset, break, run, step.

No The emulator is not restricted to real-time runs.

All commands, regardless of whether or not they require a break to the monitor, are accepted by the emulator.

Set Breakpoints at Delay Slot

A breakpoint at delay slot causes slot invalid instruction exception when it is hit during user program execution.

This option allows you to allow/prohibit setting a breakpoint at delay slot.

Yes Allows you to set a breakpoint at delay slot.

No Prohibits you from setting a breakpoint at delay slot. Normally, select this option.

When setting a breakpoint at delay slot is prohibited, the emulator checks if the instruction before the requested breakpoint address is a delayed branch or not. For a delayed branch, the emulator will not set the breakpoint, recognizing it an invalid setting.

Note that it cannot be evaluated if the code checked is an instruction or data. Therefore, if data immediately in front of the requested breakpoint address is the same code as a delayed branch, setting a breakpoint will fail. In such cases, select **Yes**.

PE13/TIOC4B/MRES Pin Function

This option is available for the HP E3472A SH7040 Emulator only, and allows you to select the function of the PE13/TIOC4B/MRES pin.

PE13/TIOC4B Select this option when the PE13/TIOC4B/$\overline{\text{MRES}}$ pin is used as PE13 or TIOC4B in your target system, Select this option also when the pin is not used.

MRES Select this option when the PE13/TIOC4B/$\overline{\text{MRES}}$ pin is used as MRES in your target system.

Note

This option is set to control the operation of the emulator in a manual-reset state.

Note that it does not set the PE13 mode bit (PE13MD) in the port E control register 1 (PECR1). Set the PE13MD with user programs or manually, in the same manner for other registers.

Quick-Break Mode

This option allows you to select whether the emulator does "quick" temporary break to access processor registers and target memory while running the user program.

Yes Quick-break is used for a temporary break to the monitor.

Monitor execution period in the quick-break mode is shortened to several tens of microseconds or several hundred microseconds, while that in the normal break mode is several milliseconds or several tens of milliseconds.

While running the monitor, the emulator responds to no interrupts. Try this setting to eliminate a problem caused by interrupt response time during program execution.

No Quick-break is not used for a temporary break to the monitor.

Note

While running the monitor, the emulator responds to no interrupts.
The emulator suspends interrupt requests in the monitor; the requests will be serviced upon return to the user program.

Processor Type

This option allows you to select the emulation processor.

For HP E3472A SH7040 Emulator, one of the following processors can be specified:

SH7040 The emulator emulates the SH7040.

SH7041 The emulator emulates the SH7041.

SH7042 The emulator emulates the SH7042.

SH7043 The emulator emulates the SH7043.

SH7044 The emulator emulates the SH7044.

SH7045 The emulator emulates the SH7045.

For HP E3473A SH7050 Emulator, one of the following processors can be specified:

SH7050 The emulator emulates the SH7050.

SH7051 The emulator emulates the SH7051.

Processor Operation Mode

This option allows you to select the processor operation mode.

Mode_0 The emulator operates in mode 0.

Mode_1 The emulator operates in mode 1.

Mode_2 The emulator operates in mode 2.

Mode_3 The emulator operates in mode 3.

Note

The emulator ignores the MD3 to MD0 inputs, and uses this option setting instead.

Stack Pointer Reset Value

This option allows you to specify the value that the stack pointer (SP, R15) is set to when the monitor is entered after emulation reset.

The stack pointer must be set to a 32-bit address and take a value multiple of 4. Normally, specify the default value of the user program.

Memory Map

The HP E3472/73A Emulator enables you to map memory for the external memory space of the processor.

Operation of the on-chip resources, including on-chip ROM/RAM and on-chip peripheral module registers, does not depend on the memory map.

Note

The memory map cannot be defined when emulating mode 3, in which no external memory space is assumed.

The external memory area is divided into blocks called a map block. The map block divisions differ depending on the processor operation mode, as shown in the following tables.

Table 2-1. Map block for Mode 0 and 1

Area	Address	Size
CS0 Space	**00000000..0001ffff**	128 kB
	00020000..0003ffff	128 kB
	00040000..0005ffff	128 kB
	00060000..0007ffff	128 kB
	00080000..0009ffff	128 kB
	000a0000..000bffff	128 kB
	000c0000..000dffff	128 kB
	000e0000..000fffff	128 kB
	00100000..0011ffff	128 kB
	00120000..0013ffff	128 kB
	00140000..0015ffff	128 kB
	00160000..0017ffff	128 kB
	00180000..0019ffff	128 kB
	001a0000..001bffff	128 kB
	001c0000..001dffff	128 kB
	001e0000..001fffff	128 kB
	00200000..002fffff	1 MB
	00300000..003fffff	1 MB

Table 2-1. Map block for Mode 0 and 1 (Continued)

Area	Address	Size
CS1 Space	**00400000..004fffff**	1 MB
	00500000..005fffff	1 MB
	00600000..006fffff	1 MB
	00700000..007fffff	1 MB
CS2 Space	**00800000..008fffff**	1 MB
	00900000..009fffff	1 MB
	00a00000..00afffff	1 MB
	00b00000..00bfffff	1 MB
CS3 Space	**00c00000..00dfffff**	2 MB
	00e00000..00ffffff	2 MB
DRAM Space (SH7040)	**01000000..013fffff**	4 MB
	01400000..017fffff	4 MB
	01800000..01bfffff	4 MB
	01c00000..01ffffff	4 MB

Table 2-2. Map block for Mode 2

Area	Address	Size
CS0 Space	**00200000..0021ffff**	128 kB
	00220000..0023ffff	128 kB
	00240000..0025ffff	128 kB
	00260000..0027ffff	128 kB
	00280000..0029ffff	128 kB
	002a0000..002bffff	128 kB
	002c0000..002dffff	128 kB
	002e0000..002fffff	128 kB
	00300000..0031ffff	128 kB
	00320000..0033ffff	128 kB
	00340000..0035ffff	128 kB
	00360000..0037ffff	128 kB
	00380000..0039ffff	128 kB
	003a0000..003bffff	128 kB
	003c0000..003dffff	128 kB
	003e0000..003fffff	128 kB
CS1 Space	**00400000..004fffff**	1 MB
	00500000..005fffff	1 MB
	00600000..006fffff	1 MB
	00700000..007fffff	1 MB

Table 2-2. Map block for Mode 2 (Continued)

Area	Address	Size
CS2 Space	**00800000..008fffff**	1 MB
	00900000..009fffff	1 MB
	00a00000..00afffff	1 MB
	00b00000..00bfffff	1 MB
CS3 Space	**00c00000..00dfffff**	2 MB
	00e00000..00ffffff	2 MB
DRAM Space (SH7040)	**01000000..013fffff**	4 MB
	01400000..017fffff	4 MB
	01800000..01bfffff	4 MB
	01c00000..01ffffff	4 MB

You can specify only one memory type for each map block.

If you map part of a map block as the emulation memory and want to use the remaining area, map the area as the same memory type. Operation of the emulator is not unpredictable when an access occurs to the remaining area which is not mapped.

The memory mapper allows you to define up to 16 different map terms. You can specify one of the following memory types to each map term.

eram Emulation RAM.

This area operates as read/write emulation memory. The minimum size of each map is 1k bytes.

erom Emulation ROM.

This area operates as read only emulation memory. The minimum size of each map is 1k bytes. When the user program writes to this area, the data is not written and the emulator will break to the monitor.

tram Target RAM.

This area operates as read/write target memory. The map term to this area can be specified with a map block as a unit.

trom Target ROM.

This area operates as read only target memory. The map term to this area can be specified with a map block as a unit. The emulator will break to the monitor when the user program writes to this area.

grd Guarded memory.

This area operates as an access-prohibited area. The map term to this area can be specified with a map block as a unit. When the user program attempts to access to this area, the emulator breaks to the monitor. Access with emulator commands are also prohibited.

The memory type of other area (area of no map terms defined) can be defaulted to **tram**, **trom**, or **grd**.

Note The target system cannot perform direct memory access to the emulation memory.

Note Single address mode transfer to the emulation memory by internal DMAC is not allowed.

Setting the Memory Map

To set the memory map,

1 Choose **Settings→Configuration→Memory Map...** (Alt, S, C, M) from the control menu of the Debug window.

2 Set the memory map using the Memory Map dialog box.

- **Setting a map term**

  1. Specify an area to the Address Range text box.

  Format: <*start address*>..<*end address*>

  2. Select a memory type in the Attribute option box.
  3. Click the Apply button.

- **Deleting a map term**

  1. Select a map term in the Map Term list box.
  2. Click the Delete button.

- **Deleting all map terms**

  1. Click the Del.All button.

- **Setting a memory type of other area**

  1. Select a memory type in the Other option box.

3 Click the Close button.

Note Set the hardware options prior to setting the memory map.

Note Setting the memory map will drive the emulator into a reset state.

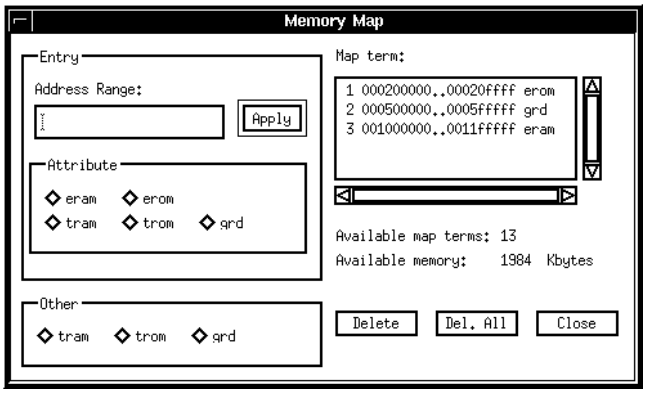

Figure 2-2. Memory Map Dialog Box

On-Chip ROM

The on-chip ROM is mapped automatically as the memory dedicated for the on-chip ROM regardless of the memory map settings. Mapping to this area will result in an error.

When the user program writes to this area, the data is not written and the emulator will break to the monitor.

On-Chip RAM

The on-chip RAM is mapped automatically as the memory dedicated for the on-chip RAM regardless of the memory map settings. Mapping to this area will result in an error.

On-Chip Peripheral Module Registers

The on-chip peripheral module registers work as the on-chip peripheral module registers regardless of the memory map settings. You don't have to map this area. Mapping to this area will result in an error.

Configuration Commands

You can also configure the emulator by configuration files or command files. The HP B3755A/56A Debug User Interface has the following configuration commands. Case is not significant in both commands and parameters.

Note The hardware option commands should appear followed by the the memory map commands.

Note The memory map cannot be defined when emulating mode 3, in which no external memory space is assumed. Thus, the memory map command cannot be used.

Note The hardware option commands and the memory map commands must be placed between its own start and end commands.

Table 2-3. Configuration Commands

Command	Parameter 1	Parameter 2	Operation
config	start		Start of Hardware Option Commands
config	rrt	enable | disable	Restrict to Real Time
config	bpds	enable | disable	Set Breakpoints at Delay Slot
config	mrst	enable | disable	PE13/TIOC4B/MRES Pin Function (SH7040)
config	qbrk	enable | disable	Quick-Break Mode
config	chip	<*processor type*>	Processor Type
config	mode	<*mode number*>	Processor Clock / Operation Modes
config	rsp	<*sp value*>	Stack Pointer Reset Value
config	end		End of Hardware Option Commands
map	start		Start of Memory Map Commands
map	<*map range*>	<*memory type*>	Setting Map Term
map	other	<*memory type*>	Setting Memory Type of Other Area
map	end		End of Memory Map Commands

enable | disable Specify **`enable`** when **Yes**, **`disable`** when **No**.

<*processor type*> Specify one of the following emulation processors.

For HP E3472A SH7040 Emulator,

- **SH7040**
- **SH7041**
- **SH7042**
- **SH7043**
- **SH7044**
- **SH7045**

For HP E3473A SH7050 Emulator,

- **SH7050**
- **SH7051**

<*mode number*> Specify decimal numbers for the processor clock and the operation mode.

<*sp value*> Specify a 32-bit address which takes a value multiple of 4. Normally, specify the default value of the user program.

<*map range*> Specify an area to be mapped.

Format: <*start address*>..<*end address*>

<*memory type*> Specify one of the following memory types.

- **eram**
- **erom**
- **tram**
- **trom**
- **grd**

For a memory type of other area, **eram** and **erom** cannot be specified.

```
# Configuration File

# Hardware Options
config start
config bpds disable
config chip SH7042
config mode 6
config mrst disable
config qbrk enable
config rrt disable
config rsp 000000000
config end


# Memory Map
map start
map 000200000..00020ffff erom
map 000500000..0005fffff grd
map 001000000..00111ffff eram
map other tram
map end
```

Figure 2-3. Configuration File Example

Note

3

Language Tools

Language Tools

This chapter describes language tools which can be used with the HP B3755A/56A Debug User Interface.

Hitachi Language Tools

The HP B3755A/56A Debug User Interface can debug user programs created with the following Hitachi language tools.

Table 3-1. Hitachi Language Tools

Tool	Command	Description
C Compiler	`shc`	SH Series C Compiler
Assembler	`asmsh`	SH Series Assembler
Linker	`lnk`	H Series Linkage Editor

For version numbers of language tools supported by the HP B3755A/56A Debug User Interface, contact your nearest HP support office.

Command Options

This section describes important command options when using the Hitachi language tools.

C Compiler

`-debug` Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

Assembler

`-debug` Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

Linker

`-debug` Generates debug information.
You must always specify this option. Programs without debug information cannot be debugged.

Note

4

Emulation Status

Emulation Status

This chapter describes the emulation status messages which are displayed in the Debug window.

An emulation status message is displayed in the Debug window.
The HP B3755A/56A Debug User Interface has the following emulation status messages.

- **Emulation reset**

  The emulator is resetting the processor.

  The resetting procedure is power-on reset.

- **Running in monitor**

  The emulator is executing the monitor.

- **Running user program**

  The emulator is executing the user program.

- **Awaiting target reset**

  The emulator is awaiting a reset signal from the target system.

  When a "run from reset" command is executed, the emulator enters this state. During this state, the emulator cannot break to the monitor.

- **Target reset**

  The target system is resetting the processor.

  When the emulator accepts the $\overline{\text{RES}}$ signal from the target system while running the user program, the emulator enters this state. The HP E3472A SH7040 Emulator also enters this state when it accepts the $\overline{\text{MRES}}$ signal from the target system. During this state, the emulator cannot break to the monitor.

- **Bus grant**

  A bus-released state.

  When the emulator accepts the $\overline{\text{BREQ}}$ signal from the target system, the emulator enters this state.

- **Sleep**

  Sleep mode.

  Sleep mode is cleared when the emulator breaks to the monitor. When entering the monitor from sleep mode, the program counter (PC) points to the next instruction from the SLEEP instruction.

- **Software Standby**

  Software standby mode.

  Software standby mode is cleared when the emulator breaks to the monitor. When entering the monitor from software standby mode, the program counter (PC) points to the next instruction from the SLEEP instruction.

- **Hardware standby**

  Only the HP E3473A SH7050 Emulator enters this state.

  When the emulator accepts the $\overline{\text{HSTBY}}$ signal from the target system while running the user program, the emulator enters this state. During this state, the emulator cannot break to the monitor.

- **No target power**

  The target system's power is off.

- **Slow clock**

  The processor's clock is abnormally slow or stopped.

  A broken-down clock on the target system may cause this state.

- **Unknown state**

  An abnormal state.

  The emulator also enters this mode when the $\overline{\text{WAIT}}$ signal from the target system is left asserted.

- **Probe power failed**

  The power supply of the emulation probe shows anomaly.

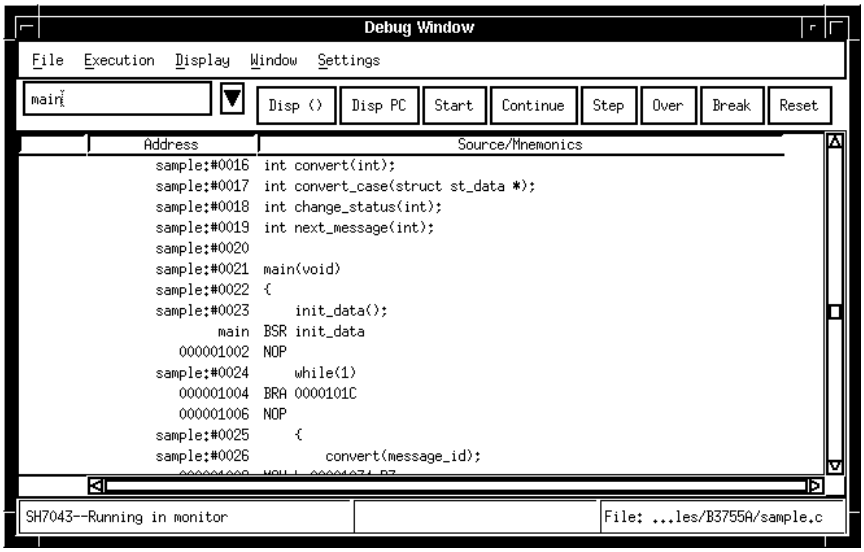

Figure 4-1. Debug Window

Note

5

Trace

Trace

This chapter describes trace functions specific to the HP B3755A/56A Debug User Interface.

Logic Analyzer

A logic analyzer is required to trace programs with the HP B3755/56A Debug User Interface.

Connecting a Logic Analyzer

The emulator and the logic analyzer must be connected by plugging both of the two paths shown below:

- Pod connection

  Attach the **HP 01650-63203** termination adapters to the specified 5 pods of the logic analyzer and plug them to the emulation probe.

- Trigger signal line connection

  Plug the BNC cable that comes with the emulator between the external trigger output connector on the logic analyzer and the **BREAK IN** connector on the emulation controller.

Pods used for the connection vary depending on the model of your logic analyzer, and therefore check pod numbers carefully when connecting them.

Table 5-1. Pod Numbers of the Logic Analyzer

Emulation Probe	Portable Logic Analyzer			HP 16500B/C System	
	1660/61C/CS	1670A/D	1671A/D	16550A	16554/55/56A/D
POD 1	Pod 1	Pod 1	Pod 1	Pod 1	Master Pod 1
POD 2	Pod 2	Pod 2	Pod 2	Pod 2	Master Pod 2
POD 3	Pod 3	**Pod 5**	Pod 3	Pod 3	**Extended Pod 1**
POD 4	Pod 4	**Pod 6**	Pod 4	Pod 4	**Extended Pod 2**
POD 5	Pod 5	**Pod 7**	Pod 5	Pod 5	**Extended Pod 3**

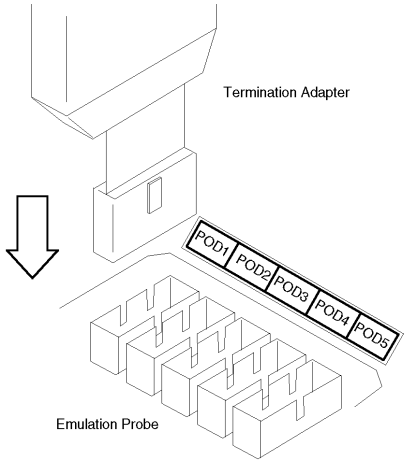

Figure 5-1. Plugging the Logic Analyzer Pods

Configuring the Logic Analyzer

The HP B3755/56A Debug User Interface controls the logic analyzer via LAN. Specify the LAN settings for the logic analyzer as shown below.

- Select **Ethernet** for Controller Settings in the System External I/O menu or System Configuration menu.
- Specify an **IP address** in the Lan Settings or Ethernet Configuration dialog box.

See the user's guide of your logic analyzer for details.

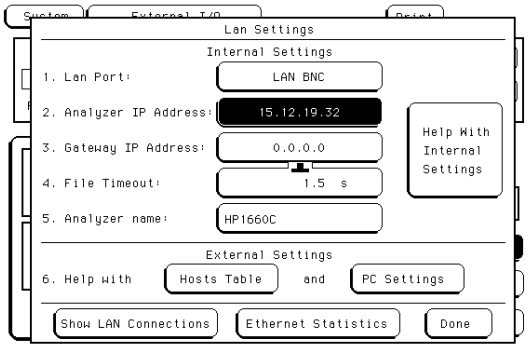

Figure 5-2. Specifying the Logic Analyzer IP Address

Opening the Trace Window

Follow the steps below to open the Trace window.

1 From the control menu of the HP Debug User I/F window, choose **Connect→Logic Analyzer**... (Alt, C, L).

2 When the Logic Analyzer Connection dialog box appears, specify the following items in it.

LAN Address: Specifies the host name or IP address of the logic analyzer.

Slot: When the HP 16500B/C system includes multiple logic analyzers, this item specifies the slot ID for the logic analyzer used for tracing.

When **AUTOSELECT** is specified, the HP B3755/56A Debug User Interface searches all slots for logic analyzers starting from slot A and uses the first-detected logic analyzer for tracing.

When the HP 16500B/C system includes only one logic analyzer or when you use a portable logic analyzer, specify **AUTOSELECT**.

Connection Timeout: Specifies the timeout period to connect to the logic analyzer (in seconds).

If the connection to the logic analyzer is not established within the specified time period, the HP B3755/56A Debug User Interface regards it as an error and aborts the connection.

3 Click the Connect button.

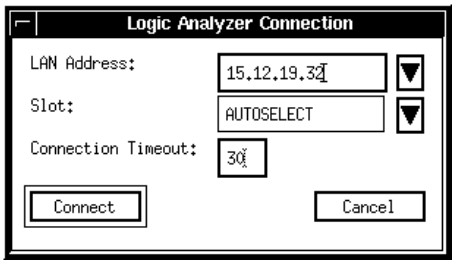

Figure 5-3. Logic Analyzer Connection Dialog Box

You can also open the Trace window with the command used to start up the HP B3755/56A Debug User Interface.

Format

```
netrap -a <emulator> -l <analyzer> [-s <slot>]
```

Options

-a <*emulator*>	Specifies the host name or IP address of the emulator.
-l <*analyzer*>	Specifies the host name or IP address of the logic analyzer.
-s <*slot*>	When the HP 16500B/C system includes multiple logic analyzers, this option specifies the slot ID of the logic analyzer used for tracing by one of characters, **A** through **J** or **a** through **j**. If this option is not specified, it defaults to **AUTOSELECT**.

Resources of the Logic Analyzer

The HP B3755/56A Debug User Interface uses the following resources of the logic analyzer. User can use the remaining resources or modules other than logic analyzers such as oscilloscopes without restraint.

- **Analyzer modules**

  The HP B3755/56A Debug User Interface selects **Analyzer 1** to use from two analyzer modules in the logic analyzer. Do not change the settings of **Analyzer 1**.

  Analyzer 2 can be used as a timing analyzer for example.

- **Pods**

  In addition to the pods listed in Table 5-1, you cannot use the pods shown in the following table although they are connected nowhere.

Table 5-2. Unavailable Pods

Portable Logic Analyzer			**HP 16500B/C System**	
1660/61C/CS	**1670A/D**	**1671A/D**	**16550A**	**16554/55/56A/D**
Pod 6	Pod 8	Pod 6	Pod 6	Extended Pod 4

Other pods can be used by assigning them to **Analyzer 2**.

- **Trigger terms**

  The HP B3755/56A Debug User Interface uses the trigger terms on the left side in the following figure. Do not change the settings of these trigger terms.

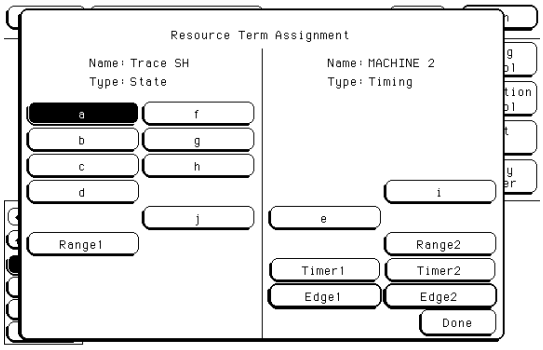

Figure 5-4. Trigger Terms of the Logic Analyzer

  Trigger terms on the right side can be used by assigning them to **Analyzer 2**.

- **External trigger**

  The HP B3755/56A Debug User Interface uses the external trigger output (PORT OUT). Do not change the settings of the external trigger output.

  The external trigger input (PORT IN) can be used without restraint.

Note

Before operating resources of the logic analyzer the HP B3755/56A Debug User Interface does not use, be sure to stop tracing (Trace Halt).

Data and Status Conditions

This section describes the data and status conditions in the following dialog boxes of the HP B3755A/56A Debug User Interface.

- Trace Trigger Store Condition dialog box.
- Trace Pattern dialog box of sequential trace.

Data Condition

The data bus to the emulation analyzer is 32-bit width. You should consider which of four byte data is valid when setting the data condition.

Bus width, access size, and address determine the valid byte data among the four, as shown in the following table. Use "**x**" for invalid byte data to set the data condition.

Table 5-3. Data Condition Settings

Area	Bus Width	Access Size	Address	Upper Word		Lower Word		Example
				Upper Byte	Lower Byte	Upper Byte	Lower Byte	
On-Chip ROM	32-Bit	Byte	4n	Valid	-	-	-	**0a1xxxxxx**
			4n+1	-	Valid	-	-	**0xxb2xxxx**
			4n+2	-	-	Valid	-	**0xxxxc3xx**
			4n+3	-	-	-	Valid	**0xxxxxxd4**
		Word	4n	Valid	Valid	-	-	**0a1b2xxxx**
			4n+2	-	-	Valid	Valid	**0xxxxc3d4**
		Long word	4n	Valid	Valid	Valid	Valid	**0a1b2c3d4**
On-Chip RAM On-Chip peripheral module	16-Bit	Byte	2n	-	-	Valid	-	**0xxxxa1xx**
			2n+1	-	-	-	Valid	**0xxxxxxb2**
		Word	2n	-	-	Valid	Valid	**0xxxxa1b2**
	32-Bit	Long word	4n	Valid	Valid	Valid	Valid	**0a1b2c3d4**

Table 5-3. Data Condition Settings (Continued)

Area	Bus Width	Access Size	Address	Upper Word		Lower Word		Example
				Upper Byte	Lower Byte	Upper Byte	Lower Byte	
External Memory	8-Bit	Byte	n	-	-	-	Valid	**0xxxxxxa1**
		Word	2n (1st)	-	-	-	Valid	**0xxxxxxa1**
			2n+1 (2nd)	-	-	-	Valid	**0xxxxxxb2**
		Long word	4n (1st)	-	-	-	Valid	**0xxxxxxa1**
			4n+1 (2nd)	-	-	-	Valid	**0xxxxxxb2**
			4n+2 (3rd)	-	-	-	Valid	**0xxxxxxc3**
			4n+3 (4th)	-	-	-	Valid	**0xxxxxxd4**
	16-Bit	Byte	2n	-	-	Valid	-	**0xxxxa1xx**
			2n+1	-	-	-	Valid	**0xxxxxxb2**
		Word	2n	-	-	Valid	Valid	**0xxxxa1b2**
		Long word	4n (1st)	-	-	Valid	Valid	**0xxxxa1b2**
			4n+2(2nd)	-	-	Valid	Valid	**0xxxxc3d4**
	32-Bit (SH7040)	Byte	4n	Valid	-	-	-	**0a1xxxxxx**
			4n+1	-	Valid	-	-	**0xxb2xxxx**
			4n+2	-	-	Valid	-	**0xxxxc3xx**
			4n+3	-	-	-	Valid	**0xxxxxxd4**
		Word	4n	Valid	Valid	-	-	**0a1b2xxxx**
			4n+2	-	-	Valid	Valid	**0xxxxc3d4**
		Long word	4n	Valid	Valid	Valid	Valid	**0a1b2c3d4**

Note

In the single address transfer by the DMA controller (DMAC), the analyzer cannot correctly trace data, capturing unexpected values.

Status Condition

You can specify the following items as the status condition.

fetch Instruction fetch cycle.

data Data access cycle.

read Read cycle.

write Write cycle.

irom On-chip ROM access cycle.

iram On-chip RAM access cycle.

cache Cache access cycle.

This status condition is available for the HP E3472A SH 7040 Emulator only.

dma DMA controller (DMAC) cycle.

Data transfer controller (DTC) cycle is also included for the HP E3472A SH 7040 Emulator.

intack Interrupt acknowledge cycle.
When the emulator breaks to the monitor, an interrupt acknowledge cycle may also happens.

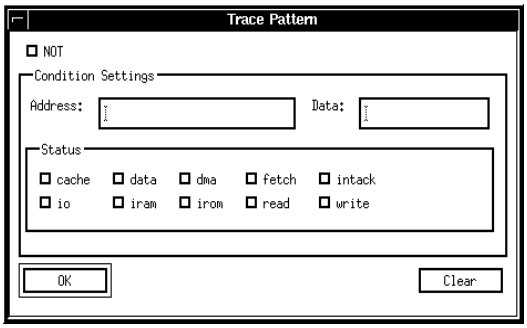

Figure 5-5. Trace Pattern Dialog Box

6

Windows

Windows

This chapter describes windows specific to the HP B3755A/56A Debug User Interface.

Register Window

In the Register window of the HP B3755A/56A Debug User Interface, the internal registers of the CPU can be displayed and modified.

- Program Counter (PC)
- Status Register (SR)
- General Registers (R0 to R15)
- Stack Pointer (SP)
- Global Base Register (GBR)
- Vector Base Register (VBR)
- Procedure Register (PR)
- Multiply-Accumulate Register (MACH, MACL)

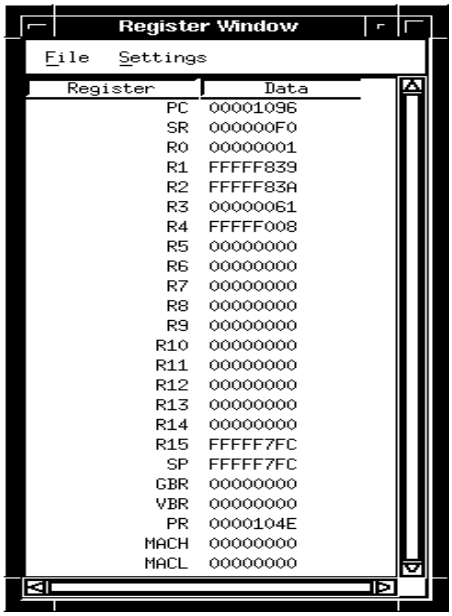

Figure 6-1. Register Window

Peripheral Window

In the Peripheral window of the HP B3755A/56A Debug User Interface, all registers of the following on-chip peripheral modules can be displayed and modified.

- Interrupt Controller (INTC)
- User Break Controller (UBC)
- Data Transfer Controller (DTC) (SH7040)
- Cache Controller (CAC) (SH7040)
- Bus State Controller (BSC)
- DMA Controller (DMAC)
- Multiple Function Timer Pulse Unit (MTU) (SH7040)
- Advanced Timer Unit (ITU) (SH7050)
- Advanced Pulse Controller (APC) (SH7050)
- Watchdog Timer (WDT)
- Serial Communication Interface (SCI)
- A/D Converter
- Compare Match Timer (CMT)
- Pin Function Controller (PFC)
- I/O Ports
- Port Output Enable (POC) (SH7040)
- System Control Registers

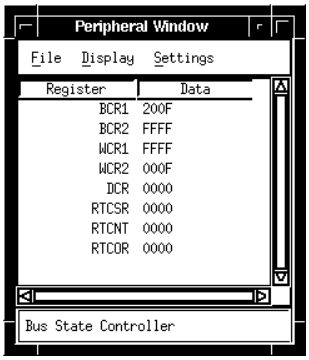

Figure 6-2. Peripheral Window

Note

7

Restrictions and Limitations

Restrictions and Limitations

This chapter describes restrictions and limitations.

The HP B3755A/56A Debug User Interface and the HP E3472/73A Emulator have the following restrictions and limitations.

- **Direct Memory Access**

  The target system cannot perform direct memory access to the emulation memory.

- **Single address mode transfer**

  Single address mode transfer to the emulation memory by internal DMAC is not allowed.

  In the single address transfer by the DMA controller (DMAC), the analyzer cannot correctly trace data, capturing unexpected values.

- **Reset**

  The HP E3472A SH7040 Emulator ignores the $\overline{\text{RES}}$ and $\overline{\text{MRES}}$ signals from the target system while running the monitor.

  The HP E3473A SH7050 Emulator ignores the $\overline{\text{RES}}$ and $\overline{\text{HSTBY}}$ signals from the target system while running the monitor.

- **Interrupts**

  While running the monitor, the emulator responds to no interrupts.

  The emulator suspends interrupt requests in the monitor; the requests will be serviced upon return to the user program.

- **Watchdog Timer**

  When entering the monitor, the watchdog timer (WDT) stops counting regardless of its mode, watchdog or interval. And, it resumes counting upon return to the user program.

- **Sleep and Software Standby Modes**

  Sleep and software standby modes are cleared when the emulator breaks to the monitor.

  When entering the monitor, the program counter (PC) points to the next of the SLEEP instruction.

- **Flash Memory**

  The emulator does not support on-board programming mode of the on-chip flash memory.

Writing to the flash memory control register (FLMCR) or the block set register (EBR) is invalid. Reading from these registers will result in unpredictable values.

The emulation of the flash memory using the on-chip RAM is also not supported.

Index