User's Guide

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

# Agilent Technologies E2406A Analysis Probe for Motorola 68030

The E2406A Analysis Probe — At a Glance

The E2406A Analysis Probe provides a complete interface for state or timing analysis between of the supported 68030 microprocessors listed below and Agilent logic analyzers. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

Microprocessor	Package	Ordering Information
68030	128-pin PGA	E2406A
68030	132-pin PQFP	E2406A option 1CC

The analysis probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software on the enclosed disks set up the logic analyzer for compatibility with the analysis probe. The inverse assemblers let you obtain displays of the 68030 data in 68030 assembly language mnemonics.
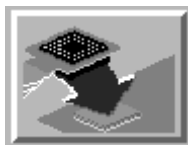
If you are using the analysis probe with the 16600 or 16700 series logic analysis systems, you only need this manual as a reference. The 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.
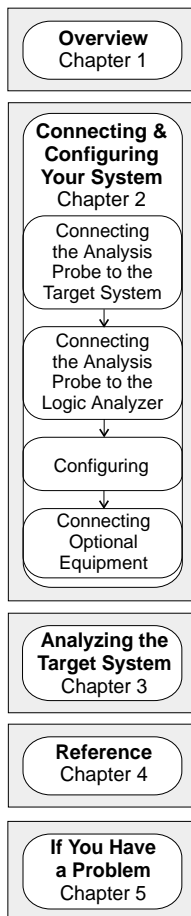
Logic
Analyzer

Target
System

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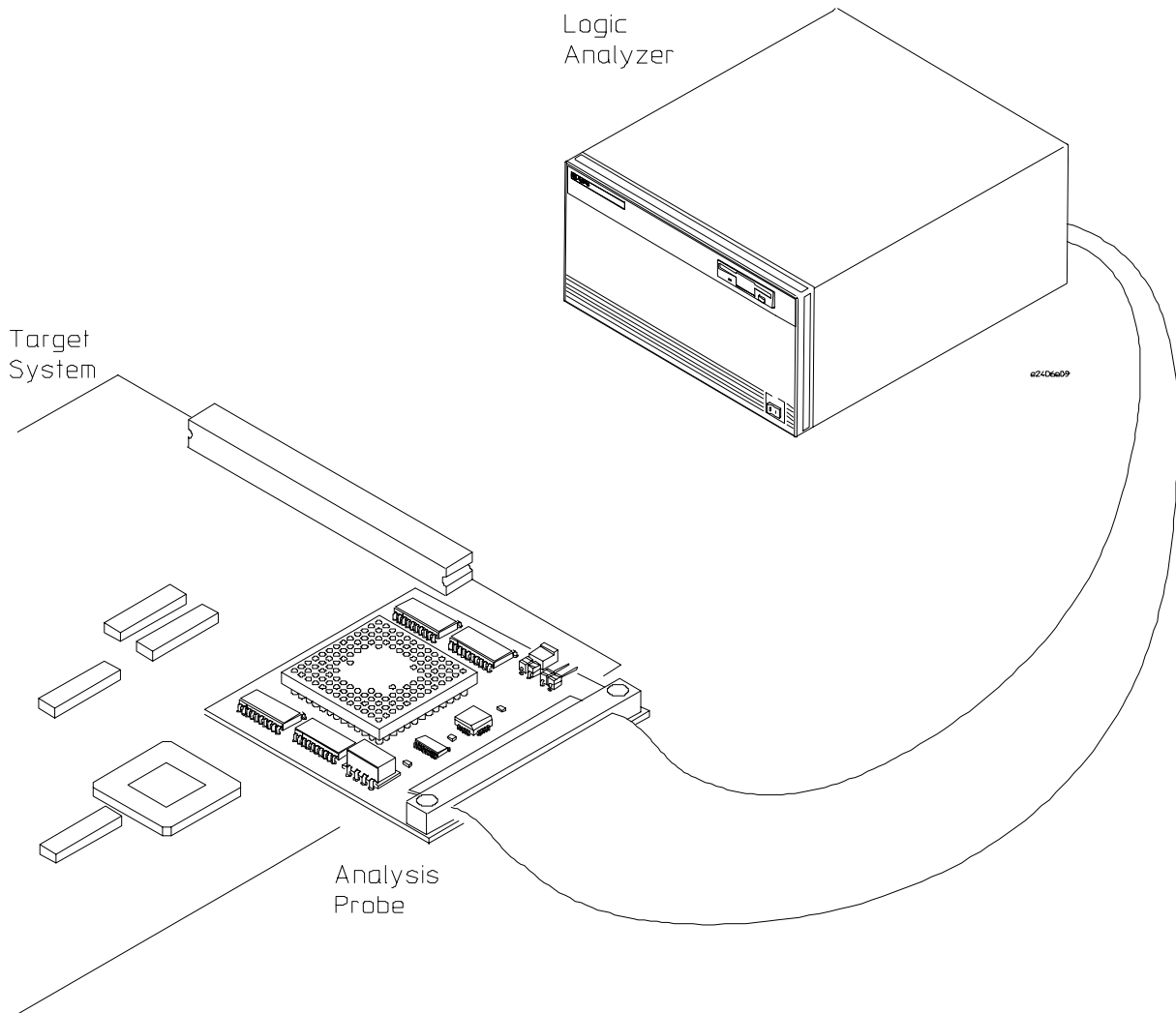
Analysis
Probe

Analyzing a Target System with the E2406A Analysis Probe

In This Book

This book is the User's Guide for the E2406A Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:

Overview
Chapter 1

Chapter 1 contains overview information, including a list of required equipment.

Connecting & Configuring Your System
Chapter 2

Connecting the Analysis Probe to the Target System

↓

Connecting the Analysis Probe to the Logic Analyzer

↓

Configuring

↓

Connecting Optional Equipment

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

16600 and 16700 Series Logic Analysis Systems

If you are using the analysis probe with 16600 or 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The 16600 and 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Analyzing the Target System
Chapter 3

Chapter 3 provides information on analyzing the supported microprocessors.

Reference
Chapter 4

Chapter 4 contains reference information on the analysis probe.

If You Have a Problem
Chapter 5

Chapter 5 contains troubleshooting information.

Contents

Overview

Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported

Overview
Chapter 1

Connecting &
Configuring
Your System
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

Analyzing the
Target System
Chapter 3

Reference
Chapter 4

If You Have
a Problem
Chapter 5
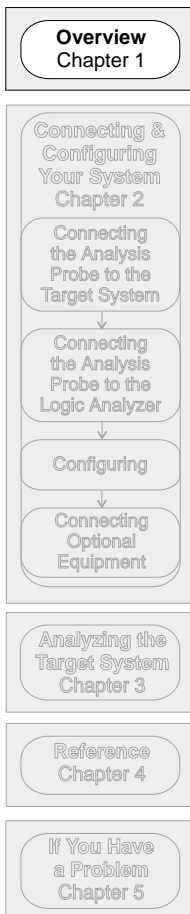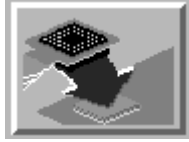
Setup Assistant

Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the 16600 and 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the M68030 Processor Support Package. Use the procedure on the CD-ROM jacket to install the M68030 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the E2406A analysis probe. Logic analyzer software version requirements are shown on the following page.

The E2406A requires five logic analyzer pods (80 channels) for inverse assembly.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16550A (one card)	102/card	100 MHz	250 MHz	4 k states
16554A (two cards)	68/card	70 MHz	125 MHz	512 k states
16555A (two cards)	68/card	110 MHz	250 MHz	1 M states
16555D (two cards)	68/card	110 MHz	250 MHz	2 M states
16556A (two cards)	68/card	100 MHz	200 MHz	1 M states
16556D (two cards)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the E2406A. If your software version is older than those listed, load new system software before loading the E2406A software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with E2406A
16600 Series	The latest 16600 logic analyzer software version is on the CD-ROM shipped with this product.
1660A/AS Series	A.03.01
1660C/CS/CP Series	A.02.01
1670A/D Series	A.02.01
Mainframes*	
16700 Series	The latest 16700 logic analyzer software version is on the CD-ROM shipped with this product.
16500C Mainframe	A.01.05
16500B Mainframe	A.03.14

* The mainframes are used with the 16550 and 16554/55/56 logic analyzer modules.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

E2406A

- The analysis probe, which includes the analysis probe circuit card and cables.
- Five 100 kOhm Termination Modules (part number 01650-63206).
- Four jumpers (part number 1252-3743) of which up to two may be required at one time.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- This User's Guide.

E2406A Option 1CC (for 132-pin PQFP packages)

If you ordered option 1CC, you received the following additional equipment:

- QFP Adapter Assembly.
- Transition Board.
- Pry Tool (for removing adapter).
- Mechanical Samples (not used with the analysis probe).
- Operating Note.

Analysis
Probe

Software
and Manual

User's Guide

Jumpers

Option #1CC
QFP Adapter Assembly

Transition
Board

Pry
Tool

Probe
Adapter

Mechanical
Samples (not used)

e2406e12

Termination Modules
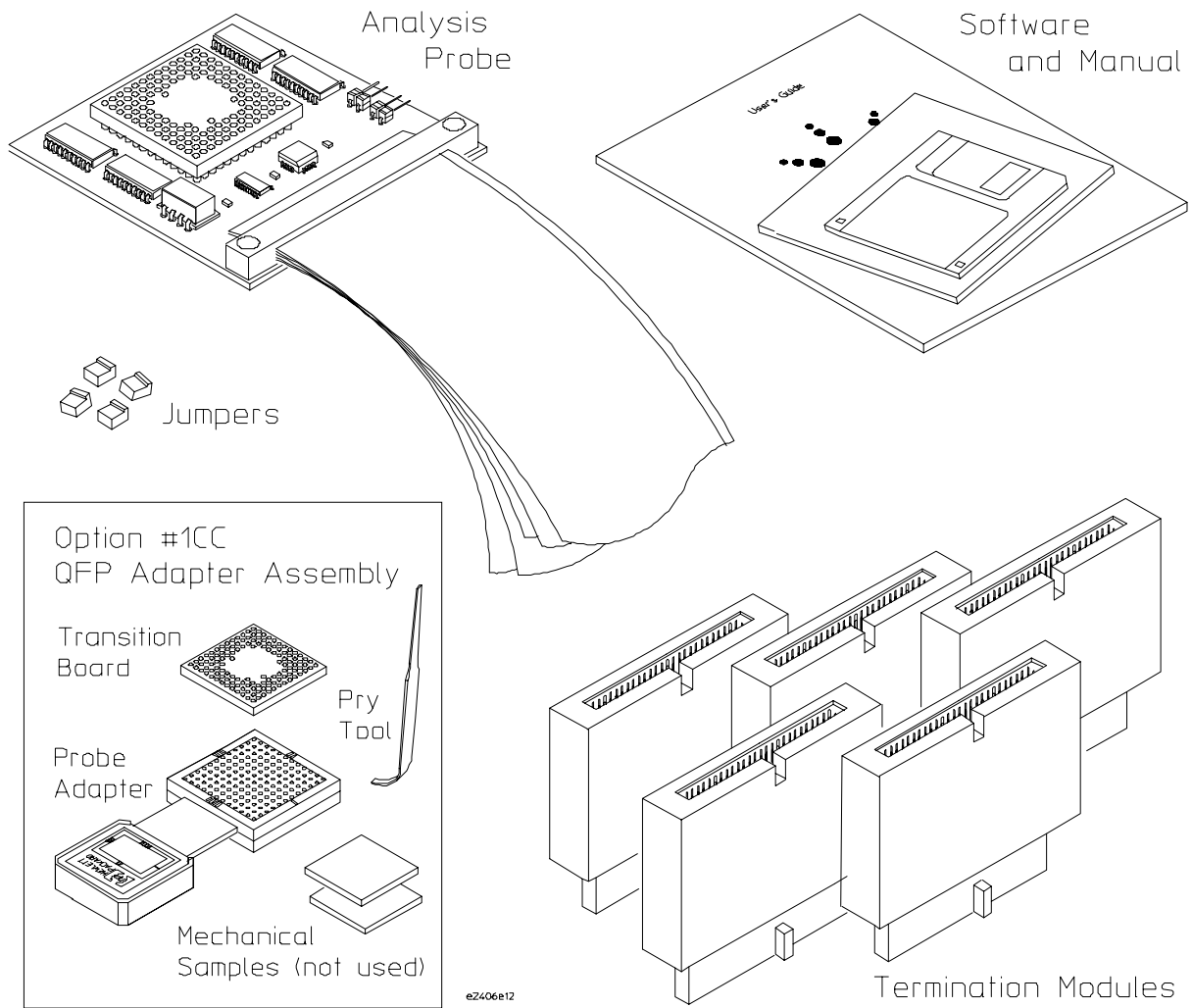
Equipment Supplied with the E2406A

Minimum equipment required

For state and timing analysis of an 68030 target system, you need all of the following items.

- The E2406A Analysis Probe.

- For 132-pin PQFP target systems, the E2406A option 1CC QFP Probe Adapter Assembly.

- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

Additional equipment supported

The E2406A does not support any additional equipment.

2

Connecting and Configuring
Your System

Connecting and Configuring Your System

**Connecting &
Configuring
Your System**
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an 16600 or 16700 series logic analysis system, follow the instructions given on-screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment

Read the power on/power off sequence.

Target System   **Analysis Probe**

Target System   Analysis Probe   **Termination Adapters**   Logic Analyzer

Target System   Analysis Probe   **Logic Analyzer**

Target System   Analysis Probe   Logic Analyzer

Set Jumpers

Target System   Analysis Probe   Logic Analyzer   **Configuration Files and Inverse Assembler Files**
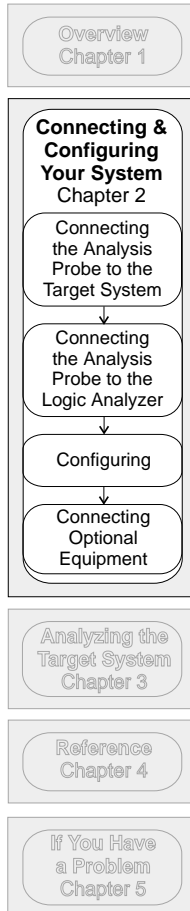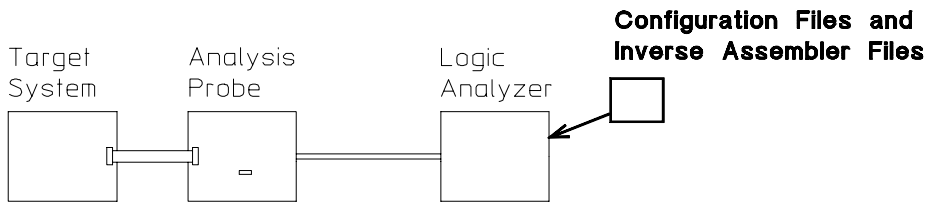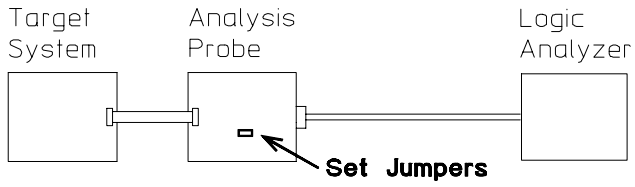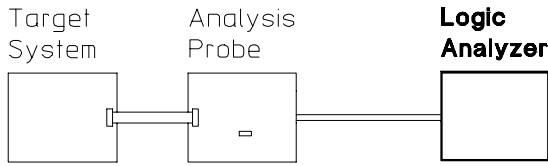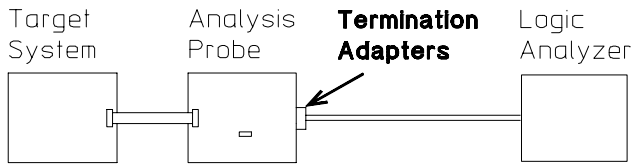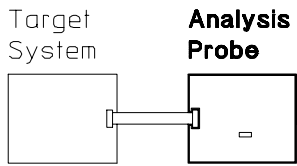
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Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on 16600 and 16700 series logic analysis systems

Ensure the target system is powered off.

1 Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2 When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

1 Logic analysis system.
2 Your target system.
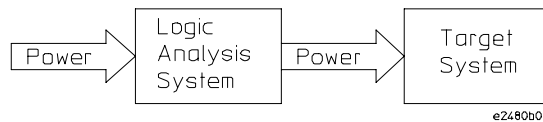
To power off

Turn off power to your system in the following order:

1 Turn off your target system.
2 Turn off your logic analysis system.
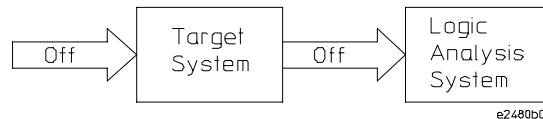
Connecting the Analysis Probe to the Target System

This section explains how to connect the E2406A analysis probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- For PGA target systems, connect the analysis probe directly to the target system.

    Refer to "To connect to a PGA target system."

- For PQFP target systems, connect the probe adapter to the target system, then connect the analysis probe to the probe adapter.

    Refer to "To connect to a PQFP target system."

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

To connect to a PGA target system

The microprocessor connector on the analysis probe connects directly to a PGA socket on the target system. You can add plastic pin protector extender sockets for increased clearance (see illustration on next page).

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

1 Turn off the target system and disconnect all logic analyzer cables from the analysis probe.

2 Remove the 68030 microprocessor from its socket on the target system and store it in a protected environment.

3 Install the analysis probe into the microprocessor socket on the target system, ensuring that pin A1 is properly aligned.

If the analysis probe connector interferes with components of the target system or if a higher profile is required, additional plastic pin protector sockets can be added. Plastic pin protector sockets can be ordered from Agilent Technologies using the part number 1200-1450. However, any 128-pin PGA IC socket with a 68030 footprint and gold-plated pins can be used.

CAUTION

Equipment Damage. Serious damage to the target system or analysis probe can result from incorrect connection. Note the position of pin A1 on the analysis probe and target system socket prior to making any connection. Also, take care to align the analysis probe connector with the pins on the target system socket so that all pins are making contact.

4 Plug the 68030 microprocessor into the socket on the analysis probe.

The socket is designed with low-insertion-force pins to allow easy installation and removal.

CAUTION

Do not use sharp objects or excessive force when removing a microprocessor or socket from the analysis probe board. Traces on the analysis probe board may be damaged.

Microprocessor

Pin A1

Analysis
Probe

Target System
Socket

e2406e11

Connecting the E2406A Analysis Probe to a PGA Target System

To connect to the PQFP target system

With the E2406A option 1CC, you can connect to a PQFP microprocessor (see below). For PQFP target systems, use the instructions in the "PQFP Probe Adapter Assembly Operating Note," to connect the probe adapter assembly to the target system microprocessor. You do not have to remove the target system microprocessor, and you do not need a PGA microprocessor on top of the analysis probe.

The probe adapter can be rotated if components on the target system interfere with the analysis probe. Ensure that pin 1 is properly aligned according to the rotations shown in the "PQFP Probe Adapter Assembly Operating Note."

Analysis Probe

Transition Board

PGA to PQFP Adapter
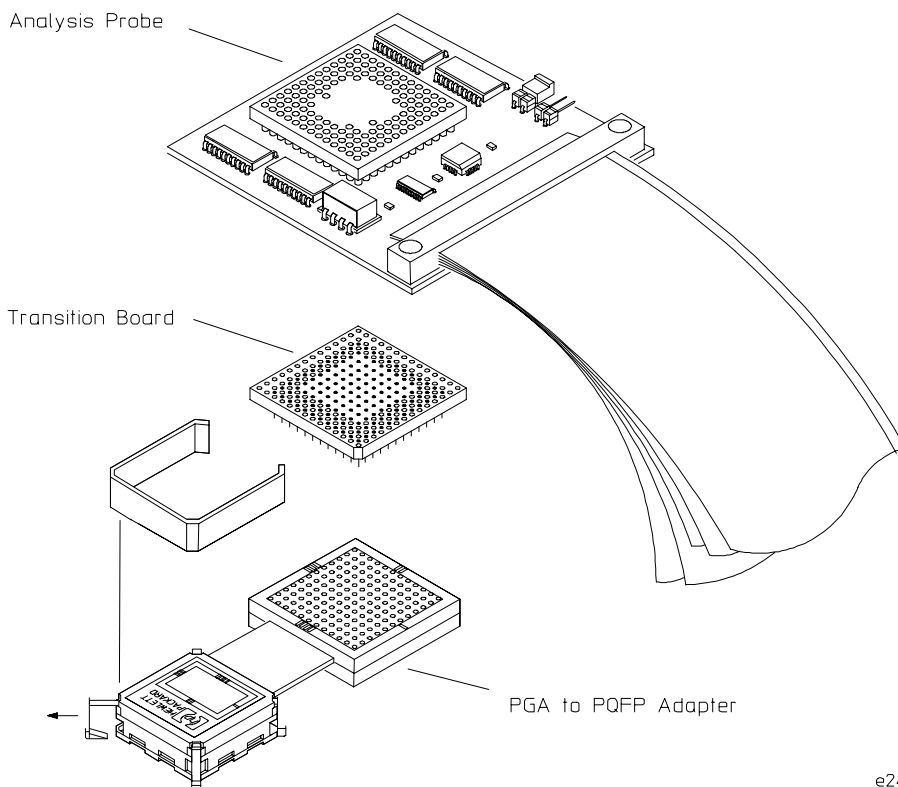
e2406e14

Connecting the E2406A Analysis Probe to a PQFP Target System

Removing the Probe Adapter

C A U T I O N	**Damage to the probe adapter.** Use the extractor tool provided (part number E3435-03801) and follow the removal instructions below. Improper removal will result in broken combs in your probe adapter.

The QFP Probe Adapter Assembly is carefully designed in a robust mechanical package to make reliable electrical contact to each lead of your target IC. Installing and removing the probe requires you to overcome cumulative friction between 132 target leads and corresponding parts of the probe. Removing the probe requires greater force due to the triangular cross-section of the plastic comb teeth that fit between target leads and align the probe contacts. Tests show little risk of probe damage in installing the probe. However, removing the probe by hand from a target with very little space between leads has resulted in broken combs. A simple tool is provided with your QFP Probe Adapter to reduce the risk of such damage. Use the following steps for removal:

1 Place the extractor tool in one of six indentations on the side of the probe adapter next to the PC board as shown below.

2 Gently pry the probe approximately 1/16 inch (1.588 mm) by leveraging against the PC board.

3 Repeat this process on all four sides of the probe adapter until the probe adapter is free from the target system.
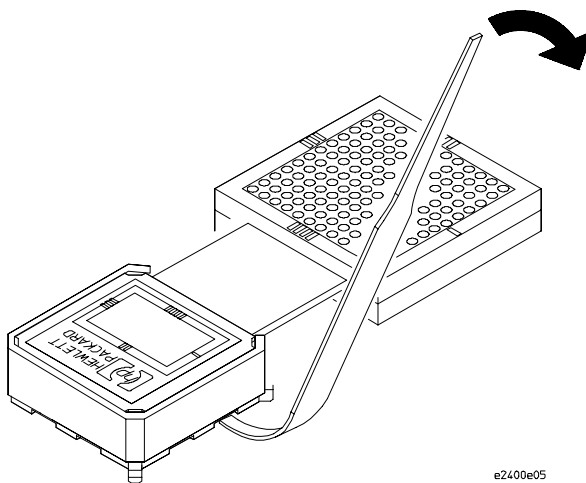
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Removing the QFP Probe Adapter

Connecting the Analysis Probe to the Logic Analyzer
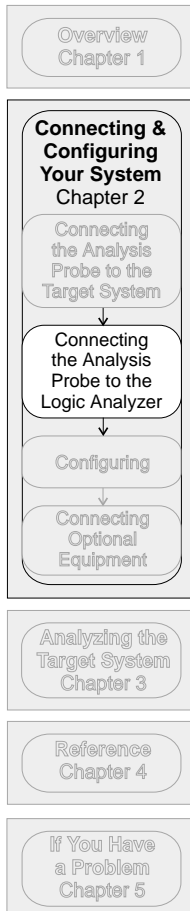
The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

All five analysis probe pods are required for inverse assembly. Note that you must connect the termination adapters to the analysis probe cables in order to connect the logic analyzer cables. The illustration on the following page shows the pod locations on the analysis probe, and the following page shows the procedure for connecting the termination adapters.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- 16600A logic analysis system
- 16601A logic analysis system
- 16602A logic analysis system
- 16550A logic analyzer (one card)
- 16554/55/56 logic analyzers (two cards)
- 1660A/AS/C/CS/CP logic analyzers
- 1661A/AS/C/CS/CP logic analyzers
- 1670A/D logic analyzers
- 1671A/D logic analyzers

Analysis probe pod locations

The illustration below shows the pod locations on the analysis probe.
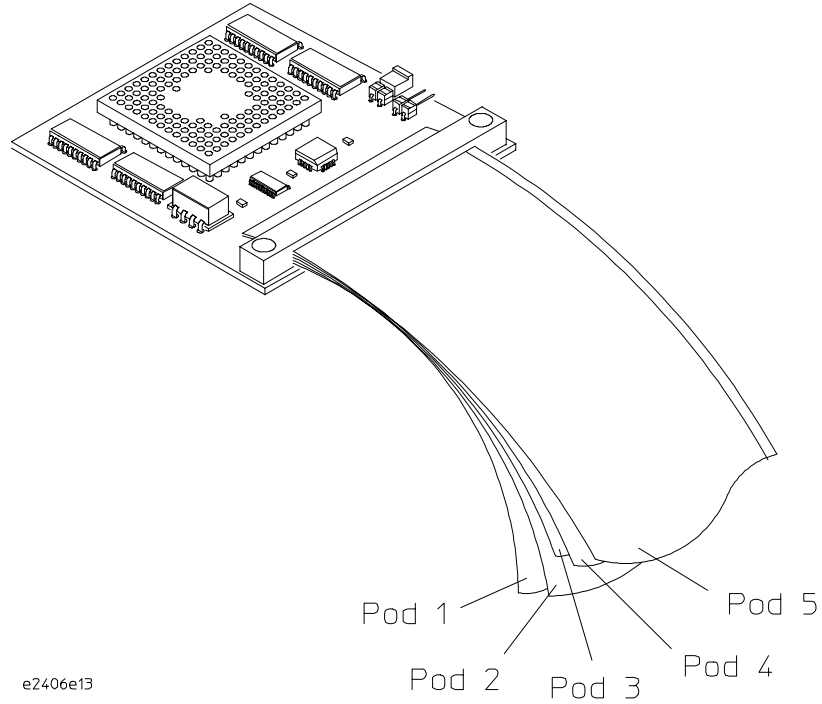
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E2406A Analysis Probe Pod Locations

To connect the termination adapters

The logic analyzer must be properly terminated to operate. The 100 kOhm Termination Adapters (part number 01650-63206) provide this termination.

To connect the termination adapters:

- Connect the female end of the termination adapter to the analysis probe cable.
- Align the key on the male end of the termination adapter with the slot on the connector of the appropriate logic analyzer cables. Push the termination adapter into the connector.

Termination Module

Analysis Probe Cable

e2406e03
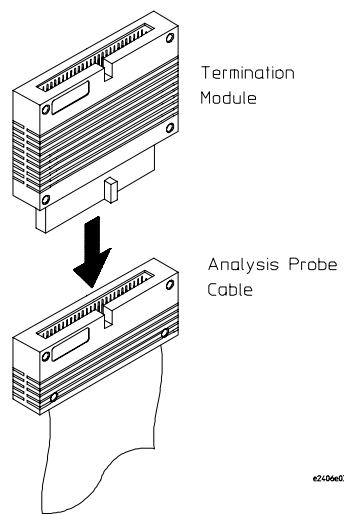
Connecting the Termination Adapters

To connect to the 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the 16600A logic analysis system.

Pods 5-8, 10-12 not used
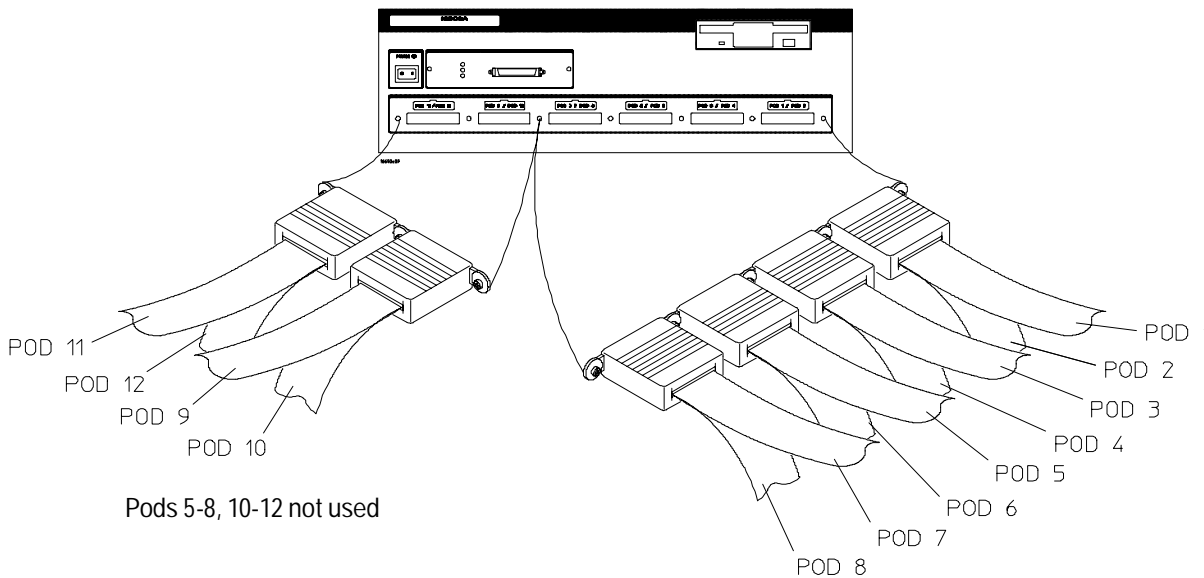
16600	Pods 10-12	Pod 9	Pods 5-8	Pod 4	Pod 3	Pod 2	Pod 1
E2406A Connector	not used	P3 STAT clk ↑	not used	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

> **Configuration File**
> Use configuration file C68030_4 for the 16600 logic analyzer.

To connect to the 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the 16601A
logic analysis system.

16601	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2406A **Connector**	not used	not used	not used	P3 STAT clk ↑	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

Configuration File
Use configuration file C68030_4 for the 16601 logic analyzer.

To connect to the 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the 16602A logic analysis system.
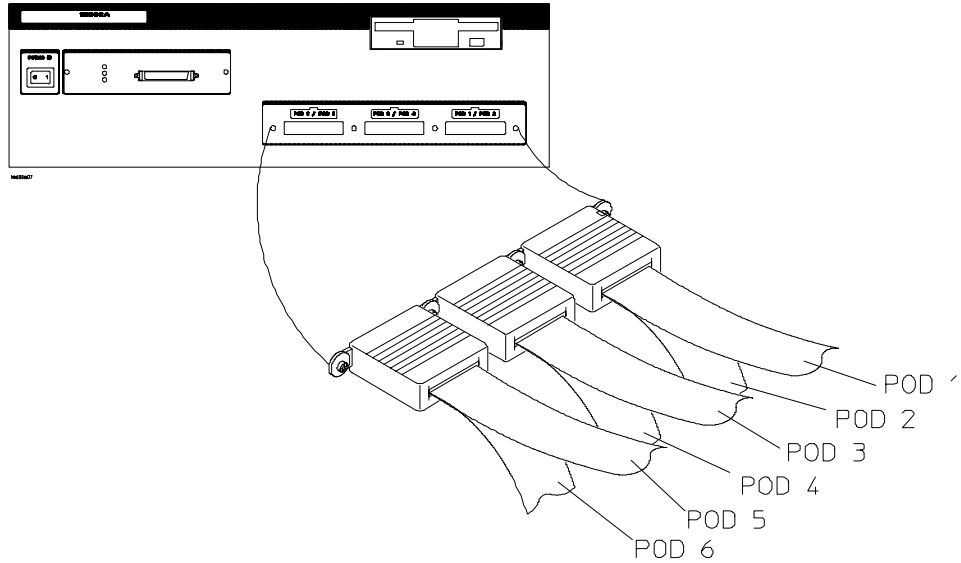
16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2406A Connector	not used	P3 STAT clk ↑	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

Configuration File
Use configuration file C68030_4 for the 16602 logic analyzer.

To connect to the 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the 16550A logic analyzer.

16550A
Master Card

The E2406A does not require the 16550A Expansion Card.
If you are using a multi-card 16550A, use the 16550A
Master Card.
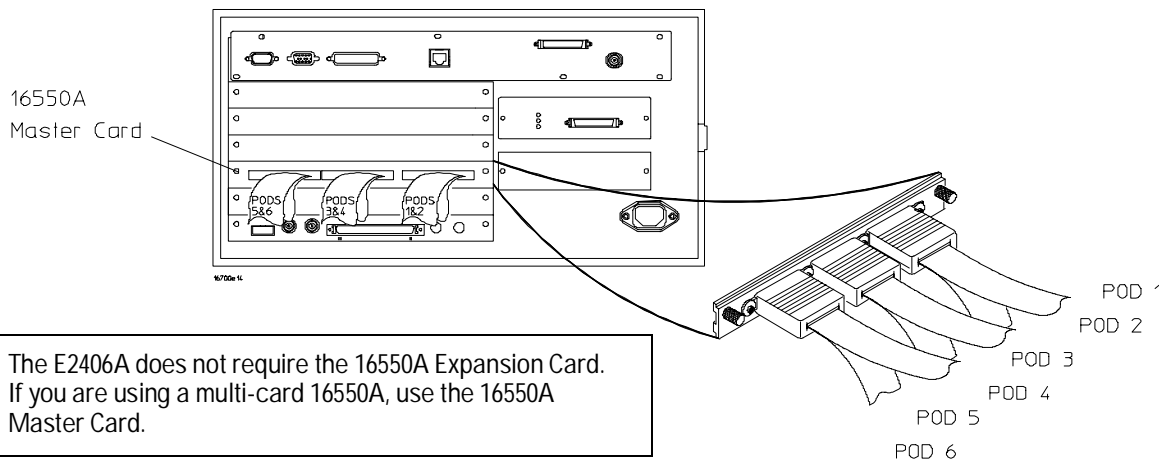
16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
E2406A Connector	not used	P3 STAT clk ↑	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

Configuration File
Use configuration file C68030_4 for the 16550A logic analyzer.

To connect to the 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the
16554A/55A/56A and 16555D/56D logic analyzers.
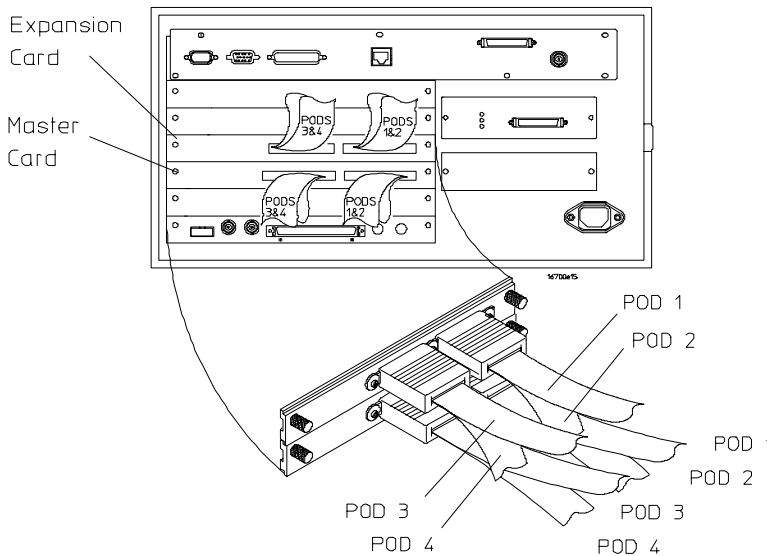
16554/55/56 Exp. Card 1	Expansion Card 1 Pod 4	Expansion Card 1 Pod 3	Expansion Card 1 Pod 2	Expansion Card 1 Pod 1
E2406A Connector	not used	not used	not used	P3 STAT clk ↑
16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
E2406A Connector	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

> **Configuration File**
> Use configuration file C68030_4 for the 16554/55/56 logic analyzers.

To connect to the 1660A/AS/C/CS/CP logic analyzers

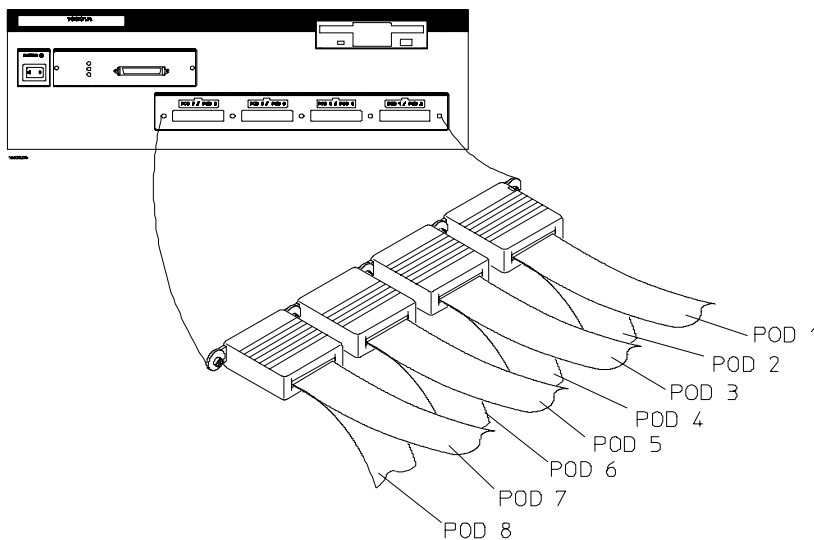Use the figure and table below to connect the analysis probe to the 1660A/C logic analyzers.

1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6	Pod 7	Pod 8
E2406A Connector	P1 DATA	P2 DATA clk ↑	P4 ADDR	P5 ADDR	not used	not used	P3 STAT clk ↑	not used

Configuration File
Use configuration file C68030_4 for the 1660A/AS/C/CS/CP logic analyzers.

To connect to the 1661A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the 1661A/C logic analyzers.
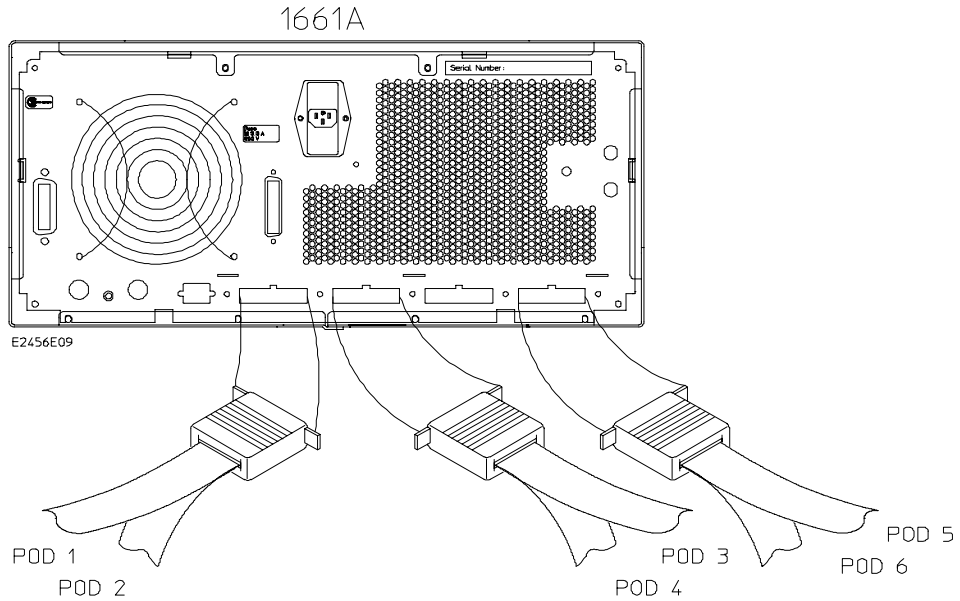
1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
E2406A Connector	P1 DATA	P2 DATA clk ↑	P4 ADDR	P5 ADDR	P3 STAT clk ↑	not used

Configuration File
Use configuration file C68030_4 for the 1661A/AS/C/CS/CP logic analyzers.

To connect to the 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the 1670A/D logic analyzers.

POD 5
POD 6
POD 7
POD 8

POD 1
POD 2
POD 3
POD 4

e2465e01
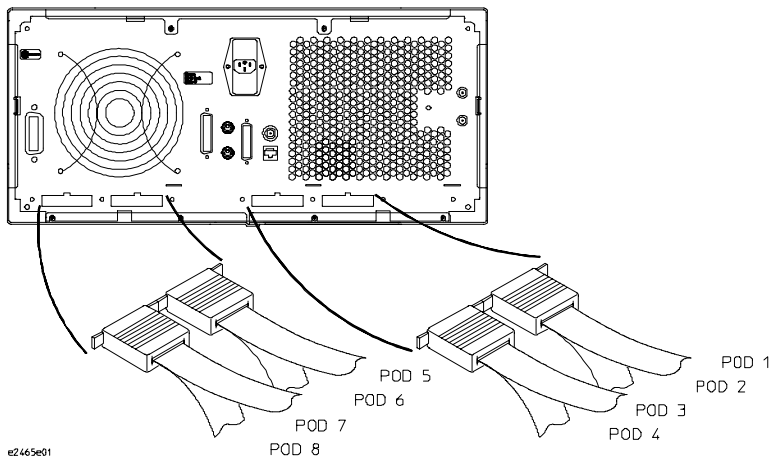
1670A/D	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2406A Connector	not used	P3 STAT clk ↑	not used	not used	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

Configuration File
Use configuration file C68030_4 for the 1670A/D logic analyzer.

To connect to the 1671A/D logic analyzer

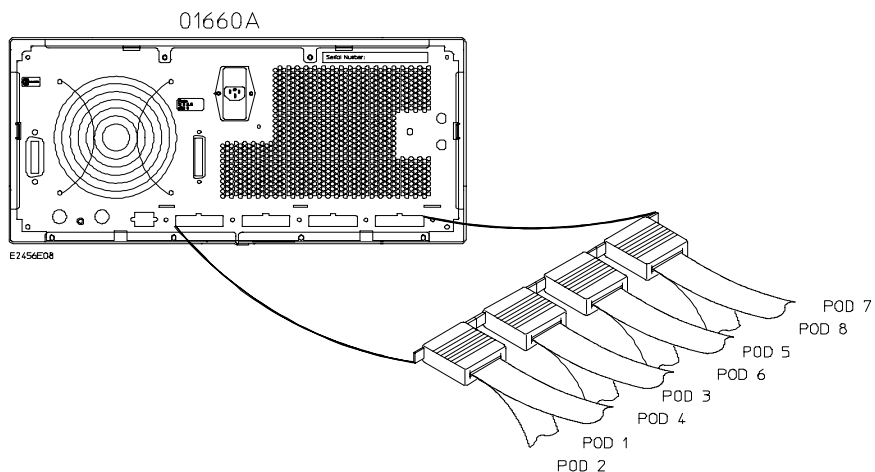Use the figure and table below to connect the analysis probe to the 1671A/D logic analyzer.
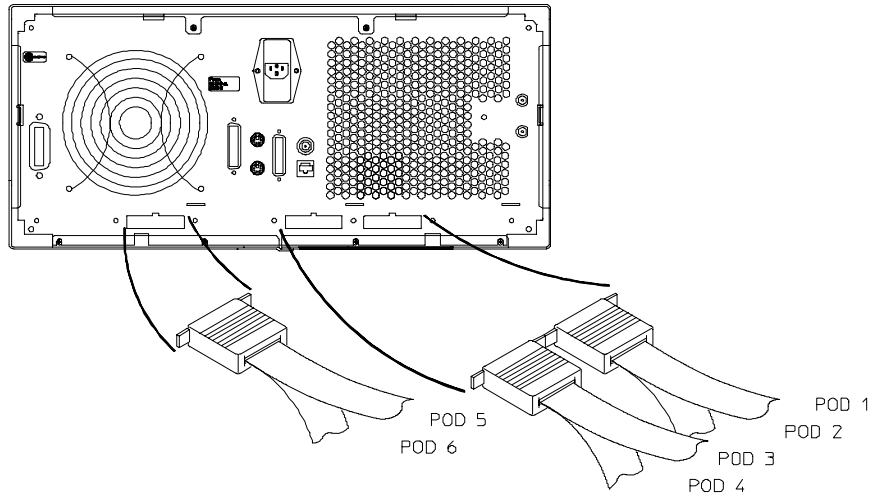
e2473e05

1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2406A Connector	not used	P3 STAT clk ↑	P5 ADDR	P4 ADDR	P2 DATA clk ↑	P1 DATA

Configuration File
Use configuration file C68030_4 for the 1671A/D logic analyzer.

Configuring

This section shows you how to configure the E2406A Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe and target system
- Configuring the logic analyzer

Overview
Chapter 1

**Connecting &
Configuring
Your System**
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

Analyzing the
Target System
Chapter 3

Reference
Chapter 4

If You Have
a Problem
Chapter 5
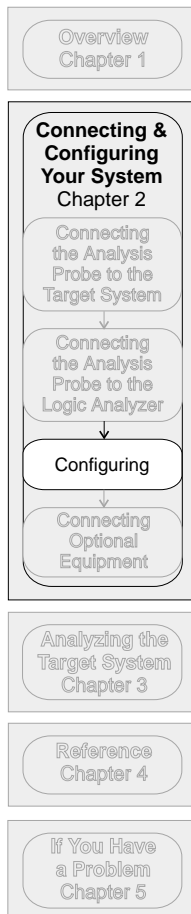
Configuring the Analysis Probe and Target System

Configuring the analysis probe and target system consists of the following:

• Setting the CDIS and MMUDIS jumpers (see next page)
• Disabling the cache memory and MMU, if required

The jumper location is shown in the illustration below.

e2406e10

Jumper Locations

To set the CDIS and MMUDIS jumpers

If you want the code (non-burst) to be disassembled, disable the cache memory to ensure proper disassembly. This can be disabled by setting the least significant bit of the cache control register (CACR) to zero.

CAUTION

Another way to disable the cache memory is to connect the 68030 CDIS pin to ground with the supplied jumper (see previous figure). This method can result in damage to the analysis probe and target system if the target system is designed such that CDIS cannot be grounded (for example, CDIS hardwired to +5 V). Make sure that your target system is designed so that CDIS can be grounded before you connect this pin to ground.

If you are using the 68030 inverse assembler, you may want to disable the MMU so that the physical addresses the analysis probe monitors are effectively the logical addresses. This can be disabled by setting bit 31 of the TC register to zero.

CAUTION
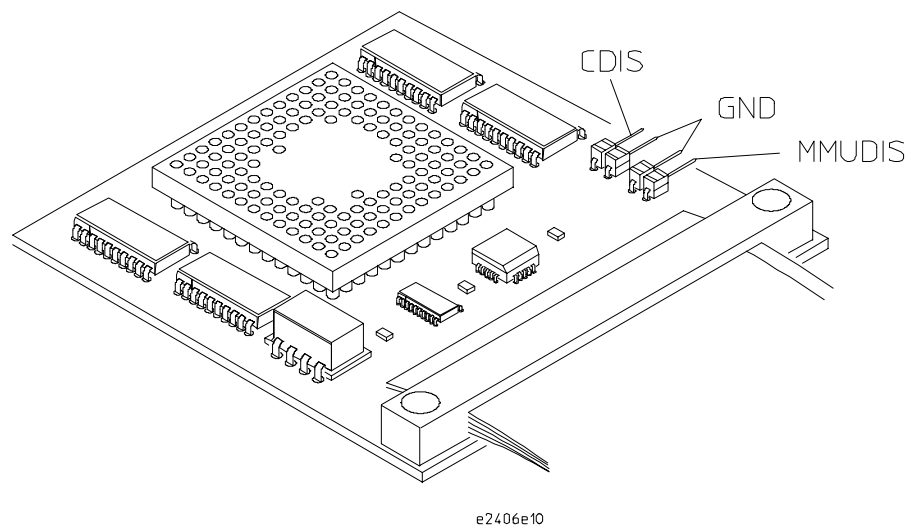
Another way to disable the MMU is to connect the 68030 MMUDIS pin to ground with the supplied jumper (see previous figure). This method can result in damage to the analysis probe and target system if the target system is designed such that MMUDIS cannot be grounded (for example, MMUDIS hardwired to +5 V). Make sure that your target system is designed so that MMUDIS can be grounded before you connect this pin to ground.

Leaving the MMU enabled may result in missing data for some applications. For more information, refer to the section "Interpreting Data" in chapter 3.

Configuring the Logic Analysis System

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the 16600/700 series logic analysis systems, and another procedure for the 1660-series, 1670-series, and logic analyzer modules in an 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/m68030/ exists.

> If the above directory does not exist, you need to install the M68030 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the M68030 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/m68030/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for 68030 analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an 1660-series, 1670-series, or logic analyzer modules in an 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 68030 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1 Insert the floppy disk in the front disk drive of the logic analyzer.

2 Go to the Flexible Disk menu.

3 Configure the menu to load.

4 Use the knob to select the appropriate configuration file.

Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.

5 Select the appropriate analyzer on the menu. The 16500 logic analyzer modules are shown in the Logic Analyzer Configuration Files table.

6 Execute the load operation on the menu to load the file into the logic analyzer.

The logic analyzer is configured for 68030 analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler if the logic analyzer has the appropriate software version.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File
16600A		C68030_4
16601A		C68030_4
16602A		C68030_4
16550A (one card)	100 MHz STATE 500 MHz TIMING	C68030_4
16554A (two card)	0.5M SAMPLE 70/125 MHz LA	C68030_4
16555A (two card)	1.0M SAMPLE 110/250 MHz LA	C68030_4
16555D (two card)	2.0M SAMPLE 110/250 MHz LA	C68030_4
16556A (two card)	1.0M SAMPLE 100/200 MHz LA	C68030_4
16556D (two card)	2.0M SAMPLE 100/200 MHz LA	C68030_4
1660A/AS/C/CS		C68030_4
1661A/AS/C/CS		C68030_4
1670A/D		C68030_4
1671A/D		C68030_4

Connecting Optional Equipment

The E2406A does not support any additional equipment.

3
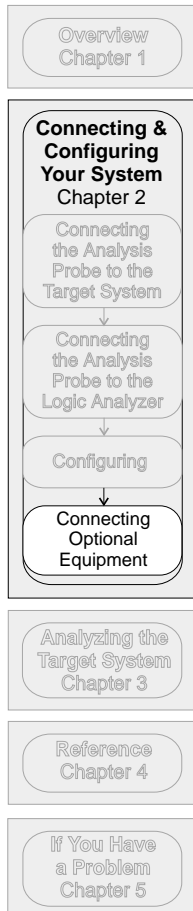
Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the E2406A Analysis Probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.

The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers

Overview
Chapter 1

Connecting &
Configuring
Your System
Chapter 2

Connecting
the Analysis
Probe to the
Target System

Connecting
the Analysis
Probe to the
Logic Analyzer

Configuring

Connecting
Optional
Equipment

**Analyzing the
Target System**
Chapter 3

Reference
Chapter 4

If You Have
a Problem
Chapter 5
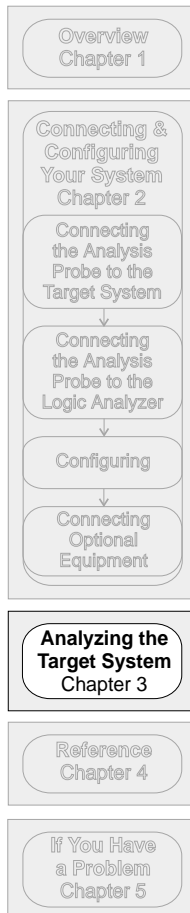
Modes of Operation

The E2406A analysis probe can be used in two different analysis modes: State-per-transfer and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

The 68030's address strobe (AS) indicates that address, function code, size, and R/W state information is on the bus and valid. In state-per-transfer mode, the logic analyzer uses the rising edge of AS to clock two types of information into the logic analyzer:

- All non-burst information.
- The last long word of a burst transfer.

The rising edge of AS is the rising N clock.

The first three long words of a burst transfer are clocked into the logic analyzer by a second clock (rising K clock).

Timing mode

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1 Select the Configuration menu of the logic analyzer.

2 Select the Type field for the analyzer and select Timing.

Timing data is displayed in the Waveform menu of the logic analyzer.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, incorrect inverse assembly may result.

Unwanted triggers

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor may prefetch one or more long words, one technique to avoid unwanted triggering from unused prefetches is to add "8 hex" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

Format specification

The configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor. The tables on the following pages show the signals used in the STAT label and the predefined symbols set up by the configuration files.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes to these labels may cause incorrect or incomplete inverse assembly.

The Format specification display is shown in the following figure. There may be some slight differences in the display shown by your particular analyzer.
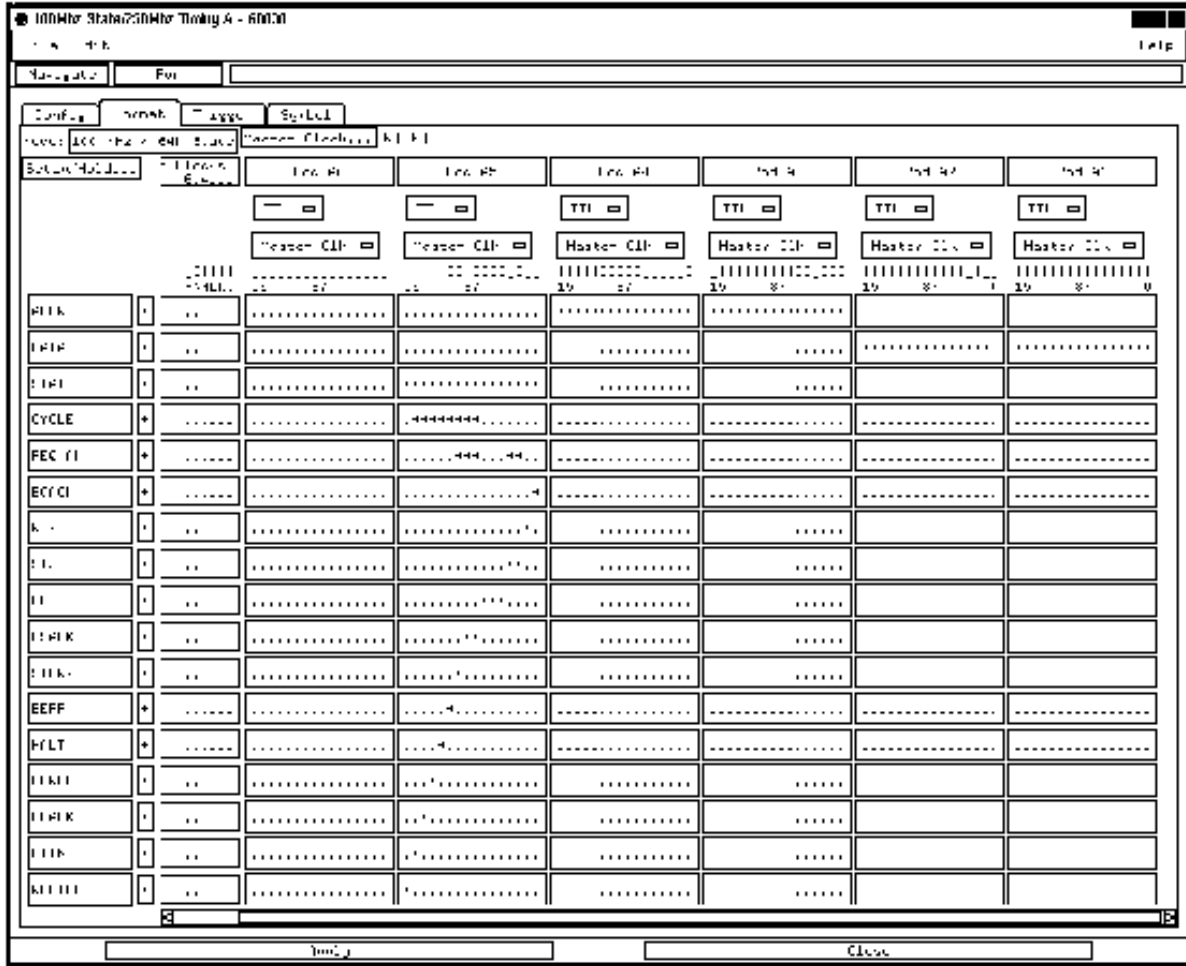
Format Specification

Status Label Bits

Each of the bits of the STAT label is described in the table below. The table on the following page shows the encoding for the STAT labels.

68030 STAT Label Bits

Bit	Status Signals	Description
0	BGACK	This signal is low when the microprocessor has granted control of the bus to another device.
1	R/W	This signal is high for read cycles and low for write cycles.
2-3	SIZ0-SIZ1	These signals indicate the size of the bus transfer requested by the microprocessor.
4-6	FC0-FC2	These signals indicate the type of cycle the microprocessor is executing.
7-8	DSACK0-DSACK1	These signals indicate the size of the bus transfer that was completed.
9	STERM	This signal indicates a port size of 32 bits and that data may be latched on the next falling edge of the CLK.
10	BERR	This signal indicates that an erroneous bus operation is being attempted.
11	HALT	This signal indicates that the microprocessor should suspend bus activity.
12	CBREQ	This signal indicates a burst request for the instruction or data cache.
13	CBACK	This signal indicates that the accessed device can operate in the burst mode.
14	CIIN	This signal indicates that the current bus transfer should not be cached.
15	REFILL	This signal indicates that the instruction pipeline has been flushed and is being refilled by the current state.

68030 STAT Label Encoding

68030 Cycle Type	**Status Bit**
	6 5 4 3 2 1 0
Bus Grant	x x x x x x 0
User Data Write	0 0 1 x x 0 1
User Data Read	0 0 1 x x 1 1
User Program Read	0 1 0 x x 1 1
Supervisor Data Write	1 0 1 x x 0 1
Supervisor Data Read	1 0 1 x x 1 1
Supervisor Program Read	1 1 0 x x 1 1
CPU Space	1 1 1 x x x x

Size of Transfer Requested

Byte Transfer	x x x 0 1 x x
Word Transfer	x x x 1 0 x x
3-Byte Transfer	x x x 1 1 x x
Long Word Transfer	x x x 0 0 x x

Type of Cycle **Actually Run by Memory**	**Status Bit** **14 13 12 11 10 9 8 7**
Burst	1 0 0 1 1 0 1 1
Synchronous	x x x 1 1 0 1 1
Asynchronous 32-Bit Port	x x x 1 1 1 0 0
Asynchronous 16-bit Port	x x x 1 1 1 0 1
Asynchronous 8-Bit Port	x x x 1 1 1 1 0
Bus Error	x x x 1 0 x x x
Halt	x x x 0 1 x x x
Retry	x x x 0 0 x x x

Logic Analyzer Symbols

The E2406A configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

Symbols

68030 Labels and Symbols

Label	Symbol	Pattern
STAT	DMA	x x x x x x x x x x x x x x x 0
	USER DATA WRITE	x x x x x x x x x 0 0 1 x x 0 1
	USER DATA READ	x x x x x x x x x 0 0 1 x x 1 1
	USER PRGM READ	x x x x x x x x x 0 1 0 x x 1 1
	SUPR DATA WRITE	x x x x x x x x x 1 0 1 x x 0 1
	SUPR DATA READ	x x x x x x x x x 1 0 1 x x 1 1
	SUPR PRGM READ	x x x x x x x x x 1 1 0 x x 1 1
	CPU SPACE	x x x x x x x x x 1 1 1 x x x x
	OPCODE FETCH	x x x x x x x x x x 1 0 x x 1 1
	READ	x x x x x x x x x x x x x x 1 1
	WRITE	x x x x x x x x x x x x x x 0 1
	(Blank)	x x x x x x x x x x x x x x x x

Label	Symbol	Pattern
SIZ	BYTE	0 1
	WORD	1 0
	3 BYTE	1 1
	LONG	0 0
CYCLE	BURST	1 0 0 1 1 0 1 1
	SYNC	x x x 1 1 0 1 1
	ASYNC 32	x x x 1 1 1 0 0
	ASYNC 16	x x x 1 1 1 0 1
	ASYNC 8	x x x 1 1 1 1 0
	BUS ERR	x x x 1 0 x x x
	HALT	x x x 0 1 x x x
	RETRY	x x x 0 0 x x x
	(Blank)	x x x x x x x x
REQ_AK	BYTE_SYNC	0 1 1 0 1
	BYTE_DS32	1 0 0 0 1
	BYTE_DS16	1 0 1 0 1
	BYTE_DS8	1 1 0 0 1
	WORD_SYNC	0 1 1 1 0
	WORD_DS32	1 0 0 1 0
	WORD_DS16	1 0 1 1 0
	WORD_DS8	1 1 0 1 0
	3BYT_SYNC	0 1 1 1 1
	3BYT_DS32	1 0 0 1 1
	3BYT_DS16	1 0 1 1 1
	3BYT_DS8	1 1 0 1 1
	LONG_SYNC	0 1 1 0 0
	LONG_DS32	1 0 0 0 0
	LONG_DS16	1 0 1 0 0
	LONG_DS8	1 1 0 0 0
	(Blank)	x x x x x

The symbols for the REQ_AK label allow you to quickly identify the size and type of transfer the microprocessor requested and the target system acknowledged.

Using the Inverse Assemblers

The E2406A analysis probe contains two inverse assemblers: IA68030 and IA68030E. The E suffix indicates an enhanced version of the inverse assembler. The enhanced inverse assembler contains all the functions of the other inverse assembler, plus additional features. For information on the enhanced inverse assembler features, see "The enhanced inverse assembler" on page 3-18.
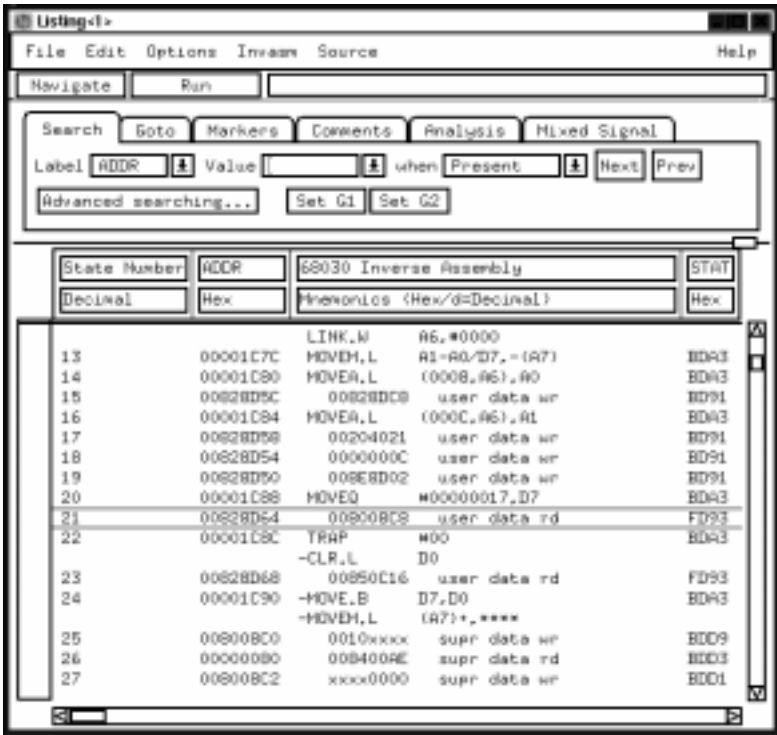
The configuration software checks the logic analyzer during the load process. If the logic analyzer has the appropriate software version, the configuration file loads the enhanced inverse assembler. For information on the logic analyzer operating system version requirements, refer to "Logic analyzer software version requirements" on page 1-5.

The following sections describe the features common to both inverse assemblers.

To display captured state data

The logic analyzer displays captured data in the Listing menu. The inverse assembler disassembles the captured data in a format that closely resembles the assembly source code for your processor.

Captured data is displayed as shown below. This figure shows the data for 16- and 32-bit bus cycles after disassembly.

Listing Menu

The logic analyzers always probe the full 32-bit data bus of the 68030. There are some memory systems that occasionally use only 8 or 16 bits for memory transactions. The size of the bus cycle is indicated by the DSACK signals from memory to the microprocessor. When fewer than the full 32 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x."

The inverse assembler displays the low order bits of the actual byte address in the first column of the display.

The "#" symbol in the state listing for the E2406A refers to an immediate operand.

If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the analysis probe hardware is configured for state analysis. The "Invasm" field will appear at the top of the Listing menu screen when the logic analyzer is configured for state analysis. See Chapter 2 to review the hardware configuration, correct it if needed, and then run the trace again.

To align the inverse assembler

The 68030 microprocessor does not provide enough status information for the inverse assemblers to pick out the first word of an opcode fetch from a series of program reads. To ensure correct disassembly, you may need to point to the 16-bit word that contains the first word of an opcode fetch. Once aligned, the inverse assembler will disassemble from this state through the end of the screen.

Use the following procedure to align the inverse assembler:

1 Select a line on the display that you know contains the first word of an opcode fetch.

2 Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the State Listing, line 13 is the top of the display.

3 Select the appropriate field for your analyzer.

    a For the 16600/700 series analyzers, select "Invasm," then select "Align." A pop-up menu appears with the following choices:

```
High Word
Low Word
```

    b For the other logic analyzers, select "Invasm Options" and use the "Code Synchronization" submenu. The same choices as above are available.

4 Select the choice that identifies which word of the 32-bit long word contains the first word of the instruction fetch, then select "Align."

The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 4.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble

several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

When the 68030 microprocessor is operating in the 32-bit mode, the inverse assembler may lose synchronization due to jumps and branches to odd word addresses. A state decoded as "CP7 Illegal Instruction" or "ORI.B" may also indicate that the inverse assembler has lost synchronization. When this occurs, re-synchronize the inverse assembler by repeating steps 1 through 4.

Inverse assembler output format

The next few paragraphs describe the general output format of the inverse assembler.

Disabling the Cache Memory and MMU

If you want the code (non-burst) to be disassembled, disable the cache memory to insure proper disassembly. Refer to "Configuring the Analysis Probe and Target System" in chapter 1 for additional information.

Interpreting Data

The "#" symbol in the state listing for the E2406A refers to an immediate operand.

The pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing, and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from 68030 instruction prefetch activity, storage qualification, or leaving the MMU enabled.

Examples:

ORI.B   #**,D2 (missing byte operand)

ORI.W   #****,D1   (missing word operand)

ORI.L   #234A****,D3   (missing "lower" word of the operand)

ORI.L   #********,D3   (missing both words of the operand)

In general, asterisks indicate that expected operand fetches are not stored in the logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

The 68030 is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler will display "xx" for the byte of the input data that is ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

Examples:

ORI.B   #03,D1
               xx03 supr program read (microprocessor uses
               lower byte only)

ORI.W   #1203,D1
               1203 supr program read (microprocessor uses both
               bytes of the word)

When the 68030 is operating in a full 32-bit environment, there is a chance that two instructions (16 bits each) will be fetched on one bus cycle. When this happens, the instructions will be displayed on separate lines.

The 68030 microprocessor is a prefetching microprocessor. That is, it will fetch the next two instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, the prefetched words are not used and will be discarded by the microprocessor.

The logic analyzer captures prefetches, even if they are not executed. Therefore, care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor may prefetch one or more long words, one technique to avoid unwanted triggering from unused prefetches is to add "8" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

Prefetch Marking -/?

The analysis probe sends all fetches to the logic analyzer. The inverse assemblers mark branches that may not have been taken with the prefix "?." Unused 68030 program fetches with the prefix "–" to indicate they were not used. Generally, the unused states were prefetched to keep the pipeline flowing before an instruction was executed that flushed the pipeline. Under some circumstances, the inverse assembler can determine which states are unused prefetches:

When instruction execution is a subset of the bus activity captured by the logic analyzer; the 68030 program cache should be disabled and the logic analyzer should not be store-qualifying out any program fetches.

When the logical addresses used on the microprocessor correspond to the physical addresses used off the microprocessor; the 68030 MMU should not be performing any address translation.

There are five categories of instructions which result in prefetch marking:

- The following instructions flush and refill the pipeline, without upsetting the orderly flow of instruction execution:

  ```
  move     ea , SR
  movec   Rn , Rc
  fmove   FPcr     (either way)
  fmovem           (data or control)
  ```

- The following instructions flush the pipeline and refill it from the target address:

  ```
  bra       targ
  bsr       targ
  jmp      <eak>
  jsr       <eak>
  ```
  <eak> is one of the addressing modes where the target is known:

  ```
  xxxx.W
  xxxxxxxx.L
  xxxx(PC)
  ```

- The following instructions may be somewhat ambiguous. They may or may not behave like a branch.

  ```
  bcc       targ
  dbcc      targ
  ```

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your
target software. Included with each message is a brief explanation.

Data Error Displayed if the trace memory could not be read properly on entry into
the inverse assembler. This indicates a hardware error or inverse
assembler software error.

Illegal Opcode Displayed if the inverse assembler encounters an illegal instruction.
Microprocessor action cannot be determined.

The enhanced inverse assembler

The enhanced inverse assemblers contain all the functions of the other inverse assembler (see previous sections), plus additional features.

The configuration software checks the logic analyzer during the load process. If the logic analyzer has the appropriate software version, the configuration file loads the enhanced inverse assembler. For information on the logic analyzer operating system version requirements, refer to "Logic analyzer software version requirements" on page 1-5.

The Invasm menu contains four functions: Load (16600/700 only), Filtering with Show/Suppress selections, Align, and Options. The following sections describe these functions.

Load

The Load function lets you load a different inverse assembler and apply it to the data in the Listing menu. In some cases you may have acquired raw data, in which case the Load function lets you apply an inverse assembler to that data.

Filter

The Filter function brings up a Show/Suppress menu. You can change the settings to specify whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The following figure shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, data I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

The operations which can be shown or suppressed are User/Supervisor Reads/Writes, Program Extension states, Unexecuted Prefetch instructions, Branching, Call/Return, or other instructions. The Call/Return opcodes are JSR, BSR, BKPT, TRAP, RTD, RTR, RTS, RTE, STOP, and ILLEGAL. The

Branching opcodes are BRA, Bcc, JMP, FBcc, TRAPcc, FTRAPcc, CHK, CHK2, and TRAPV.

The following figure shows the Filter menu.

Filter Menu

> If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Align

Align enables the inverse assembler to re-align with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To align the inverse assembler, roll the first incorrectly marked state to the top of the listing screen, then click Align.

Options

The Options menu lets you change the width of the display.

4

Reference

Reference

This chapter contains additional reference information including the signal mapping for the E2406A Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics of the analysis probe
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts
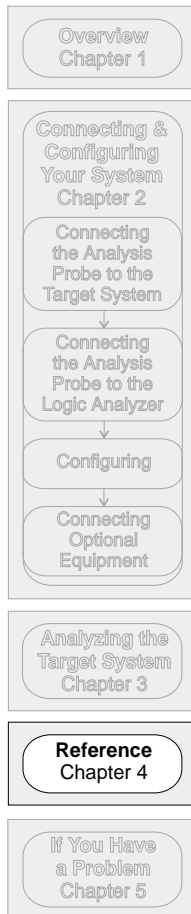
Operating characteristics of the analysis probe

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Operating Characteristics

Microprocessor Compatibility	Motorola MC68030 and all microprocessors made by other manufacturers that comply with Motorola MC68030 specifications.
Microprocessor Package	128-pin PGA. 132-pin PQFP (with option 1CC adapters).
Accessories Required	Option 1CC for PQFP target systems.
Logic Analyzer Required	1660A/AS/C/CS/CP, 1661A/AS/C/CS/CP, 1670A/D, 1671A/D, 16550A (one card), 16554A/55A/56A (two cards), 16555D/56D (two cards), 16600A, 16601A, 16602A.
Probes Required	Five pods of signals are available. All five pods are required for inverse assembly.
Maximum Clock Speed	50 MHz CLK.
Power Requirements	300 mA at +5 Vdc maximum from the logic analyzer. CAT I, Pollution degree 2.
Signal Line Loading	One FCT input plus 3 pF maximum on all lines except AS, CBREQ, CLK, REFILL, and RESET. One TTL input plus 3 pF maximum on the AS, CBREQ, REFILL, and RESET lines. One FCT input and one TTL input plus 3 pF maximum on the CLK line.
Timing Analysis	1 ns setup and 6 ns hold with respect to the falling edge of the target clock (CLK) on all lines except STERM, CBACK, and CIIN.

Operating Characteristics

Microprocessor Operations Displayed	Burst Transfer
	User Data Read/Write
	User Program Read
	Supervisor Read/Write
	Supervisor Program Read
	Bus Grant
	CPU Space Accesses including:
	        Breakpoint Acknowledge
	        Access Level Control
	        Coprocessor Communication
	        Interrupt Acknowledge

Additional Capabilities	The logic analyzer captures all bus cycles, including prefetches. The 68030 microprocessor must be operating with the internal cache memory and MMU disabled for the logic analyzer to provide correct inverse assembly.
Environmental Temperature	Operating 0 to 55 degrees C (+32 to +131 degrees F) Non-operating -40 to +75 degrees C (-40 to +167 degrees F) This product is intended for indoor use only.
Altitude	Operating 4,600 m (15,000 ft.) Non-operating 15,300 m (50,000 ft.)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Theory of operation and clocking

Interface Description

The primary function of a analysis probe is to connect the target microprocessor to the logic analyzer through the probe interface, and to perform any functions unique to that particular microprocessor. The E2406A analysis probe performs this primary function in the following ways:

- By latching and buffering the address, status, and data bus of the 68030 microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.

- By generating the logic analyzer clocks from the appropriate 68030 microprocessor signals and bus conditions.

The central portion of the analysis probe circuitry is the sample flip-flops. Most of the microprocessor signals are fed directly into these flip-flops. The latches on these flip-flops are clocked with an inverted version of the microprocessor CLK.

A version of the AS signal that is delayed approximately 8 ns enables the sample latches. These latches allow a valid sample to be held at the outputs of the sample flip-flop for at least two CLK periods for non-burst transfers. For burst transfers, the valid sample is held for only one CLK period.

The synchronous signal flip-flop latches signals which are valid on the rising edge of the microprocessor CLK. The outputs of this flip-flop are latched by the sample flip-flops one-half clock period after the signals are latched into the synchronous signal flip-flop.

The L clock is a version of the AS signal that is delayed approximately 27 ns. This clock is used to clock non-burst transfers into the logic analyzer.

The K clock is generated in the burst/refill logic by a logical combination of six microprocessor signals: CLK, STERM, CBREQ, CBACK, CIIN, and BERR. This clock is used to clock burst transfers into the logic analyzer.

The BURST/REFILL logic captures the refill signal and sends it to the logic analyzer at the appropriate time.

The figure on the following page shows the block diagram of the E2406A analysis probe.

MISC/E2406B01
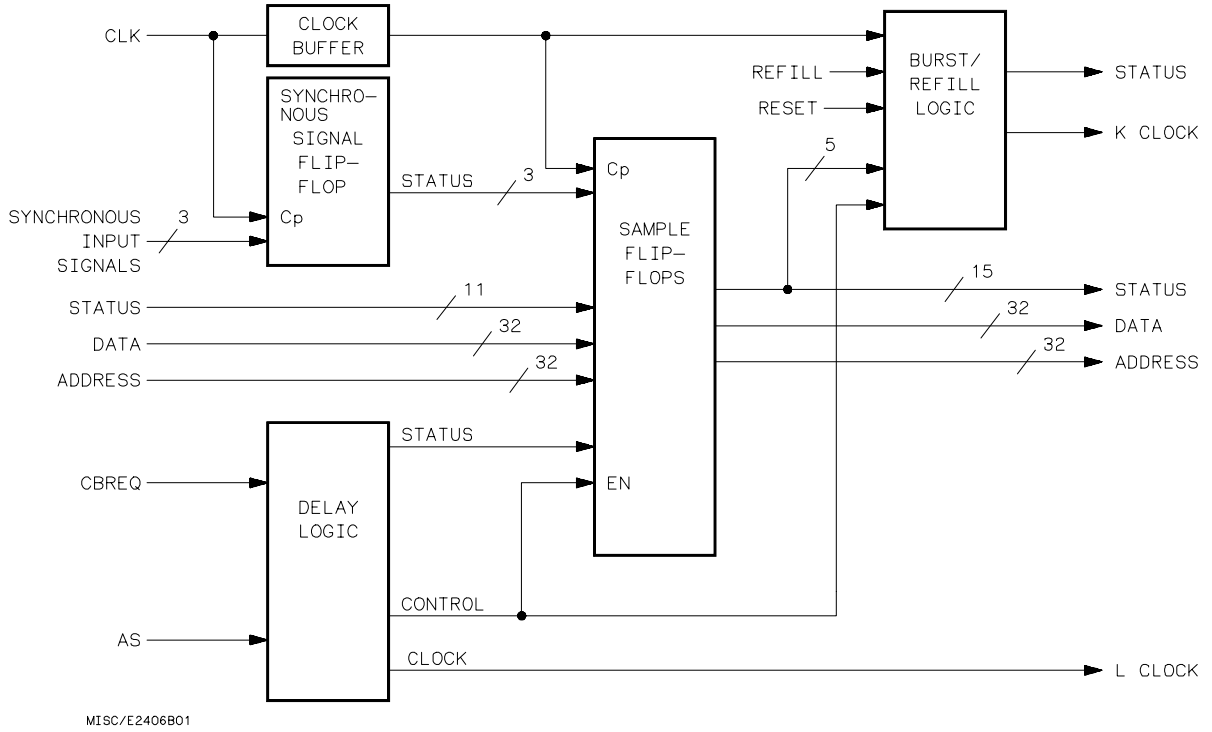
E2406A Block Diagram

Clocking

The 68030's address strobe (AS) indicates that address, function code, size, and R/W state information is on the bus and valid. The logic analyzer uses the rising edge of AS to clock two types of information into the logic analyzer:

- All non-burst information.

- The last long word of a burst transfer.

The rising edge of AS is the rising N clock.

The first three long words of a burst transfer are clocked into the logic analyzer by a second clock (rising K clock).

Signal-to-connector mapping

The following table shows the signal-to-connector mapping.

The interconnections implemented with the E2406A are not direct interconnections. The E2406A analysis probe places digital circuitry between the microprocessor pin and the logic analyzer input.

68030 Signal List

Analysis Probe Pod	Logic Analyzer Probe	68030 Pin	Pin Mnemonic	Label
P4	0	A2	A0	ADDR
P4	1	C4	A1	ADDR
P4	2	D13	A2	ADDR
P4	3	D12	A3	ADDR
P4	4	C13	A4	ADDR
P4	5	C12	A5	ADDR
P4	6	D11	A6	ADDR
P4	7	B13	A7	ADDR
P4	8	B12	A8	ADDR
P4	9	C11	A9	ADDR
P4	10	A13	A10	ADDR
P4	11	C10	A11	ADDR
P4	12	B11	A12	ADDR
P4	13	A12	A13	ADDR
P4	14	B10	A14	ADDR
P4	15	A11	A15	ADDR
P5	0	B9	A16	ADDR
P5	1	A10	A17	ADDR
P5	2	C8	A18	ADDR
P5	3	A9	A19	ADDR
P5	4	B8	A20	ADDR
P5	5	A8	A21	ADDR
P5	6	B7	A22	ADDR
P5	7	A7	A23	ADDR

68030 Signal List (continued)

Analysis Probe Pod	Logic Analyzer Probe	68030 Pin	Pin Mnemonic	Label
P5	8	A6	A24	ADDR
P5	9	B6	A25	ADDR
P5	10	A5	A26	ADDR
P5	11	B5	A27	ADDR
P5	12	A4	A28	ADDR
P5	13	B4	A29	ADDR
P5	14	A3	A30	ADDR
P5	15	B3	A31	ADDR
P3	0	C3	BGACK	STAT
P3	1	L3	R/W	STAT
P3	2	L2	SIZ0	STAT
P3	3	K3	SIZ1	STAT
P3	4	D2	FC0	STAT
P3	5	C1	FC1	STAT
P3	6	D1	FC2	STAT
P3	7	F1	DSACK0	STAT
P3	8	G2	DSACK1	STAT
P3	9	G1	STERM	STAT
P3	10	H1	BERR	STAT
P3	11	H2	HALT	STAT
P3	12	K1	CBREQ	STAT
P3	13	J1	CBACK	STAT
P3	14	L1	CIIN	STAT
P3	15	J13	REFILL	STAT

68030 Signal List (continued)

Analysis Probe Pod	Logic Analyzer Probe	68030 Pin	Pin Mnemonic	Label
P1	0	K13	D0	DATA
P1	1	K12	D1	DATA
P1	2	L13	D2	DATA
P1	3	M13	D3	DATA
P1	4	L12	D4	DATA
P1	5	K11	D5	DATA
P1	6	M12	D6	DATA
P1	7	L11	D7	DATA
P1	8	N13	D8	DATA
P1	9	M11	D9	DATA
P1	10	L10	D10	DATA
P1	11	N12	D11	DATA
P1	12	M10	D12	DATA
P1	13	N11	D13	DATA
P1	14	M9	D14	DATA
P1	15	N10	D15	DATA
P2	0	N9	D16	DATA
P2	1	M8	D17	DATA
P2	2	N8	D18	DATA
P2	3	N7	D19	DATA
P2	4	M7	D20	DATA
P2	5	N6	D21	DATA
P2	6	M6	D22	DATA
P2	7	N5	D23	DATA

68030 Signal List (continued)

Analysis Probe Pod	Logic Analyzer Probe	68030 Pin	Pin Mnemonic	Label
P2	8	M5	D24	DATA
P2	9	N4	D25	DATA
P2	10	N3	D26	DATA
P2	11	M4	D27	DATA
P2	12	N2	D28	DATA
P2	13	M3	D29	DATA
P2	14	L4	D30	DATA
P2	15	N1	D31	DATA
P3	L CLK	J2	AS	L CLOCK
P2	K CLK	*	*	K CLOCK

* Derived from a logical combination of the CBREQ, CBACK, STERM, CIIN, BERR, and CLK signals.

Circuit board dimensions

The following figure gives the dimensions for the analysis probe assembly. The dimensions are listed in inches and millimeters.
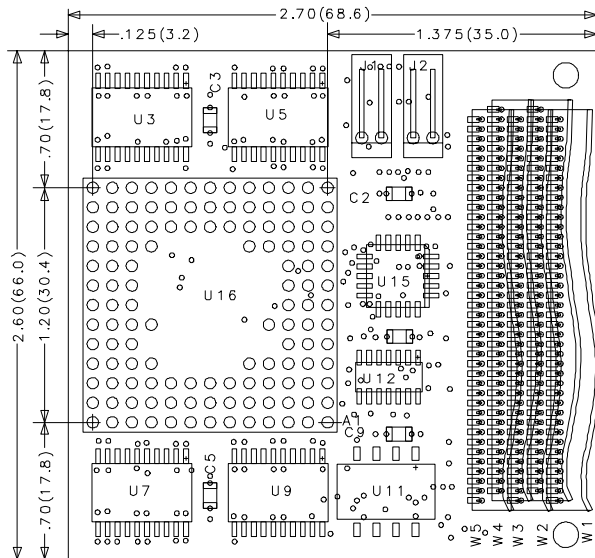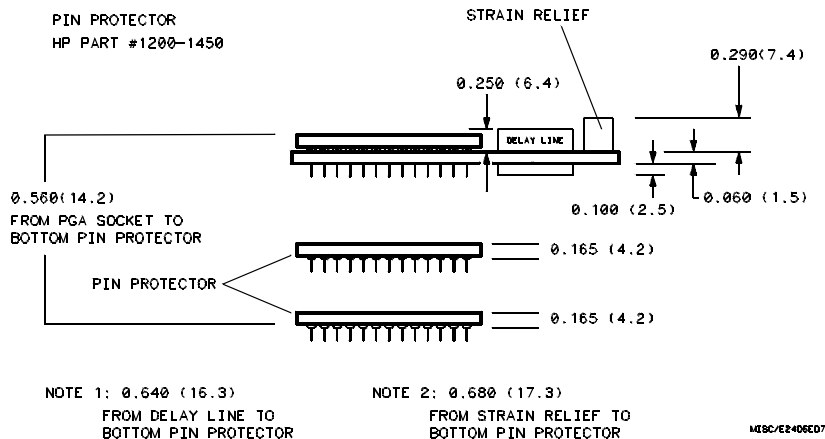
Circuit Board Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

Part Number	Description
E2406-69501	Exchange Board/Cable Assembly
E2406-68705	Inverse Assembler Disk Pouch
E2406-60002	Circuit Board/Cable Assembly
01650-63206	100 kOhm Termination Module
1200-1450	Pin Protector

HP E2406A Motorola 68030 Analysis Probe

If You Have a Problem

If You Have a Problem
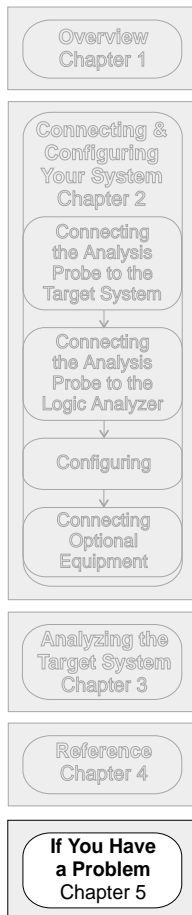
Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Agilent Technologies Service Center.

CAUTION   When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

☐ Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.

☐ Adjust the threshold level of the data pod to match the logic levels in the system under test.

☐ Use an oscilloscope to check the signal integrity of the data lines.

Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also   See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

☐ Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.

The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

☐ Check for loose cables, board connections, and analysis probe connections.

☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.

☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

☐ Ensure that you are following the correct power-on sequence for the analysis probe and target system.

    1 Power up the analyzer and analysis probe.

    2 Power up the target system.

If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

☐ Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.

☐ Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.

☐ Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

☐ Do a full reset of the target system before beginning the measurement.

Some analysis probe designs require a full reset to ensure correct configuration.

☐ Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.

See "Capacitive Loading" in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

☐ Ensure that you have sufficient cooling for the microprocessor.

Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

☐ Remove as many pin protectors, extenders, and adapters as possible.

☐ If multiple analysis probe solutions are available, use one with lower capacitive loading.

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

☐ **Check the activity indicators for status lines locked in a high or low state.**

☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

☐ Verify that all microprocessor caches and memory managers have been disabled.

In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

☐ Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

☐ For the 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.

☐ For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.

Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

☐ Adjust the skew in the Intermodule menu.

You may be able to specify a skew value that enables the event to be captured.

☐ Change the trigger specification for modules upstream of the one with the problem.

If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.
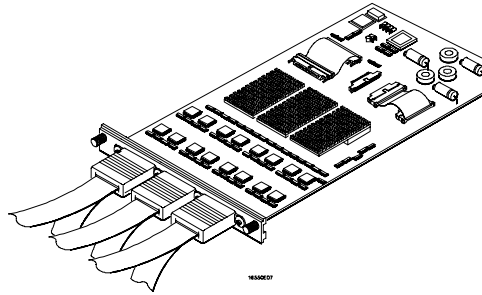
Cable Connections for One-Card 16550A Installations
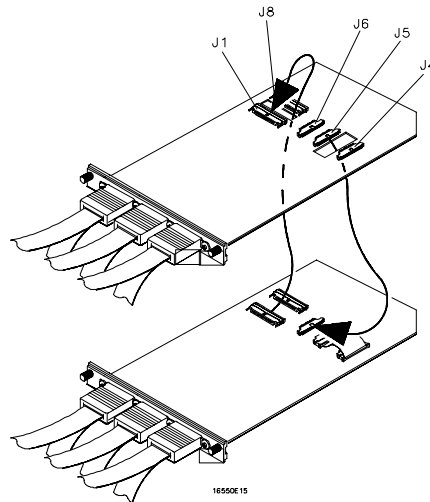
Cable Connections for Two-Card 16550A Installations

See Also The *16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on 16554A, 16555A/D, and 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.
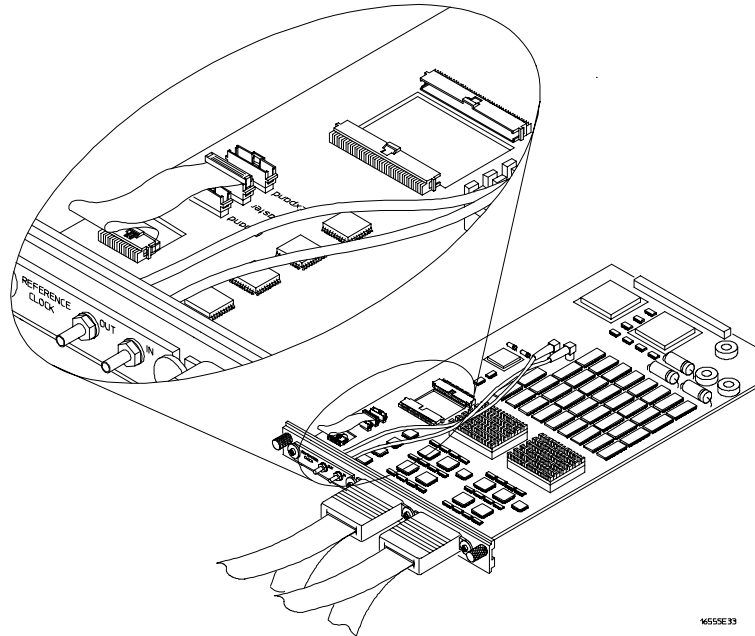
Cable Connections for One-Card 16554/55/56 Installations

16554E06
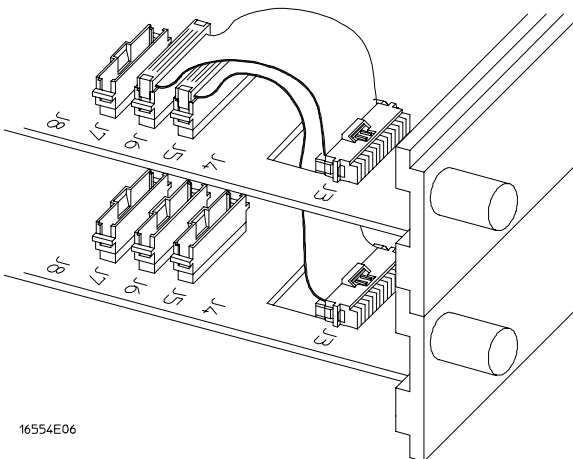
Cable Connections for Two-Card 16554/55/56 Installations

16555E36
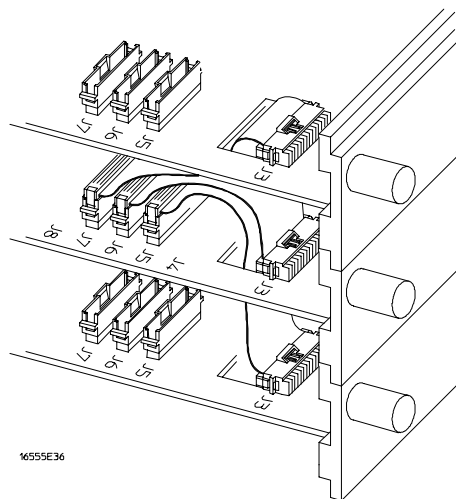
Cable Connections for Three-Card 16554/55/56 Installations

See Also

The 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.

☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.

☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

☐ When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe   A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board   A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter   A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module   An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe   An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter   Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable   A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable   Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper   Moveable direct electrical connection between two points.

Mainframe Logic Analyzer   A logic analyzer that resides on one or more board assemblies installed in an 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header   A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface   See Analysis Probe.

Preprocessor Probe   See Analysis Probe.

Probe adapter   See Elastomeric Probe Adapter.

Processor Probe   See Emulation Probe and Emulation Module.

Prototype Analyzer   The 16505A prototype analyzer acts as an analysis and display processor for the 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant   A software program that guides you through the

process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector.   See Jumper.

Stand-alone Logic Analyzer   A stand-alone logic analyzer has a pre-defined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board   A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter   An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

Index

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Safety Symbols

⚠

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

⚡

Hazardous voltage symbol.

⏚

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.