Technical Note

VXIbus Overview

Introduction

Prior to 1987 there existed only one major architecture standard for instruments...the General Purpose Interface Bus (GPIB). Although the GPIB was widely used, it did not address the need for portable test stations, nor for the market demand for faster, more cost-effective test solutions. In 1987, a consortium of test and measurement companies introduced VXIbus...a new standard instrument architecture. The VXIbus (VMEbus eXtensions for Instrumentation) was developed to meet the need for portable applications and to provide a standard modular open architecture for integrating into the traditional GPIB test system and for stand-alone applications. It was designed to be an open architecture standard for instruments on a card, allowing an instrument from any manufacturer to operate in the same mainframe as another manufacturer's instrument.

Rather than design an entirely new architecture, the VXIbus Consortium decided to enhance an existing standard that was well accepted in the data acquisition and high-speed computer markets...The VMEbus.

The VMEbus architecture, known for its excellent computer backplane, high-speed data rates of 40 MB/s, along with the necessary communication protocols, made it ideal for building instrument systems for high throughputs. VXIbus incorporates the ease-of-use features of intelligent GPIB instruments (for example, ASCII-level programming) into its message-based device, and also takes advantage of the high throughput capability of VME devices, which are programmed and communicate directly in binary (register-based devices).

Although VME is an excellent computer backplane, it is not adequate for instrumentation without further standardization. The VXIbus Consortium enhanced the VMEbus standard by further defining parameters to allow users to easily configure a workable system. Some of the enhancements added to the VMEbus standard were:

- Larger card options for higher performance instruments and to add shielding.
- Defining all signals on the backplane, avoiding problems due to user-defined signals on the VMEbus.
- Addition of EMC, cooling and power specifications to further ease system integration.
- Definition of communication protocols to ease integration with existing test systems.
- Addition of voltages for high-performance instruments.

VXIbus Basics

A VXIbus system or subsystem consists of a VXIbus mainframe, VXIbus devices, a VXIbus slot 0 card, VXIbus resource manager, and host controller. The slot 0 takes care of backplane management and includes things such as clock sources and arbitration for data movement across the backplane. The module that goes into this slot must perform these hardware functions in addition to its normal functions. The resource manager configures the modules for proper operation whenever the system is powered on or reset, allowing the user to build the test system software from a known starting point. The resource manager is not involved with the VXIbus system once normal operation begins. The VXIbus mainframe houses the VXIbus instruments and contains the power and cooling mechanism for these instruments, as well as the communication backplane.

The VXIbus was not designed to replace any existing standard, but instead as an additional tool to help in overall test or data acquisition solutions. To this end several methods of communicating with VXIbus devices were defined, enabling VXIbus solutions to be integrated with VMEbus, GPIB or as stand-alone portable solutions.

Specification Overview

MECHANICAL

The VXIbus specification defines four module sizes. The two smaller sizes, A and B, are the defined VMEbus module sizes and are true VMEbus modules in every sense. The two larger sizes, C and D, are for higher performance instrumentation. Increased module spacing in the C- and D-size systems makes it possible to fully shield sensitive circuits for high performance measurements.

The C-size VXIbus footprint has become the most common size today because it keeps systems to a smaller size than D, and allows the performance of VXIbus to be utilized (A and B being VMEbus devices). The only real D-size solutions found today are in large functional testers that include instruments or custom circuits that were developed on D-size because of real estate advantages. B-size solutions are available, but consist mainly of VMEbus type or low-performance instruments, and do not utilize the benefits of the VXIbus standard. Ninety percent of VXIbus products on the current market conform to the C-size footprint.

ELECTRICAL

Additional power supply voltages for powering analog and ECL circuits and instrumentation buses for measurement synchronization and triggering were added to the existing VMEbus signal, along with an analog sum-bus and a set of local bus lines for private module-to-module communication.

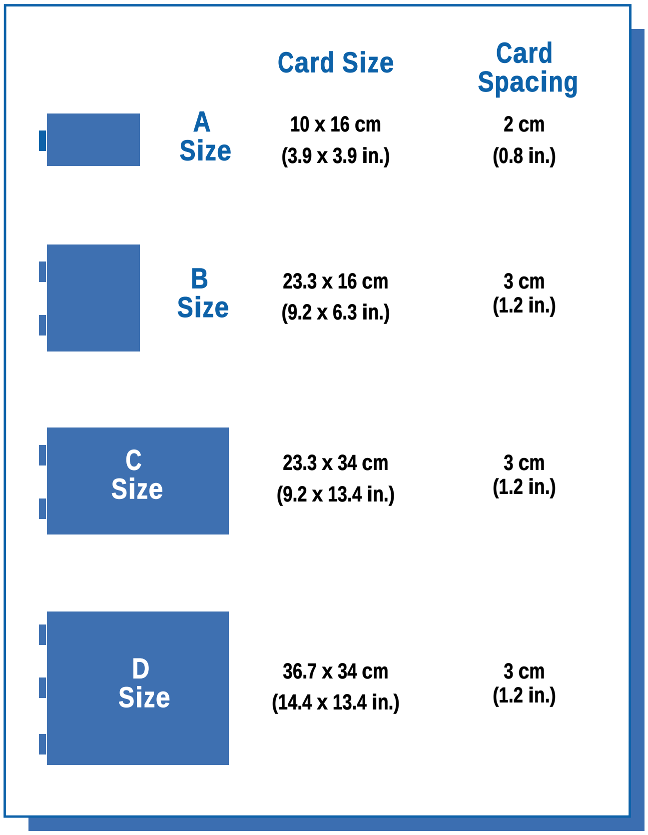

Figure 1

The VXIbus specifies three 96-pin DIN connectors called P1, P2, and P3. The P1 connector, the only mandatory one in VME or VXIbus, carries the data transfer bus (up to 24 bits addressing and 16 bits data), the interrupt bus, and some power.

P2

The optional P2 connector, available to all card sizes except A-size, expands the data transfer bus to its full 32-bit size. It also adds four additional power supply voltages, the local bus, the module identification bus (allows a VXIbus module's slot number to be determined), and the analog summing bus (a current summing bus that runs the length of the backplane). Also, there are TTL and ECL trigger buses (running the length of the backplane with four trigger protocols defined) and a 10 MHz differential ECL clock signal (buffered to each slot).

P3

The optional P3 connector, available only on D-size, expands P2 resources for specialized applications. It provides 24 more local bus lines, additional ECL trigger lines, and 100 MHz clock and star trigger lines for precision synchronization.

Local Bus

The local bus adds significant capability to VXIbus measurement systems. It is a very flexible daisy-chain bus structure. Every inner slot in a VXIbus mainframe has a set of very short, 50 ohm transmission lines running between adjacent slots on either side. The local bus is 12 lines wide each direction through the P2 connector and an additional 24 lines wide through the P3 connector. This bus allows for adjacent modules to perform private communication.

Table 1 shows the actual pin outs of P1 and P2 for reference. P3 has not been shown, because of lack of use, but can be found in the VXIbus specifications.

EMC

The VXIbus specification stipulates radiated and conducted EMC limits for both generation and susceptibility. The importance of this part of the VXIbus specification cannot be overstated. EMC limits ensure that modules containing sensitive electronic circuits perform to expectations without interference from any other module operating in the system.

POWER AND COOLING

In a typical IEEE-488 rack-and-stack or VMEbus system, the system integrator must take a rigorous approach to ensure an environment cool enough for proper operation. Each instrument's power dissipation, airflow and placement in the rack must be considered. The rack's cooling capability must be factored in as well.

To ensure adequate cooling in a VXIbus system, the design process is simpler. Every vendor's mainframe specification sheet provides a cooling graph for the worst-case module configuration. It is specified in terms of pressure across the module versus the airflow delivered. Each instrumentation manufacturer must also specify the airflow and back pressure required by the instrument for proper operation (normally for a 10˚C rise in temperature). The user would then plot the point of the module's airflow and back pressure specifications on the mainframe's cooling curve and, if located within the boundaries of the curve, the module is guaranteed to be compatible with the mainframe.

The power specification is another way the VXIbus makes the system integrator's job easier. Each VXIbus mainframe is specified for power delivered. Each power supply level has a peak DC current delivery and peak-to-peak dynamic current delivery. When selecting modules, voltage levels and current requirements are compared to the mainframe's capability. The VXIbus dynamic current specification ensures that the selected modules will not induce more ripple noise on the mainframe's power supply lines than any module is required to withstand. (Figure 2)

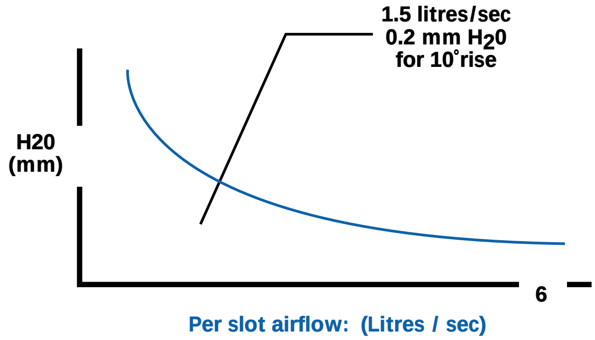

Figure 2

COMMUNICATIONS

Communications is another area of VXIbus standardization. VXIbus specifies several device types and protocols as well as communication handshakes, however, it leaves things flexible as far as how to control the VXIbus mainframe and devices -- open architecture. A VXIbus system or sub-system can be controlled using either an embedded or an external computer that can be operating system or platform independent, i.e., Windows, DOS, UNIX. If an external computer is used, the interface to the VXIbus mainframe can also be flexible, i.e., GPIB/VXI, MXI/VXI, RS-232/VXI, Ethernet/VXI. Any approach used has its own set of advantages and disadvantages dependent upon the overall system requirements. Each VXIbus mainframe must have a slot 0 card. Because of available real estate, the slot 0 functions are typically integrated with the interface to the external controller or with the embedded controller.

There is one unique logical address (ULA) per VXIbus device (numbered from 0 to 255) and up to 256 devices in a VXIbus system. Typically a voltmeter, switch, or signal generator is a single device. It is important, however, to understand that ULAs or VXIbus instruments have no relationship to individual VXIbus card slots. The VXIbus specification allows for several devices per card slot for improved portability and integration, or one instrument per several card slots for densely populated instruments.VXI modules must have registers located at specific addresses, as shown in Figure 3. The upper 16kB of the 64kB A16 address space are reserved for VXIbus devices.

The two most common types of VXIbus devices are register and message-based. A comparison is shown below.

VXIbus P1 Pin Definitions: Slot 0-12

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DSO*	BR1*	LWORD
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT*(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

VXIbus P2 Pin Definitions: Slot 0

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	ECLTRG0	+5V	CLK10+
2	-2V	GND	CLK10-
3	ECLTRG1	RSV1	GND
4	GND	A24	-5.2V
5	MODID12	A25	LBUSC00
6	MODID11	A26	LBUSC01
7	-5.2V	A27	GND
8	MODID10	A28	LBUSC02
9	MODID09	A29	LBUSC03
10	GND	A30	GND
11	MODID08	A31	LBUSC04
12	MODID07	GND	LBUSC05
13	-5.2V	+5V	-2V
14	MODID06	D16	LBUSC06
15	MODID05	D17	LBUSC07
16	GND	D18	GND
17	MODID04	D19	LBUSC08
18	MODID03	D20	LBUSC09
19	-5.2V	D21	-5.2V
20	MODID02	D22	LBUSC10
21	MODID01	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID00	D31	GND
31	GND	GND	+24V
32	SUMBUS	+5V	-24V

VXIbus P2 Pin Definitions: Slot 1-12

Pin Number	Row A Signal	Row B Signal	Row C Signal
1	ECLTRG0	+5V	CLK10+
2	-2V	GND	CLK10-
3	ECLTRG1	RSV1	GND
4	GND	A24	-5.2V
5	LBUSA00	A25	LBUSC00
6	LBUSA01	A26	LBUSC01
7	-5.2V	A27	GND
8	LBUSA02	A28	LBUSC02
9	LBUSA03	A29	LBUSC03
10	GND	A30	GND
11	LBUSA04	A31	LBUSC04
12	LBUSA05	GND	LBUSC05
13	-5.2V	+5V	-2V
14	LBUSA06	D16	LBUSC06
15	LBUSA07	D17	LBUSC07
16	GND	D18	GND
17	LBUSA08	D19	LBUSC08
18	LBUSA09	D20	LBUSC09
19	-5.2V	D21	-5.2V
20	LBUSA10	D22	LBUSC10
21	LBUSA11	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24V
32	SUMBUS	+5V	-24V

Table 1

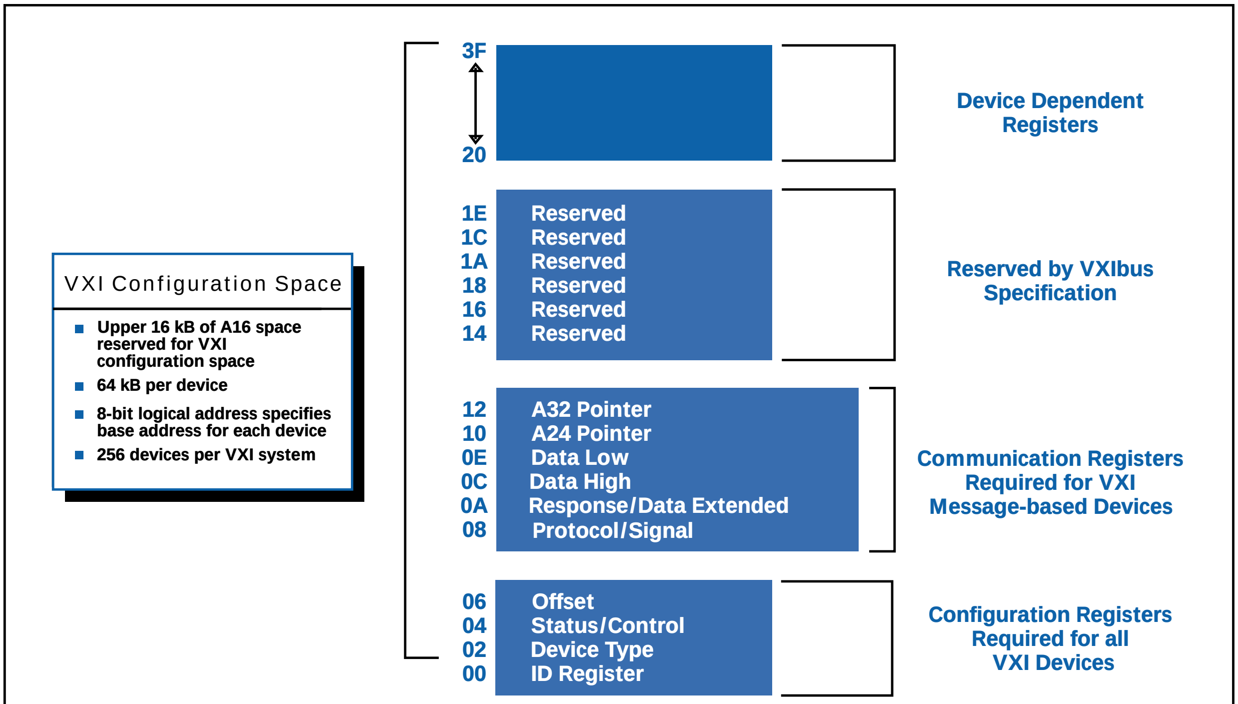

Figure 3

Register-based Device

A register-based device is the simplest VXIbus device and most often is used as the basis for simple modules. A register-based device communicates only through register reads and writes. Configuration is controlled by VXIbus-defined configuration elements but programmed through device-dependent registers.

Message-based Device

A message-based device is typically the most intelligent device of a VXIbus system. High-performance instruments are typically available as message-based devices. Besides the basic configuration registers supported by the register-based device type, the message-based device has common communication elements and a Word Serial Protocol to allow ASCII-level communication with other message-based modules. This allows easier multi-manufacturer support, though at some sacrifice in speed to interpret the ASCII messages. Typically, a message-based device uses a microprocessor and is more costly than a register-based device. Since the Word Serial Protocol mandates only a byte transfer per transition, which then must be interpreted by the on-board microprocessor, message-based devices are typically limited to IEEE-488 speeds. However, optional register-based access may be included on the module to bypass this bottleneck, while allowing ease of instrument set-up through word serial protocol.