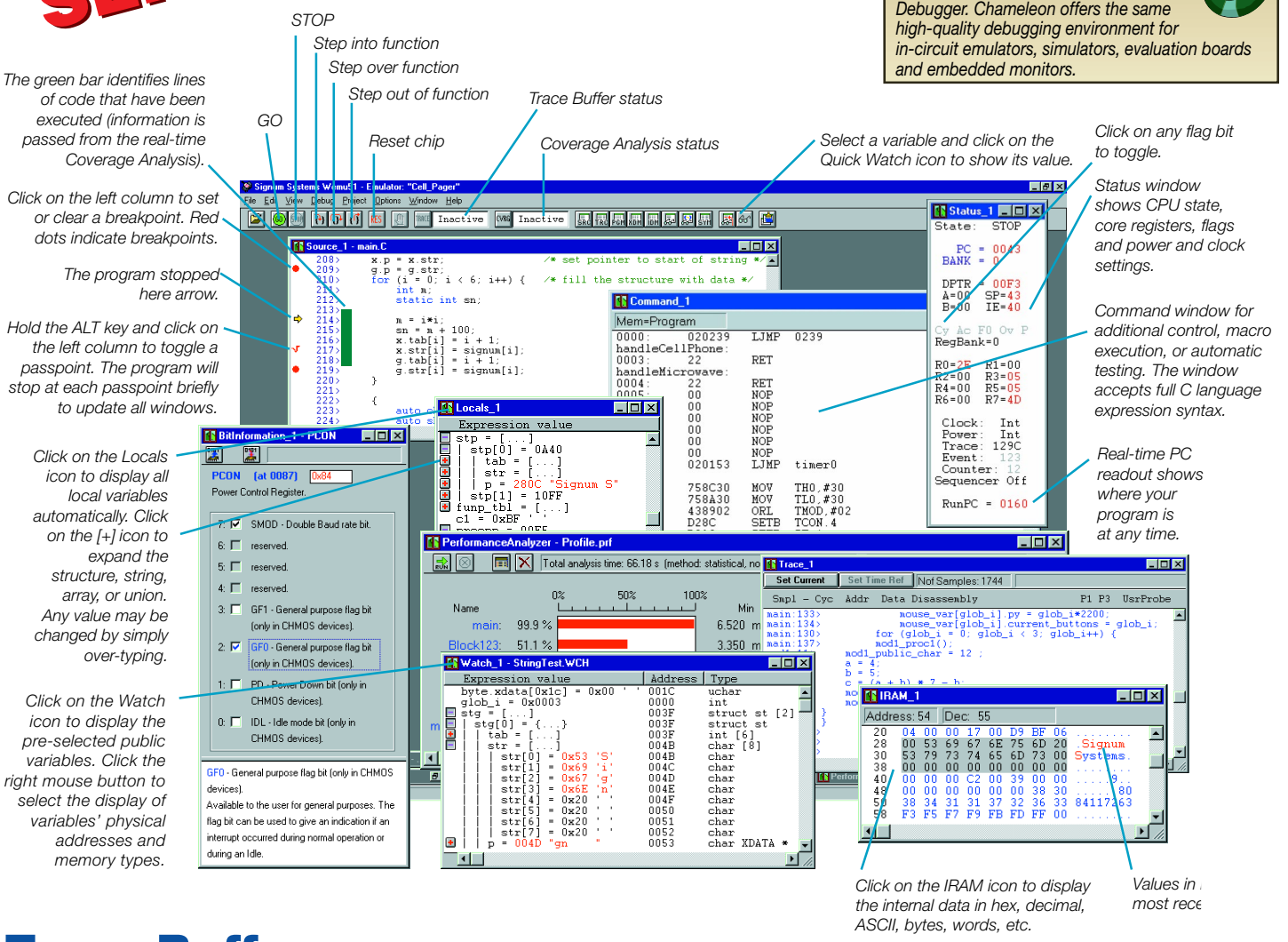
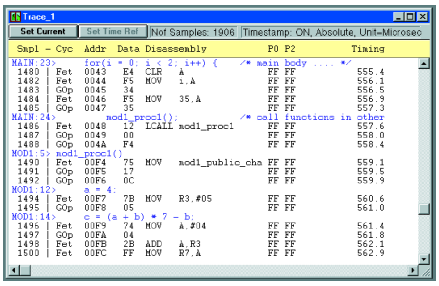
8051 SERIES

CHAMELEON® SOURCE-LEVEL DEBUGGER

All 8051-Series In-Circuit Emulators work with Signum's Chameleon® Source-Level Debugger. Chameleon offers the same high-quality debugging environment for in-circuit emulators, simulators, evaluation boards and embedded monitors.



Trace Buffer



The real-time trace buffer stores up to 32K frames of program execution history. Each fra bits wide and contains the HLL source line, cycle type, address, data, instruction executed, four 8-bit ports (P0-P3 or others), time stamp, and 8-channels of miscellaneous signals from user's target. Using trace pre-filtering setup it is possible to selectively trace only some parts of the program. With the post-filtering setup the information in the trace buffer may be further filtered to hide any unwanted frames so that the trace window is easy to read and understand. Using filters you may, for example, configure the trace buffer to capture only execution of interrupts (ISRs), or obtain a complete history of all writes or reads to a communication buffer or a mail box.

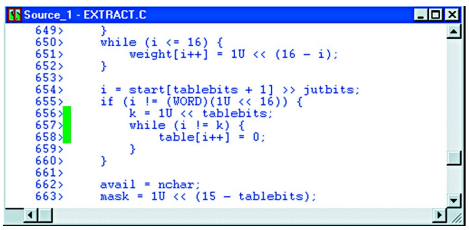
LAN Support and Remote Debugging

All 8051-Emulators support operation over a network. The IceServer™ option allows you to work with ICE connected to a networked computer from any workstation on the network. This allows you to run a remote debugging session or to take a peek at what is happening in the lab or at a test site.

SIGNUM SYSTEMS

For More Information: **www.signum.com** **1-800-838-8012**

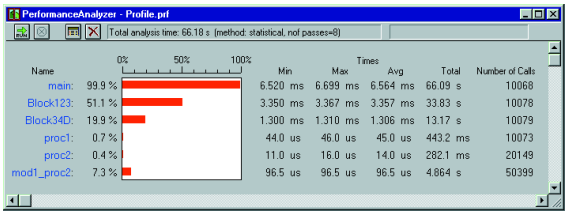
Coverage Analysis



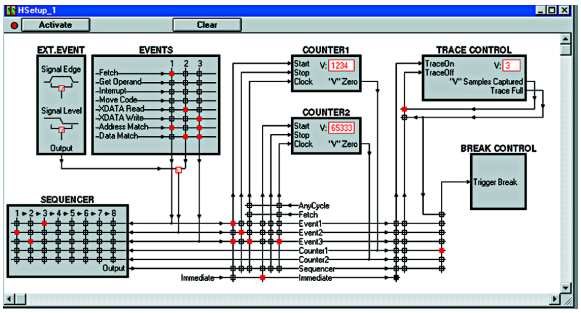
Coverage Analysis uses special hardware to capture in real-time all addresses the program has executed, written to, and read from. This feature is used for QC/QA purposes to identify areas of code that weren't tested. It can also be used during development to identify the program flow and out-of-bounds or illegal memory accesses. The results of coverage analysis are immediately passed to the Source window to graphically identify executed portions of the code. An extensive report is also generated for documentation purposes.

Performance Analysis

Performance Analysis uses the ICE hardware to keep track of how many times the user's program enters a designated area and how much time it spends there. Up to eight memory areas may be measured at one time. Based on the results of performance analysis, a bar graph is generated to graphically show where the program spends most of the time. Memory areas to be measured can be defined directly from the Symbol Explorer window by dragging and dropping definitions of the areas to the Performance Analysis Settings dialog box.



Complex Events



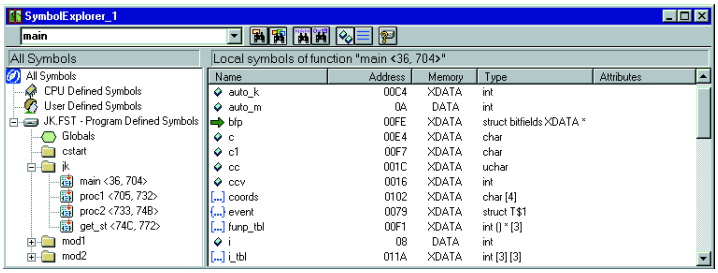
The Complex Events window is used to graphically program the three available complex events and to define how these events will be used for breakpointing and trace filtering. Each event is capable of comparing in real-time the address bus, data bus, and cycle type. This can be used, for example, to detect the writing of values between 44 and 55 to one or more specified locations in memory. Once a complex event is defined, it may be passed to one of the two available 16-bit counters to create a delayed breakpoint or trace trigger. With the use of the 8-level sequencer any combination of events and counters may be mixed to achieve a trigger based on a predetermined sequence of events. With the optional User Probe, external signals may be used to define event conditions and used to filter trace or stop program execution.

Dual Ported Memory

The ICE is equipped with a dual ported memory, which means that the executing CPU and the PC host can access the emulation memory at the same time. Since the CPU has to run in real-time, a special circuitry decodes possible bus collisions and gives higher priority to the executing CPU. This on-the-fly access to emulation memory allows debugging without ever stopping the CPU. Any code or external data variables may be read or written to without disturbing the running program. So now, you can examine error counters, mail boxes, buffer pointers and instantly change the motor speed, temperature or servo parameters by simply modifying their values in the Memory or Watch windows.

Symbol Explorer

The Symbol Explorer window displays information about all symbols and source code lines defined in user's application as well as symbols defined manually by user and in the emulated processor definition file. The window can be used to synchronize view with SOURCE window at specified variable, function, program block or module, to search for symbols, to define new symbols or to show structure of the user's application. New symbol can be added to Watch window by simply dragging and dropping the symbol from the Symbol Explorer window. Drag and drop feature can be also used to define the memory area to be measured by the Performance Analysis.



Virtual Prototyping

The Virtual Interface Panel Environment (Viper®) allows you to build custom user interfaces for your embedded applications using drag-and-drop virtual hardware components. Viper® is ideal for rapid prototyping and experimentation. You can also use Viper® to develop custom user interfaces for debugging and testing applications. A single Viper® can communicate over the network with multiple Chameleon® sessions allowing you to control multiple processors at different locations at the same time.

8051 SERIES

Features

- Network support for remote debugging
- Memory display and edit while executing in real-time
- Trace display during execution
- HLL debug for C-51 and PL/M-51 supports all major compiler vendors
- Pass-points to monitor internal RAM, variables and Registers while running
- Real time transparent emulation up to 60 MHz
- 32K frames (80 bits wide) of execution Trace Buffer with time stamp
- In-line symbolic assembler and disassembler
- Up to 256K of overlay Program RAM with bank switching
- Up to 64K of overlay External Data RAM
- Memory mapping on 256 byte boundaries
- Up to 256K of real-time hardware breakpoints
- Breakpoints on Register and internal RAM values
- Complex Events to trigger Breakpoints or Trace logic
- Two 16 bit Pass Counters with stop and reload control
- 8 level hardware event Sequencer for more precise triggering
- 8 channel user logic state analyzer to monitor misc. signals
- External trigger input and outputs
- Program performance analysis and histograms
- Coverage Analysis to identify dead code and un-initialized variables
- Wide range of uP pods to emulate virtually all 8051 family members
- Windows 95 / 98 / NT / 2000 compatible
- 115 kBaud serial download (64K program downloads in 14 sec.)
- Parallel port download (64K program downloads in 5 sec.)

Supported Microcontrollers:

Intel	***80C31, 80C32, 8xC51, 8xC52, 8xC54, 8xC58, 8xC51FA/FB/FC, 8xL52, 8xL54, 8xL58, 8xL51FA/FB/FC, 80C51GB***
Atmel	***89C51, 89C52, 89LV51, 89LV52, 89C1051, 89C2051, 89SC4051, 89S8252***
Dallas Semiconductor	***80C310, 80C320, 8xC520, 8xC530***
TEMIC	***8xC51, 80C31X2, 80C32X2, 8xC51X2, 8xC52X2, 8xC54X2, 8xC58X2, 8xC51RA2, 8xC51RB2, 8xC51RC2, 8xC51RD2, 8xC51U2***
OKI	***80c31, 80C32, 8xC51, 8xC52, 8xC154***
Philips/Signetics	***80C31, 80C32, 8xC51, 8xC52, 8xCL31, 8xCL32, 8xCL51, 8xCL52, 8xC51FA, 8xC51FB, 8xC51FC, 8xC51RA+, 8xC51RB+, 8xC51RC+, 8xC51RD+, 8xCL410, 8xC451, 8xC524, 8xC528, 8xC550, 8xC552, 8xC562, 8xC575, 8xC576, 8xCL580, 8xC652, 8xC654, 8xV748, 8xC749, 8xC750, 8xC751, 8xC752, 8xC781, 80C851***
Infineon/Siemens	***80C515, 80C535, 8xC515A, 8xC517A, 80C537, C500 family***
Silicon Systems	***K246, 73D2910, 73D2912, 73D2918***
Maximum emulation speed	***20 MHz, 40 MHz or 60 MHz***
Size	***260 mm wide, 260 mm deep, 64 mm high***
Max. Emulation Program Memory	***64 Kbytes standard, 256 Kbytes optional***
Max. Emulation External Data Memory	***64 Kbytes***
Program Memory mapping	***256 byte boundary***
Data Memory mapping	***256 byte boundary***
Pass Counters	***Two, 16 bit each with Stop/Reload control***
Trace buffer	***32 K deep, 80 bits wide with filtering control***
Real-Time Clock Stamp	***32-bit, 100 ns resolution with Absolute, Relative and Delta Modes***
Sequencer	***8 level hardware***
User probe	***8 channel logic input, 1 trigger input, 6 trigger outputs (Events, Pass Counters, Sequencer)***
Host interface	***Parallel (LPT1-LPT2), Serial (Com1-Com4)***
File upload/download format	***Intel HEX, Intel AOMF, Archimedes, IAR, Franklin , Keil, Tasking, and others***

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For More Information

1-800-838-8012

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