STEP 3

STEP ENGINEERING

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OPERATING AND MAINTENANCE MANUAL

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MANUAL

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WARRANTEE

Your Step instrument has been thoroughly inspected and tested prior to shipment. It is guaranteed to be free from defects in material and workmanship. Before applying power to the unit, inspect the unit for any signs of shipping damage. Any such damage should be reported immediately to the freight carrier and an appropriate claim filed with the carrier.

CAUTION: This unit is designed for operation from:

115V ± 10% 40-440 Hz AC power source only, U. S. Versions; or
220V ± 10% 40-440 Hz European versions.

Connection to any other power source may cause permanent damage.

All products manufactured by Step Engineering, Inc. are warranted to be free from defects, material and workmanship for a period of 180 days from date of shipment to the original purchaser. Under this warrantee, the obligation of Step Engineering, Inc. is limited to servicing any equipment returned to the factory for that purpose and restoring the equipment to its original specifications.

Step Engineering's liability is limited to the repair or replacement at our option of any defect of the product and shall in no event include incidental or consequential damages of any kind. If, in our opinion, the product must be returned to the factory, Step will issue a Return Material Authorization, RMA, for the repair. No return will be accepted without such an authorization.

NOTE: The RMA number must appear on all correspondence and paperwork.

Freight must be prepaid and insured. After repairs, the instru-

ment will be returned to you freight prepaid and insured. If a failure is caused by misuse, operation, or environment exceeding specifications, or unauthorized modification by the customer, a cost estimate will be submitted and repairs performed and billed upon request. Out of warranty repairs will be handled in the same manner. This quarantee is void if the serial number is removed.

PREFACE

This manual is designed both as a guide for the first-time user and as a reference book.

Topics include:

- How to unpack and test a new instrument
- How to organize the WCS memory
- How to connect the instrument to the system being developed
- How to enter STEP-N commands and interpret CRT displays
- How to trouble shoot the STEP-N instrument when it is not operating properly

A detailed discussion of any particular application or processor design technique is beyond the scope of this manual.

NOTE: This manual is useful with either Step-2 or its successor instrument, Step-3. Step-3 is exactly a super-set of Step-2 functionally but has added features, improved design, and some mechanical changes.

In the text, the usages "Step-N" and "Step Instrument" refer to features found in both Step-2 and Step-3.

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SECTION I

CHECKOUT AND OPERATING
YOUR NEW STEP INSTRUMENT

1.1 UNPACKING

No special instructions are required for unpacking the STEP instrument. Use proper carton-opening devices and due care in opening the carton. If the shipping container has been damaged, request that the carrier's agent be present while the instrument is being unpacked and inspected. Inspect the mainframe for damaged I/O connectors, bent or broken case housing, and for any apparent external damage.

Your unit may have several ROM Simulation modules in sealed plastic containers. These modules should be carefully inspected for broken housings and bent or broken pins on the cable terminals (DIP plug).

Place the STEP-N instrument on a clean work surface with adequate space around the chassis to allow free air flow for cooling. Before turning on the instrument, remove the side panel and check to make sure that all boards are securely plugged into the back-plane, and properly seated in the card cage. Also check to make sure that IC's are firmly seated in their sockets. Connect the STEP-N instrument to: a 115 volt AC power source with the power cord provided - U. S. versions; a 220 volt AC power source with the power cord provided - European versions. The unit is now ready for operation.

1.2 GROUNDING

It is important that the STEP-N logic ground always be connected to chassis ground at only one point in the system, so that ground loops are avoided. STEP is usually grounded via the target processor.

Before connecting STEP-N to any other equipment, make sure that STEP's grounds are properly interconnected. This is accomplished by means of the banana jacks on the side of the STEP-2 unit. Two jacks are provided, one for logic ground, a black jack, and one for chassis ground, a white jack. Chassis ground is directly connected to the 3rd wire ground of the STEP power cord. When the unit is shipped, the chassis jacks are connected together by means of a shorting wire, but the wire should be removed for use.

In the STEP-3 instrument, the jacks are located on the rear of the unit. Black is logic ground and green is chassis ground and earth ground. A shorting bar ties them, until actual use.

1.2.1 CONNECTION TO THE TARGET MACHINE

Connection should be made in the following manner:

1) Connect the black STEP-N jack, logic ground, to the logic ground of the target processor system using a heavy cable or strap. This insures that the logic grounds to the two systems remain firmly tied together even when other parts of STEP are being connected to the system. It avoids any possibility of shock damage to either piece of equipment.

2) Determine whether the target processor has its own earth chassis ground tied into logic ground. If chassis ground and logic ground are tied together on the target processor, or on the power supply of the target processor, remove the connection between the STEP chassis and logic ground on the two jacks on STEP-N.

1.2 (contiuned)

CAUTION: To avoid ground loops and possible equipment failure, chassis ground must be tied into the system at only one point. If chassis ground is not tied to logic ground at at least one point in the system, logic ground may float with respect to chassis ground causing a shock hazard.

1.3 OPERATION & CHECKOUT

1.3.1 SETUP

Due to its versatility, STEP-N permits over 200 different instrument organizations. The following setup procedure is a nominal case:

1) Determine number of memory boards and memory types: MEM128 or MEM32. If you are not sure what memory boards are installed in your instrument, check the configuration sheet shipped with the unit. The checkout parameters to be used are shown on chart 1.3.1, Checkout Parameters.

2) Set the switches properly on the side of each memory board as follows:

	S1	S2	S3	S4	S5	S6
six (6) Switch Memory	OFF	ON	ON	ON	OFF	ON
*four (4) Switch Memory	OFF	OFF	ON	ON	-	-

*(obsolescent)

NOTE: OFF = down, ON = up. See markings on side panel.

1.3.2 OPERATION

NOTE 1: *Nomenclature:* A standard alphanumeric key is represented by a number or capital letter. A special key has a ( ) around it. Example: CR would be the C key followed by an R key, while (CR) would stand for the Carriage Return key labeled "CR" on the keyboard.

CHART
1.3.1

CHECKOUT PARAMETERS

NUMBER OF MEM BOARDS	COMPOSED OF MEM 32	COMPOSED OF MEM 128	NUMBER OF ARRAYS	ARRAY I WIDTH	ARRAY I DEPTH, d	ARRAY 2 WIDTH	ARRAY 2 DEPTH, d
1	1	0	1	32 Bits	1 k words	X	X
1	0	1	1	32	4	X	X
2	2	0	1	64	1	X	X
2	0	2	1	64	4	X	X
2	1	1	2	32	1	32 Bits	4 k word
3	3	0	1	96	1	X	X
3	0	3	1	96	4	X	X
3	2	1	2	64	1	32	4
3	1	2	2	32	1	64	4
4	4	0	1	64	2	X	X
4	0	4	1	64	8	X	X
4	3	1	2	96	1	32	4
4	2	2	2	64	1	64	4
4	1	3	2	32	1	96	4
5	5	0	2	96	1	64	1
5	0	5	2	96	4	64	4
5	4	1	2	64	2	32	4
5	3	2	2	96	1	64	4
5	2	3	2	64	1	96	4
5	1	4	2	32	1	64	8
6	6	0	1	96	2	X	X
6	0	6	1	96	8	X	X
6	5	1	2	32	5	32	4
6	4	2	2	64	2	64	4
6	3	3	2	96	1	96	4
6	2	4	2	64	1	64	8
6	1	5	2	32	5	32	20

NOTE 2: *Underlined Characters:* If an input has one or more underlined characters, those alone are sufficient. Example: HEX (CR) indicates that H carriage return is sufficient for the input.

NOTE 3: *Examples:* The example shown below is for an instrument with either two MEM32 Writable Control Stores or three MEM128 WCS. Use chart 1.3.1 to enter the proper information for NUMBER OF ARRAYS, WIDTH, AND DEPTH. A superscript *"1"* stands for 64 bit organization. A superscript "2" stands for 96 bit organization.

NOTE: Board Locations: In all cases, insert all the MEM-32 boards if any below the MEM-128 boards if any. The two families cannot be mixed in one array. The STEP firmware prefers MEM-32s to dedicate to array 1.

The following is a step-by-step checkout procedure which, when completed successfully, verifies all machine functions.

We recommend that this checkout be performed when the instrument is first received. This will familiarize the user with its operation as well as check the functions prior to one-line use.

Rapid verification of instrument function in an on-line environment can be achieved using the TEST command. Expanded memory check ability is possible with the optional speed test hardware. The test command is explained in section 2.2.4.

#	COMMENTS	DISPLAY	OPERATION
	(Optionally, test routines can be run at the power-up time. These are STEP-3's built-in self-test routines. See section 2.2 for description.)		Turn on STEP Instrument Make sure Write Protect Switch is in the Write Position (lamp off).
1.3.2.1	SETUP COMMAND		
	STEP-N has the capability of simulating 2 independent memory arrays. This enables the instrument to be used simultaneously for: two projects; a dual processor project; microcode and macrocode; microcode and mapping ROMs. The following tests are nominal case per chart One array is used unless two are required for checkout, e.g. unless both MEM-32 and MEM-128 are used.	NUMBER ARRAYS =	1 (CR)
⊢	Data may be displayed in either Hexadecimal or Octal. Demo routines are in HEX.	DATA =	HEX (CR)
∞	STEP-N can configure memory to start at any arbitrary address from 0 to 7FFF (Hex).	STARTING ADDR =	0 (CR)
	The word width can be from 8 to 96 bits in each array and may be different for each array. See note 3.	WIDTH =	64 (CR)[1] 96 (CR)[2]
	Depth is given in increments of 1024 words: 1 is 1k, 2 is 2k etc... Designers utilizing memory depths of less than 1k can use the extra memory to aid code debug. Minimum depth is "1"	DEPTH =	1 (CR)[1] 4 (CR)[2]
	If the physical memory configuration does not match the values entered during SETUP, an error will be flagged and parameters must be re-entered.	CMND (indicates Step-N is ready for any command)	
1.3.2.2	ERROR CORRECTION		
	Step operation is failsafe. If an error is made during operation, it will show on the CRT and all the user does is to enter the correct value. Use (DEL) key to correct misspellings, etc...		
	Note the top line of the display. It always shows configuration, current command and array.		

#	COMMENTS	DISPLAY	OPERATION
1.3.2.3	**EDITOR** The following sequence demonstrates the use of STEP-N's editor.	ENTER COMMAND	
1.3.2.3.1	**ENTER COMMAND** Start with the main editing command, ENTER. Note that memory has random data-memory contents not altered during STEP-N operation even when "Reset" key is pressed. The contents of memory is altered only through user command. Locations 0,1,2 and 3 are displayed.	(Random WCS contents of address locations 0 thru 3).	ENTER (CR)
	Pick a convenient memory address. Four memory lines are displayed starting with the current address (in this case 1FE). Use the cursor Up/Down keys to increment, decrement, or scroll through memory.	ADDRESS =	ADDR (CR) 1FE (CR) Cursor ↓ ↑ keys to address IFO
	To modify the contents of memory, push the "ENTER" key. This moves cursor to data field. Enter some data in memory. Use cursor left and right keys to position cursor within the data. Note the binary representation of the first five digits beginning with the cursor (always 5 digits or less regardless of word width). Note binary duplicates the Hex.		(ENTER) key 0123 4567 89AB CDEF[1,2] FEDC BA98[2] 1111 1111 1111 1111[1,2] 1111 1111[2] 2222 2222 2222 2222[1,2] 2222 2222[2] 3333 3333 3333 3333[1,2] 3333 3333[2] All lines are followed by (CR).
	The line above the data contains the following information: The current address at cursor location, the current bit position of the most significant bit at the cursor location starting with bit "0" as LSB on the right, and the binary expansion field, which scrolls through the word, under cursor control.	AAA PP BBBB BBBB | | └BINARY | BIT POSITION ADDRESS	
	When entering data, note the auto scroll feature. However wide the microcode word, one line is one word. The data has a one line buffer and is not entered into memory until (CR) key is pressed. Use the (DEL) and (CLEAR) keys to restore mistakes, a character or line at a time, respectively. Use the Cancel and Home* (C & H) key to leave the data field. Quit the ENTER mode and go to top command level by typing Q (CR). *Or (HOME) on STEP-3.	0123 4567 89AB... FFFF FFF7 89AB... FFFF FF67 89AB... FFFF F567 89AB 0123 4567 89AB (cursor to line 3) ENTER COMMAND	At the address containing: 0 1 2 3...enter "F F F F F F F..." Do not hit (CR) Press (DEL) key Press (DEL) key Press (CLEAR) key Press (C & H) key QUIT (CR)

1.3.2.3.2

MOVE COMMAND

The following sequence demonstrates the use of the Move command, the second of the four editing commands. Move is non-destructive, like a "copy".

The Move command is used to 1) Save a subroutine in an unused portion of memory prior to temporary modification. 2) To insert new lines of code into a subroutine by moving a block of data up or down several lines to free space for new code. Since this wipes out existing code, and could change reference locations, care should be taken when using this command. NOPs should be placed within the code and between subroutines during debug to allow room for new code.

The following routine moves the previously entered code which starts at Source Address 1FO (see 1.3.2.1.3) to destination Address 1. The NUMBER of LOCATIONS specifies in decimal the length of the block to be moved. By using the Enter command the results of the move can be accessed at both address 0 and address 1FO. Notice that the STEP-N command is like a "copy" instruction, in that the source remains unchanged.

DISPLAY	OPERATION
ENTER COMMAND	
	MOVE (CR)
SOURCE ADDRESS =	
	1FO (CR) (assumed address containing 0123...)
DESTINATION ADDRESS =	
	1 (CR)
NUMBER LOCATIONS =	
	3 (CR)
CMND	
	ENTER (CR)
0000	
XXXX XXXX XXXX...	
0123 4567 89AB...	
1111 1111 1111...	
2222 2222 2222...	
	QUIT (CR)

Address of display window
Contents of location 0000
Contents of location 0001
Contents of location 0002
Contents of location 0003

1.3.2.3.3

SEARCH COMMAND

CMND

The following sequence demonstrates the use of the Search command, the third of the four editing commands. The Fill command, the last editing command, is demonstrated when checking memory contents.

#	COMMANDS	DISPLAY	OPERATION
1.3.2.3.3	SEARCH COMMAND (CONT)	CMND	
	The Search command is used to find all instructions with certain fixed fields. A memory block, field contents, and don't care bits may be specified. In this example all locations between START ADDRESS = 0 and END ADDRESS = 300 Hex will be examined. The memory block will be searched for a data word of 012XX... Every time the "CR" key is pressed, the search will continue from the last word found. To abort Search, use the (C & H), Cancel and Home key. (X or don't care calls for 0 in the mask)	ENTER COMMAND START ADDRESS = END ADDRESS = DATA = DON'T CARE = MATCH AT ADDR = NO MATCH FOUND CMND	SEARCH 0 (CR) 300 (CR) 0123 4567 0000...(argument) FFF0 0000 0000...(mask) (CR) (CR) ... (CR) (To create a SEARCH example with more "HITS" or matches, use fewer 1's (fewer F's) in the mask.)
1.3.2.4	USING THE RS232 LINK SETUP		
	The following sequence demonstrates the ease of establishing communication between STEP-N and an external device such as a Prom Programmer or Computer.		
1.3.2.4.1	DUMP		
	DUMP instructs STEP-N that memory contents will be transferred from STEP-N WCS to an external device. The format picked is STEP's Microword™ format. Other formats include ASCII HEX SPACE, BPNF, and GENPROM.™ For a complete list of formats see Section 2.5.	ENTER COMMAND FORMAT = START ADDR =	DUMP (CR) 0 (CR) 0 (CR) (hex - like all data and addresses)
	The START ADDRESS, in this case hex 1A, and the number of locations, in this example decimal 23, are required for Dump, Load, Compare. In addition the "logical device" (DEVICE) must be specified. There are 3 serial ports with 6 logical devices. The device specified in this example is the 3 wire RS232 port (transmit, receive, ground) with local echo. Due to the device picked, no control handshake is present and the checkout can continue without anything connected to the port.	NUMBR LOCATIONS = DEVICE = DUMP ENTER COMMAND	27(CR) (decimal - like all STEP quantities) 5(CR) (STEP has stopped prompting you, so it could go ahead with dump. But what about baud rate? STEP has stored defaults which we'll examine next.)

#	COMMANDS	DISPLAY	OPERATION
1.3.2.4.2	PORT PARAMETERS		
	After the DUMP has been setup, it is necessary to specify the port parameters. This need only be done after Power On or Reset or Setup.		
	First determine the current status using the examine "X" command. To change any parameter, enter the proper name as shown with the BAUD example given. Parity, Stop Bits, and GENPROM control characters can also be changed, until all is correct for the DUMP.	ENTER COMMAND (Parameter Display) ENTER COMMAND BAUD =	XPARAM (CR) BAUD (CR)* 2400 (CR)
1.3.2.4.3	COMMUNICATION WITH EXTERNAL DEVICE		
	Once communication with the external device is ready to proceed, it is necessary to talk to external computer/Prom Programmer/whatever, to set it up. This is done by entering TEXT. STEP-N becomes a limited terminal in this mode. Anything which is typed, is sent over the port, one character at a time.	ENTER COMMAND TEXT Message Being Typed	TEXT (CR) User "talks" (types) to the distant device in any required way, e.g. in talking to the host computer, he talks like a terminal. Teletype-based keyboard handles virtually all cases.
1.3.2.4.4	STARTING DATA TRANSFER		
	To start the data transfer once the external device is ready, press the (C & H) key. This should be done before the final command or carriage return (CR) for the final command is issued to the external device. Enter the final command, (CR). Because no echo is present in this case, press the "C" key for continue. Data transfer between STEP-2 and the external device is automatically synchronized without further user intervention. Note: sometimes an error message will appear on the screen due to UART Setup. Press (CR) key and repeat steps 1.3.2.4.1 through 1.3.2.4.4.	I/O IN PROGRESS	(C & H) (CR) (C)
	*STEP-2's default baud rate is 110 baud. STEP-3's default baud rate is 1200 baud.		

#	COMMANDS	DISPLAY	OPERATION
1.3.2.5	RUNNING A PROCESSOR		
1.3.2.5.1	MONITOR	CMND	
	The following sequence demonstrates how Step-N interfaces with a processor and displays processor state. The target processor can access STEP-N WCS memory when and only when STEP-N is in the MONITOR command.	ENTER COMMAND	MONITOR (CR) (IMPORTANT WARNING -- To prevent DAMAGE to address circuits of STEP.)
	WARNING- ONLY USE MONITOR COMMAND WHEN: a) totally disconnected from the target processor, b) WHEN TARGET PROCESSOR POWER IS ON.		
	When in MON HLT the clock control outputs are in the HALT mode. To start operation hit RU(CR).	MON HLT	RUN (CR)
1.3.2.5.2	RUNNING		
	When properly interconnected to the target processor in RUNNING, an address readout is captured every half second and displayed. ADDRESS = NONE indicates improper (or no) connection to the target processor. Also in RUNNING, the status of the breakpoints is continuously displayed: Reverse video, breakpoint was hit; flashing reverse video, breakpoint is continuously being hit; no reverse video, the breakpoint was not reached. To exit from RUNNING press "H" or "Q" key. Do not use (CR).	RUNNING ADDRESS = NONE BR1 = NONE BR2 = NONE BR3 = NONE	(Target clock starts, if STEP has been tied to control it. See sections 1.4.3 and 3.5.) Q (Target clock stays running because you QUIT; HALT would stop the target clock.)
1.3.2.5.3	MON RUN	(cursor appears, line 3.)	
	In MON RUN, breakpoints can be set and cleared, Traces setup and viewed and single step / single cycle initiated. Processor operation is unaffected by MON RUN but breakpoint status and address readout is not reported on the CRT.	MON RUN	
1.3.2.5.4	BREAKPOINTS		
	To set a breakpoint, first pick the breakpoint desired. There is one breakpoint per memory board. Each array has its own breakpoints numbered from 1 to 6. Once the breakpoint has been selected, enter the desired address. The address range for a given breakpoint is shown and	BR= RANGE=0-3FF ADDRESS = BR1=2FF	BREAK (CR) 1 (CR) 2FF (CR)

#	COMMANDS	DISPLAY	OPERATION
1.3.2.5.4	BREAKPOINTS (CONT)		
	changes with instrument configuration. In this case address 2FF hex is shown. A breakpoint only halts the target processor if the breakpoint BNC output is connected to the XHLT BNC input. Once entered, the new breakpoint value is immediately active.	BR1 = 2FF	
1.3.2.5.5	COMMAND LEVEL		
	Monitor can be exited from MON HLT or MON RUN.		QUIT (CR)
1.3.3	MEMORY CHECKOUT		
	The following routine checks that each bit in the Writable Control Store can be set and reset, and verifies address independence. It should be done when a memory malfunction is suspected or upon initial instrument receipt.	CMND ENTER COMMAND	
1.3.3.1	FILLING MEMORY		
	Fill memory to maximum depth as shown in chart 1.3.1 with all "5"s. Repeat operation by filling with all "A"s. This inverts every bit in memory. NOTE: The FILL command may take up to ten seconds to complete, depending on organization.	ENTER COMMAND START ADDRESS = END ADDRESS = DATA = ENTER COMMAND START ADDRESS END ADDRESS DATA =	FILL (CR) 0 (CR) d (CR) (d from chart 1.3.1) 555... (CR) F (CR) 0 (CR) d (CR) AAA...(CR)
1.3.3.2	SCANNING MEMORY	ENTER COMMAND	
	Visually scan the entire memory for "A"s using the cursor up key in ENTER. If an address does not have all "A"s a memory chip is probably bad: Refer to section 4.	ENTER 0000 AAAA AAAA AAA... (Scan all.)	ENTER (CR)

#	COMMANDS	DISPLAY	OPERATION
1.3.3.3	**CHECKING ADDRESS** To check the invert data pattern fill memory with all "5"s. At the address shown, load the corresponding data after first checking for "5"s. Address Data 0000 000... 0001 111... 0002 222... 0004 333... 0008 444... 0010 666... 0020 777... 0040 888... 0080 999... 0100 AAA... 0200 BBB... 0400 CCC... 0800 DDD... 1000 EEE... 2000 FFF... Last address 0123... NOTE: Depending on Step-2 configuration not all addresses shown may be present. From last address scan backwards, using the cursor down key to check that "5"s or proper data is present at each address.	ENTER COMMAND START ADDRESS = END ADDRESS = DATA = ENTER COMMAND 0000 0000 0000 0000... 1111 1111 1111... 2222 2222 2222... 5555 5555 5555... (Scan all.)	QUIT (CR) FILL (CR) 0 (CR) d (CR) 555... (CR) ENTER (CR)
1.3.3.4	**SECOND ARRAY** If two arrays are called out in chart 1.3.1 repeat sections 1.3.3 for the second array. To get second array use the ARRAY command. The preceeding section demonstrated Step-2 operation and checked basic operation. The instrument was throughly checked prior to shipment. If a malfunction is suspected, or for a more complete check, consult the trouble shooting guides in section IV and execute the memory test programs.	ENTER COMMAND ARRAY =	QUIT (CR) ARRAY (CR) 2 (CR)

1.4 QUICK INTERCONNECT TO TARGET

This section presents in brief, the necessary actions to:

Connect STEP into the Target Processor memory
Connect STEP to the Target Processor clock
Setup Trace
Connect STEP to the Host computer

It is meant both as a first-pass example of how to interconnect STEP, and also as a means to enable rapid setup of the instrument. This section does not cover the interconnections necessary for controlling the Target Processor clock (which provides single step and halt on breakpoint functions), nor the breakpoint options, the direct memory interconnect without ROM Simulation, etc. These are fully explained in section III.

1.4.1 MEMORY INTERCONNECT

The following memory interconnect information covers memory organization, and ROM Simulation. Additional information can be found in Section 3.1.

1.4.1.1 MEMORY ORGANIZATION

Determine proper memory organization for the target processor and configure switches on side of memory board accordingly (NOTE: 2 or more memory boards may be necessary to obtain full memory width/depth):

MEM ORG	MEM-32 (4-Switch)*		MEM-32 A,F (6-Switch)*		MEM-128
D x 32	S3↑	S4↑	S2↑	S3↑	S3↑
2D x 16	S3↑	S4↓	S2↑	S3↓	S3↓
4D x 8	S3↓	S4↑	S2↓	S3↑	--

D = Depth of memory board: 1k for MEM 32, 4k for MEM 128
*Memory boards with 4 DIP switches are older models; 6-switch are newer.

1.4.1.2 STANDARD MEMORY SWITCH SETTINGS

MEM-32 (4-Switch)	S1↓, S2↓
MEM-32 A,F (6-Switch)	S1↓, S4↑, S5↑, S6↑
MEM-128 A, B, F	S1↓, S2↓, S4↑, S5↑, S6↑,

1.4.1.3 MEMORY PLUG-IN

The Step instrument is very versatile and the Writable Control Store memories can be organized in many different ways. For a full discussion of organization refer to section 3.1 and Appendix B. The following is a brief set of rules with examples to guide in memory hookup. Figure 1.4.1.3, WCS Board Edge, shows an outline of the various connection points. Probing the board edge is easy, without removing cards or cables.

TOP VIEW: COMPONENT SIDE UP

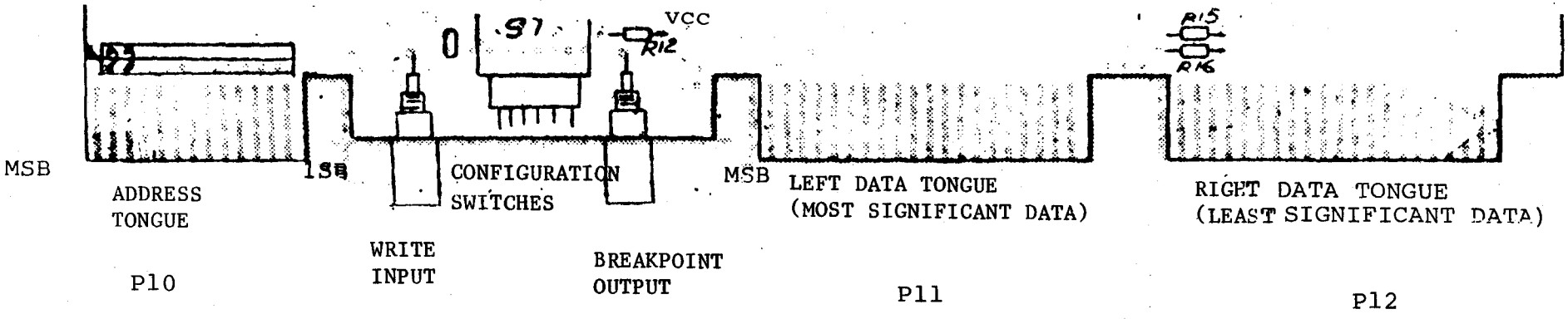


FIGURE 1.4.1.3 WCS BOARD EDGE

NOTE: The usage MEM-1, MEM-2, MEM-3, etc. tells the location (slot in the card cage) of a board. The usage MEM-32 and MEM-128F tells the size (bit storage capacity) and (when a letter follows) the speed of the WCS board. STEP-N's side panel lettering shows the slot numbers MEM-1, MEM-2, etc.

RULE 1: ADDRESS INPUT

Hookup the 26 conductor address cable to all address tongues on the WCS boards being used, and Trace address tongue (if present). Unused WCS boards are the ones uppermost in the card cage. Example: If a system has 3 MEM-32 and is organized 1k x 64, MEM-1 and MEM-2 (slots 2 and 3) will be used and MEM-3 (slot 4) will be unassigned (available to array 2 if desired). STEP firmware assigns WCS during setup mode.

RULE 2: WCS BOARD DATA OUTPUT

The right data tongue (see figure 1.4.1.3) always contains either the least significant data (horizontal organizations) or the least significant address data (vertical). The 16 bits per tongue can be wire-ORed in the cabling system, to agree with the switches. Examples:

Switched WCS width	Left Data Tongue	Right Data Tongue
8 Bits (MEM-32 only)	Bits 0-7, 2-4k	Bits 0-7, 0-2k
16 Bits	Bits 8-15, 0-2dk	Bits 0-7, 0-2dk
32 Bits	Bits 16-31, 0-dk	Bits 0-15, 0-dk

d = WCS depth: 1 for MEM-32, 4 for MEM-128

RULE 3: MEMORY ARRAY DATA OUTPUT

The lowest WCS board, MEM-1, always contains the least significant data, horizontal organizations, or the least significant addresses, vertical organizations. The highest assigned WCS always has the most significant data and/or most significant address. Examples:

WCS Width	Organization*	MEM 1	MEM 2	MEM 3
32	1k x 64	0-1k, Bits 0-31	0-1k, Bits 32-63	Unassigned
32	2k x 32	0-1k, Bits 0-31	1-2k, Bits 0-31	Unassigned
16	2k x 32	0-2k, Bits 0-15	0-2k, Bits 16-31	Unassigned
16	2k x 48	0-2k, Bits 0-15	0-2k, Bits 16-31	0-2k, Bits 32-47
32	2k x 48	NOT POSSIBLE	---	--

*"Organization" refers to array size keyed in, in Setup Mode

RULE 4: MIXING MEM-32 & MEM-128

MEM-32 and MEM-128 can both be in the same system when assigned to two different memory arrays.

RULE 5: ARRAY ASSIGNMENT IN DUAL-ARRAY SYSTEM

Array 1 is assigned the lowest WCS boards, Array 2 the remainder. Exception - When MEM-32 and MEM-128 are both present, MEM-32 WCS are always assigned to Array 1. To avoid confusion always place MEM-32 in the lowest card slots.

RULE 6: WCS PLACEMENT IN TWO-ARRAY SYSTEMS

An array must be composed of a sequence of the same type WCS. That is, MEM-32 and MEM-128 cannot be mixed in the same array. All MEM-32s must be grouped together and all MEM-128s must be grouped together. In most cases there can be a gap between the WCS boards within an array.

Example:

Array 1 2k x 64 using MEM-32 (4 WCS boards)
Array 2 8k x 16 using MEM-128 (1 WCS board)

In this example Array 1 could occupy slots 2, 3, and 4 (MEM-1, MEM-2, MEM-3) in Step-2 and slot 1 in the Expansion Chassis. Array 2 could occupy slot 2 in the Expansion Chassis, or slot 3 or slot 4, etc.

1.4.1.4 ROM SIMULATION INTERCONNECT

The following is a brief set of rules covering ROM interconnect. For a fuller description see section 3.2.

NOTE: The usage "ROM Simulation" refers to the whole cable system between STEP-N and the target system. "Modules" are the orange boxes. (For field upgrade, the IC's inside are in sockets, the cables have quick-disconnect attachments to the circuit board, and key connections are wire-wrap on the circuit board inside the orange box.) "Data cables" are the translucent flex cables with DIP plugs. Use care in handling these--do not flex repeatedly.

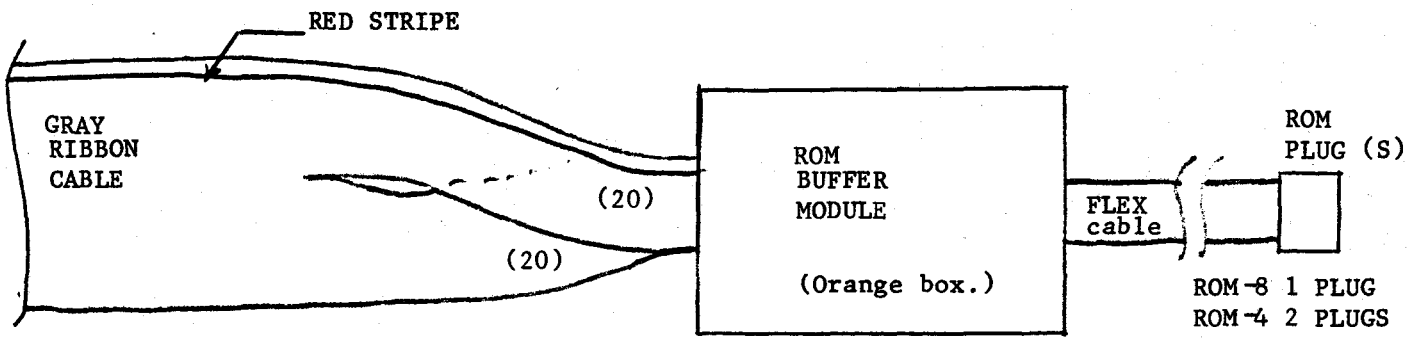


FIGURE 1.4.1.4a MULTIPLEXING ROM MODULE

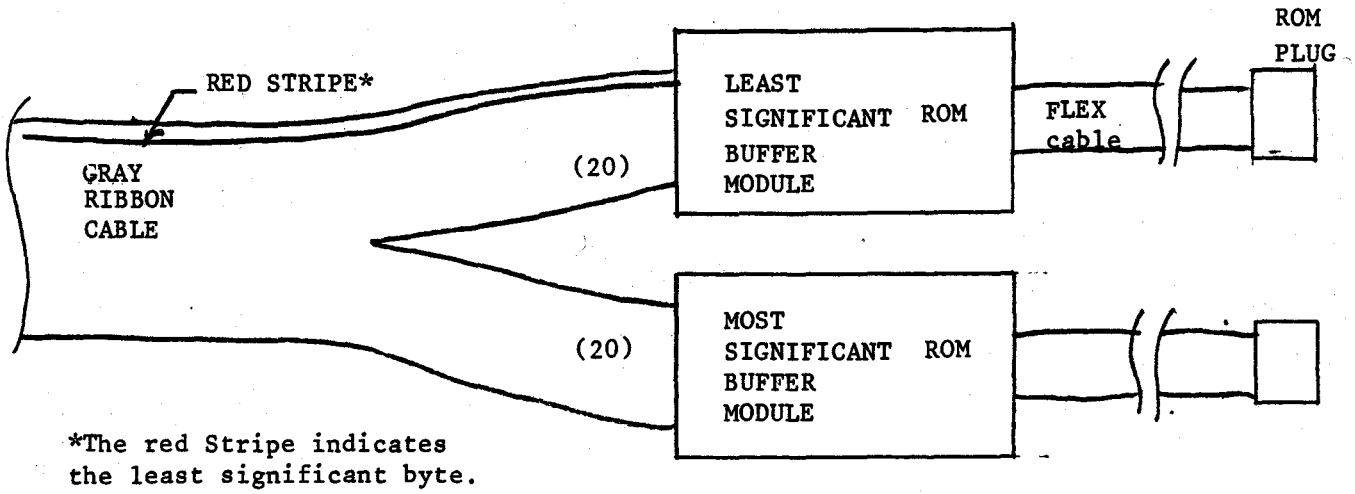


FIGURE 1.4.1.4b STANDARD (NON-MULTIPLEXING) ROM MODULE

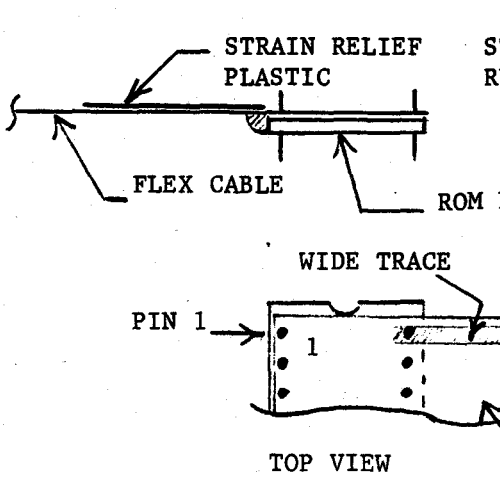


FIGURE 1.4.1.4c
OLD ROM PLUG

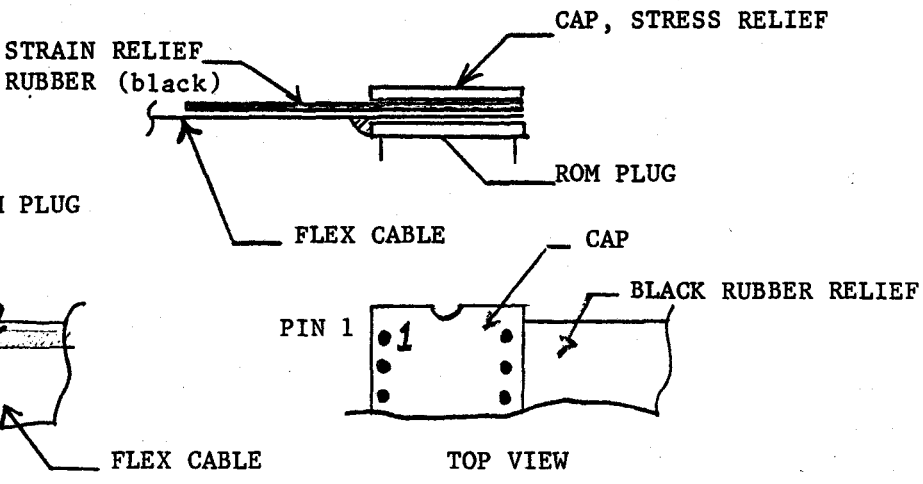
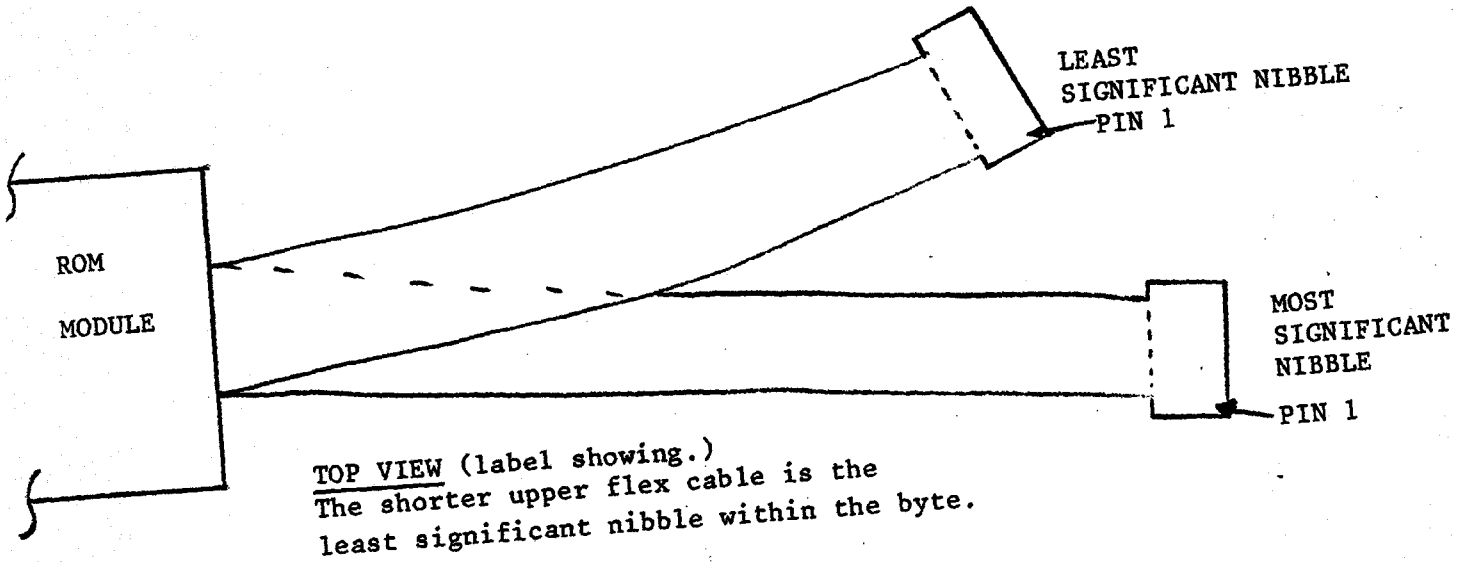


FIGURE 1.4.1.4d
NEW ROM PLUG



TOP VIEW (label showing.)
The shorter upper flex cable is the
least significant nibble within the byte.

FIGURE 1.4.1.4e ROM-4 PINOUT

RULE 1: MASTER ROM MODULE

Find the master ROM Simulation module, this will be the first used. The ROM Simulation module with the 26 conductor address cable is the "Master". All others are "Slaves" and have no address inputs.

NOTE: The Master gray cable should have a red stripe. If not, consult Section 3.2.

RULE 2: STANDARD VS MULTIPLEXING ROM SIMULATION MODULES

First, by inspection, determine whether you are using standard or multiplexing ROM modules. Multiplexing ROM Simulation modules have two (2) twenty conductor gray cables, standard have one as illustrated in figure's 1.4.1.4 a,b.

RULE 3a: STANDARD ROM MODULE INTERCONNECT

Standard ROM modules come in pairs. The module with the red stripe on the gray cable (figure 1.4.1.4b) is the least significant. Starting with the Master module in the least significant PROM socket, insert each ROM plug in turn according to the organization determined in the previous section, 1.4.1.3. Figures 1.4.1.4c, d indicate which pin is pin 1.

NOTE 1: If the Master ROM module does not have a red stripe on its gray data cable consult Section 3.2.

NOTE 2: For ROM 4 modules, the shorter, upper flex cable is the least significant nibble as shown in figure 1.4.1.4e.

RULE 3b: MULTIPLEXING ROM MODULE INTERCONNECT

Starting with the Master ROM module in the least significant PROM socket, insert each ROM plug in turn according to the orginization determined in the previous section, 1.4.1.3.

NOTE 1: If the ROM module is connected to both halves of a single gray cable as in figure 1.4.1.4a, the WCS must be organized 8 or 16 bits wide. If the ROM module is connected to two halves of two different gray cables, the WCS must be organized 32 bits wide. To reconfigure the modules see section 3.2.

RULE 4: ADDRESS READOUT

An ADDRESS = NONE readout generally indicates improper ROM connection. A proper address readout is only obtained if the full data width as determined by WCS memory switch connection is utilized on the least significant WCS. Example: If the WCS is organized 32 bits wide, all 32 bits of ROM must be inserted.

If the left data tongue will not be used*, the enable-logic loop must be completed anyway, to get rid of the "ADDRESS = NONE" message and permit normal address reporting on the CRT. This completion can be accomplished using a shorting plug (RSCP = ROM Simulation Completion Plug, furnished with STEP-N) that ties pin 17 to 19 and pin 37 to 39 on the unused tongue. Or, a ROM Simulation cable can be plugged onto the "unused" tongue. It will complete the enables, if its DIP plugs see Vcc, GND, and valid chip select (if such a pin is on the DIP).

*As, for example, when a MEM-32 is used to simulate 1k x 16 and the WCS capacity is only half used.

1.4.2 TRACE QUICK SETUP

For additional information on connecting Trace into a target processor refer to section 3.6. Information on using the Trace option is given in section 2.4.5. Here are the basics:

1.4.2.1 HOOK UP ADDRESS PROBE AS FOLLOWS:

1.1 Connect ground probe to circuit ground at target processor

1.2 Ground all unused address inputs

1.3 Connect Vcc probe to 5±0.25 volts

1.4 Connect UAC, User Address Clock, to appropriate clock

1.5 Ground EE, External Enable

1.6 Connect TQ1 and TQ2, qualifier inputs as appropriate

1.4.2.2 HOOK UP DATA PROBE (S) AS FOLLOWS (OPTIONAL):

NOTE: Data probes need not be connected for proper operation.

2.1 Connect ground probe to circuit ground (each probe)

2.2 Connect Vcc probe to five volts (each probe)

2.3 Connect UDC, User Data Clock, to appropriate (clock) signal

2.4 Connect D0-D15 as appropriate

1.4.2.3 SET UP CONFIGURATION SWITCHES TO MATCH PROCESSOR

NOTE: Refer to figure 2.3 Switch Options, or to STEP-N side panel lettering.

3.1 Select proper edge on clock configuration switches S1, S2, S3

3.2 Select proper polarity on qualifier configuration switches S4, S5

3.3 Set S6, EE polarity, OFF (DOWN) (NEGATIVE ENABLE)

3.4 Select proper clock source for TQ1 and TQ2 switches S12, S34 (optional)

1.4.3 TARGET PROCESSOR CLOCK INTERCONNECT

In general there are three ways to interface the control lines to the target processor's clock: Use the RUN/HALT output to asynchronously gate the clock on the target system breadboard; Run the clock through the STEP clock control logic and use the resulting clock output to drive the target system; Run the clock input to the clock control circuitry and use the resulting output to synchronously gate the clock on the target processor. Implementation of these three methods will be explained in detail below. Refer to drawing 0001053 sheet 1 for additional information.

1.4.3.1 PULSE (RESET)

The Pulse "P"-key lines are pins 1 and 3 on P53.* Pin 1 gives the negative-true signal and Pin 3 the positive-true signal. The pulse lasts approximately 200 ms. The pulse output can either be tied to the RESET input on the processor (if one exists) to RESET the system from the keyboard or used as an external input or interrupt for testing purposes.

1.4.3.2 RUN/HALT

Pins 5 & 7 labled CLKC (for clock control) and $\overline{\text{CLKC}}$ are the Run/Halt lines. CLKC is positive true whenever the instrument is in RUNNING or MON RUN states. If XH (external halt) goes true, CLKC goes false while the XH signal is true.

The RUN/HALT lines are designed to asynchronously gate the clock logic of the target processor. When single stepping or cycling, a 50 nanosecond pulse is generated. This pulse can be widened by placing a capacitor between U11 pin 3 and GND. The capacitor value (MICROFARADS) is 0.005T where T is the desired pulse duration (ns) less 50 nanoseconds.

*P53 is a 20-pin connector at the bottom left corner, side panel.

1.4.3.3 XH (EXTERNAL HALT)

External halt has two inputs, a BNC input and an input on pin 15. These inputs are tied together and also tied to a 51-ohm resistor to ground. A positive true step forces the processor control outputs to a halt state.

1.4.3.4 CYCLE I (OPTIONAL -- SINGLE - CYCLE CLOCK BURST)

CYCLE I (Cycle Input) appears on pin 19 and is the input for the "C"-key (Cycle) command. This signal is generally used in systems where one complete processor cycle is composed of many clock cycles. A pulse (either positive or negative) would then indicate the beginning of the next processor cycle. If CYCLE I is used, J5 should be tied to J7 (via wirewrap)* for a negative true signal and J6 to J8 for a positive true signal. Where CYCLE I is not implemented J4 should be connected to J3 to prevent system hangup. The transition to true halts the clock.

1.4.3.5 CLKI, CLKO (CLOCK INPUT AND OUTPUT)

CLK I, Clock Input is a required input if the target processor's clock line is to be driven from STEP CLKO or gated synchronously by CLKO. When using CLKO (true output pin 11, complement pin 9) to directly drive system clock lines, J1 should be tied to J2. On the negative going clock edge, U1 is set enabling U2. The clock input is then available as an output starting with the next positive going clock pulse. To use CLKO to synchronously gate the target processor clock tie CLKI (Pin 17) high and tie either J5 or J6 to J3 (depending on clock state). See schematic, clock and I/O board, drawing 0001053.

*These wire-wraps posts are beside P53, lower left corner, side panel.

1.4.4 COMPUTER INTERCONNECT (DOWNLOAD)

1.4.4.1 DETERMINE COMPUTER REQUIREMENTS

The following information is required:

Type of hookup: 20ma, RS232 with control line information, 3 wire RS232. (Only one STEP port can work at a time.)

Computer response to input: echo, no echo, by computer, to STEP.

Baud Rate: 110, 300, 600, 1200, 2400 (see section 2.3 for higher baud rate).

Number of Stop Bits: 1,2

Parity bit: 0,1, even, odd*

1.4.4.2 SETUP STEP INSTRUMENT

Use the Load command by typing "L" (CR)". ("(CR)" stands for the carraige return key.)

FORMAT = 0 (Step's microword format)

DEVICE = 0 thru 5 as follows:

0	20ma, with echo:	device 0, port 1
1	7-wire RS232, with echo:	device 1, port 1
2	3-wire RS232, with echo:	device 2, port 2
3	7-wire RS232, Data I/O	Model 7, port 1
4	20ma, no echo:	device 4, port 0
5	3 wire RS232, no echo:	device 5, port 2

START ADDRESS = 0

NUMBER OF LINES = 1 or more (in decimal)

Setup baud rate by typing "B (CR)", stop bits by typing "S (CR)", and parity by typing "P (CR)"*. Use the eXamine Parameters command to check setup by typing "XP (CR)". Once set, these parameters will not change unless reset by the operator or unless the SETUP command is utilized.

*Parity choices are 0,1,2,3, respectively for stuck-at-0, stuck-at-1, even, odd.

1.4.4.2 SETUP STEP INSTRUMENT (CONT)

Plug the serial computer interface to the proper port on the side of the Step instrument. For 20ma current loop interconnect consult section 3.4.

1.4.4.3 TALKING TO A COMPUTER, STARTING I/O LINK TRANSFER

Enter TEXT mode by typing "T (CR)". If the setup is correct, no error messages will appear. Your Step instrument now appears to be a computer terminal. Anything typed on the keyboard will be transmitted one character at a time to the computer. Anything received from the computer will appear on the CRT, wrapping around to next line if more than 32 character line.

To upload or download information enter the proper computer command without the final (CR), press the "C & H" or "HOME" key, then (CR). To exit TEXT without uploading or downloading information, hold down the SHIFT key and momentarily press the "V" key, on STEP-2 or SHIFT and 0 (zero on top key-row) on STEP-3.

1.5 STEP COMMAND SUMMARY CHART

This section presents an overview chart of the STEP-N command structure, preparatory to a full description in Section II.

Some users may wish to review figures 2.1A and 2.1B before perusing this summary chart. Most will find the chart self explanatory.

As evidenced in 1.3's checkout chart, most commands, subcommands, and parameter inputs (responses to the prompts) have no effect until (CR) or (SPACE) is pressed to enter them. This human-factors feature permits correction of wrong key-strokes by hitting (DEL) delete or (CLEAR) keys before (CR) or (SPACE). A few "key-hit commands" cause immediate action, to maximize speed of operation. These were chosen for minimum impact if hit by mistake.

Note the columns specifying which commands are in STEP-2 (the STEP model shipped during the period 12/77 thru 6/80), which are in STEP-3 (the successor model shipped in July 1980 and since), and which depend on hardware options. The usages STEP and STEP-N mean that the discussion pertains to <u>all</u> STEP machines, both STEP-2 and STEP-3.

COMMAND SUMMARY CHART

Once the instrument parameters have been specified through SETUP, the commands can be accessed in any order.

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS, (SUBCOMMANDS)*	DESCRIPTION
1.5.1.1 INSTRUMENT *Specifies array size, tests STEP instrument readiness, CPU function, WCS memory function, memory access time, and ROM simulation cables, including TOTAL access time as seen from target PROM socket.*	SETUP (or reset push-button)	X	X		NUMBER OF ARRAYS = 1,2 DATA FORMAT = HEX, OCTAL (for addr,data) STARTING ADDR = { FOR ARRAY WIDTH = { EACH ARRAY DEPTH = { ARRAY	Configures the instrument to match the requirements of the target processor. Checks for a memory array specification consistent with the number and organization of the Writable Control Stores.
	TEST		X	X	TEST FLAG = 3 thru 10 CARD TYPE = 0,1 (test 5 thru 10) SLOT NUMBER = 0 thru 7 (test 5 thru 10)* ACCESS TIME = 2-254 (test 7 thru thru 10) (Tests 7 thru 10 require a hardware option, the Speed-Test board, STEP-3S. Tests 3 thru 6, however, are available in all STEP-3's, with or without the STEP-3S.)	Tests instrument and memory operation. Test 4, SUMCHK, checks instrument CPU and EROM contents. Tests 5 and 6, GALPAT and QUICHK check slow speed RAM operation. Tests 7 thru 10 (USRPRT, ACCESS, FASTCK, and SHMOO) use the Self Test option to throughly check the Writable Control Stores at speed and determine access time.
	ARRAY	X	X		ARRAY = 1,2	Selects which memory array is to be accessed.

*Card slots in STEP-2 are numbered 0 (bottom) thru 5 (top).
Card slots in STEP-3 are numbered 0 (bottom) thru 7 (top).
In the STEP-2E expansion chassis, slot 8 (bottom) thru 13 (top).
In the STEP-3E expansion chassis, slot 8 (bottom) thru 13 (top).
Interconnection uses up slot 8 and the slot below it.

*TEST 3 uses a loop-back connector to verify serial I/O ports in all modes.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

COMMAND SUMMARY CHART

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS,(SUBCOMMANDS)*	DESCRIPTION
1.5.1.2						
EDITOR - *WCS Enables the user to examine or modify memory array contents through the keyboard*	ENTER	X	X		(ADDRESS) (cursor ↑↓ →←) (QUIT) (CLEAR) (DEL) separate function keys (C&H) (ENTER)	Enters, modifies or displays data words of up to 96 bits in octal or hex format. Cursor controls permit data to be entered at any position within the four displayed memory locations and allows the currently displayed address to be incremented/decrememted or scrolled. The address and bit position of the cursor is displayed along with a binary representation of the data.
	FILL	X	X		START ADDR = LAST ADDR = ENTER DATA (Binary display) Hex/octal display.	Fills a memory block with a specified word. When no word is specified, the default case is zeros. Binary is duplicate.
	MOVE	X	X		SOURCE ADDR = DESTINATION WORD COUNT =	Moves a block of code of at least one word from one memory location to another. The original data remains intact unless written over by the MOVE command.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

COMMAND SUMMARY CHART

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS,(SUBCOMMANDS)*	DESCRIPTION
1.5.1.2 EDITOR (continued)	SEARCH	X	X		START ADDR = END ADDR = SEARCH WORD = (Binary display dup.) (Hex/Octal search word display.) DON'T CARE WORD = (0 = don't care bits.) (1 = do care bits; must match the search word.)	Searches a block of code for a particular data pattern composed of ones, zeros, and don't cares. When a match is found, the address and memory word is displayed and the search is stopped until continued by the operator.
1.5.1.3 INPUT/OUTPUT *Permits communication over serial links with external devices such as computers, PROM programmers, etc.*	LOAD DUMP COMPARE PUNCH	X X X X	X X X		FORMAT = 0 thru 3 START ADDR = NO. LOCATIONS = DEVICE = 0 thru 5 WIDTH = { PROM at a time POSITION = { Formats only (BAUD RATE) 110 -- 2400 (PARITY) 0,1,2,3 (STOP BITS) 1,2 (HEADER, FRAME, END CHAR) (TEXT) (XPARM)	LOAD loads object memory in a MICROWORD™ (word at a time) format or one of several PROM formats. Device specifies serial link (20ma, RS232, or Modem input as well as line protocol.) DUMP dumps the contents of the specified memory array segment over the serial links in PROM or MICROWORD™ image. COMPARE compars the contents of memory to the information being received over the serial link. The address if any location whose contents do not match the incoming data is shown in an error message.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

COMMAND SUMMARY CHART

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS, (SUBCOMMANDS)*	DESCRIPTION
1.5.1.3						
INPUT/OUTPUT (cont)	TEXT	X	X			When in TEXT, the instrument acts like a limited terminal. TEXT enables easy interface to computers, printers, PROM programmers, etc.
1.5.1.4						
MONITOR *Real time simulation of processor memory and control/ display of processor activity*	MONITOR	X	X		(RUN)	Enables the Writable Control Stores, Displays breakpoint address, breakpoint and Trace Status. The subcommands RUN thru DISABLE permit full control of the target processor clock from the Step-3 front panel and current address/Trace data from the user's system.
		X	X		(HALT)	
		X	X		(STEP)	
			X		(N### STEP)	
		X	X		(CYCLE)	
			X		(M### CYCLE)	
			X		(DISABLE)	
		X	X		(PULSE)	
			X		(RALACE)	RA, RB are convenient editing commands which allow two words in memory to be temporarily replaced to help track down problems. The original memory contents are saved (and restored on command) in registers outside the WCS memory.
			X		(RBLACE)	
					REPLACE WORD =	
					REPLACE ADDR =	

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS, (SUBCOMMANDS)*	DESCRIPTION
1.5.1.4 MONITOR (continued)		X	X		(BREAK) BREAKPOINT NUMBER = 1 thru 6 BREAKPOINT ADDR =	Sets breakpoint address without disturbing target processor. Breakpoint and Trace outputs can be used to halt the target processor if desired.
			X		(FORCE) FORCE WORD = CLOCK TICKS = 1 thru 250	Forces an instruction out of the Writable Control Store for the Specified number of clock ticks.
			X		(JAM) ADDRESS = CLOCK TICKS = 1 thru 250	Jams the contents of Writable Control Store contained in the address specified for the desired number of clock ticks.
		X	X		(EXCHNG)	Displays status information for other array; alternates. See ARRAY, Setup.
		X	X	X	(TRACE) SOURCE 1 = 0 thru 12 TRIGGER EVENT NUMBER = 1 thru 255 SOURCE 2 = 0 thru 12 TRIGGER EVENT NUMBER = 1 thru 255 TRIGGER POSITION = 1 thru 250 ASSIGN TBR1 = 1 thru 6 ASSIGN TBR2 = 1 thru 6	Trace setup is accomplished through a series of self teaching menus and does not disturb target processor operation. The Trace results can be viewed on Step's CRT or downloaded to an external device using the dump command.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

COMMAND SUMMARY CHART

CLASS	COMMAND	STEP 2	STEP 3	OPTION	PROMPTS FOR PARAMETERS, (SUBCOMMANDS)*	DESCRIPTION
1.5.1.4 MONITOR (continued)		X	X	X	(XTRACE)	When examining the TRACE contents (separate memory from WCS) LXXX lets you jump to a distant line instead of scrolling; DUMP puts a chosen portion of Trace memory out on the last-used I/O port; and FORMAT lets you display the non-address portion in hex, octal or binary.
		X	X	X	(LINE ###)	
			X	X	(DUMP)	
		X	X	X	(FORMAT = 1,2,3)	
		X	X	X	(QUIT)	
			X	X	(XSTATE)	XSTATE™, examine state, allows the target processor's internal registers or I/O ports to be read.
			X	X	(XPORT)	XPORT, examine port, is the first of a pair of commands that take advantage of the STEP-3S Self-Test Board, if installed. It reads in 32 bits of data, displays on the CRT.
			X	X	(WPORT)	Second of the pair (see above) write port accepts 16 bits from the user keyboard and writes the out via the Self-Test board.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step" S is the command, single step is the function.

SECTION II

OPERATING COMMANDS

2.1 COMMAND DESCRIPTION

2.1.1 GENERAL

In general, the operation of the STEP-N commands and control functions can best be learned by actual use. By design, the commands are quick and easy to learn and use. The following summary will be most useful if the commands are entered and tried after each description is read. (See also the Command Summary Chart, section 1.5, and the example in section 1.3 of actual operation.)

Commands are entered and executed by (CR), carriage return, or (SP) space, which may be used interchangeably. In the ENTER mode, DATA is entered and displayed by (CR) only. If (DEL), delete one character, or (CLEAR) (delete whole entry) is used to correct an erroneous key-stroke in any Command or subcommand before (CR) or (SP), the mistake will have no impact.

Commands are of two types: top level commands and subcommands. Top level commands are function commands and consist of keyword entries followed by a (CR) or (SP). Some subcommands also are keyword commands, which are also followed by (CR) or (SP); other subcommands are (brown) function-key commands or (tan) key-hit commands. Execution of function-key commands and key-hit commands need no (CR) or (SP) but proceed immediately after the key is pressed.

After the command set is learned, commands may be shortened to the minimum number of characters to make up a unique input.

Study of figures 2.1 A and B on the following page will reveal the orderly hierarchical command structure.

2.1.2 STATUS

Current machine state and organization is always displayed on the top display line, Line 1. Display Line 2 is used for messages from the STEP instrument to the user, e.g. "Too many boards required" for a requested Array size, or "ILLEGAL CHARACTER" when STEP's firmware objects to a wrong key entry. On Line 3, the blinking cursor is always used as the prompt indicator, indicating the STEP instrument is waiting for the next command or subcommand entry.

2.1.3 PARAMETER ENTRY, OPTIONAL PARAMETERS, AND SUBCOMMANDS

In each command, required parameters are always prompted, thus STEP-N does not require memorization of required parameter lists. Optional parameters and commands are not prompted but may be entered using a keyword; such as: ADDRESS (CR) as a subcommand of the enter command, permitting the user to jump to another part of WCS memory.

2.1.4 ERRORS

Errors are reported on line 2 of the display. Fatal errors never cause the firmware to "hang", and are rare, but may require re-entry of an entire parameter set, as indicated with a new beginning prompt. Minor errors require only a corrected single entry. STEP firmware checks all commands for uniqueness. All parameters are checked for range and data type; i.e.: hex, octal, or decimal.

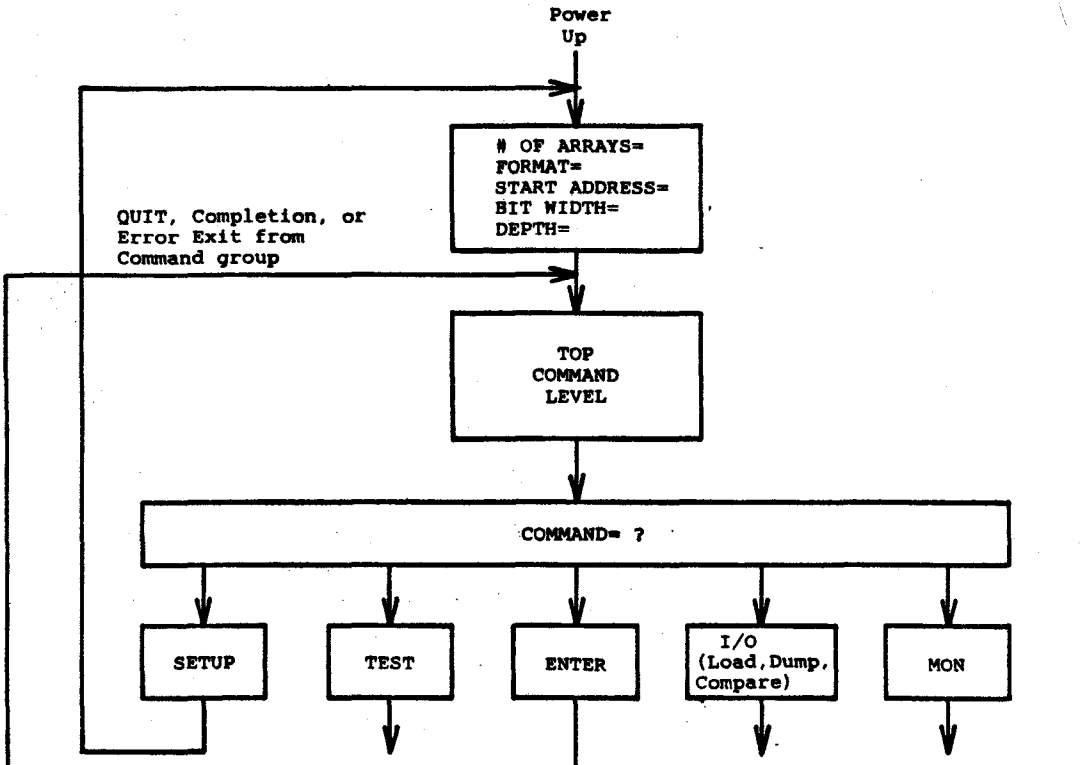


Fig. 2.1A, Top Control Path Leads to Five Command Groups

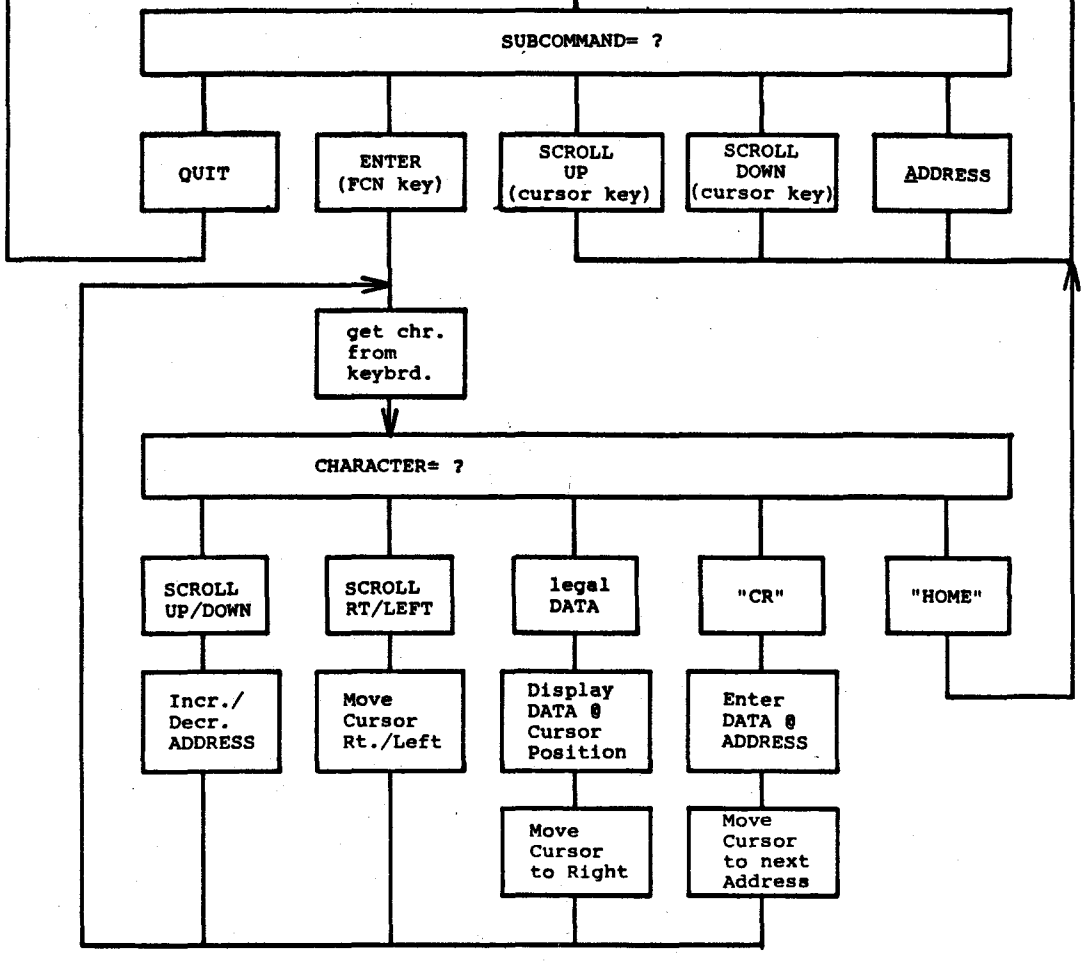


Fig. 2.1B, ENTER (EDIT) Command Structure Offers Four Sub-Commands

2.1.5 SETUP

At power on, the STEP instrument comes on in the SETUP mode as indicated on the top line of the display. The prompt NUMBER ARRAYS= is displayed, waiting for a parameter entry. After all parameters are entered in the SETUP mode, the STEP unit configures the hardware for the requested organization, assigns WCS memory hardware and address space, and checks that the organization is consistant with the available hardware. SETUP may be re-entered at any time from top command level, or by pushing the RESET push button above the keyboard.

2.1.6 TOP LEVEL COMMANDS

Top command level is always indicated by the message CMND on line 1 of the display. This means the STEP instrument is ready for any command.

Subcommand level is indicated by a specific subcommand's name displayed on line 1 of the display instead of CMND, for example, ENTER, MON HLT, or DUMP.

2.1.7 EXIT

Top level commands which have subcommands, require entry of the command QUIT (CR) to exit and return to the top command level.

2.2 INSTRUMENT COMMANDS

2.2.1 SUMMARY

SETUP

Key In:	SETUP (CR)
Enter From:	Top CMND level, STEP-N (and automatically when power comes on.)
Parameters:	Number arrays; 1 or 2 Data Format; Hex, Octal Start Address; 0000---7FFF H Word Width; 8--96 for HEX, 8-80 for OCTAL Depth; 1 → 48k/array, 2 parameters if two arrays specified.
Exit:	Following execution to top command level.

ARRAY

Key In:	ARRAY (CR)
Enter From:	Top CMND level, STEP-N
Parameters:	Array number; 1 or 2
Description:	Switches all machine functions to the specified array. The top line of the display indicates the current array.
Exit:	To top CMND level automatically, on completion.

TEST

Key In:	TEST (CR)
Enter From:	CMND
Prompts:	Menu of tests
Description:	Self-Test software permits user checking of STEP-3 operation. User selects appropriate tests from seven available. (See chart of tests, next page.)
Exit:	(Key-hit; no (CR) needed.) Takes you back to top CMND level, unless the test tells you to use 1 (one) for continue.

2.2.1 SUMMARY (CONTINUED)

CHART OF TESTS

AREA EXERCISED	TEST*	NAME	TEST TIME
Serial Port test	3	PORTCK	About 2 minutes
STEP CPU & System memory	4	SUMCHK	About 3 seconds
WCS Memory via Slow Port	5	GALPAT	20 + min, 1k; 4 hours, 4k board.
WCS Memory via Slow Port	6	QUICHK	About 1 minute (version of TEST 5)
WCS Memory via Fast Port	7	USRPRT	About 1 minute
WCS Memory via Fast Port	8	ACCESS	20 + min, 1k; 4 hours, 4k board.
WCS Memory via Fast Port	9	FASTCK	About 1 minute (version of TEST 8)
WCS Memory via Fast Port	10	SHMOO	About 1 minute

*TESTS 7-10 require hardware option STEP-3S, Speed-Test board and cables.

2.2.2 SETUP COMMAND

The SETUP command is a special command, in that it must be entered at least once when STEP power is turned on, to configure the STEP instrument for a particular test station setup. The Reset push-button above the STEP keyboard also activates the SETUP command, but does not reset or otherwise affect WCS data contents.

At power on, the instrument initializes to the SETUP command as indicated on the top line of the display, with the prompt NUMBER ARRAYS =, and waits for parameter entry.

The format of the SETUP command (used when power is already ON) is:

SETUP (CR)

2.2.2 SETUP COMMAND (CONTINUED)

where the following parameters are prompted:

1) NUMBER ARRAYS = (1 or 2)
2) DATA FORMAT = (Hex or Octal)
3) START ADDRESS = (0000----7FFF H)
4) WORD WIDTH = (8--96 for Hex)
   (8--80 for Octal)
5) DEPTH = (1--48) Array depth in k where k = 1024 locations
6) Repeat 2 thru 5 for Array 2 parameters (if two arrays are specified in parameter 1).

Notice that entry to the SETUP command can be executed in three ways. First, by powering the machine ON. Second, by depressing the Reset push button on the STEP front panel. Third, the SETUP command may be explicitly keyed in at any time the instrument is at top command level, as indicated by the message CMND on the top display line.

Following parameter entry, the SETUP command configures the available hardware for the requested array organization and checks that the array organization is consistent with available hardware. If the necessary hardware is not available, or is configured improperly for the specified organization, an error message indicating the nature of the problem is displayed for approximately 1 second, and the instrument automatically returns to the first parameter prompt in SETUP. If an error of this type occurs, the user should check the WCS memory configuration switches and make necessary changes in the hardware configuration to arrive at the required organization. If an error is again obtained, check sections 3.1.2.2 and refer to the charts at the end of 3.1.2.9.

2.2.3 ARRAY COMMAND

The format of the array command is:

ARRAY (CR)

One parameter is prompted by STEP-N to specify the desired array to be accessed, either array 1 or 2.

Execution proceeds following the (CR), switching all machine functions to the specified array. The top line of the display always indicates the currently active array.

2.2.4 TEST COMMAND

To view the menu of built-in test routines, enter:

TEST (CR)

Then, in response to the prompt:

TEST FLAG =

choose and enter a TEST NUMBER (3 thru 10) and (CR). Additional prompts follow, or the Test commences immediately, depending on which Test is chosen.

Tests for internal testing of STEP-3 are included in all STEP-3's. Test 0 thru 2 are reserved for factory use only. See list in section 2.2.1 above. Tests 3,4,5, and 6 are always included for memory and port testing, whether or not the hardware Speed-Test option STEP-3S is present. Test 7 thru 10 are included only with the Speed-Test board option STEP-3S.

2.2.4 TEST COMMAND (CONTINUED)

The Speed-Test board is a PC board and software option with 32 data input channels and 16 output channels with high speed time measurement circuitry to allow the system to test WCS control-stores at speed. The STEP-3S option includes cables to attach the Speed-Test board to the MEM board under test, including Data, Address, Write Control, and Breakpoint cables. This allows the user to make Access Time Measurement to 5 nanoseconds accuracy, and 2 nanoseconds resolution. The various test routines are described separately below.

The Speed-Test board provides distinct benefits to the user. It allows for "go / no go" checkout and maintenance on the instrument. Perhaps most important, it allows a real time instrument-quality measurement of memory integrity worst-case WCS access time, which may be performed as a periodic calibration. Short, calibrated-length cables are provided for easy user interconnect; their propagation delay is accounted for in TESTS 8 thru 10.

In conjunction with the PG board*, the user may wire-wrap particular ROM Simulation configuration sockets for ROM testing or whatever else he wants to make this type of speed measurement on. Again, measurement results are worst-case access-time, including cable, buffer, and WCS memory delays.

*Play Ground Board.

TEST 3 - PORTCK (Available on STEP-3 after November 1980)

Test 3 is a test of the 3 serial I/O ports and internal UART functions. Two shorting plugs are provided with each instrument which the user must install on the port during the test. Excution of the test transmits and receives the "QUICK BROWN FOX" algorythm. The received data is displayed on the CRT. The test is automatically repeated for each baud rate between 110 and 9600 baud. Errors are automatically detected and reported on the system CRT. Successful completion of tests on all 4 ports verifies proper functional operation of the system UART, all port select logic, and RS232 interface circuits.

TEST 4 - SUMCHK (Sum Check)

Test 4 is an internal test of the STEP-3 processor and program store. It displays the checksums of internal program store (System Memory) for each 1k up to a maximum of 30k. About 28k is now in use. Each machine as it is being produced has each of these checksums on file. They are typed on a label on the STEP-3 base. To verify correct CPU operation, the CRT totals are compared to this label.

TEST 5 thru 10 all test the WCS memory. Typical test results on the CRT are:

```
RAM TEST PASSED
    or, for one type of board failure,
LIKELY ADDRESS STUCK A0-A7
TO CONTINUE, Ø=NO 1=YES, ?
USER DATA ADDRESS 00AF
DATA READ=        FFFF   FF7F
    or, for a second failure type,
FAILED AT CODATA ADDRESS
TO CONTINUE, Ø=NO 1=YES   ?
USER DATA ADDRESS   030B
DATA READ         FFFF   FFFE
CODATA ADDRESS=   0000
CODATA            5555   5555
TEST ACCESS TIME = 030   (nanoseconds)
```

2.2.4 TEST COMMAND (CONTINUED)

In general, test results are in plain English, with much of the CRT screen devoted to specific data.

> *NOTE: If you've thoroughly checked your hookup, cables, IC's in sockets, Vcc=5.00 ± 0.20 volts, etc. and still get error indications, please phone STEP Engineering for immediate assistance.*

TEST 5 - GALPAT (GALLOPING PATTERN)

Test 5 is an internal test which runs a complete galpat on memory at non-real time speeds.

> *NOTE: For a MEM-32 this test takes approximately 20 to 40 minutes to run and approximately 4-6 hours for a MEM-128.*

The routine checks the memory completely for stuck address or data lines and crosstalk between cells by performing a walking 1's pattern test, walking 0's and galpat. This test is intended to be run once every 2 or 3 months of the instrument life.

TEST 6 - QUICHK (QUICK CHECK - SHORT VERSION OF GALPAT)

Test 6 is a quick check of memory which, although less complete than test 5, only requires about 45-60 seconds to run and may be handily used to verify that the board is functioning properly. Test 6 checks for stuck address lines and stuck data lines and normal read/write at the RAM.

2.2.5 OPTIONAL TEST FUNCTIONS AVAILABLE: With TEST Command using Purchasable Speed Test hardware

TEST 7 - User Port Test
8 - Access Time Measurment
9 - Fast Check Access time measurement
10 - Shmoo Test for "Worst Case" access time

2.2.5.1 ACCESS TIME MEASUREMENTS

Using Tests 8, 9, and 10 may also be made from the end of the ROM Simulation cables as well as the WCS board edge. Including the ROM Simulation cables has the advantage of providing a measure of preformance actually achieved at the Prom sockets of the host processor.

Hookup requirements for measurements including ROM Simulation cables are outlined in section 3.9.4.

NOTE: When conducting Speed-Test measurements using ROM Simulation cables the test will always fail on enable (EN). This is normal. Continue the test to completion by entering "1", (CR) four times. This is not required when conducting Speed-Tests at the WCS board edge using the Speed-Test address and data carves.

TEST 7 - USRPRT (USER PORT)

Test 7 is a test to verify the functioning of the user port (fast port) of a WCS control-store. It requires installation of the Speed-Test board and its interconnect cables to the board under test. This is not a speed check but a functional checkout of the board. On MEM-32 and MEM-128, all board switches should be placed in the upward position prior to running the test.

2.2.5.1 ACCESS TIME MEASUREMENTS (CONTINUED)

TEST 8 - ACCESS (ACCESS TIME)

This speed check is a thorough measurement of user-port access time. The user is prompted to specify the speed to be tested in a range from 2 to 254 nanoseconds. When a read error is encountered the user may choose to either continue the test to look for other failure locations, or abort the test. ACCESS requires approximately 45 minutes to run on a MEM-32 and approximately 5 hours on a MEM-128. The test yields a high quality measurement, using a "ping-pong" pattern which guarantees all possible address transition patterns with worst-case data. The access time measurement is performed on each operation.

TEST 9 - FASTCK (FAST CHECK - SHORT VERSION OF ACCESS)

FASTCK is a routine to make a rapid (about 60 seconds) but less complete check of memory board access time. The test checks the memory access time specified by the user at only a few locations which have been determined to be close to worst-case, through experience and analysis.

TEST 10 - SHMOO (SHMOO - ONE-DIMENSIONAL TEST vs. TIME)

Unlike Tests 8 and 9, which operate at one access time, specified by the user, SHMOO starts from the user-stated access time and works down, in 2-nanosecond increments. For example, the user enters 60ns as a starting point; if the SHMOO finds that the WCS board under test passes a test simalar to Test 9, it decrements and test at 58ns. This test-decrement-test sequence continues until the board fails in some way. At that time, the CRT displays the Worst-Case Access-Time at which the board failed, and all available data on what the failure mode was.

2.3.1 SUMMARY

ENTER

Key In:	ENTER (CR)
Enter From:	Top CMND level
Parameters:	None
Description:	Displays WCS memory contents from start address to start address + 3, a 4-microword window into WCS memory. Subcommands allow entry, modification, and display of all locations in the currently selected array. Cursor controls permit scrolling.
Exit:	QUIT (CR) returns to top CMND level.

SUB-COMMANDS

Address:

Key In:	ADDRESS (CR)
Entry From:	ENTER
Parameters:	Address in hex or octal (as SETUP).
Description:	Displays 4 lines of data at the specified address, on CRT lines 5-8. Current address is always displayed on CRT line 3, above the data field.

FUNCTION KEY SUB-COMMANDS

(ENTER):	Moves the cursor to the data field in preparation for entry. Bit number of current cursor and the binary expansion field of 5 next characters added to CRT line 4.
(CR):	Enters the data on the current edit line to WCS memory and advances the cursor to the next line. Scrolls display if necessary.
(CLEAR):	Clears data entry on current line and restores data to old value.
(DEL):	Deletes last character entered and restores it to previous value.

2.3.1 SUMMARY (CONTINUED)

Cursor up/down:	Scrolls data field to higher or lower address.
Cursor left/right:	Moves cursor right or left in the data field. Binary expansion fields scrolls thru word.
(C & H)*:	Exits to sub-command level when C & H or Home is depressed.
Hex Keypad:	Suggested for all data and parameter entry; main keyboard also works, for Octal or Hex values.

FILL

Key In:	FILL (CR)
Entry From:	Top CMND level.
Parameters:	Start Address in Hex or Octal. Last Address in Hex or Octal. Word Constant in Hex or Octal, plus binary. (ENTER DATA).
Description:	Fills a memory block with the specified word, a constant such as NO-OP, chosen by user.
Exit:	To top command level (CMND) on completion.

MOVE

Key In:	MOVE (CR)
Entry From:	Top CMND level.
Parameters:	Source Address in Hex or Octal. Destination Address in Hex or Octal. Number of locations in decimal.
Description:	Moves a block of data of at least 1 word from one memory location to another. The original data remains intact unless written over.
Exit:	To top command level (CMND) on completion.

*C & H Key on STEP-2 means "cancel and home the cursor."
HOME key on STEP-3 has same function.

2.3.1 SUMMARY (CONTINUED)

SEARCH

Key In:	SEARCH (CR)
Entry From:	Top CMND level
Parameters:	Start Address in Hex or Octal. End Address in Hex or Octal. Comparison word in Hex or Octal. Don't care word; 0 = don't care, 1 = care; displayed in binary; entered in Hex or Octal
Description:	Searches the specified block of code for a data pattern of ones, zeroes, and don't cares. When a match is found, the address and memory word is displayed and the search waits for the user to depress (CR) to continue.
Exit:	When complete, the search routine waits for the user to depress (CR) and exits to top command (CMND) level. Search may be terminated before the entire memory is searched by depressing the C & H or HOME key.

2.3.2 ENTER COMMAND

The ENTER command with its associated eight sub-commands and function key commands provides a convenient machine-code editor. The format of this command is:

ENTER (CR)

No parameters are required.

Entry to the ENTER command is always from top command level, as indicated by the message CMND on line 1 of the display.

Following the carriage return (CR), the ENTER command sets the STEP-N instrument in an edit mode and initializes the display and subcommands.

2.3.2 ENTER COMMAND (CONTINUED)

At this sub-command level, the operator may enter subcommand ADDRESS or QUIT or function-key commands. Function key commands active at this level are cursor-up and cursor-down and function-key ENTER.

The top CRT display line presents the current top level command being executed and instrument status, a reminder of the array-number, array size and starting address declared in the Setup mode. The third CRT line is the subcommand-prompt line which is indicated by a blinking cursor. CRT line 4 always presents the current cursor location in user address space. Once the function-key ENTER is hit, CRT line 4 adds more information: The bit number of the MSB at the current edit location and a "binary expansion" of the data from the cursor location to 4 characters ahead of the cursor. Thus, the address and bit-number amount to "X-Y co-ordinates" of the current cursor position, and the binary expansion "window" is a magnification in binary code of the data at (and to the right of) the cursor location. If set up in Hex, this binary window is five (5) nibbles or 20 bits shown in groups of four (4); if in Octal, the binary window is five (5) triplets or 15 bits, displayed in groups of three (3).

The following description of sub-commands and function key commands are most readily understood if each command is actually entered into STEP-N and tried, as the descriptions are read.

The format of subcommands and function key commands are:

ADDRESS

ADDRESS (CR)

2.3.2 ENTER COMMAND (CONTINUED)

One parameter is required, the desired edit address in user address space. The address must be in the current machine base (hex or Octal) and must lie within the user address space. This command "jumps" the visible window thru memory.

Following the (CR), four lines of data starting at the specified address are displayed with the current address displayed on line 3 above the data field. Again, scrolling is possible at/from this new location. After an ADDRESS jump, all four cursor control keys and the ENTER function key work the same as at address 0.

QUIT

QUIT (CR)

No parameters are required. Cursor must be at CRT line 3 in order to QUIT the ENTER mode. This may require C & H (HOME) to get the cursor up out of CRT lines 4-8.

Execution: following the (CR), this subcommand returns the STEP-N instrument to top command level (CMND).

CURSOR UP/DN

Keystroke or key-hit command. (No (CR) is needed.)

No parameters are required. Notice that holding cursor key down causes continuous scrolling.

2.3.2 ENTER COMMAND (CONTINUED)

Execution proceeds immediately following the keystroke and causes the display (CRT lines 4-8) to scroll to higher or lower addresses. Try the automatic repeat.

Because this is a WORD-ORIENTED editor, organized to minimize user errors, the up-down cursor keys won't work if the cursor is "into the microword." That is, the cursor must be at CRT line 3 or at the left-most (MSB) position of lines 4-8 for up-down scrolling to work. Hit (cursor ←) or (CLEAR) to move the cursor back to the left-most nibble/triplet position.

ENTER (FUNCTION KEY)

(ENTER) Keystroke or key-hit command. (No (CR) is needed.)

No parameters are required.

Execution proceeds immediately following the keystroke, causing the STEP-N instrument to proceed to data entry level. The cursor is positioned at the first character in the data field (left-most position) in preparation for entry. Bit number of the current cursor position and the binary expansion field of the first five (5) characters are added to line 4 of the display.

2.3.2 ENTER COMMAND (CONTINUED)

FUNCTION KEY COMMANDS WITHIN THE ENTER SUBCOMMAND

(CLEAR) Keystroke or key-hit command. (No (CR) is needed.) No parameters are required.

Execution proceeds immediately following the keystroke and clears the data entry on the current line, and restores data on the current line to its previous values. This command provides easy error recovery for the user. It returns the cursor to the left-most position, necessary for up-down scrolling.

(DELETE) KEY. Keystroke or key-hit command. (No (CR) is needed.)

Execution proceeds immediately following the keystroke, deletes the last data character entered and restores it to the previous value.

CURSOR UP/DOWN KEYS. Keystroke or key-hit command. (No (CR) is needed.)

Execution proceeds immediately following the keystrokes, moves the cursor to a higher or lower address, and scrolls the display if necessary.

CURSOR LEFT/RIGHT KEYS. Keystroke or key-hit command. (No (CR) is needed)

Execution proceeds immediately following the keystroke, moves the cursor left or right in the data field, and updates the binary expansion field for the current cursor position. (Scrolls it through the word).

2.3.2 ENTER COMMAND (CONTINUED)

(C & H) CANCEL AND HOME*. Keystroke or key-hit command. (No (CR) is needed.)

Execution proceeds immediately following the keystroke, exits data entry level, and returns to ENTER subcommand level, with cursor moved back to CRT line 3.

(CR) CARRIAGE RETURN. Keystroke or key-hit command.

Execution proceeds immediately to enter the data displayed for the current edit line, (the line containing the cursor) into WCS memory. The cursor advances one line and the display is scrolled if necessary. All data maybe entered from the HEX keypad on the instrument keyboard (recommended) but the main keyboard also works.

2.3.3 FILL COMMAND

The format of the FILL command is:

FILL (CR)

Parameters required are start address, end (last) address and word constant (ENTER DATA).

Addresses specified must be within the current machine address space and word constant must be in the current machine base (Hex or Octal).

Entry to the FILL command is always from top command level. Following execution, the machine returns to top level (CMND).

*Use (HOME) function key on Step-3. It does the same thing as Step-2's (C & H) key.

2.3.3 FILL COMMAND (CONTINUED)

Execution proceeds to fill the specified memory block with the specified word constant after the (CR). The fill command provides a convenient way to initialize all or portions of the user control store to a desired microword.

2.3.4 MOVE COMMAND

The format of the MOVE command is:

MOVE (CR)

Parameters required are source address, destination address and WORD COUNT (number of locations).

Source address specifies the first location of the data block to be moved. Destination address specifies the first location of the destination (to which the block is to be moved). Number of locations specifies how many words are to be moved. Both source and destination blocks are checked to be within current user address space.

Execution proceeds after (CR), to move a block of data of at least 1 word from one memory location to another, up or down in WCS memory. The original data remains intact unless written over. Thus the MOVE is non-destructive, like the usual "copy" command. Upon completion, the command exits to top level (CMND). The MOVE command provides a convenient way to move data blocks during testing in real time situations when jump/insert types of patching are not appropriate.

2.3.4 MOVE COMMAND (CONTINUED)

Another use is saving clean copies (in unused memory areas) of code blocks that are about to be experimentally modified. If the experiment flops, copy the saved version back over the top of it. This can save a download.

2.3.5 SEARCH COMMAND

The format of the SEARCH command is:

SEARCH (CR)

Parameters required are start address, last address, search word and don't-care word. Start address and last address specify the block of WCS memory to be searched (and must be within current user address space). The comparison word specifies the word to be searched for. The don't care word provides the user a convenient mask to specify one or many don't-care bits. For this specification the convention adopted is, a 0 in a bit position specifies don't care and a 1 in a bit position specifies care. Binary expansion helps the user enter in Hex but check in binary.

Entry to the SEARCH command is always from top command level (CMND) and exit is to top command level when complete.

Once the don't-care word is correct, execution proceeds following (CR). The WCS is searched in the specified range for the specified pattern of ones, zeros and don't cares. When a match is found, the address and memory word are displayed and SEARCH waits for the operator to depress a control function key.

2.3.5 SEARCH COMMAND (CONTINUED)

At this point, either of two control function keys may be selected:

(C & H*) CANCEL & HOME. Keystroke or key-hit command. (No (CR) is needed)

Pressing C & H causes the search to be terminated before the entire memory block is searched and returns the instrument to top command level (CMND).

(CR) CARRIAGE RETURN

Pressing (CR) causes the search to continue to the next match, then return to top command level (CMND) when SEARCH is complete.

The STEP-N SEARCH command provides the user a convenient means to find all locations where a particular bit is set in his microcode or to locate and later modify a certain set of reference addresses. Notice that any number of binary 1's can be set in a mask; therefore <u>any</u> mask pattern involving <u>any</u> number of fields, however specified (1-bit, 5-bit, etc.) can be used. In conjunction with the MOVE command, it can greatly simplify patching and debug at the microcode level.

2.4 MONITOR COMMANDS

2.4.1 SUMMARY

NOTE: Please note distinctions throughout this section as to which commands are available on all STEP machines (STEP-N, including STEP-2 and STEP-3) and which are on STEP-3 only. (STEP-3 has all the STEP-2 Monitor commands.)

Key In:	MONITOR (CR)
Entry From:	Top CMND level, STEP-N
Parameters:	None
Description:	Enters monitor level (To MON HLT) and displays current breakpoints and waits for operator commands. See following writeup for additional information.
Exit:	QUIT (CR) returns to top command level and disables WCS from the user.

SUBCOMMANDS

BREAKPOINT

Key In:	BREAK (CR)
Entry From:	MON RUN or MON HLT, STEP-N
Parameters:	Breakpoint number; 1, 2, or 3 Breakpoint address in Hex or Octal
Description:	Sets the chosen breakpoint (1, 2, or 3) depending upon organization parameters. Displays allowed breakpoint ranges as a function of setup parameters.
Exit:	To monitor level on completion.

2.4.1 SUMMARY (CONTINUED)

HALT

Key In:	"H" key (hold until MON HLT appears, 1 sec.)
Entry From:	RUNNING or MON RUN, STEP-N.
Parameters:	None
Description:	Changes clock and clock-control outputs to halt state.
Exit:	To MON HLT.

QUIT

Key In:	Q Key (hold until cursor appears, 1 sec.)
Entry From:	RUNNING, STEP-N
Parameters:	None
Description:	Changes mode from RUNNING to MON RUN. Clocks stay active, cursor reappears so that sub-commands can be keyed in.
Exit:	To MON RUN. (Do RU again to get back to RUNNING after subcommands.)

PULSE

Key In:	"P" key (momentary.)
Entry From:	Monitor levels, any of three, STEP-N
Parameters:	None
Description:	Causes output reset lines to change state for 200ms. If the key is held down the action is repeated. CRT shows "P", top right.
Exit:	To monitor level.

RUN

Key In: RUN (CR) (R is enough in STEP-2.)

Entry From: MON HLT MON RUN, STEP-N

Parameters: None

Description: Enables the WCS (Writable Control Store) and displays the current array address from the user system. When a breakpoint occurs once, the appropriate breakpoint is displayed in inverse video. If a breakpoint occurs repeatedly, the breakpoint is flashed. Starts a Trace if Trace has been previously ARMED.

NOTE: A Trace is started upon entry to RUN if it has been previously armed, otherwise the Trace memory contents are not altered, but saved for future use.

Exit: Puts STEP-N in RUNNING; the "Q" key initiates exit to MON RUN. When RUNNING or in MON RUN, the "H" (and "S", in MON RUN, only, STEP-N keys halt the target processor and change display to MON HLT.

SINGLE STEP

Key In: "S" Key (Momentary; hold for auto repeat)

Entry From: MON RUN or MON HLT, STEP-N

Parameters: None

Description: If STEP-N is in MON RUN, "S" causes the processor to halt. If halted, "S" initiates one clock cycle. CRT displays the current array address and breakpoint status. If the "S" key is continuously pressed, single step is repeated.

Exit: To MON RUN on completion. (See also N-STEP, a related STEP-3 subcommand, below.)

CYCLE

Key In: "C" key (Momentary; hold for auto repeat.)

Entry From: MON HLT, STEP-N

Parameters: None

Description: Initiates a series of single steps until CYCLE I becomes true. Displays the current array address and breakpoint status.

Exit: To MON HLT on completion. (See also M-CYCLE.)

NSTEP

Key In: Nnnn (CR)

Entry From: MON HLT or MON RUN, STEP-3 ONLY.

Parameters: Number of single-step pulses desired, is stated as part of the command, nnn. User is neither asked for leading zero's nor scolded, so N3 (CR) NØ3 (CR) and NØØ3 (CR) work equally well. The field nnn can be 1 thru 250, in decimal.

Description: Single-steps the target processor nnn times.

NOTE: Clock pulses occur at the rate of 1-2 per second. "RUNNING" is shown on CRT top line in reverse video once for each pulse. To adjust pulse width, see capacitor formula in 3.5.

Exit: To MON HLT.

MCYCLE

Key In: Mmmm (CR)

Entry From: MON HLT or MON RUN, STEP-3 ONLY.

Parameters: Number of single cycles desired, mmm. Field mmm may or may not have leading zeros, can be 1 to 250 in decimal.

Description: Cycles the target processor mmm times.

NOTE: Clock pulses within each burst (cycle) occur at about 20 microsecond intervals. About one cycle per second is the rate of separate bursts.

Exit: To MON HLT.

EXCHANGE

Key In: Exchange (CR)

Entry From: MON HLT or MON RUN, STEP-N

Parameters: None

Description: Changes the monitor functions being displayed to put the other array onto the CRT.

NOTE: This does not disable the WCS or the user system. Breakpoint status from the undisplayed array is saved and displayed when Exchange is used.

Exit: To monitor level on completion. The top line of the display indicates the currently selected array.

FORCE™ AN INSTRUCTION

Key In: FORCE (CR) (etc.)

Entry From: MON HLT, STEP-3 ONLY

Prompts: Force Word= Clock Ticks= (1-250)

Description: FORCE™ is a command which forces a user-specified instruction into the target processor and ticks the user clock a specified number of times. The command may be entered from monitor halt only, to avoid contention problems with the target processor. The user is prompted for the FORCE word with the last word FORCEd or JAMmed and prompted for the number of clock-ticks required to force the instruction. The prompt for clock-ticks also shows the user the number of ticks he used, last time he did a FORCE or JAM. Output enables remain true and do not glitch.

FORCE is powerful because, knowing his microword structure, the user can construct one or more words to control his target processor in any conceivable way. (e.g. reset, jump the sequencer, pop stack(S), preset port(S), reload registers, seize busses, set/cancel flags, etc.) STEP-3 will force the instruction without altering the contents of user WCS programs, and then return to the MON HLT state.

Exit: To MON HLT.

JAM AN ADDRESS

Key In: JAM (CR)

Entry From: MON HLT, STEP-3 ONLY

Prompts: Address=
Clock Ticks= (1-250)

Description: JAM is a command which forces the contents of a user address location into the target processor and ticks the clock the specified number of times. It does not modify the user memory address. The command has the same capability as FORCE, IF the desired instruction already exists in WCS, AND IF its address is known.

JAM provides the user a new capability. It may be utilized for controlling the path of execution or for a variety of powerful debug purposes. (FORCE has inherently greater flexibility, but JAM maybe faster for foreseen uses.)

For instance, JAM lets the user store away in unused memory a whole "passal" of friendly jumps and calls and JAM-execute them whenever he wishes. Friendly jumps and calls may be to such things as test programs, "Examine State" routines, or simply diagnostices.

Exit: To MON HLT

RA-REPLACE A/RB-REPLACE B

Key In: RA (CR) or RB (CR)

Entry From: MON HLT, STEP-3 ONLY.

Prompts: Replace word=
Address=

Description: Two replace commands are included in STEP-3: RA and RB. These commands replace the contents of user memory (WCS) at the specified address with the user-specified replace word. The word replaced is swapped with new replace word to provide an easy means of restoring the "original" data word. There are two registers A and B not in the WCS; when RA is executed, the WCS word at user-specified location is swapped into register A, and the word that was in A takes its place in WCS. Similarly with RB.

RA-REPLACE A/RB-REPLACE B

Description: Replace is entered from monitor halt only and treats output enable bits the same as force does. Replace A and B provide the STEP user a convenient, fast way to do program patching and installation of software breakpoints.

Exit: To MON HLT.

XSTATE™ (REQUIRES TRACE)

Key In: XSTATE™

Entry From: MON HLT, STEP-3 ONLY

Escape: Q Key-hit; no (CR) is needed.

Description: XSTATE™, Examine State™ is a command that operates in conjunction with user-written routines to display the contents of registers (or even more generally, any state information from the user system) on the STEP-3 CRT. The XS command may be entered from monitor halt only.

Execution of XS requires two signal inputs, UCTL1 and UCTL2, which must be controlled by the user routine. UCTL1 and UCTL2 input probes are supplied as part of the Trace data probes which provide a convienient interconnect to user control points. Usually the UCTL signals can be readily generated in one of two ways: By utilizing a spare control store bit, or a signal from any convenient latch in the target system which is set at the desired time. Following UCTL1 true, the user routine is responsible for setting the control bit false on the next clock tick to avoid multiple display of the same data. A general flow chart of the logic process required in the user routine is shown in Fig. 2.4.1. Integration of the XS routine provides the user a convient means to perform a FORCE™ or JAM to point his target processor to XS code (written in his own language,) and step thru a routine to collect the desired state information.

Upon execution of XSTATE™, STEP-3 rapidly single-steps the target processor until UCTL1 goes true, which will cause the current information at the Trace Data probes to be displayed in Hex, Octal or Binary.

The target processor will then continue single stepping while subsequent UCTL1's go true (when the second and subsequent chunks of valid data occur on the target bus and STEP-3 displays them on the CRT) or until UCTL2 goes true, signifying a "done" condition. The display then remains intact until a "Q" command initiates a return to monitor halt. Up to 20 16-bit hex values may be displayed at one time (4 on each of 5 CRT lines) and the display will scroll upward as new values are added. User diagnostics may include pauses for inspection.

XSTATE™ (CONTINUED)

Description: The Examine State™ command is a totally new and unique capability for STEP-3 instruments. It provides a convenient means for the user to examine the contents of registers or the data paths anywhere in the system; i.e. wherever he places the trace data probes.

LSAMPLE (LAST SAMPLE) (REQUIRES TRACE) (STEP-3 ONLY)

Key In: Unnecessary

Enter From: MON HLT, MON RUN, RUNNING
All automatic; always on display, LS=XXXX (hex)

Parameters: None

Description: The MONITOR displays (MON HLT, MON RUN, and RUNNING) include a display output of the current contents of the trace data probes. Since it is normally one clock tick behind the rest of the system, it is labeled "LS" for Last data sampled.

NOTE: The sample provided is a totally asynchronous sample, with no chance of sampling real time data at bit slice processor speeds. The LSAMPLE data is only guaranteed following processor single step operation.

Exit: Unnecessary

TRACE COMMAND SUMMARY

Key In: TRACE (CR)

Entry From: MON RUN or MON HLT, STEP-N

Parameters: Various - selected from "Self-Teaching" menus see 2.4.5.

Description: Selects proper Trace equation, logically assigns Trace breakpoints to system breakpoints, sets trigger position within traced information. Automatically ARMS next Trace.

Exit: To MONITOR level on completion

EXAMINE TRACE

Key In: XTRACE (CR)

Enter From: MON RUN or MON HLT, STEP-N

Parameters: None

Description: Displays the results of last trace run starting at the trigger point. If trace has not compelted, forces a completion and displays the trace starting with the last stored value. Cursor controls permit scrolling through Trace memory.

Exit: On QUIT (CR) to Monitor level.

FORMAT

Key In: FORMAT (CR)

Entry From: XTRACE, STEP-N

Parameters: 1, 2, 3 (CR)

Description: Selects the displayed format of the data inputs- 1=HEX, 2=OCTAL, 3=BINARY. *NOTE: When 80 bit expanded Trace installed, format is restricted to HEX only.*

Exit: To XTRACE

DUMP

Key In: DUMP

Entry From: XTRACE, STEP-3 ONLY

Parameters: Start line, number of lines

Description: Dumps the chosen contents of Trace across the previously selected I/O port.

Exit: To XTRACE on completion

ARM

Key In: "A" key

Enter From: MON HLT, MON RUN, STEP-N

Parameters: None

Description: Arms STEP-N to start next trace. TRACE STATUS= ARMED message displayed.

Exit: To Monitor

LXXX (LINE #)

Key In: LX, LXX, or LXXX (CR) where X, XX, and XXX are line numbers.

Enter From: XTRACE

Parameters: Line number included in command. Example: L9, LØ9, LØØ9 will address line nine.

Description: Changes trace readout to the specified line number.

Exit: To XTRACE

TRACE-DISABLE COMMAND (STEP-3 ONLY)

Key In: DISABLE (key-hits no (CR) is needed)

Enter From: MON HLT, STEP-3 ONLY

Parameters: None

Description: The STEP-3 trace design has been upgraded to incorporate new signal timing on "TD" (Trace Done) and "TGD" (Triggered) BNC outputs. A new probe design provides greatly improved setup and hold time requirements. Edge counting on the Q1 and Q2 qualified inputs may be user selected with a jumper. also, a new DISABLE command has been added to allow the user to "turn off" the TD and TGD outputs. New timing on TD and TGD coupled with the DISABLE command provides the ability for the user to utilize synchronous trace triggers and trace completions to interact directly with processor control inputs, adding new power to STEP-3 debug facilities. The DISABLE command allows the user to disable the TD and TGD outputs to allow him to continue to run from a breakpoint. Essentially it prevents the inherent deadlock condition which occurs when the system halts on a breakpoint. TD and TGD timing have been changed to only go true when a trace naturally completes (i.e.; not forced done) or naturally triggers, eliminating all possible glitching on the outputs at inopportune times.

2.4.1 SUMMARY (CONTINUED)

XPORT

Key In: XPORT

Enter From: MON RUN or MON HLT, STEP-3 ONLY

Parameters: None

Description: Statically reads in 32 bits via Speed-Test option board, displays on CRT in format.

Exit: To MON RUN or MON HLT

WPORT

Key In: WPORT

Enter From: MON RUN or MON HLT, STEP-3 ONLY

Parameters: Enter 16 bits as 4 Hex or 6 Octal character

Description: Statically outputs 16 bits via Speed-Test board outputs, TTL swings.

Exit: To MON RUN or MON HLT.

TRACE STATUS MESSAGES

ARMED - STEP-N ready to start a new trace on entry to RUN.

TRACING - STEP-N actively storing information in Trace memory pending satisfaction of trigger equation.

DONE - Current trace completed due to either a valid trigger occurrence or forcing a completion through examination of Trace memory.

TSETUP ERR - Assigned breakpoint has no value.

TRIGGERED - Current valid trigger has occurred but the 250 bytes of trace memory has not completely filled.

2.4.2 MONITOR FUNCTION

MONITOR is used to run the user program, control the state of the target processor, and examine processor operation. The outputs of the ROM simulation modules are enabled when and only when STEP-N is in MONITOR Mode. When enabled, the WCS memory can be accessed by the target processor in a read or write mode.

The state of the target processor can be controlled through the keyboard. Simple key commands RUN, HALT, STEP, CYCLE and PULSE actuate the processor-control hardware. The control lines are interfaced by ribbon cable to the target system and are available in both true and complement form. Schematic 0001053, sheet 1, shows the hardware used to implement the processor control functions.

To examine the operation of the processor, triggers/breakpoints can be set and monitored without disturbing processor activity. A halt on breakpoint function can be easily implemented. Breakpoint outputs can be used to trigger oscilloscopes, logic analyzers, etc. to aid the debug process.

2.4.3 MONITOR CLOCK-CONTROL STATES AND COMMANDS

The MONITOR command consists of three instrument states: RUNNING, MON RUN, MON HLT. When RUNNING, the current processor address is sampled and displayed and breakpoint state is continually updated. To exit the RUNNING state, two keys can be used: "Q" (QUIT) for entering MON RUN, and "H" (HALT) for entering MON HLT. In MON RUN, the target

processor is still running but address and breakpoint state are not displayed. However, if a breakpoint is reached during MON RUN, the event will be recorded and then displayed when RUNNING.

MON HLT is similar to MON RUN except the target processor is in a halted state. When a two array system is implemented the address and breakpoints for each array can be examined separately through the EXCHANGE command.

The following is a discussion of the various MONITOR commands with entering and exiting sequences, and CRT display associated with each.

PULSE - Pulse operates independently from the other processor control functions and can be obtained at any time by pressing the "P" key. Each time the key is depressed the Pulse lines (P53 pins 1,3; labeled RESET, on schematic drawing 0001053) change state for approximately 200 ms, and a "P" appears in the upper right hand side of the CRT. If the "P" key is held down, the pulses will continue at a repetitive rate, about once a second.

RUNNING - This is the normal mode of operation during debug. To enter RUNNING when in MONITOR type RUN (CR). (R is enough in STEP-2.) In the top left corner of the CRT, the word "RUNNING" will appear. To change breakpoint address, or to single-step the processor, or to exit MONITOR, the "Q" should be pressed until the cursor re-appears on the CRT's command line (line 3). The message "MON RUN" will then be displayed. A sampling of the current processor address will be displayed and updated only during the time "RUNNING" appears on the CRT. RUNNING initiates a trace if trace has been previously ARMed.

NOTE: A trace is initiated upon entry to RUNNING if it has been previously ARMed, otherwise the Trace memory is not altered.

2.4.3 MONITOR CLOCK-CONTROL STATES AND COMMANDS (CONTINUED)

HALT - HALT is the normal machine state when MONITOR is first entered. When in "RUNNING" or MON RUN, HALT can be entered by pressing the "H" key. When in MON RUN, HALT can also be entered by pressing the "S" (single step) key.

QUIT - QUIT is used to exit MONITOR before entering other commands and within MONITOR to get back to the command level from subcommands. When RUNNING, pressing the "Q" key will change the instrument state to MON RUN and enable a new command (such as BRKPT, EXCHANGE ARM, TRACE, XSTATE, FORCE, JUMP, RA, RB) to be entered. When in MON RUN or MON HLT, QUIT (CR) is used to exit the MONITOR command, and go back to top level CMND.

STEP - When in MON HLT, pressing the "S" (STEP) key pulses the RUN/HLT line and enables one clock pulse on the clock line to the target processor. The display indicates "RUNNING" for about 1 second, and breakpoint and address information are updated. When in MON RUN, pressing the "S" key changes processor state to MON HLT. The address appearing on the CRT is sampled while the processor is halted.

NSTEP - Same as STEP (single-step) above, except the STEP-3 instrument will count a specified number of steps (1 to 255). In MON HLT mode, key in N028, for example, and you get 28 steps of the target clock. Since these are at a slow rate (1 or 2 per second), you can watch ADDRESS = and LS = change as you go.

CYCLE - When in MON HLT or MON RUN, pressing the "C" cycle key puts multiple pulses in the RUN/HALT line and multiple clocks on the clock line at approximately 20 usec intervals. The CYCLE IN line (see I/O and clock schematic 0001053.) is monitored, and once it goes true the output pulses are discontinued. The display indicates "RUNNING" and address and breakpoint state are continually updated.

Most STEP users tie CYCLE IN to a target processor signal like "Command Complete" or "Macro Complete" or "Fetch Next Macro," so that the "C" key becomes a high-speed way of stepping thru known blocks of code, then halting.

2.4.3 MONITOR CLOCK-CONTROL STATES AND COMMANDS (CONTINUED)

EXCHANGE - Address and breakpoint state are displayed for one Memory Array only, at any point in time. To change memory arrays EXCHANGE (CR) should be typed.

WARNING: Since STEP-N waits for a CYCLE IN signal to come back from the target, hitting "C" will "HANG" the STEP-N firmware if nothing is hooked to CYCLE IN. Should this happen, hit RESET. WCS contents will not be lost or changed.

MCYCLE - Just as NSTEP gives a counted number of STEPs, MCYCLE generates a counted number of CYCLEs (1 to 255). This command is in STEP-3 only. In general, each cycle may be of different length, as the successive macros executed may be unlike.

WARNING: Firmware connot complete if CYCLE IN is not hooked up correctly. See warning above for CYCLE.

2.4.4 MONITOR BREAKPOINT COMMAND

Step Engineering defines a breakpoint as the detected occurrence of a pre-selected target processor address. Notice that the definition does not include halting on the address.

In STEP-N hardware, a programable breakpoint-compare circuit is part of each memory board, and a breakpoint pulse comes out of a BNC on the board at 50 Ω impedance. But the user is free to decide whether to hook it to STEP-N's EXT HALT, or a scope as a trigger, or to other devices.

BREAKPOINT - Breakpoint can be set when in MON RUN or MON HLT by typing BR (CR). The instrument response is "BR=". The number of the breakpoint to be set is then typed in. The STEP-N instrument then gives the range of breakpoint addresses available for that breakpoint and displays ADDR=. Once the address (Hex or Octal depending on mode) is typed in, the breakpoint is set.

2.4.4 MONITOR BREAKPOINT COMMAND (CONTINUED)

EXAMPLE:

Instrument	Input
	B (CR)
BR=	1 (CR) (to set brkpt 1)
ADDR=	200 (CR) (sets address 200 in brkpt 1)

BREAKPOINT - The breakpoint state is displayed on the CRT. When a breakpoint address is accessed once, the video field will be inverted. If accessed several more times at intervals of several seconds, the inverted field will blink once for every access. If it is being repetitively accessed several times per second, the breakpoint will blink constantly, about twice per second.

If two arrays are in use, each array's breakpoints start with breakpoint 1 and the appropriate array must be accessed (using the EXCHANGE command if necessary) before setting the breakpoint.

Only the breakpoints for the displayed array are seen on the screen. However, if the breakpoint address in the other array is being accessed, the information will be stored and displayed when EXCHANGE command is used to change arrays.

Breakpoints from both arrays can be used by Trace in the same trigger equation, either by direct keyboard assignment or by wiring the BNC breakpoint outputs as external (qualifier) inputs to Trace.

All breakpoints are available in real time on the appropriate BNC output. To implement the halt on breakpoint feature, a cable tying the selected breakpoint output to the XHALT input should be installed. The CLK OUT lines will be disabled on the next clock pulse and the RUN/HALT lines will change state approximately 100ns after the breakpoint address is reached. NO direct indication of the halt on breakpoint is displayed on the CRT.

BREAKPOINT - (concluded)

Every STEP ROM Simulation cable set has a BRK (breakpoint enable) clip, attached to the Master module (orange buffer box). Thru the address cable, this STEP input (also called User Latch) can enable/disable (mask) the breakpoint circuitry on every MEM board in the array, and Trace.

Use of the appropriate signal on BRK (typically UAC, user address clock, perhaps ANDed with another term) insures that the STEP boards will use only valid addresses as connector inputs. Switches 4 and 5 on the MEM boards pick high/low true and edge/level sensitive for BRK.

NOTE: *The next two commands WPORT (Write 16-bit port) and XPORT (Examine 32-bit port) make use of the Speed-Test board, if installed, in STEP-3 only. When it is not being used for testing memory boards or ROM cables, the Speed-Test board can be a convenient "window on the world". The user can statically read and write thru this card to anything that will accept TTL levels. Hookup notes appear in section 3.11.*

Step Engineering envisions the use of WPORT, the 16-bit output from STEP-3 as a way of keyboard controlling test conditions, in testing flags in the target processor, or even supplying a static simulation of the hardware the target machine will ultimately control. XPORT can be used to read in BUSSES, FLAGS or registers in a static basis. Uses are limited only by the user's architecture or imagination.

XPORT (EXAMINE 32-BIT PORT)

Key In: XPORT

Enter From: MON HLT or MON RUN, STEP-3 ONLY

Parameters: None

Description: This command reads 32-bits of data from the Speed-Test board input lines. The data is displayed as:

P4=XXX P3=XXX P2=XXX P1=XXX

Each Port (PN) corresponds to an 8-bit input port on the Speed-Test board. The exact correspondence between the displayed data and the physical port connections is as follows:

2.4.4 MONITOR COMMAND (CONTINUED)

LOGICAL DISPLAY			PHYSICAL CONNECTION	
P1	bit-0	(Low-Order Bit)	J12	pin 1
P1	bit-1		J12	pin 3
P1	bit-2		J12	pin 5
P1	bit-3		J12	pin 7
P1	bit-4		J12	pin 9
P1	bit-5		J12	pin 11
P1	bit-6		J12	pin 13
P1	bit-7	(High-Order Bit)	J12	pin 15
P2	bit-0	(Low-order Bit)	J12	pin 21
P2	bit-1		J12	pin 23
P2	bit-2		J12	pin 25
P2	bit-3		J12	pin 27
P2	bit-4		J12	pin 29
P2	bit-5		J12	pin 31
P2	bit-6		J12	pin 33
P2	bit-7	(High-Order Bit)	J12	pin 35
P3	bit-0	(Low-Order Bit)	J11	pin 1
P3	bit-1		J11	pin 3
P3	bit-2		J11	pin 5
P3	bit-3		J11	pin 7
P3	bit-4		J11	pin 9
P3	bit-5		J11	pin 11
P3	bit-6		J11	pin 13
P3	bit-7	(High-Order Bit)	J11	pin 15
P4	bit-0	(Low-Order Bit)	J11	pin 21
P4	bit-1		J11	pin 23
P4	bit-2		J11	pin 25
P4	bit-3		J11	pin 27
P4	bit-4		J11	pin 29
P4	bit-5		J11	pin 31
P4	bit-6		J11	pin 33
P4	bit-7	(High-Order Bit)	J11	pin 35

Description: A low input on an input pin corresponds to a zero bit for that display position. Display in Hex or Octal only, as set in the SETUP command.

X (CR) will re-read and display the port data.
Q (CR) will cause it to exit to MONITOR.

Exit: To MON HLT

WPORT (WRITE PORT 16-BITS)

Key In: WPORT

Enter From: MON HLT, or MON RUN, STEP-3 ONLY

Description: WPORT (Write Port) writes 16-bits of data to the Speed-Test board output lines. The clock is accepted as either a 4-digit Hexadecimal number or a 6-digit Octal number. The mapping between the entered data and the physical output is as follows:

LOGICAL DISPLAY		PHYSICAL CONNECTIONS	
bit-0	(Low-Order Bit)	J10	pin 1
bit-1		J10	pin 3
bit-2		J10	pin 5
bit-3		J10	pin 7
bit-4		J10	pin 9
bit-5		J10	pin 11
bit-6		J10	pin 13
bit-7		J10	pin 15
bit-8		J10	pin 17
bit-9		J10	pin 19
bit-10		J10	pin 21
bit-11		J10	pin 23
bit-12		J12	pin 19
bit-13		J12	pin 39
bit-14		J11	pin 19
bit-15		J11	pin 39

The user may use the CLK line on J10 pin 27 to determine when the data is available on the output pins. This pin is strobed as soon as the data is available, with a positive-going pulse.

2.4.5 TRACE

The Trace trigger equation is easily selected through the front panel. A series of self-teaching multiple-choice menus is presented on the CRT. Each menu indicates possible trigger choices along with the previous selection. The menu presented varies according to previous trigger selection so that invalid equations are locked out.

The general trigger equation has the following form:

NT → C or C → NT (reads as "NT then C" or "C then NT")

N means the number of occurrences to a trigger event, 1-255;

T means trigger input: 2 address comparators, 2 qualifiers, clock;

→ means "followed by" or "Then"

C means combinatorial trigger formed from logical AND, OR of address and qualifiers.

To set up or change the trigger equation, the command TRACE (CR) must be entered from either MON RUN or MON HLT. Use of this command does not affect target processor operation in any way. Each menu in turn will be presented automatically until the entire selection is completed. The CRT display uses the notations "SOURCE 1" and "SOURCE 2" so that the generalized equation is "TRIG=source 1 then source 2." To make a selection, a number representing the chosen item or a value is entered through the keyboard, followed by (CR). Each menu displays the previous selection or a default value for the particular item. If no change is desired, (CR) can be pressed. The final trigger selection is spelled out as a complete logic equation on the bottom line of the CRT.

EXAMPLE: Assume that a Trace on BR1 is desired. The following sequence would be used:

2.4.5 TRACE (CONTINUED)

CRT DISPLAY	USER KEYS IN	STEP-3 ACTION
RUNNING	Q	Exits to MON RUN.
MON RUN	TRACE (CR)	Initiates Trace Selection.
TRACE		Displays first menu.
SOURCE 1 = 1	2 (CR)	Picks TBR1 from selection.
NUMBER OF EVENTS = 1	(CR)	Stays with current default
:	(CR)	values for other selections.
MON RUN		(Set TBR1 to the desired trigger value prior to RUNNING.)

Once the menu selection process is complete, MON HLT or MON RUN is automatically re-entered, with trace armed. The complete list of menu selections is shown in figure 2.4.2.

2.4.5.1 SPECIAL TRIGGER SELECTIONS

In expressions involving TB1·TQ1 or TB2·TQ2, the other TQ input is preset internally to a true condition. Therefore, the resulting equation will be:

CHOSEN EQUATION	ACTUAL EQUATION
TB1·TQ1 → (N)TQ2	TB1·TQ1 → (N)UAC*
TB2·TQ2 → (N)TQ1	TB2·TQ2 → (N)UAC
(N)TQ1 → TB2·TQ2	(N)UAC → TB2·TQ2
(N)TQ2 → TB1·TQ1	(N)UAC → TB1·TQ1

2.4.5.2 OR TRIGGER EXPRESSIONS

Two "OR" trigger expressions are presented as part of the triggering equations:

TB1+TQ1+TQ2
TB1+TB2+TQ1

From these two equations the following equations can also be generated by insuring the third logic term is false:

TB1+TB2, TB1+TQ1, TB1+TQ2, TQ1+TQ2, TB2+TQ1

*UAC is user's address clock.

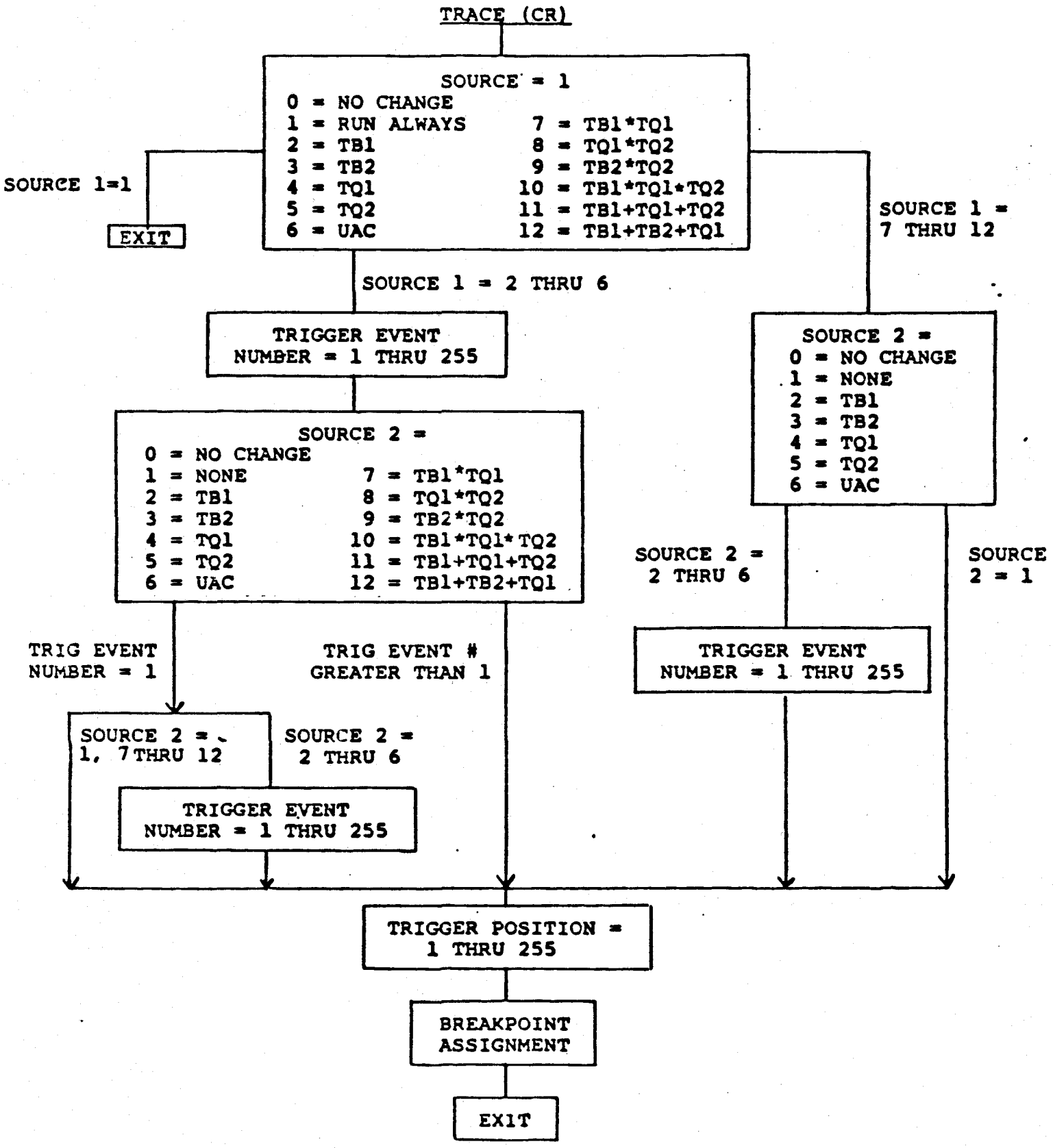


Figure 2.4.2 Menue Selections for Trace

2.4.5.2 OR TRIGGER EXPRESSIONS (CONTINUED)

In the case of the TQ inputs, this can be done by connecting the unused input to a voltage level that is logically false. In the case of an unused trigger breakpoint, it can be assigned an address that will never occur in normal operation. In both of these cases, the remaining two terms of the OR will be the only ones that can go true.

2.4.5.3 EVENT NUMBER

One counter is built into the trigger logic. This counter can be assigned to one of the five trigger inputs: TB1, TB2, TQ1, TQ2, UAC. Its specification permits a trigger on the Nth event of a given input, where N is a number from 1 to 255 (decimal). Hence, it is possible to trigger on the third occurrence of TB1, the two hundredth occurrence of UAC etc.

> *NOTE: In the case of TQ1 and TQ2, one event (or count) occurs each UAC clock time the input is true. Hence if TQ1 is true for six (6) clock periods, an event number of seven (7) would specify the second time TQ1 becomes true.**

This count is specified as part of the menu selection when Event Number is requested. This number is entered in decimal. There are two possible places where Event Number is requested during the menu selection process: When source 1 or source 2 is specified to be one of the five basic trigger inputs, rather than an AND/OR expression. If Event Number = 1 (default condition) is selected for source 1, then the event counter remains available for use on source 2.

*Edge-counting of TQ1 and TQ2 is a STEP-3 alternative; it may be selected with a wire jumper, on the Trace board. E1 jumper should be installed for TQ1 and E2 for TQ2. Both are silk screened on the PC board.

2.4.5.4 TRIGGER POSITION

Trace triggering can be set so as to capture the events leading up to a trigger, around a trigger, or after a trigger. Trigger Position specifies where the trigger occurs relative to the captured data. A decimal number 1-250, default 125, can be used. A Trigger Position of 1 places the trigger at the first event captured. In this case, the following 249 events after the trigger are captured. If a trigger position of 250 were specified, all the events captured would have occurred before the trigger.

> *NOTE: In the case where the Trigger Position is specified to be greater than 1, all events displayed before the trigger may not be valid. Example: if Trigger Position 125 is specified and only 60 clock periods occurred from the initiation of a trace to the trigger occurrence, then displayed trace contents 1 through 65 would be extraneous.*

The trigger position is indicated on the CRT during Trace readout by inverse video on the trigger line number. However, if the operator forces Trace done, the reverse video line becomes line 250 or line 1, depending on the situation, to remind the operator that Trace did not complete in a normal way.

2.4.5.5 BREAKPOINT ASSIGNMENT

The Trace board contains two sixteen bit synchronous address comparators, TB1 and TB2, which are used as part of the Trigger generation logic. These comparators are assigned by the user to the corresponding breakpoints on the Writable Control Stores. Once assigned, they can be set and modified at any time in either MON HLT or MON RUN. The default assignments of the address comparators are:

TB1 to BR1 Array 1
TB2 to BR2 Array 1

Depending upon the configuration of the memory arrays, it may be necessary to assign TB1 and TB2 to different breakpoints.* For instance, if the WCS is organized 6k X 16 using three memories organized 2k X 16, each memory board would be assigned a different address space: MEM 1 would be assigned address 0-2k, MEM 2, 2-4k, MEM 3, 4-6k. In like manner, the breakpoints assigned to each memory board, BR1, BR2 and BR3, would each have a valid address range. Hence, if it were desired to have BR1 set to address 923 hex and TB2 to 10FF hex, TB1 would be assigned to BR2 and TB2 to BR3. Once such an assignment is made, it is displayed on the CRT in Monitor. In the above example, the breakpoint display would read:

BR1= NONE ; B12= 0923 ; B23= 10FF
where BR1 has no Trace breakpoint assignment;
B12 is TB1 assigned to BR2;
B23 is TB2 assigned to BR3.

In any instrument which is configured to have two independent memory arrays, TB1 and TB2 may be assigned to either of the arrays. However, the trace board inputs only one set of address lines. Hence, TB1 and TB2 are physically derived from whichever array the Trace address inputs are connected. To assign TB1 and TB2 to two different arrays or to assign them to an array whose address is not connected to the Trace board is not a valid assignment. Regardless of the assignment, the Trace will be triggered on the breakpoint value specified applied to the address lines of the array connected to the Trace board.

2.4.5.6 SETTING BREAKPOINT

Once a trace breakpoint has been assigned to a memory breakpoint, it can be set or modified in MON RUN or MON HLT. Each time a Trace is initiated through the ARM sequence, the latest value of the breakpoint address setting is read and entered into the Trace logic. Until the Trace is again armed or rearmed, any change in breakpoint settings will not be seen by Trace.

*That is, other values than the defaults.

2.4.5.6 SETTING BREAKPOINTS (CONTINUED)

The ability to change breakpoint settings without having to redefine the Trace equation makes it very easy to follow the path of execution of the processor. Breakpoints can be repeatedly set from Monitor at successive execution points until a problem is located.

2.4.5.7 STARTING A TRACE

Once a Trigger equation has been specified, Trace is initiated from MON. Use the following sequence:

1) If breakpoints are specified as part of the Trigger equation, set the breakpoint values from MON RUN or MON HLT. (Use Q to get from RUNNING to MON RUN.)

2) Re-arm the trace if necessary, by pressing the "A" key. (Arming is automatic when you use T (CR) and page through the trace menus). The message "Trace Armed" will appear in the right hand corner of the CRT. If "A" is not pressed and the Trigger equation is not changed, the previous Trace information will be retained in Trace memory as long as STEP-N remains in Monitor.*

3) Enter RUNNING by keying in RUN (CR). Only in RUNNING is Trace information collected.

2.4.5.8 TRACE STATES

There are five possible Trace States:

ARMED - Trace is ready for initiation and will be activated when RUNNING is entered.

TRACING - Information is being captured in the Trace memory pending satisfaction of Trace trigger equation.

TRIGGERED - While RUNNING, the Trace trigger equation has been satisfied; however, insufficient data has been collected to complete.

DONE - A Trace has been completed.

TSETUP ERR - A Trace setup error has occurred. If all breakpoints used in the trigger equation do not have assigned values, a TSETUP error will be reported on entry to RUNNING, and no trace data will be collected.

*Actually, data in Trace memory will be retained until Power-down, if Trace isn't re-ARMed. But the line-number pointer may get moved in other commands, such as Setup, making the Trace data appear wrong.

2.4.5.9 TRACE COMPLETION

Trace can complete in one of two ways:

A) The Trace trigger equation is satisfied and the Trace memory is filled with the desired information.

B) The Trace is interrupted (and forced "DONE") by the operator, to examine the Trace memory. This can be done by exiting RUNNING to MON RUN or MON HLT and keying "X" (CR) to examine Trace memory.* If this is done in MON RUN, target processor operation is not affected. In either case, the message "TRACE DONE" is displayed in the lower right hand corner of the CRT, after exiting the XTRACE command.

*In STEP-3, "X" is not unique, so use XT for Examine Trace, to distinguish this subcommand from XSTATE and XPORT.

2.4.5.10 TRACE READOUT

It is possible to obtain a Trace readout at any time. If a Trace has not completed, that is, not satisfied the trigger equation, displaying the contents of the Trace memory automatically terminates the Trace. To obtain a Trace readout, MON HLT or MON RUN must be entered and the command XTRACE (CR) (eXamine Trace) used. The first column on the left of the CRT screen indicates the line number of the Trace address and trigger data. Line numbers run from 1 to 250 and the line number of the trigger position is shown in reverse video.

Example: if the trigger position is set at 120, then if Trace completes normally, line number 120 will be reversed. If Trace is forced done through the XTRACE command, then line 250 will be shown in reverse video.

The second column on the CRT screen displays the captured address information. Readout is in hex or octal, depending on whether STEP-N is set to an octal or hex mode. The captured data information is displayed on the right of the CRT in either binary, octal, or hex. The format for this display is chosen using the FORMAT command:

FORMAT=	DISPLAY	COMMENT
1	HEX	
2	OCTAL	
3	BINARY	Default Format

Upon entry to XTRACE, the Trace readout is positioned at the trigger location. The cursor up and down (↑ ↓) keys can be used to scroll through the Trace memory. A wrap-around feature permits scrolling directly from line 1 to line 250 or line 250 to line 1. In addition, a line command has been implemented to allow direct access to any portion of the Trace memory: Lx(CR), or Lxx(CR) or Lxxx(CR) where x is the new line number 1 to 250.

Once the desired information has been obtained from the Trace readout, the command QUIT(CR) can be used to return to MONITOR. Processor operation is not affected during Trace readout.

NOTE: The contents of the Trace memory may be destroyed when leaving MONITOR.

2.4.5.11 NOTES ON IMPROVED TRACE TIMING (STEP-3 80-BIT TRACE)

A 48-bit expander board now augments the 32-bit basic STEP-3 trace. Depth remains 250 words, speed 11 MHz.

Inclusion of the new timing on TD and TGD opens up availability to users of a new and different debug tool, halting at trigger points that may or may not depend on breakpoint per se', but use the power of the STEP Trigger Equation.

Essentially this provides the user a convenient way to run to a well-defined synchronous breakpoint and "look around", i.e., examine the trace memory and examine the path of execution, then examine the target machine, halted. Some users who are used to debugging with a logic analyzer only will probably set the trigger position in the center of the Trace, run past their breakpoint and never notice a timing offset. Other users may adopt a style of setting position at the end of trace for easier interaction with patching and debug.

The important point is that the TGD and TD BNC outputs will occur a few clocks times after the actual trigger occurs, since Trace is a pipelined machine. All data and address bits, as they are shifted through the probe latches and subsequent stages toward the display memory, experience a delay of several clock-times. The exact number, in the range 4-7, depends on the choice of trigger equation.

The interested user, once he has chosen his trigger equation, can experiment to determine the delay, if it must be known. Then he

selects a trigger equation that keeps him running a few ticks past the points he needs to see. This is not a severe restriction since STEP-3 always has the asynchronous breakpoints available on the memory-board BNC's if he must stop directly on an instruction. However, this may be the source of confusion if not explained properly to all project personnel.

The reason for the clock-tick offset specification is that to allow best operation at high speed, the trace data is double buffered in a front-end pipeline, a technique familiar to most users.

2.4.5.12 NEW TRACE PROBES (STEP-3 ONLY)

Beginning in August, 1980, the Trace probes have a jumper option included which may be installed to improve even further the setup and hold time specs. When installed, the data must be positive edge latched only (which most modern systems are anyway). Even without the jumper, the performance is greatly improved.

The specifications are:

DATA PROBES

A) Data setup and hold relative to UDC on either edge.
TSU TYP -4 nsec (data may arrive after the clock)
TSU MAX 2 nsec
THD TYP 8 nsec
THD MAX 12.5 nsec

B) Positive edge only (cut E1 and E2 and install E3)
TSU TYP 3 nsec
TSU MAX 5 nsec
THD TYP 1 nsec
THD MAX 2 nsec

ADDRESS PROBES

A) Address setup and hold relative to UAC on either edge.
TSU TYP -12 nsec
TSU MAX - 4 nsec
THD TYP 15 nsec
THD MAX 25 nsec

B) Positive edge only (cut E1 and E2 and install E3)
TSU TYP - 4 nsec
TSU MAX 2 nsec
THD TYP 8 nsec
THD MAX 25 nsec

"EE" External Enable
TSU TYP 30
TSU MAX 45
THD THP
THD MAX

"UCTL" User control bits (not critical; single-step speeds)
TSU TYP
TSU MAX
THD TYP
THD MAX

2.5.1 SUMMARY - I/O COMMANDS AND SUBCOMMANDS

DUMP, PUNCH

Key In: DUMP (CR); PUNCH (CR)*

Enter From: Top CMND level

Parameters: Format: 0 = MICROWORD
1 = ASCII - HEX SPACE
2 = BNPF*
3 = GENPROM

Start Address: 0000....Machine limit
Number locations: 0000....Hardware limit
**Device: 0 thru 5 (see previous page.)

For Formats 1, 2, or 3

Width 4 or 8
Position: 0 - Memory limit (Nth prom from lsb;
N = 0, 1, 2...)

Description: Dumps or punches the specified number of memory locations starting with the specified user address. During parameter entry, this routine selects the required hardware port and will not preceed until the port status is valid. Execution of these commands is initiated by the final (CR) on exit from TEXT. Dump requires an echo of the (CR). Punch is a TTY routine only and does not require echo. Data I/O device 3 also does not require echo.

Exit: QUIT (CR) enters terminal mode in preparation for execute. (See TEXT below)

Subcommands: BAUD

Key In: Baud (CR)

Enter From: Dump/Punch level

Parameters: Baud = 110, 150, 300, 1200, 2400, 4800, 9600

Description: Sets baud rate on the serial ports.

Exit: On completion, to I/O level.

*STEP-2 only.

**All devices use the same preset/default baud rate, stop bits and parity. TDUMP, TRACE DUMP, uses the entire I/O preset, including selection of device/port, format, baud rate, stop bits and parity (See Trace)

2.5.1 SUMMARY - I/O COMMANDS AND SUBCOMMANDS (CONTINUED)

XPARAM

Key In:	X PARAM (CR)
Enter From:	Dump/Punch level
Parameters:	None
Description:	I/O command setup can be examined through the use of XPARAM (examine parameters) subcommand. Typing X (CR) gives a listing of port, baud rate, stop bits, parity and GENPROM™ control characters. GENPROM™ is an ASCII hex PROM image format whose header, framing and end control characters can be set from the keyboard. GENPROM™ control characters can be entered or modified in LOAD, DUMP, PUNCH, or COMPARE by entering HEADER, FRAME or END (CR) and typing the hex equivalent of the ASCII character desired.
Exit:	Display remains valid until any new command is entered.

2.5.1 SUMMARY - I/O COMMANDS AND SUBCOMMANDS (CONTINUED)

Subcommands:

STOP

Key In: STOP (CR)

Enter From: DUMP/PUNCH level

Parameters: STOP bits = 1 or 2

Description: Sets required number of stop bits on the selected port.

Exit: On completion, to I/O level.

PARITY

Key In: PARITY (CR)

Enter From: DUMP/PUNCH level

Parameters: Parity bit = 0, 1, 2 (even, 3 (odd)

Description: Sets the parity bit (8th or MSB) of data word. (Exit is as above.)

NOTE: Subcommands Baud, Stop, and Parity must be entered at least once through the I/O group to set communication parameters. Once set, Baud, Stop, and Parity remain set until changed. Default values at power on are:

STEP-2	*STEP-3*
Baud = 110	*Baud = 1200*
Stop Bits = 2	*Stop Bits = 1*
Parity Bit = 0	*Parity Bit = 0*

LOAD, COMPARE

Key In: LOAD (CR), COMPARE (CR)

Enter From: CMND level

Parameters: Same as DUMP/PUNCH

Subcommands: Loads or compares the specified number of memory locations starting with the specified start address, except in STEP-N memory image routines. Since STEP-N files contain the user memory address, the load start address is treated as a bias address which is added to the file address; thus providing capability to offset the load data in memory within the available hardware. Execution of these commands is initiated by the final (CR) on exit from TEXT. Load and compare do not echo to the host. The compare command exits when an error is detected and displays the last address successfully loaded on the CRT display.

TEXT

Key In: TEXT (CR)

Enter From: Load, Compare, Dump, Punch, Text, or Top CMND level.

Parameters: None

Description: During execution of text, the STEP-N instrument becomes a terminal. Characters entered from the ASCII keyboard are transmitted to a host machine over the specified RS232 or 20 ma port. Characters echoed are displayed on the CRT. The instrument displays 7 bit ASCII characters received as 64 character ASCII. Control characters are ignored and not displayed. The port requires 7 bit/char ASCII, one or two stop bits, and parity is ignored. Transmitted characters are sent with the parity bit set to one or zero as specified.

On STEP-N, control characters may be generated by depressing shift and numerals 1-9. The available sets are shown in section 2.5.8.

Echo of the final carriage return (or receipt of any character) from the host starts execution of the data transfer. The assumption is that the final line of text is a command to the host computer to perform an I/O function. Upon receipt of the (CR), execution may begin, at both ends of the link.

On initiation of data transfers, start synchronization depends upon receipt of any character from the host. When executing a dump, STEP-N will begin transmission of data after receipt of a (CR) from the host. A maximum time-out of one minute is allowed.

During a load or compare operation, after depression of the final (CR), the message "I/O IN PROGRESS" is displayed and the STEP jumps to the appropriate load routine before output of the final (CR). STEP-N then waits on the first colon to proceed.

NOTE: On system interfaces where the host begins to dump immediately, the message I/O IN PROGRESS may or may not reach the CRT buffer before the first data record arrives. In this instance, data transfer will still proceed properly; however, the message I/O IN PROGRESS may not reach the display prior to arrival of the first data record. A delay of approximately 150 milliseconds before the start character will avoid this probelm and may be easily accomplished by sending a string of control characters before the first colon in the record. Suggested characters to use for delays are nulls or rub-outs. Maximum delay is one minute. Proper operation of all TEXT functions in conjunction with I/O, require restricting the baud rate to 2400 baud.

Exit: Following depression of C & H (Clear & Home), one more line of text may be entered followed by (CR). When (CR) is echoed by the host machine, STEP jumps to the I/O routine specified at entry.

Depressing shift key and Ø, top row, on the alpha-numeric portion** of the keyboard will also exit text to top command level. Essentially, this provides an escape from text.

NOTE: *MICRO-WORD™ format (format 0) is preferable to the other (PROM-oriented) formats (formats 1, 2, 3) for host STEP communications. Benefits are: a single LOAD operation handles the full array width; checksum verifies data; and LOAD address permits partial downloads into WCS, as when a few lines are reassembled and LOADed on top of otherwise correct microcode. Only when it's unavoidable do most STEP users choose the PROM-oriented transmission modes, without these features.*

When confronted with an unknown PROM programmer or PROM-oriented host computer program from which to LOAD the STEP, first determine the starting (or header), Framing and Ending characters it provides. These are programmable on STEP; the left hand group below are the default values in STEP-N.

	MOST USED COMBINATION (HEX)	ANOTHER POPULAR COMBINATION (HEX)
STARTING CHARACTER	STX = 02	SOH = 01
FRAMING CHARACTER	SPACE = 20	SPACE = 20
ENDING CHARACTER	ETX = 03	EOT = 04

**"Shift-V" on STEP-2

2.5.2 UNIQUE FEATURES OF I/O COMMAND GROUP

The I/O Command Group consists of the commands LOAD, DUMP, COMPARE, PUNCH, and TEXT. These I/O commands are unique in several ways:

1) Upon completion of parameter entry, completion of dump or after a communication error, the command maybe re-entered or another command in the I/O group may be entered without returning to top command level. This feature makes multiple commands more easily accomplished, such as multiple loads and compares while utilizing PROM-at-a-time formats.

2) The TEXT command is unique in that it may be entered from top command level or as a subcommand of any of the I/O command groups. When entered from top command level, exit must be via the "shift-zero" (escape-from-text) control key.*

NOTE: I/O communication parameters must be set up properly prior to TEXT entry from top command level. The subcommands to configure the communication ports are subcommands of LOAD, DUMP, and COMPARE. This requires entering an I/O command at least once to configure the serial ports prior to entering TEXT from top command level or I/O command level.

3) When errors during data transfers are reported on the CRT display, the instrument pauses with the error message displayed until any key is hit on the keyboard before continuing.

4) All I/O routines may be interrupted by depressing a key on the keyboard during data transfers.

2.5.3 THEORY OF I/O OPERATIONS

The STEP-N instrument can communicate with external equipment to load data, compare data, and dump data. Operation of these functions require the STEP-N to be properly connected to a serial asynchronous peripheral device according to the instructions contained in section 3.4.

*On STEP-2, this uses the "V" key on the bottom row, Ø when shifted.
On STEP-3, this uses the zero "Ø" key on the top row, Ø before shifting.

2.5.3 THEORY OF I/O OPERATIONS (CONTINUED)

Peripheral devices may include a wide range of RS232-C compatible devices including direct connect to host computers, PROM programmers, remote moderm interconnect to host computers, TTY's, reader/punch devices, and other communication machines.

In each case, establishing a communication link between STEP-N and any peripheral device requires consideration of four basic aspects of the link, which are:

1) Operation of the desired functions.
2) Communication protocol.
3) Data format, and
4) Synchronization of the processes.

A wide range of peripheral devices may be accommodated by a general I/O facility contained in STEP-N which will be described in detail in this section.

Execution of I/O operations consist of a sequence of three phases. (Figure 2.5.1 is a flow chart of the general sequence). First, upon entry of an I/O command from top level, required parameters are prompted to configure the communication parameters and PROM-at-a-time format parameter if changes are required. At I/O command level the command TEXT may be entered when ready to proceed to the second phase or QUIT if the operator wishes to return to TOP command level.

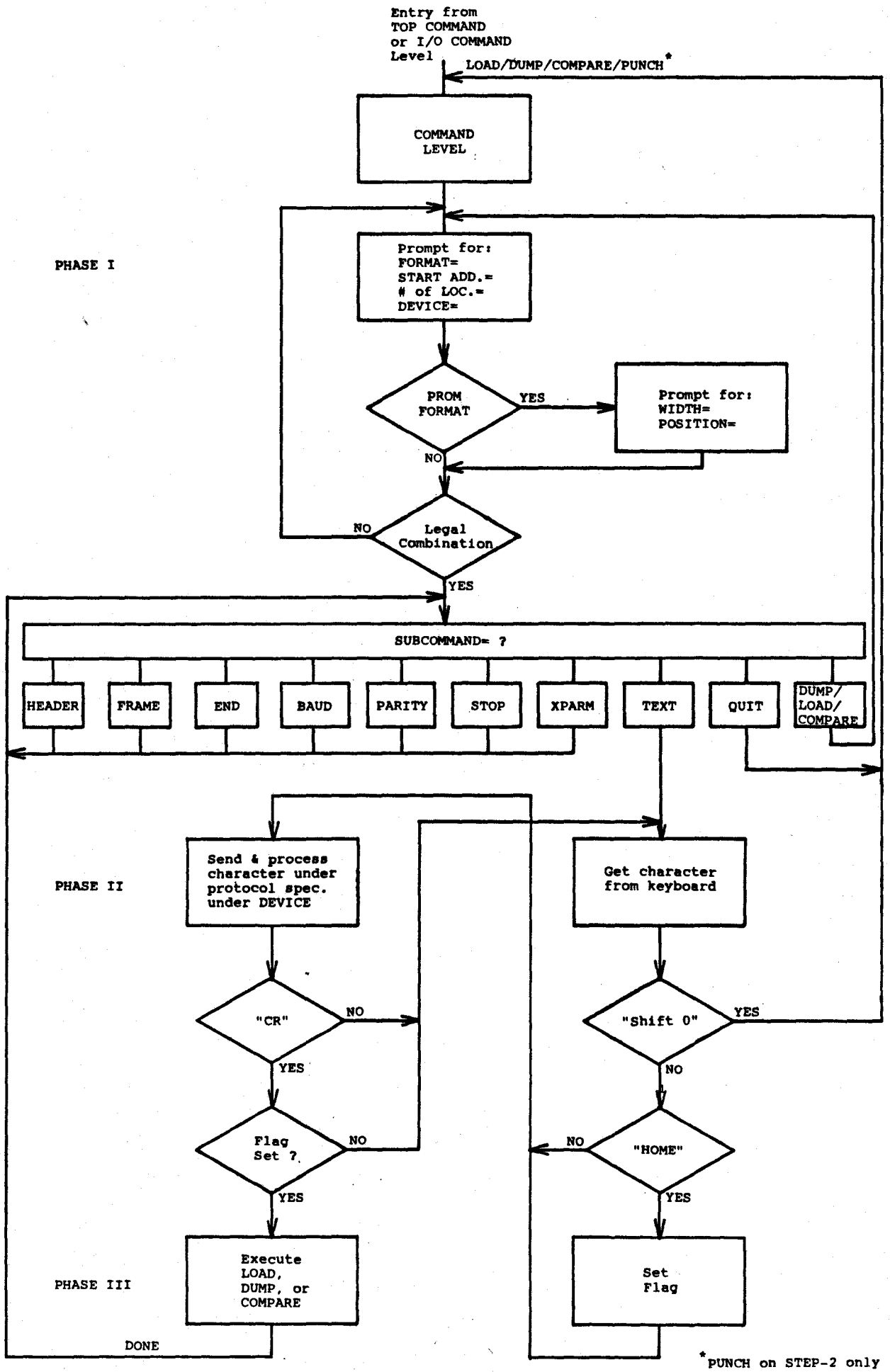


Fig. 2.5.1, General I/O Command Flow Chart

2.5.3 THEORY OF I/O OPERATIONS (CONTINUED)

The second phase is established by entry to TEXT, which establishes communication with a host computer or peripheral device. During execution of TEXT, the STEP-N instrument functions as a terminal to allow the user to access files in a host or issue commands to a peripheral through the ASCII keyboard.

Following depression of the C & H (clear & Home)* one more line of text may be entered (usually a dump or list command to the host) followed by (CR). The third phase of the I/O operation is entered following an echo of the final (CR) from the host.

> *NOTE: For LOAD operations, the echo of (CR) is only required when a device without local echo is specified.*

The third phase of the I/O operation is execution of the specified I/O function. Transmission in progress is indicated on the CRT display by the message I/O IN PROGRESS. Since I/O parameter specifications are essentially the same for all I/O operations, the following section describes the general case, with minor differences noted in the separate command descriptions.

2.5.4 LOAD AND COMPARE COMMANDS: INPUTS TO STEP-N

LOAD (CR)
COMPARE (CR)

Entry to the LOAD and COMPARE commands may be from either TOP command level or I/O subcommand level as illustrated in Figure 6.1. To perform a LOAD, parameter entry and subcommands are entered as described in section 2.5.9, and 2.9.10.

*HOME key on STEP-3.

2.5.4 LOAD AND COMPARE COMMANDS: INPUTS TO STEP-N

The TEXT command is entered and commands to the host or peripheral, if any are required, may be input from the STEP-N keyboard. Synchronization of the load operation and exit from TEXT is accomplished as follows. Prior to entry of the last line of TEXT, usually a dump or list command to the host or peripherals such as discs or cassettes, the operator must depress the Clear-and-Home key (C & H)* on the keyboard.*

The display will scroll up one line to indicate the key has been recognized. The next string of characters are processed normally until the final (CR). At the final (CR), STEP-N begins execution of the load operation by entering a wait loop on the specified port within one character time, and waiting for the start character of the specified format.

Also, a message "I/O IN PROGRESS" is output on the display as an indication that the I/O has started. The display message requires a worst case time of 150 milliseconds to reach the display buffer before start of data. Therefore on peripherals where data transfers begins immediately, the display message may not reach the display; however, the I/O operation will proceed normally. It should be noted that for the vast majority of peripherals, consideration of this display latency time is not necessary.

*HOME key on STEP-3.

2.5.4 LOAD AND COMPARE COMMANDS: INPUTS TO STEP-N

On execution following receipt of a start code in the selected data format, STEP-N translates the data and begins loading or comparing consecutive location from the specified start address. Load and compare do not echo to the peripheral.

> *NOTE: For STEP-N memory image routines in MICROWORD™ format, the start address is treated as a bias address which is added to the address contained in the data record; thus, providing capability to offset the load data in memory within the available hardware constraints.*

Execution of the LOAD or COMPARE operation continues until any one of the following events:

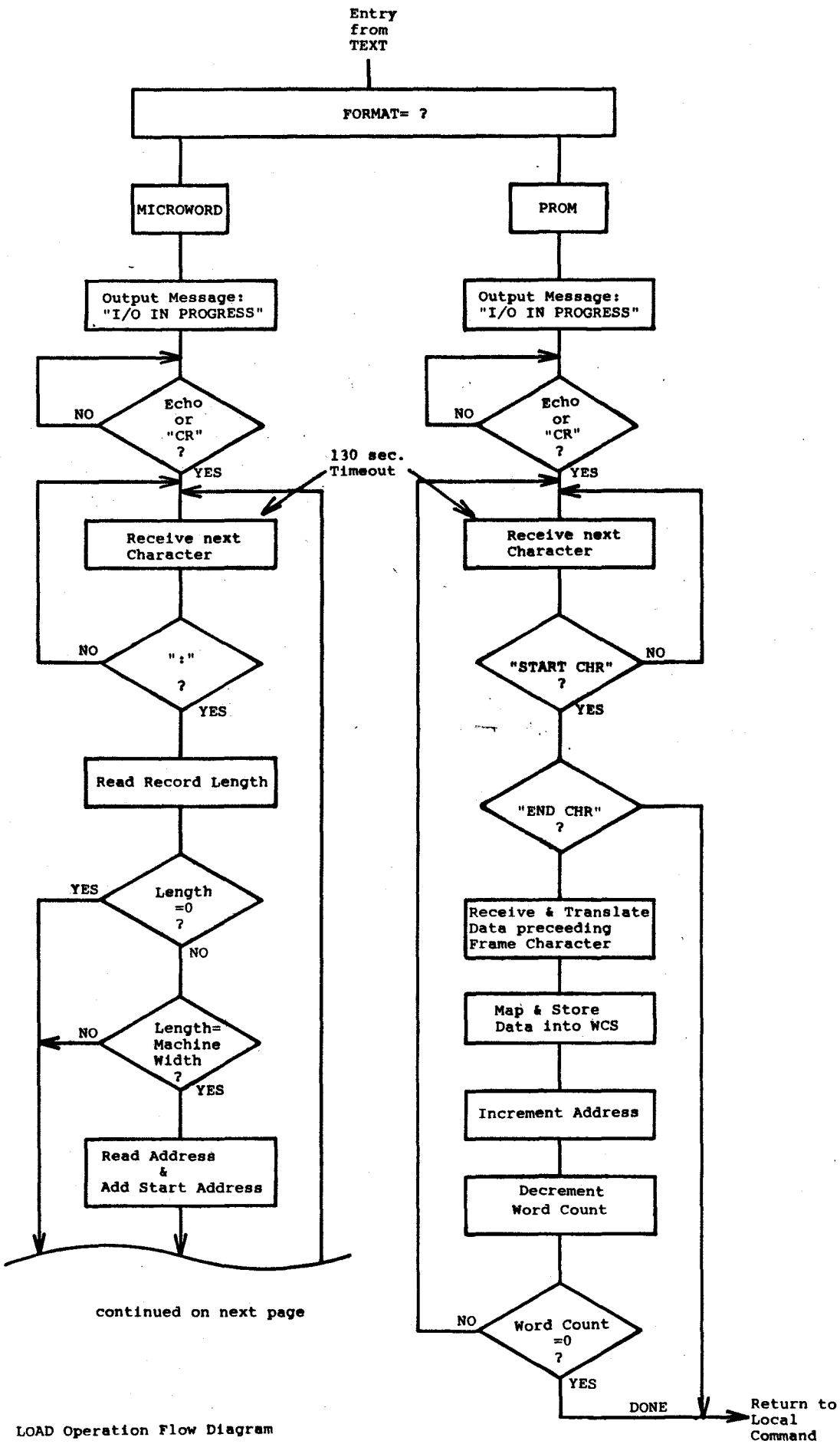
1) WORD limit is encountered as specified by the number-of-locations parameter.
2) An end of record character is encountered in MICROWORD format.
3) An end of record character is encountered in PROM formats.
4) An error such as checksum error, address limit, or character-type error is encountered.
5) A key is depressed by the operator to interrupt the process.
6) A compare error is encountered during operation of a compare operation.

Figure 2.5.2 is a flow diagram illustrating the main flow sequence for the LOAD operation. The compare operation is the same as load except that the data is reviewed rather than stored. The COMPARE command is used primarily to confirm the accuracy of an input or output operation.

After a LOAD operation, the compare operation tests WCS data against the external source data and displays the address of the last correct location when an error is encountered.

2.5.4 LOAD AND COMPARE COMMANDS: INPUTS TO STEP-N

Following a DUMP operation, a COMPARE operation will confirm that data received by the external machine is an identical copy of the data in WCS memory.



continued on next page

Fig. 2.5.2, LOAD Operation Flow Diagram

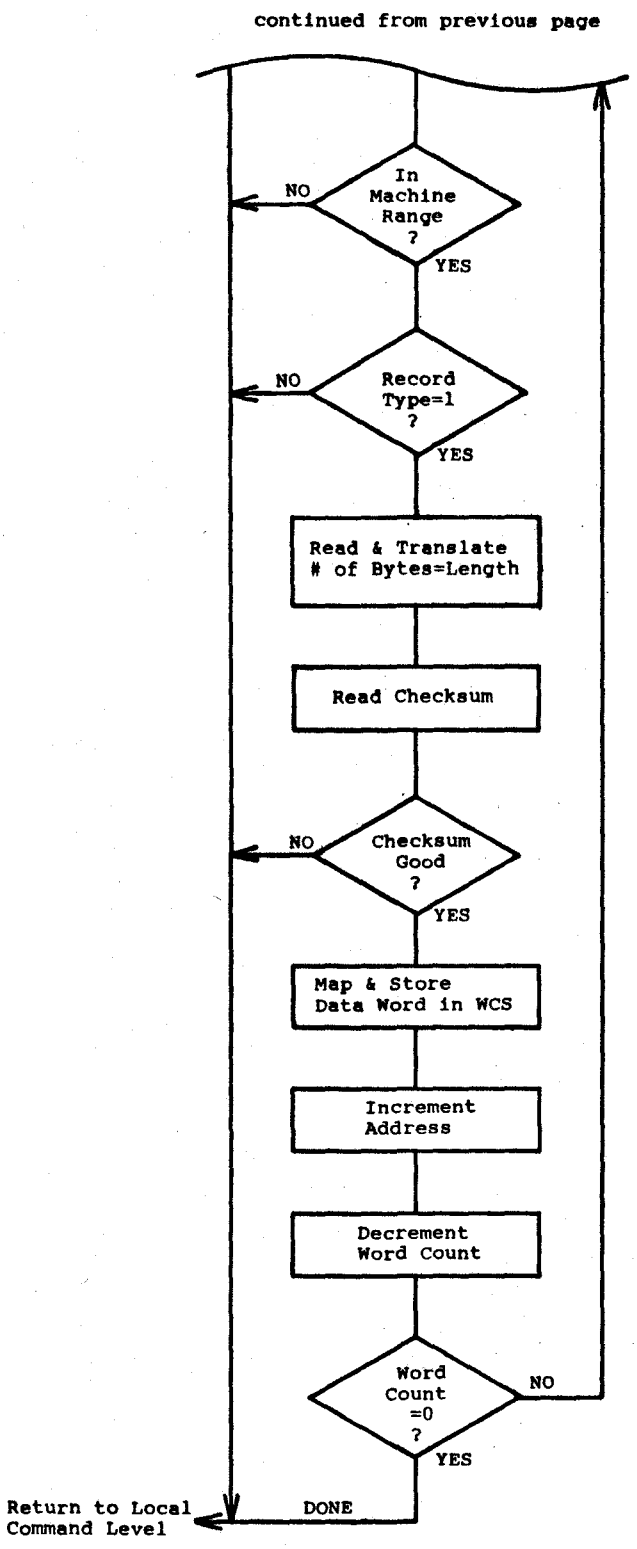


Fig. 2.5.2, (cont.) LOAD Operation Flow Diagram

2.5.5 DUMP AND PUNCH COMMANDS: OUTPUTS FROM STEP-N

DUMP (CR)
PUNCH (CR)

Entry to DUMP and PUNCH commands may be from either TOP command level or I/O subcommand level as illustrated in Figure 2.5.1. To perform an output operation, the command sequence proceeds essentially the same as for the input operations described above, with the exception of process synchronization.

Following the final (CR) on exit from TEXT, the output routines wait for echo of a (CR) from the host before proceeding with data transfers. This provision allows the peripheral to initiate the transfer when it is ready to receive data.

For passive peripherals which do not echo, a keyhit of the "C" key will cause the DUMP or PUNCH output operation to Continue. After the process is initiated, the message "I/O IN PROGRESS" is displayed on the CRT. Figure 2.5.3 is a flow diagram of the DUMP command.

The PUNCH command* is restricted to output operation utilizing device 0 or device 4 and BNPF format (2). Operation proceeds to dump BNPF data, following a pause to wait for the operator to enable the punch device.

2.5.6 FEATURES OF THE STEP ENGINEERING FORMATS

STEP-N offers the choice of MICROWORD,™ GENPROM,™ BNPF and ASCII-HEX-SPACE formats. So does each of the software packages offered by Step Engineering.

*STEP-2 only.

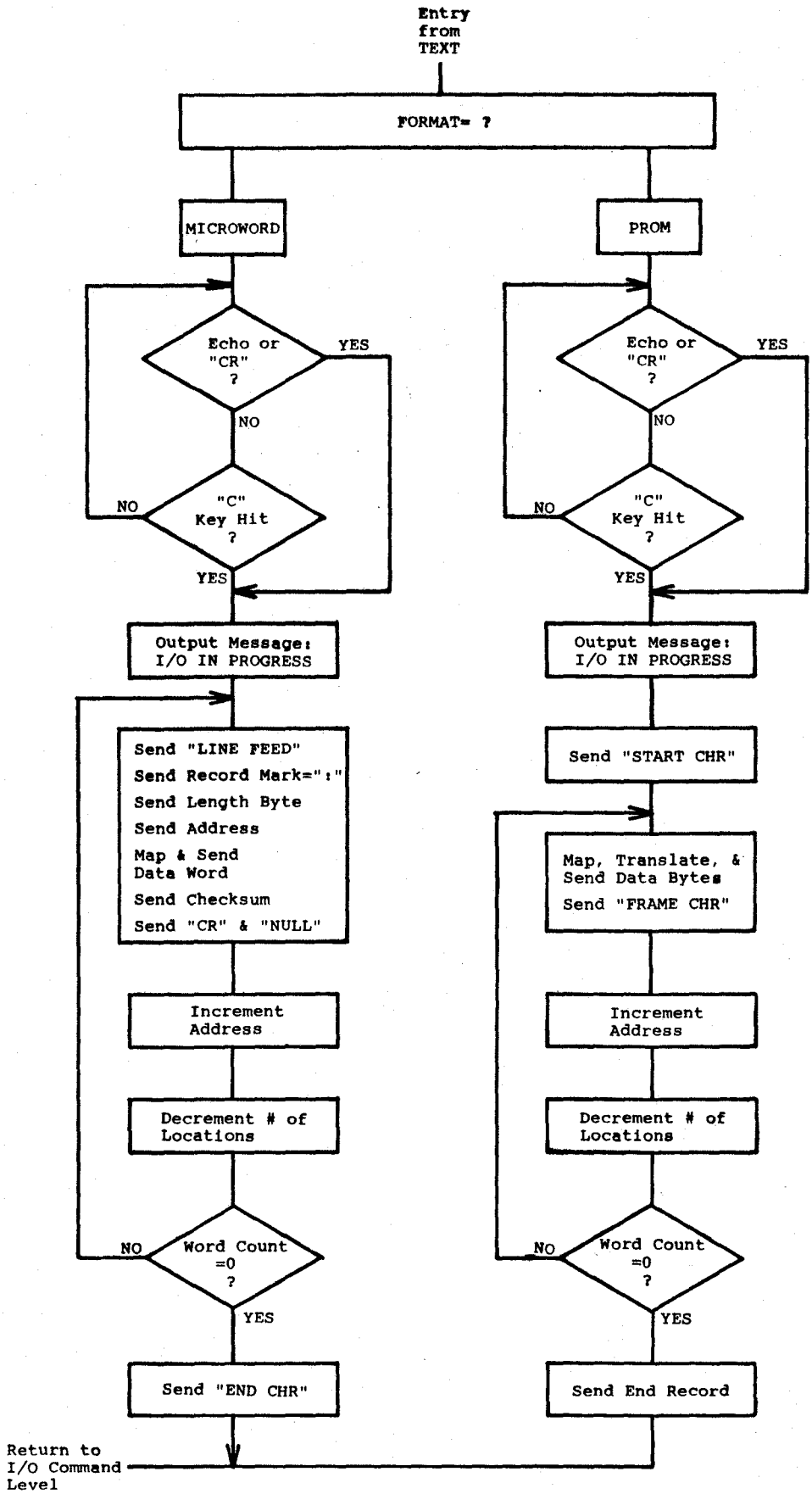


Fig. 2.5.3, DUMP Operation Flow Diagram

2.5.6 FEATURES OF THE STEP ENGINEERING FORMATS

TMA and MACRO-TMA are meta-assembler programs written in FORTRAN, host-resident, and compatible with many host computers. Their Phase-3 outputs include MICROWORD™, GENPROM™, BNPF, and ASCII-HEX-SPACE as alternate choices.

The MICROWORD™ format is a hexadecimal format utilizing a modified memory image technique. Data is blocked into discrete records with length equal to one microcode WORD. WORD is defined to be one user memory location and may be from 8 to 96 bits in width. Each record contains record length, address, record type, and a trailing checksum.

Use of the MICROWORD format provides several advantages for I/O operations. An entire control store may be transferred in a single operation, whereas PROM-image transfer would require several LOADS or DUMPS. Partial files (where only a few lines are modified) may be reassembled or easily downloaded since each record corresponds directly with one microinstruction, and carries a load address. Also, enhanced error checking capability is included in the data stream.

If existing special purpose software bases or older metassemblers do not provide a built-in MICROWORD compatible output, a small post processor program may be added to provide a MICROWORD OUTPUT file. Use of this standard is highly recommended to new users.

The GENPROM™ format is a hexadecimal format utilizing a PROM image technique whereby data is transferred a PROM at a time. Data consists of eight-bit bytes recorded as pairs of hexadecimal characters

2.5.6 FEATURES OF THE STEP ENGINEERING FORMATS

(0-9, A-F). Each pair of hex characters must be immediately followed by an ASCII framing character. Other control characters, such as line feeds and carriage returns, may be included in the data stream as long as the two hex data digits directly precede a framing character.

A start code character designated HEADER CHR procedes the start of the data stream and an end code designated END CHR signals the end of the data stream. All valid data is sandwiched between the HEADER CHR and ENDCHR.

Use of the GENPROM ™ format provides several advantages for I/O operation, compared to BNPF and to ASCII-HEX-SPACE, of which GENPROM ™ is a superset. The GENPROM™ format may be used for a generalized data interface to a wide variety of PROM programmers and existing software bases. Older Meta Assemblers usually generate some type of PROM-image output utilizing various start characters, frame characters, and end chrs. Since the GENPROM ™ format utilized in STEP-N is completely generalized, the great majority of these devices are accommodated. Where constants PROMS are being simulated, this format is particularly convenient. The major disadvantage of any PROM-oriented format is that the user must keep track of the mapping of microinstructions, into appropriate PROM locations in the hardware PROMS. Also, PROM-oriented formats require the user to perform multiple operations to input or output a single control store memory array.

2.5.7 TEXT COMMAND

TEXT (CR)

Entry to the TEXT command normally proceeds from I/O subcommand level. TEXT may also be entered from TOP command level and exited by depressing the shift key then Ø (top row in the alphanumeric portion of the keyboard)* which essentially provides an escape from TEXT.

However, when entry to TEXT from top command level is being employed, it should be remembered that baud rate, stop bit, and parity communication parameters must be set once in conjunction with an I/O command, or they'll remain at the default values. Normal exit from TEXT is accomplished at the first (CR) following depression of C & H (Clear and Home)**.

During execution of TEXT, the STEP-N instrument becomes a video terminal. Characters entered on the STEP ASCII keyboard are transmitted to a host machine or other device, over the specified RS232 or 20 ma port. Characters echoed are displayed on the CRT. The instrument displays 7 bit ASCII characters received as 64 character ASCII. Control characters are ignored and not displayed. The port requires 7 bit/char. ASCII, one or two stop bits, and parity is ignored. Transmitted characters are sent with the parity bit set to one, zero, EVEN or ODD as specified. STEP-3 has the full ASCII set of control characters, and STEP-2 can generate a limited set of control characters shown on the next page.

*Shift key then "V", bottom row, on STEP-2

**Home key on STEP-3.

2.5.7 TEXT COMMAND

SPECIAL CHARACTER	SHIFT CHARACTER	MEANING ASCII FUNCTION	LINK CHARACTERS HEXADEMIMAL
0	(V)	Reserved for Escape from TEXT	
1	(C & H)	DC1 or X-on	11 Control Q
2	(CLEAR)	DC2 or Tape Aux. on	12 Control R
3	(DEL)	DC3 or X-Off	13 Control S
4	(Z)	DC4 or Tape Aux. Off	14 Control T
5	(X)	SOH or SOM	01 Control A
6	(C)	EOT or EOT	04 Control D
7	(A)	ETX or EOM	03 Control C
8	(S)	CAN or SO	18 Control X
9	(D)	SUB or S2	1A Control Z
Blank	(B)	ESCAPE	1B Control
	( )	**BREAK	

The STEP-3 keyboard generates the standard 64 character, upper-case ASCII set. Five characters labeled on the keyboard are not part of the 64 character set. STEP-3 translates these by masking off the most significant bit. A translation table is shown below.

CHARACTER	DISPLAYED AS
! = 7C	< = 3C
{ = 7B	; = 3B
} = 7D	= = 3D
~ = 7E	> = 3E
' = 6I	@ = 2I

Also DEL = 7F not displayed.

**Generates a space on the port as long as key depressed when in TEXT command.

2.5.8 I/O COMMON PARAMETER SPECIFICATIONS

Following entry of LOAD, DUMP, COMPARE, or PUNCH* commands, the user is prompted to specify all required I/O parameters.

2.5.8.1 FORMAT

Current data format codes are:

FORMAT: 0 = STEP MICROWORD™ format.
1 = ASCII-HEX-SPACE (for use with device 3)
2 = BNPF (STEP-2 only)
3 = GENPROM™

Section 3.8 titled "STEP Standard Object File Formats" presents a detailed specification for each current object file format.

2.5.8.2 START ADDRESS

For all DUMP operations and LOAD operations in PROM formats, start address specifies the beginning address (in user memory space) of data to be dumped. The allowed range is: machine start address to memory limit. For LOAD operations, in STEP MICROWORD™ memory image format, the LOAD start address is treated as a bias offset. Since STEP-N files contain user memory addresses, treating the start address as a bias provides the capability to offset the load data in memory within available hardware limits.

*STEP-2 only.

2.5.8.3 DEVICE

Current allowed device codes are: (PORT 0, REMOTE ECHO)

DEVICE:	0 = 20 ma loop	(Port 0)
	1 = modem	(Port 1)
	2 = RS232 Link remote echo	(Port 2)
	*3 = DATA I/O Model	(Port 1)
	4 = TTY Local Echo	(Port 0)
	5 = RS232-C Local Echo	(Port 2)

NOTE: Format 3 may be utilized to communicate with PRO-LOG Model M-900-B PROM programmers at 300 baud utilizing device 1, 2, or 5.

All I/O communications with the STEP-N instrument is accomplished over one of three serial hardware ports utilizing ASCII standard codes. As defined, "device" refers to one of six sets of peripheral or host characteristics and assigns one of the three ports as the active communication port.

It should be noted that not all possible combinations of devices and formats are currently allowed. The brief matrix below summarizes the allowed I/O combinations:

DEVICE NUMBER	FORMAT 0	1	2	3
0	OK	NA***	OK **	OK
1	OK	NA***	NA	OK
2	OK	NA***	NA	OK
3	NA	OK *	NA	NA
4	OK	NA***	NA	OK
5	OK	NA***	NA	OK

OK = Allowed for LOAD, DUMP AND COMPARE.
NA = NOT ALLOWED

*DUMP only in compliance with Data I/O model 7 specs, STEP does not generate an initial (CR) on the Port as with other Devices. Instead, the initial protocol must come from the Data I/O end of the link.

**STEP-2 only, PUNCH command only.
***Hint: Use format 3.

2.5.8.4 WIDTH

Width is an optional parameter which is prompted only when PROM formats are specified. Valid parameters are 4 and 8, for 4 bit PROM data or 8 bit PROM data, respectively.

2.5.8.5 POSITION

Position is an optional parameter which is prompted only when PROM formats are specified. PROM image formats (GENPROM™) require a memory mapping consideration by the user, to specify which data from the memory array is intended for each particular PROM.

The convention employed in STEP-N instruments is that the least significant nibble of a location in user memory is position 0. For 8 bit PROM-data width, positions are labeled 0 - 11, proceeding to higher order bytes. For 4 bit PROM data, positions are labeled 0 - 23, proceeding to higher order nibbles.

2.5.9 I/O COMMON SUBCOMMANDS

Following entry of I/O parameters, the STEP INSTRUMENT remains at I/O command level. The current function being performed is displayed on the top display line and the user prompt on the command line (CRT line 3). The operator may take one of three paths:

1) subcommands to enter communication parameters OR I/O format parameters may be entered; or

2) The operation may enter subcommand QUIT, to abort the operation and return to top command level, or

3) The subcommand TEXT may be entered to continue an I/O operation, using the I/O port parameters already pre-set.

In the case of choice 1 above, the subcommands available are BAUD, STOP, PARITY, END CHR, HEADER, TRAILER, QUIT, and TEXT. Descriptions of each of these commands follows with exception of TEXT which is contained in 2.5.8.

2.5.9.1 BAUD

BAUD (CR)

One parameter is required which may be 110, 150, 300, 1200, 2400, 4800, or 9600. Execution following (CR) sets the baud rate on the serial ports and exits to I/O command level on completion. Default at power on is 110 baud for STEP-2, 1200 baud for STEP-3.

2.5.9.2 STOP

STOP (CR)

One parameter is required which may be either 1 or 2 stop bits. Execution following (CR) sets the serial port, then exits to I/O command level on completion. Default at power on is 2 stop bits in STEP-2, 1 in STEP-3.

2.5.9.3 PARITY

PARITY (CR)

One parameter is required which may be:

0 = set parity bit off always (stuck-at-zero)
1 = set parity bit to a 1 always (stuck-at-one)
2 = even parity
3 = odd parity

2.5.9.3 PARITY (CONTINUED)

Execution following (CR) sets parity error checking internal to STEP-2 and exits to the I/O command level on completion. Default at power on is "0" or parity bit off, stuck-at-zero.

2.5.9.4 EXAMINE PARAMETERS

XPARAM (CR)

Execution following (CR), displays a listing of which port is on, plus the defaults or pre-set values of BAUD rate, STOP BITS, PARITY, and GENPROM parameters. All of these parameters can be modified at I/O command level with the subcommands described below, then XPARAM can be re-executed for another examination, to make sure the port is set up correctly.

NOTE: Until the user knows the list, he uses the XPARAM menu as a reminder.

2.5.9.5 ENDCHR, HEADER, AND FRAMCHR

ENDCHR (CR), HEADER (CR), FRAMCHR (CR)

These subcommands are included for use with the STEP-N GENPROM ™ format to allow the user to specify a general PROM-at-a-time data stream in ANY of the ASCII HEX formats commonly in use.

The generalized load parameters in GENPROM™ format need only be set once following power on and are specified as two hexadecimal characters to provide complete generality.

2.5.9.5 ENDCHR, HEADER, AND FRAMCHR (CONTINUED)

Data in ASCII-HEX GENPROM ™ format consists of eight-bit bytes recorded as pairs of hexadecimal characters (0-9, A-F). Each pair of hex characters is immediately followed by another ASCII character which is the framing character. Extraneous ASCII or control characters, such as line feeds and carriage returns may be included in the data stream as long as the valid hex digits immediately preceed the frame character. When four-bit data is specified, only the single hex digit proceeding the frame character is considered valid data. For a more detailed specification see section 3.8 titled "STEP Object File Formats"

SECTION III

HARDWARE INTERCONNECT

3.1 WRITABLE CONTROL STORE MODULES

3.1.1 INTRODUCTION AND APPLICATION

Writable Control Store modules provide the capability to simulate all or part of the user's microcode/application memory in real time. The STEP-N instrument may contain one to five WCS modules with memory organizations from 8 to 96 bits per microword. Memory depths that vary from 1k to 40k are possible with various combinations of the STEP WCS modules, of the MEM-32 and MEM-128 families.

The total WCS module capacity may also be expanded to 10 modules by use of an expansion chassis option. Two independent stores (arrays) may be simulated at once.

The WCS modules are dual-port memories. One port is accessed via the chassis/backplane of STEP-N from the STEP microcomputer board to edit and manipulate data, and load and dump microprograms. This port of memory is called "slow speed", in that operations are performed at 8080A access rates.

The second port is a high-speed port and is accessed by the user's system, normally in a read-only mode. Current versions of MEM-32 and MEM-128 modules also allow write access to the WCS. Each WCS module has an internal real-time breakpoint which may be used to halt the users system or to trigger diagnostic instruments. The fact that a real-time breakpoint has occurred is reported to the user system by a real-time signal (BNC at 50Ω impedance) which remains true as long as the user's system address compare is valid or a minimum of 50 nsec.

3.1.1 INTRODUCTION AND APPLICATION (CONTINUED)

As mentioned previously, the STEP microcomputer interfaces to WCS boards are restricted to slow speed operations. Thus, the STEP microcomputer sets breakpoints and monitors status to be reported on the CRT display, but does not interact in any way in real time. The high speed hardware implementation of breakpoints and corresponding outputs provides for real-time simulation, and never depends on the STEP microcomputer to react in real time.

3.1.1.1 INTERFACING AREA

WCS data outputs and address inputs interface to the user system by way of the interface area on each WCS module. User interface flexibility is aided by socket options physically located next to the fast-port edge of the WCS, which is accessible thru the side of the STEP-N instrument. The interface area permits address inputs or data outputs to be swapped to allow for differences between wire wrap prototypes and final printed circuit layouts. Also, four different interface options are available for data termination allowing the designer an array of choices between latching and non-latching design approaches.

Either the factory or in the field, the standard INT-1 series termination resistors (mounted in SIPs, single in-line packs) can be unplugged and various octal buffers, latches or register IC's can be plugged in, in the same sockets. STEP provides these sockets and surrounds them with wire-wrap fields to give the user maximum convenience in adapting to new applications. Any SIPs or DIPs up to 20 pins can be used, and any pinout is acceptable, since all connections can be put thru a wire-wrap patch field.

3.1.1.1 INTERFACING AREA (CONTINUED)

WCS board-edge interface options include the standard INT-1 series termination for use with ROM simulation modules, buffered outputs with OR-tying capability, edge-triggered latching, and shine-through latching capability. For purposes of discussing memory organization, only the resistor termination INT-1 case will be described. Other interface options are described in the MEM-32 and MEM-128 data sheets.

Combinations of WCS, interface board and ROM simulation options provide the user great flexibility in test station setup. At one extreme the user may choose to simulate an entire array employing a single connector on his target processor while at the other extreme, all or part of a user array may be simulated employing ROM simulation options, STEP's ROM 4/8 cable sets. The following section describes addressing and data memory mapping from the user side of the WCS.

3.1.1.2 ADDRESS INPUTS

The user address signals are connected through standard edge connectors to P10 on each WCS module. When utilizing ROM simulation, these signals are interconnected to the user's target system through a ROM MASTER module and edge connector provided with the unit. (3M #3462-0001 or equivalent.) Detailed pinouts are presented for each WCS in the STEP data sheets (section 5). In systems with multiple WCS modules, address lines are bussed together within each independent array via a buss cable between the P10's of all WCS cards in the array.

3.1.1.3 DATA OUTPUTS

User data and chip enable signals are interconnected to the users data buss or memory array through standard edge connections (3M 3464-001 or equivalent) on P11 and P12 of each WCS. Each data connector contains 16 data bits, 2 enable outputs from STEP-N and 2 enable inputs from the user system. Data is right justified on the ports proceeding from bit 0 to bit 31. On systems employing wire tied options, data may be stacked on only one port and therefore require only one connection. The user side panel on STEP-N clearly labels data output LSB and MSB.

3.1.1.4 ENABLES AND MSB ADDRESS BITS

Each data port (that is, each 16-bit connector on the 32-bit wide WCS board) has 2 enable outputs and 2 enable inputs. The enable output signals are utilized with ROM-4 and ROM-8 simulation modules to enable memory access from the user system via user chip select or address lines.

For each WCS, there are 4 enable inputs (one per byte) which may be utilized as address bits A10-A13 for vertically organized memories or as chip enables from the user memory array. The ROM-4 and ROM-8 modules may be supplied with an outboard clip to provide a convenient means for the user to interconnect the required signal for his application. Enable outputs are connected on pin 17 or 37 of P11 and P12 and low true enable input signals on pins 19 and 39.

3.1.1.5 DATA MAPPING

Each WCS module may be reconfigured in width and depth. Each MEM-32 WCS module may be configured as 1k x 32, 2k x 16, or 4k x 8. Each MEM-128 WCS module can be configured 4k x 32 or 8k x 16.

A set of organization switches are located on the WCS board edge and are easily accessible from the user side panel on STEP-N.

Data Mapping is most readily understood by considering data organization within a single control store and then proceeding to multiple control store organizations. Within an individual WCS data is organized as 8 bit or 16 bit building blocks with each WCS divided into 1k sections (or 4k sections in the case of MEM-128.) Each section is thus either 1k x 8 (MEM-32) or 4k x 8 (MEM-128).

A set of organization switches are located on the WCS board edge and are easily accessible from the user side panel on STEP-N. Switch settings for different WCS organizations are given in section 3.1.2. Data mapping within each WCS module is shown in figure 3.1.2 for the MEM-32 WCS module. For purposes of uniformity, the following convention has been adopted:

CONVENTION: *Data words are considered to be made up of 8 bit bytes with the lowest order byte as the least significant, labeled Byte 0. Data bits within a byte are labeled as D0 → D7, with the least significant bit labeled D0. Thus, a 96 bit word will consist of 12 bytes and a particular bit may be referenced by bit number (bit 56) or by byte number and the bit number within the referenced byte.*

3.1.1.5 DATA MAPPING (CONTINUED)

Each data byte on either port P11 or P12 has associated with it an enable bit input which is interpreted by the STEP-N instrument in calculating user addresses. For a particular WCS module to have a valid address, the enable signals must be true in a pattern consistant with the module memory organization. If this is not true, the STEP-2 display will display ADDRESS=NONE when RUNNING or single Step routines are entered.

The valid enable bit patterns for each module are illustrated in Charts 4-6 at the end of section 3.1.2. As can be seen from the tables, the enable bit patterns correspond exactly to the chip selects of a typical user memory array.

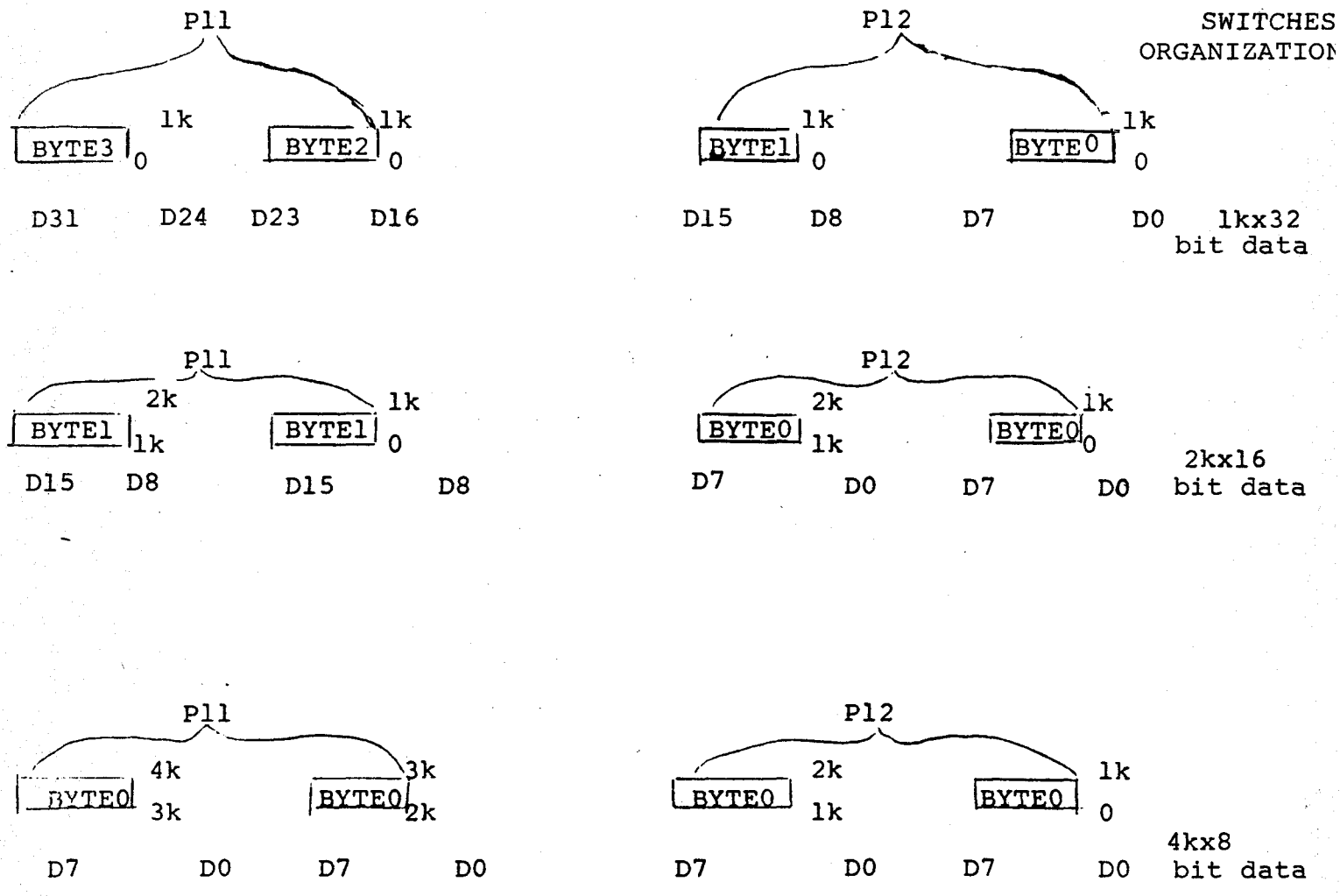


Figure 3.1.2 Data Mapping Within Each WCS module for 3 Switch Settings

3.1.1.5 DATA MAPPING

When using STEP ROM simulation, the ROM chip enables are buffered and interconnected directly to the STEP-N data ports and are transparent to the user. Section 3.3 deals with direct cable hookups designed by the user.

3.1.1.6 MEMORY ARRAY ORGANIZATIONS

Multiple WCS modules may be configured in a maximum of 2 independent arrays. Each array is totally independent (in access rate, address space, etc.) and may be expanded in both width and depth. Working with data words up to 192 bits may be accomplished by concatenating the two arrays.* Width may be added in 4 bit increments from 8 bits to 96 bits. Depth may be added in 1k or 4k increments from 1 to 48k. Within each independent array, WCS organization switches must be set the same and WCS modules must be of the same type.

Within these few constraints, the user may readily configure the STEP-N instrument for multiprocessor applications or utilize one array for microcode and the other array for application programs. The boundary organization, or max configurations, which may be configured with MEM-32 WCS modules are illrstrated in Figure 3.1.5; MEM-128 boundries are shown in Figure 3.1.6. It should be noted that when the user specifies word widths which are less than the WCS board width, the data in WCS are right justified; i.e. the MSB's of the relevant WCS are unused when the machine word width is less than an organization boundary. For example, a 28 bit word width specified on a single WCS

*However, it should be noted that functions such as FORCE and JAM are restricted to 96 bits without special considerations.

module would not utilize the 4 most significant bits of the WCS and the display would start with bit 27 in the MSB position. Similarly for a 60-bit word on two WCS modules.

MEM-32 Modules

HARDWARE SWITCHES	WIDTH	DEPTH	SLOTS
1kx32	8-32	1k	1
	8-32	2k*	2
	8-32	3k	3
	8-32	4k*	4
	8-32	5k	5
	8-32	6k*	6
	36-64	1k	2
	36-64	2k	4
	36-64	3k	6
	68-96	1k	3
	68-96	2k	6
2kx16	8-16	2k	1
	8-16	4k	2
	8-16	6k	3
	8-16	8k	4
	8-16	10k	5
	8-16	12k	6
	20-32	2k*	2
	20-32	4k*	4
	20-32	6k*	6
	36-48	2k	3
	36-48	4k	6

Figure 3.1.5 Boundry Organizations for Multiple MEM-32 Arrays

HARDWARE SWITCHES	WIDTH	DEPTH	SLOTS
	8	4	1
	8	8	2
	8	12	3
	8	16	4
	8	20	5
	8	24	6
	12-16	4	2
	12-16	8	4
	12-16	12	6
	20-24	4k	3
	20-24	8k	6

*Card 2 is address range 1-2k etc.

Figure 3.1.5 Boundary Organizations for Multiple MEM-32 Arrays.

MEM 128 Modules

	WIDTH	DEPTH	SLOTS
32 Bit Switches	8-32	4k	1
	8-32	8k	2
	8-32	12k	3
	8-32	16k	4
	8-32	20K	5
	8-32	24k	6
	36-64	4k	2
	36-64	8k	4
	36-64	12k	6
	68-96	4k	3
	68-96	8k	6
16 Bit Switches	8-16	8k	1
	8-16	16k	2
	8-16	24k	3
	8-16	32k	4
	8-16	40k	5
	8-16	48k	6
	20-32	8k	2
	20-32	16k	4
	20-32	24k	6
	36-48	8k	3
	36-48	16k	6

Figure 3.1.6 Boundary Organizations for Multiple MEM-128 configurations.

3.1.1.7 WCS MODULE ASSIGNMENT

Execution of the SETUP command assigns STEP WCS memory to the user system. The general rule employed in the STEP firmware is to assign WCS modules to add data width first and memory depth second. The three boundary organization switch specifications define maximum data word width per WCS memory module. The user target system must supply the address bits and enable bits to access the WCS data. Address bits are independent of the STEP memory configuration; however, enable bits are a function of memory configuration.

To interconnect to the user system address drivers, all WCS address inputs within an array are bussed together on port P10.
When the WCS boards are used as 8-bit or 16-bit building blocks, each WCS is divided into 1k sections (or 4k sections in the case of MEM-128). Each 1k section must be enabled by the user-supplied signal for data to be accessed properly. In systems employing ROM simulation, the interconnect of the enables and data lines is incorporated in ROM 4/8 modules; however, the data mapping given below should still be referenced for interconnecting data cables. The following paragraphs describe how data and enable signals appear at the user side panel. WCS modules slots are referenced as MEM-1, MEM-2, etc., proceeding to higher order modules. Bytes are referenced from byte 0 to byte 4, proceeding from least significant to most significant. Figure 3.1.3 illustrates the user interconnect arrangements for a three module system, configured as a 1k x 96 bit array, with 32 bit organization switches. As viewed from the user side panel, the data will appear mapped as shown in figure 3.1.4.

NOTE: Organizations less than full systems are a proper subset of the illustrations.

3.1.1.7 WCS MODULE ASSIGNMENT (CONTINUED)

For user convience Appendix B Tables B-1 thru B-9 specify graphically data mapping at the user interface for 32, 16 and 8 bit organization switch settings utilizing MEM-32 modules. Tables B-10 thru B-15 specify data mapping for 32 and 16 bit switch settings on MEM-128 WCS modules.

3.1.1.8 NON-ZERO-START ADDRESSING

Start addressing of the memory array from the user system is completely specified by user system hardware. The STEP-N start address may be set as a base address from 0000 to 7FFF (hex) programatically to correspond to user system address space. Once set, all STEP-N commands referencing user memory addresses utilize the new address space. The start address may also be employed to offset data loaded into the WCS modules that has been assembled in a different (now-wrong) address space.

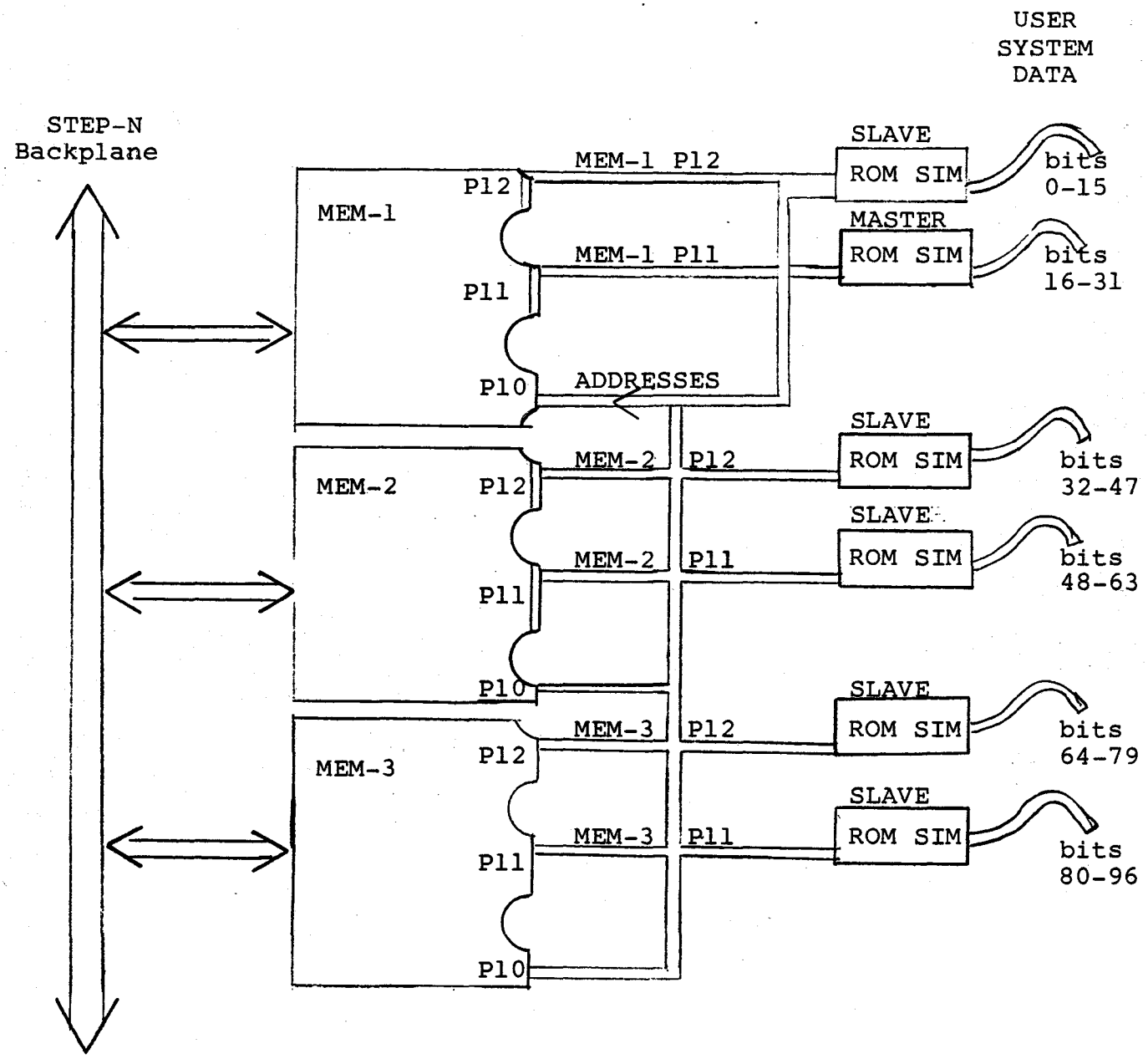


Figure 3.1.3a INTERCONNECT EXAMPLE WITH THREE MEM-32's ORGANIZED 1kx96.

WCS Boards are shown in top view, component sideup, unstacked, for clarity; edge tongues are numbered P10 (nearest keyboard) to P12 (rear of machine).

VIEW: Side view of STEP-N machine, showing 3 memory slots.

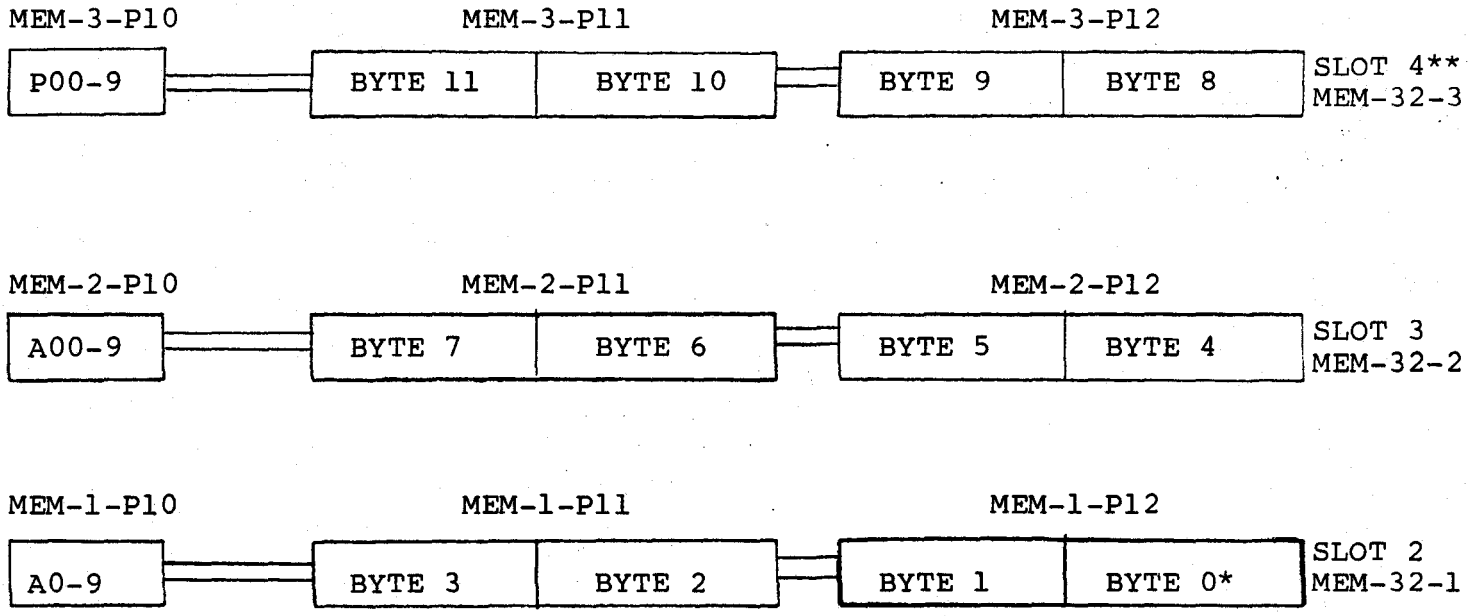


Figure 3.1.4 Data Mapping for MEM-32 WCS modules, organized 1kx96.

NOTE: *Each Data Byte has 1 associated enable input bit. For valid address reporting on the CRT, all enables must be satisfied.*

*Least-significant byte.

**Any three slots can be used, but preferably the lowest-numbered ones.

3.1.2.1 GENERAL

This operation description covers five memory systems. They are MEM-32A, MEM-32F, MEM-128A, MEM-128B, MEM-128F. These WCS units are asynchronous dual-port memory systems with internal trigger generation and address compare. They can be operated in a read/write or read-only mode. Access time, storage capability and organization is shown in Chart 1. MEM-32 boards are faster and less dense than MEM-128 boards.

All user connections are through the side connectors, switches and BNCs accessible through the side panel of Step-N. Address and breakpoint inputs connect to one tongue of the edge connector and output data is available on two other tongues. The real-time trigger output is available on BNC2*(labled "BKPT" on the side panel). BNC1*(labled "SMPL" on the side panel) serves as the input for the user WRITE signal.

*Viewed from the right side of the STEP instrument, BNC-1 is on the left, nearer the keyboard. All STEP boards are used component side up.

3.1.2.2 SWITCH SETTINGS

Memory operation is controlled through the six * switches located between BNC 1 and BNC 2. These switches have the following function:

Switch	Position	Function	
		MEM 32	MEM 128
S1	On ↑	Enables external write operation for the entire memory	Enables external write operation for the upper 4Kx16 bits (8Kx16org) or bits 8-15, and 24-31 (4Kx32 org)
	Off ↓	Disables external write operation	Disables external write operation described
S2	On ↑	Selects either 2Kx16 or 1Kx32 operation	Enables external write operation for the lower 4Kx16 bits (8Kx16 org) or bits 0-7, 16-32 (4Kx32 org)
	Off ↓	Selects 4Kx8 operation (note S3 must be on)	Disables external write operation described above
S3	On ↑	Selects 1Kx32 or 4Kx8 organization (dependent on S2)	Selects 4Kx32 organization
	Off ↓	Selects 2Kx16 organization (note S2 must be ON)	Selects 8Kx16 organization

*The earliest WCS boards from STEP (MEM-32 two-piece boards, dating from before MEM-32A) had 4 switches. See appendix F.

3.1.2.2 SWITCH SETTINGS (CONTINUED)

S4	On	Sets breakpoint enable to be level sensitive
	Off	Sets breakpoint enable to be edge sensitive
S5	Off	Sets breakpoint enable to be positive true
	On	Sets breakpoint enable to be negative true
S6	On	Step-N controls user access to memory board
	Off	Memory board dedicated to target processor, board-edge is always enabled.

The normal switch settings are:

MEM 32A/F: S1-OFF; S2, S3, S4, S5, S6-ON

MEM128 all: S1, S2 OFF; S3, S4, S5, S6-ON

3.1.2.3 MEMORY ACCESS

Each memory board is a dual port memory, one port tied to the internal Step-N microprocessor bus, and the other port connected to the target processor. Only one port can be active at a time. Under normal Step-N control, the memory is available to the target system when in MONITOR mode after "RUN" has been initiated. It remains available to the target processor until MONITOR is exited. However, if S6 is in the "OFF" position, the memory is available to the target processor regardless of the command input to STEP-N and STEP-N can not read or write the memory. This feature is useful in dual processor systems where it is desired that one processor remain operating while the second is being modified.

3.1.2.4 READ/WRITE OPERATION

For normal read only operation S1 (MEM-128 and MEM-32) and S2 (MEM-128 only) should be off. When using the memory in a read/write mode from the target processor S1 and S2 must be set to the proper position as shown in Chart 3.* To initiate a Write operation a low true signal should be applied to BNC1 and data to be written placed on the data tongues.

3.1.2.5 ADDRESS INPUT/DISPLAY

P10 is used for address and breakpoint enable input. The following pin assignments apply:

BKPT	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
25	23	21	19	17	15	13	11	9	7	5	3	1

Even-number pins are at ground level and are located on the bottom side of the board. Pin 1 is the top right pin on the connector.

The BKPT input serves multiple functions.

It is used as part of the address compare circuitry (as described under "TRIGGER").

It is used as the clock input to the latch/register output drivers when installed in place of the series resistive terminations normally supplied. When latches are used (part 74S373) a positive BKPT signal allows

*Charts are located at the end of section 3.1.2.9.

data to pass through the latches unaltered. A negative signal causes the last data output to be latched. When registers are used (part 74S374) a positive edge of the BKPT signal results in the output being set to the logic states that were setup at the input to the register. (Called "User Latch".)

It is used as an input to the address latch as part of the address display circuitry. This circuitry works as follows:

The Step-N CPU sends out a signal which on all memory boards latches the current address and enable inputs. It also sets a flip-flop which is ANDed with the BRKT signal to latch the current address. If a BRKT signal occurs within ten microseconds (10 usec) of the CPU signal, new address and enable information is latched synchronously with respect to the BRKT signal. This signal also resets the flip-flop. This would normally occur if the target processor were in a run state and the BKPT signal were attached to the target clock. If the target processor is single stepping or no clock signal were present on BKPT the original latched information would remain in the register. The Step-N CPU then reads the address display register on all memory boards and displays on the CRT the first one containing the proper enable input EI pattern for the

chosen memory organization. If the correct enable pattern is not found, "ADDRESS=NONE" is displayed. The CRT display is updated twice a second.

3.1.2.6 TRIGGER OUTPUT

The trigger (breakpoint) output is available approximately 60 nanoseconds after a matching address and enable is present on P10. When S4 is "ON" the trigger signal is available for the length of time that the address compare is valid. When S4 is "OFF" the trigger signal is available for approximately 50 ns.

The breakpoint enable line is present on the same input (P10) tongue as the address lines. Whenever this line is true state or the proper signal transition occurs as defined by S4 and S5, the breakpoint compare circuitry is enabled. When using ROM Simulation modules, the green clip on the Master module serves as the input. This input is used to insure that the address lines are valid when the address compare is made. By leaving the breakpoint enable (Pin 25) open, and setting S4 and S5 "ON", the address compare is always enabled. The output signal is positive true and can be used to drive 50 ohm terminated lines.

3.1.2.7 DATA OUTPUT

P11 and P12 are used for data output. The following pin assignments apply:

3.1.2.7 DATA OUTPUT (CONTINUED)

The even numbered pins are grounded and are located on the bottom sides of the board. Pin 1 is the top right hand pin on the connector. In order to insure proper address readout on the CRT the enable input lines, EI, must be low for the 32 bit organization (MEM-128 and MEM-32) when the memory is enabled. For the 16 bit case (MEM-128 & MEM-32), EI1 and EI3 or EI2 and EI4 must be low for the memory to be enabled. For the 8 bit use (MEM-32) one of the EI lines must be low for the memory to be enabled.

3.1.2.8 DATA OUTPUT CONFIGURATION

The standard MEM-128 A/B/F and MEM-32 A & F boards are shipped with resistive series termination on the data output lines. These are placed in 20 pin IC sockets and can be replaced by a variety of integrated circuits to achieve a special interface. Latches and registers (TI types 74S373 and 74S374) as well as buffers (TI types 74S240, 74S241 and 74S244) can be used. A small wirewrap area allows wiring to be modified to match the desired IC or to permit bit mapping (re-pinout of edge-connectors).

3.1.2.9 DIRECT MEMORY INTERCONNECTION

The memory boards can be connected to the target processor in one of two methods using the optional ROM Simulator Assemblies (covered next section) or directly with the ribbon cable provided. When using

ribbon cable, care should be taken to insure that the Enable Input (EI) lines mentioned in section 3.1.2.7, re Data Output, are properly connected. If not connected properly either "ADDRESS=NONE" or an invalid address will appear on the CRT. These lines can be grounded, connected to the Enable Out (EO) lines or connected to address decoders depending on the memory organization. The EO lines are negative true outputs which go to the true state (low) whenever the memory is available for access by the target processor. One use of these lines is to disable ROM program store during testing when Step-2 is attached and active. Chart 4&5 shows the proper state of the EI lines for various memory organizations. Section 3.3 gives more guidelines for Direct Memory Interconnect.

SUMMARY OF
MEMORY OPERATION

3.1.2.10

Chart 1

Board type	Storage	Organization	Access time[1]
MEM-32A	32K bits	4Kx8, 2Kx16, 1Kx32	45ns*
MEM-128A	128K bits	8Kx16, 4Kx32	70ns**
MEM-128B	128K bits	8Kx16, 4Kx32	180ns

Note 1: Access time is the worst case access time measured from P10 (Address Input) to P11 or P12 (Data Output) assuming series resistive terminations. Cables add to these times.

Chart 2

MEM-32			MEM-128	
S2	S3	ORG	S3	ORG
On	On	1Kx32	On	4Kx32
On	Off	2Kx16	Off	8Kx16
Off	On	4Kx8		
Off	Off	Illegal		

Chart 3

Read/Write Operation

MEM-32		MEM-128		Organization	
S1	Operation	S1	S2	8Kx16	4kx32
On	Read/Write	On	On	Read/Write	R/W all
Off	Read Only	On	Off	4-8K R/W	8-15bits & 24-31,R/W
		Off	On	0-4K R/W	0-7bits & 16-23,R/W
		Off	Off	Read Only	Read Only

*MEM-32F is identical, but 36ns, worst-case.

**MEM-128F is identical, but 50ns, worst case.

Chart 4

MEM-32

ENABLE INPUT

Address Range	Mem Bd Org	Mem Org	$\overline{EI3}$	$\overline{EI2}$	$\overline{EI1}$	$\overline{EI0}$	Comment
			1	1	1	1	Board not selected
0-1K	1Kx32	1KxN	0	0	0	0	Valid memory address
0-NK	1Kx32	NKxM	0	0	0	0	The memory board or boards with "O" EI will indicate selected address space. Example, in a 2Kx64 organization "O" EI on MEM 1&2 indicate address 0-1K, "O" EI on MEM 3&4 indicate address 1-2K
0-2K	2Kx16	2KxN	1	0	1	0	Address 0-1K
0-2K	2Kx16	2KxN	0	1	0	1	Address 1-2K
0-NK	2Kx16	NKxM	1	0	1	0	Memory address RK +0 RK +1 Memory address RK+1 to RK+2 Actual memory address depends on selected boards Example: 4Kx16 organization If MEM32-1 EI="A" hex, address range 0-1K EI=5 hex, address range 1-2K. If MEM 32-1 EI="F" hex and MEM 32-2 EI="A" hex, address range = 2-3K etc.

0-4K	4Kx8	4KxN	1	1	1	0	Memory address=0-1K
			1	1	0	1	Memory address=1-2K
			1	0	1	1	Memory address=2-3K
			0	1	1	1	Memory address=3-4K

Chart 5

MEM-128

ENABLE INPUT

Address Range	Mem Bd Org	Mem Org	$\overline{EI3}$	$\overline{EI2}$	$\overline{EI1}$	$\overline{EI0}$	Comment
-	-	-	1	1	1	1	Board not selected
0-4K	4Kx32	4KxN	0	0	0	0	Valid memory address
0-NK	4Kx32	NKxM	0	0	0	0	The memory board or boards with "0" EI will indicate selected address space. Example, in a 8Kx64 organization "0" EI on MEM 1&2 indicate address 0-4K a "0" EI on MEM 3&4 indicate address 4-8K
0-8K	8Kx16	8KxN	1	0	1	0	Address 0-4K
0-8K	8Kx16	8KxN	0	1	0	1	Address 4-8K
0-NK	8Kx16	NKxM	1	0	1	0	Memory address RK +0 RK +1
			0	1	0	1	Memory address RK+1 to RK+2 Actual memory address depends on selected boards) Example: 16Kx16 organization. If MEM32-1 EI="A" hex, address range 0-4K EI=5 hex, address range 4-8K. If MEM32-1 EI="F" hex and MEM32-2 EI="A" hex, address range=8-12K etc.

CHART 6

MEM-128 A & B DATA MAPPING

ORGANIZATION	8kx16		4kx32			8kx16		4kx32	
PIN #	P11	P12	P11	P12	PIN #	P11	P12	P11	P12
1	D8	D0	D16	D0	21	D8	D0	D24	D8
3	D9	D1	D17	D1	23	D9	D1	D25	D9
5	D10	D2	D18	D2	25	D10	D2	D26	D10
7	D11	D3	D19	D3	27	D11	D3	D27	D11
9	D12	D4	D20	D4	29	D12	D4	D28	D12
11	D13	D5	D21	D5	31	D13	D5	D29	D13
13	D14	D6	D22	D6	33	D14	D6	D30	D14
15	D15	D7	D23	D7	35	D15	D7	D31	D15
17	$\overline{EO2}$	$\overline{EO0}$	$\overline{EO2}$	$\overline{EO0}$	37	$\overline{EO3}$	$\overline{EO1}$	$\overline{EO3}$	$\overline{EO1}$
19	$\overline{EI2}$	$\overline{EI0}$	$\overline{EI2}$	$\overline{EI0}$	39	$\overline{EI3}$	$\overline{EI1}$	$\overline{EI3}$	$\overline{EI1}$
Address Range	0-4k		0-4k			4k-8k		0-4k	

MEM-32A DATA MAPPING

ORGANIZATION	4Kx8		2Kx16		1Kx32	
PIN #	P11	P12	P11	P12	P11	P12
1	DO	DO	D8	D0	D16	D0
3	D1	D1	D9	D1	D17	D1
5	D2	D2	D10	D2	D18	D2
7	D3	D3	D11	D3	D19	D3
9	D4	D4	D12	D4	D20	D4
11	D5	D5	D13	D5	D21	D5
13	D6	D6	D14	D6	D22	D6
15	D7	D7	D15	D7	D23	D7
17	$\overline{EO2}$	$\overline{EO0}$	$\overline{EO2}$	$\overline{EO0}$	$\overline{EO2}$	$\overline{EO0}$
19	$\overline{EI2}$	$\overline{EI0}$	$\overline{EI2}$	$\overline{EI0}$	$\overline{EI2}$	$\overline{EI0}$
ADDRESS RANGE	2-3K	0-1K	0-1K		0-1K	

ORGANIZATION	4Kx8		2Kx16		1Kx32	
PIN #	P11	P12	P11	P12	P11	P12
21	D0	D0	D8	D0	D24	D8
23	D1	D1	D9	D1	D25	D9
25	D2	D2	D10	D2	D26	D10
27	D3	D3	D11	D3	D27	D11
29	D4	D4	D12	D4	D28	D12
31	D5	D5	D13	D5	D29	D13
33	D6	D6	D14	D6	D30	D14
35	D7	D7	D15	D7	D31	D15
37	$\overline{EO3}$	$\overline{EO1}$	$\overline{EO3}$	$\overline{EO1}$	$\overline{EO3}$	$\overline{EO1}$
39	$\overline{EI3}$	$\overline{EI1}$	$\overline{EI3}$	$\overline{EI1}$	$\overline{EI3}$	$\overline{EI1}$
ADDRESS RANGE	3-4K	1-2K	1-2K		0-1K	

NOTE: Here, the same pins are renamed for their bit position in the target data word.

Some may find the STEP data book explanation helpful also. There, the pins are not renamed with changes in organization. The STEP data book is Appendix A, Section 6 of this manual.

3.2 ROM SIMULATION CABLE SETS

3.2.1 GENERAL

The ROM Simulation modules serve as a way to attach the MEM-128 and MEM-32 memory boards to the target processor. They connect to the edge connectors of the memory board and plug into the PROM sockets of the target processor. They enable rapid system hookup, and provide an excellent way of interconnecting high speed memory signals without distortion, reflections, or crosstalk.

Two basic types of ROM Simulation modules exist, Masters and Slaves. The Masters have address information which connects via a separate cable to the memory boards. Both the Masters and Slaves have data outputs and chip select inputs. Data is buffered by active devices within the modules. Power for these devices come from PROM sockets.

The ROM Simulation modules need not plug into all ROM sockets to simulate two or more ROMs wired-ORed together to obtain a greater memory depth. This ability increases interconnect reliability.

3.2.2 ADDRESSING, WITH EXAMPLES

For each memory array, the address bus is picked up from only one ROM socket. The ROM module having address interconnect circuitry is called the Master ROM module. Where more than three memory boards exist in a system, an additional Master module needs to be used. Memory access time increases by approximately 2 nanoseconds per board for

each board above two. Address information is transmitted from the Master module to the memory boards across ribbon cable arranged signal-ground, signal-ground configuration. The cable has a dynamic impedance of 100 ohms. It is series terminated within the Master module to damp excessive line reflections. Both memory and trace boards have high input impedance buffers minimizing DC loading problems. The effects of cable loading are roughly equivalent to the capacitive loading found in a PROM array and no signal drivers or precaution need be used.

One of three types of memory addressing schemes can be used, depending on user memory/PROM configuration. Examples of each configuration are shown at the end of the section.

CONFIGURATION 1

User Memory Depth and ROM Depth equals 1k (MEM-32) or 4k (MEM-128).

CONFIGURATION 2

User Memory Depth equals 1k (MEM-32) or 4k (MEM-128). User Prom depth is less than user memory depth.
In this case, one ROM simulation module replaces two or more PROMS in a wired-ORed configuration. The Master ROM Simulation module contains additional MSB memory address inputs. These inputs are generally in the form of external grabbers*, but can be wired in place of chip select inputs on the DIP plug in (at a customer's request).

*"GRABBERS" are springloaded micro-clips attached to the orange ROM simulation boxes.

When additional address inputs are present, chip select inputs must also be modified. The chip select inputs on the ROM Simulation modules can be disconnected by STEP Engineering or by the customer. When disconnected by STEP they are replaced by an external input on a grabber. As an alternative, chip select inputs can be modified on the target processor. The reason for modification is to insure that a valid address input will not produce a chip select signal which tristates the ROM Simulation module. This occurs when the module is plugged in place of a ROM whose socket is wired for a limited address range. Both chip select and address modifications are made at the time of order placement. Actual module pinout is shown on the attached label. Since the chip select inputs are wirewrapped within the module, they may be changed at any time by the user.

CONFIGURATION 3

User Memory depth is greater than 1k (MEM-32) or 4k (MEM-128) and equal to or greater than PROM depth.

Case 1 - PROM depth is 2k (MEM-32)
or 8k (MEM-128)

Step manufactures a number of ROM Simulation modules which contain internal multiplexers: ROM 8J, ROM 8K, ROM 8N, ROM 4E are examples. These modules take in two groups of eight data lines each and use the highest order address input to select the output group. The MEM-32 and MEM-128 boards have switch settings for this operation. Since the ROM Simulation module emulates the PROM it is replacing, multiplexing operation has no effect on performance although it may affect system interconnect (see next section). Where the memory is deeper than 2k (MEM-32) or 8k (MEM-128) ROM Simulation modules

replace PROMs on a one for one basis and would operate in a wired-ORed configuration.

Case 2 - PROM depth is 1k or under (MEM-32) or 4k or under (MEM-128)

In this case, the ROM modules would replace PROMs on a one for one basis and be wired-ORed. To minimize interconnect difficulties, it is recommended that the multiplexing ROM types mentioned im case 1 above be used in place of multiple wired-ORed PROMs. As in configuration 2, when this is done, chip select inputs must be customized.

The following examples illustrate some common configurations and the memory addressing schemes used.

Example 1 - MEMORY ARRAY: 1k X 64
ROM TYPE: 1k X 4 or 1k X 8

Plug into each ROM socket; chip enables and memory addressing behaves like ROM

Example 2 - MEMORY ARRAY: 512 X 64
ROM TYPE: 512 X 4, 512 X 8

Plug into all ROM sockets. Ground external address input A9 on grabber. Tie any external chip select inputs on grabber to chip select input on DIP plug. NOTE: if desired two sets of code can reside in STEP-2, one in the lower half of memory, one in the upper half A9 can be used to arm either set by grounding or tieing to Vcc.

Example 3 - MEMORY ARRAY: 1k X 64
ROM TYPE: 512 X 4 (ROM 4B)
512 X 8 (ROM 8F)

Plug into all ROM sockets with address space 0 - 511. Tie external address input A9 (in grabber) to A9 output on target processor. Ground external chip select input on grabber or tie to chip select output on target processor before it interacts with A9.

Example 4 - MEMORY ARRAY: 1k X 64
ROM TYPE: 512 X 8 ROM 8D, ROM 8E

Determine which chip select input is used to carry address information, disconnect it from A9 on target processor or in ROM Simulation modules. Plug into all ROM sockets with address space 0 - 511. Tie external address input A9 (on grabber) to A9 output on target processor, and tie to appropriate logic level.

Example 5 - MEMORY ARRAY: 2k X 32
ROM TYPE: 512 X 8

Determine which chip select signal is used to carry address information and disconnect it from A9 on target processor or in ROM Simulation modules and attach to the appropriate logic level. If a two to four decoder or three to eight decoder is used to decode address lines to chip selects, detach A9 from the decoder and ground that decoder input. Plug ROM Simulation modules across the full word width in address locations 0 - 511 and 1024- 1535. Attach external input A9 grabber to target processor.

Example 6 - MEMORY ARRAY: 2k X 32
ROM TYPE: 512 X 8
ROM SIMULATION TYPE: 2k X 8

Determine which chip select lines are used for A9 and A10 and disconnect them on the target processor or in the ROM module. If an address decoder (2 to 4 or 3 to 8) is used to generate chip select signals, either disconnect A9, A10 from the decoder or disconnect that chip select line within the ROM Simulation module. If the ROM Simulation module has an external chip select input on a grabber, connect it to the memory (ROM) enable signal. Connect disconnected chip select inputs to the proper logic levels and plug in the ROM Simulation modules into all PROM sockets with address locations 0 - 511.

Example 7 - MEMORY ARRAY: 3k X 64
ROM TYPE: 1k X 8 using MEM-128

This example is similar to example 6 above.

3.2.3 CHANGING ROM SIMULATION CHIP SELECTS

Changing the chip selects is accomplished by changing wire-wrapped connections on the ROM module P.C. boards.
Two different circuits are most commonly used to process the chip select inputs within the ROM Simulation Module. Schematic 1016 shows a typical circuit used for the non-multiplexing ROM Simulation module. It is based on a 74S151, an 8 to 1 multiplexer. The multiplexer can have up to four inputs from the ROM socket: the 3 selector inputs A, B, C and one signal input. The selector inputs determine which one of eight lines are multiplexed to the output. Seven of the eight lines are tied low, which when selected would disable the output. The eighth is tied high or tied to a positive true chip select input. When disconnected as described under Addressing, these lines should be tied to the following logic levels:

Pin	Designation	Logic Level
11	A	GND
10	B	GND
9	C	VCC*
15	D4	VCC*

Where VCC* is located on J78, the enable input to the 74S151 is controlled by STEP- N.

An example of the second enable circuit used is shown in schematics 1021 and 1022. Here a three to eight decoder is used to select between: output disable, data low order address, and data high order address. The following signal inputs are used:

Pin	Input From	Use	Notes
1	ROM SOCKET	$\overline{CS}$	On 2k X 4 Simulation
2	ROM SOCKET	$\overline{CS}$	Pin 182 connect to different ROM plugs
3	ROM SOCKET	A10	Selects data source
4	STEP-N	Enable	Both Pin 4 and Pin 5
5	STEP-N	Enable	must be low for output enable.
6	ROM SOCKET	$\overline{CS}$	May be tied high internally.

3.2.4 ROM INTERCONNECTION PROCEDURES

After memory organization has been decided, doing the actual ROM module interconnect is simple.

First determine if the ROM module is multiplexing or non-multiplexing. Multiplexing types have two (2) twenty-conductor gray data cables running to the same ROM module, as shown in figure 1.4.1.4a*. Non-multiplexing versions have one twenty-conductor cable per module as in figure 1.4.1.4b.

3.2.4.1 NON-MULTIPLEXING ROM SIMULATION MODULES

Insert each ROM Simulation plug into its corresponding socket on the target processor starting with the Master ROM module. The Master ROM module contains the least significant bits and can be recognized by the 26-conductor address cable, with multiple board edge receptacles. Its data cable should be plugged into the least significant memory board , right tongue. For proper DIP insertion technique see section 3.2.4.2.

The ROM Simulation modules (orange boxes) usually come in pairs. To determine which module in the pair contains the least significant data byte and which has the most significant data byte look at the attached gray data cable. The cable having the red stripe (figure 1.4.1.4b) carries the least significant data.

*Located in Section 1.4 of this manual.

3.2.4.1 NON-MULTIPLEXING ROM SIMULATION MODULES (CONTINUED)

ROM 8 modules have one ROM Simulation DIP only per module while ROM 4 modules have two. On ROM 4 modules, the shorter upper flex cable contains the least significant nibble (figure 1.4.1.4e). On master ROM 4 modules, this upper cable is the only one with address information.

Insert each ROM Simulation plug in turn into the proper target processor socket. The ROM data is determined by the data on the WCS data tongue to which the data cable is plugged.

3.2.4.2 INSERTING THE ROM PLUG

Two versions of the STEP ROM plug exist:

Old Version:	Plug has flex cable soldered on top with a grey strain relief.
New Version:	Termination is composed of a sandwich consisting of the plug, flex circuit, black rubber strain relief and PC cap.

Both versions insert into the socket in the same manner. Figures 1.4.1.4 e and d show a drawing of these plugs along with pinout.

CAUTION: *Identify pin 1 on the ROM plug and the socket before inserting the DIP plug. If the plug is inserted backwards, damage will result to the active buffer circuits in the orange box.*

Even the new version of the ROM plug can be broken if handled inproperly. Damage to the flex circuit and pins will result if the plug is yanked out of the socket by the cable. Handle with care!

NOTE: *Plug life can be prolonged by permanently plugging the STEP DIP plug into a socket. If damage occurs to the pins from improper insertion or withdrawals, this low-cost adapter can be discarded and replaced with another. See next page.*

3.2.4.2 INSERTING THE ROM PLUG (CONTINUED)

ROCOMMENDED SOCKETS

#PINS	AUGAT PART NUMBER	
16	516 - AG xx D	xx=10,19,11,37
18	518 - AG xx D	xx=10,19,11,37
20	520 - AG xx D	xx=10,19,11,37
22	522 - AG xx D	xx=10,19,11,37
24	524 - AG xx D	xx=10,19,11,37

3.2.4.3 ROM INTERCONNECT RULES

1) Determine if the ROM module is multiplexing or non-multiplexing. Multiplexing types have two (2) twenty conductor data cables running to the same ROM module, non-multiplexing versions have one twenty conductor cable.

NON MULTIPLEXING

2) Find the Master ROM module: is labled master and has the 26 conductor address cable running to it.

3) Determine if the Master module is the least significant or most significant ROM module in the pair: The least significant ROM module has a red stripe on the data cable.

NOTE: Master ROM modules produced after 1978 should have the least significant 8 of 16 bits in the module pair.

4) Determine memory organization: d x 32, 2d x 16 or 4d x 8.

5) Starting with MEM-1, the lowest-slot memory board, plug the data cable from the Master ROM module into the data tongue in ascending order of significance.

6) Carefully determining which the least significant PROM DIP in each module and cable, proceed to plug in all DIPs from lsb to msb of the micro-word, handling with care.

7) If any strain is placed on the flex cables or DIP plugs, relieve it. Often, users simply tie up bundles of ROM simulation cables with string or wire to a bench shelf or other "sky-hook," to support their weight. This pays off in:

3.2.4.3 ROM INTERCONNECT RULES (CONTINUED)

a) Probing convenience - keeps the cables out of your way during debug.

b) Cable life - cuts down flexing.

c) Trouble-free operation - with good practice, you need never have an intermittent in your cables.

3.3 DIRECT WCS INTERCONNECT (WITHOUT ROM SIMULATION)

Direct Interconnect of the WCS to the Target Processor offers several advantages vs. ROM Simulation Interconnect:

1) It is less costly.
2) It offers less signal propagation delay when buffers are not in use.
3) It uses less board space.

However, if the interconnect is not properly engineered, reflections and crosstalk within the interconnect cabling can double or quadruple access time.

When designing the interconnect:

1) Don't leave signal lines unterminated.
2) Don't remove grounds or leave ground lines connected at one end only.
3) Don't splice cables together.
4) Don't lengthen lines unnecessarily.

3.3.1 SIGNAL TERMINATION

If signals are not properly terminated, reflections and crosstalk will occur seriously degrading performance. The following sections detail termination techniques for standard cases.

3.3.2 GROUNDING

The interconnect cabling used by Step is designed to have one ground line between each signal line: Signal, Ground, Signal, Ground, etc. This cuts down crosstalk since 80-90% of any signal coupling occurs between adjacent lines. It also provides a convenient ground return for each signal line. It is important that each ground line be connected to a solid ground point on each side of the cable. Without connections at

3.3.2 GROUNDING (CONT)

both ends, signal reflections on the ungrounded lines will occur which can lead to erroneous signals on data lines. Each WCS automatically terminates ground lines at the cable interface. It is up to the user to properly connect the ground lines at the other end of the cable.

3.3.3 CABLE SPLICING

Cable Splicing should be avoided wherever possible. The type of cable used in the Step Engineering instruments has controlled impedance characteristics. Terminations and splices do not have this same impedance and therefore cause undesirable line reflections and loss of signal energy at the receiving end.

3.3.4 CABLE LENGTH

Cable Length should be minimized and under no circumstance exceed 10 feet (3 meters) to avoid transmission problems. If cable length exceeds 10 feet special drivers and receivers should be used. To calculate signal delay through the cable, a figure of 1.75ns/foot (5.9ns/meter) should be used for each direction of signal travel. This corresponds to a figure of 3.5ns/foot for combined address/data delay (round trip).

3.3.5 DATA INTERCONNECT

The type of interconnect chosen depends primarily on the load of the output at the target processor.

For the discussion which follows, examples will be given for two load types:

UNIT LOAD - A load of one high impendance TTL gate near the cable termination. Such termination is commonly found in

pipeline systems where the output of the control store feeds directly into a register such as a 74S374.

DRIVEN LOAD - A load of multiple schottky gates located randomly on the target process board. This type of loading occurs where a control output runs to several circuit elements.

Interconnect methods for the DRIVEN load should work regardless of loading.

3.3.5.1 DATA LINE INTERCONNECT - UNIT LOAD

Using a UNIT load to terminate a cable is close to the ideal open circuit transmission line. Theory for an open circuit transmission line states that the signal reflects from the open end, doubling in voltage. Hence a change in voltage from 3.5 volts to .5 volts would result in an open circuit voltage of -2.5 volts and a change from .5 volts to 3.5 volts would result in an instantaneous voltage of 6.5 volts. These voltages could damage both driver and receiver circuitry. In addition, the reflections take time to die out and can cause excessive crosstalk. To avoid this problem either a series resistor at the source, or a parallel resistor combination at the cable termination is used to match the cable impedance. A pair of resistors (Vcc/ground termination of 220/330 ohms) roughly matches cable impedance of 90-105 ohms with the result that the reflections and attendant excessive voltage swings do not occur. For series source terminations, ideally one would match the cable impedance. However, the actual impedance at the cable end is not infinite and a critically damped wave adds excessive delay time. In practice, a source resistor of 1/3 to 1/2 of cable impedance results in reasonable delay and minimum under and over shoot. Step uses a value of 33 or 47 ohms on its INTl, resistive interface.

NOTE: Resistive source termination is not desirable for driving long transmission lines.

3.3.5.2 DATA LINE INTERCONNECT - DRIVEN LOAD

As the impedance of the cable end decreases from that of the unit load (approximated by infinite impedance), different types of line termination become necessary. If the termination impedance of the line matches the line termination no other termination is necessary. However, with today's technology, the impedance of a logic low is a factor of five less than a logic high. Hence this condition is never met. Even worse is the case where the line terminates in a zero impedance load. This occurs with heavy capacitive loading such is commonly found when driving backplanes or additional cables. A zero impedance load results in a reflective signal of equal and opposite polarity to the incoming signal resulting in temporary signal cancelation. Line reflections will continue as signals propagate up and down the cable until the quiescent value is reached, several cable delay times later. The only way to avoid these problems is to buffer the signal at the cable termination.

3.3.6 ADDRESS LINE INTERCONNECT

The WCS memories supplied by Step have a high impedance buffer on the address lines. If the output from the address generator is solely driving the Step system, resistive source termination of the type described under Data Lines, Unit Load, is sufficient. If heavy loading in addition to the Step system is expected, a separate set of buffers followed by resistive source termination is recommended. This buffer/ termination pair to be used exclusively for driving the WCS address cable.

3.3.7 ENABLE LINES

In order to obtain address readout and breakpoint information, the Enable Out, EO, and Enable In, EI, signals must be properly connected. EO is used to indicate valid memory data on the output of the Writable Control Stores. These four signals, one for each output byte on the WCS memory, are low true whenever the instrument is in the RUNNING or MON RUN mode and may be low true in MON HLT. In other instrument states they are high (False).

> *NOTE: EO lines should be ANDed with system memory enable lines to generate memory enable and Enable In, EI signals. See figure 3.3e.*

Use of enable out lines prevent false information from the Step WCS from affecting system state on non-synchronous control lines.

To generate proper address and breakpoint, the EI lines must be in the proper state. An ADDRESS = NONE message indicates that no valid EI pattern is present. This is generally true when target processor power is off or improper connection exists between the target processor and the Step instrument.

> *CAUTION: Damage or loss of memory data may occur if the target processor power is turned off while the Step instrument is in MONITOR command: RUNNING, MON RUN, or MON HLT.*

The following represents valid EI patterns to obtain proper address and breakpoints.

WCS ORGANIZATION	$\overline{EI3}$	$\overline{EI2}$	$\overline{EI1}$	$\overline{EI0}$ (LSB)	CONNECT
D x 32	LOW	LOW	LOW	LOW	MEM Enable
2D x 16	HIGH	LOW	HIGH	LOW	Least Sig
	LOW	HIGH	LOW	HIGH	Most Signi.
4D x 8	HIGH	HIGH	HIGH	LOW	Least signi.
	HIGH	HIGH	LOW	HIGH	2nd LEAST significant
	HIGH	LOW	HIGH	HIGH	3rd Least significant
	LOW	HIGH	HIGH	HIGH	Most signi.

D = "1" for MEM-32 and "4" for MEM-128

When the WCS memory is organized 2D x 16 or 4D x 8 the most significant target processor address lines must be decoded and ANDed with other memory enable lines to obtain proper EI signals.

3.3.8 RECOMMENDATIONS

3.3.8.1 ADDRESS

Address drivers should be resistive source terminated as in diagram 3.3d.

3.3.8.2 DATA, DRIVEN LOAD

Data lines should be buffered as close as possible to the target processor - 6" or less interconnect for optimum results, see diagram 3.3c. For recommended IC types, see section 3.3.10, recommended Data Drivers.

3.3.8.3 DATA, UNIT LOAD

Depending on cable length and desired output characteristics, two terminations are possible: The data lines should be resistively source terminated using Step interface 1 per diagram 3.3a. Alternatively they can be source buffered with a parallel termination at the target processor, diagram 3.3b.

3.3.9 WCS ACCESS TIME

Total access time of the WCS memory system can be calculated as follows:

$$S_{ac} = M_{ac} + C_D + B_D$$

Where:

S_{ac} = Worst Case System access time

M_{ac} = Worst case memory access time

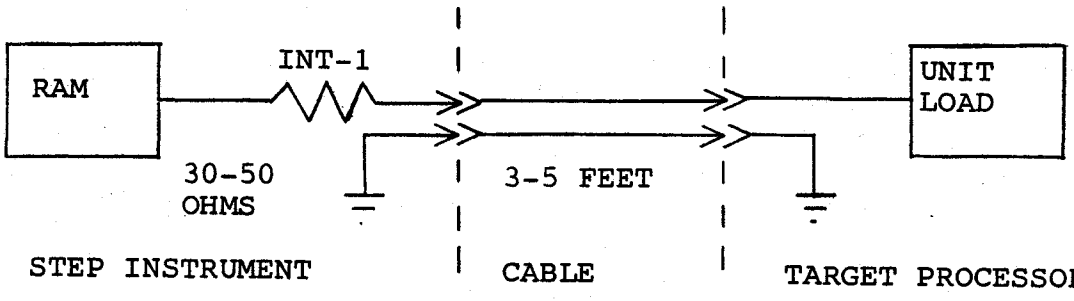
C_D = Cable delay @ 1.8ns/foot (or 3.5ns/ft round trip)

B_D = Buffer or register delay time (if present in the circuit.)

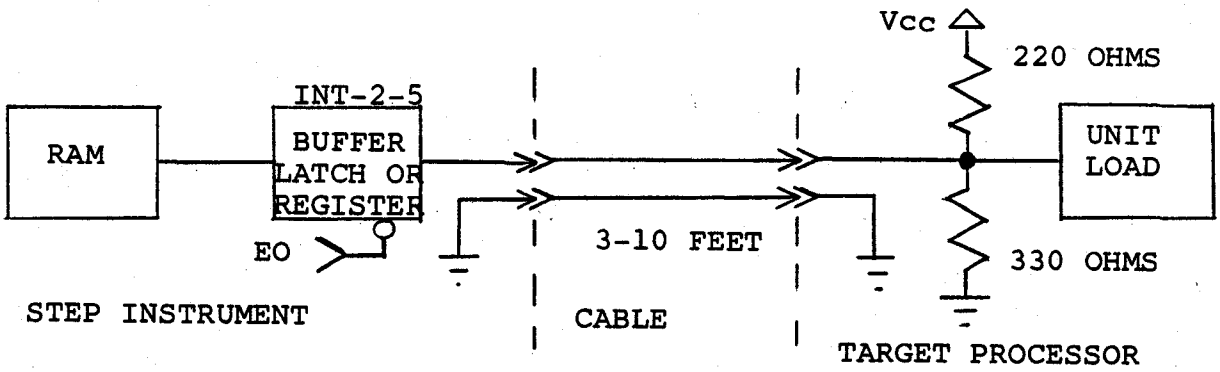
3.3.10 RECOMMENDED DATA DRIVERS

Whether data drivers are located in the sockets on the STEP WCS board (figure 3.3b) or close to the loads in the target machine (figure 3.3e), we suggest the following IC's:

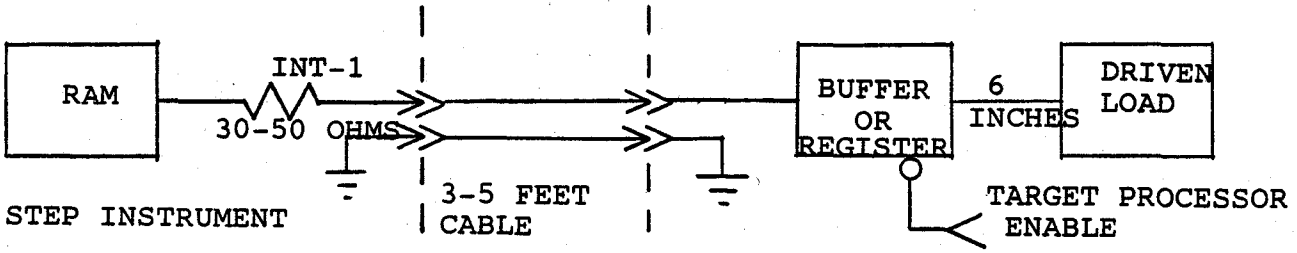
SUGGESTED BUFFERS:	74S241, 74S257 or Equiv. (non-inverting) 74S240 or equivalent (inverting).
SUGGESTED REGISTER:	74S374 or equivalent
SUGGESTED LATCH:	74S373 or equivalent



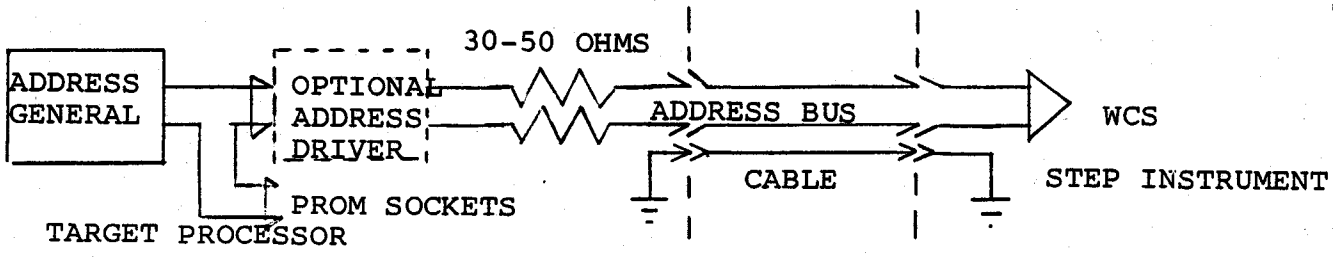
3.3a DATA OUTPUT - UNIT LOAD



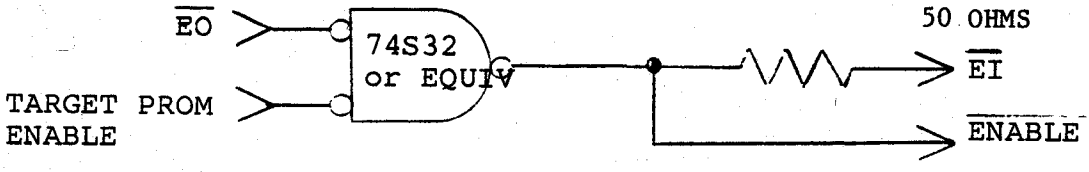
3.3b DATA OUTPUT - BUFFERED UNIT LOAD



3.3c DATA OUTPUT -DRIVEN LOAD



3.3d ADDRESS INPUT



3.3e ENABLE LINES

3.4 SERIAL I/O INTERCONNECT

STEP instruments are equipped with three serial I/O ports designed for communication in the RS-232C or 20 ma current loop protocol. The ports are optically isolated from internal signal ground. Port 0 is for 20 ma current loop only, Port 1 is a full implementation of RS232C and Port 2 is the popular 3-wire RS232 -- a partial implementation in which the CTS, DSR, and CDET inputs are ignored and RTS and DTR are set true when the port is selected. This section describes the data format, RS232 signal definitions, and typical user wiring for interconnect.

The three serial ports are defined according to RS232-C and 20 ma current loop specifications. The 20 ma port (port 0) provides easy communication between TTY's and computers employing 20 ma 4-wire interfaces and is recommended for serial links where transmission is over greater distances than the normal 50' specified in RS232-C. The ports may be operated either full or half duplex in conjunction with the DEVICE specified.

PORT 1, the modem port, is a complete RS232-C interface assuming the peripheral device connected is a Bell 202-type machine. This port provides the normal link to most time-share facilities. The port 1 interface provides for a wait for Clear To Send (CTS), and will detect loss of Carrier Detect (CDET) or Data Set Ready (DSR) by displaying an error message.

3.4 SERIAL I/O INTERCONNECT (CONTINUED)

The Request To Send (RTS) and Data Terminal Ready (DTR) signals are set true on the interface following parameter specification. If the CTS input is not present on the port following device specification, a message "Waiting for CTS = 0" is displayed and the STEP-N instrument pauses until CTS is TRUE.

This feature provides a convenient prompt for time share users to dial up the time share number and place a telephone receiver in the modem. When the connection is made and a carrier is detected, operation proceeds. All timing on the interface conforms to RS232-C and 20 ma current loop specifications.

PORT 2, the RS232-C port, is a general purpose port which essentially ignores the Clear to Send (CTS), Data Set Ready (DSR), and Carrier Detect (CDET) signals of the complete RS232-C specification.

Port 2 is generally used for direct interconnect to RS232 ports on Host computers, glass teletypes, PROM or RS232 storage devices. Port 2 may be operated in either a full or half duplex system by choosing 2 or 5, as the device number.

> *NOTE: This port may be used to download to STEP-N, because the STEP-N is never too busy. But trying to upload to a multi-tasking host without the CTS is asking for trouble. If you must upload, use Port 1.*

3.4.1 DISALLOWED I/O COMBINATIONS

It should be noted that all possible combinations of functions, devices, and formats are not currently allowed.

3.4.1 DISALLOWED I/O COMBINATIONS (CONTINUED)

Restrictions and disallowed combinations are tabulated and enumerated in section 2.5.1. Note especially:

1) BNPF is restricted to punch functions only (STEP-2 only) and device 0 or 4. Note this is the only punch combination allowed. Punch has been included primarily for punching a paper tape on a TTY, and only in STEP-2.

2) Device 3 and format 1 must be specified concurrently for Data I/O model 7 or 9, since there is interaction between device and format on this device. This provision has been included for dumping to Data I/O PROM programmers.

The remainder of the possible combinations have been allowed to provide a flexible and powerful data transfer capability.

3.4.2 DATA TRANSMISSION FORMAT

Serial I/O information is coded in asychronous serial start/stop format, for both transmit and receive. Operation of transmit and receive data is half or full-duplex. The STEP-N instrument does not echo characters received.

Data is coded in seven level ASCII plus parity. Each character is sent as one start bit, 8 data bits and at least one stop bit. Parity is not utilized or checked by STEP-N; however, parity may be transmitted from STEP-N as specified by the user. The STEP-N uses asynchronous transmission. This means each character is transmitted as a complete, self-contained message consisting of the data character with parity, preceded by a start bit and followed by one or two stop bits.

When the start bit is received, a clock signal is initiated to clock in the remainder of the word. The one or two stop bits are used to signify the end of the word and terminate the receive clock.

Generally, transmission rates of 110 baud and lower use two stop bits, and rates of 150 and higher use one stop bit.

Figure 3.4.1 illustrates the serial data format employed:

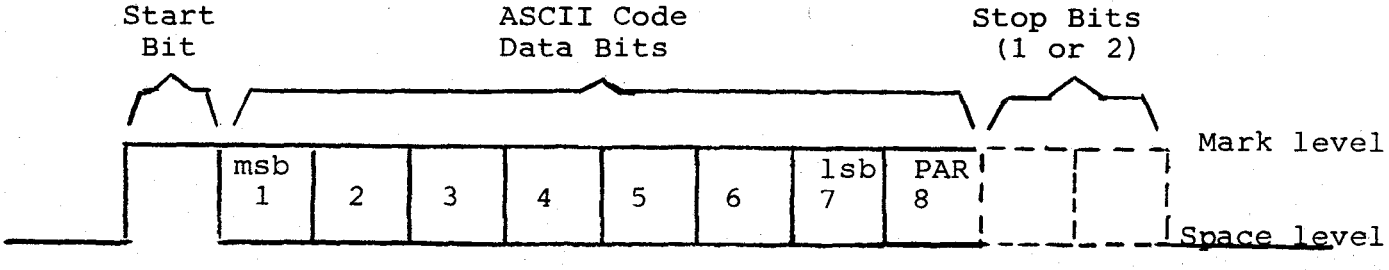


Figure 3.4.1 Data Format for Step Engineering Serial Input-Output

3.4.3 SIGNAL DEFINITIONS FOR THE SERIAL INTERFACE

1) Ground - In the RS232C environment, this line provides Safety Ground.

2) TX - Transmit Data - This line transfers data to an RS232C terminal.

3) RX - Receive Data - This line accepts the input data from an RS232C compatible terminal.

4) RTS - Request to Send - This line held high by STEP-N to announce its intention to send data.

5) CTS - Clear to Send - This line is received high true by the STEP-N from a RS232 data terminal and informs STEP-N the terminal is ready to accept data. On Port 1, the modem port, CTS is the modem's response to RTS. The transmitting of data from Port 1 on STEP-N may be held up at any time by lowering CTS. This will stop transmission at the completion of the current character being transmitted. (This input is ignored on Port 2.)

6) DSR - Data Set Ready - This line is received high true by STEP-N on Port 1 and indicates when a valid data terminal is connected. It is normally held true whenever power is turned on, on a modem on Port 1, and is ignored on Port 2.

7) SG - Signal Ground - This line provides the common signal connection to the RS232C data lines.

8) CDET - Carrier Detect - This line is received high true by STEP-N. It is normally sent true by the modem connected to Port 1, to indicate a carrier is received. STEP-N will not proceed with I/O until a carrier is detected and loss of carrier during transmission results in an error. This signal is ignored on Port 2.

9) DTR - Data Terminal Ready - A high level on this line is generated by STEP-N to indicate that it is ready to receive or transmit.

PORT Ø

PIN #

1) SOL - Serial Output Low - This line transmits serial data to a 20 ma device.

2) V5 - +5V supply - Available for external use if required.

4) SIL - Serial Input Low - This line receives low-true data from a 20 ma device.

3.4.3 SIGNAL DEFINITIONS FOR THE SERIAL INTERFACE (CONTINUED)

5) GND - Common Connection for signal ground when optical isolation is not required.

6) SIH - Serial Input High - This line receives high-true data from the 20 ma device.

7) V12 - +12V supply - Available for external use if required.

Use schematic 0001053, sheet 2 to understand the circuits involved, before connecting.

3.4.4 INTERCONNECT WIRING CONNECTIONS

The STEP-N unit may be interconnected to another RS232C device in a variety of ways as either a terminal or Data Communication Device, depending on wiring interconnect. Interconnect to a modem (Bell 202 type) interconnect to Port 1 is a one for one interconnect and the modem cable provided with your STEP-N unit may be directly connected.

When interconnecting other devices to PORT 1, the DTR, RTS outputs may be cross wired back to DSR, CDET, and CTS respectively to disable the wait and error detect functions. Figures 3.4.2, 3.4.3, and 3.4.4 give the proper interconnects for normal use. Other combinations may be employed by the user to accommodate a wide variety of peripherals. For detailed pinouts, see STEP ENGINEERING drawing number 0001053 sheet 2.

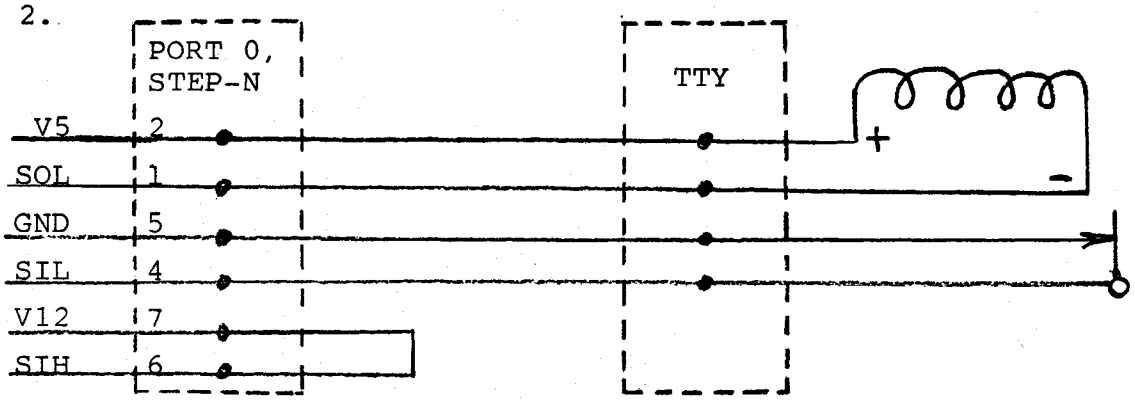


Figure 3.4.2 TTY/STEP-N, Typical Interconnect for Full/Half Duplex

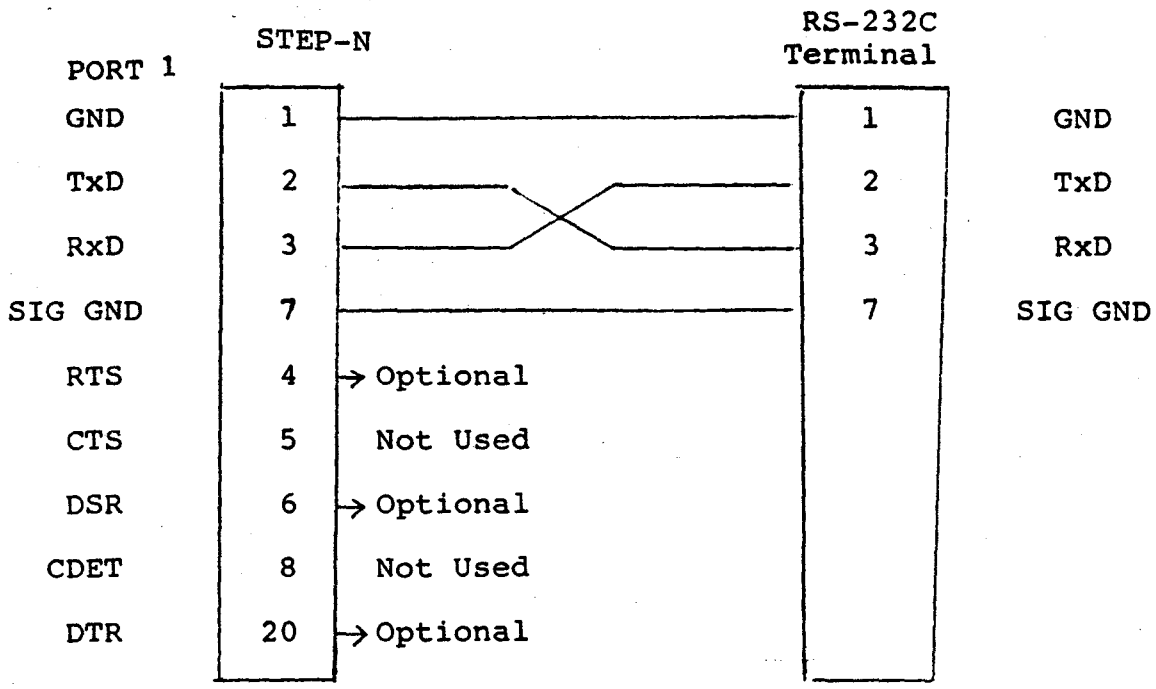


Figure 3.4.3 RS-232-C STEP-N full/half duplex Interconnect for PORT 2.

NOTE: See Appendixe D for full ASCII charts.

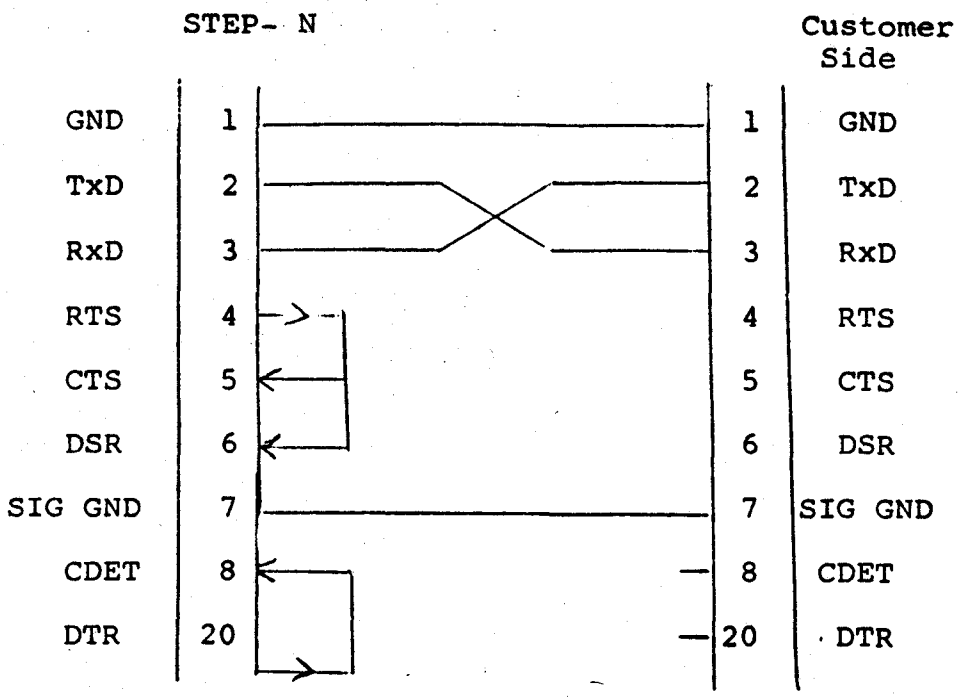


Figure 3.4.4a. Interconnect for operation without handshake on CTS.

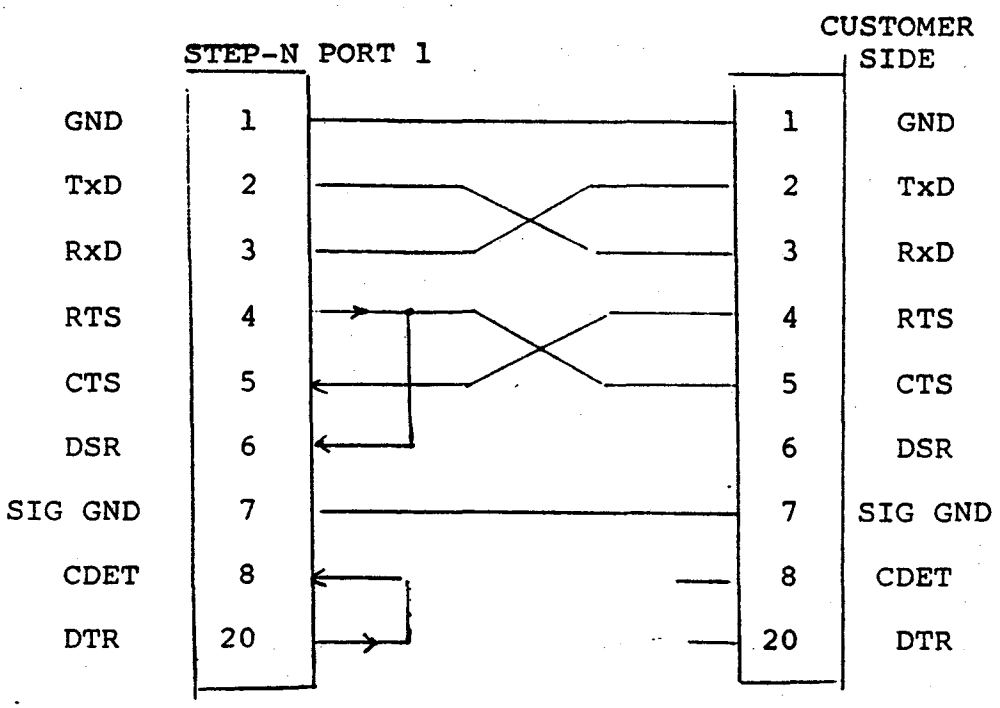


Figure 3.4.4b Use of PORT 1 with cross-wired interconnect to non-modem devices.

Interconnect for operation with handshake on CTS.

3.5 CLOCK CONTROL

3.5.1 GENERAL

Clock Control circuity within STEP-N is necessary for:

RNN/HLT control, Single and NSTEP, Single and MULTI CYCLE,

Halt on event, Halt on Breakpoint, FORCE™, JAM and XSTATE™.

For further information on the above commands, refer to section 2.4, Monitor Commands .

NOTE: Clock Control is not necessary for the proper functioning of TRACE or the Writable Control Stores.

3.5.2 STEP and CYCLE

3.5.2.1 STEP and CYCLE DEFINITIONS

CYCLE: One complete instruction cycle composed of one or more clocks.

MACROCYCLE: A macro instruction cycle composed of one or more microinstructions. Example each instruciton within the assembly language instruction set of a CPU is a macrocycle. In an "ADD" instruction, a macrocycle may be composed of only one microinstruction. In an "FFT" instruction, it is composed of many micro-instructions.

MICROCYCLE: A microinstruction cycle composed of multiple clocks or a variable number of clock phases.

STEP, MICROSTEP: An instruction cycle composed of one clock, or a fixed number of clock phases.

3.5.2.2 STEP and CYCLE FUNCTIONS

The STEP-N instrument is capable of providing both a single step or an Nstep function as well as a single cycle or multicycle function. On STEP or NSTEP, one clock cycle is initiated every ½ second. On cycle or MCYCLE, one clock cycle is initiated every ten microseconds until the CYCLEI input goes true. The CYCLEI signal is an input signal to the STEP instrument indicating the end or start of the next cycle. It is sampled at the end of each STEP, and if not true, another step clock is initiated. The CYCLEI signal can be positive or negative true. It can be connected to any of the following signal types:

3.5.2.2 STEP AND CYCLE FUNCTIONS (CONTINUED)

SIGNAL	USE
NONE	Function not used.
MICROSTATE	Hookup to the signal indicating the beginning or end of a microcycle. Allows microcycles of various lengths to be automatically handled by the instrument.
MACROSTATE	Hookup to the control signal used to fetch the next macroinstruction. Allows non real time run through of a macroinstruction cycle.
OTHER	Hookup to a breakpoint, microcode flag or other signal to allow non real time running up to an examination point.

3.5.2.3 HOOKUP

The following refers to sheet 1 drawing 1053, Schematic I/O and CLOCK. P53 is the clock interconnect port found on the bottom left on the right side of the STEP-N instrument. J1 through J8 are jumper posts found on both sides of P53. The STEP-N side panel is labled to show the locations of P53 and J1 throuth J8.

INPUT	P53	JUMPER	
CYCLEI	PIN19	J6 - J8	If positive true or pin 19 not connected.
		J7 - J5	If negative true.
		J2 - J4	If CYCLEI input is used for single step and CLKI is tied high (see section 3.5.3.2)

3.5.3 CLOCK INTERCONNECT TYPES: Gated Clock, Synchronous Control, Asynchronous Control, (AM 2925 Control)

To determine proper interconnect type:

1) Choose if Step, Cycle or both functions are necessary, section 3.5.2.

2) Choose type of clock interconnect desired: Asynchronous control, Synchronous control, Gated Clock, figure 3.5.3.

3) Establish timing criteria and control level edge requirements and check compatibility with chosen interconnect.

4) Look up the suggested interconnect scheme based on "1" and "2" above, section 3.5.5.

3.5.3.1 GATED CLOCK

In the Gated Clock interconnect method the clock provided from the target processor oscillator is combined with the RUN HALT, SS signals generated by the STEP instrument and used directly as the target processor clock. Figure 3.5.3.1 illustrates this scheme. This scheme can be used with single phase clocks or multiphase clocks with the clock phases regenerated from the STEP gated clock. The major advantage of using this method is simplicity. The disadvantages include:

1) the extra resistors and buffers to insure solid signals
2) clock distortion through the cable and 74265
3) the need to actively select either the STEP input or oscillator input for use. If the Step system is being used in manufacturing, having to switch clock sources is undesirable.

3.5.3.2 SYNCHRONOUS CONTROL

In the Synchronous Control interconnect method the clock gating circuitry is provided on the target processor, TP, board. From the STEP system, a set of control lines, synchronous with respect to the target clock, is generated. These signals are used to gate the clock. Figure 3.5.3.2 illustrates this design. Note that the CLKO signal (pin 11 on P53) is positive, true, during a RUN or SS state. Any type of gating circuitry including the counter used to generate clock phases (if present) can be used in place of the gate shown. The major advantages of this circuit are:

1) No clock skew.
2) Proper operation with or without STEP instrument connected
3) Design choice over clock level on HALT

The major disadvantages are:

1) Design time to insure timing and signal level constraints are met: In the design shown the negative clock transition must be used.
2) The Cycle function can no longer be used since the CYCLEI input is used for the clock.

If the CYCLE function is desired (see section 3.5.2), pin 12 of U2 can be cut from CLKI, J1 jumpered to J2, and pin 17, CLKI, used to input the clock signal in place of pin 19, CYCLEI.

NOTE: When using this control method, CLKO will go positive for one clock cycle for each single step.

3.5.3.3 ASYNCHRONOUS CONTROL (AM2925)

In the Asynchronous Control interconnect method both clock gating and clock synchronization must be supplied by circuitry on the target processor board. An example of this would be the AM2925 chip which internally synchronzes these signals. On the 2925, as long as the HALT level is present before the positive edge preceeding the chosen clock period (first or last) the clock will stop. No clock input from the TP must be supplied to the step I/O and CLOCK board. During Single Step a clock pulse of approximately 50ns is supplied to the TP. To lengthen this pulse, a capacitor may be connected from U11 pin 3 or U4 pin 3 to ground. U11, a 1489, has a current limited output of 10ma, hence each 100pf of capacitance will increase pulse width approximately 10ns. Figure 3.5.3.3 shows the interconnect of the Asynchronous Control lines to the 2925. Note that since the Single Step pulse and RUN/HALT are ORed together by the STEP circuitry the Single Step inputs on the 2925 are not required.

3.5.4 TIMING, EXTERNAL HALT

3.5.4.1 GENERAL

One of the important functions of the clock control circuitry is its ability to halt the target processor in real time to enable processor examination. Four different signals can be used as halt inputs:

WCS Breakpoint Output	(Non Latched)
Flag bit from the Control Store	
Target Processor Flag or Input	
Trace Output (STEP-3 only)	(Latched)

If the signal being used is not latched, then it must obey the timing constraints given below to halt the processor, Appendix G gives a schematic and modification instructions to the CLK and I/O board to enable it to latch incoming halt signals regardless of timing.

It is possible to halt the target processor either at the end or beginning of a cycle (Macro or Micro) if either the Gated Clock or Synchronous clock control method is being used:

JUMPER	HALT ON
J5 - J3	Positive Cycle
J6 - J3	Negative Cycle
J1 - J2	Negative Step
J5 - J3	Positive Step (assuming the clock input is tied to CYCLEI, P53 pin 19.

3.5.4.2 TIMING CONSTRAINTS

	MIN	TYP	MAX
XH Input to CLKC (or CLKC) output:	13.5ns	23.5*ns	39.0ns
XH Setup time required W.R.T.CLKI edge	16.0	28.5*	46.0

*Typical time for XH going positive (i.e. to halt the target processor.) Add 1.5ns to typical time for XH going negative (i.e. restart of processor)

tpd for CLKI to CLKO (delay thru U2, 74265)	6.0	10.0	18.0
XH Setup time required w.r.t CLOCK input on CYCLEI	-2.0	18.5	40.0
Delay for address to breakpoint out- (assuming ROM Simulation and a 5 foot cable)	60.0	75.0	85.0

3.5.5 HOOKUP SUMMARY (Superscripts refer to notes)

CONTROL TYPE	CLOCK INPUT	CYCLEI INPUT POS	CYCLEI INPUT NEG	CONTROL/CLK OUTPUT POS	CONTROL/CLK OUTPUT NEG	JUMPERS
ASYNCHRONOUS	NONE	x		CLKC,5	CLKC,7	J6-J8
	NONE		X	CLKC,5	CLKC,7	J5-J7
GATED CLOCK						
Halt on NEG STEP	CLKI,17			CLKO,11	CLKO,9	J1-J2, J6-J8
	CLKI,17		x	CLKO,9	CLKO,11	J1-J2 J5-J7
Halt on POS STEP	CYCLEI,19			CLKO,9	CLKO,11	J1-J2, J3-J5, J6-J8
Halt on CYCLE [2]	CLKI,17	x		CLKO,11	CLKO,9	J5-J3, J6-J8
	CLKI,17		x	CLKO,11	CLKO,9	J6-J3 J5-J7
SYNCHRONOUS						
Halt on NEG STEP[3]	CYCLEI, 19	none		CLKO,11	CLKO,9	J6-J3, J5-J7
Halt on POS STEP[3]	CYCLEI,19	NONE		CLKO,11	CLKO,9	J5-J3, J6-J8
Halt on CYCLE[2,3]	NONE	x		CLKO,11	CLKO,9	J5-J3 J6-J8
	NONE		x	CLKO,11	CLKO,9	J6-J3, J5-J7

3.5.5 HOOKUP SUMMARY

NOTES:

1) Precludes the use of cycle
2) Hookup is for halting in real time at the end or beginning of a Micro or Macro cycle. It assumes halt on a low logic level clock and requires an externally latched input if being used on a Macrocycle.
3) CLKI, must be tied high.

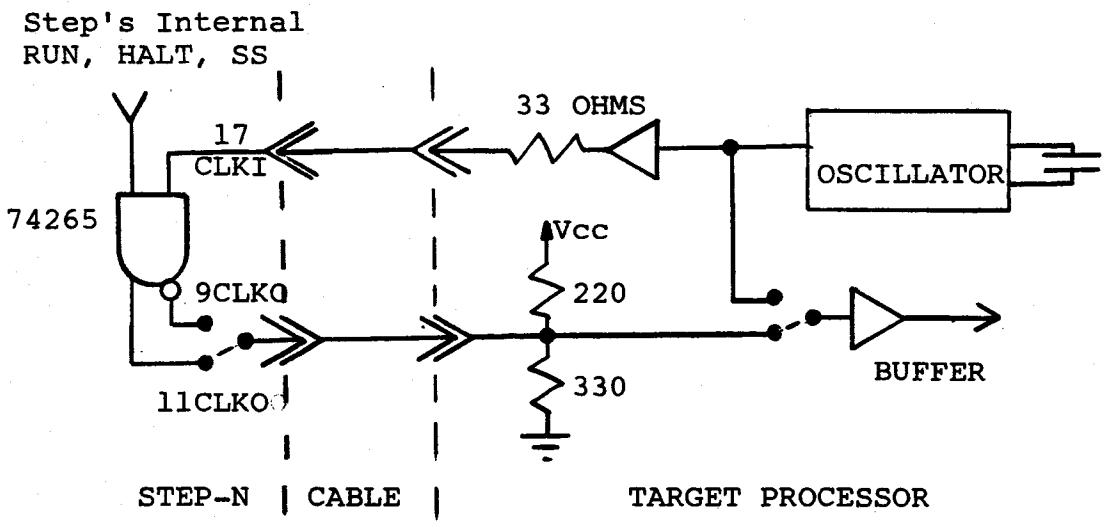


FIGURE 3.5.3.1 GATED CLOCK INTERCONNECT

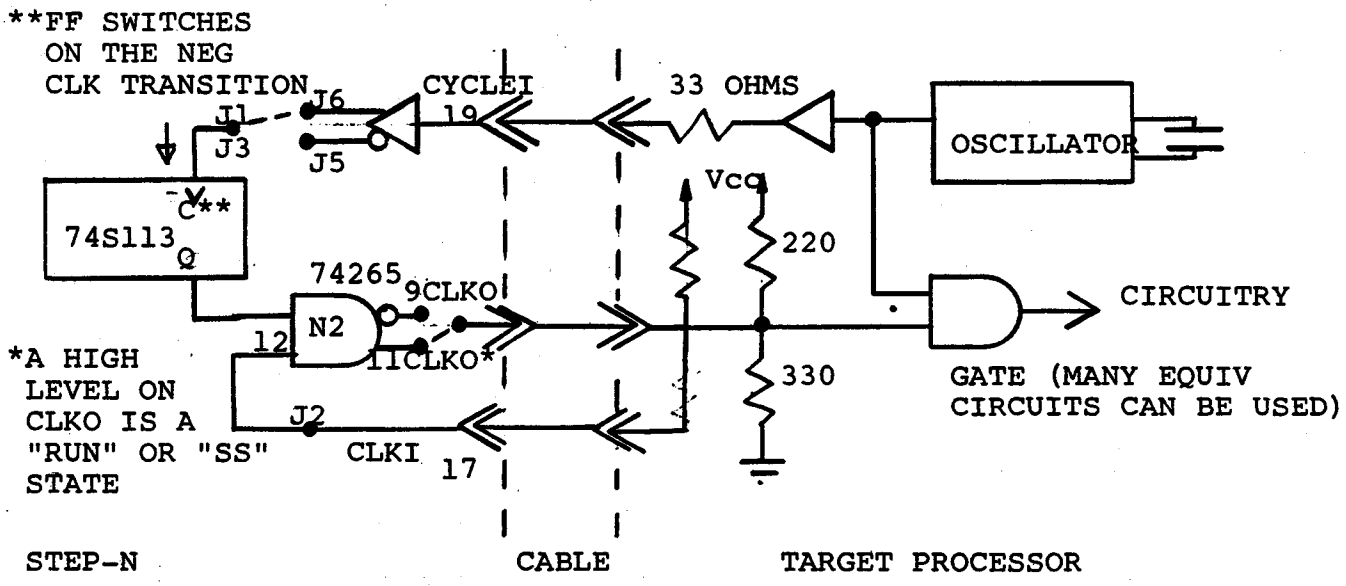


FIGURE 3.5.3.2 SYNCHRONOUS CONTROL INTERCONNECT

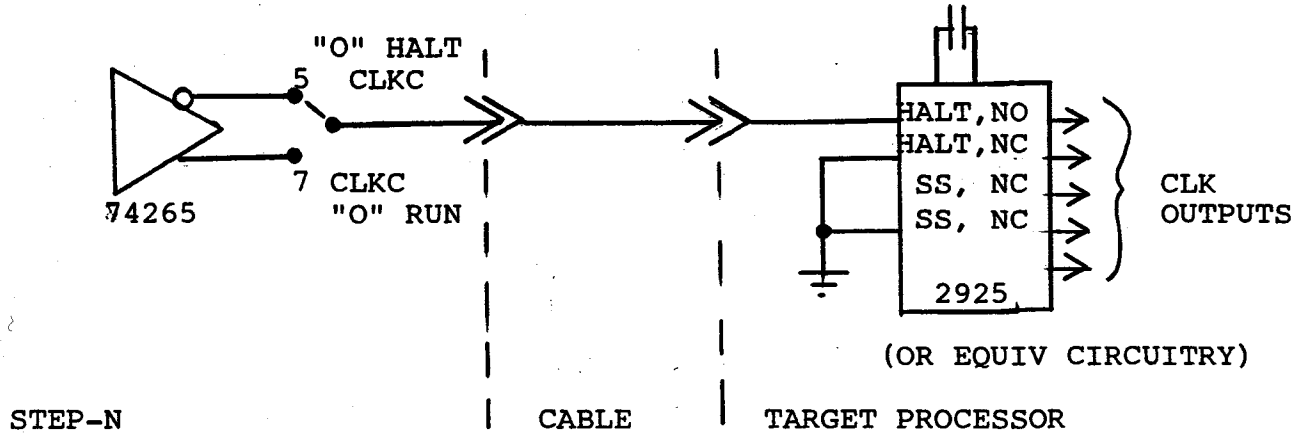


FIGURE 3.5.3.3 ASYNCHRONOUS CONTROL INTERCONNECT

3.6 TRACE HOOKUP

3.6.1 GENERAL

Trace permits the user to synchronously follow the path of execution of the target processor in real time. To do so, Trace inputs must be properly connected to the target processor. Also the Trace board must be configured (through switches) to match the target processor. Once this is done, Trace operation can be controlled from the front panel.

The Trace board is self contained. It has all the logic and memory required to perform Trace functions: two address comparators, trigger logic, synchronizing logic, and a 250 x 32 bit memory. Therefore, the complete WCS memory is available to the target processor, and is unaffected by the addition of Trace to a STEP-N machine.

Trace is active only in MONITOR. From MON HLT or MON RUN the equation used to specify the trigger is selected from a series of menus presented on the CRT. The results of Trace are displayed on the CRT. Trace is only activated to receive data on entry to RUNNING with Trace status in the ARMed state. The Trace trigger may be ARMed from either MONITOR halt by use fo the ARM command or by completing a Trace setup procedure.

3.6.2 TRACE INPUTS

There are four sources of Trace inputs:

Master ROM simulation Module	-	Low order address inputs.
Address Probe	-	Upper order address inputs, qualifiers, external enable, address clock.
Data Probe, LSB	-	Least significant data input, data clock, and user control latch UCTL1.
Data Probe, MSB	-	Most significant data input, local data clock, and user control latch UCTL2.

Figure 3.6.1 gives a detailed description of the signals on three Trace probes. The probes may be connected to the target processor in one of three ways:

1) Using standard twenty six conductor ribbon cable (alternate signal, ground, signal, ground as shown in figure 3.6.2.)

2) Using the interconnect cable provided and plugging the individual leads into test points, wirewrap pins, or IC clips.

3) Connecting the interconnect pins to HP clips (provided) to attach directly to IC leads.

3.6.2.1 CLOCK INPUTS

Trace operates in a totally synchronous manner. Clock inputs are required to strobe the incoming information into latches, and these same clock (s) are used to synchronize Trace with the target processor. The most important of the clocks is the User Address Clock, UAC, from which Trace timing is derived. This signal input (UAC from the Address Probe) must be connected to the target processor or Trace will not operate.

The active edge of the UAC can be selected by switch S1 on the TRACE board. With S1 "ON" (up) the positive going clock edge is used to strobe address information and for the internal Trace clock generation. With S1 "OFF" the

negative going edge is used. For proper operation, the setup times detailed in Trace Specification must be observed. The UAC is used to latch the information from both the Address Probe and the Master ROM Simulation module. These latches are on the Trace PC board and do not affect memory board operation.

Each Data Probe has its own input clock. These User Data Clocks, UDC, are used in the same manner as the UAC. Switch S2 is used to select the active edge of the LSB Data Probe clock and S3 the active edge of the MSB Data Probe clock. UDCs affect only the latch in the probe.

The operation of these switches is identical to that of S1 (see figure 3.6.3)*. The UDC on the MSB Data Probe is <u>not</u> used for any internal Trace board timing. When this clock is different than the LSB UDC for proper operation, the active edge of the MSB UDC must occur between the active edge of the UAC and LSB UDC. The LSB UDC is used on the trace board to generate internal timing signals for incoming data from Data Probes.

The UDC can be derived from a totally different source than the UAC. However, the UDC should have a fixed timing relationship with respect to UAC. Depending upon the relative occurrance of the two signals, the displayed results may show recorded data offset by one clock from its associated address.

*At end of section 3.6.

3.6.2.1 CLOCK INPUTS (CONTINUED)

Example 1: If UDC and UAC are the same signal, data will be paired with the proper address.

Example 2: If UDC follows UAC by 55ns or more, data will be paired with the address clocked on the following UAC.

Example 3: If UDC follows UAC by 15ns to 55ns, data will be paired consistantly with either the address latched on the preceeding or succeeding UAC depending on Trace board timing.

NOTE: There exists a 3ns period of uncertainty. If UDC falls within this period, pairing may change on two successive traces.

Data/address pairing will always remain consistant within a given Trace.

3.6.2.2 ADDRESS INPUTS

The two sources of address inputs for Trace are the Master ROM Simulation module and Address Probe. The Master ROM Simulation module provides AØ-A9 and optionally A1Ø, and A11. The address Probe contains A10 through A15. Selection as to the source of A10 and A11 is made based upon the memory board in the system. With MEM-128, A10 and A11 are pre-wired as inputs from the ROM Simulation Module, or address cable if no ROM Simulation is used. In this case, A10 and A11 on the Address Probe should not be plugged in. This reduces address line loading. When MEM-32s are used, A10 and A11 are sourced from the Address Probe.

A10 and A11 source selection can be modified at any time through Wiring options on the Trace board:

3.6.2.2 ADDRESS INPUTS (CONTINUED)

1T-4 to 1T-2, A10 from ROM module
1T-4 to 1T-6, A10 from Address Probe
1T-3 to 1T-1, A11 from ROM module
1T-3 to 1T-5, A11 from Address Probe

NOTE: ALL UNUSED ADDRESS INPUTS MUST BE GROUNDED

Example: If the control store of the target processor only has addresses A0-A9 connected up, then address inputs A10 through A15 on the Address Probe must be grounded. The Trace board uses two sixteen bit comparators to generate the address breakpoint. If unused upper order address bits are not grounded, then no breakpoints will be generated.

3.6.2.3 DATA INPUTS

Sixteen data inputs are provided on two Data Probes. All inputs are TTL compatible and exhibit high impendance characteristics as shown on figure 3.6.1. These inputs are optional and need not be used. Each group of eight data inputs is strobed directly into a data register. To optimize timing, the data register is located within the data probe. The strobe signal used to latch the data is derived from the UDC input. The data should be stable prior to the clock input.

3.6.2.4 QUALIFIER INPUTS

Two qualifier inputs TQ1 and TQ2, are provided to extend triggering capability. These inputs are located on the Address Probe. As shown in figure 2.1 these inputs offer negligible DC loading to the circuit and provide a controlled dynamic input impedance of 100 ohms. As in other Trace input signals, the qualifier inputs are synchronously latched. Either the UAC or UDC can be used as the reference clock source. Switch S12 determines the clock source for TQ1 and S34 for TQ2 as shown in figure 3.6.3. True polarity, positive or negative, for the qualifier inputs can also be individually selected using switches S4 and S5 (figure 3.6.3).

3.6.2.5 EXTERNAL ENABLE

The External Enable, EE, signal is provided to allow the operator to directly control Trace data capture. When this signal is logically true, data is captured in the normal fashion. When logically false, no new data is captured until the signal goes true. True polarity, negative or positive is set using switch S6 (figure 3.6.3)

> *NOTE: If the external enable function is not being used, ground the EE line and set S6 on (negative enable).*

The EE signal is located on the Address probe and is fully buffered. Timing requirements are given in section 3.6.4.

3.6.2.6 USER CONTROL LATCH SIGNALS

Two user control latch input signals, UCTL1 and UCTL2, are provided on the Trace data probes for use with the system Examine State (XSTATE)™ command. These inputs are optional and do not affect other trace functions when XSTATE™ is not in use. UCTL1 is present on the least significant data probe and UCTL2 on the most significant data probe. UCTL1 is a positive true signal which causes the XSTATE™ routine to move the last sampled data from the data probes to the display. UCTL2 is a positive true signal used as a "done" input causing the XSTATE™ routine to terminate.

3.6.3 TRACE OUTPUTS

Two signal outputs are available to provide Trace status. They are Trace Triggered, TGD, and Trace Done, TD. The Trace Triggered signal is a positive true signal which becomes true two clock cycles after the trigger conditions have been properly satisfied. The signal remains true until Trace is re-armed from the front panel. TGD can be used to trigger an external logic analyzer, a storage oscilloscope, or other device and is available on the left-most BNC of the Trace board. The PC board uses the label TGD to identify the left BNC.

Trace Done (TD) is a positive true signal (some older systems prior to STEP-3 provide a negative true signal limiting its utility), which indicates the completion of a Trace Capture. Depending upon the actual trigger equation picked, the signal becomes true 2 to 7 clock cycles after trace completion. This signal, available on the right-most BNC, labeled TD, can be used to halt the processor for further examination. This is done by connecting the TD output to the external halt (EXT HLT) input BNC. In order to restart the processor, Trace must be ARMed or the Disable command executed.

3.6.3 TRACE OUTPUTS (CONTINUED)

NOTE: As with any EXT HLT stop, the CRT will still show RUNNING or MON RUN, but the cessation of clocks can be inferred from the fact that addresses stop changing.

3.6.4 AC SPECIFICATIONS

Setup time from clock edge (ns):

	CLOCK EDGE NEGATIVE		CLOCK EDGE POSITIVE		REFERENCE CLOCK
	TYP	MIN	TYP	MIN	
Data	25	30	20	25	UDC
Address	25	35	20	30	UAC
EE	30	45	25	40	UAC & UDC

Minimum clock width (high or low: 25ns)

Trace cycle time: 90ns guaranteed, 80ns typical

3.6.5 EXPANDED TRACE

Trace data capture width may be extended to a maximum of 80 bits wide by inclusion of optional Trace Expander hardware. Three additional data probes are required and are identical to the data probes described earlier. Trace expander functions as a slave to existing Trace hardware and is installed in the next available slot above or below the Trace 32 bit hardware. A single interconnect signal is required between them to synchronize timing. This signal, (TME) is jumpered between 3T-4 on the Trace hardware and 1T-4 on the Trace Expander with a paired ground on 3T-2 and 1T-2. A convient jumper is provided with each expander for this purpose.

FIGURE 3.6.1 - TRACE INPUTS

Signal Name	Signal Definition	Signal Loading
PROBE 1	ADDRESS	
GND	Ground input for probe	-
UAC	User address clock	30pf, 100 µa, -400 µa low
VCC	Power input for probe	5±.25 volts, 150ma
Q1	Qualifier input 1 (used in trigger equations)	100 ohms, 2ma
Q2	Qualifier input 2 (used in trigger equations)	100 ohms 2 ma (logic "0")
A10 thru A15	Most significant address inputs; Should be grounded if not used	100 ohms, 50µa
EE	External Enable; used to inhibit trace action.	30pf, 100 µa, -400 µa low
PROBE 2	DATA	
GND	Ground input for probe	-
UDC	User data clock	30pf, 100 µa, -400 µa low
VCC	Power input for probe	250 ma
D0-D7	Least significant data input (D0 is LSB)	30pf, 50 µa, -250 µa low
UCTL1	User control latch 1	30pf, 50 µa, -2ma low
PROBE 3	(DATA)	
GND	Probe ground	-
UDC	User data clock 2	30pf, 100 µa
VCC	Probe power	5±.25 volts, 250 ma
D8-D15	Most significant data input (D15 is MSB)	30pf, 50 µa
UCTL 2	User control latch2	30pf, 50 µa -2ma low

FIGURE 3.6.2 TRACE INPUTS USING RIBBON CABLE

DATA PROBE

Signal	Pin # [1,2]		Pin # [2]		Signal (LSB)	Signal (MSB)
GND	1	(1)	(2)	0	GND	GND
GND	3	(3)	(4)	2	UDC	UDC
GND	5	(5)	(6)	4	5 Volts	5 Volts
GND	7	(7)	(8)	6	UD0	UD8
GND	9	(9)	(10)	8	UD1	UD9
GND	11	(11)	(12)	10	UD2	UD10
GND	13	(13)	(14)	12	UD3	UD11
GND	15	(15)	(16)	14	UD4	UD12
GND	17	(17)	(18)	16	UD5	UD13
GND	19	(19)	(20)	18	UD6	UD14
GND	21	(21)	(22)	20	UD7	UD15
GND	23	(23)	(24)	22	UCTL1	UCTL2
Not Present	25	(25)	(26)	24	Not Present	Not Present

ADDRESS PROBE

Signal	Pin # [1,2]		Pin # [2]		Signal
GND	1	(1)	(2)	0	GND
GND	3	(3)	(4)	2	UAC
GND	5	(5)	(6)	4	5 Volts
GND	7	(7)	(8)	6	TQ1
GND	9	(9)	(10)	8	TQ2
GND	11	(11)	(12)	10	A10
GND	13	(13)	(14)	12	A11
GND	15	(15)	(16)	14	A12
GND	17	(17)	(18)	16	A13
GND	19	(19)	(20)	18	A14
GND	21	(21)	(22)	20	A15
GND	23	(23)	(24)	22	EE
Not Present	25	(25)	(26)	24	Not Present

NOTES: 1 Pin 1 Removed For Keying

2 Pin Numbers shown are marked on documentation and probe PC board. Numbers in parantheses refer to 3M number system.

3 Suggested interconnect cable 3M#3365/26, 6-12 inches
Suggested termination, probe pod end 3M#3399-0000
keyed location 1, 25, 26 with 3M#3435

FIGURE 3.6.3 TRACE SWITCH OPTIONS

SWITCH	DESCRIPTION	UP (ON)	DOWN (OFF)
S1	Selects active edge of address clock	Positive-Going	Negative-Going
S2	Selects active edge of LSB data clock	Positive-Going	Negative-Going
S3	Selects active edge of MSB data clock	Positive-Going	Negative Going
S4	Selects true polarity of TQ1 input	Positive True	Negative True
S5	Selects true polarity of TQ2 input	Positive True	Negative True
S6	Selects Enable polarity of EE input	Positive Enable	Negative Enable
S12	Selects clock source for TQ1	BDC*	BAC *
S34	Selects clock source for TQ2	BDC*	BAC *

*DEFINITIONS:

BDC - Buffered Data Clock - Derived from the UDC (User Data Clock) of the LSB Data Probe of the basic 32-bit Trace Board, active edge chosen by S2 above.

BAC - Buffered Address Clock - Derived from the UAC (User Address Clock) on the Basic 32-bit Trace Board, active edge chosen by S1 above.

Both signals are buffered in their respective probe modules (orange boxes).

3.7 MAINFRAME

3.7.1 SYSTEM ORGANIZATION

The system consists of six to 15 major units, each of which performs an integral function within the STEP instrument. The block diagram shown in figure 3.7.1 provides an over view of the system organization. A particular STEP instrument may consist of 1 to 10 Writable Control Stores, one or two Trace boards, a Speed-Test board, and ROM Simulation cables. The following paragraphs discuss the function of each functional unit shown in figure 3.7.1.

3.7.1.1 CHASSIS AND BACKPLANE

The STEP-2 backplane acts as a communication link between as many as eight PCB modules. Three of the six slots* in the backplane are dedicated to the instrument. Slot 0 (bottom slot) is dedicated to the microcomputer board, slot 1 is dedicated to the CRT keyboard and slot 5 is dedicated to the microcomputer memory or the Trace Logic Analyzer.** Some modules are slot dependent and restricted as to placement in the card cage; however, all WCS models are independent of position in the backplane. The only constraint placed upon WCS modules in that modules within a single array must be placed in contigous (adjacent) locations in the backplane.

*Eight slots in STEP-3; six in STEP-2.

**Slot 5 in STEP-2; slot 7 in STEP-3.

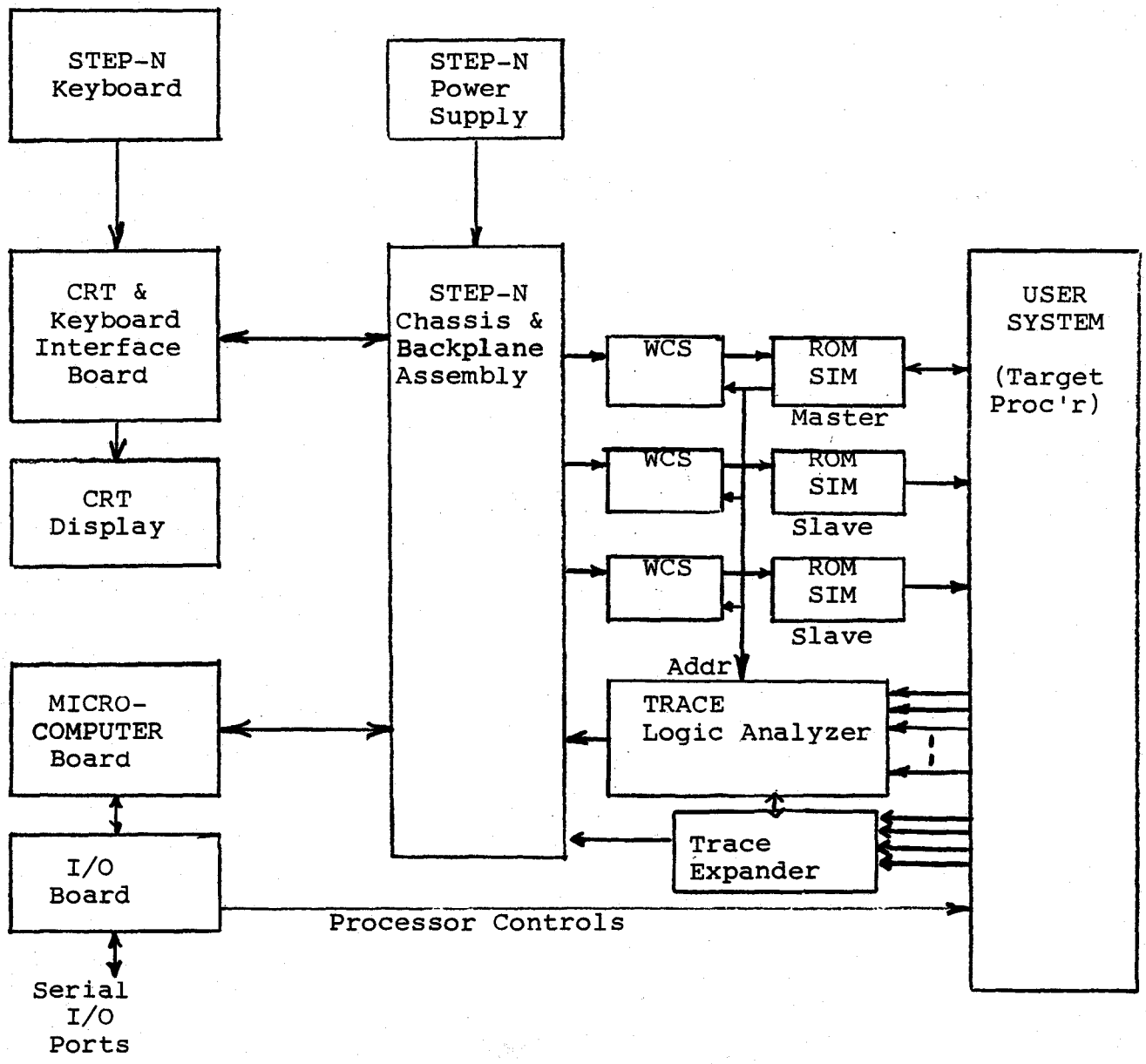


Figure 3.7.1 STEP Instrument Organization and Functions

3.7.1.1 CHASSIS AND BACKPLANE (CONTINUED)

Use of the basic six-slot backplane provides considerable flexibility in system design for specific applications. For example, the total WCS memory capacity may be expanded in either of two ways. One, a series of up to three* MEM-128 modules may be installed to provide up to 4k x 96 WCS capacity at a small penalty in speed. Second a backplane extender board may be used to provide a communication path to an extender option containing up to three* more MEM-32's or MEM-128 modules.

3.7.1.2 MICROCOMPUTER MODULE

The microcomputer module provides control of the entire STEP-N instrument. It contains an 8080A microprocessor chip, 1k of slow speed static RAM and the first 7k of program store in EPROM. The microcomputer board also contains an asynchronous communication interface, data I/O buffers, interrupt control logic and hardware interval timers used within the STEP-N instrument.

Functionally, the microcomputer module controls all operator interface functions through the CRT/keyboard and serial I/O ports. In comparison to WCS and user system speeds the microcomputer board is slow speed. Therefore, the 8080A-based CPU never is involved in the target interface, but functions to control data manipulation, editing, and machine initialization at non-real time speeds outside the user's system.

*2 more in STEP-3

3.7.1.2 MICROCOMPUTER MODULE (CONTINUED)

When the user enters the command RUN, none of the 8080A controlled data functions are in series with high speed data paths. At run time the CPU module samples and reports status on the CRT display. As will be described later, all real-time data-path and control functions are implemented in highspeed bipolar logic, to insure a valid real-time test of the user's microcode.

3.7.1.3 CRT/KEYBOARD INTERFACE MODULE

The CRT/keyboard interface module provides interfacing between the keyboard assembly, CRT assembly and the microcomputer module used in STEP-N. This module provides character generation, and display refresh timing. It also buffers the keyboard interface signals to the microcomputer module.

The CRT interface circuitry develops a 7 x 9 dot-matrix character output as TTL video information with corresponding TTL vertical and horizontal syn information. Composite video output is also developed to drive the system CRT assembly, and optionally an external NTSC video monitor. There are 64 possible character functions available including alphabetic, numeric and punctuation. Character blink, reverse video, cursor control and screen format for the eight lines of 32 characters each are controlled in hardware implemented on the CRT interface module. This module contains a display buffer which updates the display at a rate of 60 times per second. Communication between the microcomputer module and the display buffer is accomplished by the CRT interface circurity which generates an interrupt request to the 8080 CPU at the start of vertical retrace

of the CRT. Data to be displayed is written to the display buffer in response to the interrupt request, and thus does not disturb the CRT display's stability.

3.7.1.4 CRT MODULE

The CRT display module provides a fully solid-state display unit (except CRT) for display of data and operation/command interaction. The CRT module receives a composite video input, from the CRT/keyboard interface module, which combines video information (blanking pulses) with horizontal and vertical sync pulses. The video information removes blanking from the CRT at the proper intervals to present a display on the CRT. The CRT itself is a magnetic deflection type with integral implosion protection. The CRT assembly has several controls which are provided for maintenance and initial factory adjustments to produce a proper picture. See Section 4 for a description of the adjustments available.

> *NOTE: Improper adjustment may result in damage to the CRT. Only qualified personnel should be allowed to attempt modification of CRT adjustments.*

3.7.1.5 KEYBOARD ASSEMBLY

The keyboard assembly contains 60 individual key switches to provide entry of alphanumeric characters and various control functions. The keyboard is strobed from interface circuity on the KBD/CRT interface module, which employs an 8 x 8 matrix scanner. Control of the scan operations of the key matrix is from system software on the micro-computer module.

3.7.1.5 KEYBOARD ASSEMBLY (CONTINUED)

A hexadecimal keypad is located on the right section of the keyboard for input of data. An ASCII keypad in the center of the cabinet allows easy command entry and communication with external devices such as computers and storage devices. The ASCII keypad allows the STEP-N instrument to function as a limited terminal. This facilitates down-loading operation from a wide variety of host machines.

Since the numeric characters on the ASCII section of the keyboard are in fact redundant duplicates of those on the hex keypad, these keys have been dedicated to a set of selected ASCII control characters to enhance the STEP-N communications capabilities. A chart of ASCII characters generated by STEP-N is given in Appendix D.

The capability of STEP-N to function as a video terminal provides a powerful, general purpose ability to coordinate STEP-N functions with a large array of host processes. However, the STEP-N instrument is <u>not</u> intended as a entry text terminal device to large computer systems.

Users should plan on text entry for file manipulation and meta-assembler operations to be performed via a standard garden-variety terminal on their system. While the STEP-N instrument has the capability to perform text entry functions, many readily available and inexpensive terminal devices will prove more cost-effective for that purpose.

3.8 STEP STANDARD OBJECT FILE FORMATS

3.8.1 INTRODUCTION

This document defines the STEP-N standard for object files produced and loadable by the STEP Engineering Firmware Integration and Test Station. Regardless of which of four available formats is chosen, the object file format is a hexadecimal representation of the binary data coded into ASCII. The ASCII standard is defined in the document titled: American National Standard Institute, Code for Information Interchange, X3.4-1968.

The available formats include three PROM-oriented formats GENPROM ™, ASCII-HEX, and BNPF; and STEP's word-oriented MICROWORD ™ format. These four are supported by STEP firmware and also by the STEP meta-assemblers, TMA and MACRO-TMA. (Software has separate manuals.)

3.8.1.1 ASCII HEX -- USED IN BOTH GENPROM ™ AND MICROWORD ™ FORMATS

The ASCII HEX representation requires twice as many bytes of ASCII characters as the straight binary file. For example, the 8-bit binary value Ø1Ø1ØØ11 is 53 in hexadecimal. To code this in ASCII HEX, the first byte would contain the ASCII code for 5 (35) and the second byte would contain the code for 3 (33). Thus, every representation of 8-bit data is 2 successive ASCII characters.

Since ASCII characters require only 7 bits, the highest order bit may be used by some routines as a parity bit of each 8-bit byte. However, since checksum and the compare function are included in the STEP-N capabilities, the highest bit of each data word is masked off as the

3.8.1.1 ASCII HEX -- (CONTINUED)

incoming ASCII characters are converted to binary. Also, STEP-N does generate parity bits on records created.

3.8.2 MICROWORD ™ FORMAT

The preferred format used for downloads to STEP-N is a modified memory image, blocked into discrete records with length equal to one word. WORD is defined to be one-user memory location and may be from 8 to 96 bits in width, as defined by the STEP-N setup procedure. While loading data, record length is contained in the record header (defined below) and must agree with the current machine parameters or else an error is generated. Widths between 97 and 192 use both STEP-N arrays.

In cases where the micro-word width is an odd number of nibbles, the most significant byte of the data word is prefaced with four "Ø" bits, to ensure that data records always contain a whole number of bytes.

Each record starts with a record mark and header consisting of length, type, and memory address (in user memory space) and is followed by a trailer consisting of two checksum characters. STEP-N ignores any characters such as (CR)/ (LF) or nulls either preceding the record mark or following the checksum. When creating files STEP-N inserts a (CR)/NULL following the checksum of each record and (LF) prior to each colon.

3.8.2 MICROWORD ™ FORMAT - STEP-N

A frame-by frame description of the STEP MICROWORD ™ record follows:

Frame Ø	Record Mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1,2 (Ø-9,A-F)	Record Length. Two ASCII characters representing a hexadecimal number in the range Ø to 'FF'H (Ø to 255). This is the range of actual data bytes. A record length of Ø indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the memory location where the data following will be loaded. The data is stored in the location pointed to by the load address.
Frames 7,8	Record Type. Two ASCII characters. Currently data records are type Ø and the end record is type 1, Ø length.
Frames 9 to 9+2* (Record Length)-1	Data. Each 8 bits of memory is represented by two frames containing the ASCII characters (Ø to 9, A to F) to represent a hexadecimal value Ø to 'FF'H (Ø to 255). These proceed from MSN to LSN up to the record length.
Frames 9+2* (Record Length) to 9+2* (Record Length)+1	Checksum. The checksum is the negative (two's complement) of the sum of all 8-bit bytes (decoded from the ASCII characters) in the record since the record mark (":") evaluated modulos 256. That is, if you add together all the 8-bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: IF memory locations 1C4Ø through 1C42 contain 32-bit data of 53F8 EC4Ø
1111 2222
3333 4444
the hex file produced (including control characters) would be:

LF :041C400053F8EC4029 CR NULL
LF :041C41001111222239 CR NULL
LF :041C420033334444BØ CR NULL
LF :ØØØØØØØ1FF CR NULL

3.8.2.1 BNPF OBJECT FILES FOR TTY PUNCH - (STEP-2 OUTPUT FILE FORMAT ONLY, OPTIONAL)

The BNPF object code uses the ASCII characters N and P to represent the actual binary digits Ø and 1, respectively. An ASCII "B" indicates the beginning of a byte, an ASCII "F" indicates the end of the byte. All characters following the F are ignored until another B is encountered. This allows comments and characters that do not contain the character B to appear between bytes to data in BNPF format.

Ten bytes (frames on paper tape) are required to represent one byte of data. For example, the byte containing the value ØØ11 1111 (3F in hexadecimal) would be represented as follows in BNPF:

BNNPPPPPPF

Exactly eight characters occur between the B and its following F. No character other than N or P is used between the B and the F.

A BNPF object file may contain either 8-bit or 4-bit data but not both. In the case of 4-bit data, only the high-order or low-order 4 bits are punched. For ease of reading, STEP-2 inserts 4 spaces following each F and a (CR) / (LF) after each 4 bytes of data. Also, prom location number, always starting with ØØØØ, are inserted to allow easy examination of the TTY listing.

3.8.2.2 ASCII HEX SPACE PROM IMAGE FILES (STEP-N)

The ASCII HEX SPACE PROM image object file format is another format which represents data as ASCII characters (as described earlier under ASCII HEX). The difference is that this format contains either 4 or 8 bit data in continuous ascending addresses rather than a word at a time with addresses contained within the data record. The ASCII "space" character is used as a delimiter between data bytes.*

Files produced begin with a leader consisting of a carriage return (CR), a null, and a line feed (LF) followed by 32 null characters and 32 rub-outs. The ASCII character STX, indicates the beginning of actual data. Following the STX start character, any ASCII characters may be contained in the record up to the first space; the two characters following the space are the first data byte. The data stream continues with more spaces followed by data bytes until the ETX character, which is the end of record mark. When files are produced by STEP-2, a trailer of 32 rub-outs and 32 nulls is appended to the end of the record.

An ASCII HEX SPACE file may contain either 8 bit or 4 bit data, but not both. In the case of 4 bit data, the high order nibble is extraneous. Data files produced with 4 bit data from STEP-2 set the high order nibble to ØH. For ease of listing STEP-2 inserts a CR/null/LF after each 16 bytes of data. Figure 1 illustrates the ASCII HEX SPACE format.

*NOTE: *GENPROM™ is a superset of this, with programmable header, frame and end characters. (ref. 2.5.7)*

FIG. 1

ASCII HEX SPACE FORMAT

RECORD	DESCRIPTION
CR NULL LF	For ease of listing
NULL . . NULL	32 nulls in leader
RUBOUT . . RUBOUT	32 rubouts in leader
STX	Start of text
CHR CHR SPACE CHR . .	Contents of memory at specified position through number of locations
ETX	End of data
RUBOUTS	32 rubouts in trailer
NULLS	32 nulls in trailer

NOTE: A CR/null/LF is inserted after 16 data characters for easy listing.

3.9 SPEED TEST HARDWARE INTERCONNECT

3.9.1 GENERAL

The Speed-Test option expands the Self testing capability of the STEP-3 when using the test command function. The additional tests available are described in section 2.2.4. The hardware consists of a P.C. board, a set of cables for address and data lines, and a breakpoint cable.

3.9.2 P.C. BOARD INSTALLATION

The Speed-Test board replaces the system memory P.C. board in the STEP-3. If the option is purchased initially, the STEP-3 is shipped with the Speed-Test P.C. board installed in slot 7, the top slot of the card cage. Address, Data, and Breakpoint cables are provided.

If the Speed-Test option is purchased seperately, the user must remove the system memory P.C. board from slot 7 and insert the Speed-Test P.C. board. The following steps should be followed:

1. Turn power off.
2. Remove the side panel.
3. Remove the system memory P.C. board.
4. Insert the Speed-Test P.C. board.

CAUTION: Normally, moderate force is required to fully seat a P.C. board into the card cage. Make sure that the back plane pins are correctly seated into the P.C. board connector before applying inordinate pressure.

5. Replace the side panel.

3.9.3 CABLE INTERCONNECT

The cables are used to connect the Speed-Test P.C. Board to the memory P.C. board under test.

1. Data lines are connected through two 40 conductor ribbon cables. One connects MSB data from the memory P.C. board to J11 of the Speed-Test P.C. board. The other connects LSB data to J12 of the Speed-Test P.C. board. Each Speed-Test P.C. board connector is directly above the corresponding memory P.C. board output, so, when connected, the cables should lie flat and be perpendicular.

2. Address lines are connected through a 26 conductor flat cable using a 26 position connector on one end and a 40 position connector on the other. The 26 position end is connected to the Address inputs of the memory P.C. board under test. The 40 position end is attached to J10 of the Speed-Test P.C. board.

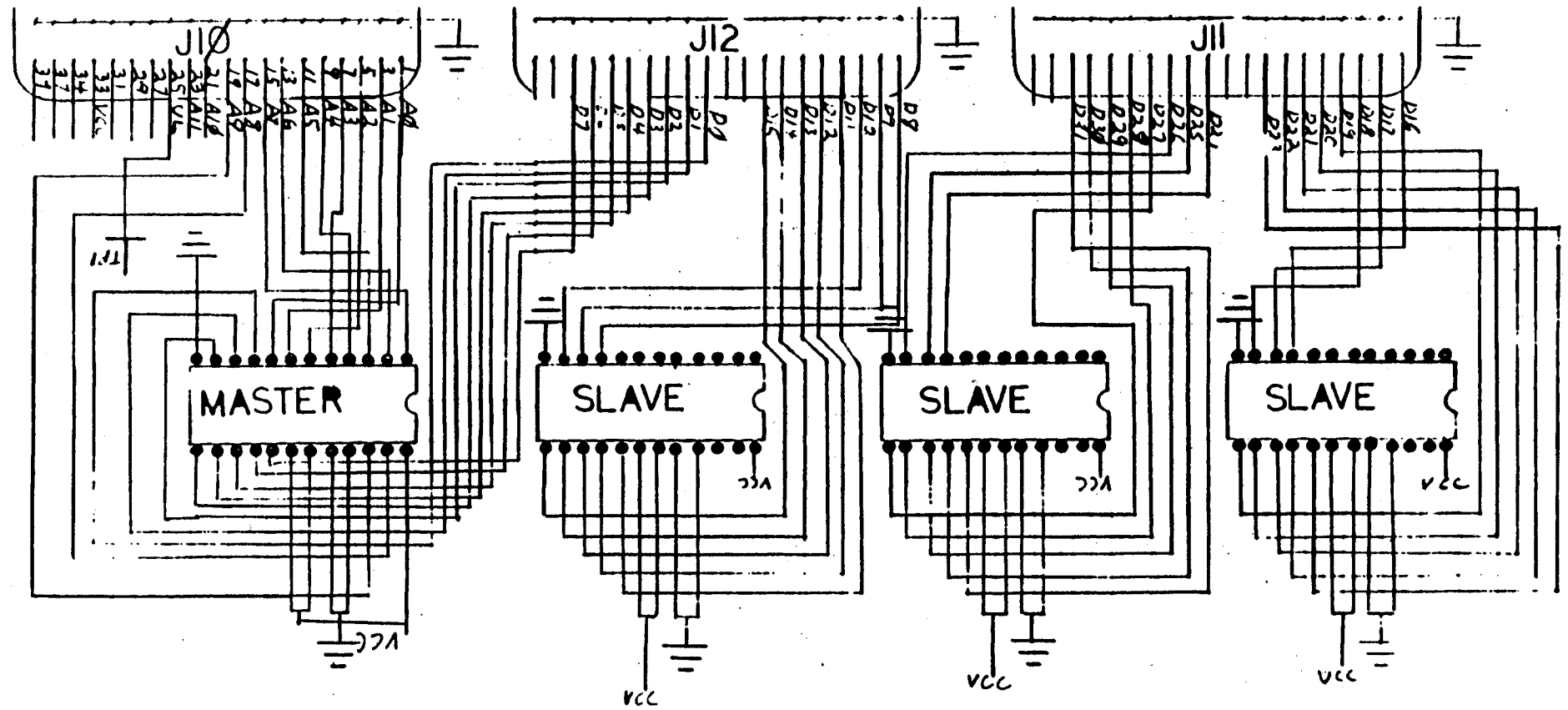
3. The breakpoint cable is a single insulated wire with a male BNC connector on each end. Make the breakpoint interconnect by connecting this cable between the breakpoint BNC connector on the Speed-Test P.C. board and the breakpoint BNC on the memory P.C. board.

3.9.4 ROM SIMULATION SPEED-TEST INTERCONNECT

ROM Simulation cables may be included in all memory Speed-Tests by using purchasable option P.G. board* hardware. This consists of a universally adaptable P.C. board with connectors to plug directly into the Speed-Test P.C. board edge, J10, J11, and J12.

The interconnection is accomplished by installing, on the P.G. board I.C. wire wrap sockets appropriate for the ROM under simulation. Data and address line connections are made by referring to the pin configurations of J10, J11, J12 on the Speed-Test P.C. board and the pin-out of the ROM under simulation. Figure 3.9.4 is an example of this for Speed-Test of any 512 x 8 ROM simulation.

*Play Ground P.C. board.


J10
J12
J11
MASTER
SLAVE
SLAVE
SLAVE
VCC
VCC
VCC
VCC
VCC

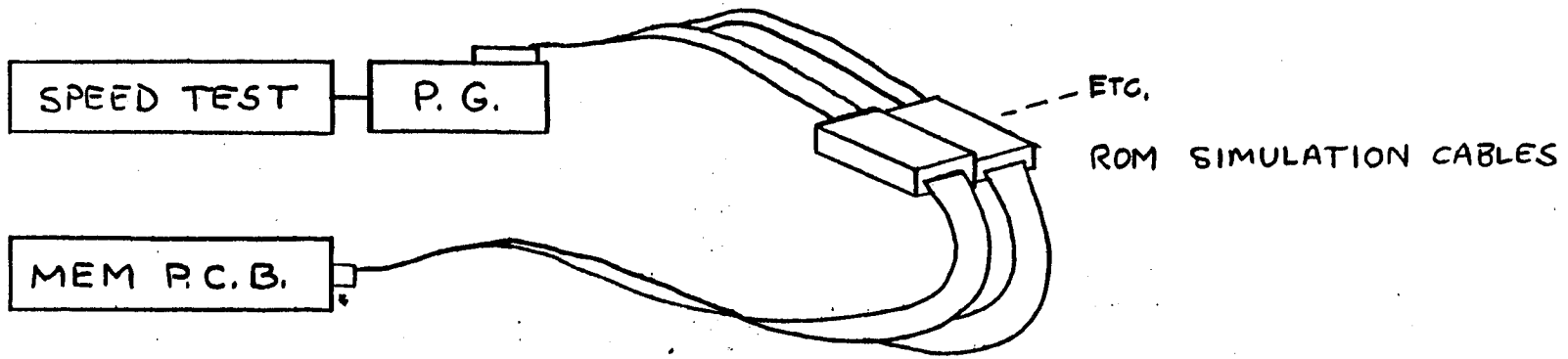

SPEED TEST
P. G.
MEM P.C.B.
ETC.
ROM SIMULATION CABLES

FIG. 3.9.4.

3.10 MAXIMUM CONFIGURATIONS FOR STEP-N AND EXPANSION BOX

3.10.1 GENERAL

The maximum size of WCS available to users is determined by two practical limits:

1. The physical number of slots available for inserting memory P.C. boards.
2. The memory organization required.

3.10.2 PHYSICAL LIMITATIONS

Within the STEP-N instrument any slot not occupied by machine function P.C. boards or purchased hardware options is available for WCS boards. To determine the number of slots available, subtract the appropriate total below from the total number of slots in the instrument.

CPU and CRT control	2 slots (required)
System memory or Speed-Test	1 slot
Trace, 32 bits	1 slot (option)
Trace Expander, 80 bits	1 slot (option)

Additional memory P.C. board slots may be obtained through the use of the purchasable option Expander Box. This provides up to five additional slots for Memory Expansion. Total expansion may be limited to four slots if Trace or Speed-Test is installed in the STEP-N instrument. This is true because an additional slot must be used to provide the interconnect to the expansion box back plane. Maximum configurations within the STEP-3 mainframe are; 5 WCS modules and system memory, 4 WCS, Trace, and Speed-Test, or 3 WCS, 2 Trace, and Speed Test.

3.10.3 MEMORY ORGANIZATION LIMITATIONS

Maximum boundry conditions for WCS organization within any array are given in Appendix B. In any case, the absolute maximum number of boards for any single array is six. Utilizing the expansion box systems may be configured to a maximum of 10 WCS modules.

3.11 XPORT AND WPORT HOOKUP

Connection to the Speed-Test board edge for XPORT and WPORT operation requires only standard to position edge connectors. (3M part number 3464 or equivalent.)

Section 2.4.4 explains pinouts and signal assignments.

SECTION IV

MAINTENANCE AND TROUBLE SHOOTING

4.0 GENERAL

This section contains general information for user level trouble shooting of the STEP-N. WCS trouble shooting is based on testing using the test command function and the Speed-Test purchased option. Further assistance is available through Step Engineering factory service:

Inside California:	(408) 733-7837
Outside California:	(800) 538-1750
TWX:	(910) 339-9506

4.1 ROUTINE CHECKS AND PREVENTIVE MAINTENANCE

Step recommends that the setup and operational checkout contained in section 1.3.2 be conducted upon receipt on the instrument and, additionally, prior to the beginning of any new application. Also recommended:

1. Conduct the checksum and WCS tests available using the test command.
2. Check and adjust Vcc to 5.0 volts.

4.1.2 POWER SUPPLY ADJUSTMENT

The power supply 5.0 volts is adjusted using a small trimmer potentiometer located on the right hand end of the power supply. It is accessable through a hole in the power supply cover. The measurement is made on the front left hand edge of the WCS P.C. lowest in the card cage. Use the breakpoint BNC connector shell as logic ground reference. 5.0 volts is measured from the right hand lead of the resistor located just behind the breakpoint BNC connector. (Figure 1.4.1.3)

4.2 MAINFRAME TROUBLE SHOOTING

The following are indications of a problem in the STEP-N mainframe:

1. Power switch on, but no lights or display.
2. Power on, but no display.
3. Power on, display flashing random characters.
4. Power on, display correct, but characters doubling.
5. Commands not executed properly.
6. CRT display too dim, unsyncronized or jittery.

The following describes probable causes for each of these:

4.2.1 PROBLEM CAUSES

Power switch on, but no lights or display: Check if cooling fans are running. If they are not, then A.C. power is not reaching the machine. Check the fuse located in the A.C. filter in the rear of the instrument next to the power cord. Check for proper and firm seating of the power cord in the plug on the A.C. filter. Check line voltage.

If the fans are operating, the power supply is not functioning. Check for loose connections on the supply.

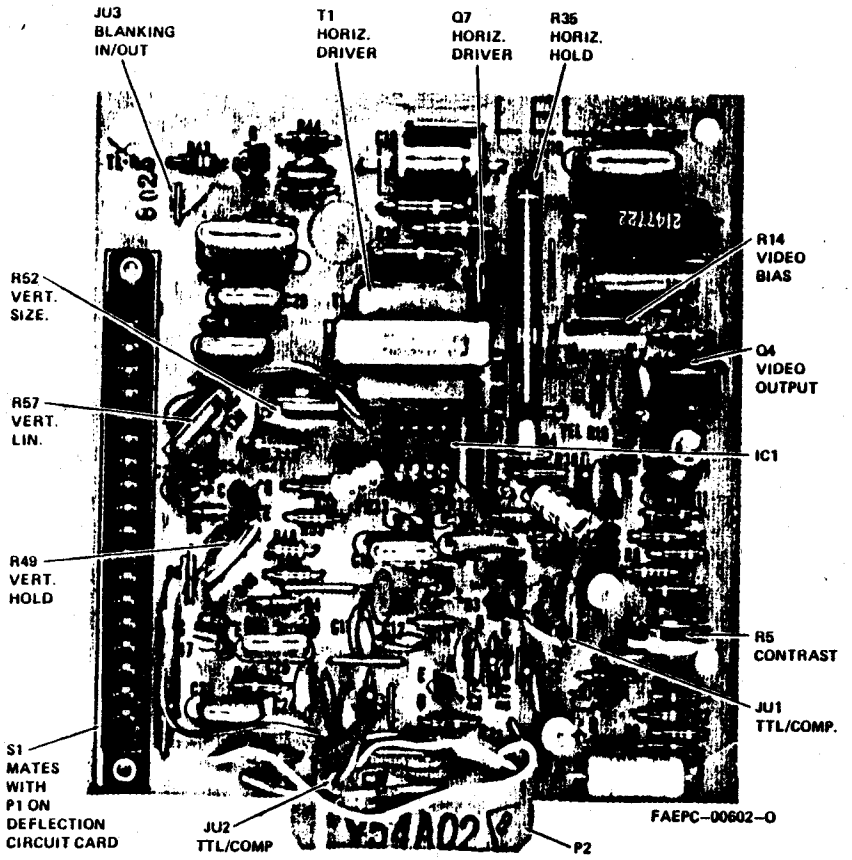
WARNING: Shock Hazard. Remove the instrument from the A.C. power source before touching any power supply connections.

The only user repairable power supply component is a 5.0 amp fuse located inside the power supply. It is necessary to remove the power suppply from the instrument and remove the cover to check this fuse. If the fuse is intact, the supply must be replaced.

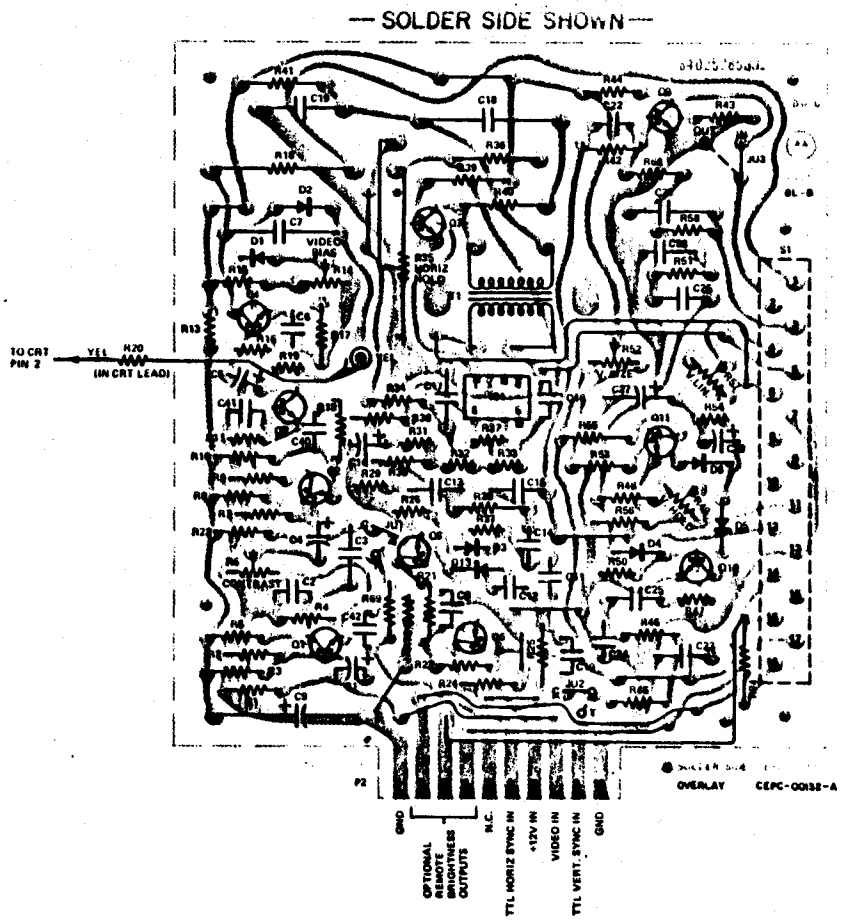
NOTE: A blown fuse in the power supply may indicate a short on one of the secondary voltage busses. Before attempting further operation check the 5.0 volt, + 12.0 volt, and -12 volt secondary lines for shorts.

4.2.2

Power on, but no display: Check that CRT video cable (coax) is connected to CRT controller board edge and to the CRT display at the CRT display connector. Adjust video output and contrast controls located on the display P.C. board. (figure 4.2.1)



Signal Circuit Card – Component Side (All Models except M1000–190)



Signal Circuit Card – Solder Side (All Models except M1000–190)

Figure 4.2.1

4.2.2 POWER ON, BUT NO DISPLAY (CONTINUED)

WARNING: *Shock Hazard. Use non-conductive adjustment tools for any adjustment on CRT display. Do not touch any portion of the CRT display circuitry.*

4.2.3 POWER ON, DISPLAY FLASHING RANDOM CHARACTERS

Power on, display flashing random characters: The system firmware is not operating. The most common reason is one or more of the system memory EROMS is not seated in a socket. This is most likely to occur during transportation or shipment which can unseat EPROMS or backplane connection due to shipping vibration. The EROMS are located on the CPU board (slot 0), and the system memory or optional Speed-Test board, if installed (slot 7 on STEP-3). (The upper system memory may be located on the optional tract board on STEP-2.) Remove and reseat all EROMS in sockets. Try operating the instrument with only CPU (slot 0) and CRT controller (slot 1) P.C. boards installed. If this corrects the problem, insert other P.C. boards one at a time until either the faulty board is discovered or all boards are installed.

NOTE: *Turn power off when inserting P. C. boards.*

4.2.4 POWER ON, DISPLAY CORRECT BUT CHARACTERS DOUBLING

Power on, display correct but characters doubling: The character generator I.C., DM8678BTK/N, is bad. This is located in the center of the CRT controller P.C. board. (slot 1).

4.2.5 COMMANDS NOT EXECUTED PROPERLY

Commands not executed properly: Possibly one or more system memory locations are altered. Check this by running TEST 4 of the test command function. This calculates the checksum values of the EROMS present in system memory. Compare this display with the checksums

4.2.5 COMMANDS NOT EXECUTED PROPERLY (CONTINUED)

printed on the label on the base of the machine. Any mismatch indicates a defective memory. This is correctable by obtaining new programmed system firmware from Step Engineering.

4.2.6 CRT DISPLAY TOO DIM, UNSYNCHRONIZED, OR JITTERY

CRT display too dim, unsynchronized, or jittery: This may be adjustable to correction. Intensity and synchronization are adjusted by potentiometers on the CRT display P.C. board, refer to Figure 4.2.1.

> *WARNING: Beware of high voltages present within CRT display. Use non-conductive adjustment tools.*

Non-synchronization or jitter may be corrected by adjustment of C35 on CRT controller P.C. board (slot 1). Refer to drawing 082015C, section V, for C35 location; Figure 4.2.2 for explaination of all CRT adjustments.

Brightness Control - The brightness control adjusts the overall or average intensity of illumination, which determines the background level in the reproduced picture. The brightness control should be adjusted so that the background raster is barely visable, then backed off until the raster just disappears. Focus is affected to some extent as the brightness control is adjusted to provide the user with optimum viewing conditions.

Focus Control - The focus control allows adjustment for the optimum spot size (smallest and sharpest) display on the CRT screen. The Focus control should be adjusted to provide a desirable amount of line detail in the reproduced picture.

Contrast Control - The contrast control determines the difference in intensity between black and white parts of the reproduced picture, as distinguished from the brightness, which is the average intensity. The contrast control should be adjusted to provide a pleasing picture, with bright white and dark black for the extreme intensity values. The contrast control is affected by the brightness control.

Vertical Hold Control - The vertical hold control allows adjustment to eliminate vertical rolling of the picture. The vertical hold control should be rotated slowly until the picture locks in vertically.

Vertical Linearity Control - The vertical linearity control allows adjustment to provide equal spacing on either side of the center line. Linearity of the vertical scanning can be checked by observing crowding or spreading from top to bottom in the raster and picture.

Vertical Size Control - The vertical size control adjusts the vertical size of the displayed area used in displaying video information.

Horizontal Hold Control - The horizontal hold control allows adjustment to eliminate horizontal rolling of the picture. The horizontal hold control should be slowly rotated until the picture locks in horizontally.

Video Bias Control - The video bias control adjusts the intensity of illumination of the background on the CRT screen. The video bias control should be adjusted to eliminate the scanning lines and provide a desirable background for the reproduced picture. This adjustment is a factory adjustment and should not be made by the user.

Figure 4.2.2

4.3 I/O PORT TROUBLE SHOOTING

I/O port difficulties are persued by reference to error messages. Refer to Appendix C for error message explainations. The following general considerations apply:

4.3.1 I/O SETUP

The I/O setup must match the situation. This setup is part of the I/O command structure. (section 2.5). If specific setup parameters are not given, the instrument sets its own values by default. (section 2.5.1). If communication to a peripheral is being setup and the result is "COMM ERROR" at STEP-N or failure to respond at the peripheral, the following conditions should be checked.

1. Wiring interconnect between pin 2 (TX) and pin 3 (RX) on STEP-N and the pin 2 and pin 3 of the peripheral. If the peripheral is a modem type device, one-to-one correspondance is normally the case. If the peripheral is is a terminal type device, cross wiring between pin 2 and pin 3 is normally needed.
2. Check the number of stop bits at both ends of the link.
3. Baud rate.
4. Data polarity from peripheral
5. Short or open circuit in the interconnect wiring.

4.3.2

The halt line is a 50 OHM terminated line. When being driven by a gate from the user system, the gate must be capable of driving a 50 OHM load. If not, cutting one lead of the ½ watt, 51 OHM resistor on the I/O clock board is necessary. See Drawing number 0001054 in Section V for the resistor location.

4.3.3

On STEP-3 instruments shipped after November, 1980, TEST 3 in the test command structure is available for off-line verification of I/O port operation. Refer to the test command portion of section II for an explaination of TEST 3.

4.4 WRITABLE CONTROL STORE TROUBLE SHOOTING

User trouble shooting of the Writable Control Store is accomplished using the test command functions. The number of tests possible is increased using the purchased option Speed-Test hardware.

In general, all of the test programs do basically two kinds of operations while testing the memory. They are:

1. Read after write while initializing memory space for tests. If the read does not compare to the write then an error message and the data at time of failure is displayed.

2. Comparisons of data stored at one location with data stored and written at another location.

On detecting a failure each program displays an error message on line 2 of the display. These error messages should be considered a strong hint as to what has failed, but they are not a sure thing. Error displayed data normally appears as follows:

```
DATA ADDRESS =
DATA =
CODATA ADDRESS =
CODATA =
```

DEFINITIONS

DATA ADDRESS = Is the address currently being read or written when an error is detected. On machine side tests the address is in 8080 address space starting at address 8000H. On user port tests, the address is reported starting at 0000H.

DATA = Is the actual data read at failure. 8 bits on 8080 side; 32 bits on user port tests. See figure 4.4.1 for data and address locations.

4.4 WRITABLE CONTROL STORE TROUBLE SHOOTING (CONTINUED)

CODATA ADDRESS = CODATA stands for comparison data and is normally the complement of data read from memory. The address points to the memory location where data being compared against is stored.

CODATA = The comparison data currently being used.

NOTE: When errors are reported and CODATA ADDRESS is not in valid memory address space the test has failed on a non-comparison type test.

When errors are detected at a CODATA ADDRESS, it will equal the data address.

ERROR MESSAGES DISPLAYED AT VARIOUS TIMES

1. DATA BIT STUCK = 0
   DATA BIT STUCK = 1
   LIKELY ADDRESS X TALK
   CODATA TRASHED FROM LAST BLOCK
   WRITE AT CODATA ADDRESS FIELD
   STUCK DATA BIT
   MEM WRITE PROTECTED
   INCORRECT CARD TYPE
   LIKELY ADDRESS STUCK A0-A7
   LIKELY ADDRESS STUCK A8-A11
   ENABLE OUTPUT STUCK
   ENABLE SAMPLED INVALID
   ENABLE CONTROL STUCK
   SAMPLED ADDRESS INCORRECT
   BREAKPOINT FAILED
   USER STROBE FAILED
   FAILED AT CODATA ADDRESS
   FAILED AT DATA ADDRESS

4.4.1

The following general considerations apply:

1. If a few bits are being dropped, check and adjust the power supply for 5.0 volts Vcc at the WCS board edge. (see 4.1.2)

2. If the data is good on the instrument display, but not on the user side port:

   a. The memory orginization switches on the WCS P.C. board may not be set properly. (section 3.1.2.2)

b. The bi-directional octal buffers, 74S240, may be damaged. Replace. Consult drawing 0001114 for I.C. location.

NOTE: *Damage to the 74S240's is usually caused by turning off the host processor before returning to top command mode in the STEP-N.*

3. Any bit dropping difficulty may be attributable to a bad RAM in one or more memory locations. Refer to Figure 4.4.1 for locations of data in RAM. Switching I.C.'s in a logical manner will verify the faulty I.C.

4. Another general cause of bit dropping is high operating temperature within the Instrument. Check for proper fan operation, fan obstructions, and free access and exit of cooling air. With large WCS arrays and higher ambient temperature operating conditions, normal instrument coling should be augmented by external cooling.

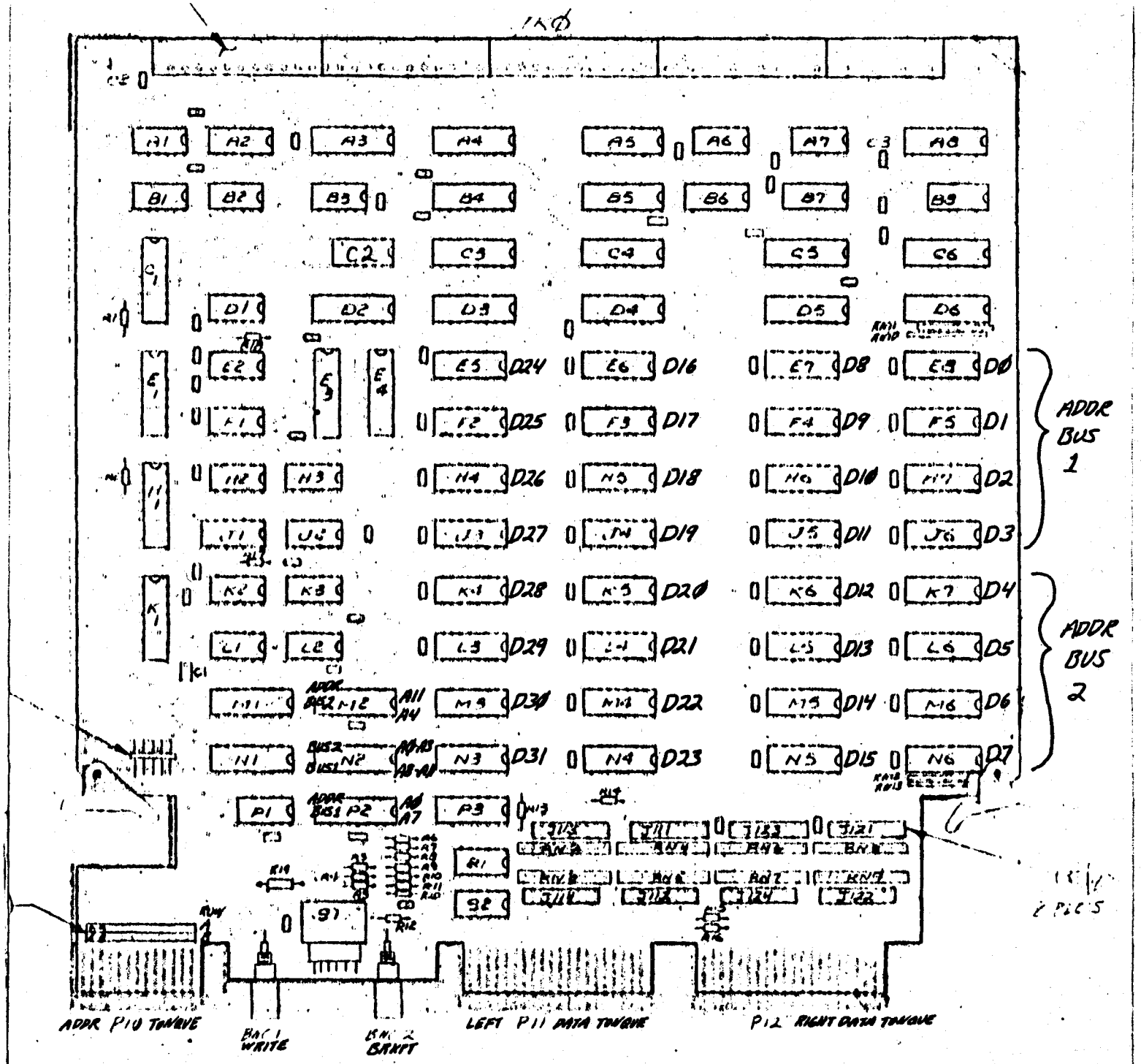

ADDR BUS 1
ADDR BUS 2
ADDR P10 TONGUE
LEFT P11 DATA TONGUE
P12 RIGHT DATA TONGUE

Figure 4.4.1

4.5 TRACE TROUBLE SHOOTING

Refer to figure 4.5.1 for a summary of common symptoms, their cause, and recommended corrective action.

4.5.1

If bit dropping in captive memory is occurring, one or more bad RAMs may be the cause. Logical RAM switching should isolate which RAM. Refer to figure 4.5.2 for address locations in the RAM I.C. array.

TRACE TROUBLESHOOTING

SYMPTOM	PROBABLE CAUSE	CORRECTIVE
Random Data in Trace Address Memory	* Trace not enabled * No Trace Address Clock * Address probe VCC or GND not present	Check EE Check Clock connection Check VCC, Ground connections
Random data in trace data memory, but address memory is correct	* No trace data clock * Data probe VCC or GND not present	Check clock connection Check VCC, Ground connections
Trace not completing properly on address breakpoint, Trace OK	* Unused address lines not grounded	Check address line grounding
Address or data capture sometimes improper	* Wrong address or data clock edge selected	Check timing on address lines and switch S1(S2,S3 for data)
Error message=Trace Setup	* Improperly selected breakpoints * Improper breakpoint assignment	Check breakpoint values. Check breakpoint assignment and reassign if necessary
Trace does not change	* Trace not armed * Not in "Running"	Press "A" to rearm Key R (CR) for Running
Trace improperly completes on qualifier (TQ) specification	* TQ active state improper * TQ clock source improper	Check switches S1(TQ1)& S5(TQ2) Check switches S12(TQ1)& S34(TQ2)

Figure 4.5.1

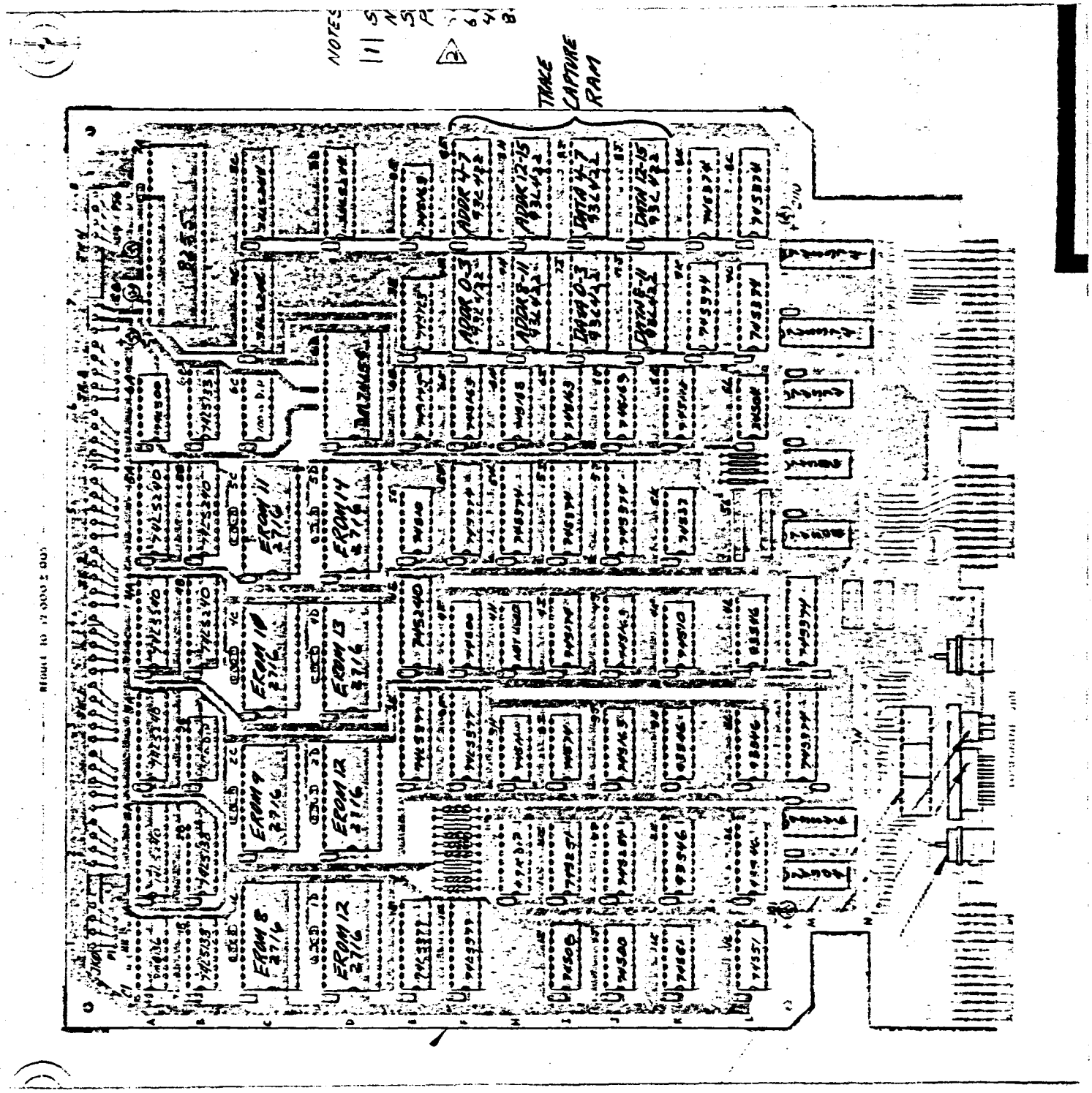

TIMER CAPTURE RAM
EPROM 8
EPROM 9
EPROM 10
EPROM 11
EPROM 12
EPROM 13
EPROM 14
EPROM 15

Figure 4.5.2

4.6 GENERAL DIFFICULTIES

4.6.1 ADDRESS = NONE

This is the normal address message which appears on the STEP-N display when no valid address is present at the user port. It usually means that enable inputs to WCS memory are not connected properly. See section 3.1.1.4.

SECTION V

DETAILED LOGIC DRAWINGS

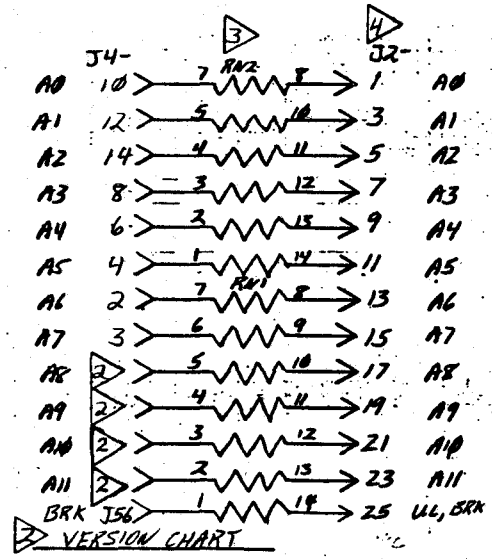
5.0 LIST OF DRAWINGS

5.1 LIST OF PROPRIETARY DRAWINGS

5.0 This Section contains the following Drawings in the order listed:

DRAWING NUMBER	TITLE
0001010	Schematic, buffer board, dual 4 bit master
0001011	Assemble, buffer board, 256, 516, 1K slave
0001012	Schematic, buffer board, dual 4 bit slave
0001013	Assembly, buffer board, 256, 512, 1K mater
0001014	Schematic, 256 x 8, 512 x 8, 20 pin
0001015	Schematic, 256 x 8, 512 x 8, latcheing
0001016	Schematic, 256 x 8, 512 x 8, 1K x 8 Std
0001017	Assembly, 2K word master
0001021	Schematic, dual 2K x 4
0001022	Schematic, 2K x 8
0001039	Schematic, Old mem 32 board interface
0001040	Assembly, Old mem 32 board interface
0001041	Assembly, memory module 1K x 32
0001049	Schematic, buffer board, 1K x 32 master
0001053	Schematic, I/O and Clock board
0001054	Assembly, I/O and Clock board
0001062	TTY Cable
0001063	Schematic, system memory board
0001064	Assembly, system memory board
0001074	Schematic, buffer boatd, dual 512 x 4
0001075	Assembly, buffer board, 2k word slave
0001078	Schematic, buffer board, 1K x 8 latching
81862-003E	Assembly, CPU board
81864E	Schematic, CPU board
082015C	Assembly , CRT controller board
082017C	Schematic, CRT controller board
0001172	Assembly, Trace
0001122	Summary, ROM Simulation
0001108	Assembly, Trace probes
0001112	Assembly, mem 32 A
0001113	Parts list, mem 32 A
0001110	Schematic, Trace probes
0001098	Assembly, multiwire Trace
0001094	Parts list, mem 128 A, B, F
0001080	Assembly, wire list, mem 128 A, B, F
0001028	ROM Sim pinouts
0300001	Assembly, new Trace probe
0400001	Schematic, new Trace probe
0300002	Assembly, Speed Test board
0300006	Assembly Trace expoander
0300010	Assembly, Step-3 system memory board
0400010	Schematic, Step-3 system emeory board

MASTER

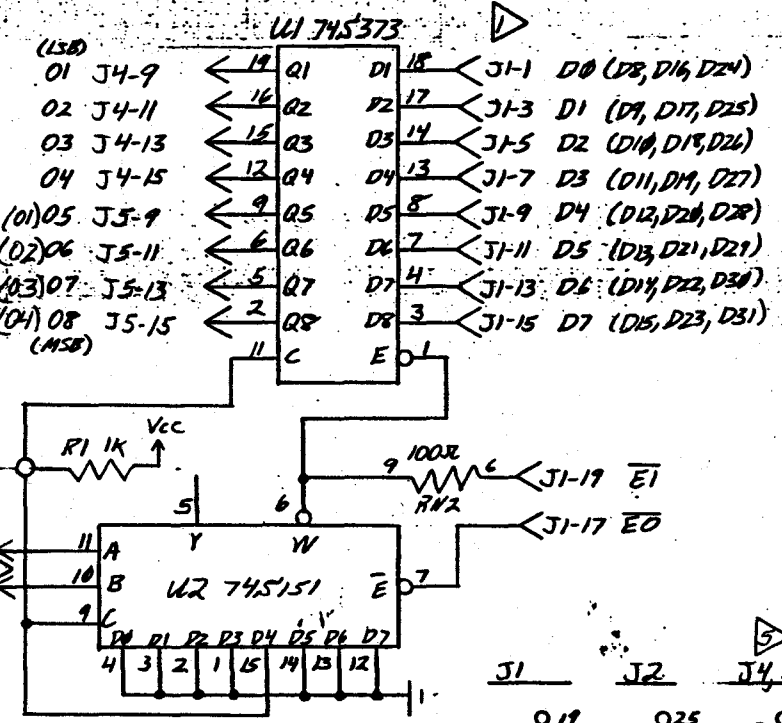


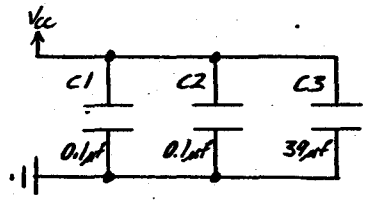
3 VERSION CHART

VER	RN1-5	RN1-4	RN1-3	RN1-2	U2-10	U2-11	TYPE
-001	J53	J54	J4-24	J4-0	J5-7	J4-7	256X4
-002	J4-5	J54	J4-24	J4-0	J5-7	J4-7	512x4
-003	J4-5	J4-7	J4-24	J4-0	U2-13	U2-4	1Kx4(NEW)
-004	J4-5	J4-7	J4-24	J4-0	J4-16	J4-17	1Kx4(08)
-005	J4-5	J4-7	J-54	J-53	U2-13	J-55	1Kx4(10)
-006	J4-5	J54	J4-24	J4-0	U2-13	J55	512x4

VCC	GND
J4-1	J1-2,4,6,8,16,18, 10,12,14,20
U1-20	J4-0,24
U2-16	J2-2,4,6,8,16,18,20 10,12,14,22,24,26
R1	U1-10
	U2-1,2,3,4,8,12,13,14
	J4-0,24

VER	RN1-5	RN1-4	RN1-3	RN1-2	U2-10	U2-11	TYPE
-012	J4-5	J4-7	J4-16	J4-17	J4-15	J4-19	4K×4
-011	J4-5	J53	J54	J4-24	U2-13	J55	512, 2K DUAL
-010	J4-5	J4-7	J4-16	J53	U2-13	J4-17	2K×4, 2K DUAL
-007	J4-5	J4-7	J4-16	J53	U2-13	J-55	2K×4 (10)
-008	J4-5	J4-7	J4-24	J4-0	U2-13	J4-17	2K×4 (10 OCT)
-009	J53	J54	J4-24	J4-0	U2-13	J55	256×4





J1	J2	J4, J5
19	25	0
18 17	24 23	2
16 15	22 21	4
14 13	20 19	6
12 11	18 17	8
10 9	16 15	10
8 7	14 13	12
6 5	12 11	14
4 3	10 9	16
2 1	8 7	18
	6 5	20
	4 3	22
	1	24

REVISIONS

LTR	REV NO	REASON	DATE	BY
TB		REVISED PREFRANK	1/7/78	PWB
C		ADDED VERSION -008 & 009	2/3/78	DHM
D		ADDED VERSION -007	2/24/78	PWB
E	Z6	ADD VER 8 THRU 12	2/24/78	PWB

NOTES: UNLESS OTHERWISE SPECIFIED

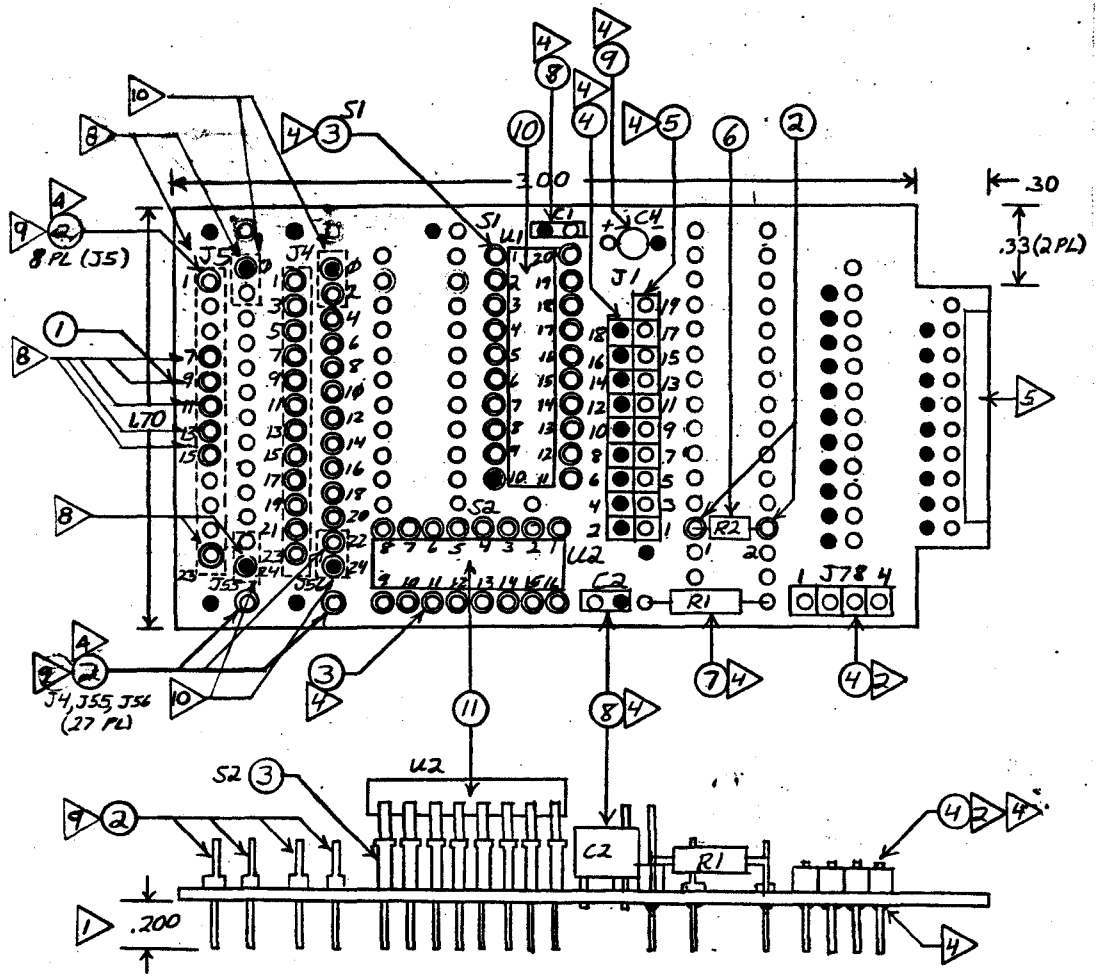
1. J1 PIN 20 REMOVED FOR KEYING
2. SEE VERSION CHART FOR PINOUT
3. RN1, RN2 .33 OHM RESISTOR PACKS
4. J2 PINS 2,26 REMOVED FOR KEYING
5. J4, J5 CONNECT TO ROM SIM PLUG
6. WARNING: $\overline{CS}$ (DIP PIN 10) MUST BE LOGIC LOW ON BOTH DIP PLUGS FOR OUTPUTS TO BE ENABLED.

STEP ENGINEERING

SCHEMATIC, BUFFER BOARD
DUAL 4 BIT MASTER

DRAWN	DATE	APPROVED	DATE
SMH	1/7/78		

DWG NO 0001010 SHT 1/1



REVISIONS				
LTR	REV NO	REASON	BY	DATE
TA		SCHEMATIC ERROR	[illegible]	10/11/77
TB		LSB-MSB ERROR	[illegible]	1/3/78
TC		ADD -008 VERSION	[illegible]	1/4/78
D		RLSE & ADD GND PINS ON WL	[illegible]	5/5/78
E		MOD 003 VER & MOD NOTE 7	[illegible]	5/30/78
F		ADD 009 VER, CLEAN UP	KEM	7/5/78
G		ADD 010 VER	KEM	9/9/78
H		ADD 011 VERSION	[illegible]	1/10/79
I		ADD 012 VERSION	[illegible]	1/26/79
J		CHNG ITEM 2 - NOTE 2, 9, 10	[illegible]	7/11/79
K	054	DELETE SHT 3	[illegible]	3/8/80

NOTES: UNLESS OTHERWISED SPECIFIED

1. CUT LEADS WHERE NECESSARY TO .200 INCH AFTER ASSY IS WIREWRAPPED.
2. INSTALL POST WITH LONG PIN DOWN TRIM TOP POST FLUSH WITH INSULATOR
3. PINS CALLED OUT AS "GND" ON WIRE LIST SHOULD BE SOLDERED TO GROUND PLANE, FAR SIDE
4. ITEM 2, 3, 4, 5, 7, 8, 9 TO BE SOLDERED TO BOARD FAR SIDE
5. MARK ASSY NO IN SPACE INDICATED
6. ASSY NO SHALL BE DWG NO-VERSION-REV LTR
7. CUT TRACE U2-12 TO U2-13 (THIS APPLIES ONLY TO VERSION 003)
8. THESE PINS CAN BE OMITTED ON ALL VERSIONS EXCEPT 006, 007, 008, 009
9. ASSEMBLE ITEM 2 WITH LONG END DOWN
10. ON VERSION 011 REPLACE ITEM 2 WITH ITEM 4 SHORT
11. CUT TRACE J1-1 TO RN2-6 = ALL BOARDS

STEP ENGINEERING			
ASSEMBLY, BUFFER BOARD 256, 512, 1K WORD SLAVE			
DRAWN [illegible]	DATE 7/23/77	APPROVED	DATE
DWG NO 0001011			SHT 1/2

VERSION CHART

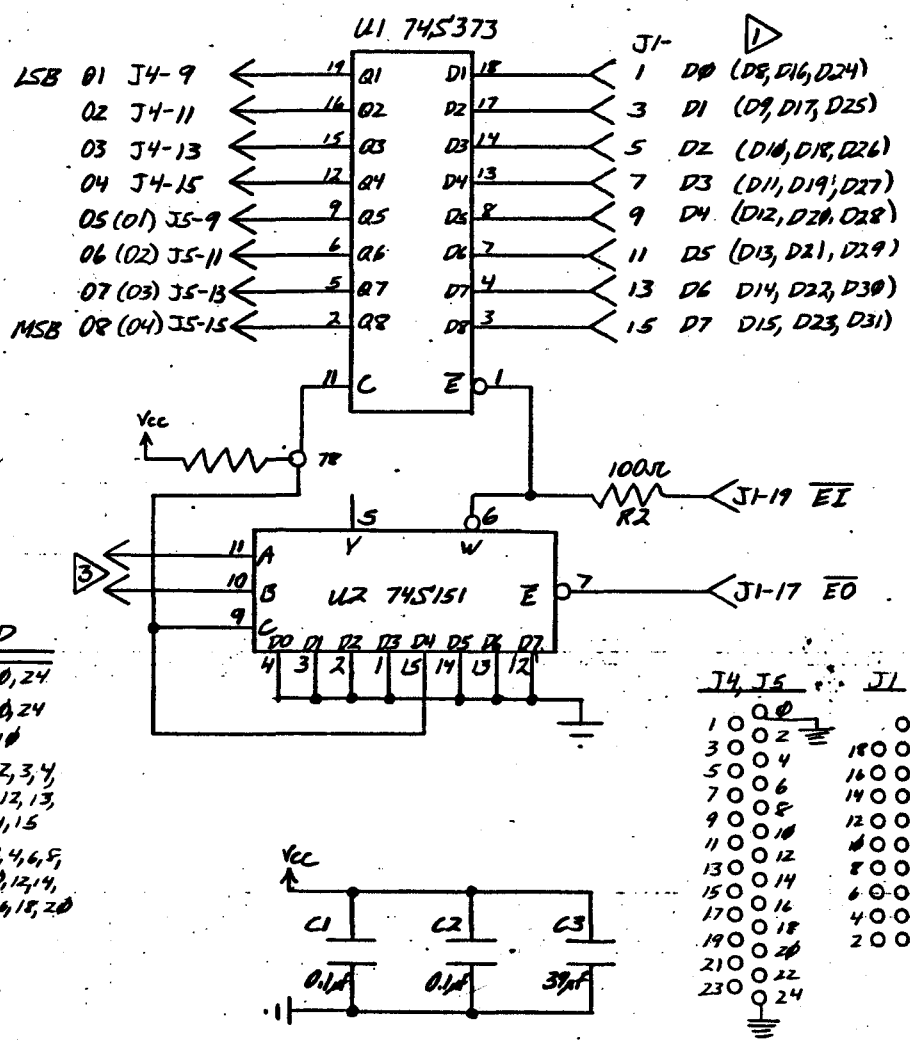
VERSION	DESCRIPTION	SCHEM NO
-001	~~BUFFER, 256×8, 20 PIN~~	~~0001014~~
-002	BUFFER, 8 BIT, 20 PIN	0001014-003
-003	BUFFER, 8 BIT LATCHING, 24 PIN	0001015-003
-004	BUFFER, 8 BIT STANDARD, 24 PIN	0001016-005
-005	BUFFER, 1K×8 EROM 24 PIN	0001016-006
-006	BUFFER, 4 BIT STANDARD, 16 PIN 256×4, 512×4, DUAL	0001012-001
-007	BUFFER, 4 BIT STANDARD, 18 PIN DUAL	0001012-002
-008	BUFFER 32×8, 16 PIN	0001049-002
-009	BUFFER 4 BIT DUAL 16 PIN 1K×4	0001012-003
-010	BUFFER 8 BIT STD LATCHING, 24 PIN, 1K×8	0001078-002
-011	BUFFER 4 BIT DUAL 16 PIN 1K×4 (MEM 128)	0001012-001
-012	BUFFER 8 BIT 1K×8 TO SIM 4K×8 (MEM 128)	0001016-009
-001	BUFFER 8 BIT 4K×8 TO SIM 2732 (MEM 128)	0001016-011
-013	BUFFER [illegible]	[illegible]

PARTS LIST

PART NO	REF DESIG	DESCRIPTION	QUANTITY	PART NUMBER
1	———	PC BOARD, BUFFER GEN PURPOSE	1	0001018-001
~~2~~	~~J4, J5, J55, J56~~	~~TERMINAL, FEED THRU, WIREWRAP~~	~~35~~	~~AUGUT 8128-19R3~~
3	S1, S2	LEAD SOCKET, WIRE WRAP PINS	36	AUGUT LSG-1FG10-1
4	~~J5~~ J78	STRIP LINE PLUG, WW, .43 LONG	AIR	CA-536SP100-230-430
5	J[illegible]	STRIP LINE PLUG, WW, .60 LONG	AIR	CA-536SP100-230-600
6	R2	RESISTOR, CARBON FILM, 100 OHM, 1/4W, 5%	1	RC07GF101K
7	R1	RESISTOR, 1K OHM, 10%, 1/4W	1	RC07GF102K
8	C1, C2	CAPACITOR, CERAMIC 0.1 MF	2	CENTRALAB CY20C104P
9	C4	CAPACITOR, TANTALUM, 39 MF, 10V	1	~~SPRAGUE~~ 196D396X9010KA1
10	U1	OCTAL D TYPE TRANSPARENT LATCH	1	74S373
11	U2	ONE OF EIGHT DATA SELECTOR	1	74S151
12	———	SOLDER, ROSEN CORE	AIR	
13	———	WIRE, KYNER COATED, 30 AWG, STRIPPED, 3" LONG	AIR	AUGUT 1410-KG11
14	———	WIRE, KYNER COATED, 30 AWG, STRIPPED, 4" LONG	AIR	AUGUT 1410-KG12
15	———	SCHEMATIC	REF	SEE VERSION CHART
2	J4, J5, J55, J56	STRIP LINE PLUG WW, .50 LONG	AIR	CA-536SP100-170-500

STEP ENGINEERING

DWG NO 0001011 SHT2



3 VERSION CHART

VER	U2-9	U2-10	U2-11
-001	J1-2	J5-7	J4-7
-002	J1-2	J4-17	J4-16
-003	J1-2	J4-17 (GND) U2-13	J4-16 (GND) U2-4
-004	J1-2	J4-17 (GND) U2-13	J5-5
-005	J1-2	U2-13	J4-17
-006	J1-2	J4-18	J4-19

VCC	GND
J4-1	J4-0, 24
J5-1	J5-0, 24
U1-20	U1-10
U2-16	U2-1, 2, 3, 4, 8, 12, 13, 14, 15
R1	J1-3, 4, 6, 8, 10, 12, 14, 16, 18, 20

REVISIONS

LTR	REV NO	REASON	DATE	BY
TB		REVISED AND REDRAWN	1/4/78	SMD
C		ADDED VERSION -004	3/24/78	DV
D		ADD VER 5, 6	7/19/80	SMD

NOTES: UNLESS OTHERWISE SPECIFIED

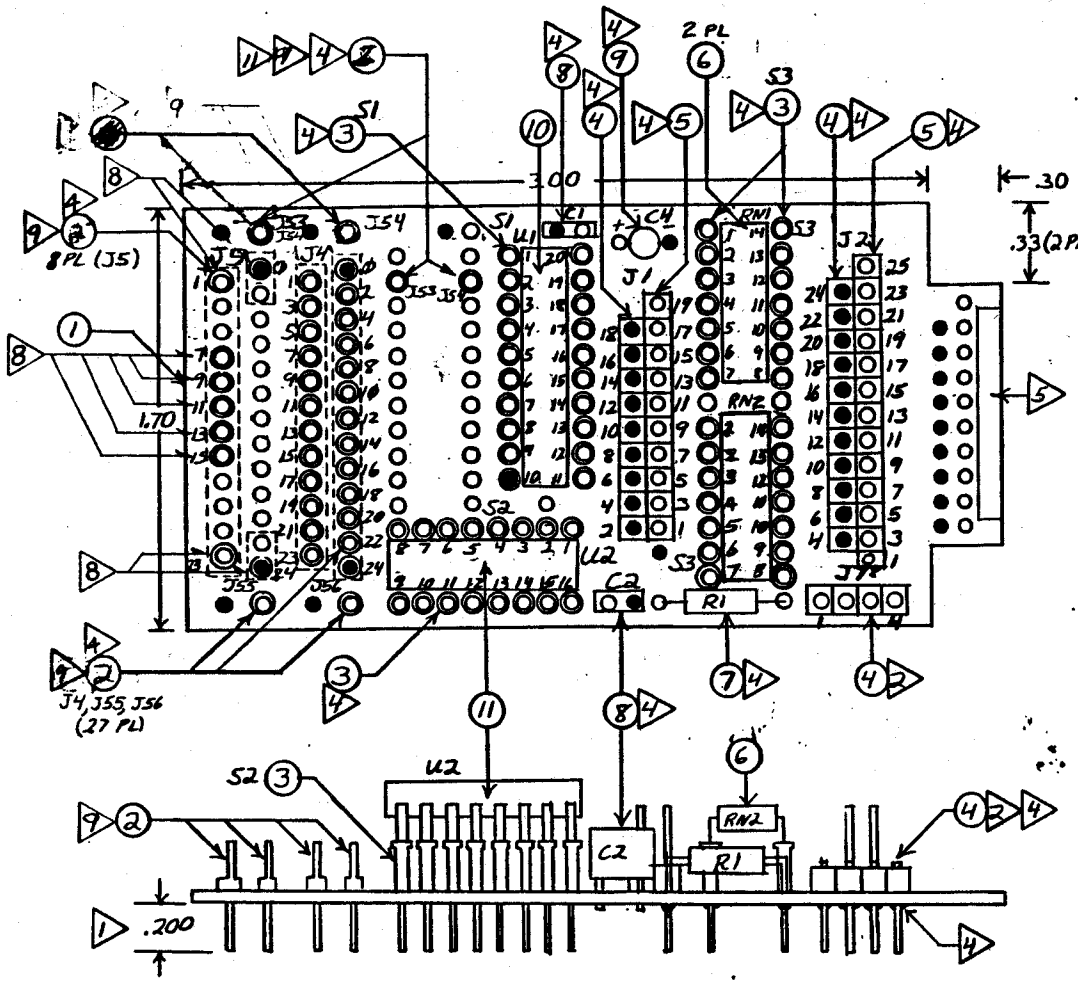
1. J1 PIN 20 REMOVED FOR KEYING
2. WARNING: $\overline{CS}$ (DIP PIN 10, VERSIONS 1 256x9 + 512x4) MUST BE LOGIC LOW ON BOTH DIP PLUGS FOR OUTPUTS TO BE ENABLED.
3. SEE VERSION CHART FOR PINOUT

STEP ENGINEERING

SCHEMATIC, BUFFER BOARD
DUAL 4BIT SLAVE

DRAWN	DATE	APPROVED	DATE
SMD	1/4/78		

DWG NO 0001012 SHT 1/1



REVISIONS				
LTR	REV NO	REASON	BY	DATE
TA		SCHEMATIC ERRORS	[illegible]	10/11/77
TB		MSB-LSB ERROR	[illegible]	11/3/77
TC		ADD -013 VERSION	[illegible]	11/15/77
D		RLSE + ADD GND PINS ON W/L	[illegible]	5/15/78
E	9	ADD NOTE 7, MOD VER 3,4 MOD NOTE 9	[illegible]	5/29/78
F		ADD J5-7 PIN, CLEAN UP	KSM	26/8/78
G		ADD 014 VERSION	KSM	9/9/78
H		ADD 015 VERSION	[illegible]	11/10/78
I		ADD 016 + 017 VERSION	[illegible]	1/24/79
J		ADD VERSION 018	[illegible]	2/20/79
K		CHANGE ITEM 2 TO NOTES 8, 9	[illegible]	7/11/79
L	034	CHNG J53, J54; DEL SHT 3,4	[illegible]	3/6/80

NOTES: UNLESS OTHERWISED SPECIFIED

1. CUT LEADS WHERE NECESSARY TO .200 INCH AFTER ASSY IS WIREWRAPPED.
2. INSTALL POST WITH LONG PIN DOWN TRIM TOP POST FLUSH WITH INSULATOR
3. PINS CALLED OUT AS "GND" ON WIRE LIST SHOULD BE SOLDERED TO GROUND PLANE, FAR SIDE
4. ITEM 2, 3, 4, 5, 7, 8, 9 TO BE SOLDERED TO BOARD FAR SIDE
5. MARK ASSY NO IN SPACE INDICATED
6. ASSY NO SHALL BE DWG NO-VERSION-REV LTR
7. CUT TRACE U2-12 TO U2-13 (THIS APPLIES ONLY TO VERSIONS 003, 004)
8. THESE PINS CAN BE OMITTED ON ALL VERSIONS EXCEPT 004, 010, 014, 013, 015, 016, [illegible]
9. ASSEMBLE ITEM 2 WITH LONG END DOWN
10. CUT TRACE J1-1 TO RN2-6 = ALL BOARDS
11. PREFERRED LOCATION OF J53 (J54) IS BETWEEN J4, J5 EXCEPT ON 4 BIT ROM SIMS

STEP ENGINEERING			
ASSEMBLY, BUFFER BOARD 256, 512, 1K WORD MASTER			
DRAWN [illegible]	DATE 7/23/77	APPROVED	DATE
DWG NO 0001013			SHT 1/2

VERSION CHART

VERSION	DESCRIPTION	SCHEM NO
-001	BUFFER, 256x8, 20 PIN	0001014-001
-002	BUFFER, 512x8, 20 PIN	0001014-002
-003	BUFFER, 256x8 LATCHING, 24 PIN	0001015-001
-004	BUFFER, 512x8 LATCHING, 24 PIN	0001015-002
-005	BUFFER, 256x8 STANDARD, 24 PIN	0001016-001
-006	BUFFER, 512x8 STANDARD, 24 PIN	0001016-002
-007	BUFFER, 1Kx8 STANDARD, 24 PIN	0001016-003
-008	BUFFER, 1Kx8 EROM, 24 PIN	0001016-004
-009	BUFFER, 256x4, DUAL 16 PIN	0001010-001
-010	BUFFER, 512x4, DUAL 16 PIN	0001010-002
-011	BUFFER, 1Kx4, DUAL 16 PIN	0001010-003
-012	BUFFER, 1Kx4, DUAL 18 PIN	0001010-004
-013	BUFFER, 32x8, 16 PIN	0001019-001
-014	BUFFER, 1Kx8, LATCHING, 24 PIN	0001078-001
-015	BUFFER, 512x4, DUAL 16 PIN	0001010-002
-016	BUFFER, 1Kx4, DUAL 18 PIN	0001010-002
-017	BUFFER, 512x8, 24 PIN	0001016-007
-020	BUFFER, 4Kx8, 24 PIN, STD FOR USE WITH MEM128	0001016-008
-019	BUFFER, 4Kx8, 24 PIN, (2732) FOR USE WITH MEM128	0001016-010
-018	BUFFER, 2Kx8, 18 PIN (MEM128)	0001010-005

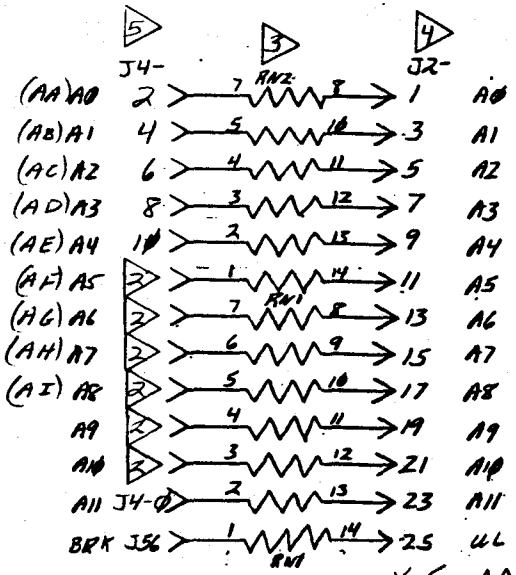
PART NO	REF DESIG	DESCRIPTION	QUANTITY			PART NUMBER
1	———	PC BOARD, BUFFER GEN PURPOSE	1			0001018-001
~~8~~	~~J1,J2,J3,J4~~	~~TERMINAL, FEED THRU, WIREWRAP~~	~~37~~			~~AUGAT 8128-1R23~~
3	S1, S2, S3	LEAD SOCKET, WIRE WRAP PINS	64			AUGAT LSG-1FG10-1
4	~~J2~~, J2, J78	STRIP LINE PLUG, WW, .43 LONG	A/R			CA-5365P100-230-430
5	J1	STRIP LINE PLUG, WW, .60 LONG	A/R			CA-5365P100-230-600
6	RN1, RN2	RESISTOR NETWORK, 330 OHMS, 5%, DIP	2			BOURNS 4114R-001-330
7	R1	RESISTOR, 1K OHM, 10%, 1/4W	1			RC07GF102K
8	C1, C2	CAPACITOR, CERAMIC 0.1mF	2			CENTRALAB CY20C104P
9	C4	CAPACITOR, TANTALUM, 39mF, 10V	1			SPRAGUE 196D396X9010M1
10	U1	OCTAL 'D' TYPE TRANSPARENT LATCH	1			74S373
11	U2	ONE OF EIGHT DATA SELECTOR	1			74S151
12	———	SOLDER, ROSEN CORE	A/R			
13	———	WIRE, KYNER COATED, 30AWG, STRIPPED, 3" LONG	A/R			AUGAT 1410-KG11
14	———	WIRE, KYNER COATED, 30AWG, STRIPPED, 4" LONG	A/R			AUGAT 1410-KG12
15	———	SCHEMATIC	REF			SEE VERSION CHART
2	J4, J5, J6, J7, J8	STRIP LINE PLUG WW, .50 LONG	A/R			CA-5365P100-170-500

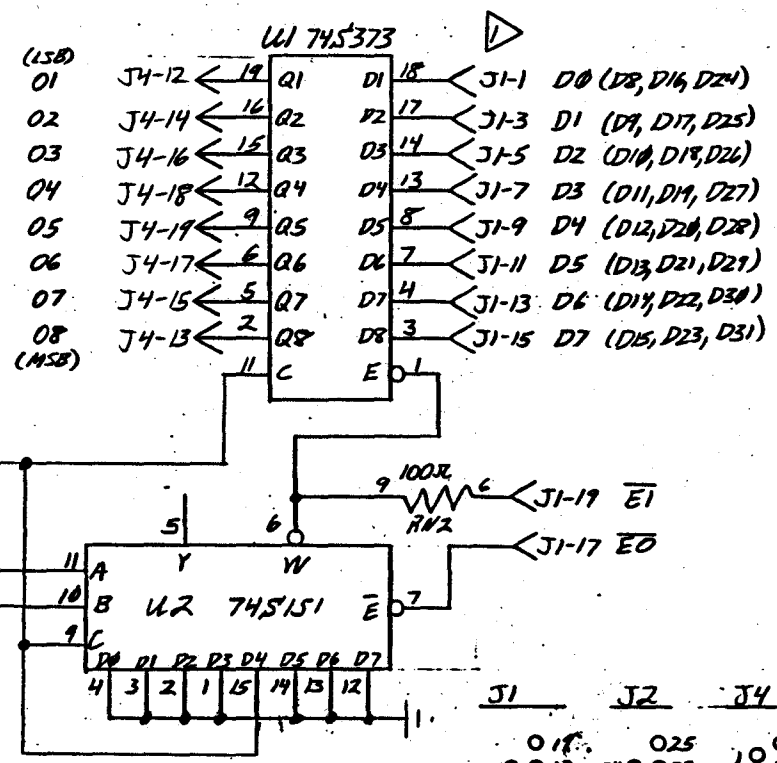
PART LIST

STEP ENGINEERING

DWG NO 0001013 SHT2

MASTER (VERSION -001, -002)



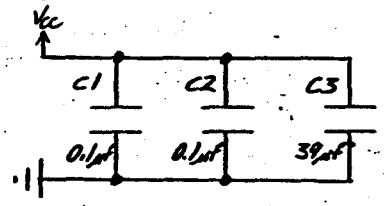


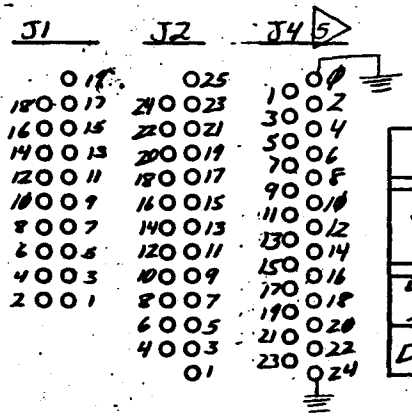
REVISIONS				
LTR	REV NO	REASON	DATE	BY
JB		REVISED & REDRAWN	1/78	
C	26	ADDED Ø4-08 MOD VER 01		

NOTES: UNLESS OTHERWISE SPECIFIED

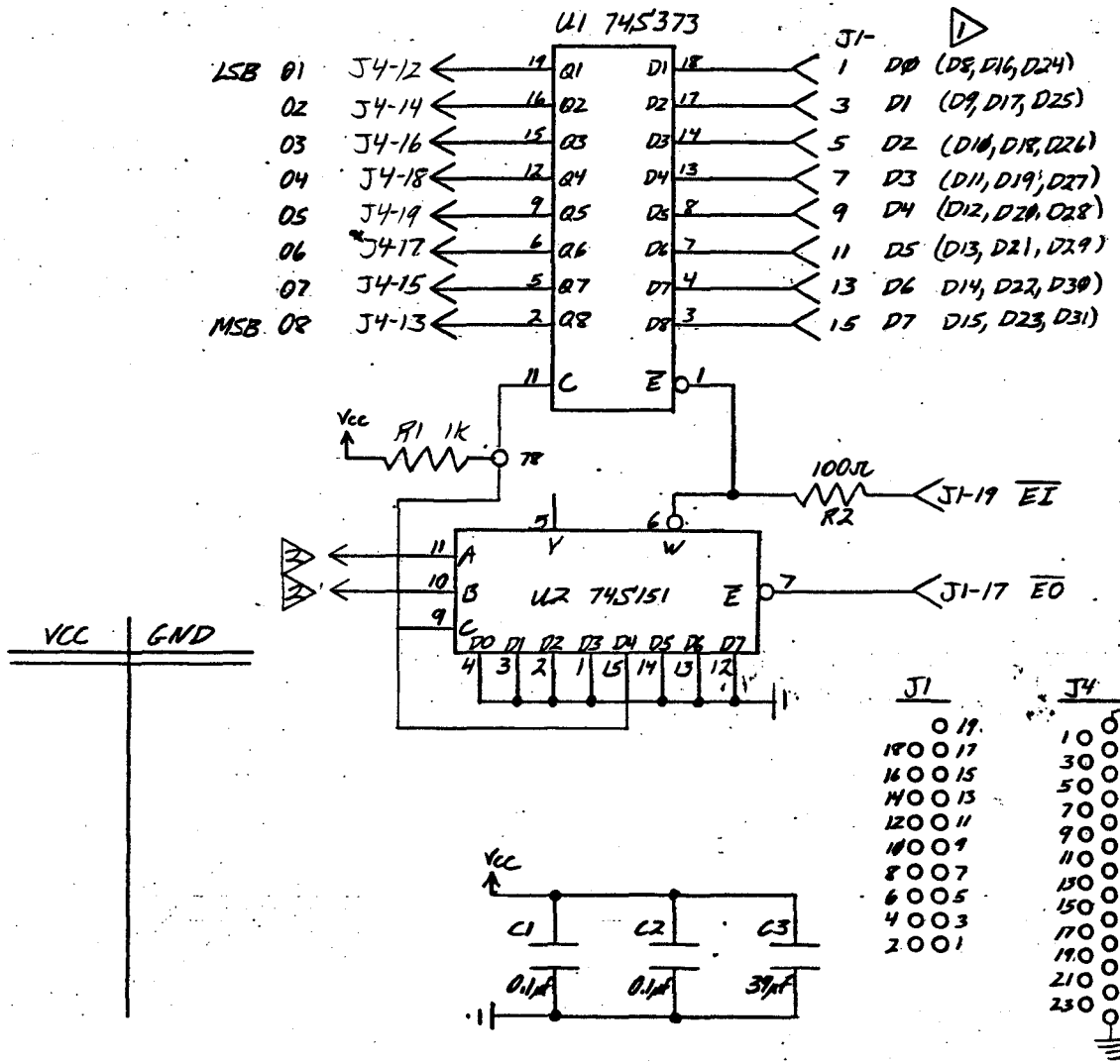
1. J1 PIN 2Ø REMOVED FOR KEYING
2. SEE VERSION CHART (SHEET 2) FOR PINOUT
3. RN1, RN2 100 OHM RESISTOR PACKS
4. J2 PINS 2, 26 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG

Vcc	GND
J4-1	J1-2, 4, 6, 8, 10, 12, 14, 16, 18, 20
U1-20	J2-2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26
U2-16	J4-Ø, 24
R1	U1-1Ø
	U2: 1, 2, 3, 4, 8, 12, 13, 14





STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256×8, 512×8, 20 PIN			
DRAWN	DATE	APPROVED	DATE
	1/17/78		
DWG NO 0001014		SHT 1/2	



REVISIONS (SEE SHT 1)				
LTR	REV NO	REASON	DATE	BY

NOTES: UNLESS OTHERWISE SPECIFIED

1. J1 PIN 20 REMOVED FOR KEYING

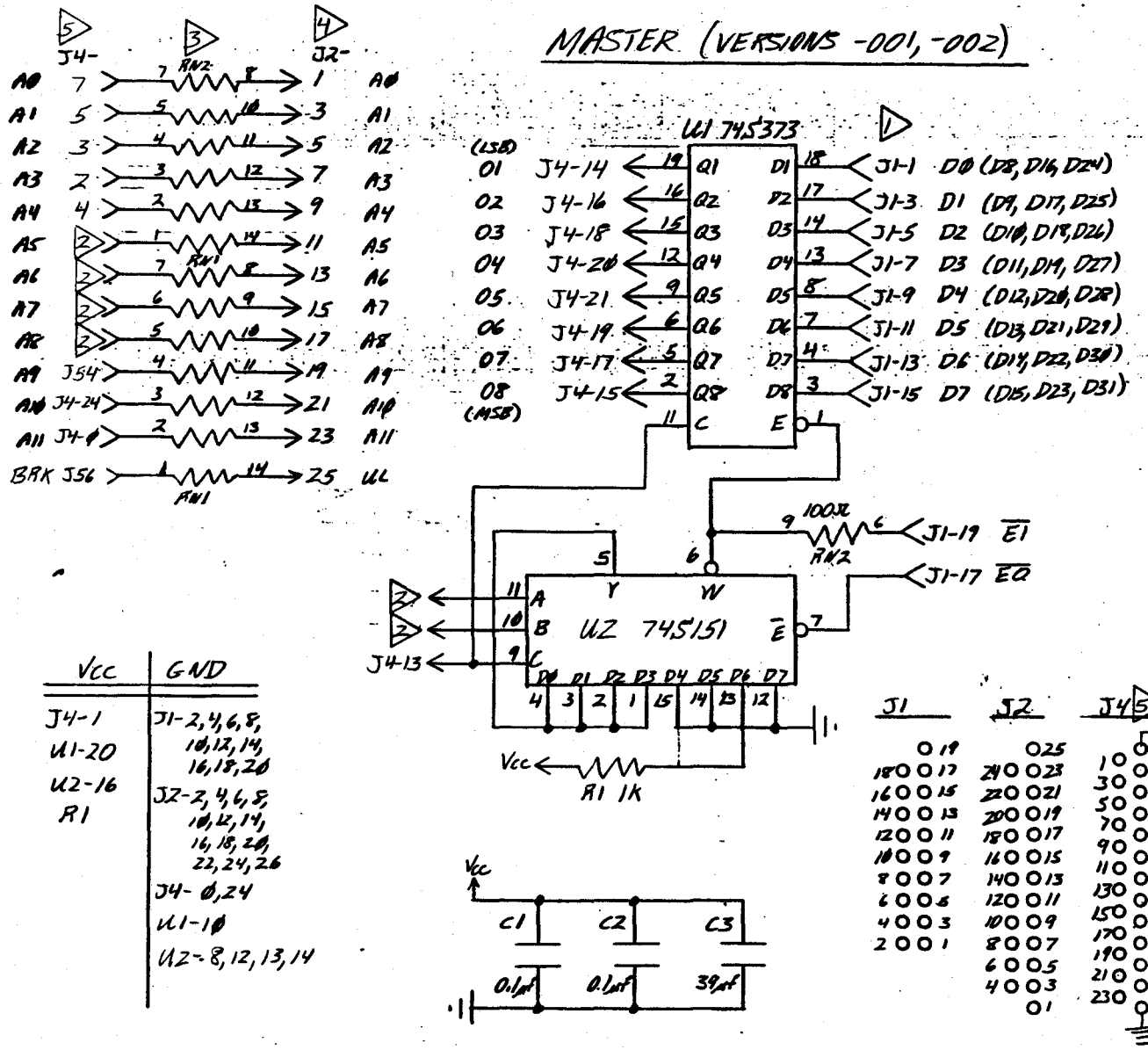
2. VERSION CHART

DESCRIPTION	VER	U2-11	U2-10	RN1-9	RN1-3	RN1-7	RN1-6	RN1-5	RN2-1
256×8 MASTER	-001	J4-11	J4-9	J53	J4-24	J4-5	J4-3	J54	J4-7
512×8 MASTER	-002	J4-11	U2-4	J54	J4-24	J4-7	J4-5	J4-3	J4-9
256×8 SLAVE	-003	J4-11	J4-9	—	—	—	—	—	—
256×8 MASTER	-004	J55	U2-4	J53	J4-24	J4-5	J4-3	J53	J4-7
8 BIT SLAVE	-005	J55	U2-4	—	—	—	—	—	—
512×8 SLAVE	-006	J4-11	U2-4	—	—	—	—	—	—
512×8 MASTER	-007	J55	U2-4	J54	J4-24	J4-7	J4-5	J4-3	J4-9
512×8 MASTER	-008	J55	U2-4	J54	J53	J4-7	J4-5	J4-3	J4-9

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256×8, 512×8 20 PIN			
DRAWN	DATE	APPROVED	DATE
DWG NO 0001014		SHT 2/2	

C 10

MASTER (VERSIONS -001, -002)



REVISIONS				
LTR	REV NO	REASON	DATE	BY
TA		REVISED & REDRAWN	11/1/78	[illegible]
C		REVISE & RELEASE	4/01/78	[illegible]
D	26	ADD VER 04, 05 & UPDATE	11/1/78	[illegible]

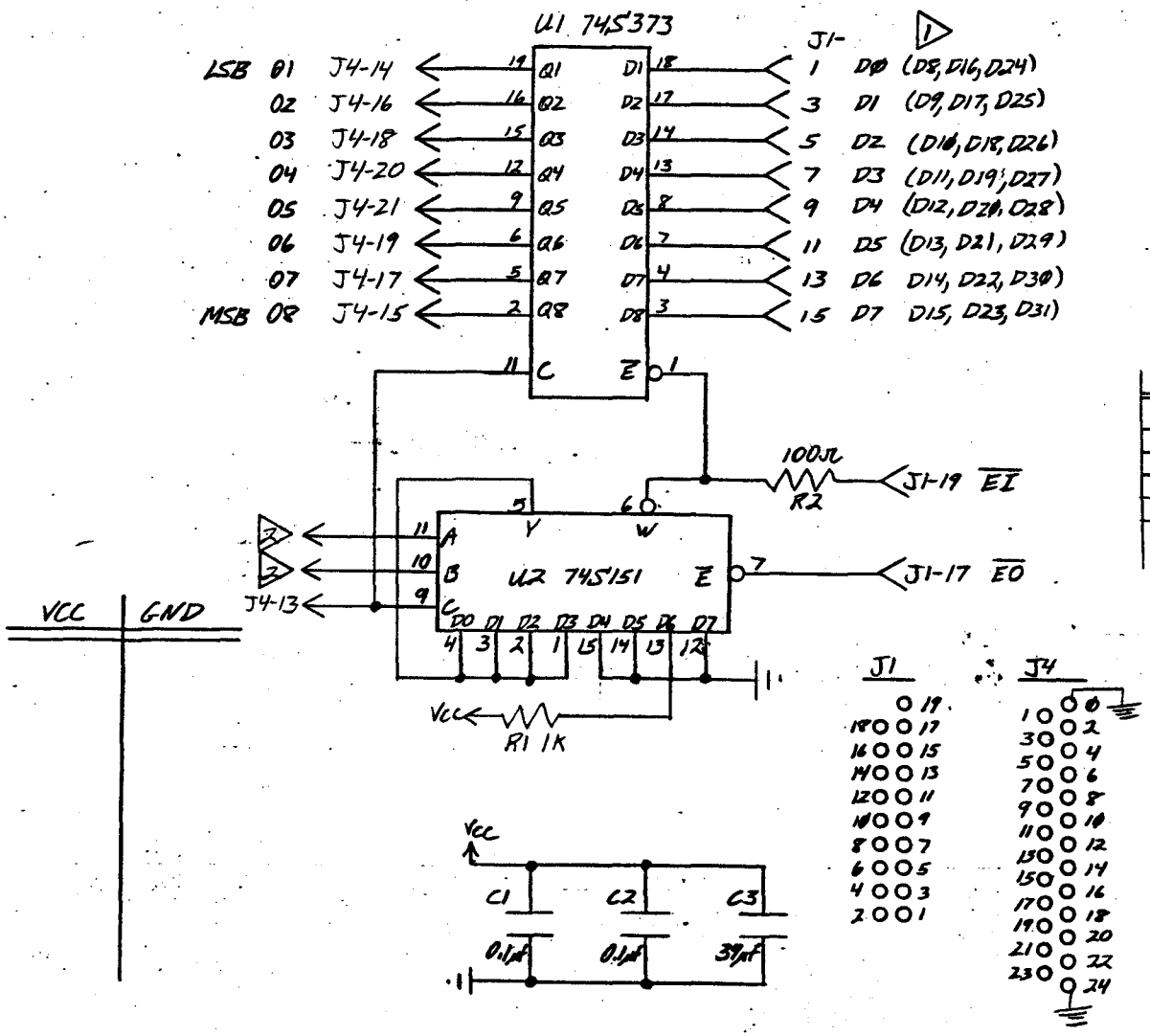
NOTES: UNLESS OTHERWISE SPECIFIED

1. J1 PIN 2Ø REMOVED FOR KEYING
2. SEE VERSION CHART, SHEET 2, FOR PINOUT
3. RN1, RN2 100 OHM RESISTOR PACKS
4. J2 PINS 2, 26 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG

Vcc	GND
J4-1	J1-2, 4, 6, 8, 10, 12, 14, 16, 18, 2Ø
U1-2Ø	J2-2, 4, 6, 8, 10, 12, 14, 16, 18, 2Ø, 22, 24, 26
U2-16	J4-Ø, 24
R1	U1-1Ø
	U2-8, 12, 13, 14

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256x8, 512x8 LATCHING			
DRAWN	DATE	APPROVED	DATE
[illegible]	1/7/78		
DWG NO 0001015		SHT 1/2	

SLAVE (VERSION 3)



REVISIONS (SEE SHEET 1)				
LTR	REV NO	REASON	DATE	BY

NOTES: SEE SHEET 1

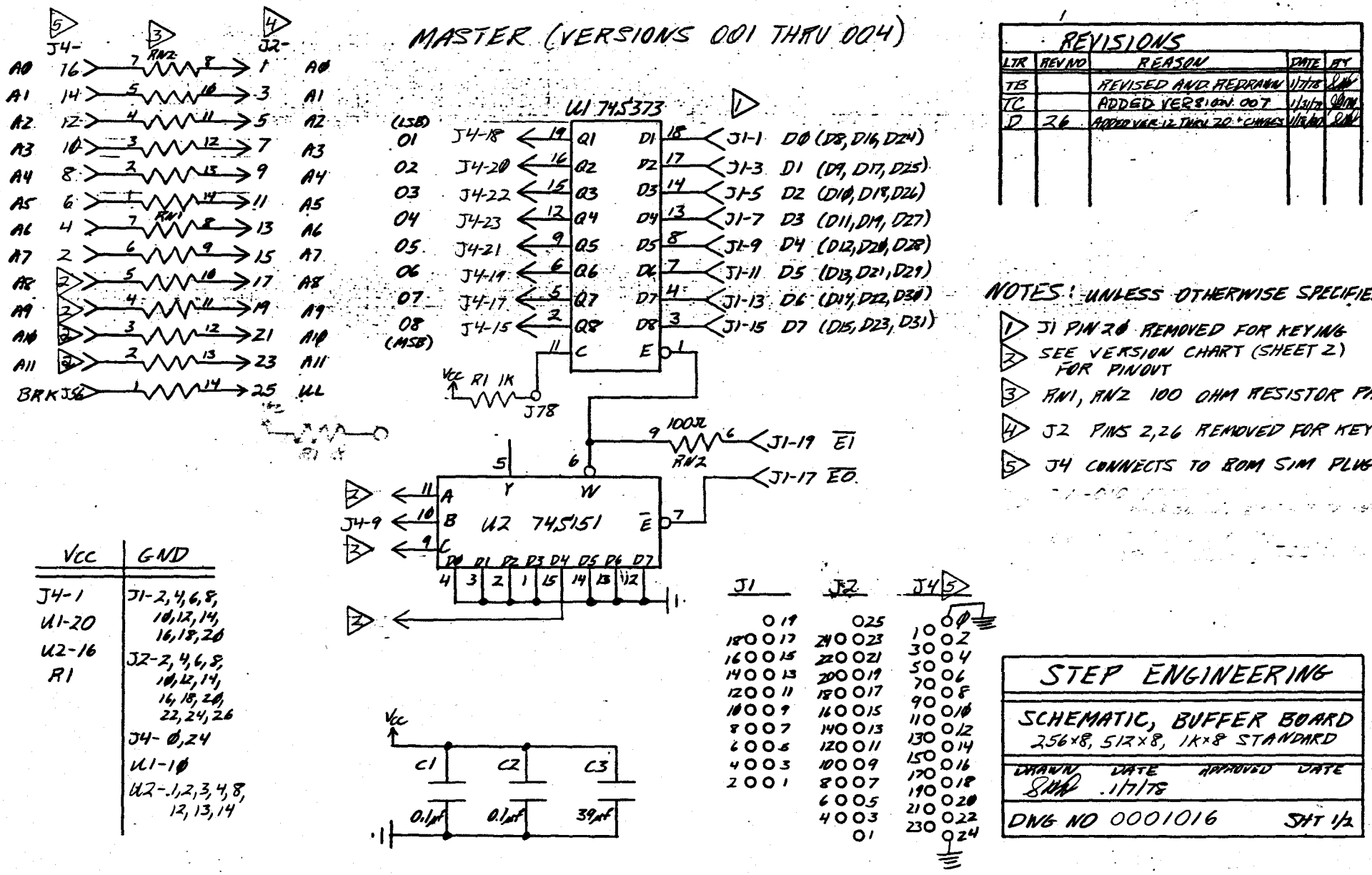
~~NOTES: 1. UNLESS OTHERWISE SPECIFIED~~

~~1 J1 PIN 20 REMOVED FOR KEYING~~

VER	DESCRIP	RN2-1	RN1-7	RN1-6	RN1-5	U2-11	U2-10
-001	256x8 MASTER	J4-8	J4-10	J4-12	J53	J4-9	J4-11
-002	512x8 MASTER	J4-6	J4-8	J4-10	J4-12	J4-9	J4-11
-003	8 BIT SLAVE	—	—	—	—	J4-9	J4-11
004	512x8 MASTER	J4-6	J4-8	J4-10	J4-12	J53	J55
005	512x8 SLAVE	—	—	—	—	J56	J55

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256x8, 512x8 LATCHING			
DRAWN	DATE	APPROVED	DATE
DWG NO 0001015		SHT 2/2	

MASTER (VERSIONS 001 THRU 004)



REVISIONS				
LTR	REV NO	REASON	DATE	BY
TB		REVISED AND REDRAWN	1/7/78	[illegible]
TC		ADDED VERSION 007	1/24/78	[illegible]
D	26	ADDED VER 12 THRU 20 * CHGES	1/25/80	[illegible]

NOTES: UNLESS OTHERWISE SPECIFIED

1. J1 PIN 26 REMOVED FOR KEYING
2. SEE VERSION CHART (SHEET 2) FOR PINOUT
3. RN1, RN2 100 OHM RESISTOR PACKS
4. J2 PINS 2,26 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG

VCC	GND
J4-1	J1-2, 4, 6, 8, 10, 12, 14, 16, 18, 20
U1-20	J2-2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26
U2-16	J4- 0, 24
R1	U1-10
	U2-1, 2, 3, 4, 8, 12, 13, 14

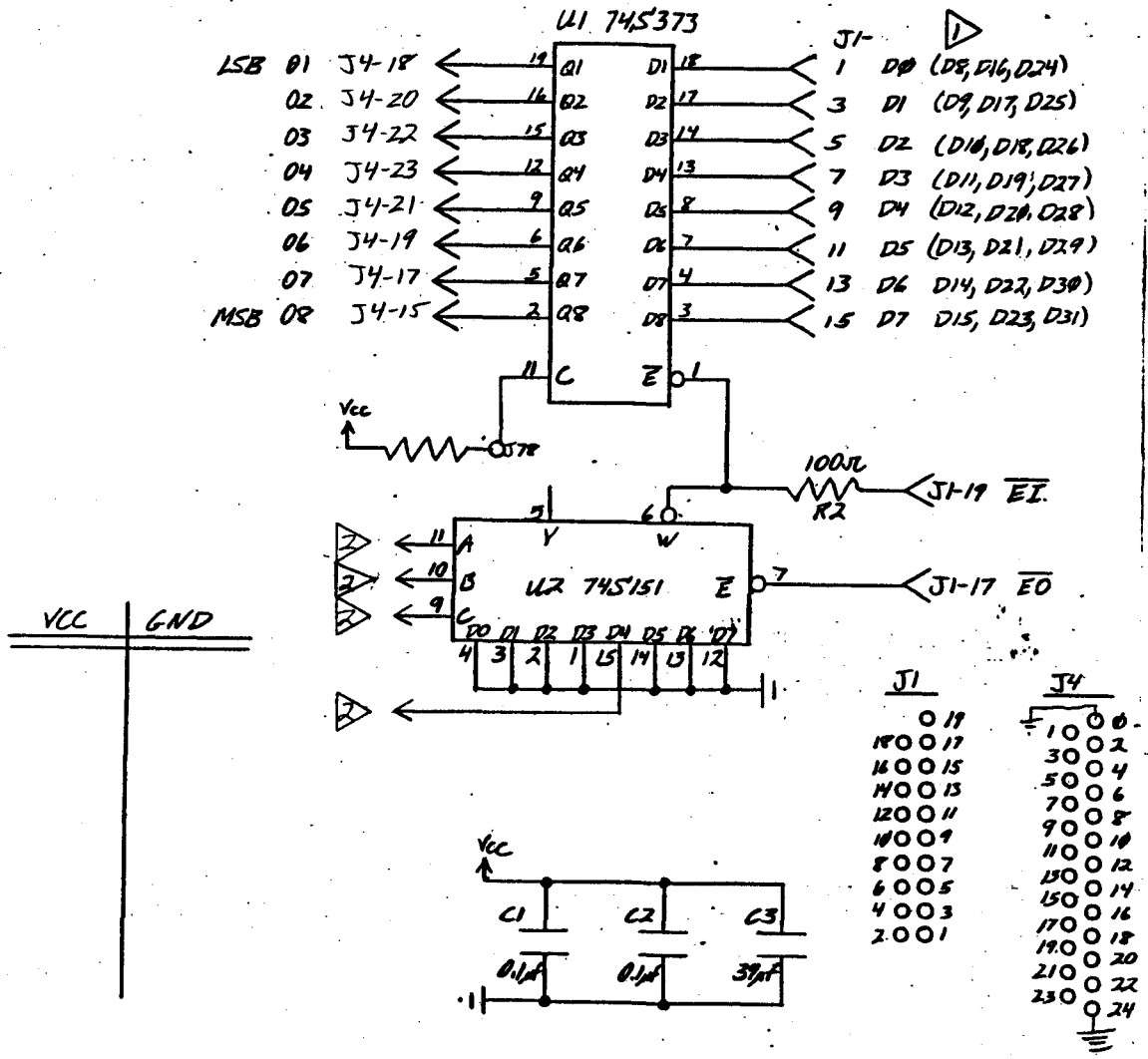
J1: 1 3 5 7 9 11 13 15 17 19 21 23 25 / 2 4 6 8 10 12 14 16 18 20 22 24 26

J2: 1 3 5 7 9 11 13 15 17 19 21 23 25 / 2 4 6 8 10 12 14 16 18 20 22 24

J4: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256×8, 512×8, 1K×8 STANDARD			
DRAWN	DATE	APPROVED	DATE
[illegible]	1/7/78		
DWG NO 0001016		SHT 1/2	

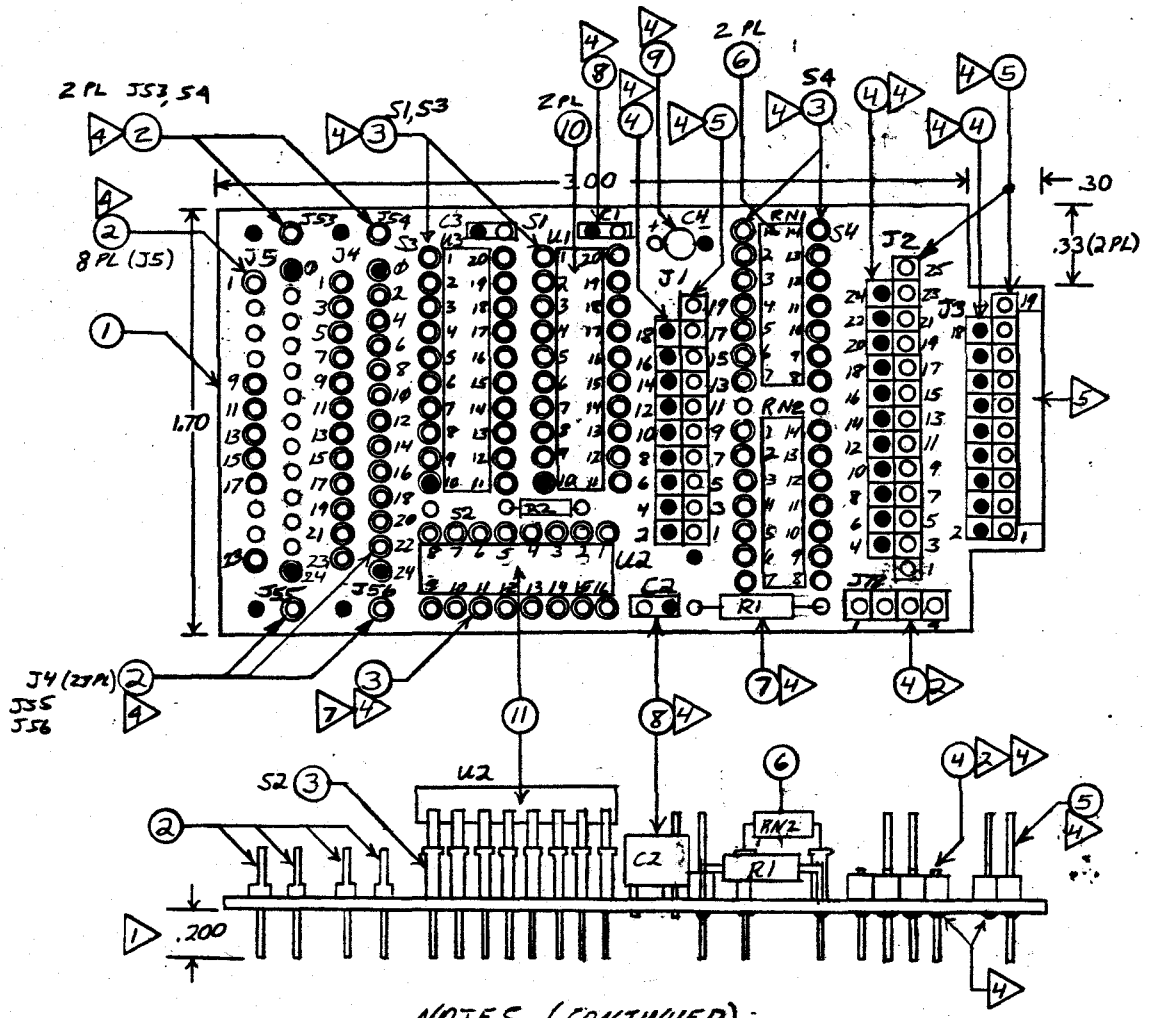
SLAVE (VERSIONS 005, 006)



PINOUT VERSION CHART

VER	DESCRIPTION	RN1-3	RN1-2	RN1-5	RN1-4	U2-9	U2-11	U2-15	U2-10
01	256X8 MASTER	J4-24	J4-0	J53	J54	J4-11	J4-7	J4-13	J4-9
02	512X8 MASTER	J4-24	J4-0	J4-3	J54	J4-11	J4-7	J4-13	J4-9
03	1KX8 MASTER	J4-24	J4-0	J4-3	J4-5	J4-11	J4-7	J4-13	J4-9
04	1KX8 (2708)MAS	J4-24	J4-0	J4-3	J4-5	J78	GND	J78	J4-9
05	8 BIT SLAVE	—	—	—	—	J4-11	J4-7	J4-13	J4-9
06	8BIT (2708)SL	—	—	—	—	J78-2	GND	J78-3	J4-9
~~07~~	~~SIXB MASTER~~	~~J54~~	~~J53~~	~~J4-3~~	~~J5-3~~	~~J4-11~~	~~J4-7~~	~~J4-13~~	~~J4-9~~
08	1KX8 (4KX8)M	J54	J53	J4-3	J4-5	J78-2	J55	J78-3	GND
09	1KX8 (4KX8)S	—	—	—	—	J78-2	J55	J78-3	GND
10	4KX8 (2732)M	J4-11	J4-7	J4-5	J4-5	J78-2	J4-13	J78-3	J4-9
11	4KX8 (2732)S	—	—	—	—	J78-2	J4-13	J78-3	J4-9
12	256,512,1KSLAVE	—	—	—	—	J78-2	J55	J78-3	U2-4
13	256X8 MASTER	J4-24	J4-0	J53	Q541	J78-2	J55	J78-3	U2-4
14	512X8 MASTER	J4-24	J4-0	J4-3	J54	J78-2	J55	J78-3	U2-4
15	512X8 (2K)MASTER	J54	J4-24	J4-3	J53	J78-2	J55	J78-3	U2-4
16	2KX8 (2K) MASTER	J4-7	J4-24	J4-3	J4-5	J4-11	U2-4	J4-13	J4-9
17	2KX8 (2K) SLAVE	—	—	—	—	J4-11	U2-4	J4-13	J4-9
18	2KX8 (4K) MASTER	J4-7	J54	J4-3	J4-5	J78-2	J55	J78-3	U2-4
19	2KX8 EPROM MASTER	J4-11	J4-24	J4-3	J4-5	J78-2	J4-9	J78-3	J4-13
20	2KX8 EPROM SLAVE	—	—	—	—	J78-2	J4-9	J78-3	J4-13

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 256×8, 512×8, 1K×8 STD			
DRAWN	DATE	APPROVED	DATE
DWG NO 0001016		SHT 2/2	



NOTES (CONTINUED)

MODIFY PCB TRACES — ALL VERSIONS

7. CUT SHORTING TRACES BETWEEN U2-1, 2, 3, 4. CUT SHORTING TRACES BETWEEN U2-12, 13
   - CUT TRACES FROM U2-6 TO U1-1 AND U3-1
   - CUT TRACE FROM J3-1 TO R3-2

REVISIONS

LTR	REV NO	REASON	BY	DATE
TA		SCHEMATIC ERRORS	[illegible]	10/17
TB		MSB-LSB ERROR	SHD	1/3/78
C		DELETE VERSION 3, 4, 6. ADD VERSION 7. CHANGE TO MASTER ONLY	Kem	26/JAN
D		CHANGE ITEM 6 TO BE 33 PL	[illegible]	2/2/79
E		ADD R2 100Ω ¼Ω	[illegible]	5/3/79
F		CHNG ITEM 2	[illegible]	7/18/79
G	34	DEL SHT 3	[illegible]	3/7/80
H	37	DEL PART OF 4	SHD	6/3/80

NOTES: UNLESS OTHERWISED SPECIFIED

1. CUT LEADS WHERE NECESSARY TO .200 INCH AFTER ASSY IS WIREWRAPPED.
2. INSTALL POST WITH LONG PIN DOWN TRIM TOP POST FLUSH WITH INSULATOR
3. PINS CALLED OUT AS "GND" ON WIRE LIST SHOULD BE SOLDERED TO GROUND PLANE, FAR SIDE
4. ITEM 2, 3, 4, 5, 7, 8, 9 TO BE SOLDERED TO BOARD FAR SIDE
5. MARK ASSY NO IN SPACE INDICATED
6. ASSY NO SHALL BE DWG NO-VERSION-REV LTR

STEP ENGINEERING			
ASSEMBLY, BUFFER BOARD 2K WORD MASTER			
DRAWN [illegible]	DATE 7/23/77	APPROVED	DATE
DWG NO 0001017			SHT 1/2

VERSION CHART

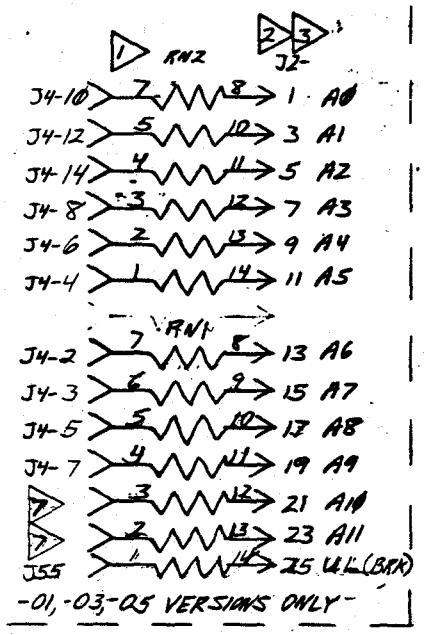
VERSION	DESCRIPTION	SCHEM NO
-001	BUFFER, DUAL 2K x 4 (18 PIN)	0001021-001
-002	BUFFER, 2K x 8 (24 PIN)	0001022-001
-003		
-004	BUFFER, 2K x 8 (24 PIN AJ VERSION)	0001022-006
-005	BUFFER, 2K x 8 (24 PIN GE VERSION)	0001022-003
-006	BUFFER, 8K x 8 (24 PIN)	0001022-010
-007		
-008		
-009		
-010		
-011		
-012		

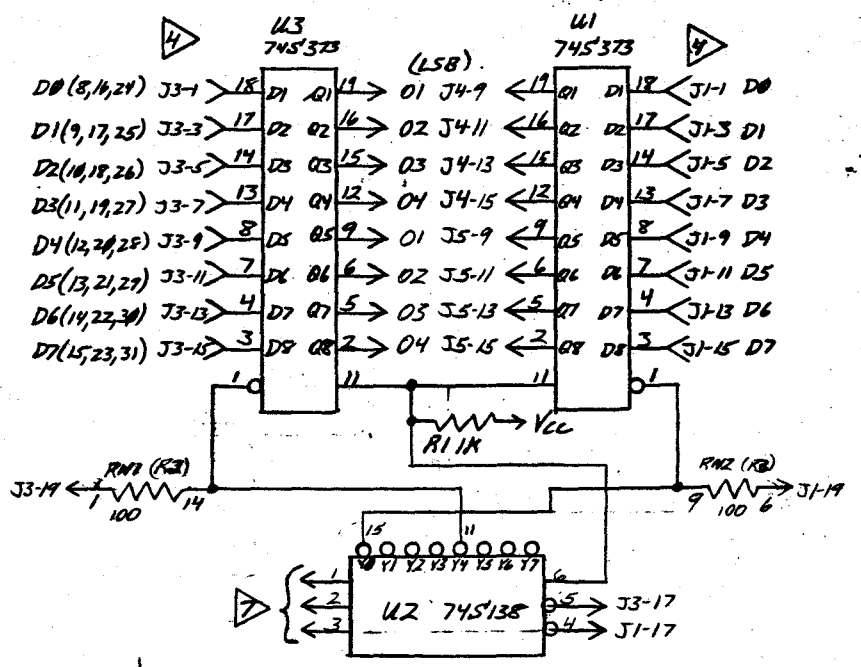
PARTS LIST

PART NO	REF DESIG	DESCRIPTION	QUANTITY	PART NUMBER
1	———	PC BOARD, BUFFER GEN PURPOSE	1	0001018-001
2	J1, J2, J3, J4	STRIP LINE PLUG, WW, .50 LONG	4	CA-536SP100-170-500
3	S1, S2, S3, S4	LEAD SOCKET, WIRE WRAP PINS	84	AUGAT LSG-1FG10-1
4	J1, J2, J3, J4	STRIP LINE PLUG, WW, .43 LONG	3/4	CA-536SP100-230-430
5	J1, J2, J3	STRIP LINE PLUG, WW, .60 LONG	2/3	CA-536SP100-230-600
6	RN1, RN2	RESISTOR PACK 33 OHM WW 5% 8 PIN	2	BOURNS 4114R-001-330
7	R1	RESISTOR, 1K OHM, 10%, 1/4W	1	RC07GF102K
8	C1, C2, C3	CAPACITOR, CERAMIC 0.1 mf	3	CENTRALAB CY20C104P
9	C4	CAPACITOR, TANTALUM, 39 mF, 10V	1	SPRAGUE 196D396X9010KA1
10	U1, U3	OCTAL "D" TYPE TRANSPARENT LATCH	2	74S373
11	U2	THREE TO EIGHT LINE DECODER	1	74S138
12	———	SOLDER, ROSEN CORE	AIR	
13	———	WIRE, KYNER COATED, 30 AWG, STRIPPED, 3" LONG	AIR	AUGAT 1410-KG11
14	———	WIRE, KYNER COATED, 30 AWG, STRIPPED, 4" LONG	AIR	AUGAT 1410-KG12
15	———	WIRE, KYNER COATED, 30 AWG, STRIPPED, 5" LONG	A/R	AUGAT 1410-KG13
15	———	SCHEMATIC	REF	SEE VERSION CHART
16	R2	RESISTOR, 100Ω 1/4 WATT	1	RC07GF101K

STEP ENGINEERING

DWG NO 0001017 SHT2





REVISIONS				
LTR	REV NO	REASON	DATE	BY
TB		REVISED PER MEMO	3/20	SMP
C	026	ADD VER 05 THRU 06	7/20/78	SMP

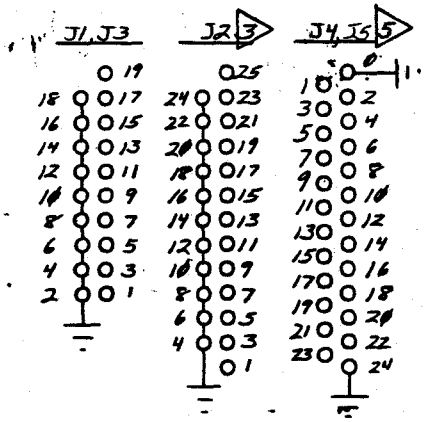
NOTES: UNLESS OTHERWISE SPEC:

1. RN1, RN2 100Ω RESISTOR PACKS
2. J2 PINS 2, 26 REMOVED FOR KEYING
3. RN1, RN2, J2 ONLY PRESENT ON 01, 03, 05 VERSIONS
4. J1, J3 PIN 20 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG
6. WARNING: CS (DIP PIN 10) MUST BE LOGIC LOW ON BOTH DIP PLUGS FOR OUTPUTS TO BE ENABLED ON VER 01, 02
7. REFER TO VERSION CHART FOR PINOUT

VERSION CHART 7

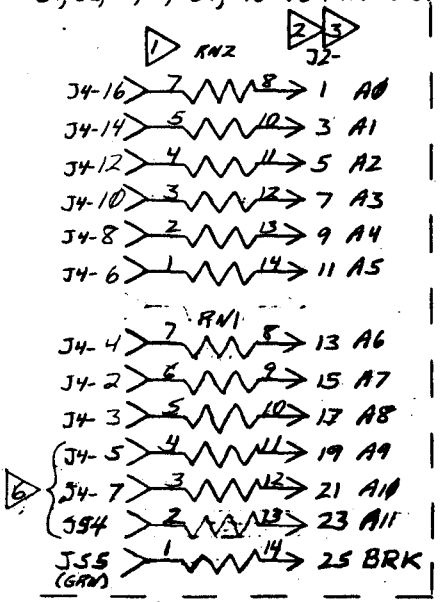
VER	U2-1	U2-2	U2-3	RN1-2	RN1-3	DESCRIPTION
001	J4-17	J5-17	J4-16	J4-24	J4-16	2K×4 M (2K ROM)
002	J4-17	J5-17	J4-16	—	—	2K×4 S (2K RAM)
003	J54	U2-8	J53	J4-24	J53	2K×4 M FOR 1K ROM
004	J55	U2-8	J56	—	—	2K×4 S FOR 1K RAM
005	J54	U2-8	J56	J53	J4-16	8K×4 M FOR 2K ROM
006	J55	U2-8	J56	—	—	8K×4 S FOR 2K ROM
007				—	—	
008				—	—	

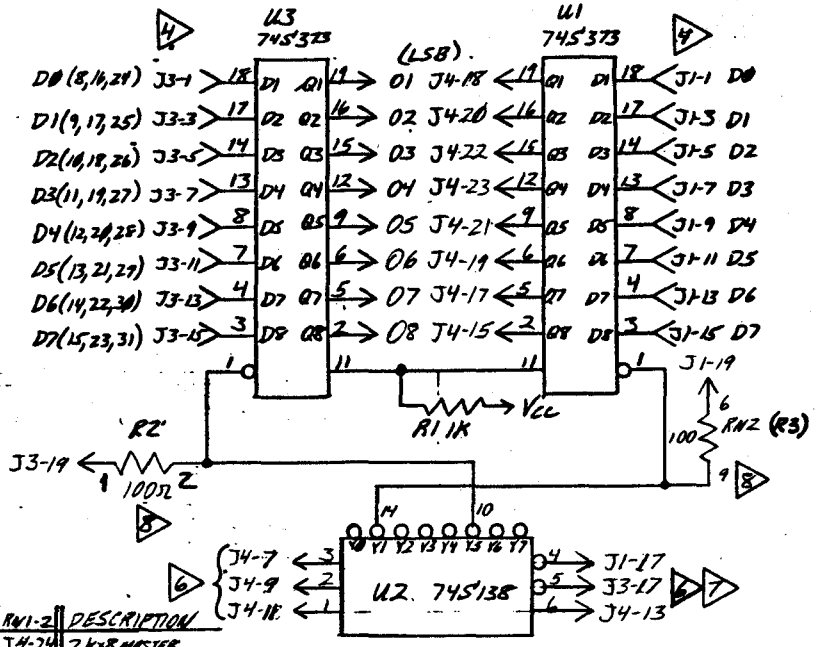
U1-20 U2-16 U3-20 R1 J4-1	J1, J3-2, 4, 6, 8, 10, 12, 14, 16, 18, 20 J2 - 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 J4, J5-0, 24 U1, U3 - 10 U2 - 8
VCC	GND



STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD DUAL 2K×4, MULT			
DRAWN SMP	DATE 3/20/78	APPROVED	BY
DWG NO 0001021		SHT 1/1	

-01,-03,-05,-07,-09,-10 VERSIONS ONLY

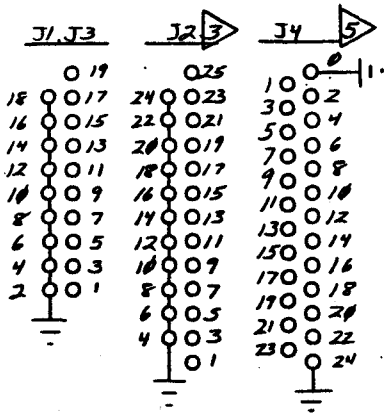




VERSION CHART 6

VER	U2-3	U2-2	U2-1	U2-6	RN1-4	RN1-3	RN1-2	DESCRIPTION
01	J4-7, RN1-3	J4-9	J4-11	J4-18	J4-5	*	J4-24	2K×8 MASTER
02	J4-7	J4-9	J4-11	J4-13	—	—	—	2K×8 SLAVE
03	J54, RN1-3	J4-9	J4-11	J4-13	J53	*	J4-24	2K×8 MASTER SPECIAL 7
04	J55	J4-9	J4-11	J4-13	—	—	—	2K×8 SLAVE SPECIAL
05	RN1-3, J56	U2-8	J4-11	J4-13	J4-7	*	J4-24	512×8 (2K) MAS "
06	J55	U2-8	J4-11	J4-13	—	—	—	512×8 (2K) SLAVE "
07	RN1-3, J4-11	J4-9	J78-3	J78-4	J4-5	*	J4-24	2K×8 EPROM MASTER
08	J4-11	J4-9	J78-3	J78-4	—	—	—	2K×8 EPROM SLAVE
09	J56	J4-9	J4-11	J4-13	J4-5	J53	J54	1K×8 (8K) MASTER
10	J56	J4-9	J4-11	J4-13	—	—	—	1K×8 (8K) SLAVE
11	J53	J56	J78-3	J78-3	J4-6	J4-7	J54	2K×8 (8K) MASTER
12	J55	J56	J78-4	J78-4	—	—	—	2K×8 (8K) SLAVE
13	J56	J4-9	J4-13	J78-4	J4-5	J4-11	J4-7	4K×8 (8K) MASTER
14	J56	J49	J4-13	J78-4	—	—	—	4K×8 (8K) SLAVE
15	J56	J54	J53	J78-4	J4-5	J4-11	J4-7	4K×8 (8K) MASTER
16	J56	J54	J53	J78-4	—	—	—	4K×8 (8K) SLAVE

R1
U3-20 J4-24
U1,U3 12 10
U2-16
U1-20
VCC GND
U2-8
J2-2,4,6,8,10,12,14,16,18,20,22,24
J1,J3 PINS 2,4,6,8,10,12,14,16,18,20



REVISIONS				
LTR	REV NO	REASON	DATE	BY
TB		REVISED & REDRAWN	3/20/78	SMD
TC		ADD U1, VER -003, 004	7/7/78	SMD
TD		ADD VERSION 010 + 011	5/10/79	SMD
E	0026	ADD VER 7,8,11,12 YMAD	2/1/80	SMD
F	37	SWITCH R2 & R3	6-3-80	SMD
G		UPDATE DWG	8-22-80	DA

NOTES: UNLESS OTHERWISE SPEC:

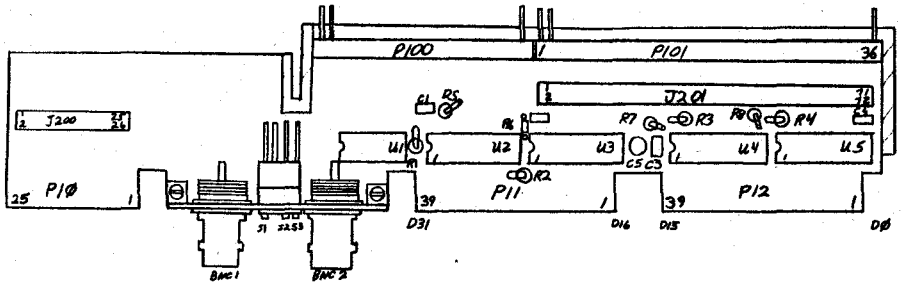
1. RN1, RN2 100Ω RESISTOR PACKS
2. J2 PINS 2,26 REMOVED FOR KEYING
3. RN2, J2 ONLY PRESENT ON -001 VERSION
4. J1, J3 PIN 20 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG
6. PINOUT FOR -001, -002 VERSIONS SHOWN. FOR OTHER VERSIONS SEE VERSION CHART
7. ON -03 AND -04 VERSIONS: U2-5 CONNECTED TO J4-7
8. ODD NUMBER VERSIONS, MASTERS, USE RN1, RN2 FOR SERIES TERMINATIONS; EVEN NUMBER VERSIONS, SLAVES, USE R3, R2.

STEP ENGINEERING

SCHEMATIC, BUFFER BOARD 2K×8

DRAWN SMD DATE 3/20/78 APPROVED BY

DWG NO 0001022 SHT 1/1



DEVICE	GND
U1	PIN 7
U2	PIN 10
U3	PIN 10
U4	PIN 10
U5	PIN 10
P10	2 THRU 26 EVEN
P11	2 THRU 40 EVEN
P12	2 THRU 40 EVEN
P100	22 THRU 40 EVEN
P101	1,2,35,36

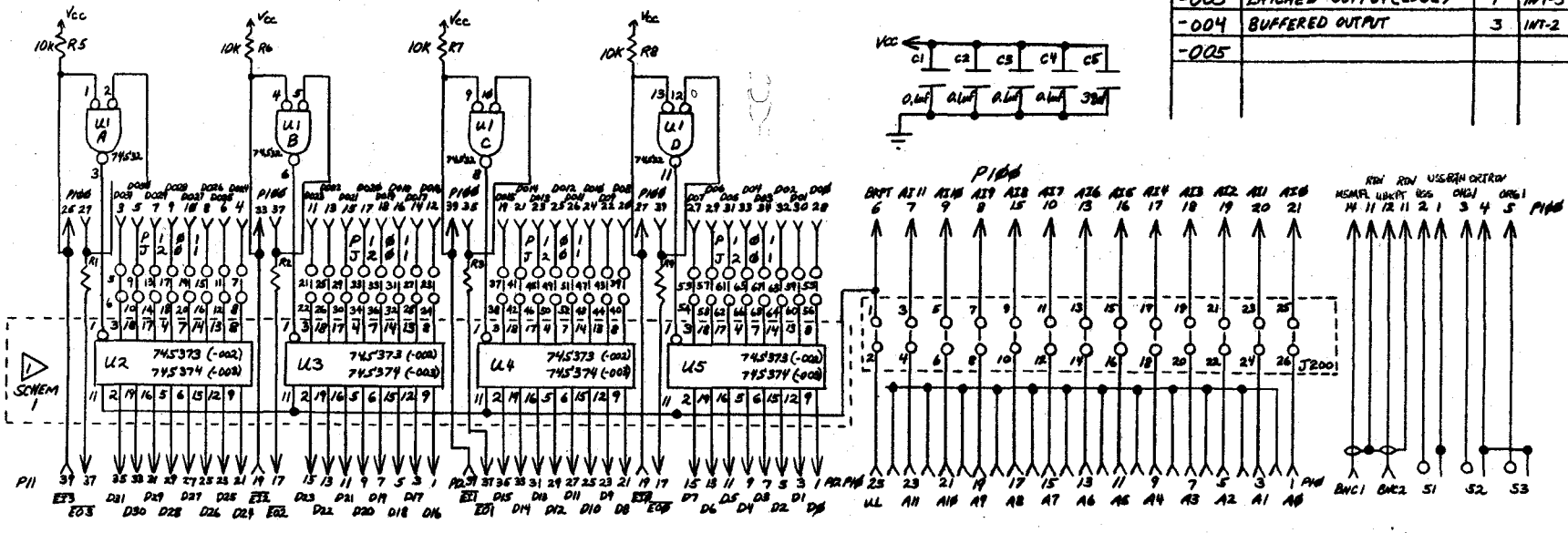
DEVICE	VCC
U1	PIN 14
U2	PIN 20
U3	PIN 20
U4	PIN 20
U5	PIN 20
P100	PIN 4,5,6

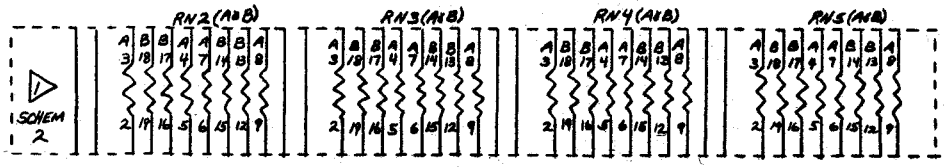
REVISIONS

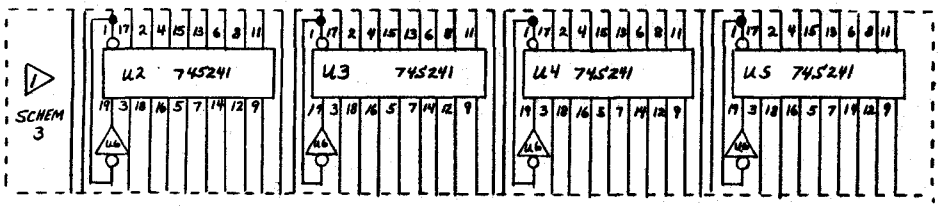
LTR	REV NO	REASON	DATE	BY
TA		PRELIMINARY RELEASE	4/7	
TB		RELEASE P10, P11, P12	12/30	
C		ADD R5, R6, R7, R8 PROD RLSE	1/19/78	
D	9	ADD J200-1 TO P100-6	5/4/78	
D1		RENUMBER J201 ADD NOTE 3		

VERSION CHART

DASH NO	DESCRIPTION	SCHEM NO	MODEL NO	PART NO
-001	RESISTIVE TERMINATION	2	INT-1	0001040-001
-002	BUFFERED OUTPUT (WITH LATCH)	1	INT-2,4	0001040-002
-003	LATCHED OUTPUT (EDGE)	1	INT-3	0001040-003
-004	BUFFERED OUTPUT	3	INT-2	0001040-004
-005				







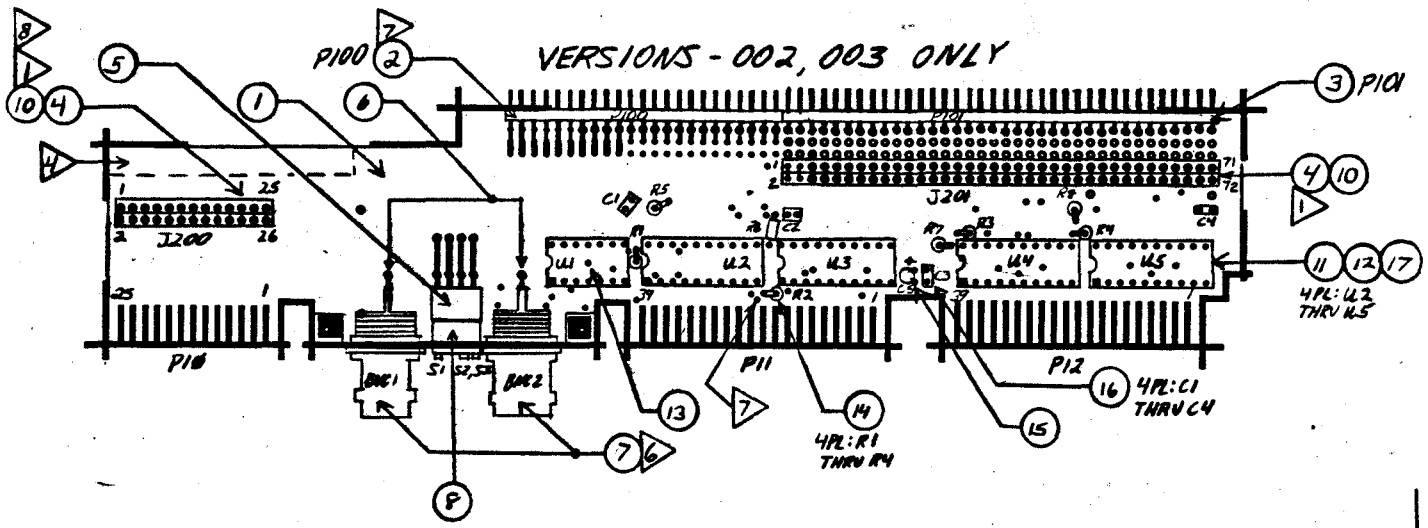
NOTES

1. FOR PROPER SCHEMATIC REFER TO VERSION CHART
2. ALL RESISTORS 91Ω - 1/4 WATT (EXCEPT R5-R8)
3. J200, J201 ARE WIREWRAPPED SUCH THAT D31 IS CONNECTED TO D31, D30 TO D30, ETC.
4. DASH -004 CANNOT BE ASSEMBLED WITHOUT ARTWORK MODIFICATIONS. CONSIDER THIS VERSION TO BE AN ENGINEERING VERSION ONLY

STEP ENGINEERING

SCHEMATIC, MEMORY INTERFACE BOARD

DWG NO 0001039 SHT 1/1



FOR NOTES SEE SHT 2

CHART 1 : PARTS LIST

ITEM	REF DESIG	DESCRIPTION	PART NUMBER	QTY -001	QTY -002	QTY -003	QTY -004
1	———	PC BOARD	0001035	1	1	1	
2	P100	STRIP LINE PLUG, DUAL 46 POS, .1" CTR, RIGHT ANGLE	CA D46 RSP100-310-.090	1	1	1	
3	P101	STRIP LINE PLUG, 36 POS, .1" CTR, RIGHT ANGLE	CA S36 RSP100-420-.090	1	1	1	
4	J200, J201	STRIP LINE PLUG, DUAL 72 POS, .1" CTR, STRAIGHT	CA D72 SP100-.230-.430	1½	1½	1½	
5	(S1 THRU S3)	RIGHT ANGLE DIP SOCKET, 8 POSITION	CA 08SE-10RAC3-01	1	1	1	
6	———	WIRE, SOLID, 24 GA, BARE	ALPHA #299 OR EQUIV	A/R	A/R	A/R	
7	BNC1, BNC2	BNC RECEPTACLE, STRAIGHT BULKHEAD MNT	MIL # MLE-10894/14	2	2	2	
8	S1 THRU S3	SWITCH, DIP, 4 POSITION SPST	MOLEX 01-70-0104	1	1	1	
9							
10	———	WIRE, SOLID, 30 GA SILVER COATED, BARE	ALPHA #5951 (STRIPPED)	A/R	A/R	A/R	
11	U2 THRU U5	INTEGRATED CIRCUIT, OCTAL SHIFT THRU LATCH	SN 74S373N-00	—	4	—	
12	U2 THRU U5	INTEGRATED CIRCUIT, OCTAL EDGE TRIG LATCH	SN 74S374N-00	—	—	4	
13	U1	INTEGRATED CIRCUIT, QUAD 2 INPUT OR GATE	SN 74S32N-00	—	1	1	
14	R1 THRU R4	RESISTOR, 51 OHM ±5%, 1/4 W, CARBON	RC07GF510J	4	4	4	
15	C5	CAPACITOR, 39 μF, 10 VOLT, TANTALUM	SPRAGUE 196D396X9010KA1	—	1	1	
16	C1 THRU C4	CAPACITOR, .01 μF, CERAMIC	CENTRALAB CY20C104P OR EQUIV	—	4	4	
17	(U2 THRU U5)	SOCKET, IC, 20 PIN	AUGAT 720-AG2D OR EQUIV	—	4	4	
18	RN1 THRU RN4	RESISTOR NETWORK 100 OHMS ±5%, 1/4 W	CTS 784-3-R100	8	—	—	
19	(REF)	SCHEMATIC, MEMORY INTERFACE BOARD	(0001039)	—	—	—	
20	R5 THRU R8	RESISTOR 10K OHM 1/4 W, 10%	RC07GF103J	4	4	4	
21							

8

LTR	REV #	REASON	BY	DATE
E		CHANGE FROM 14 TO 8E SIA RC07GF510J	[illegible]	2/2/79
D1		CHANGE ITEM 17 VENDOR ADD NOTE 8	KEM	2/7/78
D	9	ADD NOTE 7	[illegible]	5/25/78
C		DELETE ITEMS, ADD ITEM 17 RLSE	[illegible]	3/9/78
TB		ADD AS THRU #7	[illegible]	11/2/77
TA	———	PRELIMINARY RLSE	[illegible]	11/9/77

REVISIONS

STEP ENGINEERING			
ASSEMBLY, MEMORY INTERFACE BOARD			
DRAWN	DATE	APPROVED	DATE
[illegible]	10/8/77		
DWG NO 0001040			SHT 1/2

1040 SH1 REV E

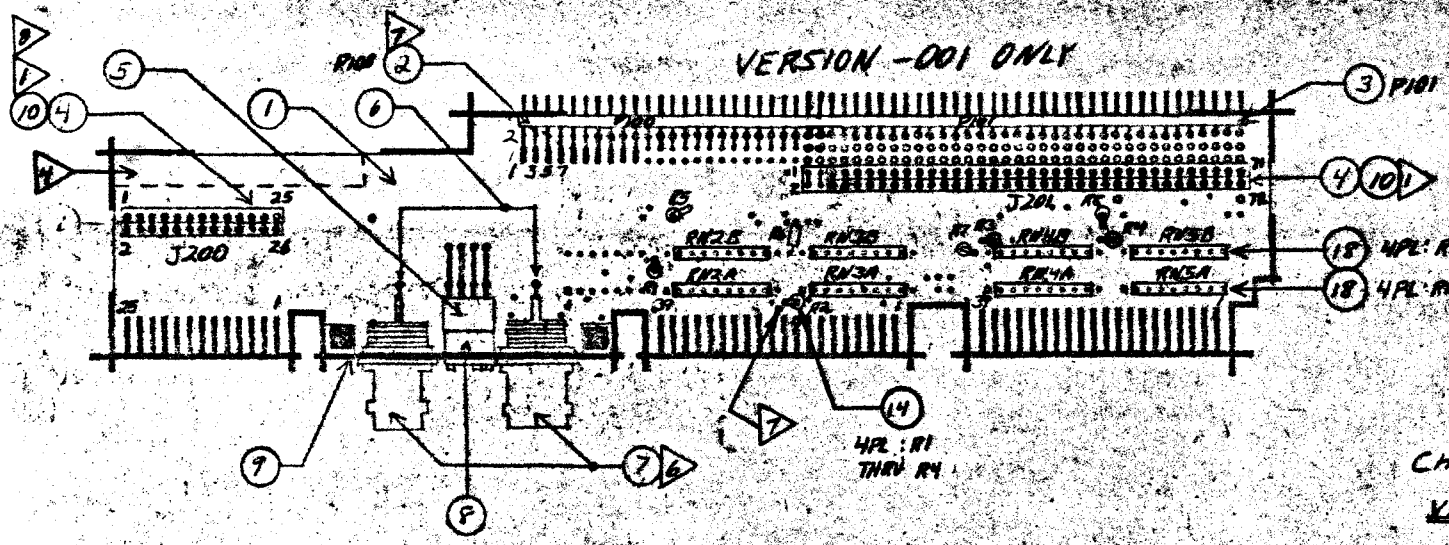


CHART 2 : PART NUMBER (5)

VERSION	PART NUMBER
-001	1040-001
-002	1040-002
-003	1040-003

NOTES: UNLESS OTHERWISE SPECIFIED

(1) ON J200 AND J201 WIREWRAP PINS 1 TO 2; 3 TO 4; 5 TO 6; ETC USING ITEM 10, WIRE

(2) SQUARE PAD MARKS PIN 1 ON ULTIMO UG.

(3) PART NUMBER TO BE PER CHART 2 PLUS DRAWING REVISION LETTER

(4) MARK PART NUMBER AND SERIAL NUMBER WITHIN DASHED AREA

(5) VERSIONS -002, -003 INTERCHANGEABLE BY CHANGING U2 THRU U5

(6) SOLDER ITEM 7, BNC, DIRECTLY TO PC BD WITH FLAT SIDE DOWN. SPACE BNC APPROX 0.1 INCH FROM SWITCH ASSY.

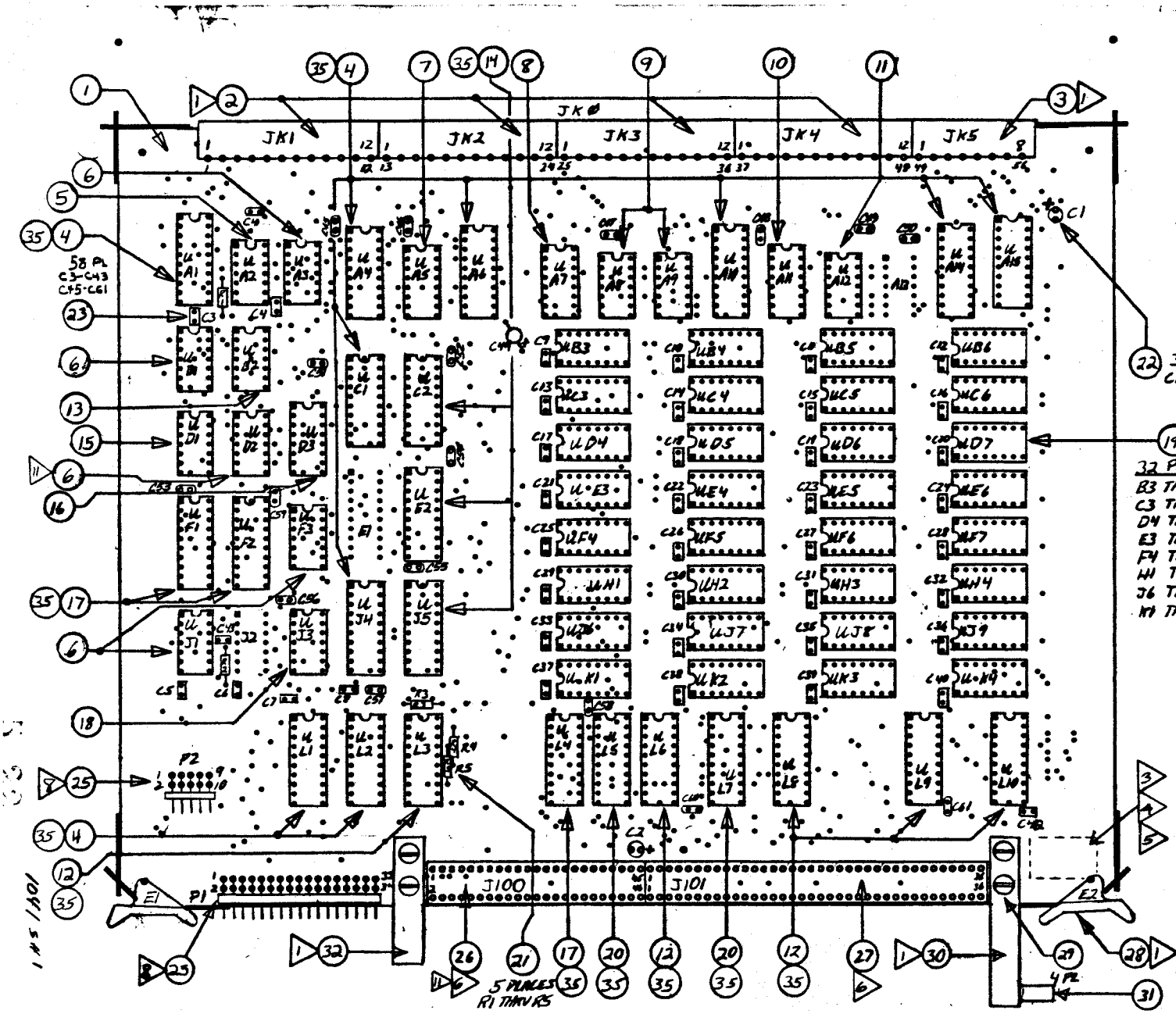
(7) ADD 30GA WIRE (UNSH) FROM E102-6 TO PAD SHOWN (ON CIRCUIT SIDE OF PCB) THIS PAD IS ELECTRICALLY TIED TO J200, PIN 1.

(8) 72 PIN DUAL STRIP LINE PLUG MUST BE CUT INTO SHORTER LENGTHS PRIOR TO ASSEMBLY INTO J200 (26 PIN DUAL). TWO J200 CONNECTORS MAY BE MADE FROM A SINGLE PART.

STEP ENGINEERING			
ASSEMBLY, MEMORY INTERFACE BOARD			
DRAWN	DATE	APPROVED	DATE
DWG NO 0001040			SHT 2

5 21

1040 SHT 2



REVISIONS				
LTR	REV NO	REASON	DATE	BY
TA	—	PRELIMINARY RLSE	11/17	
TB	—	CHNG L3 FROM LS240 TO 244	12/5	
TC	—	ADD C45 THRU C58	3/1	
D	—	ADD ITEMS 35,36 (ASSEMBLY) RELEASE	3/14/78	
E	9	ADD NOTE 11, 12	5/11/78	
E1		REVISED ALL NOTES CORRECT PART NR ITEM 30	25/7/78	KCM

NOTES:
SEE SHEET 2

STEP ENGINEERING			
ASSEMBLY, MEMORY MODULE 1K x 32			
DRAWN	DATE	APPROVED	DATE
	11/17/77		
DWG NO 0001041		SNT 1/2	

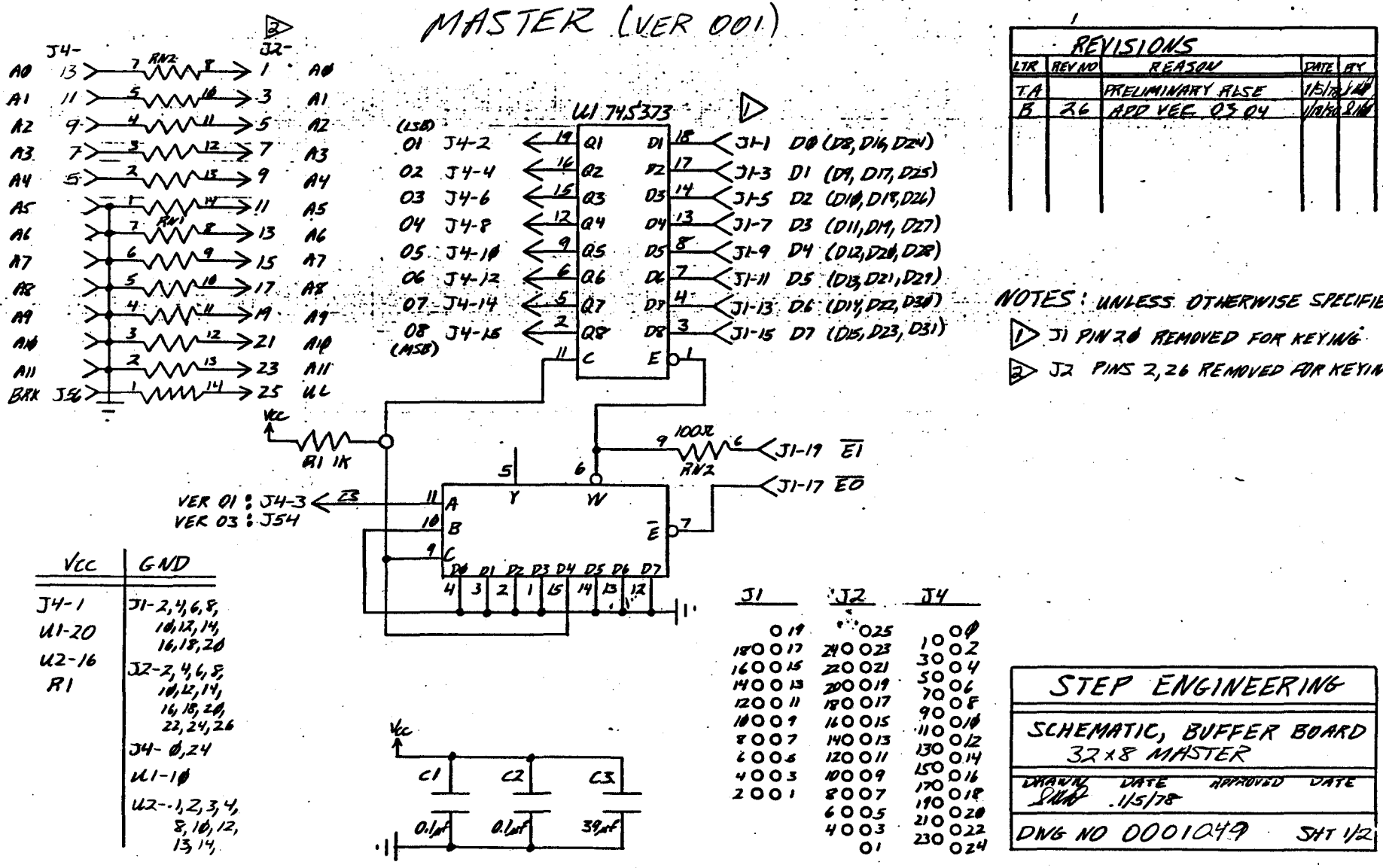
ITEM NO	REF DESIG	DESCRIPTION	QTY	PART NUMBER
36	2	LEAD SOCKET CARRIER ASSY, 16 PIN	32	AUGAT 716-AG2D
35	9	LEAD SOCKET CARRIER ASSY, 20 PIN	23	AUGAT 720-AG2D
1	—	PC BOARD, MEM 32	1	0001036
2	JK1 THRU JK4	RIGHT ANGLE PC BOARD CONN: 12 POS	4	MOLEX 09-52-3121
3	JK5	RIGHT ANGLE PC BOARD CONN: 8 POS	1	MOLEX 09-52-3081 OR TYCO 09-52-3041
4	A1, A4, A6, A10, A13, A19, A14	IC, OCTAL TRISTATE BUFFER	10	SN74LS240N OR EQUIV
5	A2	IC, 8 INPUT POSITIVE NAND GATE	1	SN74LS30N OR EQUIV
6	A3, B1, D2, J1, F3	IC, QUAD EXCLUSIVE OR	5	SN74S86N OR EQUIV
7	A5	IC, 3 TO 8 LINE DECODER	1	SN74LS138N OR EQUIV
8	A7	IC, 4 BIT MAGNITUDE COMPARATOR	1	SN74LS85N OR EQUIV
9	A8, A9	IC, QUAD 2 INPUT NAND GATE	2	SN74LS00N OR EQUIV
10	A11	IC, DUAL 2 TO 4 LINE DECODER	1	SN74LS139N OR EQUIV
11	A12	IC, DUAL 4 INPUT POSITIVE NAND SCHMITT TRIGGER	1	SN74LS13N OR EQUIV
12	L8, L9, L10, L6, L13	IC, OCTAL BUFFER	5	SN74LS244N OR EQUIV
13	B2	IC, QUAD 2 INPUT SCHMITT TRIGGER	1	SN74LS132N OR EQUIV
14	C2, E2, J5	IC, OCTAL TRISTATE BUFFER	3	SN74S240N OR EQUIV - CERAMIC PREFERRED
15	D1	IC, QUAD 2 INPUT NAND GATE	1	SN74S00N OR EQUIV
16	D3	IC, 13 INPUT POSITIVE NAND GATE	1	SN74S133N OR EQUIV
17	F1, F2, L4	IC, OCTAL LATCH	3	SN74LS377N OR EQUIV
18	J3	IC, 50 OHM LINE DRIVER	1	SN74128N OR EQUIV
19	3	IC, 1K×1 RAM, TRISTATE 30NS ACCESS	32	93425ADC OR EQUIV
20	L5, L7	IC, OCTAL D TYPE FLIP FLOP	2	SN74S374N, SN74LS374N OR EQUIV 12
21	R1 THRU R5	RESISTOR 1K OHM 10% ¼ W	5	RC07GF102K
22	C1, C2, C44	CAPACITOR, TANTALUM 39μF, 10V	3	SPRAGUE 196D396X9010KA1
23	C3 THRU C43 C45 THRU C61	CAPACITOR, CERAMIC 0.1μF	58	CENTRALAB CY20C104P
24				
25	P1, P2	STRIP LINE PLUG, DUAL RIGHT ANGLE, 34 POS	1⅓	CA D34RSP100-.230-.090 8
26	J100	PC CARD CONN, DOUBLE ROW, 23 CONTACTS/ROW	1	BERG 65000-32 OR EQUIV
27	J101	PC CARD CONN, SINGLE ROW, 36 CONTACTS	1	BERG 65001-58 OR EQUIV
28	E1, E2	CARD EJECTOR .375 WIDE	2	SCANBE S-200
29	—	SCREW, MACHINE, ROUND HEAD, 6-32, 3/8", CAD PLATE	4	SAMSH 1001C, 1426C OR EQUIV
30	—	CARD GUIDE	1	0001044-001
31	—	KNURLED THUMBSCREW #6-32	1	OR EQUIV
32	—	CARD GUIDE	1	0001044-002
33	—	SCHEMATIC, MEMORY MODULE, 1K×32	—	REF DWG 0001001
34				

NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL ITEMS 2 & 3, PC BOARD CONN, ITEM 28, CARD EJECTOR, ITEMS 30, 32, CARD GUIDES AFTER WAVE SOLDERING.
2. REF DESIGNATIONS FOR ITEMS 19 + 36, 1K×1 RAMS; B3 THRU B6, C3 THRU C6, D4 THRU D7, E3 THRU E6, F4 THRU F7, H1 THRU N4, J6 THRU J9, K1 THRU K4.
3. PART NUMBER TO BE 0001041 PLUS DRAWING REVISION LETTER
4. PART NUMBER AND SERIAL NUMBER TO BE MARKED IN AREA SHOWN.
5. SERIAL NUMBER TO BE "M" - YEAR(1) - MONTH(2) - DAY(2) - SEQUENTIAL NUMBER(2)
   EXAMPLE IS: M805121A (14TH UNIT ON 12 MAY '78)
   DATE WILL BE INSPECTION DATE AFTER ASSEMBLY.
6. INSTALL ITEMS 26 + 27 WITH OPEN EDGES AT CARD EDGE
7. SQUARE PAD MARKS PIN 1 OF ALL IC's
8. INSTALL ITEM 25 SUCH THAT RIGHT ANGLE SECTION IS SOLDERED TO PCB. 34 POSITION DUAL PLUG MUST BE CUT INTO SHORTER LENGTHS (10 POSITION) PRIOR TO ASSEMBLY INTO P2.
   (THREE P2 PLUGS MAY BE MADE FROM ONE PART)
9. REFERENCE DESIGNATORS FOR 20 PIN IC SOCKETS ARE: A1, A4, A6, A10, A13, A19, C1, C2, E2, F1, F2, J4, J5, L1 THRU L10
11. CUT TRACES: GND TO J100-6 (SOLDER SIDE); GND TO P2-5 (COMP SIDE) 1D-12 TO 1D-13 (COMP SIDE)
    RUN 30GA WIRE (UNSUL) FROM 1D-12 TO J100-6 AND P2-5, SOLDER SIDE
12. SN74LS374N PREFERRED

STEP ENGINEERING
DWG NO 0001041 SHT 2

MASTER (VER 001)



REVISIONS				
LTR	REV NO	REASON	DATE	BY
TA		PRELIMINARY RLSE	1/5/78	JMP
B	26	ADD VEE, Q3 Q4	1/26/78	JMP

NOTES: UNLESS OTHERWISE SPECIFIED

1. J1 PIN 20 REMOVED FOR KEYING
2. J2 PINS 2, 26 REMOVED FOR KEYING

Vcc	GND
J4-1	J1-2,4,6,8, 10,12,14, 16,18,20
U1-20	J2-2,4,6,8, 10,12,14, 16,18,20, 22,24,26
U2-16	J4- 0,24
R1	U1-10
	U2-1,2,3,4, 8,10,12, 13,14,

J1	J2	J4
19	25	0
18 17	24 23	1 2
16 15	22 21	3 4
14 13	20 19	5 6
12 11	18 17	7 8
10 9	16 15	9 10
8 7	14 13	11 12
6 5	12 11	13 14
4 3	10 9	15 16
2 1	8 7	17 18
	6 5	19 20
	4 3	21 22
	1	23 24

STEP ENGINEERING

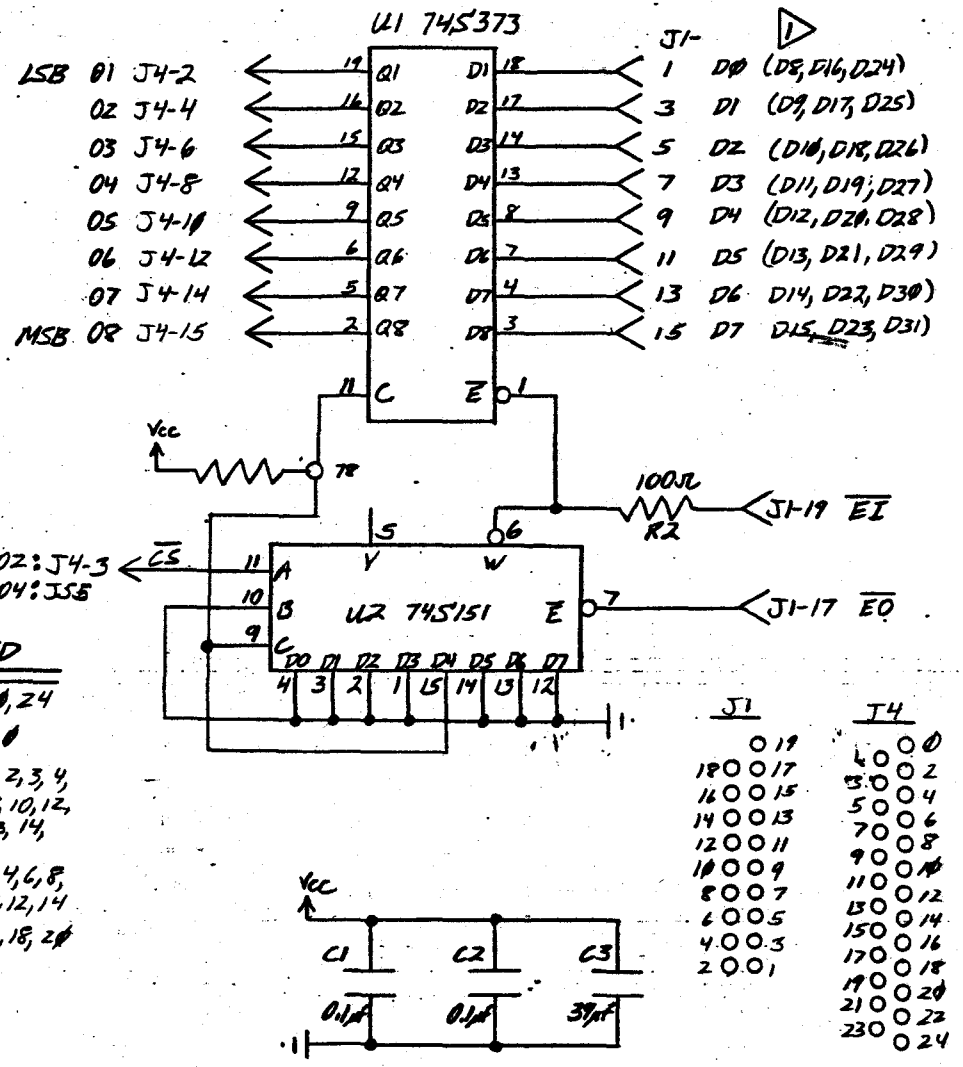
SCHEMATIC, BUFFER BOARD
32x8 MASTER

DRAWN SMP DATE 1/5/78 APPROVED DATE

DWG NO 0001049 SHT 1/2

5-24

SLAVE (VERSION 002)



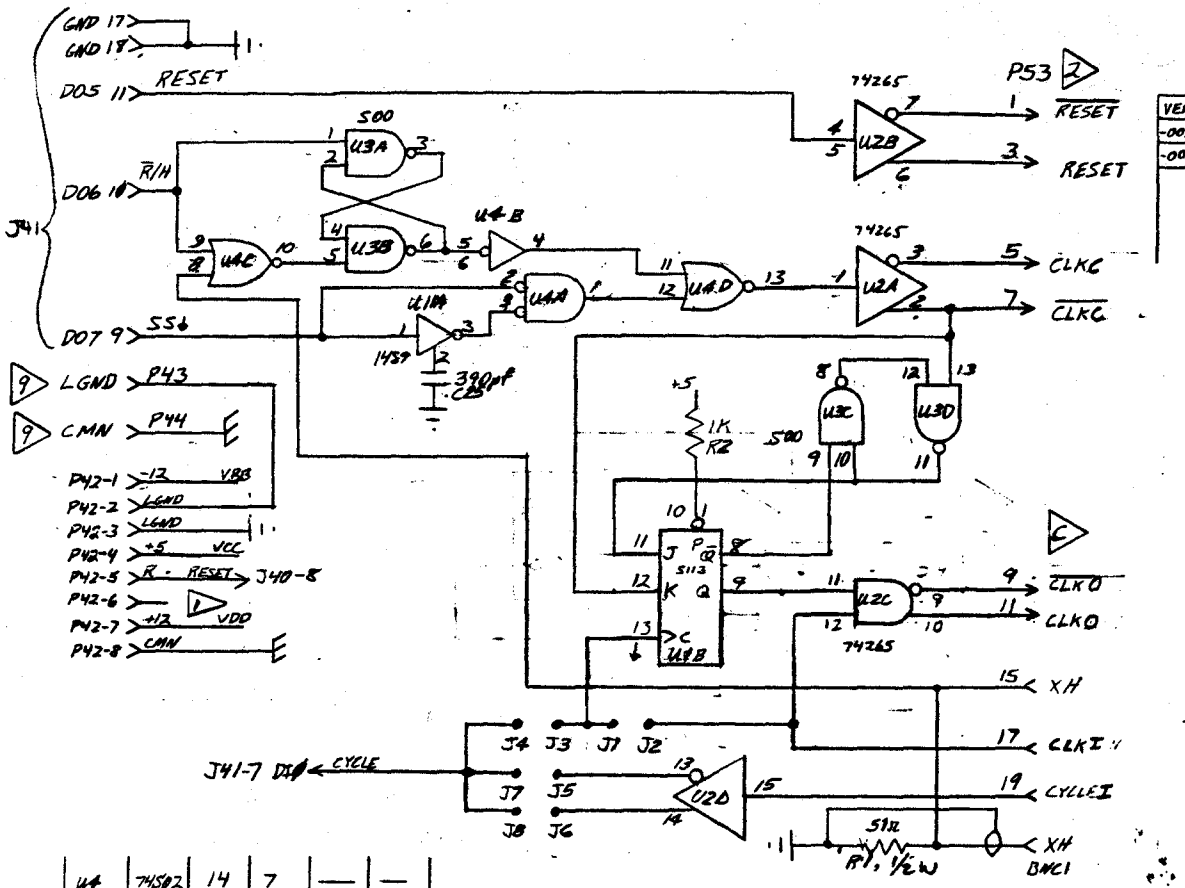
VCC	GND
J4-1	J4-8, 24
U1-20	U1-10
U2-16	U2-1, 2, 3, 4, 8, 10, 12, 13, 14,
R1	J1-2, 4, 6, 8, 10, 12, 14 16, 18, 20

REVISIONS				
LTR	REV NO	REASON	DATE	BY

NOTES: 1 UNLESS OTHERWISE SPECIFIED

1 J1 PIN 20 REMOVED FOR KEYING

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 32×8 SLAVE			
DRAWN	DATE 1/4/77	APPROVED	DATE
DWG NO 0001049		SHT 2/2	



VER	Description
-001	With P43 & P44
-002	Without P43 & P44

REVISIONS

LTR	REV NO	REASON	DATE	BY
TA		MINOR CHNGS	12/27	
TB		CIRCUIT CHNGS	1/27/78	
TC		REMOVED R6		
D		REMOVE C5,C6,C11, GND J41-5,6,8	5/21/78	
D_1		UPDATED ASSY/PL	7/11/78	KEM
E		CHNG WIRING NOTES	10/26/78	
F		Create Version chart	4/8/80	STW

U4	74S02	14	7	—	—
U12	4N28	—	—	—	—
U5	1489A	14	7	—	—
U9	1488	—	7	1	14
U6	1489A	14	7	—	—
U8	74LS195	16	2,8,14	—	—
U7	74LS153	16	1,8	—	—
U10	1488	—	7	1	14
U1	74S113	14	7	—	—
U2	74265	16	8	—	—
U3	74S00	14	7	—	—
U11	1489A	14	7	—	—
REF	TYPE	VCC	GND	VBB	VDD

LAST REF DES USED: C32 CR3 R13 Q2 U12

NOT USED: R6

NOTES: UNLESS OTHERWISE SPECIFIED

1. PIN 6, P42, REMOVED FOR KEYING
2. PIN 13 P53 REMOVED FOR KEYING EVEN NUMBERED PINS ON P53 ARE GROUND
3. OPTION WIRING SHOWN IN "WIRING NOTES"
4. ALL RESISTORS 1/4 W. VALUES IN OHMS
5. ALL CAPACITORS IN MICROFARADS
6. PIN 3 P50 REMOVED FOR KEYING
7. CAPACITORS C1-C4, C7, 12, 16, 20 ON VCC PIN OF U1-U8 AND U11 RESPECTIVELY
8. CAPACITORS C17, C19 AND C18, C2A ON VBB AND VDD PIN RESPECTIVELY OF U9 AND U10
9. P43 & P44 NOT INSTALLED ON VER. -002

WIRING NOTES 3

A. WIRE J7 TO J5 IF CYCLEI IS NEGATIVE TRUE
WIRE J8 TO J6 IF CYCLEI IS POSITIVE TRUE

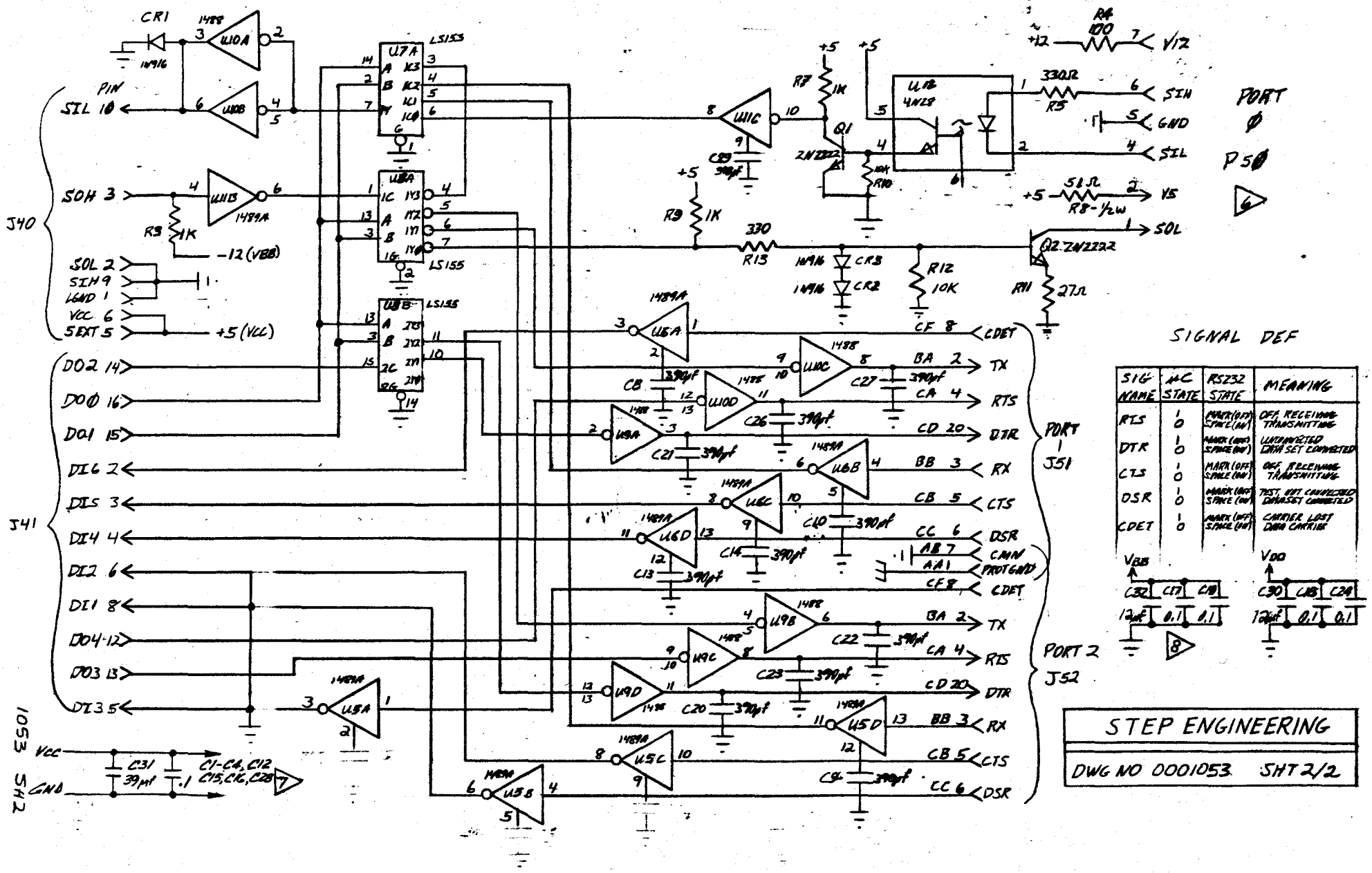
B. FOR SINGLE STEPPING THROUGH A CYCLE OR IF CYCLEI IS NOT USED WIRE J2 TO J4

FOR SINGLE CYCLING (RUNNING THROUGH ONE CYCLE) JUMPER J4 TO J3

C. CLKO HAS A "LOW" QUIESCENT STATE

STEP ENGINEERING			
SCHEMATIC, I/O & CLOCK			
DRAWN	DATE	APPROVED	DATE
	11/28/77		
DWG NO 0001053 D_1 SHT 1/2			

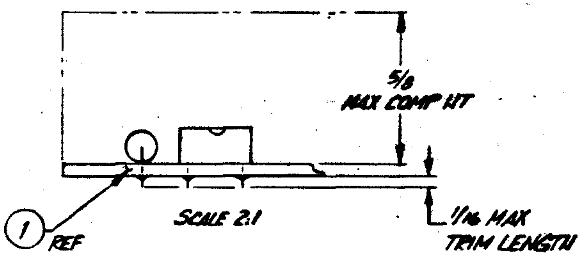
1053 SH1


J40
J41
J51
J52
PORT 1
PORT 2
PORT Ø
P5Ø
SIL 10
SOH 3
SOL 2
SIH 9
GND 1
VCC 6
SEXT 5
-12 (VBB)
+5 (VCC)
DO2 14
DOØ 16
DO1 15
DI6 2
DI5 3
DI4 4
DI2 6
DI1 8
DO4 12
DO3 13
DI3 5
SIN
GND
SIL
VS
SOL
CDET
TX
RTS
DTR
RX
CTS
DSR
CAIN
PROTGND
BA 2
CA 4
CD 20
BB 3
CB 5
CC 6
CF 8
+12
V12
+5
-12
SIGNAL DEF
SIG NAME
μC STATE
RS232 STATE
MEANING
RTS
DTR
CTS
DSR
CDET
VBB
VDD
STEP ENGINEERING
DWG NO 0001053 SHT 2/2
1053 SH2
Vcc
GND
C31 39μf
C1-C4, C12 C15, C16, C28 .1

VER.	Description
-001	Items 28+29 installed
-002	Items 28+29 not installed

REV	DESCRIPTION	BY	APP	DATE
F	Create Version chart	TW		4/2/80

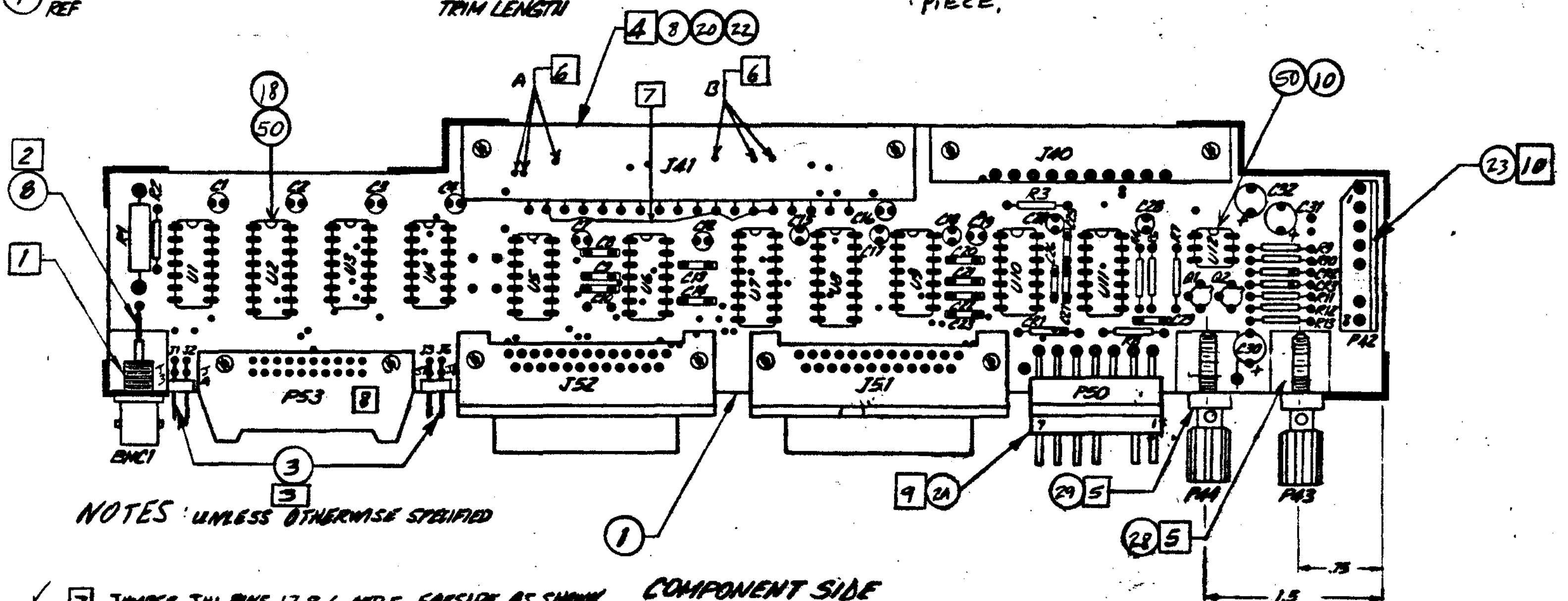
REV	DESCRIPTION	BY	APP	DATE
A	BASE LINE	[illegible]		
B	REMOVED R6	[illegible]		
C	ADD NOTES 8 THRU 8, [illegible]	[illegible]		[illegible]
D	ADD ITEM 3, SOCKET U12	[illegible]		[illegible]
D1	UPDATED ASSY/PL TO SPEC	KEM		[illegible]
E	ADD NOTE 8	[illegible]		11/17/7[illegible]



8 CUT PIN 13 OF P53 FOR KEYING

✓ 9 PIN 3 OF CONNECTOR P50 IS CUT OFF PRIOR TO ASSEMBLY INTO PCB.

✓ 10 PIN 6 OF CONNECTOR P42 IS CUT OFF PRIOR TO ASSEMBLY INTO PCB. ALSO A 45° 1/8" CHAMFER IS CUT OFF OF THE PIN 1 CORNER OF THIS PIECE.



NOTES: UNLESS OTHERWISE SPECIFIED

COMPONENT SIDE
SCALE 1:1

✓ 7 JUMPER J41 PINS 17, 8, 6, AND 5, FARSIDE AS SHOWN

✓ 6 CUT TRACES (3) BETWEEN POINT A+B, FARSIDE

✓ 1 SOLDER BNC1 TO MOUNTING PAD, FAR LEFT

✓ 2 SOLDER WIRE (ITEM 8) FROM BNC1 TO PLATED THRU HOLE AS SHOWN

✓ 3 PART MUST BE CUT INTO SHORT LENGTHS PRIOR TO ASSEMBLY.

✓ 4 SOLDER WIRE (ITEM 8) TO TERMINAL (ITEM 20) AND INSERT IN CONNECTOR J41 (ITEM 22) INSERT AND SOLDER WIRE TO PLATED THRU HOLES

✓ 5 SOLDER THREADED BOLT OF ITEMS 28 AND 29 TO MOUNTING PADS (ITEMS 28 + 29 ARE NOT INSTALLED ON VERSION -002.)

1 PART WILL MAKE PLUGS FOR 5 ASSEMBLIES

STEP ENGINEERING

DRAWN	APPR	DATE	TITLE
[illegible]			ASSEMBLY, I/O CLOCK

PART NO.	REV	SHT
0001054	D1	1 of 2

1054

5 20

STEP ENGINEERING

TITLE: BOM, I/O CLOCK

PART NO: 0001054 REV: D1 SHT: 2 OF 2

REV	DESCRIPTION	BY	APPR	DATE
*A	BASE LINE			
*B	REMOVED R6			
C	REMOVE C5, C6, C11			3/21/77
D	ADD ITEM 3, SOCKET U12			5/17/77
D1	UPDATED ASSY/PL TO SPECS	KEM		2/7/77

ITEM	QTY	STEP ENG P/N	DESCRIPTION	VENDOR P/N	REF DES
1	1	0001055	PCB, I/O CLOCK		
2	REF	0001053	SCHEMATIC, I/O CLOCK		
3	1/5	<3>	STRIP LINE PLUG, 4 POS	D46-RSP100-310-090	J1-J8
4	2		HEX SPACER BRASS 6/32 ½"		
5					
6					
7					
8					
9					
10	1		IC 4N28		U12
11	2		1488		U9, U10
12	3		1489A		U5, U6, U11
13	1		74S00		U3
14	1		74S02		U4
16	1		74S113		U1
16	1		74LS153		U7
17	1		74LS155		U8
18	1		IC 74265		U2
19					
20	18	<A>	TERMINAL MOLEX	08-50-0106	
21	1		CONNECTOR, (10)	09-03-2105	J40
22	1	<A>	(18)	09-01-7181	J41
23	1	<10>	(8)	09-65-1081	P42
24	1	<9>	(7) MOLEX	09-75-1071	P50
25	2		CONNECTOR CANNON	DBP-25S4A	J51, J52

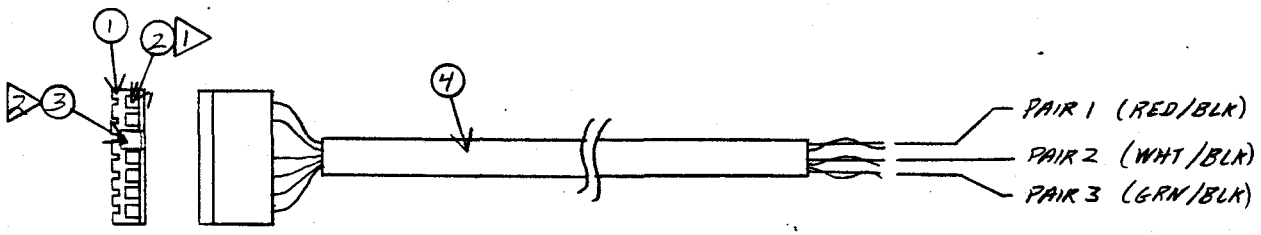
STEP ENGINEERING

TITLE: BOM, I/O CLOCK

PART NO: 0001054 REV: D1 SHT: 2 OF 2

REV	DESCRIPTION	BY	APPR	DATE
.	SEE SHT 1			

ITEM	QTY	STEP ENG P/N	DESCRIPTION	VENDOR P/N	REF DES
26	1		CONNECTOR, 20 PIN 3M#	3428-1002	P53
27	1		BNC RECEPTACLE	UG-1094/U	BNC1
28	1	NOT USED ON VER. -002	BINDING POST, POMONA	3760-0 BLK	P43
29	1	NOT USED ON VER. -002	BINDING POST, POMONA	3760-9 WHT	P44
30					
31	13		CAPACITOR .1	CY20C104P	C1-C4, C15-C19, C22, C24, C28, C7
32	2		12 µf	196D126X9020JA1	C30, C32
33	1		39 µf	196D396X9010KA1	C31
34	13		CAPACITOR 330 pf	CK05BX391K	C9, C10, C13, C14, C20-C23, C26, C25-C27, C29
35					
36	3		DIODE IN916		CR1, CR2, CR3
37					
38	1		RESISTOR 27Ω ¼W, 5%,	RC07GF270J	R11
39					
40	1		100Ω	101J	R4
41	2		330Ω	331J	R5, R13
42	4		1K	102J	R2, R3, R7, R9
43	2		RESISTOR 10K ¼W, 5%,	RC07GF103J	R10, R12
44					
45					
46	2		RESISTOR 51Ω, ½W, 5%,	RC20GF510J	R1, R8
47					
48	2		TRANSISTOR 2N2222		Q1, Q2
49					
50	2		SOCKET, AUGAT 316 AG 39D	"or EQUIV	U2, U12



REVISIONS				
LTR	NO	REASON	DATE	BY
JA		PRELIM RLSE	1/30/78	[illegible]
JB		ADD NOTES, CONN METHOD	2/1/78	[illegible]

PARTS LIST			
ITEM	QTY	DESCRIPTION	PART NUMBER
1	1	CRIMP TYPE CONNECTOR	MOLEX 09-50-3071
2	6	TERMINALS	MOLEX 08-50-0106
3	1	KEY, POLARIZING	MOLEX 2560-1
4	15'	TWISTED PAIR CABLE (3 PAIR)	ALPHA 1318

WIRE ASSIGNMENT			
PIN	COLOR	PAIR	USE
1	BLK	1	SERIAL OUTPUT LOW (20MA SINK)
2	RED	1	+5 VOLTS (51Ω)
3	—	—	KEY
4	BLK	2	SERIAL INPUT LOW
5	BLK	3	GND
6	WHT	2	SERIAL INPUT
7	GRN	3	+12 VOLTS (100Ω)

NOTES: UNLESS OTHERWISE SPECIFIED

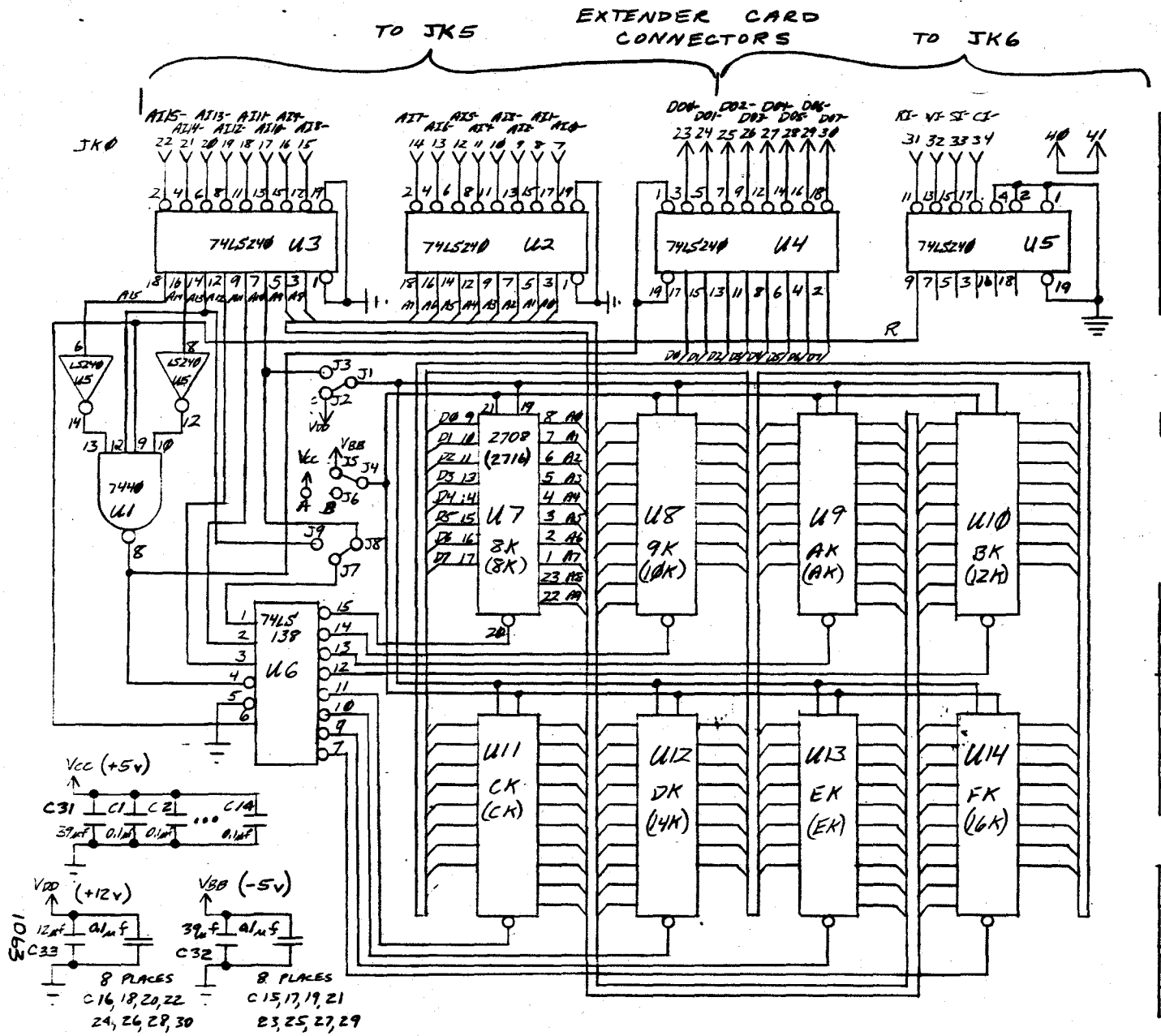
1. INSERT TERMINALS, ITEM 2, IN CONNECTOR BODY ITEM 1 AFTER SOLDERING TO TWISTED PAIR CABLE
2. POSITION 3 KEYED USING POLARIZING KEY, ITEM 3
3. PART NUMBER TO BE DWG NO PLUS DWG REV LTR

CONNECTION METHOD

FOR SYSTEMS EMPLOYING ACTIVE CURRENT SOURCE DRIVERS (20MA FOR DATA TRANSMISSION), CONNECT SERIAL INPUT LOW (PIN 4) TO CURRENT RTN OR SINK AND SERIAL INPUT HIGH (PIN 6) TO CURRENT SINK. CONNECT SYSTEM SERIAL INPUT LOW (RECIEVE RTN) TO CABLE SERIAL OUTPUT (PIN 1) AND SYSTEM SERIAL INPUT HIGH (RECIEVE SOURCE) TO CABLE +5 VOLTS (PIN 2). IF ADDL DRIVE IS REQUIRED USE CABLE PIN 7 (+12 VOLTS). FOR SYSTEMS EMPLOYING PASSIVE DATA TRANSMISSION CIRCUITRY (SWITCHES) CONNECT SERIAL INPUT LOW (PIN 4) TO GND (PIN 5) AND USE SERIAL INPUT. (PIN 6) AND UNUSED VOLTAGE OUTPUT (+12 VOLTS, PIN 7 OR +5 VOLTS, PIN 2) TO CONNECT TO SYSTEM TRANSMIT CIRCUITRY.

STEP ENGINEERING			
TTY CABLE			
DRAWN [illegible]	DATE 1/30/78	APPROVED	DATE
DWG 0001062		SHT 1/1	

1062



REVISIONS				
LTR	NBR	DESCRIPTION	BY	DATE
A		BASELINE RLSE	[illegible]	2/6/78
B		CORRECTIONS RECORD CHANGE	KEM	2/9/78
C		ADDED JK5+JK6	KEM	4/4/78

NOTES: UNLESS OTHERWISE SPECIFIED

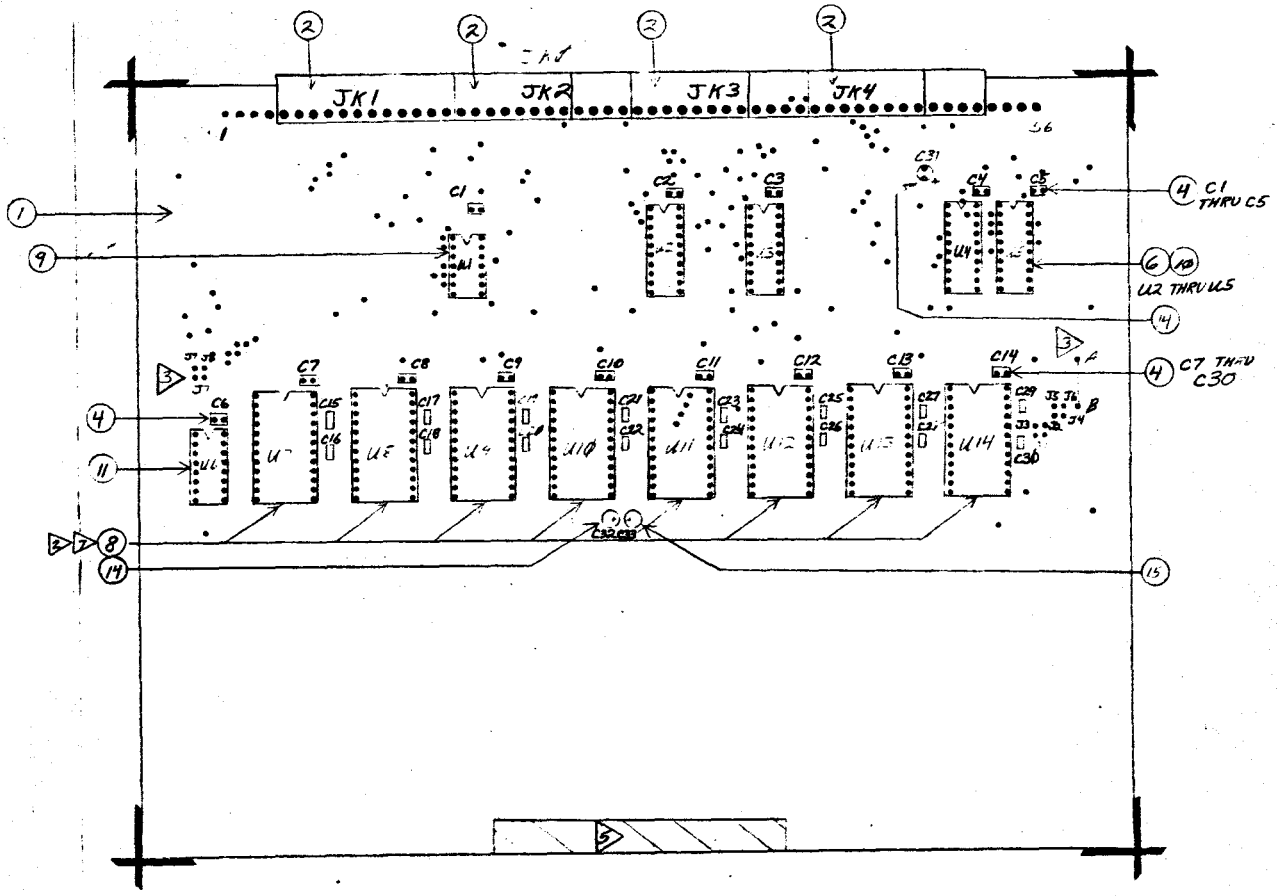
1. FOR 2716 VERSION CONNECT A TO B, BREAK TRACES J4/J5, J1/J2, J7/J8, AND CONNECT JUMPERS J1/J3, J4/J6, J7/J9

JK0	CONN	5,6	47	51,52	48	-01,02
U7 U9	2708	12,18	21	24	19	-01
U7 U9	2716	12,18	—	24	—	-02
U6	74LS138	5, 8	—	16	—	-01,02
U5	74LS240	1,2,4,10,19	—	20	—	-01,02
U4	74LS240	10	—	20	—	-01,02
U2,U3	74LS240	1, 10, 19	—	20	—	-01,02
U1	7440	5, 7	—	14	—	-01,02
REF	DEVICE	GND	VBB	VCC	VDD	VERS

POWER & GND ASSIGNMENTS

STEP ENGINEERING			
SCHEM : SYSTEM MEM BD			
DRAWN [illegible]	DATE 1/2/78	APPROVED	DATE
DWG 0001063		SHT 1/1	

1063



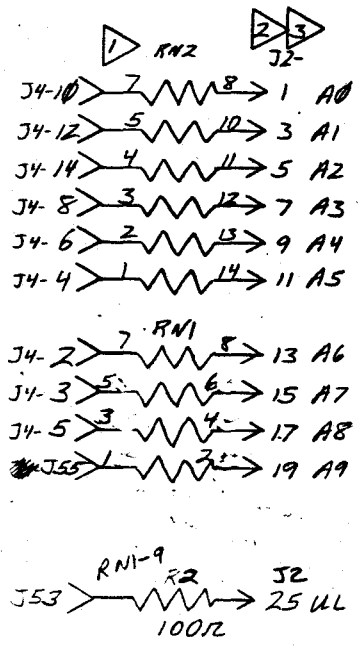
BILL OF MATERIALS

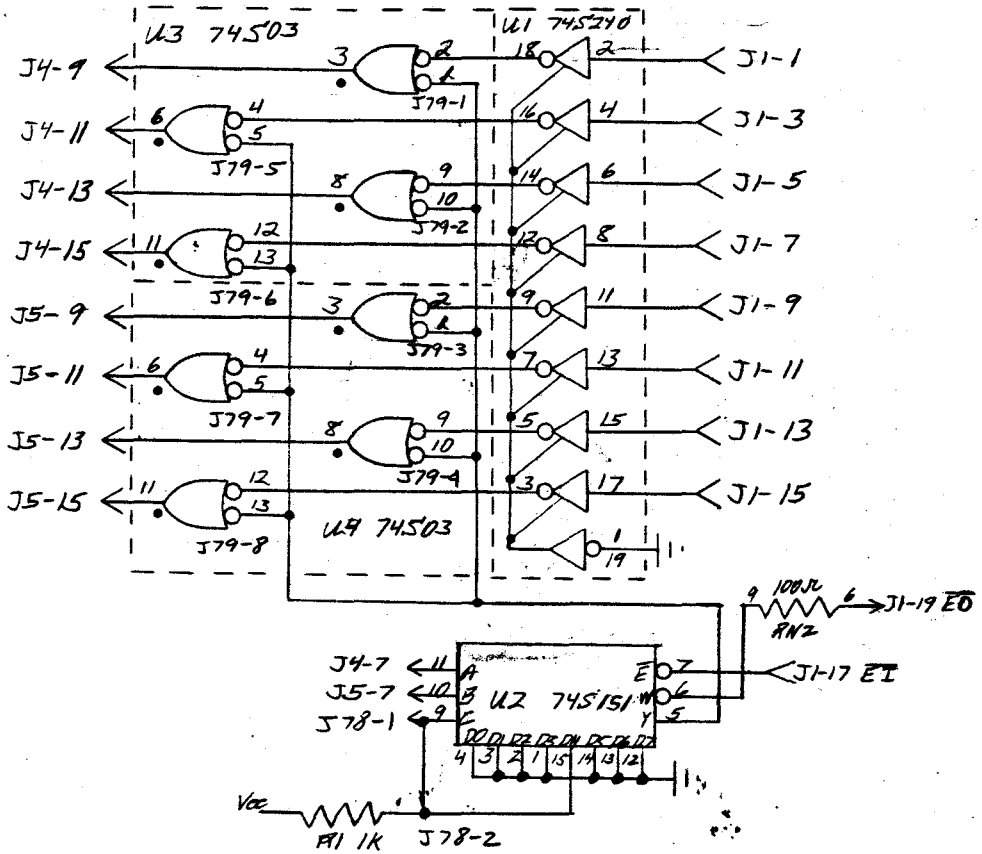
ITEM #	REF DES	DESCRIPTION	QTY	PART NUMBER	NOTES
1	———	PC BOARD, SYSTEM MEMORY	1	0001060	
2	JK1 THRU JK4	RIGHT ANGLE PC BD CONN 12 POS	4	MOLEX 09-52-3121	
3		CARD EJECTOR	2	5200	
4	C1 THRU C30	CAPACITOR CERAMIC, 0.1 uf	30	CENTRALAB CY20C104P	
8	U1 THRU U14	IC SOCKET 24 PIN	8	CA 24CS2-TSDORBRUV	
9	U1	INTEGRATED CIRCUIT DUAL 4 INPUT NAND	1	7440N	
10	U2 THRU U5	IC OCTAL INVERTING BUFFER	4	SN74LS240N	
11	U6	IC 3 TO 8 LINE DECODER	1	74LS138N	
12					
13					
14	C31, C32	CAPACITOR 10 VOLT 33 uf TANT	2	SPRAGUE 196D336X9010A1	
15	C33	CAPACITOR 20 VOLT 12 uf TANT	1	SPRAGUE 196D126X9020A1	
16	———	SCHEMATIC, SYSTEM MEMORY		REF DWG 0001063	

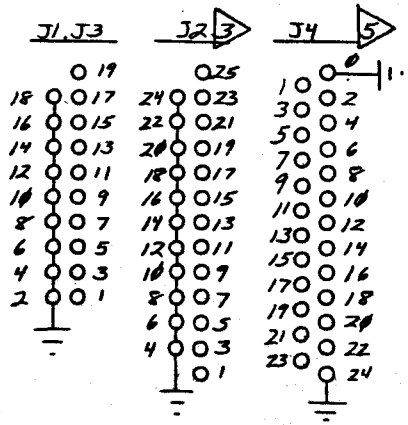
NOTES: UNLESS OTHERWISE SPECIFIED

1. A SECOND VERSION OF THIS ASSEMBLY MAY BE BUILT USING 2716 PROMS INSTEAD OF 2708 PROMS.
2. THE PROM'S ARE NOT A PART OF THIS ASSEMBLY, BUT ARE LISTED AS PART OF THE TOP ASSEMBLY. THIS ALLOWS THE PROGRAM TO BE CHANGED INDEPENDENT OF PC
3. ON SECOND VERSION (2716) CUT JUMPERS J4/J5, J1/J2; J7/J8 AND INSTALL JUMPERS A/B, J1/J3, J4/J6 J7/J9
4. ON SECOND VERSION (2716) CAPACITORS C15 THRU C30 AND C32/C33 ARE DELETED
5. ASSEMBLY PART NUMBER PLUS ASSY REVISION LEVEL TO BE MARKED IN AREA INDICATED
6.
7. SOFTWARE VERSION TO BE MARKED ON PROMS.
8. ON 1060 REV TA BOARDS ONLY, CAPS C15, 18, 19, 22, 23, 26, 27, 30 IMPLEMENTED BY SOLDERING ON BACK OF BOARD: C15, 19, 27 0.1 uf BETWEEN GND & PIN 21; C18, 22, 30 0.1 uf BETWEEN GND & PIN 19; C23 12 uf BETWEEN GND & PIN 19 WITH + POL ON PIN 19; C26 12 uf BETWEEN GND & PIN 21 WITH + POL ON GND (NOTE: PINS 12, 18 ARE GND)

		STEP ENGINEERING
	SPEC. NUMBER	ASSY, SYSTEM MEMORY BD







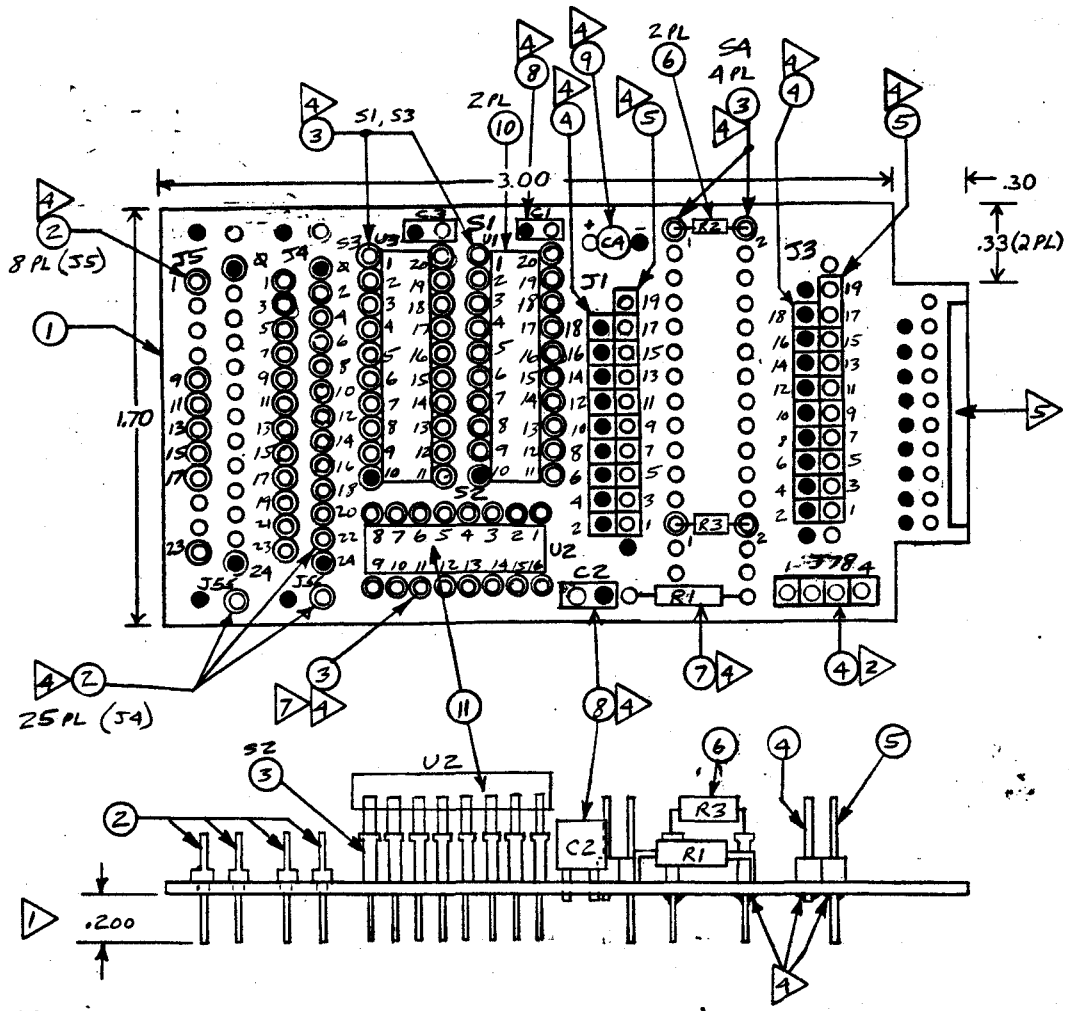
REVISIONS				
LTR	REV NO	REASON	DATE	BY

NOTES: UNLESS OTHERWISE SPEC:

1. RN1, RN2 100Ω RESISTOR PACKS
2. J2 PINS 2, 26 REMOVED FOR KEYING
3. RN2, J2 ONLY PRESENT ON -001 VERSION
4. J1, J3 PIN 20 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG
6. VERSION: -001 MASTER
   -002 SLAVE

VCC	GND
U1-20	J1 2,4,6,8,10,12,14,16,18,20
U2-16	J2 - 2,4,6,8,10,12,14,16,18,20,23,24
U3-20	J4 0, 24
R1	U1, U3 - 10
J4-1	U2

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD DUAL 512x4 OPEN COLLECTOR			
DRAWN	DATE	APPROVED	BY
DWG NO 0001074 SHT 1/1			



NOTES: MODIFY PCB TRACES - ALL VERSIONS

7. CUT SHORTING TRACES BETWEEN U2-1, 2, 3, 4.
   CUT SHORTING TRACES BETWEEN U2-12, 13.
   CUT TRACES FROM U2-6 TO U1-1 AND U3-1.

REVISIONS

LTR	REV NO	REASON	BY	DATE
A		RELEASE TO PROD	KEM	26/8/78
B		CHNG ITEM 2	SAM	7/12/78
C	34	ADD J35, J36 OBSHTS	SAM	16/1/80

NOTES: UNLESS OTHERWISE SPECIFIED

1. CUT LEADS WHERE NECESSARY TO .200 INCH AFTER ASSY IS WIREWRAPPED.
2. INSTALL POST WITH LONG PIN DOWN TRIM TOP POST FLUSH WITH INSULATOR
3. PINS CALLED OUT AS "GND" ON WIRE LIST SHOULD BE SOLDERED TO GROUND PLANE, FAR SIDE.
4. ITEM 2, 3, 4, 5, 7, 8, 9 TO BE SOLDERED TO BOARD FAR SIDE.
5. MARK ASSY NUMBER IN SPACE INDICATED.
6. ASSY NUMBER SHALL BE DWG NO - VERSION - REV

STEP ENGINEERING			
ASSEMBLY, BUFFER BOARD ZK WORD, SLAVE			
DRAWN	DATE	APPROVED	DATE
KEM	26/8/78		
DWG NO 0001075		SHT 1/2	

VERSION CHART

VERSION	DESCRIPTION	SCHEM NO.
-001	BUFFER 2K×8 (24 PIN)	0001022-002
-002	BUFFER DUAL 2K×4 (18 PIN)	0001021-002
-003	BUFFER 2K×8 (24 PIN GE VERSION)	0001022-004
-004	BUFFER 2K×8 (24 PIN AJ VERSION)	0001022-006
-005	BUFFER 8K×8 (24 PIN)	
-006		
-007		
-008		
-009		
-010		
-011		
-012		

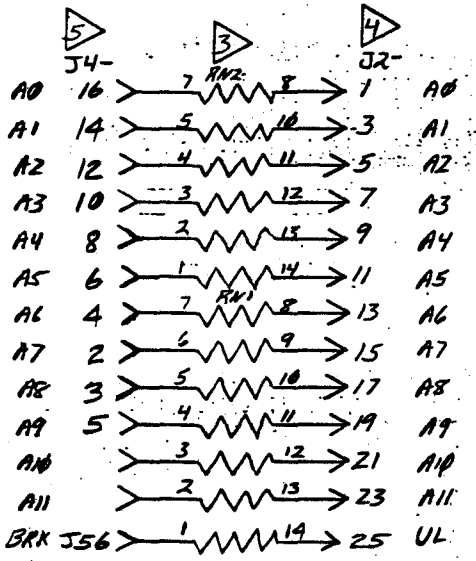
PARTS LIST

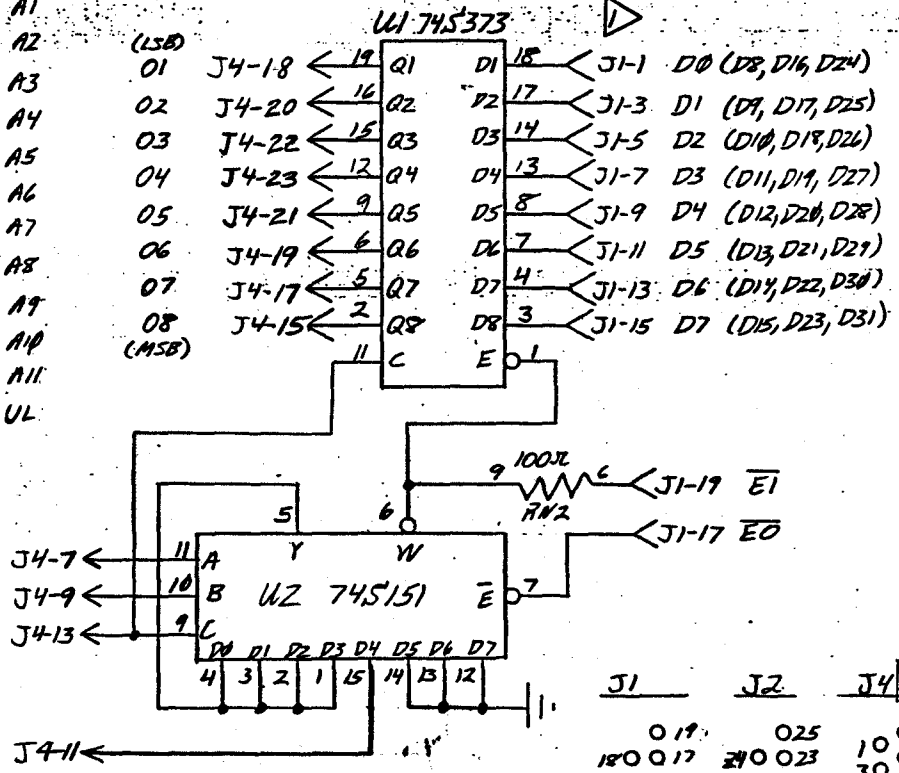
PART NO	REF DESIG	DESCRIPTION	QUANTITY	PART NUMBER
1	—	PC BOARD, BUFFER GEN PURPOSE	1	0001018-001
2	J4,J5,J6,J7,J8	STRIP LINE PLUG, WW, .50 LONG	1	CA-536P100-170-500
3	S1,S2,S3,S4	LEAD SOCKET, WIRE WRAP PINS	60	AUGAT LSG-1FG10-1
4	J1, J3, J78	STRIP LINE PLUG, WW, .43 LONG	1	CA-536P100-230-430
5	J1, J3	STRIP LINE PLUG, WW, .60 LONG	1	CA-536P100-230-600
6	R2, R3	RESISTOR, 100Ω 10% ¼W	2	RC07GF101K
7	R1	RESISTOR, 1000Ω, 10%, ¼W	1	RC07GF102K
8	C1, C2, C3	CAPACITOR, CERAMIC, 0.1μf	3	CENTRALAB CY20C104P
9	C4	CAPACITOR, TANTALUM, 3.9μf, 10V	1	SPRAGUE 196D396X9010KA1
10	U1, U3	OCTAL "D" TYPE TRANSPARENT LATCH	2	745373
11	U2	THREE TO EIGHT LINE DECODER	1	745138
12	—	SOLDER, ROSIN CORE	A/R	
13	—	WIRE, KYNER COATED, 30 AWG, STRIPPED, 3"L	A/R	AUGAT 1410-KG11
14	—	WIRE, KYNER COATED, 30 AWG, STRIPPED, 4"L	A/R	AUGAT 1410-KG12
15	—	SCHEMATIC	REF	SEE VERSION CHART

STEP ENGINEERING

DWG NO 0001075 SHT 2

MASTER (VERSIONS -001, -002)



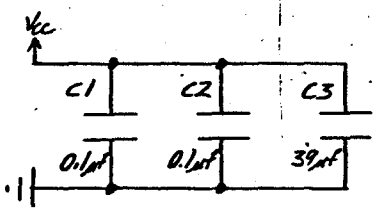


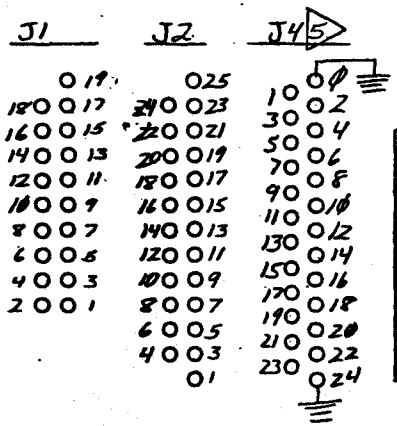
REVISIONS				
LTR	REV NO	REASON	DATE	BY
TB		REVISED & REDRAWN	11/1/78	GWW
C		REVISE & RELEASE	5/5/79	GWW

NOTES: UNLESS OTHERWISE SPECIFIED

1. J1 PIN 20 REMOVED FOR KEYING
2. SEE VERSION CHART, SHEET 2, FOR PINOUT
3. RN1, RN2 100 OHM RESISTOR PACKS
4. J2 PINS 2, 26 REMOVED FOR KEYING
5. J4 CONNECTS TO ROM SIM PLUG

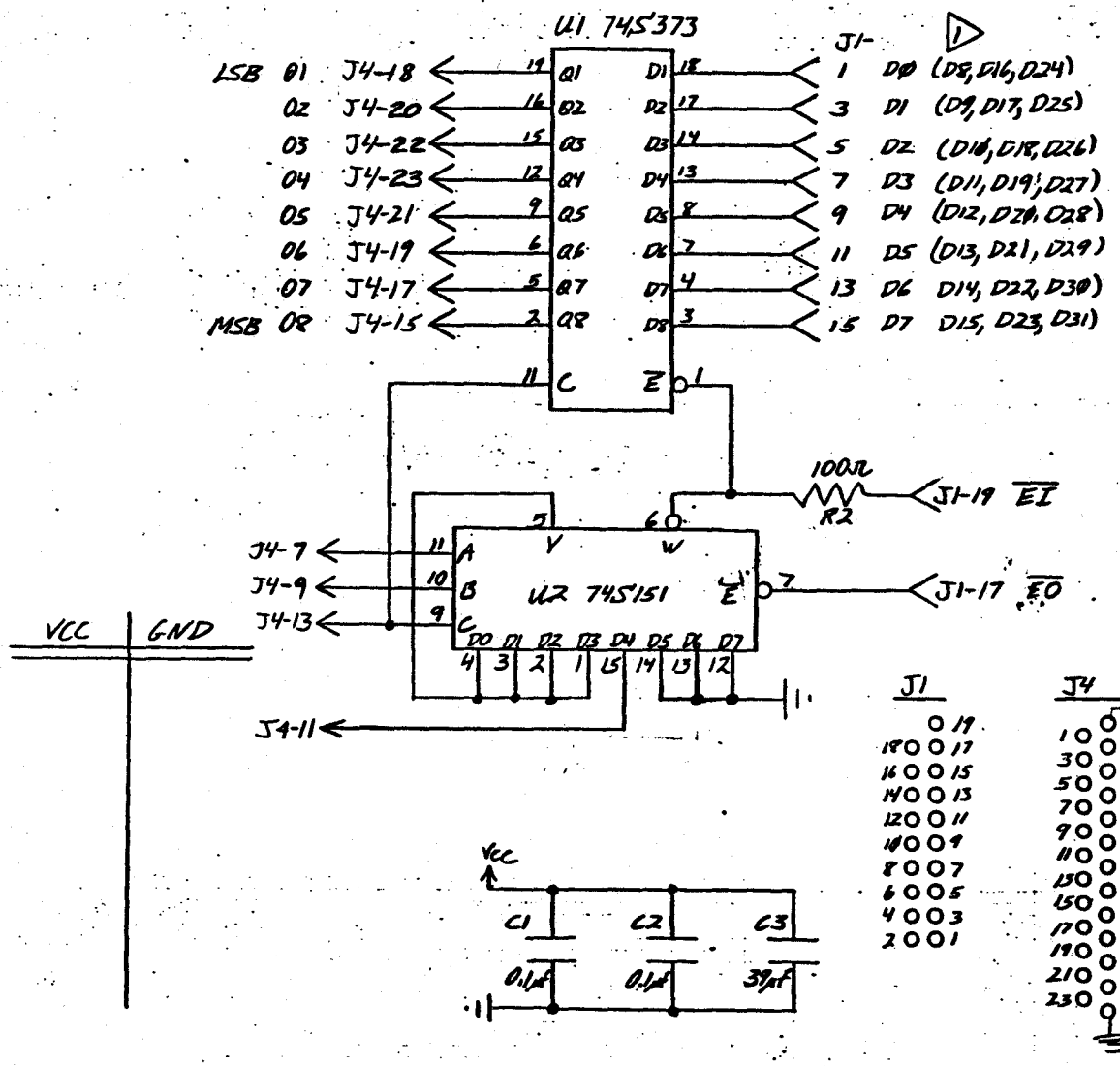
Vcc	GND
J4-1	J1-2, 4, 6, 8, 10, 12, 14, 16, 18, 20
U1-20	
U2-16	J2-2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26
R1	J4-0, 24
	U1-10
	U2-8, 12, 13, 14





STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 1K × 8 LATCHING			
DRAWN	DATE	APPROVED	DATE
	1/7/78		
DWG NO 0001078		SHT 1/2	

SLAVE (VERSION 3)



REVISIONS (SEE SHEET 1)				
LTR	REVNO	REASON	DATE	BY

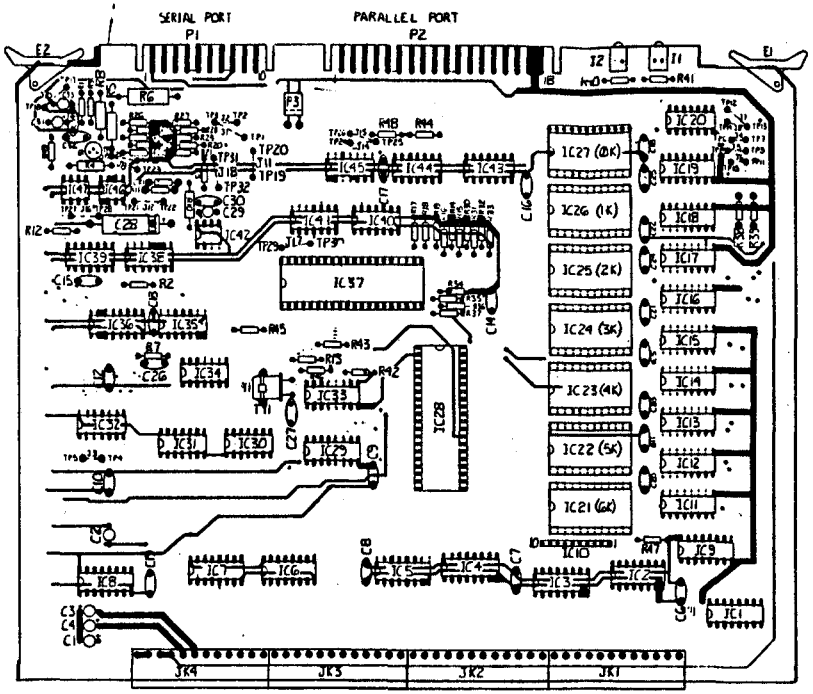
NOTES: SEE SHEET 1

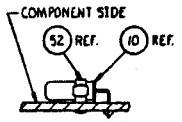
~~NOTES: UNLESS OTHERWISE SPECIFIED~~

1 ~~J1 PIN 20 REMOVED FOR KEYING~~

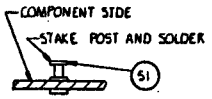
VER	DESCRIP	RN2-1	RN1-7	RN1-6	RN1-5		
-001	256x8 MASTER	J4-8	J4-10	J4-12	J4-13		
-002	512x8 MASTER	J4-6	J4-8	J4-10	J4-12		
-003	8 BIT SLAVE	—	—	—	—		

STEP ENGINEERING			
SCHEMATIC, BUFFER BOARD 1K x 8 LATCHING			
DRAWN SWP	DATE	APPROVED	DATE
DWG NO 0001078		SHT 2/2	

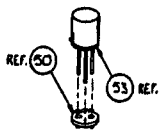




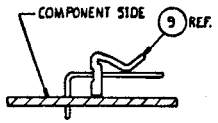
SECTION A-A
2 x SIZE



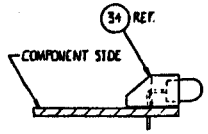
SECTION B-B
2 x SIZE



VIEW C
2 x SIZE



SECTION D-D
2 x SIZE



SECTION E-E
2 x SIZE

NOTES: ⚠ SPECIAL HANDLING REQUIRED

REV	ECO NO.	DESCRIPTION	DR.	DATE	CK.	DATE
A	———	ENG. REL	DS	8-2-77	DD	8-3-77
B	5983	REV'D P/L & ASM DWG	DS	8-9-77	RK	8-25-77
C	———	REL FOR PROD	DS	9-2-77	RK	9-2-77

ITEM	QTY	PART NO.	DESCRIPTION	REFERENCE	NOTES
33	1	82896	IC-GN139	IC47	
32	1	81675	IC-75452	IC46	
31	1	06008	IC-7438	IC45	
30	1	06006	IC-7430	IC44	
29	1	82929	IC-GN135	IC42	
28	2	06007	IC-7437	IC40, IC41	
27	1	06001	IC-7400	IC39	
26	2	06004	IC-7410	IC38, IC43	
25	1	81682	IC-5501	IC37	
24	1	81287	IC-9L5109	IC36	
23	1	81288	IC-8224	IC33	
22	1	06003	IC-7408	IC31	
21	2	06015	IC-BT380	IC30, IC35	
20	1	06321	IC-74175	IC29	
19	1	80788	IC-8080	IC28	
18	1	06002	IC-7404	IC32	
17	1	06324	IC-74155	IC19	
16	8	81289	IC-2102	IC11-IC18	
15	1	82581	RESISTOR NETWORK-10K SIP	IC10	
14	5	80312	IC-8838	IC2-IC5, IC8	
13	4	06000	IC-BT26	IC1, IC6, IC7, IC9	
12	2	81710	EJECTOR-CARD	E1, E2	
11	1	01213	DIODE IN914	CR1	
10	1	82579	CRYSTAL-18.00 MHZ, 32 pF	Y1	SEC A-A
9	1	81969	CONN-2 PIN RIGHT ANGLE WAFER	P3	SEC D-D
8	4	81267	CONN-12 PIN, RIGHT ANGLE	JK1-JK4	
7	1	81183	CAP.-100 μF, 12V	C28	⚠
6	1	01176	CAP.-750 μF, 15V	C26	
5	20	06296	CAP.-.047 μF, 12V	C6-C25	
4	2	06120	CAP.-.05 μF, 25V	C5, C34	
3	2	80800	CAP.-4.7 μF, 35V	C4, C33	
2	5	80632	CAP.-10 μF, 25V	C1-C3, C29, C31	
1	1	81626	BOARD, P.C.-1806		

TABULATED PARTS LIST

PERF SPEC. 82115E	
SCH 81864E	
ASSOCIATED DWGS	

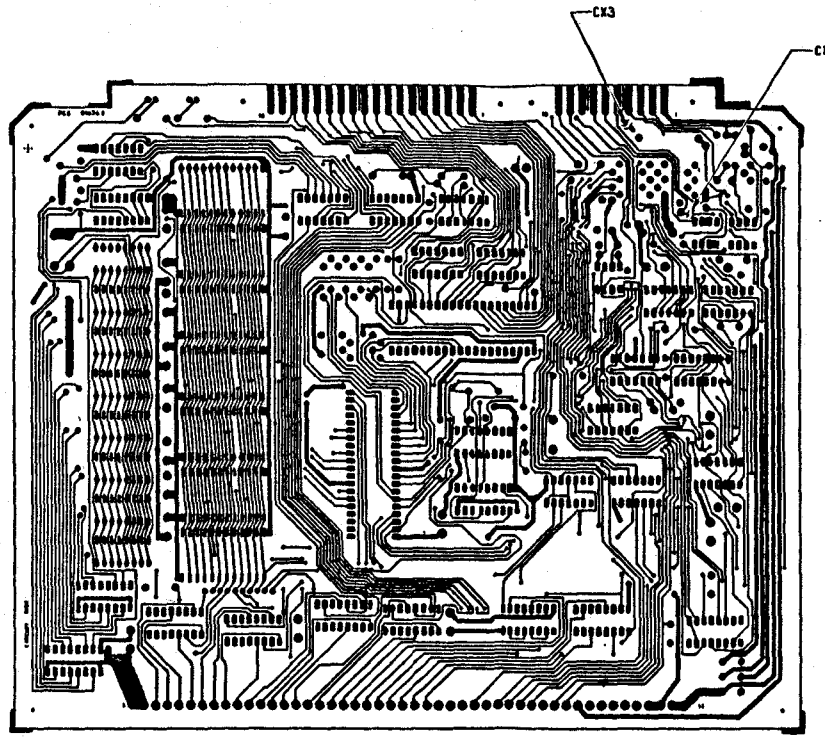
DATE 8-2-77
SCALE FULL
DRAWN BY SWARTWOOD
CHECKED BY
APPROVED BY
RELEASED 8-3-77

DGS PROCESS COMPUTER SYSTEMS
FLINT, MICHIGAN 48507 USA

TITLE: ASM-1806 8-BIT MICROCOMPUTER SYSTEM

SHEET 1 OF 3
DRAWING NUMBER 81862-003E

REV	ECO NO	DESCRIPTION	DR	DATE	CK	DATE
A	———	ENG. REL	DS	8-2-77	[illegible]	8-2-77
B	5983	REVD P/L & ASM DWG	DS	8-15-77	PR	8-25-77
C	———	REL FOR PROD	DS	9-2-77	PR	9-2-77



QTY	PART NO	DESCRIPTION	REFERENCE	NOTES	ITEM
1	80567	RES.-12K, ¼W, 5%	R2		56
2	81066	CAP.-10μf, 1KV	C30, C32		55
2	82495	IC-74LS04	IC20, IC31		54
1	06327	TRANS.-2N2907A	Q1	VIEW C	53
1	91495	TIE CABLE (100 x 4.00)	TY1		52
32	06262	TERMINAL-PC SOLDER	TP1-TP32	SEC B-B	51
1	80727	STANDOFF-TO 18 INSULATOR	Q1		50
2	80348	SOCKET-40 PIN	IC28, IC37		49
7	80347	SOCKET-24 PIN	IC21-IC27		48
8	80339	SOCKET 16 PIN	IC11-IC18		47
2	06043	RES. 330, ¼W, 5%	R40, R41		46
25	06055	RES-10K, ¼W, 5%	R1-R2, R4-R21, R40, R42, R44-R48		45
		REMOVED PER ECO 5983			44
2	06047	RES-1K, ¼W, 5%	R9, R13		43
1	06210	RES-220, ¼W, 5%	R8		42
1	81681	RES-360 ¼W, 5%	R7		41
		REMOVED PER ECO 5983			40
3	82412	RES-301, ¼W, 1%	R5, R6, R10		39
2	01227	RES-402, ¼W, 1%	R4, R49		38
2	06057	RES-20K, ¼W, 5%	R42, R43		37
1	06078	RES-100K, ¼W, 5%	R1		36
6	———	JUMPER-20 GA. WIRE	J1, 4, 7, 11, 14, 16		35
2	80025	INDICATOR-LED (GREEN) 550 SERIES	I1, I2	SEC. E-E	34

TABULATED PARTS LIST

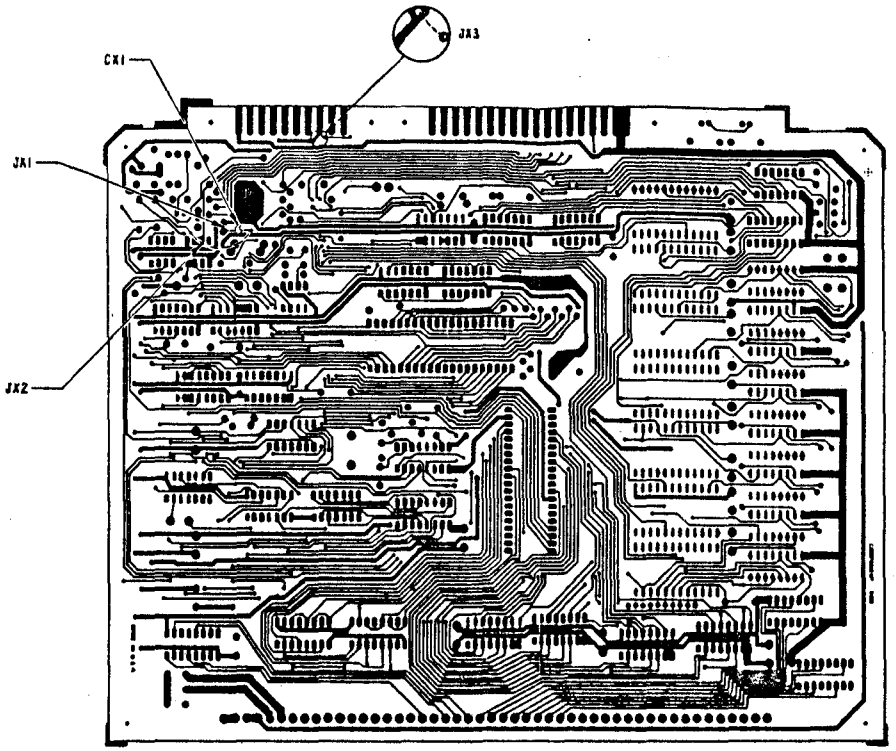
DATE: 8-2-77
SCALE: FULL
DRAWN BY: WARWOOD
CHECKED BY:
ENGINEER: [illegible]
APPROVED BY: [illegible]
DATE: 8-3-77

DGC PROCESS COMPUTER SYSTEMS

TITLE: ASM 1800 8 BIT MICROCOMPUTER SYSTEM

SHEET: 2 or 3
DRAWING NUMBER: 81862-003E

		DESCRIPTION	DR	DATE	CH	DATE
B	5983	ADDED SW 3 (CUTS + JUMPERS)	DK	8 24 77	AR	8 25 77
C	———	REL FOR PROD	DS	9 2 77	AR	9 2 77



CUT (CX)			JUMPER (JX)		
REF.	TO	FROM	REF.	TO	FROM
CX1	TP23	IC 37-2	JX1	TP16	TP13
CX2	TP25	R 49	JX2	R49	IC 37-2
CX3	P1-B	C33(-)	JX3	P1-B	P3-1

ITEM	NOTES	REFERENCE	DESCRIPTION	PART NO

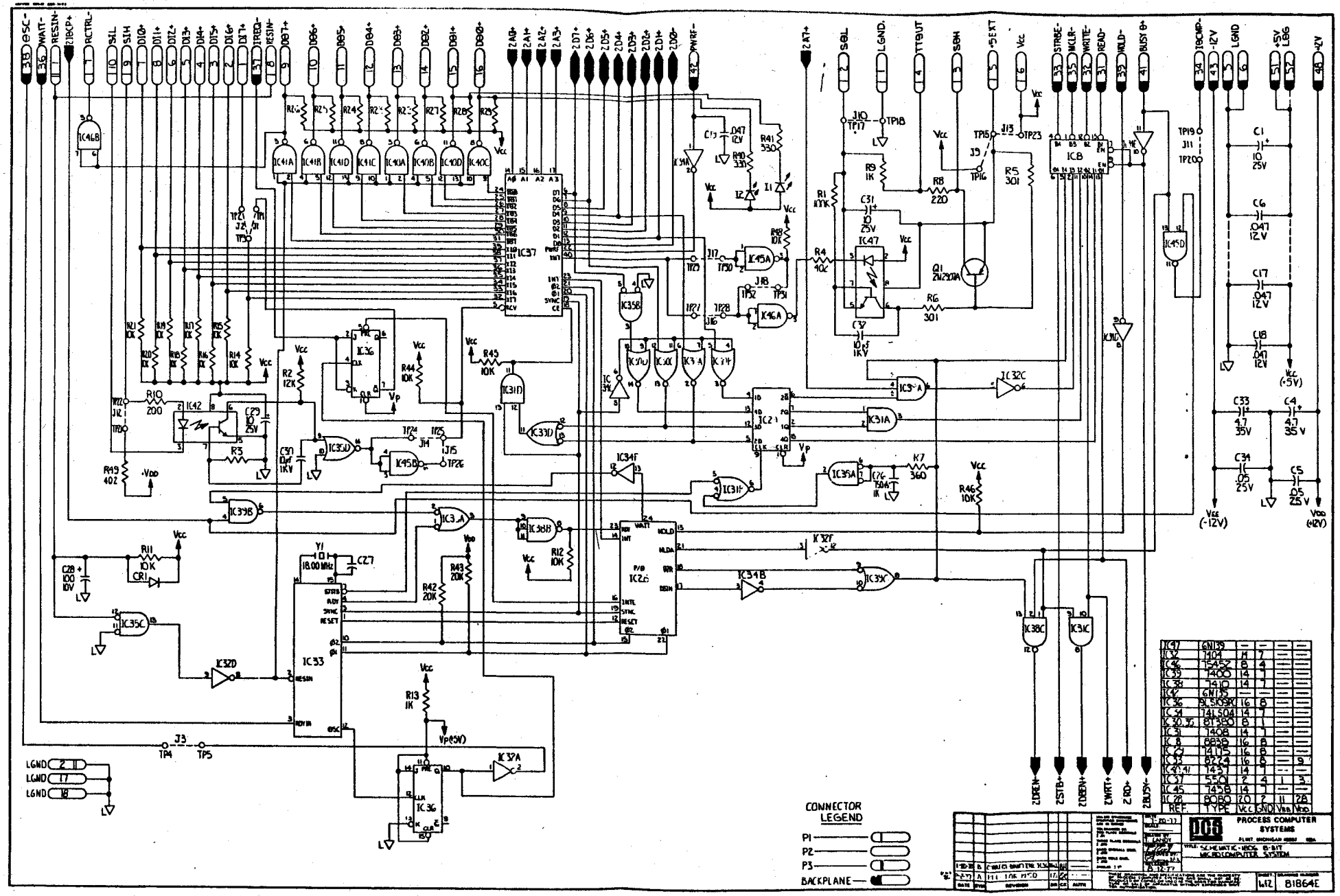
TABULATED PARTS LIST

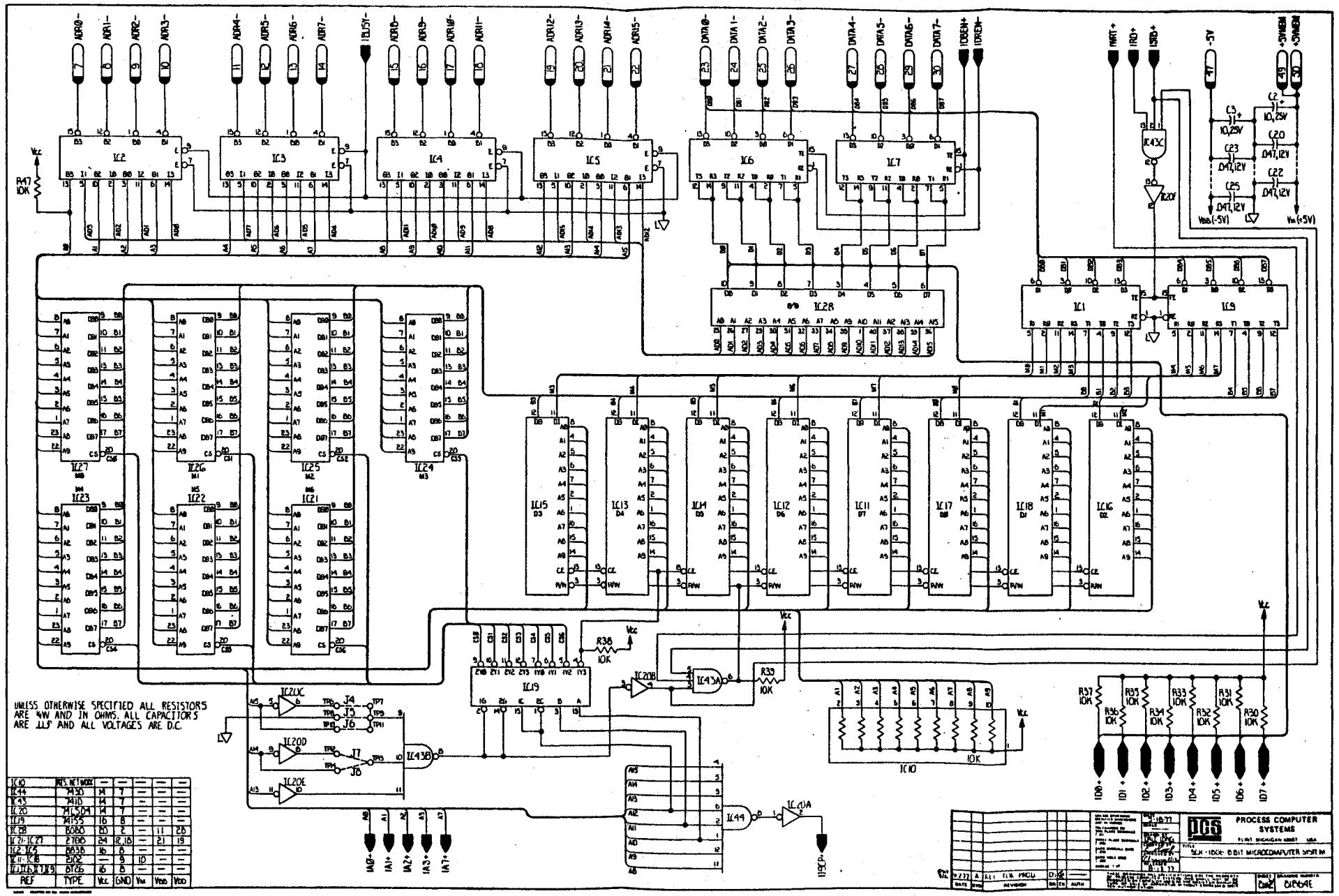
DATE 8-23-77
SCALE FULL
DRAWN BY TIM CANDY
CHECKED BY
APPROVED BY
RELEASED 8-25-77

DIGITAL EQUIPMENT CORPORATION
PROCESS COMPUTER SYSTEMS

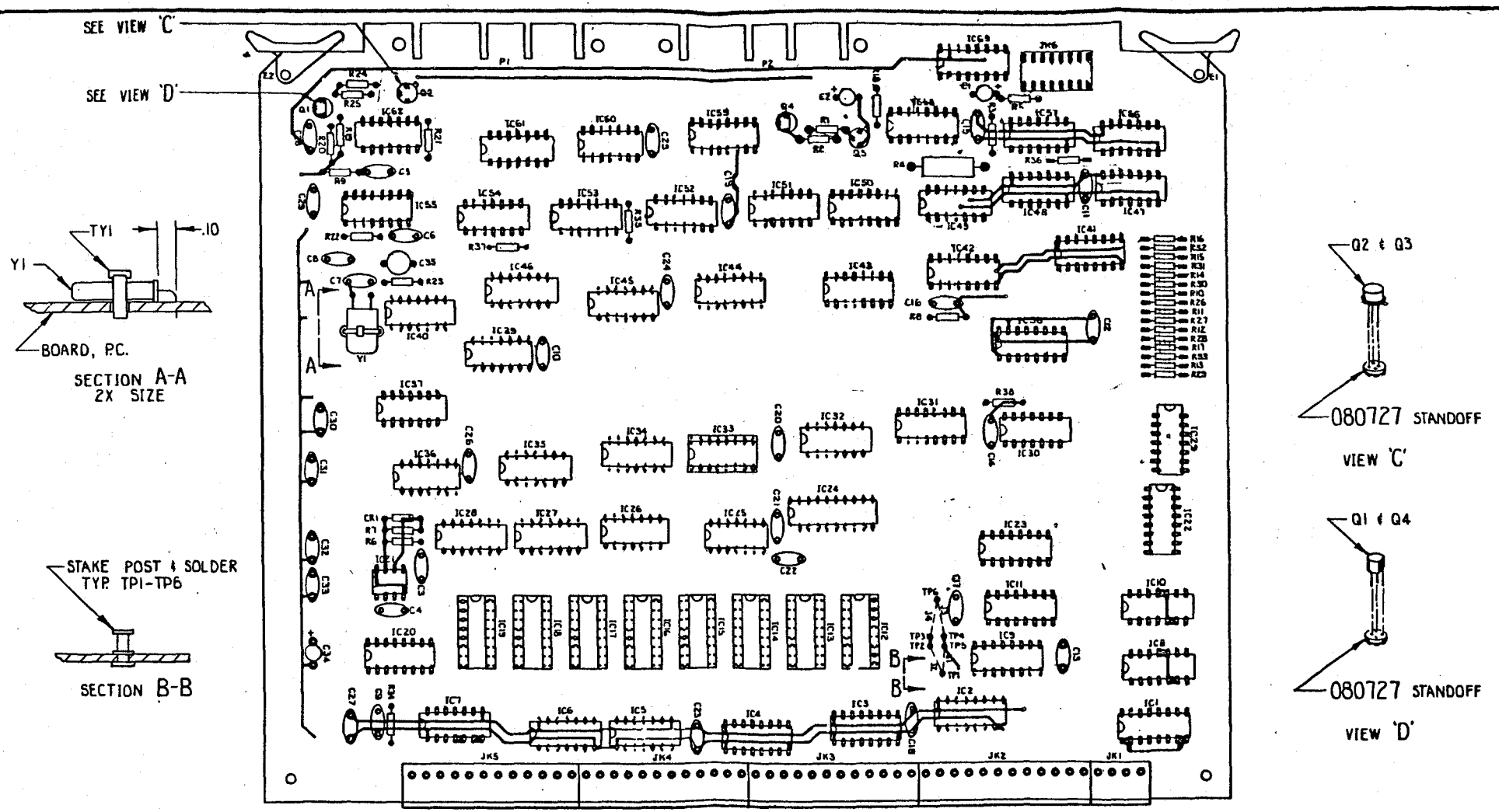
TITLE ASM-1806 8-BIT MICROCOMPUTER SYSTEM

SIZE | SHEET 3 of 3 | DRAWING NUMBER 81662-003E


CONNECTOR LEGEND
P1
P2
P3
BACKPLANE
PROCESS COMPUTER SYSTEMS
B1864E



IC#	PKG NET INDEX					
IC44	7430	14	7	—	—	—
IC43	7410	14	7	—	—	—
IC20	74LS04	14	7	—	—	—
IC19	74155	16	8	—	—	—
IC28	8080	40	2	—	11	26
IC27-IC24	2708	24	12,16	—	21	19
IC2-IC5	8638	16	8	—	—	—
IC1-IC6	8T02	—	8	10	—	—
IC10,X,X,X,9	8T26	16	8	—	—	—
REF	TYPE	Vcc	GND	Vm	Vbb	Vdd



SECTION A-A
2X SIZE

SECTION B-B

VIEW 'C'

VIEW 'D'

DATE	SYM	REVISION	DR	CK	AUTH
2-23-77	A	ENG REL.	DS	GR	

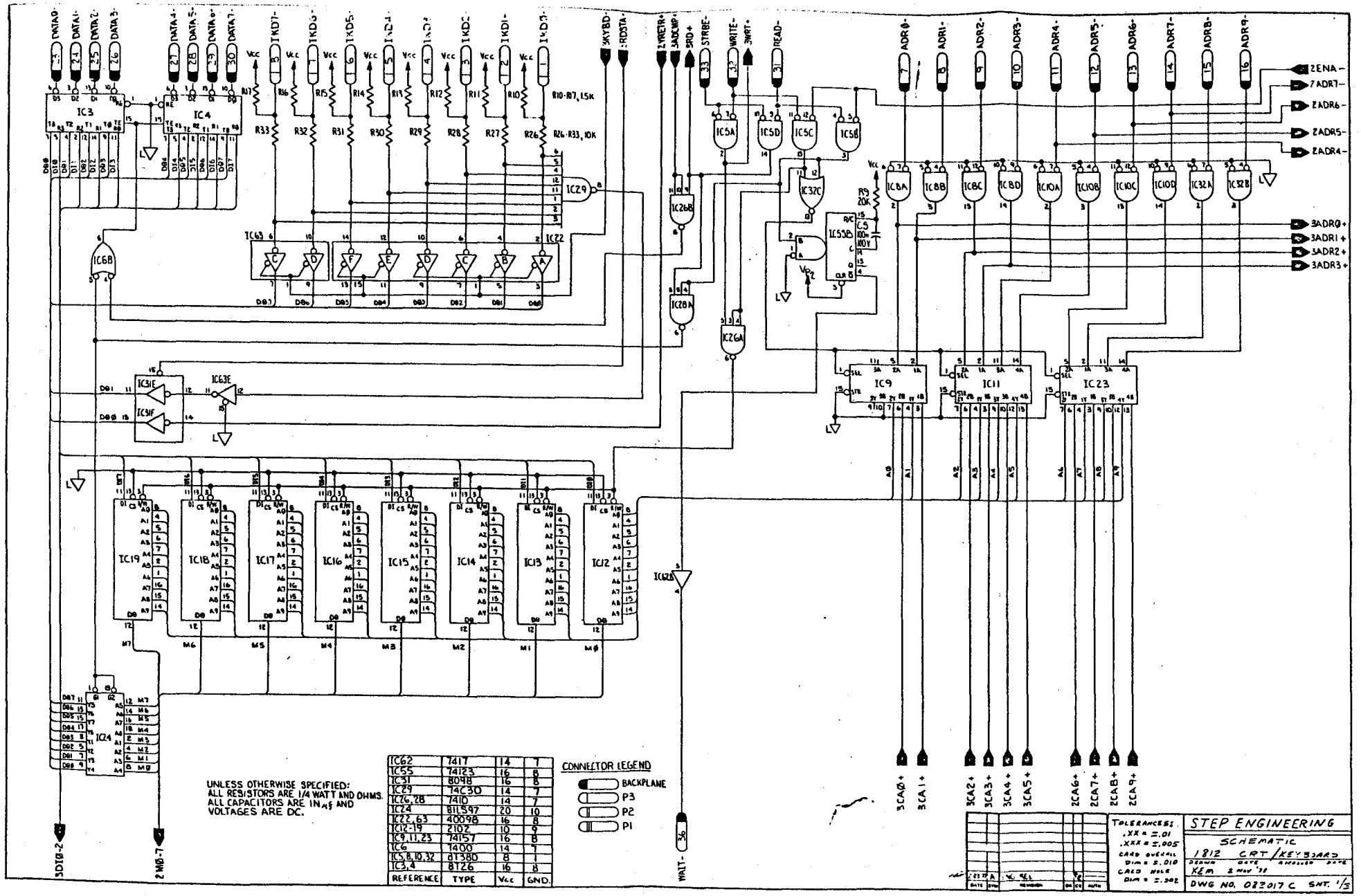
TOLERANCES:
.XX = ±.01
.XXX = ±.005
CARD OVERALL DIM = ±.010
CARD HOLE DIM = ±.002

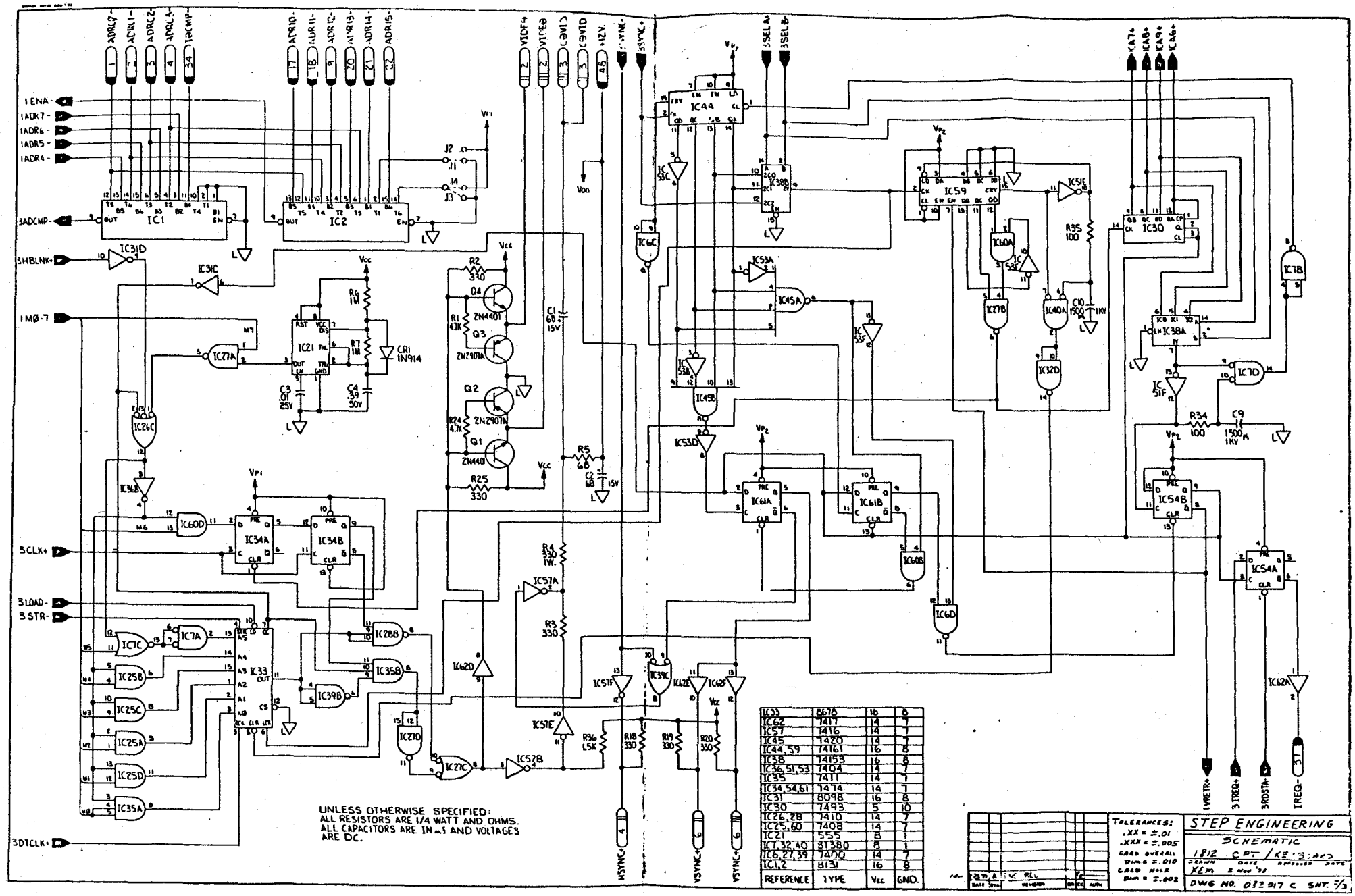
STEP ENGINEERING

ASSEMBLY
1812 CRT/KEYBOARD

DRAWN	DATE	APPROVED	DATE
KEM	2 NOV '78		

DWG NO. 082015C SHT. 1/1


UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 WATT AND OHMS.
ALL CAPACITORS ARE IN μF AND
VOLTAGES ARE DC.
CONNECTOR LEGEND
BACKPLANE
P3
P2
P1
IC62 7417 14 7
IC55 74123 16 8
IC31 8098 16 8
IC29 74C30 14 7
IC26,28 7410 14 7
IC24 81LS97 20 10
IC22,63 40098 16 8
IC12-19 2102 10 9
IC9,11,23 74157 16 8
IC6 7400 14 7
IC5,8,10,32 81388 16 8
IC3,4 8126 16 8
REFERENCE TYPE Vcc GND.
TOLERANCES:
.XX = ±.01
.XXX = ±.005
CARD OVERALL DIM = ±.010
CARD HOLE DIM = ±.002
STEP ENGINEERING
SCHEMATIC
1812 CRT/KEYBOARD
DRAWN KEM 2 MAY '75
DATE
APPROVED
DATE
DWG NO. 022017 C SHT. 1/3

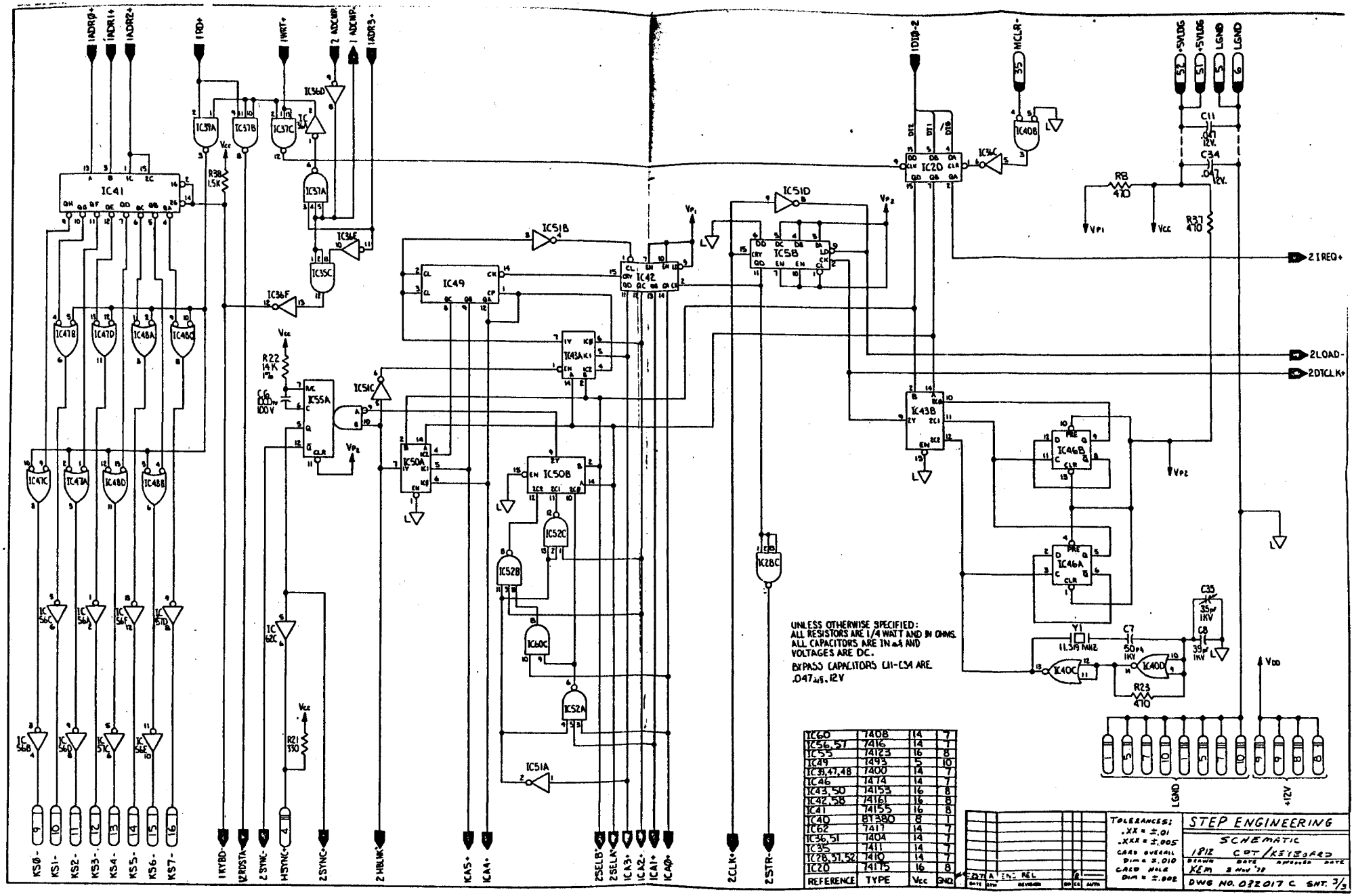


UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 WATT AND OHMS.
ALL CAPACITORS ARE IN μF AND VOLTAGES ARE DC.

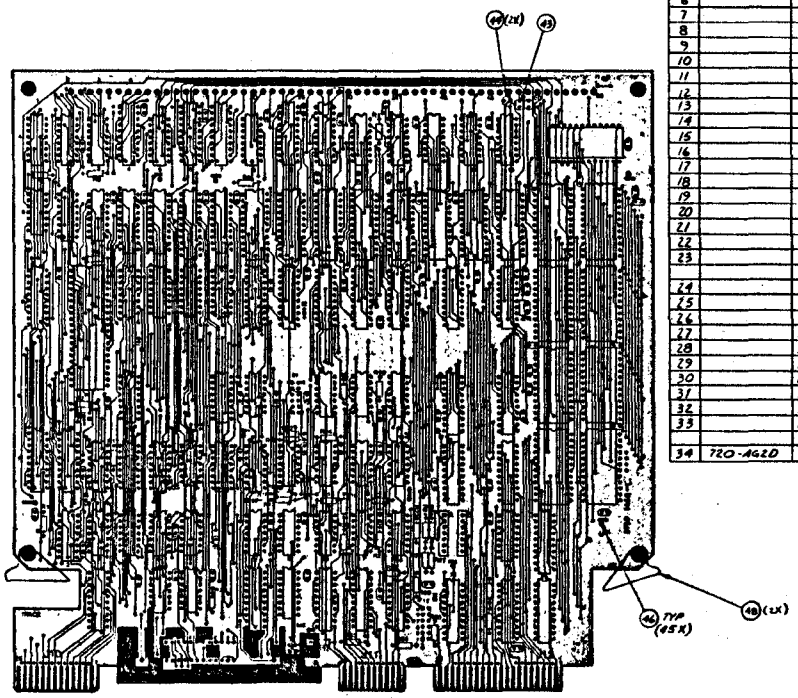
IC33	8616	16	8
IC62	7417	14	7
IC57	1416	14	1
IC45	7420	14	7
IC44,59	74161	16	8
IC38	74153	16	8
IC36,51,53	7404	14	7
IC35	7411	14	7
IC34,54,61	7474	14	7
IC31	8098	16	8
IC30	7493	5	10
IC26,28	7410	14	7
IC25,60	7408	14	7
IC21	555	8	1
IC7,32,40	81380	8	1
IC6,27,39	7400	14	7
IC1,2	8131	16	8
REFERENCE	TYPE	Vcc	GND.

TOLERANCES:
.XX = ±.01
.XXX = ±.005
CARD OVERALL DIM = ±.010
CARD HOLE DIM = ±.002

STEP ENGINEERING
SCHEMATIC
1812 CPT/KE-3 2nd
DRAWN DATE APPROVED DATE
KEM 2 NOV '78
DWG NO. 012017 C SHT. 5/3



REFERENCE	TYPE	Vcc	GND
IC60	7408	14	7
IC56,57	7416	14	7
IC55	74123	16	8
IC49	7493	5	10
IC39,47,48	7400	14	7
IC46	7474	14	7
IC43,50	74153	16	8
IC42,58	74161	16	8
IC41	74155	16	8
IC40	81S80	8	1
IC62	7417	14	7
IC36,51	7404	14	7
IC35	7411	14	7
IC28,31,52	7410	14	7
IC20	74175	16	8



ITEM NO	P/N	DESCRIPTION	LOCATIONS/REMARKS	QTY
1	0001150	PCB TRACE		1
2		MOLEX CONN.	36 PINS	1
3		IC 74LS00	1B	1
4		74S00	10E, 3G	2
5		74S04	6G, 12E	2
6		74S08	11F, 12F	2
7		74S10	8E, 9F, 5H, 6F	4
8		74S11	4G	1
9		74S37	6H, 12G	2
10		74S51	8G, 5G	2
11		74S74	10F, 10G, 11E	3
12		74S86	11G	1
13		74S112	12H	1
14		74LS133	15A	1
15		74LS138	1A, 2A	2
16		74154	17A SEE NOTE [2]	1
17		74S174	8F	1
18		74S163	2B, 3B, 5D, 6D, 11B, 12A, 13A, 14A	8
19		74S175	5F	1
20		74LS240	6A, 4A, 7A, 10A, 9A, 1D, 8H	7
21		74S240	10H, 15H	2
22		74LS244	1F, 2F, 12D, 16H, 16G, 14H	6
23		74S374	8D, 9D, 10D, 11D, 13D, 15D, 13E, 15E, 13F, 15F, 3H, 11H	12
24		74S251	3F, 2G	2
25		IC 74LS377	5B, 4B, 7B, 6B	4
26		IC 8255A	3D	1
27		IC DM8136	3A	1
28		IC 93S46	4D, 7D, 4E, 7E, 4F, 7F	6
29		IC 93L422	8B THRU 15B	8
30		20NS DELAY LINE	13GA, 13GB	2
31		100Ω R-PKG	5A, 8A	2
32		22 PIN SOCKET	8B THRU 15B	8
33		24 PIN SOCKET	17A, 16B, 17B, 16D, 17D, 16E, 17E, 16F, 17F SEE NOTE [3]	9
34	720-AG2D	AUGAT SOCKET	3D, 13GA, 13GB, 12F	4

ITEM NO	P/N	DESCRIPTION	LOCATIONS/REMARKS	QTY
35		RES. 4.7K, 1/4W 5%	R1,2,4,5,6,7,8,9,10,11,12,13,14,15, 16,17,18,21,22,23,28,29,30	23
36		RES. 1K, 1/4W, 5%	R3	1
37		RES. 220Ω	R19, R31, R32, R34	4
38		RES. 330Ω	R33, R20, R35, R36	4
39		RES. 470Ω	R24, R25,	2
40				
41				
42		CAP. .1uF		64
43		CAP. 12uF		1
44		CAP. 39pF		2
45				
46	534-5P100	STRIP LINES		45
47		BNC		2
48		EJECTORS		2

NOTES:
1. ASSEMBLE PER STEP ENG. STANDARDS.
2. INSTALL PULL-UP MODULE PART = 0300009-00 IN PLACE OF 74154 ON BOARDS NOT TO BE LOADED WITH 2716 PROMS.
3. DO NOT INSTALL SOCKETS ON BOARDS NOT TO BE LOADED WITH 2716 PROMS.

LTR	DESCRIPTION	BY	APP	DATE
D	DCO # 48	D.AR.		11-5-80
C	DCO # 47	APPD		9/23/80
B	NEW RELEASE	D.AR.		7-80

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES. TOLERANCES ARE FRACTIONS 1/16" DECIMALS X PLACE ± .01 3 PLACE ± .005 ANGLES ± 1/2°

DO NOT SCALE DRAWING

STEP ENGINEERING

MATERIAL ~ | DRAWN D APPD | DATE 7-80 | FINISH ~ | APPR | DATE

NEXT ASSY ~ | USED ON STEP 3

TITLE ASSY, TRACE BD.

SCALE FULL | SIZE D | DWG NO 0001172 | SHT V1

ROM NAME	PARTS LIST	WIRE LIST	LABLE	MEM	ROM SIZE	ARRAY DEPTH	CHIP SELECT PLUG	CHIP SELECT CLIP	MULTI-PLEX	STD	NO PINS	OUTPUT TYPE	COMMENT	SCHEMATIC NO MASTER/SLAVE
4AM/S	0001123-01	0001118/9-07	0001028-01/02	32	256x4	256	X				16	TS		1010-01/1012-01
4AM/S	0001123-02	0001118/9-08	0001028-03/04	32	256x4	1K		X			16	TS		1010-08/1012-04
4BM/S	0001123-03	0001118/9-05	0001028-11/12	32	512x4	1K		X		X	16	TS		1010-06/1012-04
4BM/S	0001123-04	0001118/9-06	0001028-09/10	32	512x4	512	X				16	TS		1010-02/1012-01
4EM/S	0001123-05	0001118/9-04	0001028-13/14	32	1Kx4	1K	NONE				16	TTL		1010-03/1012-03
4DM/S	0001123-06	0001118/9-01	0001028-19/20	32	1Kx4	1K	X			X	18	TS		1010-04/1012-02
4DM/S	0001123-07	0001118/9-02	0001028-21/22	32	2Kx4	1K	X				18	TS	SIMULATES 1K OF 2Kx4 ROM	1010-08/1012-05
4EM/S	0001123-08	0001120/1-01	0001028-23/24	32	2Kx4	2K	X		X		18	TS		1021-01/02
4EM/S	0001123-09	0001120/1-02	0001028-25/26	32	1Kx4	2K		X	X		18	TS		1021-03/04
4FM/S	0001123-10	0001118/9-11	0001028-15/16	128	512x4	2K		X			18	TS		1010-11/1012-04
4GM/S	0001123-11	0001118/9-03	0001028-27/28	128	1Kx4	4K		X			18	TS		1010-05/1012-04
4HM/S	0001123-12	0001118/9-09	0001028-29/30	128	2Kx4	2K	X				18	TS		1010-10/1012-05
4HM/S	0001123-13	0001118/9-10	0001028-31/32	128	2Kx4	4K		X			18	TS		1010-07/1012-04
4JM/S	0001123-14	0001120/1-03	0001028-33/34	128	2Kx4	8K		X	X		18	TS		1021-05/06
4KM/S	0001123-15	0001118/9-12	0001028-43/44	128	4Kx4	4K	X				20	TS		1010-12/1012-06
	0001123-	0001	0001028-											

THIS PAGE CONTAINS NON LATCHING 4 BIT ROM SIMULATION

NOTES: UNLESS OTHERWISE SPECIFIED

1) CHIP SELECT: AN "X" UNDER PLUG INDICATES THE CHIP SELECT INPUTS ARE PICKED UP ON THE ROM SOCKET THRU THE ROM SIMULATION CABLE

AN "X" UNDER CLIP INDICATES CHIP SELECT INPUTS ARE PICKED UP ON AN EXTERNAL CLIP. THIS ALLOWS EASIER SIMULATION OF "WIRED-ORed" ROMS IN DEEP MEMORY ARRAYS

2) MULTIPLEXING: TWO BYTES OF 8 BITS EACH ARE MULTIPLEXED ON A SINGLE LINE. USED TO INCREASE MEMORY DEPTH. NOTE: NON MULTIPLEXING ROM MODULES HAVE FOUR MODULES PER MEMORY BOARD; MULTIPLEXING TYPES HAVE TWO MODULES PER MEMORY BOARD.

3) STD: ROM SIMULATION TYPES MARKED STD (STANDARD) ARE GENERALLY IN STOCK.

4) OUTPUT TYPE: TS - TRISTATE; TTL - TOTEM POLE; L - LATCHING; R - REGISTER

LTR	DESCRIPTION	BY	APP	DATE
A	FINAL RISE # 0032	CM		3/8/84

REVISIONS

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON ROM SIM

MATERIAL | DRAWN JM 12/19/84

TITLE SUMMARY ROM SIMULATION

DO NOT SCALE DRAWING | FINISH | APPR | DATE | SCALE | DWG NO 0001122 | REV | SHT 1/4

ROM NAME	PARTS LIST	WIRE LIST	LABLE	MEM	ROM SIZE	ARRAY DEPTH	CHIP SELECT PLUG	CHIP SELECT CLIP	MULTI-PLEX	STD	NO PINS	OUTPUT TYPE	COMMENT	SCHEMATIC NO MASTER/SLAVE
8LM/S	0001123-16	0001126/7-01	0001028-05 06	32	32x8	32	X				16	TS		1049-01/02
8LM/S	0001123-17	0001126/7-02	0001028-07 08	32	32x8	64		X			16	TS		1049-03/04
8CM/S	0001123-18	0001128/9-01	0001028-49 50	32	256x8	256	X				20	TS		1014-01/03
8CM/S	0001123-19	0001128/9-02	0001028-51 52	32	256x8	1K		X			20	TS		1014-04/05
8FM/S	0001123-20	0001128/9-03	0001028-53 54	32	512x8	512	X				20	TS		1014-02/06
8FM/S	0001123-21	0001128/9-04	0001028-55 56	32	512x8	1K		X		X	20	TS		1014-07/05
8AAM/S	0001123-22	0001131/2-01	0001028-57 58	32	512x8	2K		X	X		20	TS		NONE
8BBM/S	0001123-23	0001128/9-05	0001028-59 60	128	512x8	2K		X			20	TS		1014-08/05
8RM/S	0001123-24	0001133/4-01	0001028-67 68	32	512x8	512	X				22	R		1135-01/02
8RM/S	0001123-25	0001133/4-02	0001028-69 70	32/128	512x8	1K/2K		X			22	R	(A)(B)	1135-03/04
8RM/S	0001123-26	0001133/4-03	0001028-71 72	32/128	512x8	1K/2K		X			22	R	(A)(C)	1135-05/06
8AM/S	0001123-27	0001136/7-01	0001028-79 80	32	256x8	256	X				24	L		1015-01/03
8DM/S	0001123-28	0001136/7-02	0001028-81 82	32	512x8	512	X			X	24	L		1015-02/03
8DM/S	0001123-48	0001136/7-04	0001028-109 110	32	512x8	1K		X			24	L		1015-04/05
8PM/S	0001123-29	0001136/7-03	0001028-83 84	32	1Kx8	1K	X				24	L		1078-01/02
8EE M/S	0001123-51	0001142/3-01	0001028-133 134	32/128	512x8	1K/4K	X			X	24SL	R	27S25	0400011-01/02
8EE M/S	0001123-52	0001142/3-02	0001028-135	32	512x8	1K		X		X	24SL	R	27S25	0400011-03/04

THIS PAGE CONTAINS 8 BIT ROM SIMULATION: LATCHING, <24 PIN DIPS

NOTES: UNLESS OTHERWISE SPECIFIED

(A) ON ROM 8RM/S VER 25, 26 ARRAY DEPTH DEPENDS ON MEMORY USED: 2K (MEM 128); 1K (MEM 32)

(B) DEPTH EXPANSION THRU EXTERNAL ASYNCRONOUS ENABLE

(C) DEPTH EXPANSION THRU EXTERNAL SYNCRONOUS ENABLE

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

MATERIAL | DRAWN | DATE 12/2/76

TITLE SUMMARY ROM SIMULATION

DO NOT SCALE DRAWING | FINISH | APPR | DATE | DWG NO 0001122 | REV | SHT 2

ROM NAME	PARTS LIST	WIRE LIST	LABLE MASTER/SLAVE	MEM	ROM SIZE	ARRAY DEPTH	CHIP SELECT PLUG	CHIP SELECT CLIP	MULTI-PLEX	STD	NO PINS	OUT PUT TYPE	COMMENT	SCHEMATIC NUMBER-MASTER/SLAVE
8BM/S	0001123-30	0001124/5-01	0001028- 85/86	32	256x8	256	X				24	TS		1016-01/05
8BM/S	0001123-31	0001124/5-02	0001028- 87/88	32	256x8	1K		X			24	TS		1016-13/12
8EM/S	0001123-32	0001124/5-03	0001028- 89/90	32	512x8	512	X				24	TS		1016-02/05
8EM/S	0001123-33	0001124/5-04	0001028- 91/92	32	512x8	1K		X			24	TS		1016-14/12
8GM/S	0001123-34	0001124/5-05	0001028- 93/94	32	1Kx8	1K	X			X	24	TS		1016-03/05
8HM/S	0001123-35	0001124/5-06	0001028- 95/96	32	1Kx8	1K	X				24	TS	EROM REPLACEMENT	1016-04/06
8QM/S	0001123-36	0001124/5-07	0001028- 97/98	128	512x8	2K		X			24	TS		1016-15/12
8UM/S	0001123-37	0001124/5-08	0001028- 99/100	128	4Kx8	4K	X				24	TS	EROM REPLACEMENT	1016-10/11
8VM/S	0001123-38	0001124/5-09	0001028- 101/102	128	1Kx8	4K		X			24	TS		1016-08/09
8WM/S	0001123-39	0001124/5-10	0001028- 103/104	128	2Kx8	2K	X				24	TS		1016-16/17
8WM/S	0001123-40	0001124/5-11	0001028- 105/106	128	2Kx8	4K		X			24	TS		1016-18/12
8CCM/S	0001123-41	0001124/5-12	0001028- 107/108	128	2Kx8	2K	X				24	TS	EROM REPLACEMENT	1016-19/20
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											

THIS PAGE CONTAINS NONMULTIPLEXING 8 BIT, 24 PIN ROM SIMULATION

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 USED ON

TITLE SUMMARY ROM SIMULATION

MATERIAL | DRAWN SGH 12/20/84 | DATE

FINISH | CHKD | DATE

DO NOT SCALE DRAWING | SCALE | SIZE | DWG NO 0001122 | REV | SH 3

ROM NAME	PARTS LIST	WIRE LIST	LABLE	MEM	ROM SIZE	ARRAY DEPTH	CHIP SELECT PLUG	CHIP SELECT CLIP	MULTI-PLEX	STD	NO PINS	OUT PUT	COMMENT	SCHEMATIC NO MASTER/SLAVE
8JM/S	0001123-42	0001138/9-01	0001028-115/116	32	2K×8	2K	X		X		24	TS		1022-01/02
8KM/S	0001123-43	0001138/9-02	0001028-117/118	32	2K×8	2K	X		X		24	TS	EROM REPLACEMENT	1022-07/08
8NM/S	0001123-44	0001138/9-03	0001028-119/120	32	512×8	2K	X		X		24	TS		1022-03/04
8TM/S	0001123-45	0001138/9-04	0001028-121/122	128	1K×8	8K	X		X		24	TS		1022-09/10
8TM/S	0001123-46	0001138/9-05	0001028-123/124	128	2K×8	8K		X	X		24	TS		1022-11/12
8YM/S	0001123-47	0001138/9-06	0001028-125/126	32	1K×8	2K	X		X		24	TS		1022-05/06
8DDM/S	0001123-49	0001140/1-01	0001028-127/128	128	4K×8	8K	X		X		24	TS	2732	1022-13/14
8DDM/S	0001123-50	0001140/1-02	0001028-129/130	128	4K×8	8K		X	X		24	TS	2732	1022-15/16
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											
	0001123-	0001	0001028-											

THIS PAGE CONTAINS MULTIPLEXING 8 BIT 24 PIN ROM SIMULATION

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: 1/32 DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

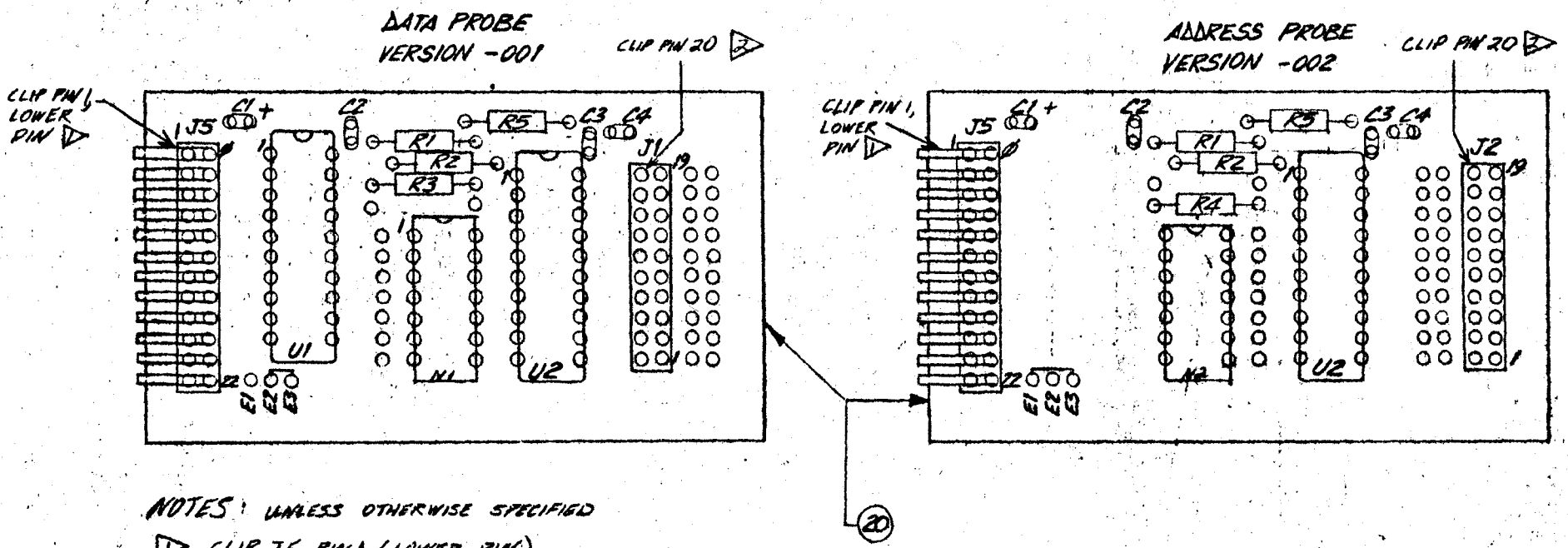
NEXT ASSY 0001123 USED ON

MATERIAL | DRAWN | DATE

FINISH | APPR | DATE

TITLE SUMMARY, ROM SIMULATION

DO NOT SCALE DRAWING | SCALE | SIZE | DWG NO 0001122 | REV | SHT 4



NOTES: UNLESS OTHERWISE SPECIFIED

1. CLIP J5 PIN 1 (LOWER PIN)
2. CLIP J1, J2 PIN 20
3. ON REV A PC BOARDS: J5 SHOULD USE STRAIGHT STRIPLINE PLUGS, ITEM 13 IN PLACE OF ITEM 14

WIRE LIST

VERSION	CONNECTION
001	E2 TO E3
002	E1 TO E3

LTR	ITEM	DESCRIPTION	BY	APP	DATE
B		REVERSE N1, N2 POSITION	PMP	PMP	6/11/79
A		PROD RLSE	SMP	PMP	5/14/79

REVISION CHART

STEP ENGINEERING

SCALE: 2:1 | DATE: 5-4-79 | APPROVED BY: SMP 6/1/79 | DRAWN BY: PMP | REVISED

ASSEMBLY, DATA/ADDRESS PROBE

SHEET 1 OF 2 | SIZE B | REV A | DRAWING NUMBER 0001108

5 4 3

1 MS 8 1/80

BILL OF MATERIALS

ITEM	PART NO.	QTY	DESCRIPTION	VERSION -001	VERSION -002
1	2N74S374	1	I.C.	U1	
2	2N74S240	1	I.C.	U2	U2
3	8R1-3-R100	1	I.C. R-NETWORK, 100Ω	N1	
4	4114R-001-330	1	I.C. R-NETWORK, 33-Ω		N2
5	RC07GF101J	1	RESISTOR 100Ω, ¼W, 5%	R3	R4
6	RC07GF331J	1	330Ω	R2	R2
7	RC07GF102J	1	1K	R5	R5
8	RC07GF472J	1	RESISTOR 4.7K, ¼W, 5%	R1	R1
9					
10	CY20C104P	3	CAPACITOR, 0.1 μf	C2,3,4	C2,3,4
11	196D396X9010AM1 SPRAGUE	1	CAPACITOR, 39 μf	C1	C1
12					
13	D725P100-.230-.430	1	STRIP LINE PLUG, DUAL 20 POS	J1	J2
14	D725P100-.230-.430	1	STRIP LINE PLUG, DUAL 11 POS.	J5	J5
15					
16	CA336SP100-.230-.430	1/10	SQUARE POST	A/R	A/R
17	720AG-20	1	SOCKET FOR ITEM 2	—	—
18					
19					
20	0001107	1	PC BOARD	X	X
21					
22					
				DATA PROBE	ADDR PROBE

3

LTR	REV#	DESCRIPTION	DATE	BY
	B	CORRECT FOR MULTIWIRE ADD SOCKET FOR S240	12/7/79	BW

REVISION CHART

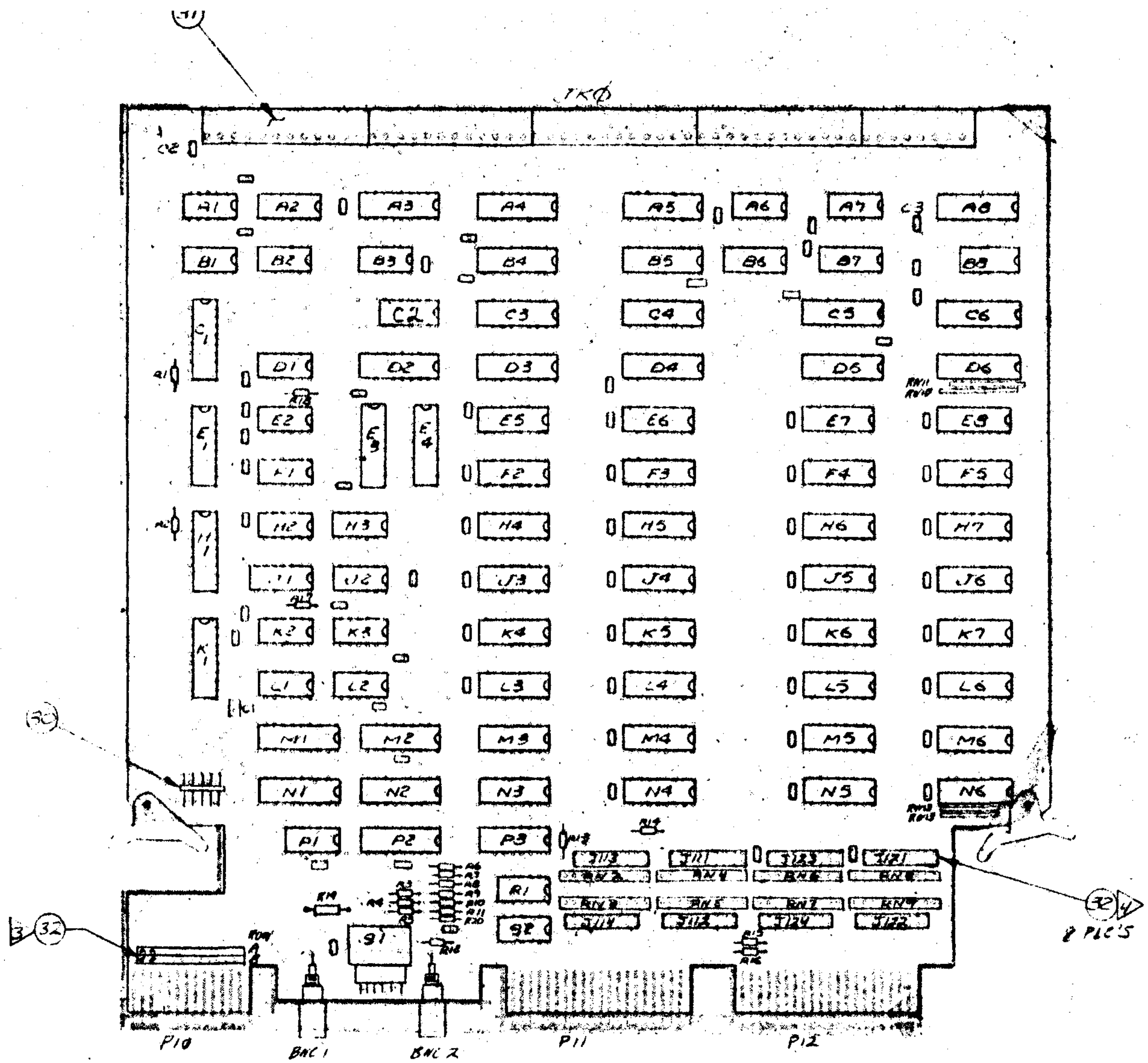
STER ENGINEERING

SCALE: ~ | APPROVED BY: BW 6/1/79 | DRAWN BY: LM | DATE: 5-2-79 | REVISED

ASSEMBLY, DATA/ADDRESS PROBE

SHEET 2 OF 2 | SIZE B | REV A | DRAWING NUMBER 0001108

8011 SH2



VERSION CHART ⚠4

DWG NO	PART NAME	PART NUMBER	LIST OF MATERIALS	WIRE LIST (SEE SHT 2)
-10	MEM 32F	0001112-10	0001113-10	
-20	MEM 32A	0001112-20	0001113-20	
-30	MEM 32A	0001112-30	0001113-30	

LTR	NUMBER	DESCRIPTION	BY	DATE
D	#40	USER PORT WET FIX	QA	6/6/8
C	—	NO CIRCUIT CHANGE DOC ONLY	QA	[illegible]
B	021	[illegible]	[illegible]	[illegible]
A	—	PRODUCT RELEASE	[illegible]	

REVISIONS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS TO BE .1uF EXCEPT C1, C2, C3.
2. .1uF CAPACITORS SHOWN WITHOUT REF NUMBERS ON ASSY DWG

⚠3 WIREWRAP BETWEEN CORRESPONDING POSTS ON ROW A AND ROW B (13 WIREWRAPS)

⚠4 [illegible] VERSION CHART FOR LIST OF MATERIALS AND APPLICABLE WIRE LIST

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
		1	0	0	0001112-30	MEM 32 A	45NS VERSION, INTEL RAM	3
		0	1	0	0001112-20	MEM 32 A	45NS VERSION, FAIRCH RAM	2
		0	0	1	0001112-10	MEM 32 F	HIGH SPEED VERSION	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS ✓

TOLERANCE
DIMENSIONAL: .X ± .1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010
HOLE SIZE: 0 .599 ± .003; .600 .999 ± .004; 1.000-1.499 ± .005

BEND RADIUS

FINISH

DASH NO. | NUMBER | QTY | NEXT ASSEMBLY

DRAWN: E. Good — DATE: 11/1/75
CHECKED: [illegible] — 5/[illegible]
ENGINEER
MANUFACTURING
QUALITY ASSUR

STEP ENGINEERING

TITLE: ASSEMBLY MEM 32 A & F

SCALE: 1 to 1 | SIZE: C | PART NUMBER: 0001112 | REV: D

CODE | SHEET 1 OF 2

WIRE LIST CHARTS

TO	FROM	NAME J121	J123	J111	J113
3	4	R0	R10	R20	R30
7	8	R2	R12	R22	R32
11	12	R4	R14	R24	R34
15	16	R6	R16	R26	R36

J111 TO J116
J113 TO J115
J121 TO J121
J123 TO J123

TO	FROM	NAME J122	J124	J112	J114
5	6	D1	D9	D17	D25
9	10	D3	D11	D19	D27
13	14	D5	D13	D21	D29
17	18	D7	D15	D23	D31

J112 TO J112
J114 TO J114
J122 TO J122
J124 TO J124

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
6	4	D0	D8	D16	D24
5	3	R1	R11	R21	R31
10	8	D2	D10	D18	D26
9	7	R3	R13	R23	R33
14	12	D4	D12	D20	D28
13	11	R5	R15	R25	R35
18	16	D6	D14	D22	D30
17	15	R7	R17	R27	R37

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

VERSION X1

RESISTIVE TERMINATION

TO	FROM	NAME J121	J123	J111	J113
5	6	R1	R11	R21	R31
7	8	R2	R12	R22	R32
13	14	R5	R15	R25	R35
15	16	R6	R16	R26	R36
1	2	E0	E1	E2	E3

J111 TO J111
J113 TO J113
J121 TO J121
J123 TO J123

TO	FROM	NAME J122	J124	J112	J114
1	4	D0	D8	D16	D24
7	10	D3	D11	D19	D27
9	12	D4	D12	D20	D28
15	18	D7	D15	D23	D31
2	17	UL	UL	UL	UL

9

J112 TO J112
J114 TO J114
J122 TO J122
J124 TO J124

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
3	3	R0	R10	R20	R30
4	6	D1	D9	D17	D25
10	8	D2	D10	D18	D26
9	5	R3	R13	R23	R33
11	11	R4	R14	R24	R34
12	14	D5	D13	D21	D29
18	16	D6	D14	D22	D30
17	13	R7	R17	R27	R37

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

VERSION X3, X4, X5

X3: REGISTER OUTPUT (TS)
X4: LATCHING OUTPUT (TS)
X5: BUFFER OUTPUT (TRISTATE)

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
3	4	R0 D0	R10 D8	R20 D16	R30 D24
5	6	R1 D1	R11 D9	R21 D17	R31 D25
7	8	R2 D2	R12 D10	R22 D18	R32 D26
9	10	R3 D3	R13 D11	R23 D19	R33 D27
11	12	R4 D4	R14 D12	R24 D20	R34 D28
13	14	R5 D5	R15 D13	R25 D21	R35 D29
15	16	R6 D6	R16 D14	R26 D22	R36 D30
17	18	R7 D7	R17 D15	R27 D23	R37 D31

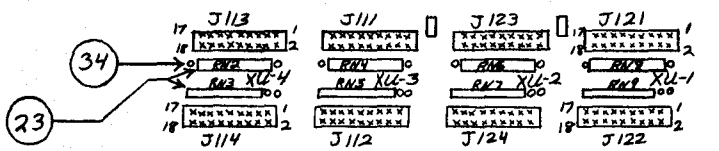
J111 TO J111
J112 TO J112
J113 TO J113
J114 TO J114
J121 TO J121
J122 TO J122
J123 TO J123
J124 TO J124

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
1	1	E0	E1	E2	E3
2	2	W00	W01	W00	W01

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

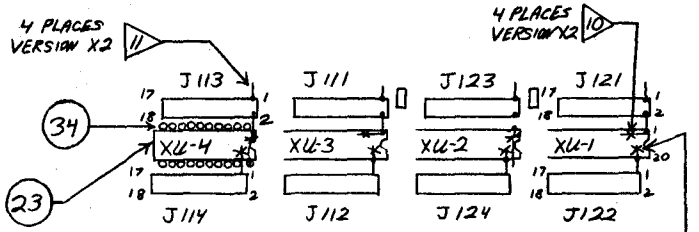
VERSION X2

BIDIRECTIONAL TRISTATE DRIVER



RN2 THRU RN9
51Ω SIP RESISTORS

VERSION X1



XU-1 THRU XU-4: ON -X2 VER 74LS245
ON -X3 VER 74S374
ON -X4 VER 74S373
ON -X5 VER 74S 373

VERSIONS -X2, -X3, -X4, -X5

NOTES (CONTINUED)

10 ON VERSION X2 WIRE THE FOLLOWING:
W00: S2 PIN 11 TO J112 & J122 PIN 2; W01: S2 PIN 8 TO J114 & J124 PIN 2
E0: R1 PIN 6 TO J121 PIN 1 ; E2: R1 PIN 3 TO J111 PIN 1
E1: R1 PIN 11 TO J123 PIN 1 ; E3: R1 PIN 8 TO J113 PIN 1

THE ABOVE APPLIES TO REV A PC BOARDS ONLY

ON REV B AND HIGHER PC BOARDS:

CUT UL LINE JUST PRIOR TO CONNECTION WITH J114 PIN 2
FEEDTHRU AND WIRE S2 PIN 11 TO THE J114 PIN 2 FEEDTHRU
NOTE: TO CHANGE TO VER X3, X4, OR X5 THE ORIGINAL CONNECTIONS MUST BE RESTORED

NOTES (CONTINUED)

6 WIRE WRAP PER WIRE LISTCHART AND ASSEMBLE PER DIAGRAM SHOWN FOR EACH VERSION

7 ASSEMBLY VERSION SHOWN AS DASH XY (0001080-XY) WHERE "X" SPECIFIES MEMORY TYPE AND "Y" SPECIFIES INTERFACE CONFIGURATION

8 CUT TRACE FROM UL TO J112, J114, J122, J124 PIN 1 ON COMPONENT SIDE OF BOARD AS SHOWN FOR VERSIONS X2, X3, X4, X5. ON VERSIONS X3, X4, X5 WIRE UL TO PIN 2 OF J112, J114, J122, J124. THIS APPLIES TO REV A PC BOARDS ONLY

9 WIRE PIN 2 TO PIN 17 ON VERSIONS X3, X4 ONLY. LEAVE PIN 2 OPEN ON X5

10 ON VERSION X2 CUT TRACES FROM: E0 TO XU-1 PIN 1 (SOLDER SIDE), E1 TO XU-2 PIN 1 (COMPONENT SIDE), E2 TO XU-3 PIN 1 (SOLDER SIDE), E3 TO XU-4 PIN 1 (COMPONENT SIDE). THIS APPLIES TO REV A PC BOARDS ONLY

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ±1/32 DECIMAL .01 ANGLES ± 0°30'

STEP ENGINEERING

NEXT ASSY | USED ON

TITLE ASSEMBLY MEM32A PC BOARD

MATERIAL | DRAWN | DATE | FINISH | APPR | DATE | SCALE | SIZE | DWG NO 0001112 | REV D | SHT

DO NOT SCALE DRAWING

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1				1	1	1	0001114	P.C. BOARD				
2				1	1	1		INTEGRATED CIRCUIT	F1	74S00	QUAD 2 INPUT NAND GATE	
3				4	4	4			A6, B1, B3, L2	74LS00	QUAD 2 INPUT NAND GATE	
4				1	1	1			P1	74LS05	HEX INVERTERS	
5				1	1	1			P3	74LS08	QUAD 2 INPUT POS. AND GATE	
6				1	1	1			A7	74LS13	DUAL 4 INPUT POS NAND SCHMITT TRIG.	
7				1	1	1			L1	74S30	8 INPUT POS. NAND GATE	
8				2	2	2			A1, D1	74LS30	8 INPUT POS. NAND GATE	
9				2	2	2			R1, S2, B8	74S32	QUAD 2 INPUT POS. OR GATE	
10				6	6	6			B2, H2, N3, J2, K3, L2	74S86	QUAD EXCLUSIVE OR	
11				2	2	2			E2, K2	74128	50 OHM LINE DRIVER	
12				1	1	1			J1	74S133	13 INPUT POS NAND GATE	
13				1	1	1			A2	74LS138	3 TO 8 LINE DECODER	
14				1	1	1			B6	74LS139	2 TO 4 LINE DECODER	
15				9	9	9			A3, A4, A5, A8, B4, D2, E3, E4,	74LS240	OCTAL TRISTATE BUFFER	
16				9	9	9			C3, C4, C5, C6, D3, D4, D5, D6, C1	74LS244	OCTAL BUFFER	
17				3	3	3			E1, H1, K1	74LS377	OCTAL LATCH	
18				1	1	1		INTEGRATED CIRCUIT	B7	74S257	QUAD MULTIPLEXER	

REF. DRAWINGS
0001112
0001111

REV	DESCRIPTION	DATE	DWN	CKD	APPD
D	USER PART NUMBER FIX DCO# 40	8/4/80	D.A.	D.A.	
C	MOD FOR REV C PCB, ADD SHT 4 DCO# 270	2/27/80			
B	ADD -20 VERSION	1/3/79			
A	PRODUCT RELEASE	12/6/78			

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

		DATE
DRAWN	E. Good	11/9/78
CHECKED		12/8/78
ENGINEER		12/8/78
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

MEM 32 PCB

STEP ENGINEERING

B	000-1113-	REV D

MODEL | CODE | SHEET 1 OF 4

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE	COMMENTS	TOTAL COST	UNIT COST
19				0	0	32		INTEGRATED CIRCUIT	E5,E6,E7,E8 F2,F3,F4,F5	D2125H-3	RAM, STATIC, 1K×1 20 NS ACCESS				
—				0	32	0		↕	H4,H5,H6,H7 J3,J4,J5,J6	93425ADC	RAM, STATIC, 1K×1 30NS ACCESS				
—				32	0	0		↕	K4,K5,K6,K7 L3,L4,L5,L6	D2115H-1	RAM, STATIC, 1K×1 30NS ACCESS				
—				—	—	—		INTEGRATED CIRCUIT	M3,M4,M5,M6 N3,N4,N5,N6						
20				5	5	5		RESISTOR	R2,8,9,10,11	RC07GF103J	10K, 5%, 1/4W				
21				4	4	4		RESISTOR	R13,14,15,16	RC07GF510J	51Ω, 5%, 1/4W				
22				10	10	10		RESISTOR	R1,3,4,5,6,7 12,17,18,19,20	RC07GF102J	1KΩ, 5%, 1/4W				
23															
24				~~8~~	~~8~~	~~8~~		~~RESISTOR NETWORK~~	~~RN2 THRU RN 9~~	~~764-3-R 100 BECKMAN OR EQUIV~~	~~100Ω 5% SIP 4 RESISTORS~~				
25				4	4	4		RESISTOR NETWORK	RN 10 THRU RN 13	764-5-R 220/330 BECKMAN OR EQUIV	220/330 LOW PROFILE SIP, 6 COMBM				
26				1	1	1		CAPACITOR	C1	CK05BX391K	390Pf, 10%				
27				62	62	62		CAPACITOR		CY20C104P	.1μf				
28				2	2	2		CAPACITOR	C2,C3	1960396X 9010KA1	39μf, 10V				
29				3	3	3		INTEGRATED CIRCUIT	M2, N2, P2	74S240	OCTAL TRI-STATE BUFFER	CERAMIC PLASTIC			
30				1	1	1		CONNECTOR	P2	CA-034 RSR100-230-000	(CIRCUIT ASSEMBLIES)				
31				1	1	1		CONNECTOR	JKΦ	09-52-3081	(MOLEX)				
32				3	3	13		CONNECTOR	*	D18-3P100-230-430	(MADE BY CUTTING 072				
33				1	1	1		SW. SOCKET	S1	CA-163E 10RAC3-01					

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

MEM 32 PCB

B	000-1113	REV	D
MODEL		CODE	SHEET 2 OF 3

05 03 3/11/83 SH 2

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE	COMMENTS	TOTAL COST	UNIT COST
34				26	26	26		IC SOCKET		720-AG2D	AUGUT (20 PIN)				
35				2	2	2		INTEGATED CKT	N1, M1	74LS374	REGISTER, 8 BITS				
36				2	2	2		EXTRACTOR		3-200	SCANBE				
37				4	4	4		CONNECTOR		09.52.3121	MOLEX				
38				2	2	2		BNC RECEPT.		MIL# UG109A	AMPHENOL				
39				1	1	1		6 POS. SW		01-70-0106	MOLEX				
40				1	1	1	0001111				SCHEMATIC, REF				
41				34	34	34		IC SOCKET		716-AG2D	AUGUT (16 PIN)		USE ON ITEM 19		

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

MEM32 PCB

MODEL

B	000-1113	REV 0
CODE		SHEET 3 OF 3

1113 SH3

COMMENT	ITEM	QUANTITY PER ASSEMBLY X8	X7	X6	X5	X4	X3	X2	X1	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION
X=1,2,3	23				0	0	0	0	8		RESISTOR PACK	RN2 THRU RN9	784-3-R051 RECKHAM MC 5004	51 OHM SIP RES PACK (4)
X=1,2,3	23				0	0	0	4	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74LS245	OCTAL BUS TRANCEIVER
X=1,2,3	23				0	0	4	0	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74S374	OCTAL D TYPE FLIP FLOP
X=1,2,3	23				4	4	0	0	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74S373	OCTAL D LATCH

VERSION CHART

MEMORY	INTERFACE TYPE X1	X2	X3	X4	X5	X6
1Y	RESISTIVE 36NS ACCESS	BIDIR 48NS ACCESS	REGISTER 58 NS ACCESS	LATCH 54 NS ACCESS	BUFFER 49 NS ACCESS	
2Y	RESISTIVE 45 NS ACCESS	BIDIR 57 NS ACCESS	REGISTER 67 NS ACCESS	LATCH 63 NS ACCESS	BUFFER 58 NS ACCESS	
3Y	RESISTIVE 45 NS ACCESS	BIDIR 57 NS ACCESS	REGISTER 67 NS ACCESS	LATCH 63 NS ACCESS	BUFFER 58 NS ACCESS	
4Y	RESISTIVE	BIDIR	REGISTER	LATCH	BUFFER	
5Y	RESISTIVE	BIDIR	REGISTER	LATCH	BUFFER	
6Y	RESISTIVE	BIDIR	REGISTER	LATCH	BUFFER	

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS: 1/32"
DECIMALS:
2 PLACE ±.01
3 PLACE ±.005
ANGLES: ± 1/2°

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY | USED ON

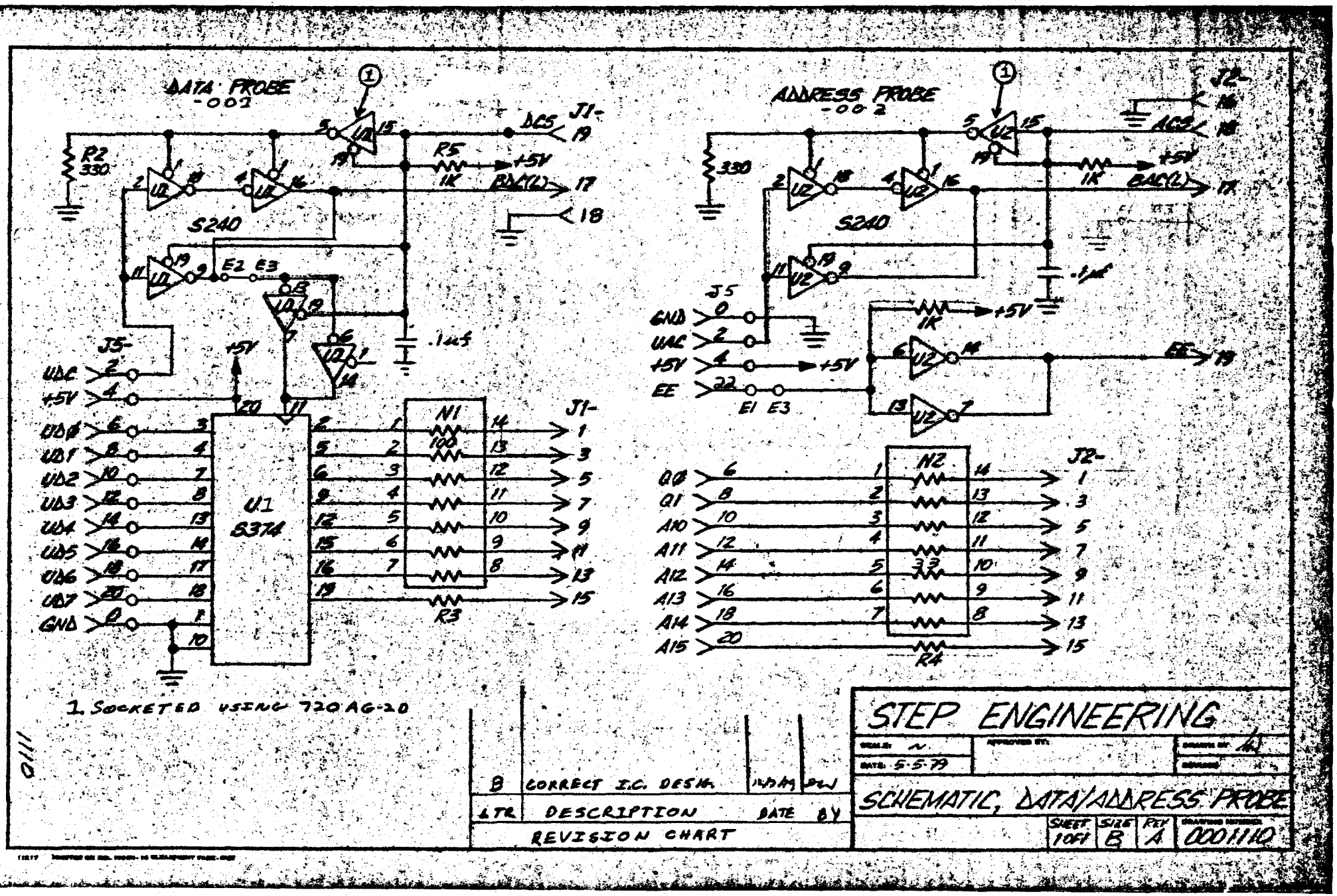
TITLE LIST OF MATERIAL MEM 32 PCB

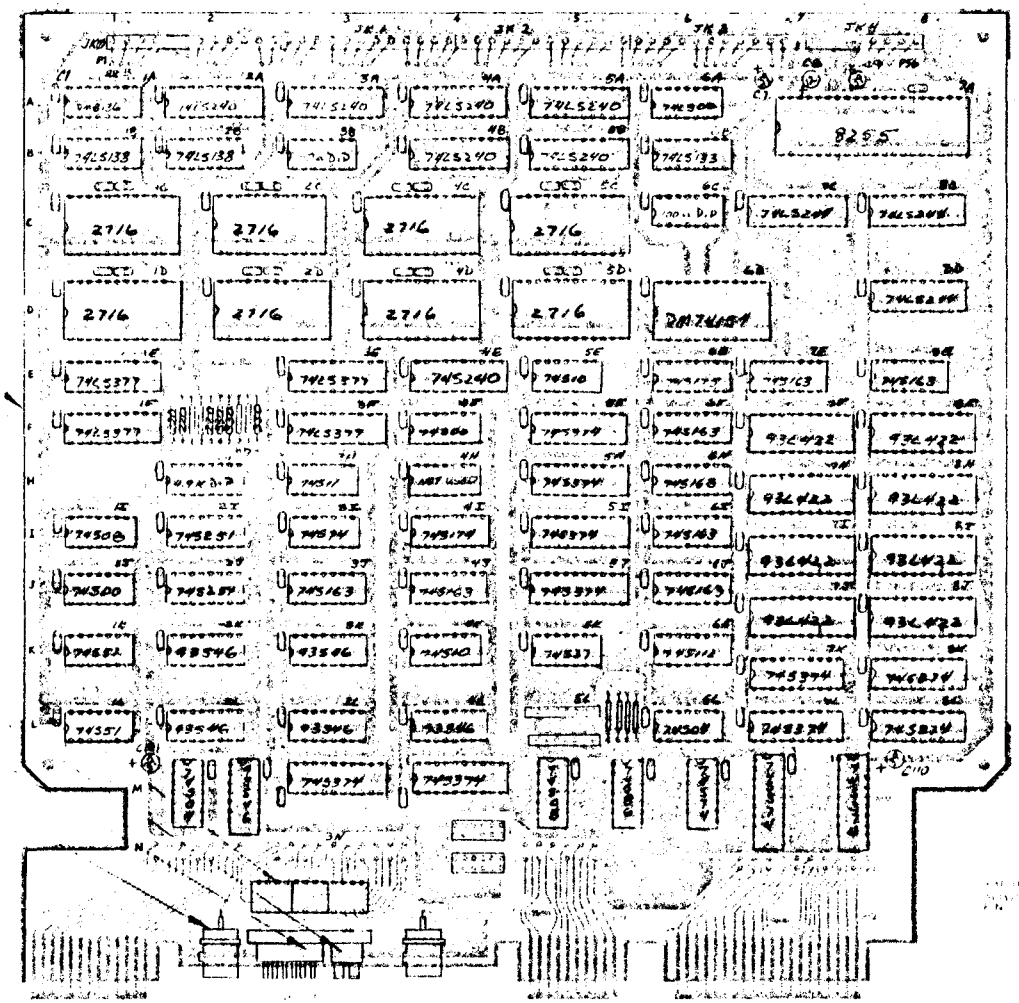
MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001113 | REV D | SHT 4

0001113 SHT 4


DATA PROBE
-002
ADDRESS PROBE
-002
S240
S240
U1
S374
R2
330
R5
1K
330
1K
.1uF
.1uF
+5V
GND
BCS
BAC(L)
ACS
BAC(L)
EE
E1 E3
E2 E3
J1-
J2-
J5
J5-
UD0
UD1
UD2
UD3
UD4
UD5
UD6
UD7
UDC
Q0
Q1
A10
A11
A12
A13
A14
A15
N1
N2
R3
R4
1. SOCKETED USING 720AG-20
B
CORRECT I.C. DESIG.
LTR
DESCRIPTION
DATE
BY
REVISION CHART
STEP ENGINEERING
SCHEMATIC, DATA/ADDRESS PROBE
SHEET 1 OF 1
SIZE B
REV A
000110
1110



NOTES, UNLESS OTHERWISE SPECIFIED:

1. SOLDER BNC TABS & TABS BETWEEN NOTCHES ON GND PAD. SOLDER WIRE FROM BNC LUG TO PCB FEEDTHRU
2. SOCKET I.C.'S - 4A, 5A, 8A, 7B, 6E, 7E, 8E, 3J, 4J, 5L, 5M, 1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D, 7F, 8F, 7I, 8I, 7J, 8J

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: 1/32" DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°					
	B	VERSION MULTIWIRE	MW		12/1/79
	A	BASE RELEASE	MW		
	LTR	DESCRIPTION	BY	APP	DATE
		REVISIONS			

STEP ENGINEERING				NEXT ASSY	USED ON
	MATERIAL	DRAWN MW	DATE 4-26-79	TITLE ASSEMBLY DWG PCB, TRACE	
DO NOT SCALE DRAWING	FINISH ~	APPR	DATE	SCALE 1:1	SIZE C
				DWG NO 0001093	REV A
					SHT 1 of 2

ITEM	QTY	PART NUMBER	DESCRIPTION
1	1	000109E	P.C. BOARD
2	REF	000 1099	SCHEMATIC
3			
4			
5			
6	2	SN 74S00	I.C. 4F, 4J
7	1	LS X	6A
8	2	S04	6L, 1A1
9	2	S08	1I, 5A1
10	2	S10	5E, 4K
11	1	S11	3N
12	1	S37	7K
13	2	S51	1K, 1L
14	2	S74	3I, 7M
15	1	S86	6M
16	1	S112	6K
17	1	LS133	6B
18	2	LS138	1B, 2B
19	1	154	6D
20	8	S163	6F, 7E, 8E, 6N, 6I, 6J, 3J, 4J
21	1	S174	4I
22	1	S175	6E
23	6	LS240	2A, 3A, 4A, 5A, 4B, 5B,
24	3	LS244	7C, 8C, 8D
25	2	S251	2I, 2J
26	12	S 374	5F, 5H, 5I, 5J, 7K, 8K, 7L, 8L, 3M, 4M, 8M, 9M
27	4	SN74LS377	I.C. 1E, 3E, 1F, 3F
28	1	145240	4E
29			
30			

ITEM	QTY	PART NUMBER	DESCRIPTION
31	1	DM8136	I.C. 1A
32	1	8255A	8A & 7B
33	8	2716	1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D
34	8	93L422	7F, 8F, 7K, 8K, 7I, 8I, 7J, 8J
35	6	93S46	2K, 3K, 2L, 3L, 4L, 2M
36	2	4114R-001-101	3B, 6C 100-Ω R. PACK
37	1	4116R-002-472	I.C. 2H 4.7K R PACK
38	2	PE 2 - 63	DELAY LINE 5LA, 5LB
39	3	RC07GF221J	RESISTOR, ¼W, 5% 220Ω, RA, RB, RE
40	3	RC07GF331J	330Ω, RF, RH, RK
41	1	RC07GF102J	1K, VHW
42			
43	1	196D126X9020AA1	CAPACITOR, 12 μF C8
44	4	196D396X9010AA1	CAPACITOR, 39 μF C7, 9, 101, 110
45	105	CY20C104M	CAPACITOR, .1 μF C1-C6, C100-C100, C102-C109
46	2	1094-U	CONNECTOR, BNC T6D, TD
47	1	D125P100 230-480	CONNECTOR, 1T, 2T
48	4	09-52-3121	CONNECTOR, JK0, JK1, JK2, JK3
49	1	01-70-0160	SWITCH, MOLEX 5A-5F
50	1	01-71-0102	SWITCH, MOLEX 5H, 5J
51	1	09-52-3031	CONNECTOR JK4
52	3	CA-08BE-10R0C3-0A	SOCKET, RIGHT ANGLE
53	12	720AG20	I.C. SOCKETS FOR 4A, 5A
54			8A & 7B, 6E, 7E, 8E, 3J, 4J, 5H, 5M
55	8	CA24CS2-750	24 PIN I.C. SOCKETS FOR
56			1C, 2C, 4C, 5C, 1D, 2D, 4D, 5D
57	8	CA22CS2-750	22 PIN I.C. SOCKETS FOR
58			7F, 8F, 7H, 8H, 7I, 8I, 7J, 8J
59			
60			

C7
C1
C3

STEP ENGINEERING

SCALE: —	APPROVED BY:	DRAWN BY: [illegible]
DATE 3-15-1979		REVISED

BILL OF MATERIAL

0001098	REV A	DRAWING NUMBER SHT 2 OF 2

COMMENTS		TOTAL COST	UNIT COST	ITEM	-60	-50	4Y	3Y	2Y	1Y	PART NUMBER	PART NAME	REF. DESIGNATION	[illegible]	DESCRIPTION	
				1			1	0	1	1	0001082	PC BOARD			[illegible]	
				2			1	1	1	1		INTEGRATED CIRCUIT	F1	[illegible]	QUAD 2 INPUT NAND GATE	
REF DES'G C2 REFERS TO REV B PCB [illegible]				3			4	4	4	4			A6, B1, B3, C	74LS00	QUAD 2 INPUT NAND GATE	
				4			1	1	1	1			P1	74LS05	HEX INVERTERS	
				5			1	1	1	1			P3	74LS08	QUAD 2 INPUT POS. AND GATE	
				6			1	1	1	1			A7	74LS13	DUAL 4 INPUT POS NAND SCHMITT TRIG.	
				7			1	1	1	1			L1	74S30	8 INPUT POS. NAND GATE	
				8			2	2	2	2			A1, D1	74LS30	8 INPUT POS. NAND GATE	
				9			2	2	2	2			R1, S2, B8	74S32	QUAD 2 INPUT POS OR GATE	
				10			6	6	6	6			B2, H2, N2, J2, K5, L2	74S86	QUAD EXCLUSIVE OR	
				11			2	2	2	2			E2, K2	74128	50 OHM LINE DRIVER	
				12			1	1	1	1			J1	74S133	13 INPUT POS NAND GATE	
				13			1	1	1	1			A2	74LS138	3 TO 8 LINE DECODER	
				14			1	1	1	1			B6	74LS139	2 TO 4 LINE DECODER	
ON -20 VERSION REF DES'G N3, N4, P2 APPLY				15			9	9	12	9			A3, A4, A5, A8, B4, B5, D2, E3, E4	74LS240	OCTAL TRISTATE BUFFER	
				16			9	9	9	9			C3, C4, C5, C6, D3, D4, D5, D6	74LS244	OCTAL BUFFER	
				17			3	3	3	3			E1, H1, K1	74LS373	OCTAL LATCH	
				18			1	1	1	1		INTEGRATED CIRCUIT	B7	74S257	QUAD MULTIPLEXER	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	D	USED PART W27 FOR DCO # [illegible]	[illegible]	[illegible]	[illegible]	
	E	ADDED [illegible] PER ECO # [illegible]	[illegible]			
0001080	D	ADD -40 VERSION	[illegible]			
0001080	C	ADD -30 VERSION	[illegible]			
0001080	B	ADD -20 VERSION				
0001079	A	PRIMARY RELEASE				

DASH NO.	NUMBER	QTY			DATE
	NEXT ASSEMBLY		DRAWN	E. GOOD	4/9/79
			CHECKED	[illegible]	[illegible]
			ENGINEER	[illegible]	[illegible]
			MANUFACTURING		
			QUALITY ASSURANCE		

LIST OF MATERIAL [redacted]

MEM 128 [illegible]

D

4

ITEM	QUANTITY PER ASSEMBLY -60	-50	4Y	3Y	2Y	1Y	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE	COMMENTS	TOTAL COST	UNIT COST
19			0	0	0	32		INTEGRATED CIRCUIT	E5,E6,E7,E8 F2,F3,F4,F5	2147-3	4096 x 1 BIT STATIC RAM, 55ns				
—			0	0	32	0			H4,H5,H6,H7 J3,J4,J5,J6	2141-3	INTEL 4096 x 1 BIT STATIC RAM, 150ns				
—			0	32	0	0			K4,K5,K6,K7 L3,L4,L5,L6	FAIRCHILD 93471	4096 x 1 STATIC RAM 50NS				
—			32	0	0	0		INTEGRATED CIRCUIT	M3,M4,M5,M6 N3,N4,N5,N6	INTEL D2147H-1	4096 x 1 STATIC RAM 35NS				
20			5	5	5	5		RESISTOR	R2,8,9,10,11	RC07GF103K	10K, 5%, 1/4W				
21			4	4	4	4		RESISTOR	R13,14,15,16	RC07GF510M	51Ω, 5%, 1/4W				
22			10	10	10	10		RESISTOR	R1,3,4,5,6,7 12,17,18,19,20	RC07GF102K	1KΩ, 5%, 1/4W		R20 IS PRESENT ON REVC AND HIGHER PC.B.		
23													SEE VERSION CHART		
~~24~~			—	~~8~~	~~8~~	~~8~~		~~RESISTOR NETWORK~~	~~RN2 THRU RN 9~~	~~764-3-R 150 SCHEMATRONIX~~	~~150Ω SIP 4 RESISTORS~~		~~100Ω RESISTORS PN 7943-R100 MANSFIELD~~		
25			4	4	4	4		RESISTOR NETWORK	RN 10 THRU RN 13	764-3-R 330/330 SCHEMATRONIX	220/330 LOW PROFILE SIP, 6 CONDO				
26			1	1	1	1		CAPACITOR	C1	CK06BX391K	390PF, 10%				
27			62	62	62	62		CAPACITOR		CY20C104P	.1μF				
28			2	2	2	2		CAPACITOR	C2 C3	1960396 X 9010KA1	39μF, 10V				
29			3	3	0	3		INTEGRATED CIRCUIT	M2, N2, P2	74S240	OCTAL TRI-STATE BUFFER		ON -20 VERSION: M2, N2, P2 REPLACED WITH ITEM 15		
30			1	1	1	1		CONNECTOR	P2	CA-034 SERIES 230-AM	(CIRCUIT ASSEMBLIES)				
31			1	1	1	1		CONNECTOR	JKΦ	09-52-3081	(MOLEX)				
32			3	3	3	3		CONNECTOR		DIP-SP100-230-030	(MADE BY CUTTING DIP)				
33			1	1	1	1		SIL SOCKET	S1	CA-K38 10RAC3-01					

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN — DATE

CHECKED

ENGINEER

MANUFACTURING

QUALITY ASSURANCE

LIST OF MATERIAL

MEM128 PCB

MODEL

B | 600-1099 | D

CODE

SHEET 2 OF 4

COMMENTS		TOTAL COST	UNIT COST	ITEM	-60	-50	4Y	3Y	2Y	1Y	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				34			59	59	59	59		IC SOCKET		720-AG20	AUGUT (20 AW)	
				35			2	2	2	2		INTEGATED CKT	N1, M1	74LS374	8 BIT REGISTER	
				36			2	2	2	2		EXTRACTOR		S-200	SCANBE	
				37			4	4	4	4		CONNECTOR		09.52.3121	MOLEX	
				38			2	2	2	2		BNC RECEPT		MIL# UG1094	AMPHENOL	
				39			1	1	1	1		6 POS. SW		01-70-0106	MOLEX	
ON REV A PCB USE 761-1-R2K ... EVLS OR HIGHER - SEE ITEM 3				40			0	0	0	0		INTEGRATED CKT	C2	SEE COMMENT	RES. PACK	
				41			1	1	1	1	0001079				SCHEMATIC (REF)	
CAN USE FAB DWG ... 0001032 WITH CORRECT ARTWORK				42			0	1	0	0	0001101	PC BOARD			FABRICATION DWG AND ARTWORK	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

MEM 128 PCB

B [illegible]

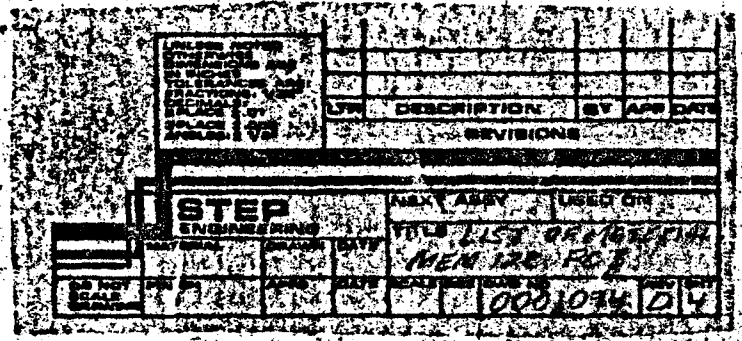
MODEL

CODE SHEET 2

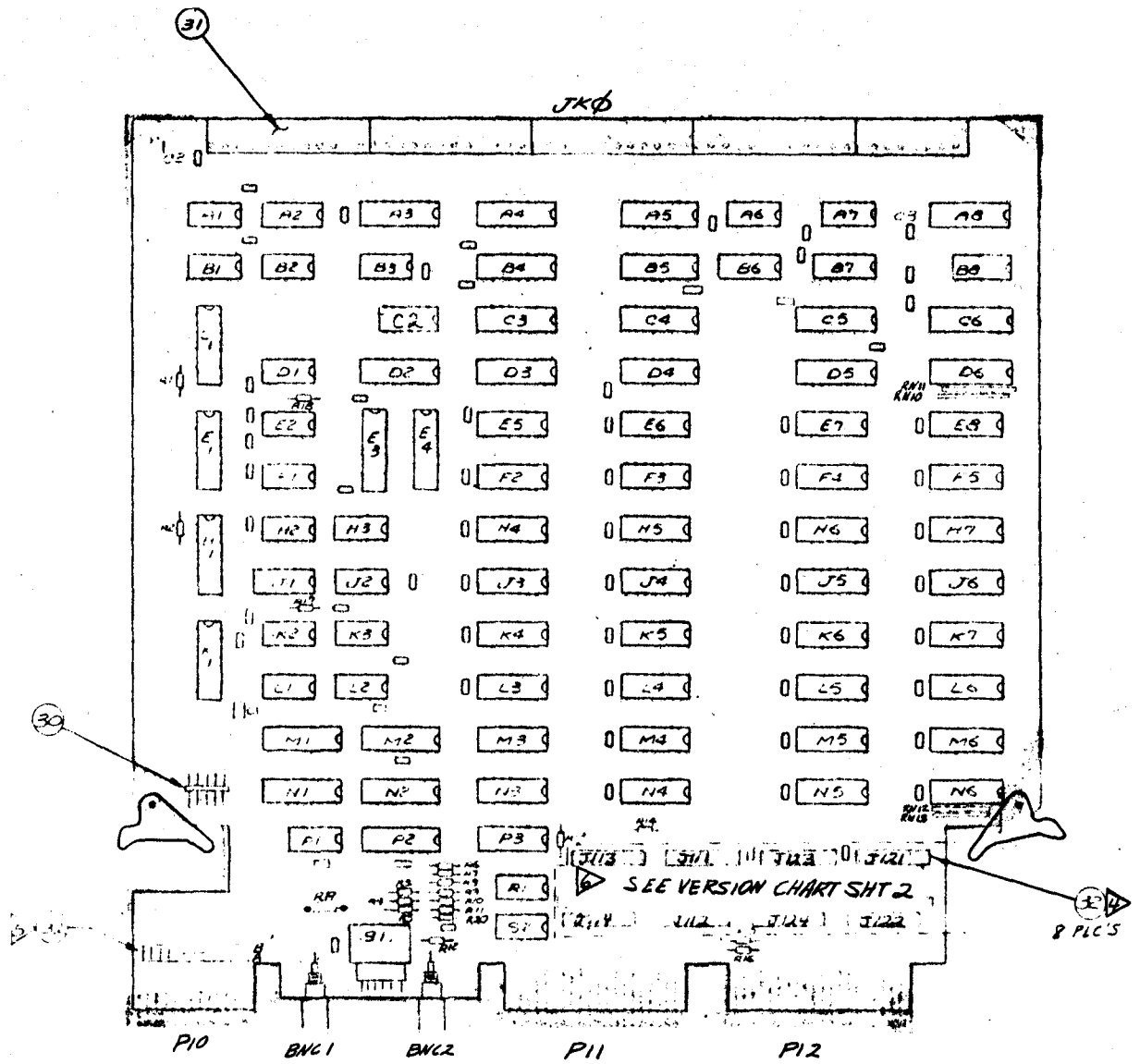
COMMENT	ITEM	QUANTITY PER ASSEMBLY X8	X7	X6	X5	X4	X3	X2	X1	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION
X=1,2,3,4	23				0	0	0	0	8		RESISTOR PACK	RN2 THRU RN9	78+3-R51	51 OHM SIP RES NET (4)
X=1,2,3,4	23				0	0	0	4	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74LS245	OCTAL BUS TRANCEIVER
X=1,2,3,4	23				0	0	4	0	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74LS374	OCTAL D TYPE FLIP FLOP
X=1,2,3,4	23				4	4	0	0	0		INTEGRATED CIRCUIT	XU1, XU2, XU3, XU4	74LS373	OCTAL D LATCH

VERSION CHART

MEMORY	INTERFACE TYPE X1	X2	X3	X4	X5	X6
1Y	RESISTIVE 70NS ACCESS	BIDIR 83 NS ACCESS	REGISTER 92 NS ACCESS	LATCH 88 NS ACCESS	BUFFER 83 NS ACCESS	
2Y	RESISTIVE 150 NS ACCESS	BIDIR 195 NS ACCESS	REGISTER 205 NS ACCESS	LATCH 199 NS ACCESS	BUFFER 195 NS ACCESS	
3Y	RESISTIVE 70 NS ACCESS	BIDIR 82 NS ACCESS	REGISTER 92 NS ACCESS	LATCH 88 NS ACCESS	BUFFER 83 NS ACCESS	
4Y	RESISTIVE 50 NS ACCESS	BIDIR 62 NS ACCESS	REGISTER 72 NS ACCESS	LATCH 68 NS ACCESS	BUFFER 63 NS ACCESS	
5Y	RESISTIVE	BIDIR	REGISTER	LATCH	BUFFER	
6Y	RESISTIVE	BIDIR	REGISTER	LATCH	BUFFER	



1094 SHT 4



VERSION CHART ▷4				
WSH NO	PART NAME	PART NUMBER	LIST OF MATERIALS	WIRE LIST (SEE SHT 2)
-10	MEMBRA	0001080-10	0001094-10	
-20	MEMBRB	0001080-20	0001094-20	
-30	MEMBRA	0001080-30	0001094-30	
-40	MEMBRB	0001080-40	0001094-40	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS TO BE .1uF except C1, C2, C3 (C1, C2, C3 ARE CAPS STUFF A PART REVISION LOST DWG)
2. .1uF CAPACITORS ON CHIPS M2, N-2 AND P-2 ARE LOCATED ON SOLDER SIDE OF BOARD (ALL A PC BOARD ONLY)
3. RN10, RN-11, RN-12, AND RN-13 LOCATED ON SOLDER SIDE OF BOARD (A' & A" BOARD ONLY)

▷4 SEE VERSION CHART FOR LIST OF MATERIALS AND APPLICABLE WIRE LIST.

▷5 WIREWRAP BETWEEN CORRESPONDING POSTS ON ROW A AND ROW B (13 WIREWRAPS) ON REV B PC BOARD

	1	0	0	0	0001080-40	MEMBRB	SEE SCMS VERSION	4
	0	1	0	0	0001080-30	MEMBRA	FOR 4 70 NS VERSION	3
	0	0	1	0	0001080-20	MEMBRB	STD 100NS VERSION	2
	0	0	0	1	0001080-10	MEMBRA	STD 70 NS VERSION	1
	-50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL: X ± 1 ANGLES ±1°; .XX ± .030 ±1°; .XXX ± .010
HOLE SIZE: .0 to .598 ± .006; .600 to .998 ± .004; 1.000 & OVER ± .005
BEND RADIUS
FINISH

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN E Good 11/7/78
CHECKED J.M.N. 12/4/78
ENGINEER J.M. 12/8/78
MANUFACTURING
QUALITY ASSUR

STEP ENGINEERING

TITLE ASSEMBLY
A/M M 12" PC BOARD

SCALE 1 to 1 | SIZE C | PART NUMBER 0001080 | REV D

CODE | SHEET / OF

WIRE LIST CHARTS

TO	FROM	NAME J121	J123	J111	J113
3	4	R0	R10	R20	R30
7	8	R2	R12	R22	R32
11	12	R4	R14	R24	R34
15	16	R6	R16	R26	R36

J111 TO J111
J113 TO J113
J121 TO J121
J123 TO J123

TO	FROM	NAME J122	J124	J112	J114
5	6	D1	D9	D17	D25
9	10	D3	D11	D19	D27
13	14	D5	D13	D21	D29
17	18	D7	D15	D23	D31

J112 TO J112
J114 TO J114
J122 TO J122
J124 TO J124

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
6	4	D0	D8	D16	D24
5	3	R1	R11	R21	R31
10	8	D2	D10	D18	D26
9	7	R3	R13	R23	R33
14	12	D4	D12	D20	D28
13	11	R5	R15	R25	R35
18	16	D6	D14	D22	D30
17	15	R7	R17	R27	R37

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

VERSION X1

RESISTIVE TERMINATION

TO	FROM	NAME J121	J123	J111	J113
5	6	R1	R11	R21	R31
7	8	R2	R12	R22	R32
13	14	R5	R15	R25	R35
15	16	R6	R16	R26	R36
1	2	$\overline{E0}$	$\overline{E1}$	$\overline{E2}$	$\overline{E3}$

J114 TO J111
J115 TO J113
J121 TO J121
J123 TO J123

TO	FROM	NAME J122	J124	J112	J114
1	4	D0	D8	D16	D24
7	10	D3	D11	D19	D27
9	12	D4	D12	D20	D28
15	18	D7	D15	D23	D31
2	17	UL	UL	UL	UL

J112 TO J112
J114 TO J114
J122 TO J122
J124 TO J124

TO	FROM	NAME J121 J122	J123 J124	J111 J112	J113 J114
3	3	R0	R10	R20	R30
4	6	D1	D9	D17	D25
10	8	D2	D10	D18	D26
9	5	R3	R13	R23	R33
11	11	R4	R14	R24	R34
12	14	D5	D13	D21	D29
18	16	D6	D14	D22	D30
17	13	R7	R17	R27	R37

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

VERSION X3, X4, X5

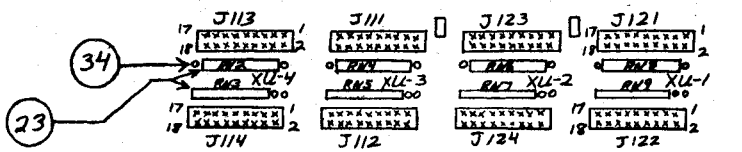
X3: TRISTATE REGISTER OUTPUT
X4: TRISTATE LATCHING OUTPUT
X5: TRISTATE BUFFER OUTPUT

TO	FROM	NAME J121 J123	J123 J124	J111 J112	J113 J114
1	1	$\overline{E0}$	$\overline{E1}$	$\overline{E2}$	$\overline{E3}$
2	2	$\overline{WOB}$	$\overline{WO1}$	$\overline{WOB}$	$\overline{WO1}$

J111 TO J112
J113 TO J114
J121 TO J122
J123 TO J124

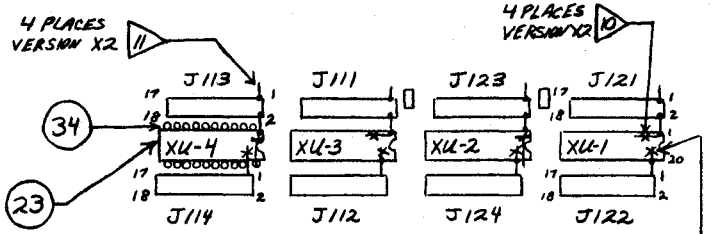
VERSION X2

BIDIRECTIONAL TRISTATE DRIVER



RN2 THRU RN9
5132 SIP RESISTORS

VERSION X1



XU-1 THRU XU-4: ON-X2 VER 74LS245
ON-X3 VER 74S374
ON-X4 VER 74S373
ON-X5 VER 74S373

VERSIONS -X2, -X3, -X4 - X5

NOTES (CONTINUED)

11 ON VERSION X2 WIRE THE FOLLOWING:
$\overline{WOB}$: S2 PIN 11 TO J112 & J122 PIN 2; $\overline{WO1}$: S2 PIN 8 TO J114 & J124 PIN 2
$\overline{E0}$: R1 PIN 6 TO J121 PIN 1 ; $\overline{E2}$: R1 PIN 3 TO J111 PIN 1
$\overline{E1}$: R1 PIN 11 TO J123 PIN 1 ; $\overline{E3}$: R1 PIN 8 TO J113 PIN 1
THE ABOVE APPLIES TO REV A&B PC BOARDS ONLY

ON REV C AND HIGHER PC BOARDS
CUT UL LINE IN FOUR PLACES: JUST PRIOR TO J112, J114, J122, J124 PIN 2. WIRE $\overline{WOB}$: S2 PIN 11 TO J112 & J122 PIN 2; $\overline{WO1}$: S2 PIN 8 TO J114 & J124 PIN 2. NOTE: TO CHANGE TO VERSIONS -X3, -X4, -X5 THE ORIGINAL CONNECTIONS MUST BE RESTORED

NOTES (CONTINUED)

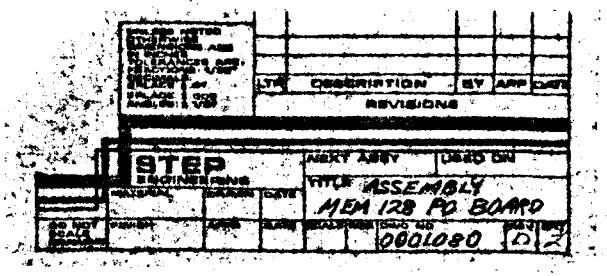
6 WIRE WRAP PER WIRE LISTCHART AND ASSEMBLE PER DIAGRAM SHOWN FOR EACH VERSION

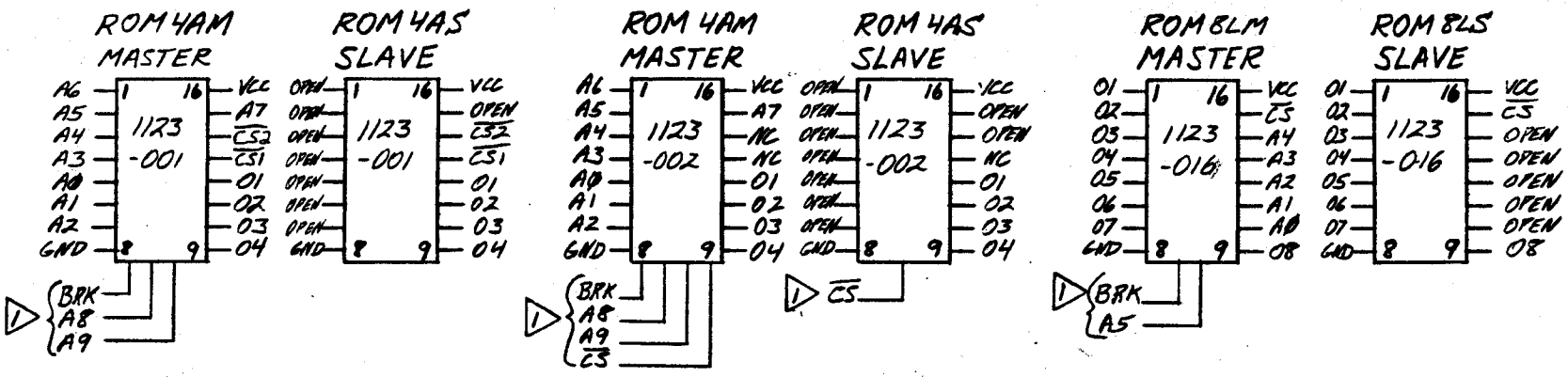
7 ASSEMBLY VERSION SHOWN AS DASM XY (0001080-XY) WHERE "X" SPECIFIES MEMORY TYPE AND "Y" SPECIFIES INTERFACE CONFIGURATION

8 CUT TRACE FROM UL TO J112, J114, J122, J124 PIN 1 ON COMPONENT SIDE OF BOARD AS SHOWN FOR VERSIONS X2, X3, X4, X5. ON VERSIONS X3, X4, X5 ONLY, WIRE UL TO PIN 2 OF J112, J114, J122, J124 THIS APPLIES TO REV A&B PC BOARDS ONLY

9 WIRE PIN 2 TO PIN 17 ON VERSIONS X3, X4 ONLY

10 ON VERSION X2 CUT TRACES FROM: $\overline{E0}$ TO XU-1 PIN 1 (SOLDER SIDE), $\overline{E1}$ TO XU-2 PIN 1 (COMPONENT SIDE), $\overline{E2}$ TO XU-3 PIN 1 (SOLDER SIDE), $\overline{E3}$ TO XU-4 PIN 1 (COMPONENT SIDE). THIS APPLIES TO REV A&B PC BOARDS ONLY





VER 001 VER 002 VER 003 VER 004 VER 005 VER 006

NOTES: UNLESS OTHERWISE SPECIFIED

1. AUXILLARY INPUTS FROM EXTERNAL PROBES
2. PINS MARKED "OPEN" HAVE LEADS CUT ON ROM SIM CABLE OR AT HEADER PINS. PINS MARKED "NC" HAVE INPUTS TO THE ROM SIM MODULE WHICH ARE NOT USED.
3. ITEMS WITH "*" IN FRONT OF MODEL DESIGNATION ARE DESIGNED FOR USE WITH MEM 128
4. THE FOLLOWING VERSIONS ARE NOT ASSIGNED:
   017, 018, 035, 036, 037, 038, 039, 040, 041, 042, 045, 046, 047, 048, 061, 062, 063, 064, 065, 066, 073, 074, 075, 076, 077, 078, H9, H0, 111, 112, 113, 114, 127, 128, 129, 130, 131, 132
5. PART NUMBER TO BE DWG # - VER #
6. NUMBER SHOWN WITHIN DWG, "1123-XXX", TO BE INCLUDED IN LABEL

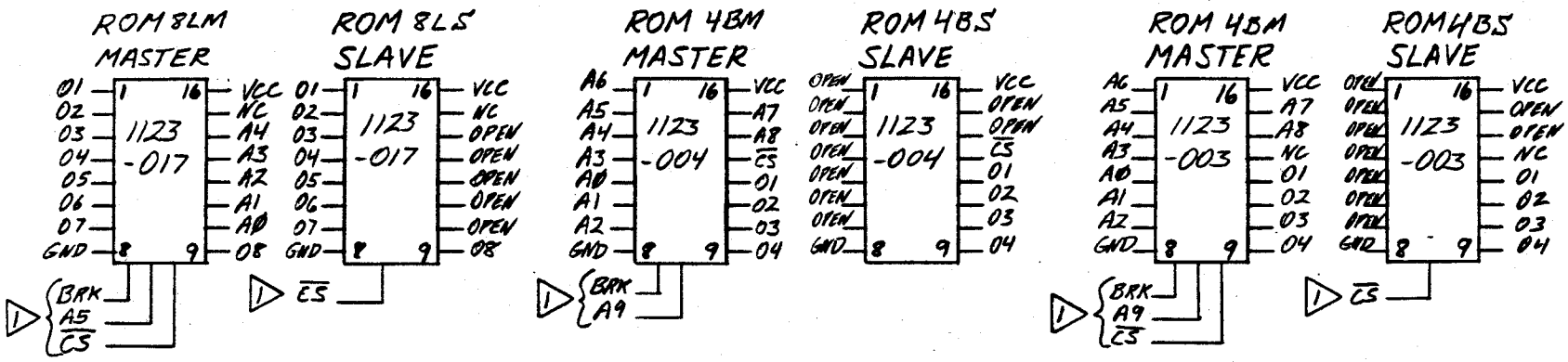
LTR	DESCRIPTION	BY	APP	DATE
D	NOTES 5, 6 + RELEASED TO 31			3/6/87
C	REVISED + RELEASED			12/8/86

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

STEP ENGINEERING

MATERIAL	DRAWN	DATE	NEXT ASSY 0001123	USED ON
	SMW	12/8/86	TITLE LABLES, ROM SIMULATOR ASSY	
DO NOT SCALE DRAWING	FINISH	APPR	DATE	SCALE / SIZE / DWG NO 0001028 REV SHT 1/23



VER 007 VER 008 VER 009 VER 010 VER 011 VER 012

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 USED ON

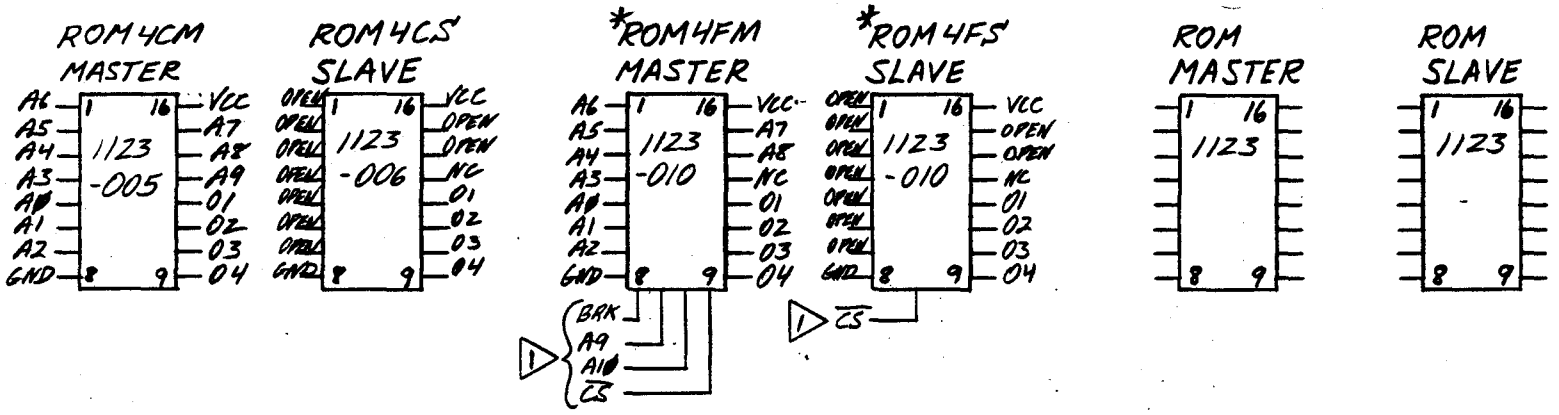
TITLE CABLES, ROM SIMULATOR ASSY

MATERIAL DRAWN DATE 12/19/

FINISH APPR DATE

DO NOT SCALE DRAWING

SCALE SIZE DWG NO 0001128 REV SHT 2



VER Ø13 VER Ø14 VER Ø15 VER Ø16 VER Ø17 VER Ø18

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: 2 PLACE ±.01 3 PLACE ±.005 ANGLES: ±1°

STEP ENGINEERING

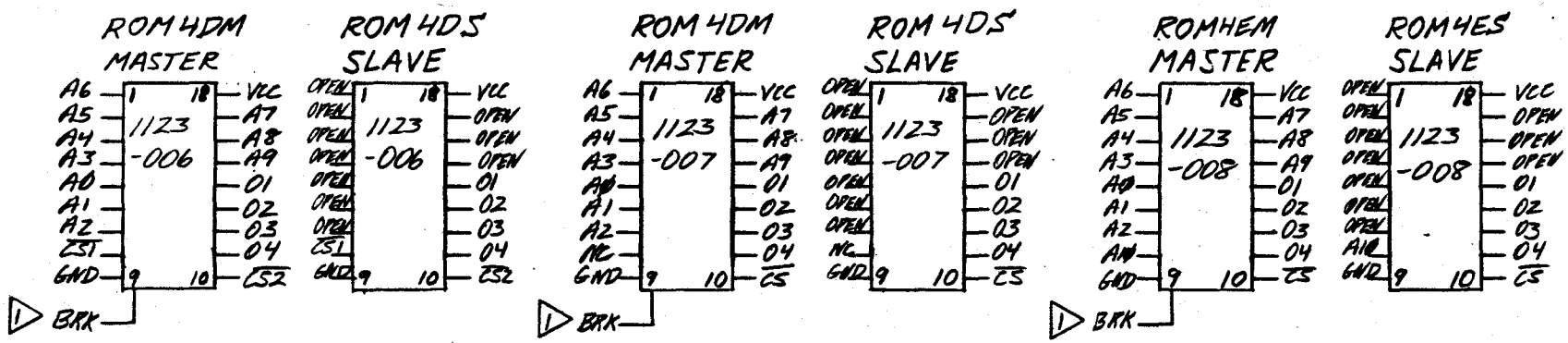
NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001028 | REV | SHT 3



VER Ø19 VER Ø20 VER Ø21 VER Ø22 VER Ø23 VER Ø24

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 USED ON

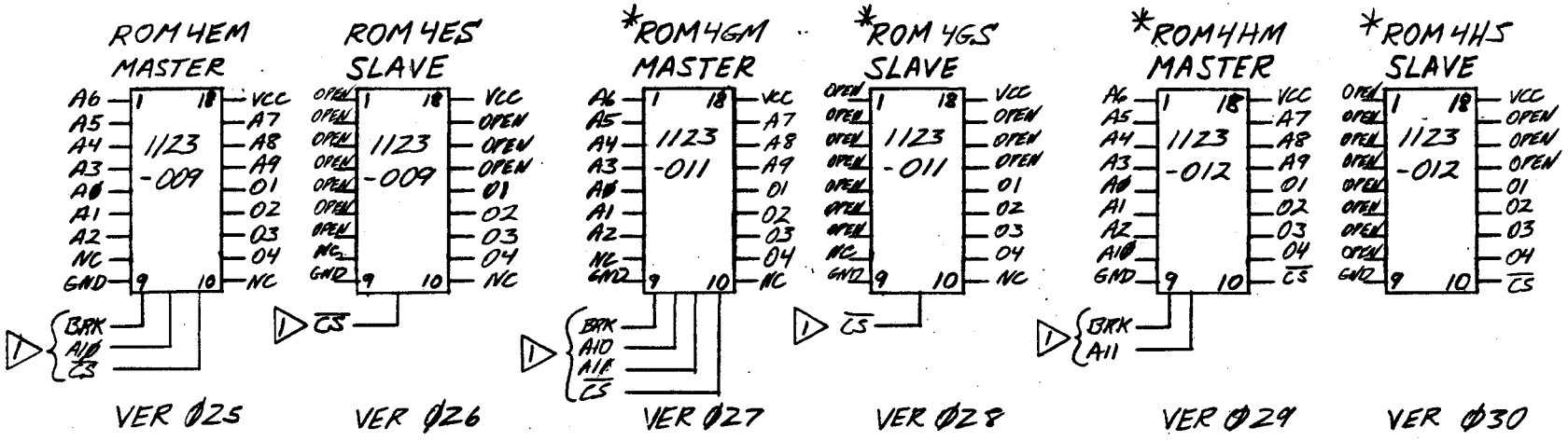
TITLE CABLES, ROM SIMULATOR ASSY

MATERIAL DRAWN DATE

FINISH APPR DATE

DO NOT SCALE DRAWING

SCALE SIZE DWG NO 0001028 REV SHT 4



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

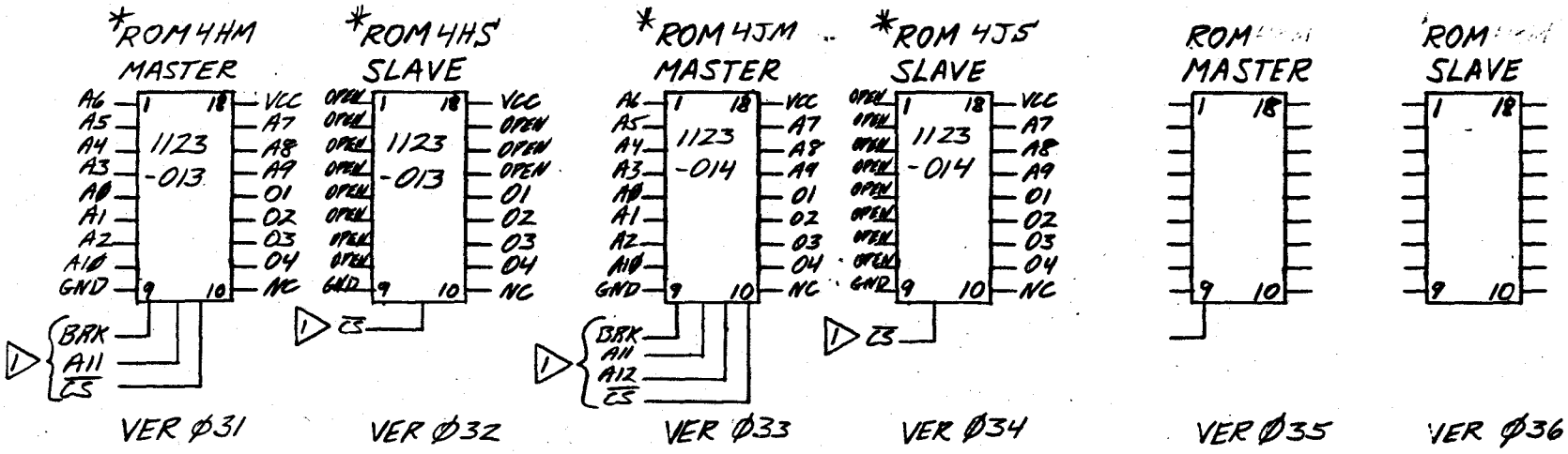
TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE

FINISH | APPR | DATE

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001028 | REV | SHT 5



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

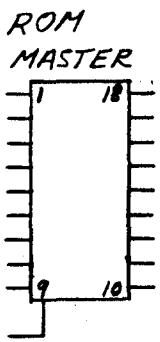
NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

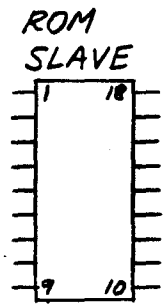
MATERIAL | DRAWN | DATE

FINISH | APPR | DATE | SCALE | SIZE | DWG NO 0001028 | REV | SHT 6

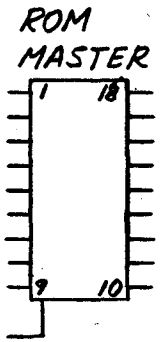
DO NOT SCALE DRAWING



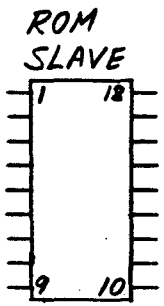
VER Ø37



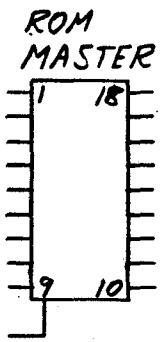
VER Ø38



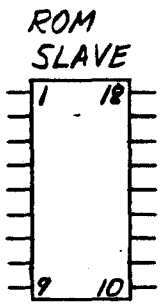
VER Ø39



VER Ø40



VER Ø41



VER Ø42

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: 2 PLACE ±.01 3 PLACE ±.005 ANGLES: ± 1/2°

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

STEP ENGINEERING

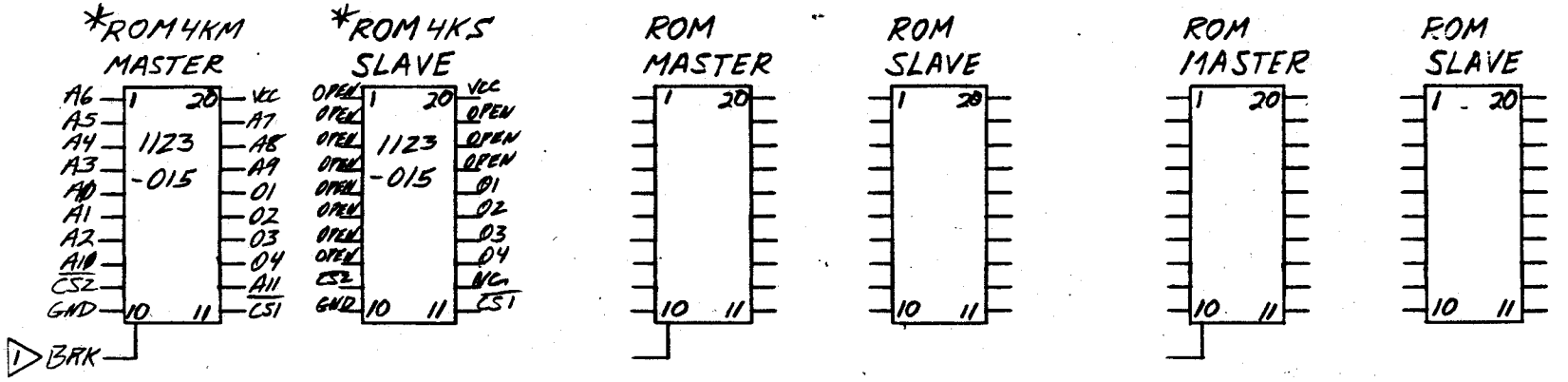
MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

DO NOT SCALE DRAWING

NEXT ASSY 0001123 USED ON

TITLE CABLES, ROM SIMULATOR ASSY

SCALE SIZE DWG NO 0001028 REV SHT 7



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: 3 PLACE ±.01 2 PLACE ±.005 ANGLES: ± 1/2°

STEP ENGINEERING

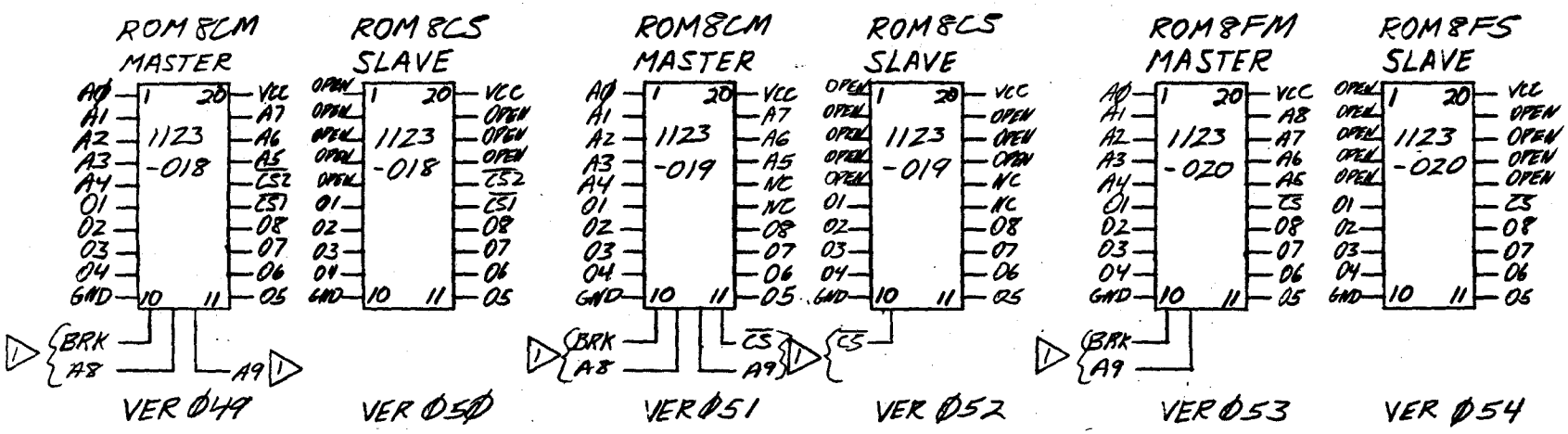
MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

DO NOT SCALE DRAWING

NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

SCALE | SIZE | DWG NO 0001028 | REV | SHT 8



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

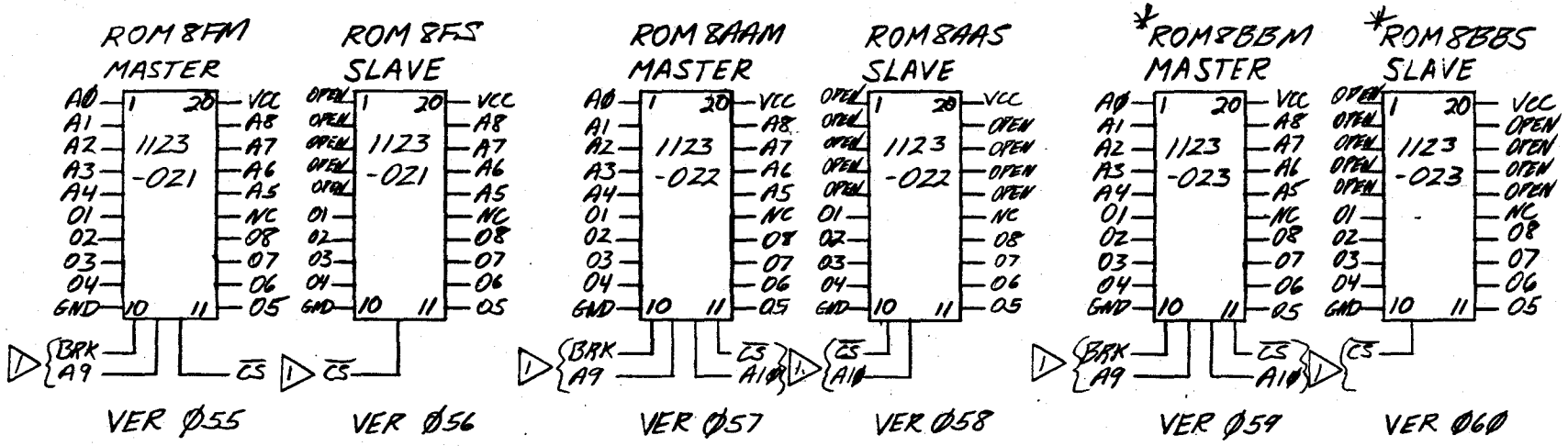
NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE 11/2/84

FINISH | APPR | DATE

DO NOT SCALE DRAWING | SCALE | SIZE | DWG NO 0001128 | REV | SHT 9



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

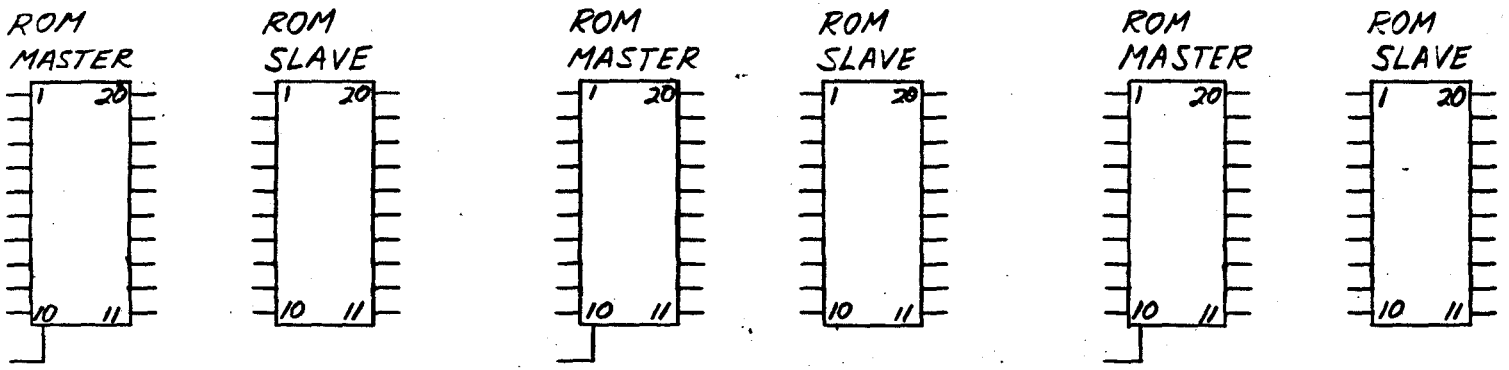
TITLE LABELS, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE

FINISH | APPR | DATE

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001028 | REV | SHT 1Ø



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES
TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: .XX ± .01 .XXX ± .005 ANGLES: ± 1/2°

STEP ENGINEERING

MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

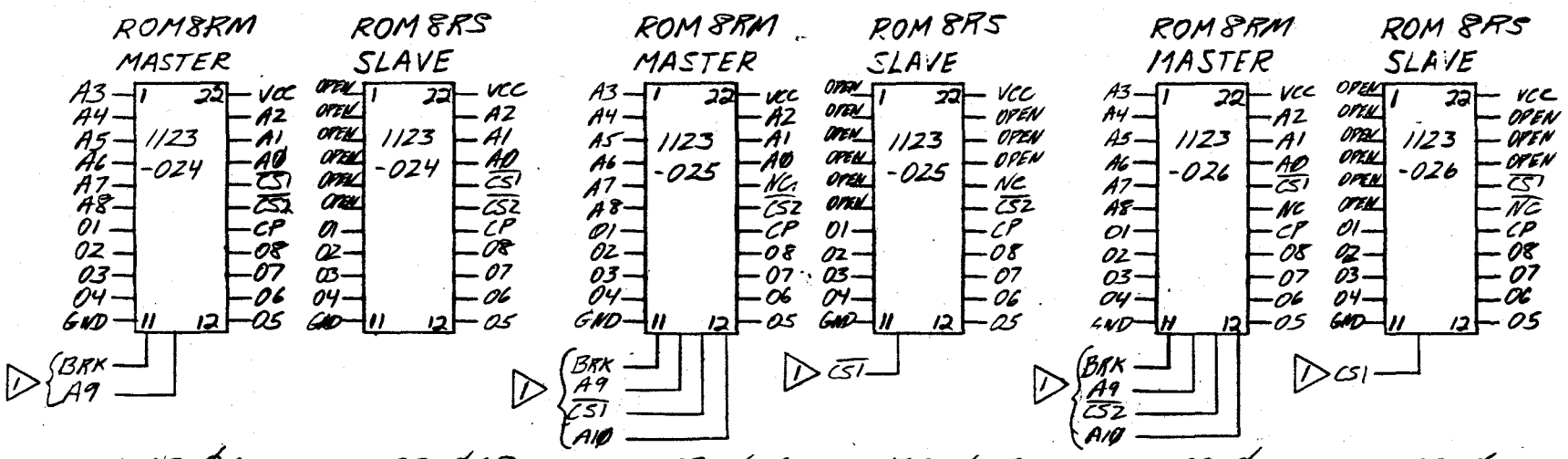
NEXT ASSY 0001123

USED ON

TITLE LABLES, ROM SIMULATOR ASSY

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001128 | REV | SHT 11



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001.23 | USED ON

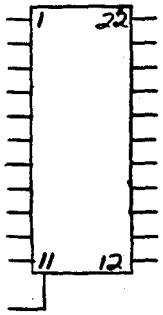
TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN SMW | DATE 12/29/81

FINISH | APPR | DATE

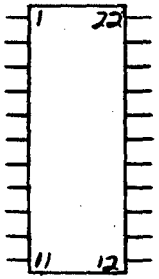
DO NOT SCALE DRAWING | SCALE | SIZE | DWG NO 0001328 | REV | SHT 12

ROM MASTER



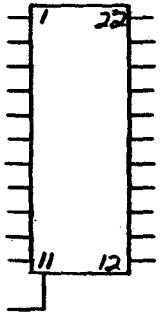
VER Ø73

ROM SLAVE



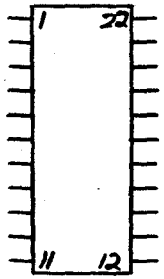
VER Ø74

ROM MASTER



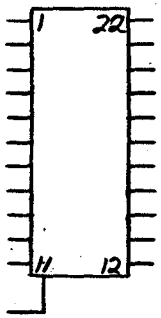
VER Ø75

ROM SLAVE



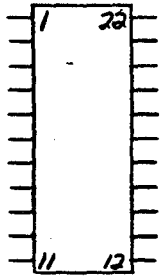
VER Ø76

ROM MASTER



VER Ø77

ROM SLAVE



VER Ø78

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

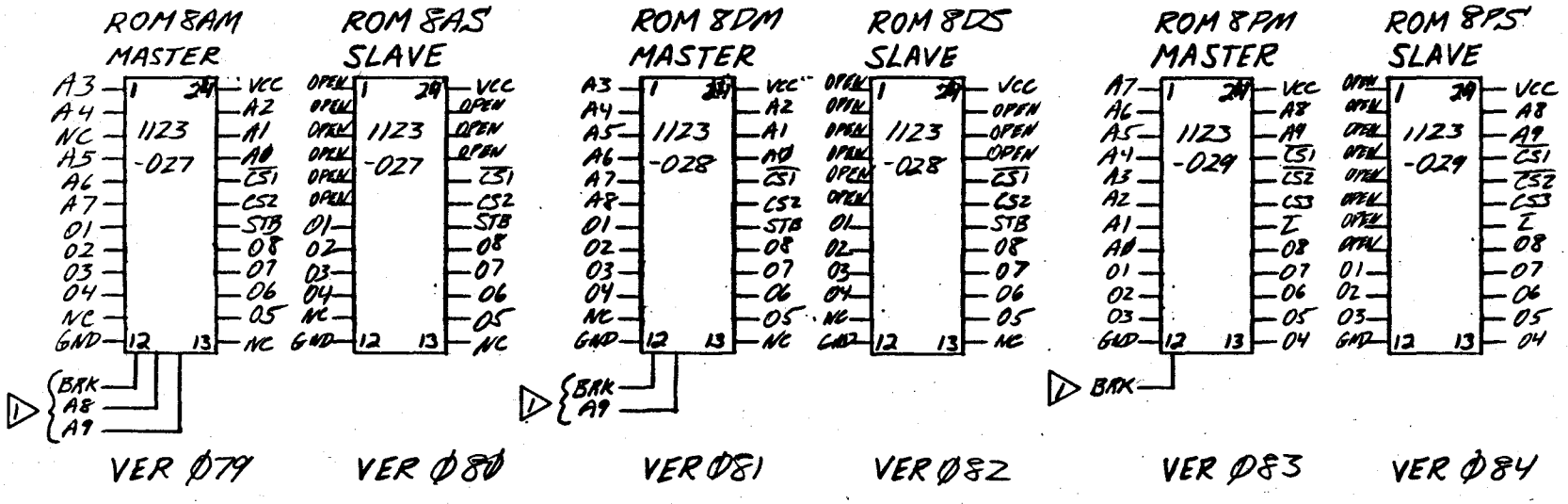
STEP ENGINEERING

NEXT ASSY 000123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE 12/6/79

DO NOT SCALE DRAWING | FINISH | APPR | DATE | SCALE | SIZE | DWG NO 000128 | REV | SHT 13



NOTES : UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

STEP ENGINEERING

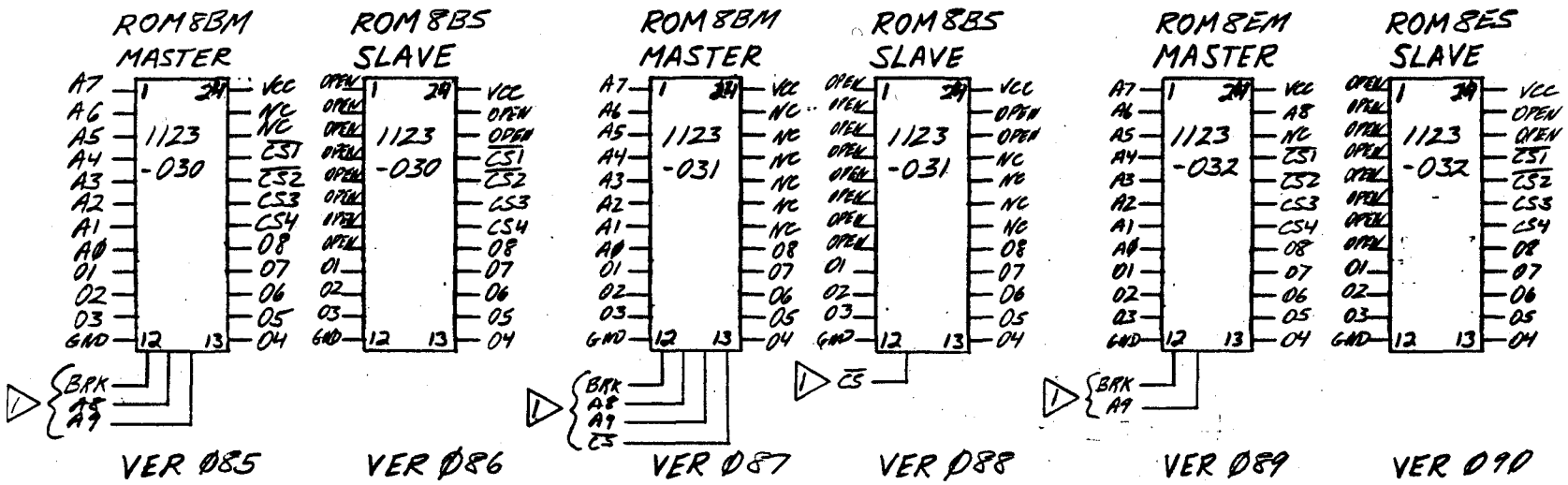
NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL	DRAWN	DATE
FINISH	APPR	DATE

DO NOT SCALE DRAWING

SCALE | SIZE | DWG NO 0001028 | REV | SHT 14



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

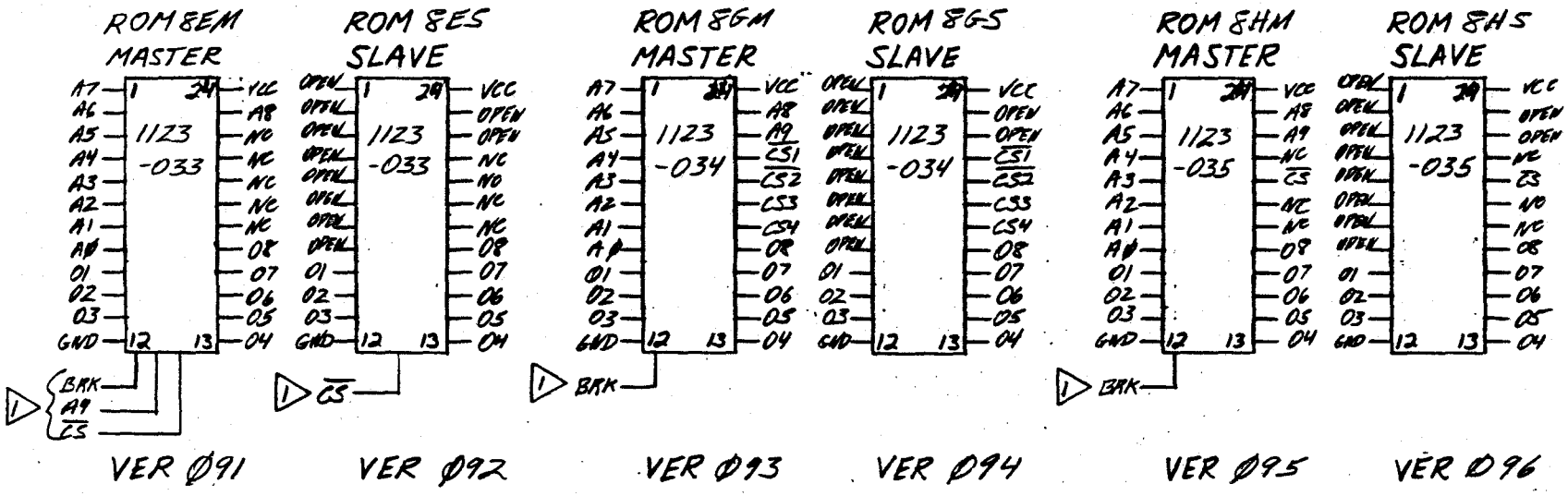
TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE

FINISH | APPR | DATE

DO NOT SCALE DRAWING

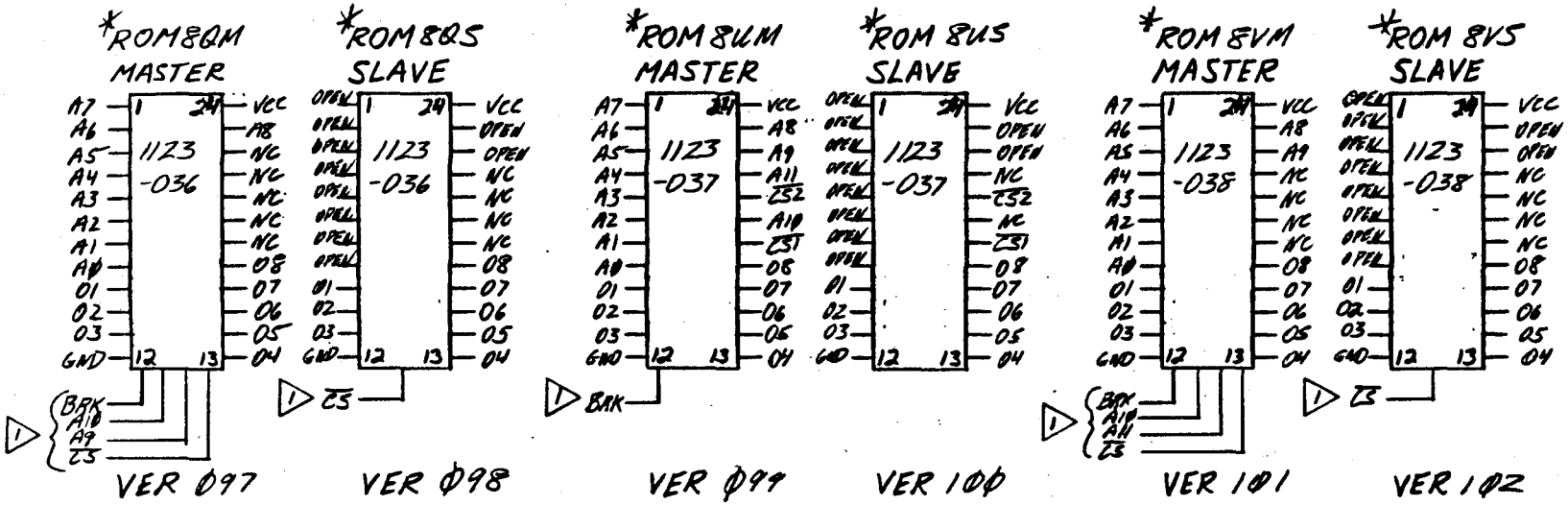
SCALE | SIZE | DWG NO 0001028 | REV | SHT 15



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING	NEXT ASSY 0001123	USED ON	
MATERIAL	DRAWN	DATE	TITLE LABLES, ROM SIMULATOR ASSY
DO NOT SCALE DRAWING	FINISH	APPR	DATE
SCALE	SIZE	DWG NO 0001028	REV / SHT 16



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

REVISIONS

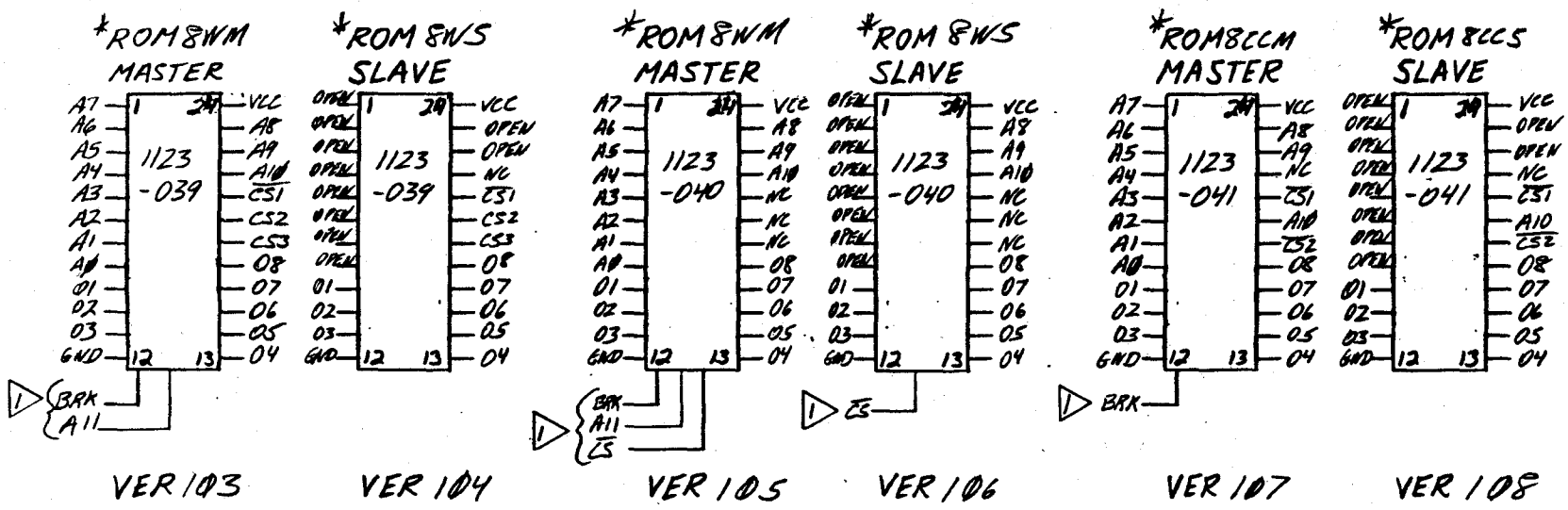
STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE

DO NOT SCALE DRAWING | FINISH | APPD | DATE | SCALE | SIZE | DWG NO 0001028 | REV | SHT 17



NOTES : UNLESS OTHERWISE SPECIFIED

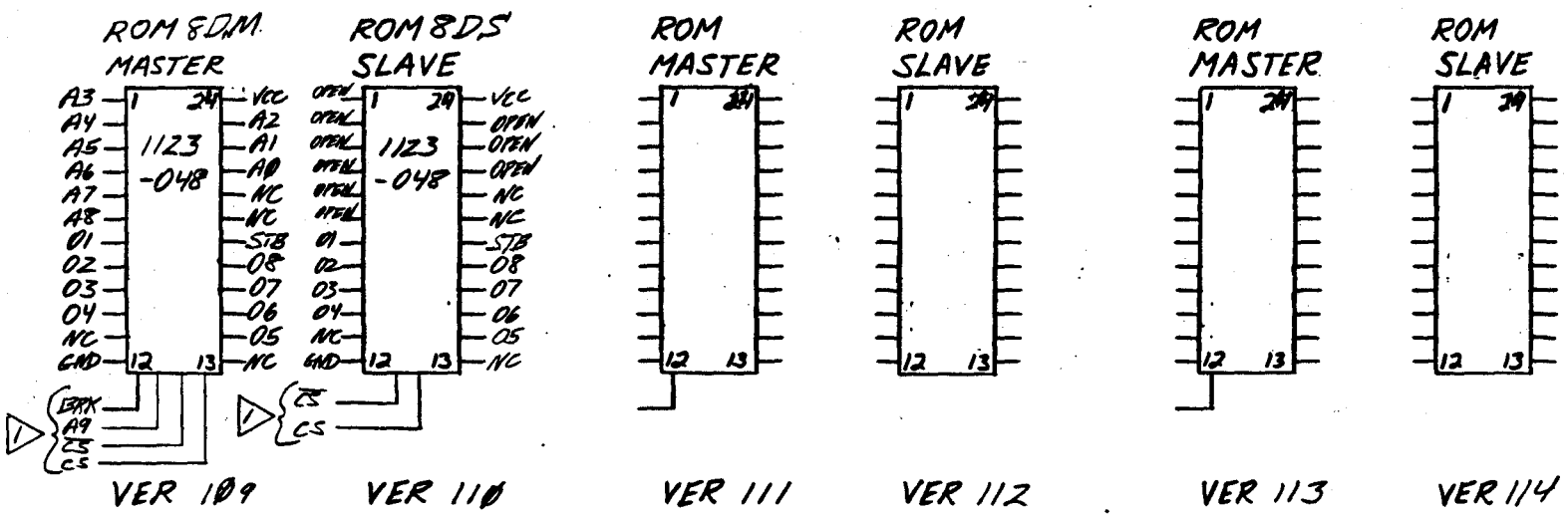
LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 USED ON

TITLE LABLES, ROM SIMULATOR ASSY

DWG NO 0001028 REV SHT 18



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

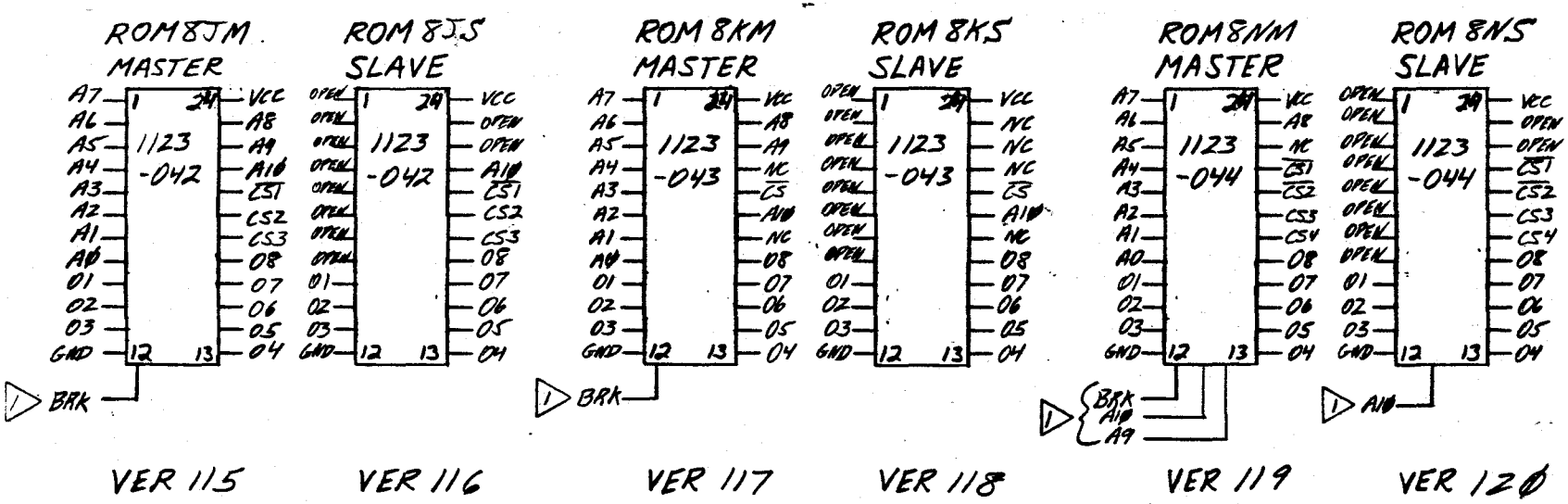
STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

MATERIAL | DRAWN | DATE

DO NOT SCALE DRAWING | FINISH | APPR | DATE | SCALE | SIZE | DWG NO 0001028 | REV | SHT 19



NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	BY	APP	DATE

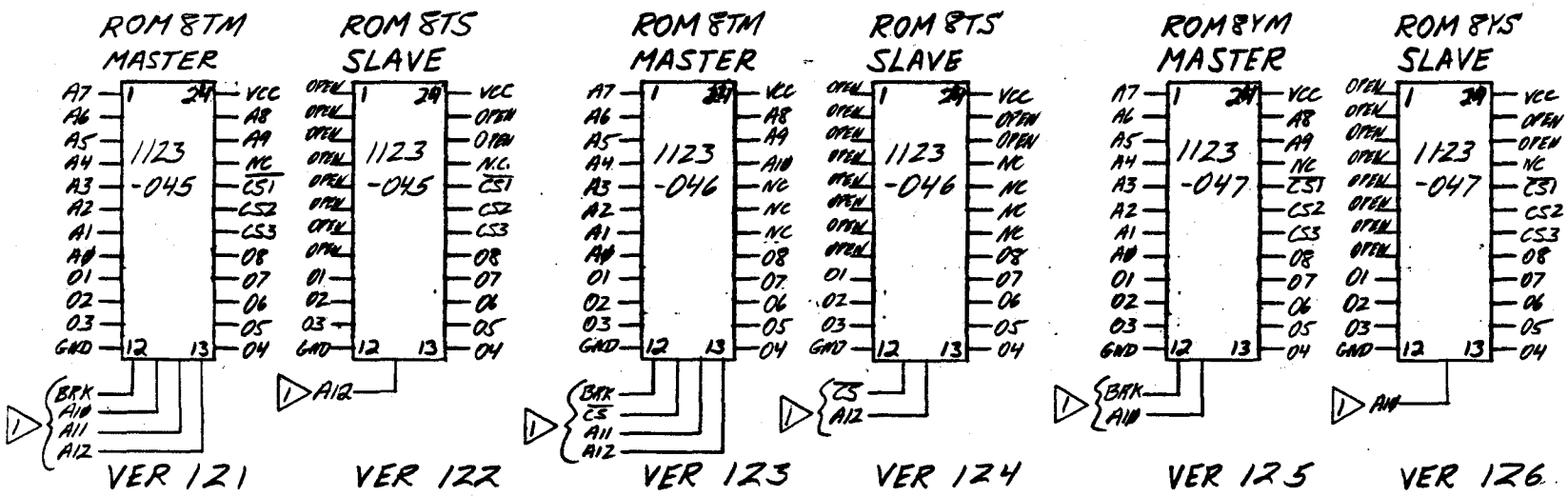
REVISIONS

STEP ENGINEERING

NEXT ASSY 0001123 | USED ON

TITLE LABLES, ROM SIMULATOR ASSY

DWG NO 0001028 | REV | SHT 20



NOTES: UNLESS OTHERWISE SPECIFIED

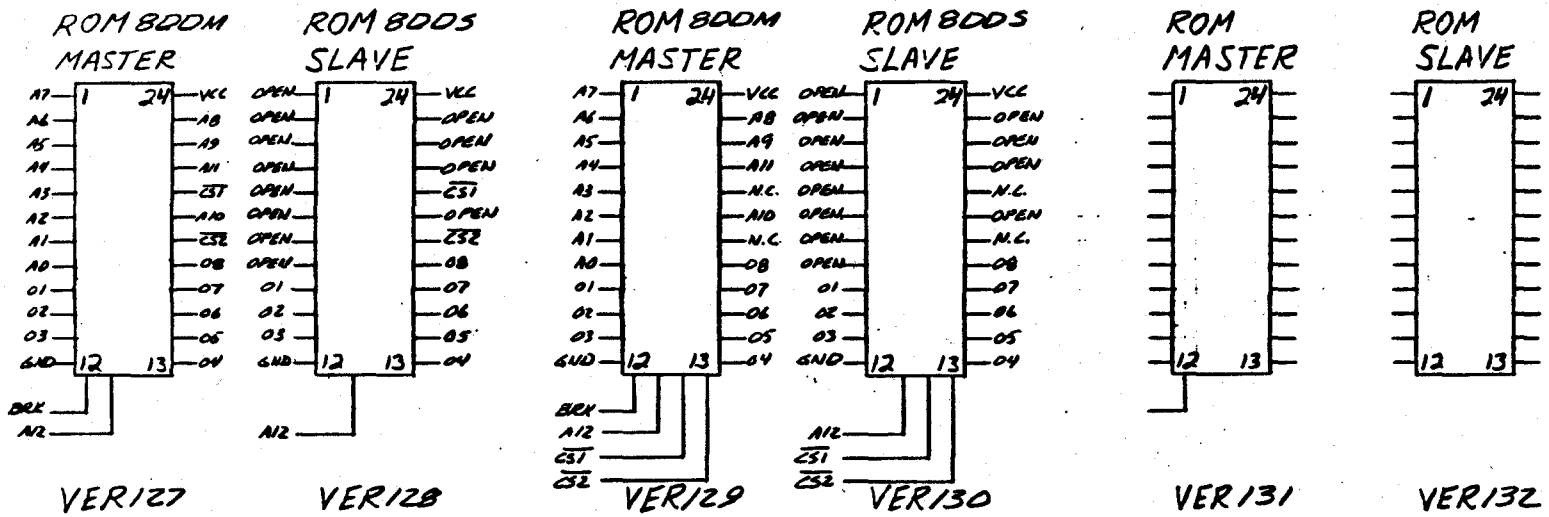
LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS			

STEP ENGINEERING

NEXT ASSY 0001123 USED ON

TITLE LABLES, ROM SIMULATOR ASSY

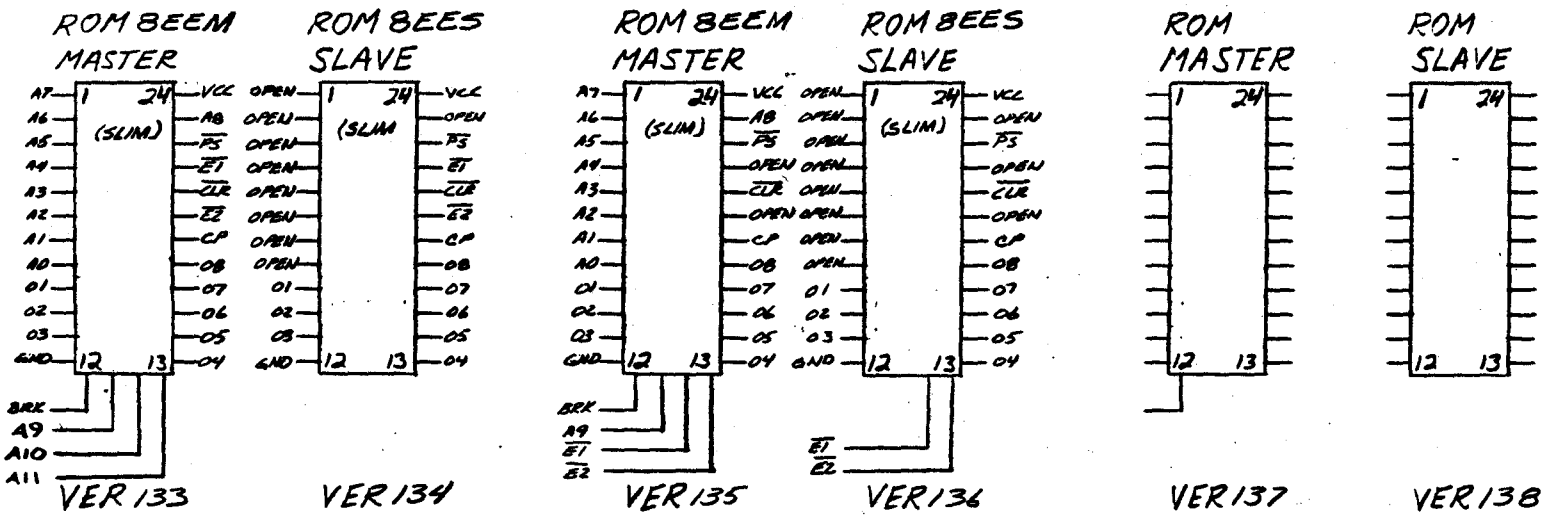
DRWG NO 0001028 REV SHT 21



NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32" DECIMALS: 2 PLACE ±.01 3 PLACE ±.005 ANGLES: ± 1/2°					
	LTR	DESCRIPTION	BY	APP	DATE
	REVISIONS				

STEP ENGINEERING			NEXT ASSY 0001123	USED ON	
	MATERIAL	DRAWN	DATE	TITLE LABLES, ROM SIMULATOR ASSY	
DO NOT SCALE DRAWING	FINISH	APPR	DATE	SCALE / SIZE / DWG NO 0001028	REV / SHT 22



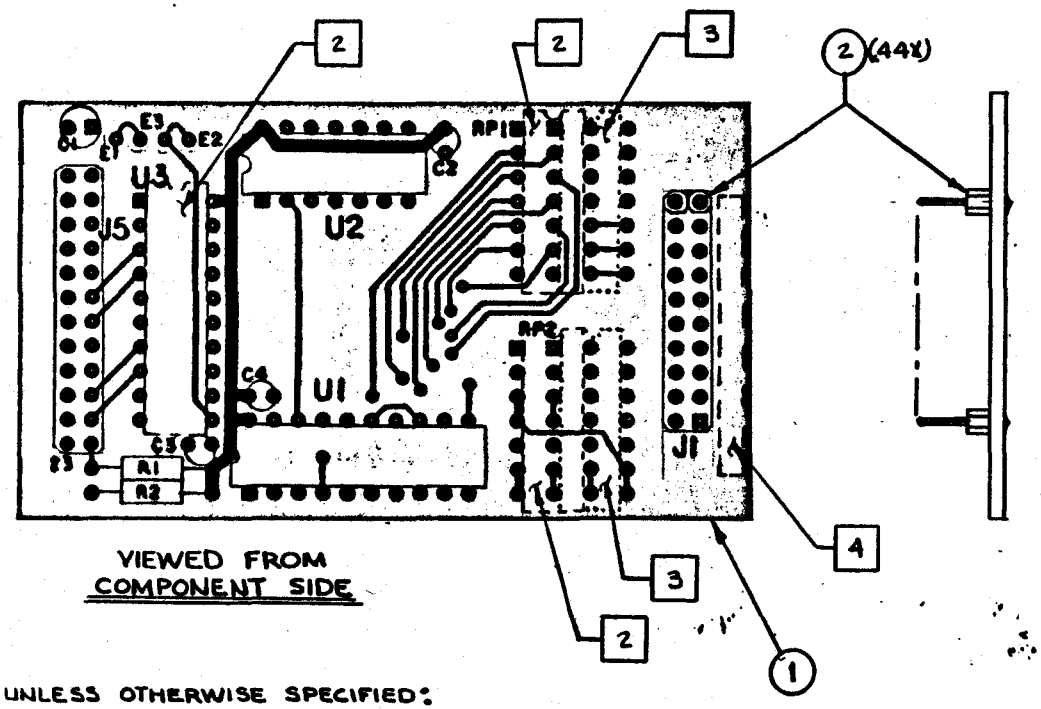
NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: 1/32" DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°	LTR	DESCRIPTION	BY	APP	DATE
		REVISIONS			

STEP ENGINEERING			NEXT ASSY 1001123	USED ON
MATERIAL	DRAWN	DATE	TITLE LABLES, ROM SIMULATOR ASSY	
DO NOT SCALE DRAWING — FINISH	APPR	DATE	SCALE / SIZE / DWG NO 0001028	REV / SHT 23

LIST OF MATERIALS

ITEM NO	PART NUMBER	DESCRIPTION	QTY -01	QTY -02	NOTES
1	0200001-00	PCB, NEW TRACE PR.	1	1	
2	LSG-1FG-10-1	PINS	44	44	J1, J5
3	196D396X9010KA1	39uF CAP.	1	1	C1
4	CY20C104P	.1uf CAP.	1	1	C2-C4
5	RC07GF472J	4.7K RESISTOR	2	2	R1, R2
6	745240	745240 I.C	1	1	U1
7	74S86	74S86 I.C	1	1	U2
8	74S374	74S374 I.C.	1	—	U3
9	4114-R-001-330	RP, 33Ω	1	1	RP1,2



VIEWED FROM COMPONENT SIDE

NOTES; UNLESS OTHERWISE SPECIFIED:

1. ASSEMBLE PER STEP ENGINEERING STANDARDS.
2. FOR DATA PROBE VERSION (-01) INSTALL ALL DASHED COMPONENTS. (SEE LIST OF MATERIAL).
3. FOR ADDRESS PROBE VERSION (-02) INSTALL ALL DOTTED COMPONENTS. (SEE LIST OF MATERIAL).
4. MARK THE PART NUMBER AND APPROPRIATE DASH NUMBER AND REV. LEVEL IN AREA SHOWN.

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: 1/32" DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

LTR	DESCRIPTION	BY	APP	DATE
B	UP-DATE A/W	DA		6-80
A				

REVISIONS

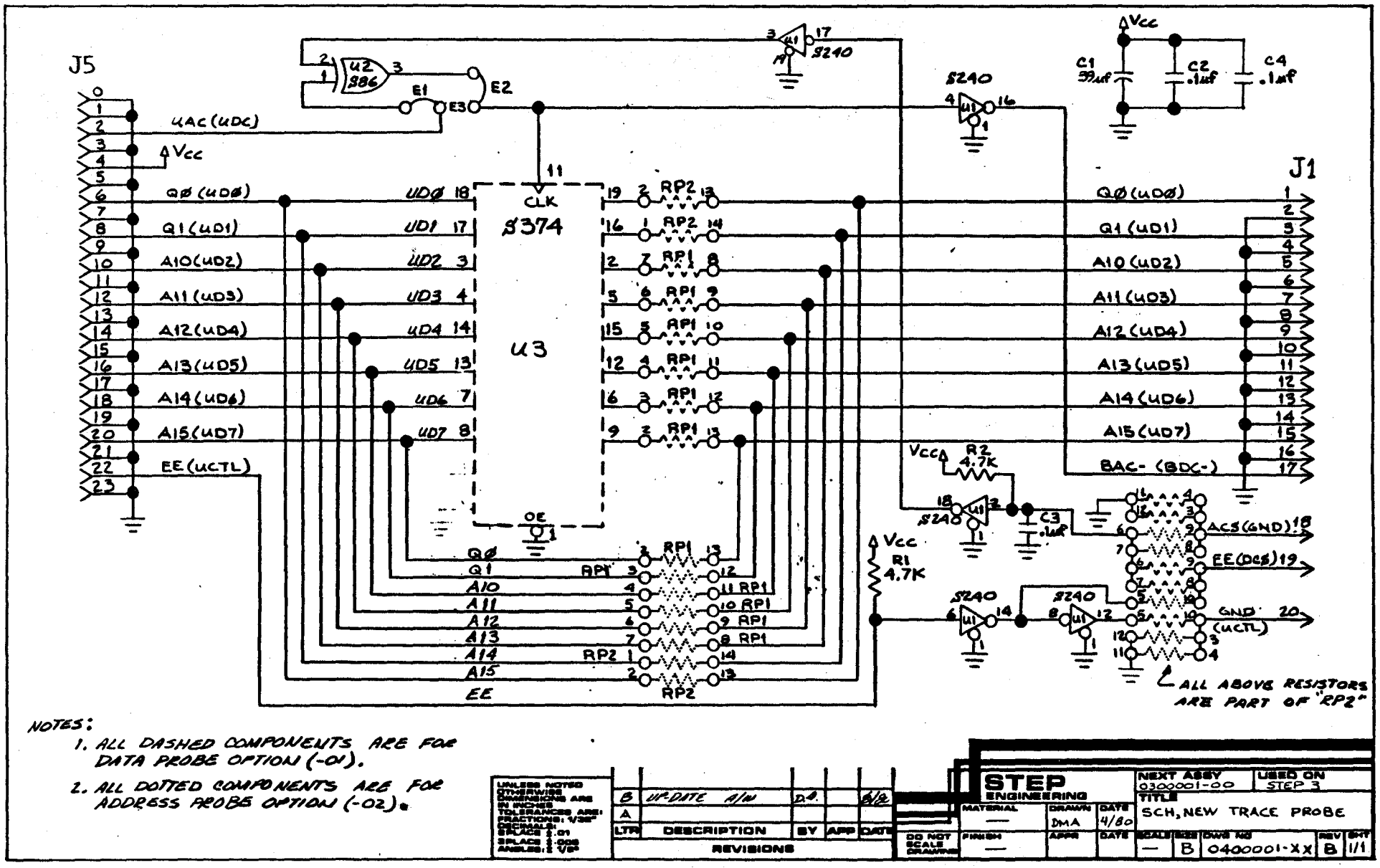
STEP ENGINEERING

NEXT ASSY: NONE | USED ON: STEP 3

TITLE: ASSY, NEW TRACE PROBE

MATERIAL	DRAWN	DATE	SCALE	SIZE	DWG NO	REV	SHT
SEE L/M	DMA	4/80	2/1	B	0300001-XX	B	V1

DO NOT SCALE DRAWING | FINISH: 125 | APPR | DATE



NOTES:

1. ALL DASHED COMPONENTS ARE FOR DATA PROBE OPTION (-01).
2. ALL DOTTED COMPONENTS ARE FOR ADDRESS PROBE OPTION (-02).

LTR	DESCRIPTION	BY	APP	DATE
B	UP-DATE A/W	DA		6/82
A				

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: ±1/32 DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

DO NOT SCALE DRAWING

STEP ENGINEERING

MATERIAL	DRAWN	DATE
—	DMA	4/80
FINISH	APPR	DATE
—		

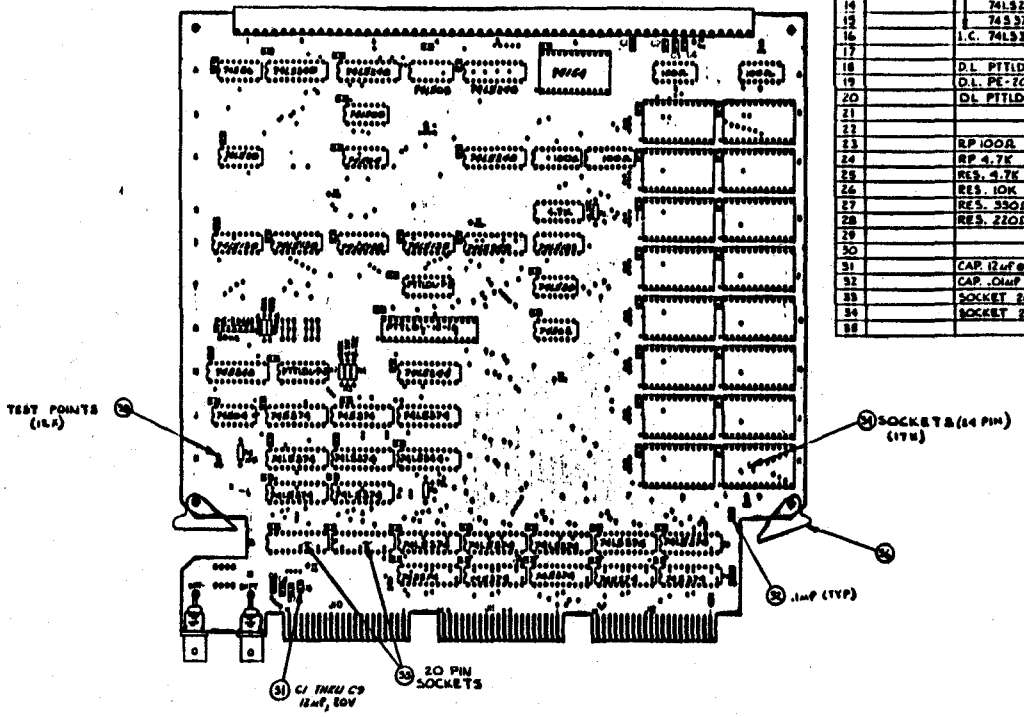
NEXT ASSY 0300001-00 | USED ON STEP 3

TITLE: SCH, NEW TRACE PROBE

SCALE	SIZE	DWG NO	REV	SHT
—	B	0400001-XX	B	1/1

ITEM NO	PART NUMBER	DESCRIPTION	LOCATION/ REMARKS	QTY
1	0300002-00	SELF TEST P.C.B.		1
2		MOLEX CONN.	56 PIN	A/R
3		I.C. 74LS00	3B	1
4		74S02	6G	1
5		74S04	5C, 1J	2
6		74LS08	4A	1
7		74LS20	1C, 6F	2
8		74S86	1A	1
9		74L9135	6E	1
10		74LS138	1E, 2E, 3E, 4E	4
11		74154	6A	1
12		74LS240	2A, 3A, 5A, 5C, 3E	5
13		74S240	1H	1
14		74LS244	4H, 4K	2
15		74S374	2M, 3M, 2J, 3J, 4H, 5H, 6H, 7H, 8H	9
16		I.C. 74LS374	4J, 2K, 3K, 2L, 3L, 5M, 6M, 7M, 8M, 4H	10
17				
18		D.L. PTTLDL-7-2	4F, 2H,	2
19		D.L. PE-70663	1G	1
20		DL PTTLDL-15-16	4G	1
21				
22				
23		RP 100Ω	8A, 9A, 6C, 7C	4
24		RP 4.7K	6D	1
25		RES. 4.7K	R1, R2, R3, R4, R5	5
26		RES. 10K	R6	1
27		RES. 330Ω	R1A	1
28		RES. 220Ω	R1B	1
29				
30				
31		CAP. 12uF @ 20V	C1 THRU C9	9
32		CAP. .01uF	ALL UNMARKED CAPACITORS	53
33		SOCKET 20 PIN	2M, 3M	2
34		SOCKET 24 PIN	8B, 9B, 8C, 9C, 8D, 9D, 8F, 9F, 8G, 9G, 8H, 9H, 8J, 9J, 8K, 9K, 6A	17

ITEM NO	PART NUMBER	DESCRIPTION	LOCATION/ REMARKS	QTY
35		EJECTORS		2
37		BNC	WRT-, DEPT	2
38		TEST POINTS		12
39				
40				
41		3M CABLES		2



NOTES:
1. ASSEMBLE PER STEP ENG. STANDARDS.

LTR	DESCRIPTION	BY	APP	DATE
B	UP-DATE A/W1DOC	DA		

REVISIONS

STEP ENGINEERING

NEXT ASSY | USED ON: STEP 3

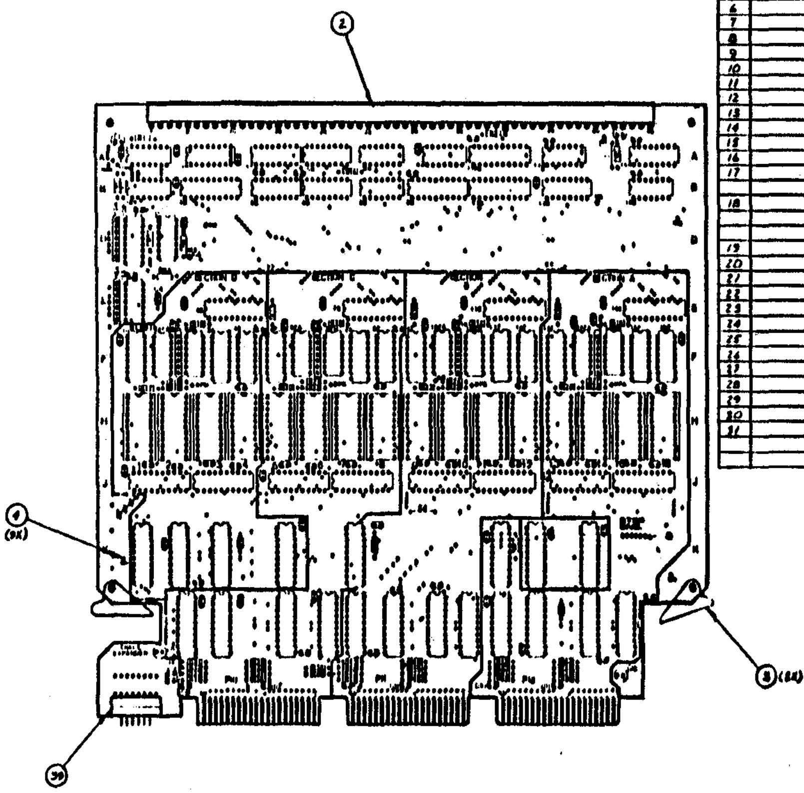
TITLE: ASSY, SELF TEST BD.

MATERIAL | DRAWN | DATE

FINISH | APPR | DATE

DO NOT SCALE DRAWING

SCALE: FULL | SIZE: D | DWG NO: 0300002-00 | REV: B | SHT: 1/1



NOTES: UNLESS OTHERWISE SPECIFIED
1. ASSEMBLE PER STEP ENG STANDARDS.

ITEM NO	PART NUMBER	DESCRIPTION	LOCATION / REMARKS	QTY
1	0200006-00	TRACE EXPANDER		1
2		MOLEX CONN.	56 PINS	A/R
3		EJECTORS		2
4		TEST POINTS		9
5				
6		IC 74LS00	9A, 1B	2
7		74LS04	1A, 13A	2
8		74S08	8A, 15B, 14FC, 10FC, 6FC	5
9		74S11	8B	1
10		74S37	14FA, 10FA, 6FA	3
11		74S112	15A, 13F, 9F, 5F	4
12		74LS138	5A, 6A, 5B, 6B.	4
13		74S163	7F, 8F, 11F, 12F, 15F, 16F	6
14		74S175	13B	1
15		74LS240	8B, 9B, 11B	3
16		74S241	7K, 11K	2
17		74LS244	11A, 7C, 11C, 15C, 3L, 6L, 7L, 10L, 11L, 15L	10
18		74S374	5J, 7J, 9J, 11J, 13J, 15J, 12K, 14K, 3L, 5L, 8L, 9L, 12L, 14L.	14
19				
20		IC DM8136	3A	1
21		IC 93L422	5N THRU 16N	12
22		SOCKETS 22 PIN	5N THRU 16N	12
23				
24		DELAY LINE	6FB, 10FB, 14FB	3
25				
26				
27		CAP. 39μF	C1, C2, C5, C12.	4
28		CAP. .1μF		24
29				
30		RES. 1K 1/4W	R1	1
31		RES. 4.7K	R2, R3, R11, R12, R13, R14, R15, R16, R20, R23, R26, R29, R30, R4	14

ITEM NO	PART NUMBER	DESCRIPTION	LOCATION / REMARKS	QTY
32		RES. 470Ω	R21, R22, R24, R25, R27, R28, R40,	7
33		RES. 330Ω	R32, R34, R36, R38, R39, R42, R44, R46, R48, R50, R52, R54, R56	13
34		RES. 220	R31, R33, R35, R37, R41, R43, R45, R47, R49, R51, R53, R55	12
35				
36				
37				
38				
39		SWITCH 6POS		1
40				

LTR	DESCRIPTION	BY	APP	DATE
B	DCO# 98	DAK		
A	RELEASE	DAK		

REVISIONS

STEP ENGINEERING

NEXT ASSY | USED ON STEP 3

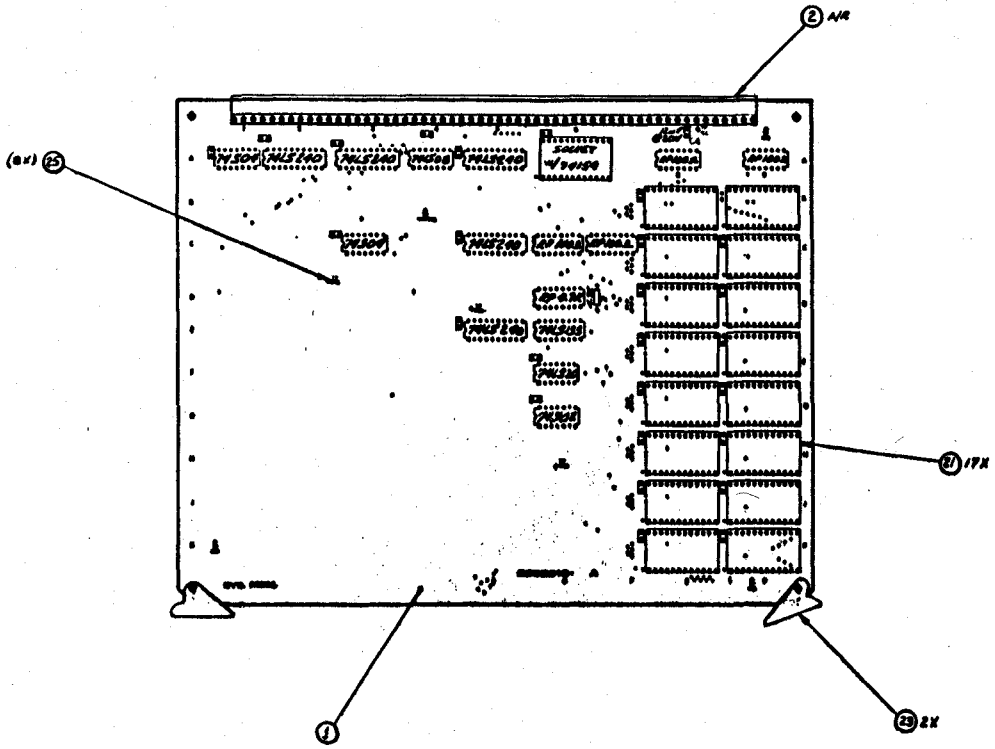
TITLE ASSY, TRACE EXPANDER

MATERIAL — | DRAWN AKAO | DATE 8-80

FINISH — | APPR | DATE

SCALE FULL | SIZE D | DWG NO 0300006-00 | REV V1

DO NOT SCALE DRAWING



ITEM NO	PART NUMBER	DESCRIPTION	LOCATION / REMARKS	QTY
1	0200010-00	SYS. MEM. PCB		1
2		MOLEX CONN	36 PINS	A/R
3				
4		IC. 74S02	6G	1
5		74S04	1A, 3C	2
6		74LS08	4A	1
7		74LS20	6F	1
8		74LS133	6E	1
9		74154	6A	1
10		IC. 74LS240	2A, 3A, 5A, 5C, 5E	5
11				
12		RP 100Ω	8A, 9A, 6C, 7C	4
13		RP 4.7K	6D	1
14		RES. 4.7K	R1	1
15				
16				
17		CAP, 12 uf @ 20V	C4	1
18		CAP. .01uf		27
19				
20				
21		SOCKET 24 PIN	4A, 8B, 9B, 8C, 9C, 8D, 9D, 8F, 9F, 8G, 9G, 8H, 9H, 8J, 9J, 8K, 9K,	17
22				
23		EJECTOR		2
24				
25		TEST POINT		8
26				

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER STEP ENGINEERING STANDARDS.

LTR	DESCRIPTION	BY	APP	DATE
A	RELEASE	DAF		1/31/80

REVISIONS

STEP ENGINEERING

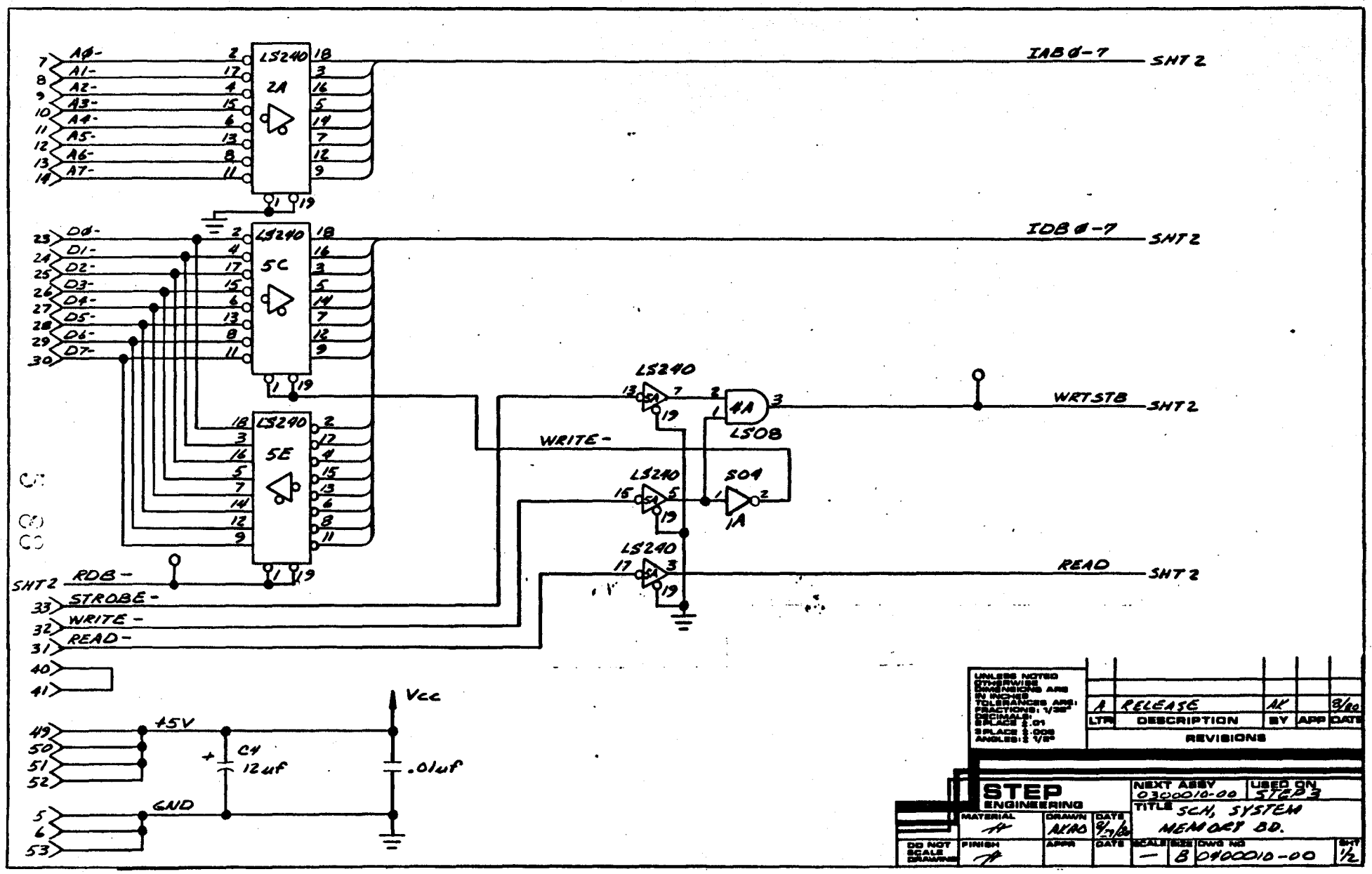
NEXT ASSY | USED ON STEP 3

TITLE ASSY, SYS. MEMORY 8D

MATERIAL -- | DRAWN DAF | DATE 4-30-80

DO NOT SCALE DRAWING | FINISH -- | APPR | DATE

SCALE NONE | SIZE D | DRAW NO 0300010-00 | REV A | SHT 1/1



LTR	DESCRIPTION	BY	APP	DATE
A	RELEASE	AK		8/80

REVISIONS

UNLESS NOTED OTHERWISE DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: 1/32 DECIMALS: 2 PLACE ± .01 3 PLACE ± .005 ANGLES: ± 1/2°

STEP ENGINEERING

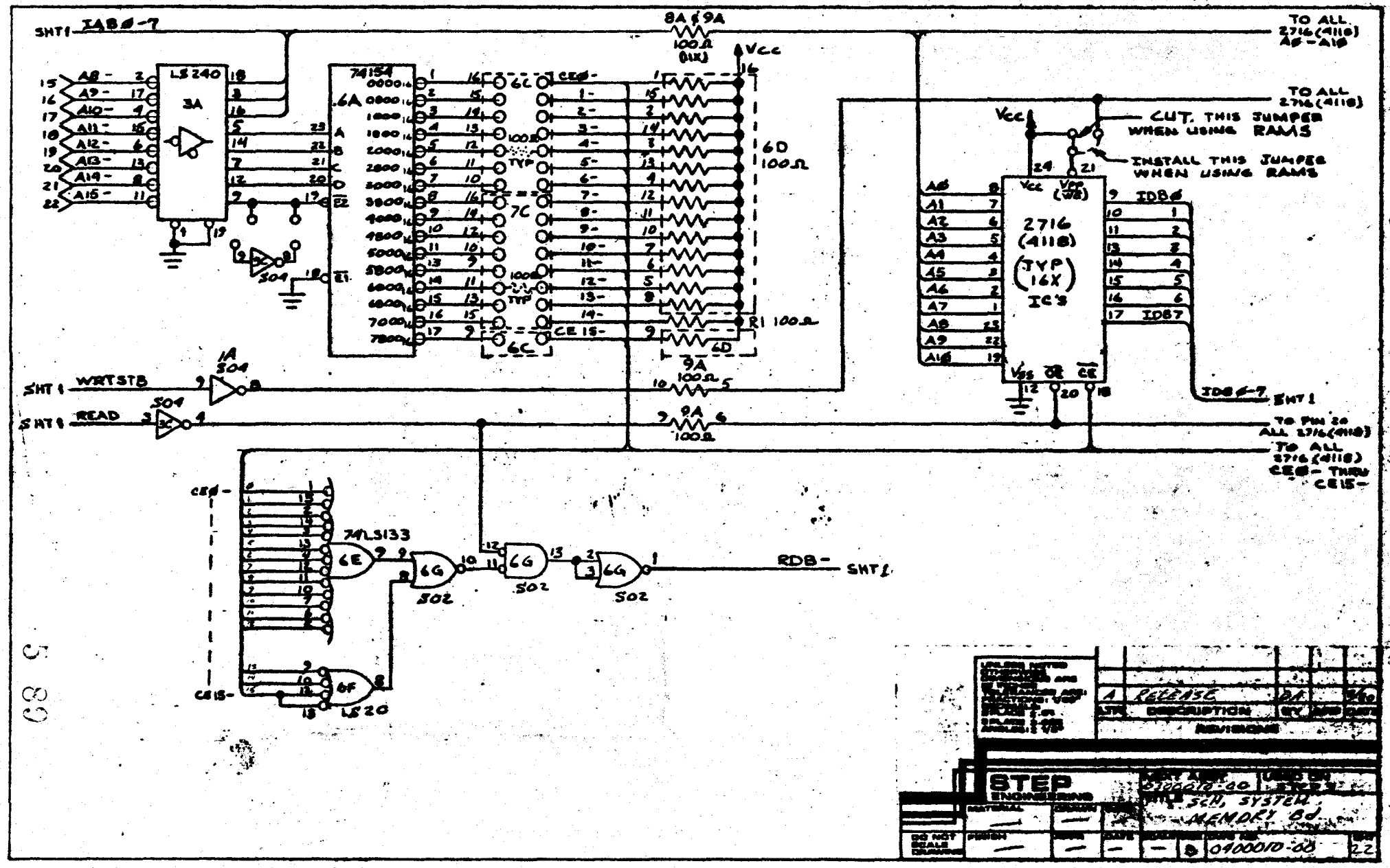
NEXT ASSY	USED ON
0300010-00	STEP 3

TITLE: SCH, SYSTEM MEMORY BD.

MATERIAL	DRAWN	DATE
—	AKRO	9/7/80

DO NOT SCALE DRAWING	FINISH	APPR	DATE
	—		

SCALE	SIZE	DWG NO	SHT
—	B	0400010-00	1/2


SHT1 IAB0-7
LS240
3A
74154
6A
6C
7C
6E
6F
LS20
8A & 9A
100Ω (1%)
Vcc
6D
100Ω
9A
R1 100Ω
TO ALL 2716(4118) A0-A10
CUT THIS JUMPER WHEN USING RAMS
INSTALL THIS JUMPER WHEN USING RAMS
2716 (4118) (TYP 16X) IC'S
IDB0
IDB7
IDB0-7
SHT1
TO PIN 20 ALL 2716(4118)
TO ALL 2716(4118) CE0- THRU CE15-
WRTSTB
READ
1A S04
S04
74LS133
S02
RDB-
SHT1
CE0-
CE15-
STEP ENGINEERING
A RELEASE
DRAWING NO. 0400010-00
SCH, SYSTEM, MEMORY BD.
0400010-00
SIZE B
SHEET 22

SECTION VI

APPENDICES

A - DATA SHEETS

B - MEMORY ORGANIZATIONS

C - ERROR MESSAGES

D - ASCII TABLES

E - TECHTRAN USAGE

F - OLD MEM-32 OPERATION

G - I/O CLOCK BOARD MODIFICATION

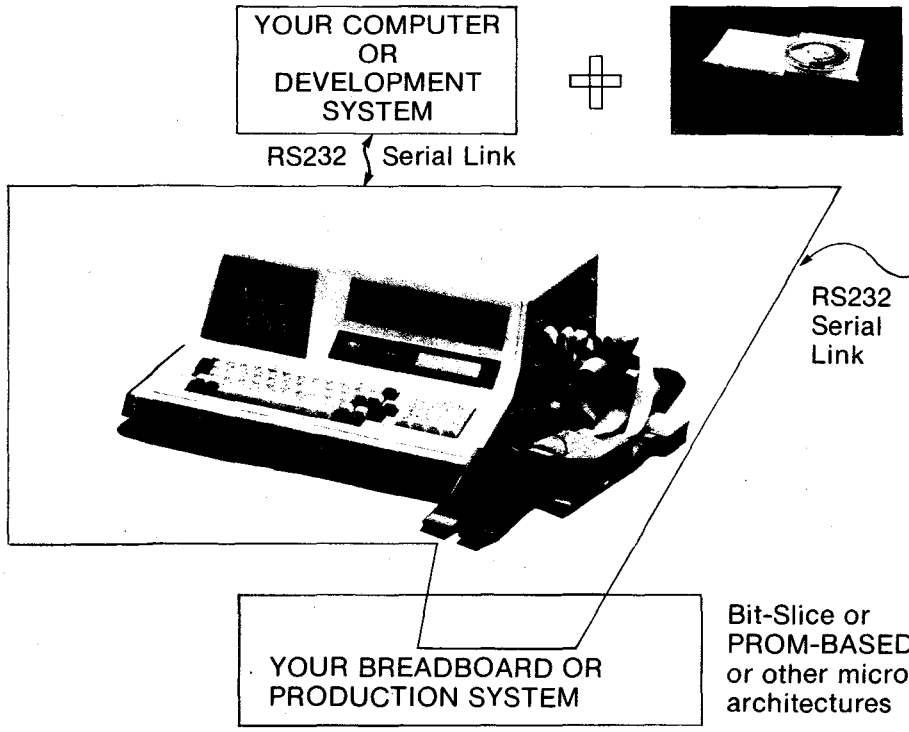
APPENDIX A

REPRINTS OF DATA SHEETS

STEP
ENGINEERING

STEP-3

DATA BOOK



A New Concept in Microcode Development, Test and Debug . . . Featuring:

SOFTWARE SUPPORT

- TMA, Industry Standard Meta Assembler
- Installs on Computers, Microcomputers, Development Systems
- MACRO-TMA, Advanced Superset of TMA
- Internal Firmware for Host-computer Interconnect
- Compatible with your Existing Software Base

MEMORY SIMULATION— Writable Control Store

- In-Circuit Memory Simulation to 40ns Worst Case
- Word Widths Reconfigurable from 8 to 96 or 288 Bits
- Up to 1152k Bits Total Memory, In Two Arrays
- User Configurable Memory Interface
- ROM Simulation or Cable Interconnect

WORD ORIENTED EDITING

- Hex or Octal and Binary Data Representation
- Enter, Fill, Move, and Search Commands
- Temporary Instruction Swap for Diagnostics

DIAGNOSTIC INSTRUMENTATION

- Multiple Breakpoints, plus External Qualifiers
- Trace Option, 250 Words by 32 or 80 Bits Wide
- Combinatorial, Sequential, and Delayed Triggering
- Internal Register, Port, and Flag Examination, XSTATE™

PROCESSOR CONTROL

- Full Target Processor Clock Controls
- Real Time Halt on Complex Conditions
- Force™ Arbitrary Instructions
- Jam Instructions at a Specified Address

OTHER FEATURES

- Total Application/Processor Independence and Transparency
- Multiple Load and Dump Options, STEP-3's the Terminal
- Simple, English Language Operation, Easily Learned
- Self Test Capability, Including Access Time

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(408) 733-STEP[7837] • TWX: (910) 339-9506

Printed in U.S.A. Due to our continuing program of product improvement, specifications are subject to change without notice.

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LISTING

STEP-3 Data Book
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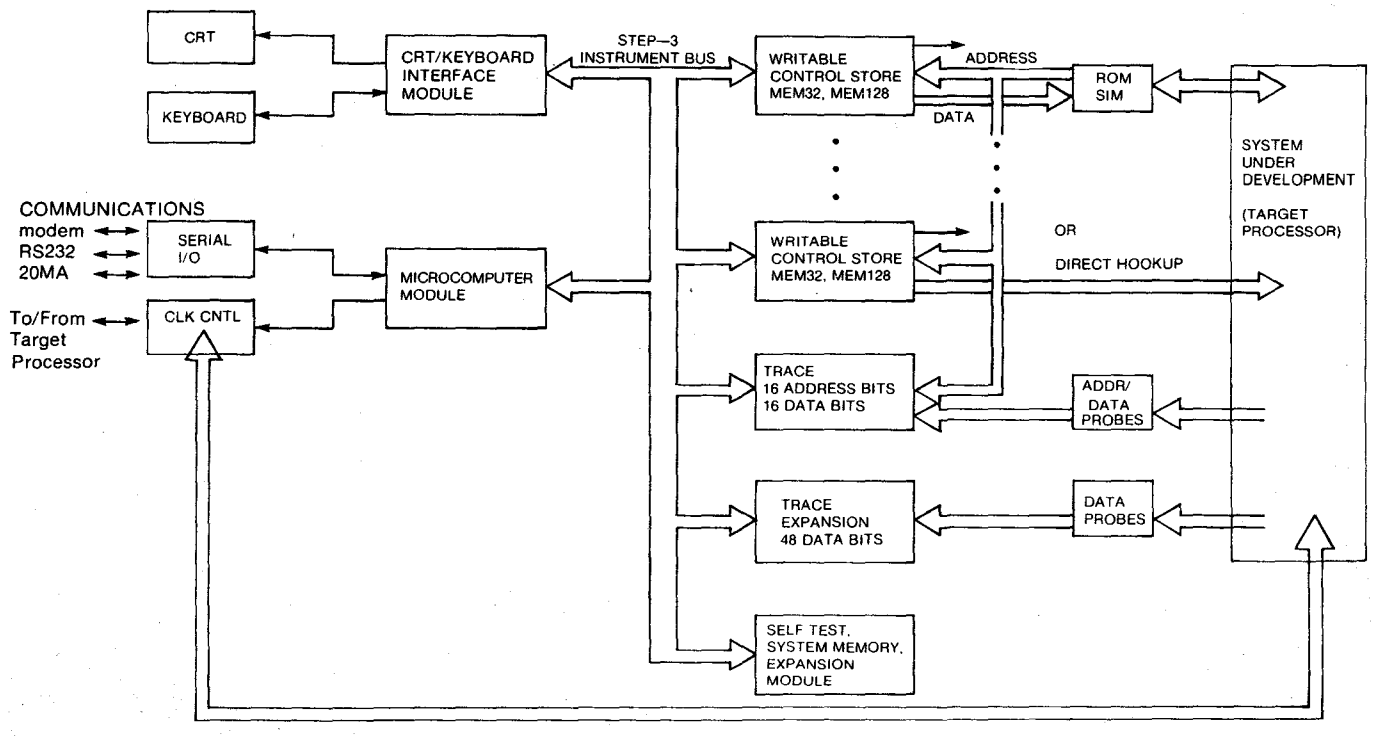


STEP-3
FUNCTIONAL BLOCK DIAGRAM

STEP 3

INTRODUCTION

Introduction

Firmware Integration and Test Station (FITS) is a flexible instrument for firmware testing, firmware integration and system testing of microcoded processors and controllers. It provides:

- A reconfigurable, variable word width, Writable Control Store for real-time firmware emulation.
- Diagnostic instrumentation for following and analyzing the path of execution of the processor/controller under development.
- Control instrumentation for starting execution at a desired point, reading and writing registers, and halting execution on complex conditions.
- A sophisticated word-oriented editor for "close to the hardware" system fault isolation and program patches.
- A method of loading and dumping programs from and to external computers and PROM programmers.
- Software packages to permit easy generation of microcode on existing computer systems.

The instrument is completely independent of and transparent to the system under development, requiring no special control lines or interconnects.

Powerful English-language commands along with extensive description messages and self test capabilities make the system easy to use and work with. All commands and data are entered through the alphanumeric and hex keyboards with the results displayed on the CRT.

Writable Control Store

The Writable Control Store, WCS, simulates all or part of the Microcode/application memory in real time during system development. It provides the ability to rapidly change program contents permitting fast and efficient checkout and generation of processor and system functions. Up to five Writable Control Stores, organized as one or two independent arrays, can be resident in Step-3. Nine Writable Control Stores can be used, with the optional Expansion Chassis. The WCS comes in two varieties: a 32k-bit version which can be organized lkx32, 2kx16 or 4kx8, and a 128k-bit version with 4kx32 or 3kx16 organization.

System organizations 8 to 96 bits per word in four bit increments can be efficiently achieved; 192 bits per word are possible if the two arrays are concatenated. The unique ability to simulate more than one memory array allows Step 3 to be useful in multiprocessor systems, systems with ROM address mapping, and systems with separate microcode and application memories.

System Interconnect

The easiest and most convenient way of connecting Step-3 to the target processor is through ROM Simulation modules. They plug directly into existing PROM sockets on both breadboard and production systems. These personality modules emulate existing ROMs and PROMs mechanically, electrically and functionally and can be field upgraded as PROM types change. Alternatively, the WCS can be connected directly to the target processor through a ribbon cable array connector. Each WCS has a bit mapping area and choice of interface type (buffered, non-buffered and register) to simplify the interconnect.

Editor

A word-oriented machine code editor simplifies the task of modifying program code to find or correct a problem. Four consecutive memory locations are displayed on the CRT along with a binary representation of the data at the current cursor location. ENTER: Through the use of the cursor controls, data may be entered at any position within the displayed word, and the current memory locations may be incremented, decremented or scrolled. MOVE: A block of data may be moved in memory to insert instructions or save a subroutine prior to modification. SEARCH: Individual instructions containing a specified data pattern composed of ones, zeros and don't cares can be searched for and located in memory, simplifying the task of modifying output routines or references to specific memory addresses. FILL: Any block of memory can be filled with a repeating word pattern. e.g. no-ops or waits.

Diagnostic Instrumentation

Several diagnostic features are incorporated in Step-3 to enable rapid system debug and test. On each Writable Control Store, a real time breakpoint (BNC output) is provided which can be used to halt the user's processor or trigger a logic analyzer or oscilloscope. The state of each breakpoint along with the current processor address is displayed on the CRT. Multiple breakpoints simplify conditional jump analysis by displaying the alternative program paths being executed.

Trace provides information as to which instructions are being executed by capturing in real time address, data, and control information. The powerful triggering capability enables capture of information the Nth time a subroutine has been entered, conditioned by the "AND" or "OR" of events and program address, or sequences of events and breakpoints.

The Trace option allows reconstruction of the processor's path of execution. Trace results can be dumped over a serial port, displayed on the CRT or used to halt the target processor.

A unique feature, XSTATE™, provides a way to use the Trace interactively with a user program to examine the contents of registers or I/O ports. The result is displayed on the CRT.

Processor Control

Step-3 provides full clock control features: Run, Step (single and multistep), Cycle (single and multicycle), Halt, and Halt on Event. By connecting to and controlling the existing target processor clock, it avoids problems encountered in clock replacement, and permits using the actual system clock.

Force™ and Jam add to the target processor control features built into Step-3. Force™ provides the ability to force an arbitrary instruction for N clocks to write a register, start execution at an unusual point in a program, or test hardware. Jam allows an existing instruction to be accessed out-of-sequence, to perform the same function.

Software Compatibility

Step-3 acts like a terminal, connecting to computers, minicomputers, development systems and timesharing systems. Through keyboard control, the baud rate and parity are configured to match an existing computer system (or PROM programmer).
Once the computer link has been established, files, source code, object code, etc. can be displayed on Step-3's CRT, or object code can be downloaded into memory. Transfer of object code to or from the external device is automatically initiated by Step-3 and synchronized on operator command.

Two formats are provided for object code transfer, MICROWORD™ and GENPROM™. The latter is a block transfer mode containing 4 or 8 bit data from successive memory addresses as PROM images. Header, frame and end characters are programmable, making it easy to interface to any assembler with a PROM output format, and to virtually any PROM programmer.

Software Support

Step offers three choices to speed software work:

- TMA, Transportable Meta Assembler
- MACRO-TMA
- Any existing assembler or compiler.

Both TMA and MACRO-TMA can be used for any microprogrammed processor. The TMA consists of a Definition Program for entry of opcodes, bit fields and symbols, a two pass Assembler Program, and a Formatter Program for outputting object code in either MICROWORD™ or PROM format. Cross reference tables, error listings, source and object code are provided as outputs. Versions are available for microcomputers, mini and maxicomputers and some development systems.

MACRO-TMA is a superset of the original TMA, with MACROS, PARITY, SPLIT FIELD, MULTILINE INSTRUCTION generation, and ENTRY POINT TABLE generation. Versions are available for mini and maxi computers. Step-3 can also be used with other assemblers and compilers, either by using existing PROM format outputs, or by writing an output format routine.

Operation

The instrument is controlled through the keyboard and front panel switches. Special purpose function keys simplify editing, downloading and controlling the target processor. An easy-to-read, fully formatted CRT displays the memory contents, system states and all information required to operate the instrument. Descriptive error messages reveal improper instrument set-up, invalid commands or addressing, and serial link failures. Recovery from an error condition is automatic upon entering the corrected information. Instrument operation is easy to learn and understand, with training time taking less than a day.

Self Test

Step-3 comes with internal Self Test programs for testing its own CPU and memory. A unique Self Test option even measures Writable Control Store and ROM Simulation access times at the target processor interface.

Testing both ports of the dual-port WCS memory dynamically, the Self Test battery of routines offers both short-form and more exhaustive long-form galloping pattern tests. Short form tests execute in about one minute; long-form tests take about 20 minutes for MEM-32 and nearly five hours for MEM-128.

Command Summary

Once the instrument parameters have been specified through SETUP, the commands can be accessed in any order.

CLASS	COMMAND	PARAMETERS (SUBCOMMANDS)*	DESCRIPTION
INSTRUMENT *Specifies and tests instrument parameters*	SETUP	NUMBER OF ARRAYS = 1,2 DATA FORMAT = HEX, QCTAL STARTING ADDR = } for ARRAY WIDTH = } each ARRAY DEPTH = } array	Configures the instrument to match the requirements of the target processor. Checks for a memory array specification consistent with the number and organization of the Writable Control Stores.
	TEST	TEST FLAG = 4 thru 10 CARD TYPE = 0,1 (tests 5 thru 10) SLOT NUMBER = 0 thru 7 (tests 5 thru 10) ACCESS TIME = 2-254 (test 7 thru 10)	Tests instrument and memory operation. Test 4, SUMCHK, checks instrument CPU and EPROM contents. Tests 5 and 6, GALPAT and QUICHK check slow speed RAM operation. Tests 7 thru 10 (USRPRT, ACCESS, FASTCK, and SHMOO) use the Self Test option to thoroughly check the Writable Control Stores at speed and determine access time.
	ARRAY	ARRAY = 1,2	Selects memory array to be accessed.
INPUT/OUTPUT *Permits communication over serial links with external devices such as computers, PROM programmers, etc.*	LOAD DUMP COMPARE	FORMAT = 0 thru 3 DEVICE = 0 thru 5 START ADDR = NO OF WORDS = WIDTH } PROM at a time POSITION } Formats only (BAUD RATE) (PARITY) (STOP BITS) (HEADER, FRAME, END CHAR) (TEXT) (XPARM)	LOAD loads the WCS memory in a MICROWORD™ (word-at-a-time) format or one of several PROM formats. DEVICE specifies serial link (20ma, RS 232, or Modem, as well as line protocol). DUMP dumps the contents of the specified memory array segment over the serial links in PROM or MICROWORD™ image. COMPARE compares the contents of memory to the information being received over the serial link. The address if any location whose contents do not match the incoming data is shown in an error message.
	TEXT		When in TEXT, the instrument acts like a limited terminal. TEXT enables easy interface to computers, printers, PROM programmers, etc.
EDITOR *Enables the user to examine or modify memory array contents through the keyboard*	ENTER	(ADDRESS) (cursor ↑↓ → ←) (QUIT) (CLEAR) (DEL) (C&H) (ENTER)	Enters, modifies or displays data words of up to 96 bits in octal or hex format. Cursor controls permit data to be entered at any position within the four displayed memory locations and allows the currently displayed window to be incremented/ decremented or scrolled. The address and bit position of the cursor are displayed along with a binary representation of the data.
	FILL	START ADDR = END ADDR = WORD CONSTANT =	Fills a memory block with a specified word. When no word is specified, defaults to zeros.
	MOVE	DESTINATION ADDR = START ADDR = NUMBER OF LOCATIONS =	Moves a block of code from one memory location to another. The original data remains intact unless written over by the MOVE command.

STEP-3

CONCLUDED

CLASS	COMMAND	PARAMETERS (SUBCOMMANDS)*	DESCRIPTION
EDITOR	SEARCH	START ADDR = END ADDR = COMPARISON WORD = DON'T CARE WORD =	Searches a block of code for a particular data pattern composed of ones, zeros, and don't cares. When a match is found, the address and memory word are displayed and the search is stopped until continued by the operator.
MONITOR *Real time simulation of processor memory and control/display of processor activity*	MONITOR	(RUN) (Halt) (Step) (N### step) (Cycle) (M### cycle) (DISABLE) (PULSE)	Enables the Writable Control Stores, displays Breakpoint Address, Breakpoint and Trace Status. The subcommands RUN thru DISABLE permit full control of the target processor clock from the Step-3 front panel and current address/ Trace data from the user's system. PULSE acts as the reset.
		(RALACE) (RBLACE) REPLACE WORD = REPLACE ADDR =	RA, RB are convenient editing commands which allow two words in memory to be temporarily replaced to help track down problems. The original memory contents are saved and restored on command.
		(BREAK) BREAKPOINT NUMBER = 1 thru 6 BREAKPOINT ADDR =	Sets breakpoint address without disturbing target processor. Breakpoint and Trace outputs can be used to halt the target processor if desired.
		(TRACE) SOURCE 1 = 0 thru 12 TRIGGER EVENT NUMBER = 1 thru 255 SOURCE 2 = 0 thru 12 TRIGGER EVENT NUMBER = 1 thru 255 TRIGGER POSITION = 1 thru 250	Trace setup is accomplished through a series of self teaching menus and does not disturb target processor operation. The Trace results can be viewed on Step's CRT or downloaded to an external device using the DUMP command.
		ASSIGN TBR1 = 1 thru 6 ASSIGN TBR2 = 1 thru 6	Any of six hardware breakpoints can be assigned to be Trace Breakpoints TBR1,2.
		(ARM TRACE)	
		(XTRACE) (Line ###) (DUMP) (FORMAT = 1,2,3) (QUIT)	
		(XSTATE)	XSTATE™, examine state, allows the target processor's internal registers or I/O ports to be read.
		(FORCE) FORCE WORD = CLOCK TICKS = 1 thru 250	Forces an instruction out of the Writable Control Store for the Specified number of clock ticks.
		(JAM) ADDRESS = CLOCK TICKS = 1 thru 250	Jams the contents of Writable Control Store contained in the address specified, for the desired number of clock ticks.
		(EXCHNG)	Displays status information for the second array.

*Items in "( )" are optionally used subcommands. "#" refers to numeric data included within the command. Lower case letters are not part of the command but are included to enhance understanding: Example "Step." S is the command, single step is the function.

MEM-32

WRITABLE CONTROL STORE

Features

- **32K bits high speed storage**
- **Switch selectable memory organization: 12K × 32, 2K × 16, 4K × 8**
- **Stackable to obtain word widths to 288 bits**
- **Real time operation**
- **User configurable interface**
- **Optional ROM emulator outputs**
- **Hardware bit mapping**
- **Integral real time breakpoint**
- **Read/Write operation**
- ***45 ns worst case access time, "A" version***
- ***36 ns worst case access time, "F" version***

Description

GENERAL

MEM-32 is a dual-port, high-speed, 32K-bit Writable Control Store family that plugs into STEP-2 Firmware Integration and Test Station. One port is accessed from STEP-2 to load, dump, or modify memory contents. The second port is accessed by the user's system (target processor) in either a read only or read/write mode. MEM-32 replaces all or part of the target processor's ROM, PROM, and even RAM memory during system debug and/or test, permitting rapid changes to the code to find or patch microcode errors. MEM-32's 36ns worst case access time allows the user's system to run at fast real time rates.

MEMORY ORGANIZATION

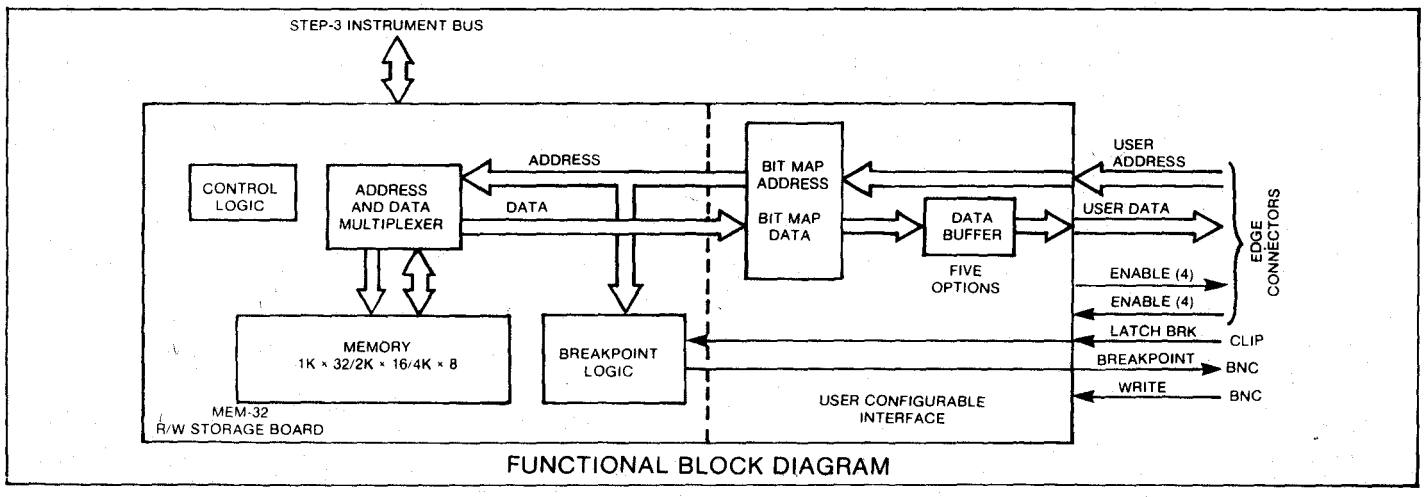
Up to three MEM-32's can be plugged into a STEP-3 instrument giving the user a total of 160K bits of memory space. With the optional expansion chassis, an additional 128K bits of storage can be added for a total of 288K bits. Both MEM-32 and MEM-128 WCS can be resident in STEP-3 when assigned to different memory arrays. Each WCS is self-contained with its own address input, breakpoint output, and data output. The standard configuration is 1K × 32 but the outputs can be OR'ed together to form a 2K × 16 array or a 4K × 8. Two or more Writable Control Stores can be combined creating either deeper or wider memory arrays. Word widths of 8, 16, 24, 32, 48, 64 or 96 bits (288 bits with expansion chassis) can be achieved.

ADDRESS COMPARATOR

Each MEM-32 has an internal real-time address comparator which can generate a breakpoint to halt the target processor or serve as a trigger for another diagnostic instrument. A breakpoint display of each comparator's output state is provided on STEP-3's CRT. An optional qualifier input is provided to insure that only valid addresses are used as comparator inputs. The qualifier input is switch selectable: high or low true, edge or level sensitive.

WRITE OPERATION

The MEM-32 contains circuitry to allow its use as a read/write memory. A BNC connector is provided for the write-control input. When this input becomes low, the data output goes tristate, allowing input data to be written to the RAM. A switch is provided to inhibit write operation when the option is not desired.



FUNCTIONAL BLOCK DIAGRAM

MEM-128

WRITABLE CONTROL STORE

Features

- **128K bits high speed storage**
- **Switch selectable memory organization: 4K × 32, 8K × 16**
- **Stackable to obtain word widths to 288 bits**
- **Real time operation**
- **User configurable interface**
- **Optional ROM emulator outputs**
- **Hardware bit mapping**
- **Integral real time breakpoint**
- **Read/Write operation**
- ***180 ns worst case access time, "B" version***
- ***70 ns worst case access time, "A" version***
- ***50 ns worst case access time, "F" version***

Description

GENERAL

MEM-128 is a dual-port, high-speed, 128K-bit Writable Control Store family that plugs into STEP-3 Firmware Integration and Test Station. One port is accessed from STEP-3 to load, dump, or modify memory contents. The second port is accessed by the user's system (target processor) in either a read only or read/write mode. MEM-128 replaces all or part of the target processor's ROM, PROM, and even RAM memory during system debug and/or test, permitting rapid changes to the code to find or patch microcode errors. MEM-128F's 50 ns worst case access time and MEM-128A's 70 ns access allow the user's system to run at fast real time rates. An economical 180 ns (option "B") version of MEM-128 is also offered for slower systems or for use as main program memory.

MEMORY ORGANIZATION

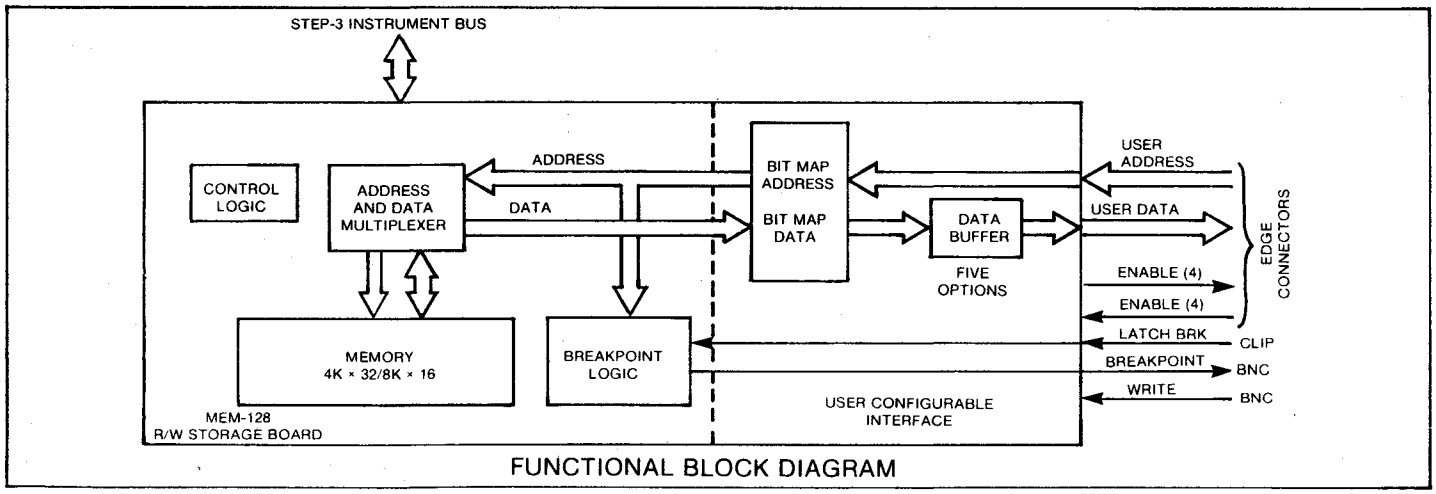
Up to five MEM-128's can be plugged into a STEP-3 instrument giving the user a total of 640K bits of memory space. With the optional expansion chassis, an additional 640K bits of storage can be added for a total of 1280K bits. Both MEM-32 and MEM-128 WCS can be resident in STEP-3 when assigned to different memory arrays. Each WCS is self-contained with its own address input, breakpoint output, and data output. The standard configuration is 4K × 32 but the outputs can be OR'ed together to form a 8K × 16 array. Two or more Writable Control Stores can be combined creating either deeper or wider memory arrays. Word widths of 16, 32, 48, 64 or 96 bits (288 bits with expansion chassis) can be achieved.

ADDRESS COMPARATOR

Each MEM-128 has an internal real-time address comparator which can generate a breakpoint to halt the target processor or serve as a trigger for another diagnostic instrument. A breakpoint display of each comparator's output state is provided on STEP-3's CRT. An optional qualifier input is provided to insure that only valid addresses are used as comparator inputs. The qualifier input is switch selectable: high or low true, edge or level sensitive.

WRITE OPERATION

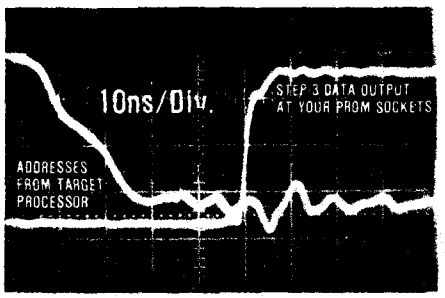
The MEM-128 contains circuitry to allow its use as a read/write memory. A BNC connector is provided for the write-control input. When this input becomes low, the data output goes tristate, allowing input data to be written to the RAM. Two switches are provided to inhibit write operation when the option is not desired. In the 8K × 16 organization, these switches permit writing into all or none of memory, or the upper 4K words only, or the lower 4K words only.



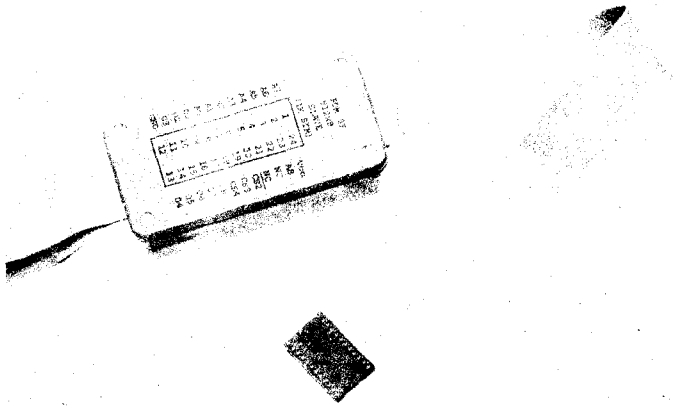
FUNCTIONAL BLOCK DIAGRAM

ROM-4/8

ROM SIMULATION



Voltage Waveform



ROM Module

Features

- **Direct plug-in to target processor ROM sockets**
- **Emulation of over 200 ROMS and PROMS**
- **Directly compatible with MEM-32 and MEM-128 writable control stores**
- **Uses full address space of writable control stores**
- **Low capacitance inputs and outputs**
- **Good signal fidelity and output rise/fall times**
- **Field upgradable**
- **Ruggedized interconnect**
- **Standard, latching, and register versions**

Description

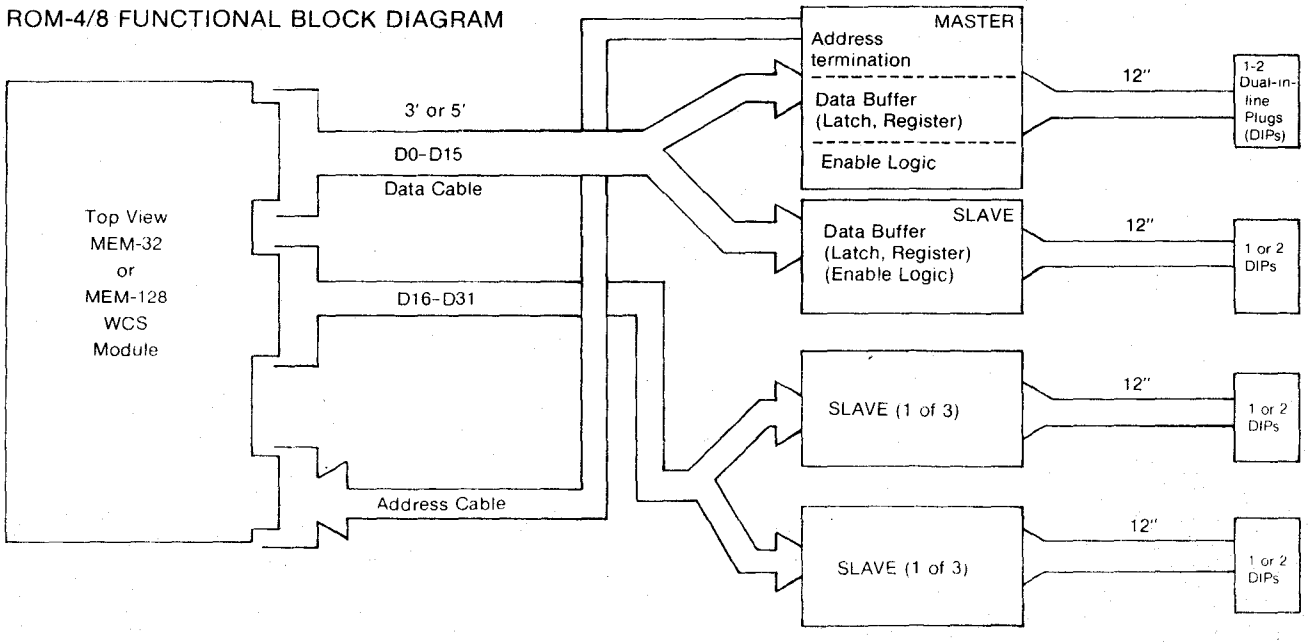
ROM-4/8 are ROM/PROM simulation options which give STEP-3 the ability to interface to an existing processor system through its ROM sockets. The outputs of ROM-4/8 are dual-in-line plugs wired to emulate the ROM or PROM of the system's program store. They are designed to interface to MEM-32 and MEM-128 Writable Control Stores, WCS, by plugging into the edge connectors.

Four ROM-4/8 modules are normally required for a complete interface to a 32-bit-wide WCS. One module, designated MASTER, contains both address inputs and data outputs. The other three, SLAVES, contain just the data outputs. Modules which emulate ROMs with less than 1K address space have external address inputs to allow the full 1K (4K) address space of MEM-32 (MEM-128) to be utilized. ROM modules can be OR'ed in the same fashion as ROMs and PROMs through the use of the Chip Select, CS, inputs.

ROM 4 is a series of dual, 4-bit output ROM emulation modules with 16 and 18 pin outputs. It can emulate ROMs with 256 × 4, 512 × 4, 1K × 4, 2K × 4, and 4K × 4 organizations. ROM-8 is a series of 8-bit output ROM emulation modules with 256 × 8, 512 × 8, 1K × 8, 2K × 8, and 4K × 8 organizations. Popular 20, 22 and 24 pin options are available as well as versions with latching and register outputs.

High reliability is maintained by using a custom, etched, flexible circuit which serves as the interconnect cable between the ROM socket and buffer module. This interconnect cable is stress relieved at each end to achieve maximum reliability. The cable design ensures low crosstalk and reduces input and output capacitance to that of the ROM array being replaced.

ROM-4/8 FUNCTIONAL BLOCK DIAGRAM



How To Pick A ROM Simulation Module

1. Determine organization of PROM (# Words × Bits), # Pins, and output type (Tristate, Register, etc.)
2. Determine array depth of the memory you are simulating: 256, 512, 1K, 2K, 4K, 8K, . . .
3. Look up the appropriate ROM (PROM) simulation modules for the type of STEP memory module being used. Determine whether to use the direct or recommended simulation module.

   NOTE: Manufacturers are adding new ROMs and PROMs weekly. If the proper simulation module for your PROM is not shown, consult Step Engineering directly.

4. Check the pinout and cross reference charts of your final choice against the actual PROM being used.

ROM 4/8

CONTINUED

5. Determine the number of bits of PROM to be simulated. If the modules are not wire-ORed, the number is the width of the control store rounded up to the nearest 16-bits increment. i.e. 1k × 44 control store would require 48 bit simulation. The number "48" would then be used as part of the item designators in place of the "*" i.e. ROM 4D/48 if a 1k × 4 PROM were being used.

   In the case of wire-ORed ROM simulation divide the depth of the memory array by the depth of the ROM module and multiply by the number of target bits, i.e. a 16k × 32 bit memory array using a ROM 8T would require (16k/8k) × 32 or ROM 8T/64.

ROM SIMULATION OPTION CHART

SIZE	ROM PINS	OUTPUT	TOTAL MEMORY DEPTH	ROM SIM FOR MEM-32 DIRECT	ROM SIM FOR MEM-32 RECOMMENDED	ROM SIM FOR MEM-128 DIRECT	ROM SIM FOR MEM-128 RECOMMENDED	ROM/ PINOUT
256 × 4	16	TS	1k	ROM4A/*	ROM4B/*	--	ROM4F/*	1
512 × 4	16	TS	1k	ROM4B/*	ROM4B/*	ROM4F/*	ROM4F/*	1
1K × 4	16	TT	1k	ROM4C/*	---	---	(NOTE B)	1
1k × 4	18	TS	1k	ROM4D/*	ROM4D/*	ROM4G/*	ROM4G/*	2
1k × 4	18	TS	2k	(ROM4D/*) D	ROM+4E/*	ROM4G/*	ROM4G/*	2
2k × 4	18	TS	2k	ROM+4E/*	ROM+4E/*	ROM4H/*	ROM4H/*	2
2k × 4	18	TS	4k	(ROM+4E/*) D	---	ROM4H/*	ROM4H/8	2
2k × 4	18	TS	8k	(ROM+4E/*) D	---	ROM4J/*	ROM4J/*	2
4k × 4	20	TS	4k	---	---	ROM+4K/*	ROM+4K/*	-
32 × 8	16	TS	1k	ROM8L/*	ROM8L/*	---	---	9
256 × 8	20	TS	1k	ROM8C/*	(ROM8F/*) C	---	(ROM8BB/*) C	3a
256 × 8	24	TS	1k	ROM8B/*	ROM8G/*	--	ROM8V/*	4
256 × 8	24	L,TS	1k	ROM8A/*	(ROM8D/*) C	--	(NOTE B)	5a
512 × 8	20	TS	1k	ROM8F/*	ROM8F/*	ROM8BB/*	ROM8BB/*	3b
512 × 8	22	R,TS	1k	ROM8R/*	ROM8R/*	ROM8R/*	ROM8R/*	6
512 × 8	24S	R,TS	1k	ROM8EE/*	ROM8EE/*	(NOTE B)	(NOTE B)	7
512 x 8	24	TS	1k	ROM8E/*	ROM8G/*	ROM8Q/*	ROM8V/*	4
512 × 8	24	L,TS	1k	ROM8D/*	ROM8D/*	(NOTE B)	(NOTE B)	5b
512 × 8	20	TS	2k	ROM+8AA/*	ROM+8AA/*	ROM8BB/*	ROM8BB/*	3b
512 × 8	24	TS	1k	ROM+8N/*	ROM+8J/*	ROM8Q/*	ROM88Q/*	4
1k × 8	24	TS	1k	ROM8G/*	ROM88G/*	ROM8V/*	ROM8V/*	4
1k × 8	24	TS	1k	ROM++8H/*	ROM++8H/*	NOTE B)	(NOTE B)	4
1k × 8	24	L,TS	1k	ROM8P/*	ROM8P/*	NOTE B)	(NOTE B)	8
1k × 8	24	TS	2k	ROM8Y/*	ROM8J/*	ROM8V/*	ROM8V/*	4
2k × 8	24	TS	4k	ROM8J/*	ROM8J/*	ROM8W/*	ROM8W/*	4
2k × 8	24	TS	2k	ROM++8k/*	ROM++8k/*	ROM++8CC/*	ROM++8CC/*	4
2k × 8	24	TS	8k	----	----	ROM8T/*	ROM8T/*	4
4k × 8	24	TS	4k	----	----	ROM++8U/*	ROM++8U/*	4

NOTES:

A) ROMs for MEM-32 can be used with MEM-128 modules except for those marked "ROM+" which are multiplexing. However, maximum address space will be 1k words.

B) ROMs for MEM-128 can be used for MEM-32 except where "ROM+" a multiplexing version is called out.

C) Pinout difference on address line, check carefully before using.

D) Must be wire-ORed to achieve desired depth.

*Number of bits simulated (see 5 above)

ROM+: Multiplexing ROM sim module for use with MEM-32 organized 2k × 16 or 4k × 8; with MEM-128 organized 8k × 16.

ROM++: EPROM replacement

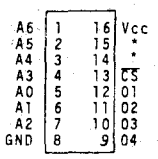
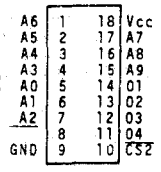
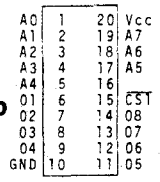
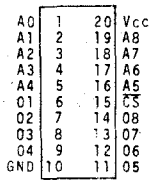
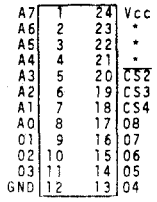
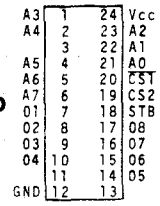
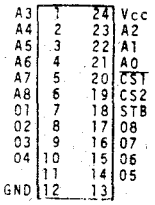
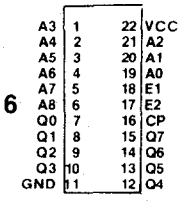
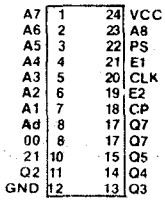
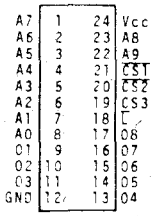
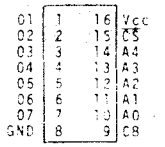
TS, Tristate; TT, Totempole; R, Register; L, Latching.

24S: 24 Pin slimline package, pin rows on .300 centers

ROM 4/8

CONCLUDED

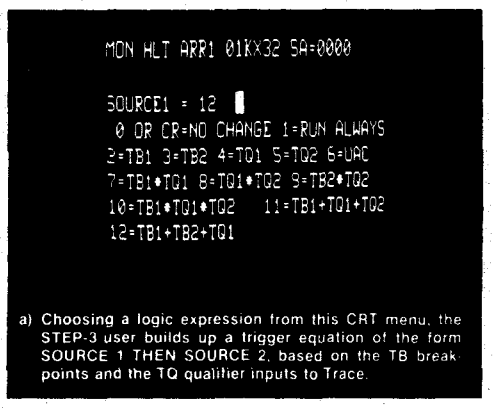
ROM CROSS REFERENCE TABLE

#	PINOUT ORGANIZATION	AMD	FAIR	HARRIS	INTEL	MMI	NAT	SIG	TI
1	 PIN * 14 / 15 256 × 4 NC / CS 512 × 4 A8 / CS 1k × 4 A8 / A9	27S21 27S13 —	93427 93446 —	7611 7621 7644	— — —	63141 63241 —	74S287 71S571 —	82S129 82S131 —	74S287 — —
2	 PIN* 8 1k × 4 CS1 2k × 4 A10	27S33 —	93453 —	7643 7685	3625 —	63441 63841	74S573 87S185	82S137 82S185	74S576 74S454
3 a,b	 a) 256 × 8  b) 512 × 8 256 × 8 512 × 8	— 29773	— —	— 7649	— —	63281 63481	— 74S472	— 82S472	74S471 74S472
4	 PIN* 21 / 22 / 23 256 × 8 CS1 / NC / NC 512 × 8 CS1 / NC / A8 1k × 8 CS1 / A9 / A8 2k × 8 A10 / A9 / A8	— 27S31 -- —	— 93448 93451 —	7629 7641 7681 76161	— 3624 3628 3636	6336 63S483 63S881 63S1681	— 74S474 87S181 —	— 82S141 82S181 82S191	— 74S474 74S478 74S452
5 a,b	 a) 256 × 8  b) 512 × 8 256 × 8 512 × 8	— —	— —	7625 7647R	— —	— —	— —	82S114 82S115	— —
6	 6	27S27	—	—	—	—	—	—	—
7	 7	27S25	—	—	—	—	—	—	—
8	 8	—	—	7681R	—	—	—	—	
9	 9	27S19	—	7603	—	6331	74S288	82S123	74S288

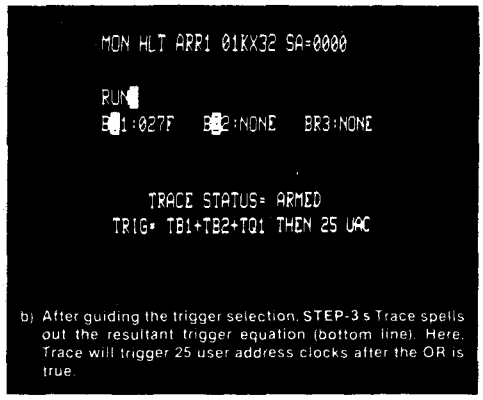
NOW 80 bits wide!

TRACE

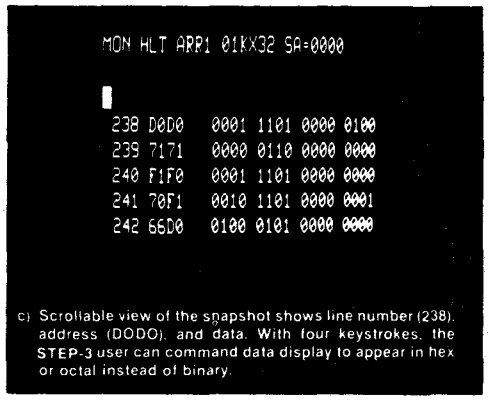
LOGIC ANALYZER OPTION



a) Choosing a logic expression from this CRT menu, the STEP-3 user builds up a trigger equation of the form SOURCE 1 THEN SOURCE 2, based on the TB break points and the TQ qualifier inputs to Trace.



b) After guiding the trigger selection, STEP-3's Trace spells out the resultant trigger equation (bottom line). Here, Trace will trigger 25 user address clocks after the OR is true.



c) Scrollable view of the snapshot shows line number (238), address (D0D0), and data. With four keystrokes, the STEP-3 user can command data display to appear in hex or octal instead of binary.

Features

- **Basic board synchronously captures:**
  - **16 Address Inputs**
  - **16 User definable inputs**
- **Expansion board captures additional 48 inputs**
- **Captures 250 cycles before, around, or after trigger**
- **Real time operation (to 11 MHz)**
- **Powerful triggering modes—TRACE initiated by:**
  - **T Trigger: Address, qualifier, or clock**
  - **NT Nth Trigger occurrance**
  - **C Trigger combinations: AND, OR of address/ qualifiers**
  - **C → NT Sequential trigger events:**
  - **NT → C Trigger event 1 followed by trigger event 2**
- **Conditional capture capability**
- **Easy TRACE setup and examination**
- **Installs in STEP-3 firmware integration and test station**
- **Output to halt target processor on trigger or TRACE completion**
- **Hard copy via serial output to printer or host computer**
- **LSAMPLE displays on data processor busses**
- **XSTATE™ displays contents of internal registers and I/O ports**

Description

The Trace option provides a convenient means to follow the path of execution of the target processor. It simplifies fault isolation of firmware problems and greatly enhances the usefulness of STEP-3. Both address and data information are synchronously captured at rates up to 11 MHz without affecting target processor operation. Captured information is stored in a separate trace memory independent of the WCS memory used by the target processor.

Extensive triggering capability provides easy isolation of the program segment to be monitored. Setting up the Trace parameters is easy—the CRT prompts you with all the choices, and the parameters can be examined or modified at any time. The "snapshot" captured is displayed on command on STEP-3's CRT, in a convenient hex, octal or binary format—your choice. To provide hard copy or computer processing, captured Trace information can be dumped on command over a serial link.

LSAMPLE, XSTATE™

LSAMPLE and XSTATE™ are new features of the Step-3 mainframe which are only available when the Step-3T Trace option is installed. LSAMPLE, last sample, provides a readout of bus status during single step and single cycle operation.

XSTATE™, examine state, works in conjunction with a user defined program to read and display the contents of internal registers and I/0 ports. For this use, the Trace option must be connected to the target processor data bus.

Installation

The Trace option installs in any slot of the STEP-3 backplane, leaving four slots available for memory boards and options such as the 48-bit Trace expansion. Connection to the target processor address bus is through the Master ROM simulation assembly and an external buffered probe. This probe is used for the remaining upper order addresses, address clock, and external triggers. Two other external probes serve as inputs for the sixteen data lines and the data clock. In all, 32 bits of information, 16 address and 16 data are captured during each processor cycle.

With the Trace expansion board an additional 48 data bits are captured during each cycle with no degradation in timing. The six expansion probes, like the three basic Trace probes, connect into the target processor through clips, or slide directly onto standard square or round wire-wrap posts. Alternatively, standard ribbon cable can be used to connect the Trace inputs directly to data busses or connectors.

TRACE

CONCLUDED

Triggering

Finding firmware problems is simplified by the extensive triggering facility built into Trace. This facility permits easy specification of the program segment to be monitored. A Trace can be initiated by a trigger, such as an address compare; by the Nth occurrence of the trigger; or by trigger followed by a second independent trigger. Twelve equations ranging from single qualifiers and address compares to long logical expressions specify the trigger sources. Qualifiers can be control bits from WCS memory, clocks, ALU outputs, interrupt inputs or any other useful signals. The trigger position within the captured data is also programmable, allowing events up to, around or after the trigger to be monitored.

The trigger flexibility makes possible the capture of complex data such as:

- The entrance/exit conditions from a subroutine
- A subroutine the Nth time it is called
- Processor activity N clocks after an event
- A routine after a control line has been set AND an external event has occurred N times.

These capabilities, combined with the ability of STEP-3 to rapidly modify control-store memory, add a new dimension to firmware diagnosis.

Trigger setup is easy to learn and takes only seconds to accomplish. A series of "menus" display the current selection and options in the following sequence: First Trigger Event, Number of Events to Trigger (if applicable), Second Trigger Event, Number of Events to Trigger (if applicable), Trigger Position within captured data, and Breakpoint Assignment. During the presentation of each option, the current selection is displayed. A new choice can be entered, or the old choice may be retained and the next menu called by hitting carriage return. At any time, the address-compare (breakpoint) values can be modified to follow the processor's execution path, without changing the Trace setup.

Event Capture

Up to 250 processor cycles are synchronously captured during a Trace. Nine separate reference signals, or clocks, may be used for information capture: one for address and one for each of the eight eight-bit data probes. The clock edge used to synchronously latch incoming addresses and data is individually switch programmable, negative or positive.

To prevent race conditions from causing improper capture, each group of sixteen address and data bits use a separate, independent internal clock generated from the corresponding user clock input.

An External Enable (EE) line is provided to allow direct control over information to be captured. This can allow a series of snapshots of processor activity, or can lengthen the time span of Trace by capturing every Nth processor cycle, or only the interesting cycles. An extra bit or flag in the target processor WCS memory itself can be used as an input to the EE line to selectively capture the information of interest.

Target Processor Control

The Trace Triggered (TG) and Trace Done (TD) outputs can be used as inputs to external devices. Both TG and TD are designed to tie to the External Halt input on the I/O and clock board. These signals go true only when the complex trace triggering conditions are met, and remain true until a new Trace is started or the Disable command is used. The Disable command forces the output false thus preventing system lockup. Hookup in this manner, along with XSTATE™, allows the target processor to be halted on a complex event and internal processor states monitored to determine problem areas.

Trigger Equations

#	EQN	MODE	DESCRIPTION
1	-	-	Always triggered, or "Run Always"
2	TB1	T	Trace Breakpoint 1 (16 bit Address Comparator)
3	TB2	T	Trace Breakpoint 2 (16 Bit Address Comparator)
4	TQ1	T	Trace Qualifier 1
5	TQ2	T	Trace Qualifier 2
6	UAC	T	User Address Clock (From Target Processor)
7	TB1•TQ1	C	Logical "AND" of TB1, TQ1
8	TB2•TQ2	C	Logical "AND" of TB2,TQ2
9	TQ1•TQ2	C	Logical "AND" of TQ1, TQ2
10	TB1•TQ1•TQ2	C	Logical "AND" of TB1, TQ1, TQ2
11	TB1+TQ1+TQ2	C	Logical "OR" of TB1, TQ1, TQ2
			NOTE: TB1+TQ1, TB1+TQ2, TQ1+TQ2 can be obtained with choice #11.
12	TB1+TB2+TQ1	C	Logical "OR" of TB1, TB2 TQ1
			NOTE: TB1+TB2, TB1+TQ1, TB2+TQ1 can be obtained with choice #12.

T — Simple Trigger
C — Combinatorial Trigger

Trigger Event Number, N

The Trigger Event Number defines the number of times a "T" trigger input occurs before a trigger is generated. N=1 to 255.

TRIGGER MODES	TRIGGER DEFINITIONS
C	Trace on the first occurrence of chosen combinatorial trigger equation.
NT	Trace on the Nth occurrence of trigger input.
C→T	Trace on the first occurrence of trigger T after the first occurrence of the combinatorial equation (C).
T→C	Trace on the first occurrence of the combinatorial equation (C) after the first occurrence of Trigger T.
NT→C	Trigger on the first occurrence of C after the Nth occurrence of T.
C→NT	Trigger on the Nth occurrence of T after the first occurrence of C.

SELF TEST

OPTION

Features

- **Complete check of Writable Control Store From User Port**
- **Measures Memory Access Time**
- **Four Memory Tests:**

  Continuity of Address, Data, and Breakpoint Lines
  Memory Access Time Verification
  Fast Check of Memory Access time
  Determination of Memory Access Time
- **Optional test of ROM Simulation Modules**

Description

The Self Test Module, STEP-3S, operates in conjunction with internal Self Test programs to provide a complete check of memory operation, It connects to both MEM-128 and MEM-32 Writable Control Stores by means of ribbon cables and jumpers (provided). It completely checks WCS operation from the target processor port including access time (worst case).

This self test board provides numerous benefits to the user. It allows for "go/no go" check out and maintenance on the instrument. It permits a real time instrument-quality measurement of memory integrity, which may be performed as a periodic calibration. Short, calibrated-length cables are provided for easy user interconnect.

A companion board, PG board, plugs into the output of the Self Test board to permit ROM Simulation testing. This uncommited board lets the user wire-wrap particular ROM configuration sockets for ROM cable testing.

Four tests may be run using the Self Test Board:

USRPRT, a test to verify the functioning of the control-store at a chosen access time using a "ping-pong" address pattern to guarantee all possible address transitions.

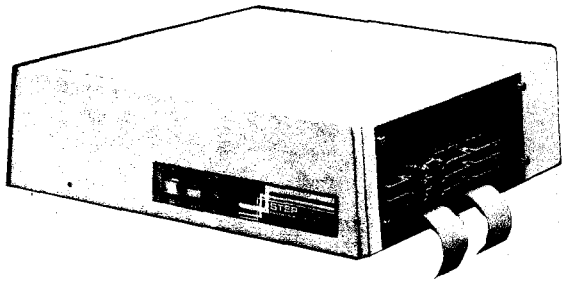
ACCESS, a thorough measurement of control store at a chosen access time using a "ping-pong" address pattern to guarantee all possible address transitions.

FASTCK, a rapid but less complete check of the control store at a specified access time.

SHMOO, a rapid determination of control store access time using address transitions close to worst case.

EXPANSION CHASSIS

OPTION



Features

- **Adds five additional card slots for:**

  Writable Control Stores
  Trace and Trace Expansion
- **Self contained**
- **Integral power supply, cooling**
- **Easy cable hookup to STEP-3**

Description

The STEP-3E Expansion Chassis allows additional capability to be added to Step-3 systems. It provides five new card slots for additional target processor memory, options such as Trace and Trace Expander, and future STEP-3 options. Any Step-3 module excepting those associated with the internal microcomputer (System Memory, Self Test, CRT, and CPU modules) can be used. An internal 5 volt 25 amp supply powers the system.

The STEP-3E Expansion Chassis sits on top of STEP-3 and is connected to it by means of two (2) fifty-conductor ribbon cables. The interconnect board occupies the sixth bottom slot in the upper box. A second interconnect board uses the top module slot in STEP-3.

The Expansion Chassis has three active control switches: ON/OFF, RESET, and WRITE PROTECT. The WRITE PROTECT SWITCH prevents the memory contents of the Writable Control Stores in the Expansion Chassis from being modified from the Step-3 instrument.

TMA

SOFTWARE

Features

- **Compatible with AMDASM**
- **Three Versions:** **Standard Fortran IV**
  Microcomputers Running CPM
  Intel MDS
- **Available on CDC timesharing service**
- **Complete cross reference tables**
- **Easy to use error listings**
- **Fully supported**
- **PROM or Microword™ output**
- **Direct interface to STEP-3 and PROM programmers**
- **Compatible with industry standards**

Description

The Transportable Meta Assembler, TMA, is a development aid for designers working on microprogrammed systems. It permits the user to generate a unique symbolic language which can then be utilized for program assembly. The TMA is compatible with AMD's AMDASM program, but comes in three versions: Standard for computers with a word length of at least 16 bits and 32k words of RAM running Fortran IV; ISIS-II for Intel® Development Systems with 64k bytes of RAM; and CPM for microcomputer systems with at least 56k bytes of RAM.

The Meta Assembler Software Package consists of three separate programs, a Definition Program, an Assembly Program, and an Output Formatter Program.

The Definition Program allows the user to define instruction memonics and their associated formats. Instruction lengths may vary from 1 to 128 bits. Symbolic constants and reserved words may also be defined in the Definition Program. An instruction format is defined by breaking the microword into fields and defining the fields as constants, don't care bits, or variables which are filled in at assembly time. Default values and certain permanent attributes may also be assigned to variable fields at Definition time. The Definition Program produces an output listing and a disk file consisting of the defined symbols and instruction mnemonics. This Definition file is used by the Assembly program as a reference when assembling a program.

The Assembly program operates like a traditional assembler. A symbolic source program utilizing the mnemonics and symbols defined in the definition Program is read as input, and a listing and object module are generated as output. The Assembler provides symbolic addressing, relative addressing, paged addressing, and other features found in typical assembly programs. The instruction syntax and assembler directives are compatible with those utilized by AMD in its literature and software products. Additional directives have been implemented to provide for versatile listing and output controls.

Conditional Assembly statements are provided in both the Definition and Assembly programs. These statements may be nested up to 16 levels and can be made dependent on general expressions. A full cross reference table is also provided in both programs.

Some features of the TMA are particularly helpful when assembling code for microprogrammable machines. The existence of don't care bits and instruction overlaying are included among these features. Bits of a microword which are not relevent to a particular instruction format may be defined as don't care bits. Don't care bits are printed as X's on the listing and do not have to be defined until the Output Formatter program is executed. An instruction format with don't care bits can be overlayed with other instruction formats. Therefore when useful, an instruction format can be used to define only part of the microword, padding out the word with don't care bits.

The Output Formatter Program reads the object module file produced by the Assembly program and translates the format into one that can be read by a PROM programmer or Step-3. Step's Microword™ format and both the BPNF and ASCII hexadecimal PROM formats are supported. Users may specify PROMs of any width and length within the object module as well as the value of don't care bits. Any or all PROMs may be listed and/or punched. To output information to Step-3 Firmware Integration and Test Station (FITS™) the object module is listed in Microword™ format over an RS232 link.

One valuable feature of the TMA is the ease of error correction. Each line in the listing is assigned a reference line number which is used for editing purposes. The error listing refers to the line number and column number, and output directives permit error messages to be listed following the line referred to, thus permitting rapid correction of source code.

TMA

CONTINUED

```
LINE          2900 KIT DEFINITIONS

    1     TITLE AM2900 KIT DEFINITIONS
    2     LIST Q
    3     LIST X
    4     !
    5     WORD 32
    6     !
    7     ! REGISTER DEFINITIONS
    8     !
    9     R0:   EQU H#0
   10     R1:   EQU H#1
   11     R2:   EQU H#2
   12     R3:   EQU H#3
   13     R4:   EQU H#4
   14     R5:   EQU H#5
   15     R6:   EQU H#6
   16     R7:   EQU H#7
   17     R8:   EQU H#8
   18     R9:   EQU H#9
   19     R10:  EQU H#A
   20     R11:  EQU H#B
   21     R12:  EQU H#C
   22     R13:  EQU H#D
   23     R14:  EQU H#E
   24     R15:  EQU H#F
   25     !
   26     ! AM2901 SOURCE OPERANDS (R S)
   27     !
   28     AQ: EQU Q#0
   29     AB: EQU Q#1
   30     ZQ: EQU Q#2
   31     ZB: EQU Q#3
   32     ZA: EQU Q#4
   33     DA: EQU Q#5
   34     DQ: EQU Q#6
   35     DZ: EQU Q#7
   36     !
   37     ! AM2901 ALU FUNCTIONS (R FUNCTION S)
   38     !
   39     ADD:  EQU Q#0
   40     SUBR: EQU Q#1
   41     SUBS: EQU Q#2
   42     OR:   EQU Q#3
   43     AND:  EQU Q#4
   44     NOTRS:EQU Q#5
   45     EXOR: EQU Q#6
   46     EXNOR:EQU Q#7
   47     !
   48     ! AM2901 DESTINATION CONTROL
   49     !
   50     QREG: EQU Q#0
   51     NOP:  EQU Q#1
   52     RAMA: EQU Q#2
   53     RAMF: EQU Q#3
   54     RAMQD:EQU Q#4
   55    RAMD: EQU Q#5
   56    RAMQU:EQU Q#6
   57    RAMU: EQU Q#7
   58    !
   59    ! SHIFT MATRIX CONTROL
   60    !
   61    SHIFT:  DEF 8X,B#0,3X,B#0,19X
   62    ROTATE: DEF 8X,B#0,3X,B#1,19X
   63    DBLROT: DEF 8X,B#1,3X,B#0,19X
   64    ARITH:  DEF 8X,B#1,3X,B#1,19X
   65    !
   66    ! NEXT MICROINSTRUCTION ADDRESS SELECT
   67    !
   68    BRFNO:      EQU H#0 !BRANCH REGISTER IF F NOT EQUAL TO ZERO
   69    BR:         EQU H#1 !BRANCH REGISTER
   70    CONT:       EQU H#2 !CONTINUE
   71    BM:         EQU H#3 !BRANCH MAP
   72    JSRFNO:     EQU H#4 !JUMP TO SUBROUTINE IF F NOT EQUAL TO ZERO
   73    JSR:        EQU H#5 !JUMP TO SUBROUTINE
   74    RTS:        EQU H#6 !RETURN FROM SUBROUTINE
   75    STKREF:     EQU H#7 !FILE REFFRENCE
   76    LOOPFNO:    EQU H#8 !END LOOP AND POP IF F=0
   77    PUSH:       EQU H#9 !PUSH AND CONTINUE
   78    POP:        EQU H#A !POP AND CONTINUE
   79    LOOPCOUT:   EQU H#B !END LOOP AND POP IF CN+4
   80    BRFEQ0:     EQU H#C !BRANCH REGISTER IF F=0
   81    BRF3:       EQU H#D !BRANCH REGISTER IF F3
   82    BROVR:      EQU H#E !BRANCH REGISTER IF OVR
   83    BRCOUT:     EQU H#F !BRANCH REGISTER IF CN+4
   84    !
   85    ! OTHER STUFF
   86    !
   87    CN0:    EQU B#0
   88    CN1:    EQU B#1
   89    LOW:    EQU B#0
   90    HIGH:   EQU B#1
   91    ZERO:   EQU B#0
   92    ONE:    EQU B#1
   93    !
   94    AM2901: DEF 9X,3VQ#1,1X,3VX,1VX,3VX,4VX,4VX,4X
   95    AM2909: DEF 4VX,4VM#2,24X
   96    DIN:    DEF 28X,4VM#
   97    !
   98    END

TOTAL DEFINITION ERRORS =     0
```

CROSS REFERENCE TABLE

LABEL	TYPE	VALUE	REFERENCES
AB	A	0000001	-29
ADD	A	0000000	-39
AM2901	D		-94
AM2909	D		-95
AND	A	0000004	-43
AQ	A	0000000	-28
ARITH	D		-64
BM	A	0000003	-71
BR	A	0000001	-69
BRCOUT	A	0000017	-83
BRF3	A	0000015	-81
BRFEQ0	A	0000014	-80
BRFNO	A	0000000	-68
BROVR	A	0000016	-82
CN0	A	0000000	-87
CN1	A	0000001	-88
CONT	A	0000002	-70
DA	A	0000005	-33
DBLROT	D		-63
DIN	D		-96
DQ	A	0000006	-34
DZ	A	0000007	-35
EXNOR	A	0000007	-46
EXOR	A	0000006	-45
HIGH	A	0000001	-90
JSR	A	0000005	-73
JSRFNO	A	0000004	-72
LOOPCOUT	A	0000013	-79
LOOPFNO	A	0000010	-76
LOW	A	0000000	-89
NOP	A	0000001	-51
NOTRS	A	0000005	-44
ONE	A	0000001	-92
OR	A	0000003	-42
POP	A	0000012	-78
PUSH	A	0000011	-77
QREG	A	0000000	-50
R0	A	0000000	-9
R1	A	0000001	-10
R10	A	0000012	-19
R11	A	0000013	-20
R12	A	0000014	-21
R13	A	0000015	-22
R14	A	0000016	-23
R15	A	0000017	-24
R2	A	0000002	-11
R3	A	0000003	-12
R4	A	0000004	-13
R5	A	0000005	-14

TMA

CONCLUDED

Software Listing

```
LINE        META ASSEMBLER TEST PROGRAM

  1   00000   TITLE     META ASSEMBLER TEST PROGRAM
  2   00000   LIST      B                              ;LIST OBJECT MODULE IN BLOCK MODE
  3   00000   NOLIST    L                              ;DO NOT LIST IN INTERLEAVED MODE
  4   000000  LIST      X,O                            ;LIST CROSS REFERENCE TABLE
  5   000000                                           ;LIST ADDRESSES IN OCTAL
  6   000000  ;
  7   000000  ; THE FOLLOWING GROUP OF STATEMENTS FORM THE EXAMPLE IN
  8   000000  ; THE AMDASM/80 MANUAL.
  9   000000  ;
 10   000000  A0:   AM2909 & AM2901 RAMF,DZ,,OR,,R0 & DIN H#F
 11   000001  A1:   AM2909 & AM2901 RAMF,DZ,,OR,,R1 & DIN 9
 12   000002  A2:   AM2909 & AM2901 RAMF,DZ,,OR,,R2 & DIN 0
 13   000003  A3:   AM2909 & AM2901 RAMF,DZ,,OR,,R4 & DIN 4
 14   000004  A4:   AM2909 & AM2901 RAMF,ZB,,AND,,R3
 15   000005  A5:   AM2909 & AM2901 ,DA,,AND,R0,R0 & DIN 1
 16   000006  A6:   AM2909 A14,JSRFNO & AM2901 RAPD,ZB,,OR,,R0
 17   000007  A7:   AM2909 & AM2901 ,DA,,AND,R1,R1 & DIN 1
 18   000010  A8:   AM2909 A14,JSRFNO & AM2901 RAPD,ZB,,OR,,R1
 19   000011  A9:   AM2909 & AM2901 ,DA,,AND,R2,R2 & DIN 1
 20   000012  A10:  AM2909 A14,JSRFNO & AM2901 RAPD,ZB,,OR,,R2
 21   000013  A11:  AM2909 & AM2901 RAMF,ZB,CN0,SUBR,,R4
 22   000014  ; NOTE THE % SIGN AFTER A5.  THE EXAMPLE IN THE AMDASM/80 MANUAL
 23   000014  ; DOES NOT SHOW THE % SIGN, AND IS IN ERROR.  WITHOUT THE
 24   000014  ; % SIGN, AN ERROR WOULD RESULT FROM PLACING A LABEL WHOSE LENGTH
 25   000014  ; IS 3 BITS INTO A 4 BIT FIELD.
 26   000014  A12:  AM2909 A5%,BRFNO & AM2901
 27   000015  A13:  AM2909 A15,BR & AM2901
 28   000016  A14:  AM2909 ,RTS & AM2901 RAMF,ZB,CN1,ADD,,R3
 29   000017  A15:  AM2909 A15, BR & AM2901 ,ZB,,OR,,R3
 30   000020  ;
 31   000020  ;
 32   000020  ; SAMPLE DIRECTIVES
 33   000020  ;
 34   000400  ORG H#100
 35   000400  LAB1: EQU 50
 36   000400  LAB3: SET LAB1
 37   000400  LAB4: SET 5+LAB1
 38   000400  LAB6: EQU LAB1*2/4+12
 39   000400  TST2: EQU 20H#1%
 40   000400  TST3: EQU 20H#1-%
 41   000400  DATA H#FFFF
 42   000401  LAB7: EQU 20(A5*2)*
 43   000401  DATA  20(A15+10)*
 44   000402  ; A 'SPACE 5' DIRECTIVE FOLLOWS, LEAVING 5 SPACES ON LISTING





 46   000402  DUP 5                                    ;DUPLICATE DIRECTIVE
 47   000402  DATA H#FFFF*
 47   000403  DATA H#FFFF*
 47   000404  DATA H#FFFF*
 47   000405  DATA H#FFFF*
 47   000406  DATA H#FFFF*
 48   000407  DATA      $                              ;LOCATION COUNTER SYMBOL
 49   000410  XLABT: SET $
 50   000410  ALIGN 4                                  ;ALIGN PROGRAM COUNTER
 51   000410  RES 10                                   ;RESERVE STORAGE
 52   000422  FF 12X,20H#12345                         ;FREE FORMAT DIRECTIVE
 53   000423            FF        32X
 54   000424  ; EXAMPLE OF CONDITIONAL ASSEMBLY
 55   000424            IF        TST2
 56   000424  BAS:      DATA      Q#20
 57   000425            AM2909
 58   000426            ELSE
 61   000426            ENDIF
 62   000426  ; EXAMPLES OF LINE CONTINUATION
 63   000426  A18:  AM2909 & AM2901 RAMU,DZ,,OR,,R0 &
 64   000426          / DIN H#F
 65   000427  A19:  AM2909 & AM2901 RAMF,DZ,,OR,,R0
 66   000427          /  & DIN H#F
 67   000430  ; DO NOT LIST NEXT 3 LINES AND THEN EJECT PAGE
 72   000433            LIST
 74   000433  ;
 75   000433  ; SAMPLE ERRORS
 76   000433  ;
 77   000433            DATA      H#100000             ;CONSTANT TOO LARGE
    ***ERROR  10 (27)
 78   000434            EQU       H#100                ;MISSING LABEL
    ***ERROR  52 ( 1)
 79   000434            ORG       100                  ;CANNOT HAVE BACKWARDS ORIGIN
    ***ERROR  11 (22)
 80   000434  TSTX:     SET       -1                   ;NEGATIVE VALUES ARE ILLEGAL
    ***ERROR  11 (21)
 81   000434            LIST      J                    ;ARGUMENT ERROR
    ***ERROR   2 (19)
 82   000434            FF        LABX,10X             ;UNDEFINED SYMBOL
    ***ERROR   5 (23)
 83   000435            DATA      B#101*-              ;CONSTANT MODIFIER ERRORS
    ***ERROR   8 (26)
 84   000436            FF        BAS,5X$,B#101        ;A FIELD CANNOT HAVE ANY MODIFIERS
    ***ERROR   2 (26)
 85   000437                                           ;DUPLICATE LABEL
 86   000437  A13:  AM2909 A15,BR # AM2901             ;ILLEGAL CHARACTER
    ***ERROR  53 ( 4)
    ***ERROR   2 (21)
 87   000440                                           ;MISSING LABEL
 88   000440          AM2909 A5,BRFNO & AM2901         ;FIELD LENGTH CONFLICT
    ***ERROR   9 (15)
 89   000441          ROTATE  &  SHIFT                 ;FORMAT OVERLAP
    ***ERROR  17 (38)
 90   000442  LABX      EQU       8                    ;ILLEGAL DIRECTIVE, FORGOT :
    ***ERROR   1 ( 4)
 91   000443  END

TOTAL ASSEMBLY ERRORS =    13
```

META ASSEMBLER TEST PROGRAM

CROSS REFERENCE TABLE

LABEL	TYPE	VALUE	REFERENCES							
A0	A	0000000	-10							
A1	A	0000001	-11							
A10	A	0000012	-20							
A11	A	0000013	-21							
A12	A	0000014	-26							
A13	A	0000015	-27	-86						
A14	A	0000016	16	18	20	-28				
A15	A	0000017	27	-29	29	43	86			
A18	A	0000426	-63							
A19	A	0000427	-65							
A2	A	0000002	-12							
A3	A	0000003	-13							
A4	A	0000004	-14							
A5	A	0000005	-15	26	42	88				
A6	A	0000006	-16							
A7	A	0000007	-17							
A8	A	0000010	-18							
A9	A	0000011	-19							
AB	A	0000001	0							
ADD	A	0000000	28							
AM2901	D		10	11	12	13	14	15	16	17
			18	19	20	21	26	27	28	29
			63	65						
AM2909	D		10	11	12	13	14	15	16	17
			18	19	20	21	26	27	28	29
			57	60	63	65	86	88		
AND	A	0000004	14	15	17	19				
AQ	A	0000000	0							
ARITH	D		0							
BAS	A	0000424	-56	84						
BM	A	0000003	0							
BR	A	0000001	27	29	86					
BRCOUT	A	0000017	0							
BRFJ	A	0000015	0							
BRFEQ0	A	0000014	0							
BRFNO	A	0000000	26							
BROVR	A	0000016	0							
CN0	A	0000000	21							
CN1	A	0000001	28							
CONT	A	0000002	0							
DA	A	0000005	15	17	19					
DBLROT	D		0							
DIN	D		10	11	12	13	15	17	19	64
			66							
DQ	A	0000006	0							
DZ	A	0000007	10	11	12	13	63	65		
EXNOR	A	0000007	0							
EXOR	A	0000006	0							
HIGH	A	0000001	0							

OBJECT MODULE

```
0000000   XXXX0010X011X111 X011XXXX00011111
0000001   XXXX0010X011X111 X011XXXX00011001
0000002   XXXX0010X011X111 X011XXXX00100000
0000003   XXXX0010X011X111 X011XXXX01000100
0000004   XXXX0010X011X011 X100XXXX0011XXXX
0000005   XXXX0010X001X101 X100000000000001
0000006   11100100X101X011 X011XXXX0000XXXX
0000007   XXXX0010X001X101 X100000100010001
0000010   11100100X101X011 X011XXXX0001XXXX
0000011   XXXX0010X001X101 X100001000100001
0000012   11100100X101X011 X011XXXX0010XXXX
0000013   XXXX0010X011X011 0001XXXX0100XXXX
0000014   01010000X001XXXX XXXXXXXXXXXXXXXX
0000015   11110001X001XXXX XXXXXXXXXXXXXXXX
0000016   XXXX0110X011X011 1000XXXX0011XXXX
0000017   11110001X001X011 X011XXXX0011XXXX
0000400   0000000000001111 1111111111111111
0000401   0000000000001111 1111111111100110
0000402   0000000000000000 0000000000000000
0000403   0000000000000000 0000000000000000
0000404   0000000000000000 0000000000000000
0000405   0000000000000000 0000000000000000
0000406   0000000000000000 0000000000000000
0000407   0000000000000000 0000000100000111
0000422   XXXXXXXXXXXX0001 0010001101000101
0000423   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0000424   0000000000000000 0000000000010000
0000425   XXXX0010XXXXXXXX XXXXXXXXXXXXXXXX
0000426   XXXX0010X101X111 X011XXXX00001111
0000427   XXXX0010X011X111 X011XXXX00001111
0000430   0000000000000000 0000000001010000
0000431   0000000000000000 0000000001010001
0000432   0000000000000000 0000000001010010
0000433   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0000434   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0000435   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0000436   100010100XXXXXXX XXXXXXXXXXXXXXXX
0000437   11110001XXXXXXXX XXXXXXXXXXXXXXXX
0000440   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
0000441   XXXXXXXX0XXX1XXX XXXXXXXXXXXXXXXX
0000442   XXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX
```

MACRO-TMA

• SOFTWARE

Features

- **Superset of TMA, in Fortran**
- **Assembles code written for TMA**
- **Complete MACRO capability**
- **Multiword per line generation**
- **Boolean and relational operators within expressions**
- **Character string manipulation**
- **Split fields**
- **Overlay of non-zero fields**
- **Column overlaying and switching in object module**
- **Single bit parity**
- **Entry point table generation**

Description

MACRO-TMA is a superset of TMA with advanced features to permit faster code generation for microprogrammed systems. Any programs written for use on TMA can be run on MACRO-TMA without modification. Versions of the program are available for mini and maxi computers with Fortran Compilers. Like TMA, MACRO-TMA consists of three separate programs: Definition, Assembly, Formatter. It provides many improvements over TMA including: macro capability, code manipulation, entry points, and English Language error messages.

PROGRAM ENTRY POINTS: In TMA there is no automatic way of generating Entry Point tables for a mapping ROM. In MACRO-TMA, a new directive, MAP, generates an object module of all entry points called out in the program.

CODE MANIPULATION: MACRO TMA allows the user to split a field to two or more subfields scattered in memory. It also contains a special operator to allow a field to replace (overlay) a second field. This permits a field shared by two different instructions to have a default condition from one instruction overlayed by code from the second instruction when present.

To make processor changes easier to handle, columns of object code can be overlayed or switched with other columns within the object module. Single bit parity can be generated across the microword and inserted into any column.

MACROS

MACRO-TMA has a complete MACRO facility which can be used to make code generation easier or generate "higher order" languages. Both recursive and nested MACROs are permitted.

MACRO expressions can be conditional with "IF" then "ELSE" construction. Assembly conditions can be based on number of expressions passed into the MACRO, on equality or non-equality of character strings or character string segments, and/or the value of variables. Boolean (and, or, shift . . .), relational (equal, not equal, greater than, . . .) and algebraic expressions can be used in the main program, as MACRO conditionals, or within a MACRO. MACRO parameters may be Symbols, Numbers, Opcodes, etc. This capability permits:

1) Multi-word microword instructions to be defined.
2) Non-Contiguous fields to be implemented.
3) Complex overlayed instructions to be coded by a single mnemonic.

MACROS can be defined in either the Definition or Assembly program, but are only expanded and checked when the Assembly program is run.

MACRO TMA

CONTINUED

```
LINE        AM2900 KIT DEFINITIONS

   1    TITLE AM2900 KIT DEFINITIONS
   2    LIST Q
   3    LIST X
   4    ;
   5    WORD 32
   6    ;
   7    ; REGISTER DEFINITIONS
   8    ;
   9    R0:   EQU H#0
  10    R1:   EQU H#1
  11    R2:   EQU H#2
  12    R3:   EQU H#3
  13    R4:   EQU H#4
  14    R5:   EQU H#5
  15    R6:   EQU H#6
  16    R7:   EQU H#7
  17    R8:   EQU H#8
  18    R9:   EQU H#9
  19    R10:  EQU H#A
  20    R11:  EQU H#B
  21    R12:  EQU H#C
  22    R13:  EQU H#D
  23    R14:  EQU H#E
  24    R15:  EQU H#F
  25    ;
  26    ; AM2901 SOURCE OPERANDS (R S)
  27    ;
  28    AQ: EQU Q#0
  29    AB: EQU Q#1
  30    ZQ: EQU Q#2
  31    ZB: EQU Q#3
  32    ZA: EQU Q#4
  33    DA: EQU Q#5
  34    DQ: EQU Q#6
  35    DZ: EQU Q#7
  36    ;
  37    ; AM2901 ALU FUNCTIONS (R FUNCTION S)
  38    ;
  39    ADD:  EQU Q#0
  40    SUBR: EQU Q#1
  41    SUBS: EQU Q#2
  42    OR:   EQU Q#3
  43    AND:  EQU Q#4
  44    NOTRS:EQU Q#5
  45    EXOR: EQU Q#6
  46    EXNOR:EQU Q#7
  47    ;
  48    ; AM2901 DESTINATION CONTROL
  49    ;
  50    QREG: EQU Q#0
  51    NOP:  EQU Q#1
  52    RAMA: EQU Q#2
  53    RAMF: EQU Q#3
  54    RAMQD:EQU Q#4
  55    RAMD: EQU Q#5
  56    RAMQU:EQU Q#6
  57    RAMU: EQU Q#7
  58    ;
  59    ; SHIFT MATRIX CONTROL
  60    ;
  61    SHIFT:  DEF 8X,B#0,3X,B#0,19X
  62    ROTATE: DEF 8X,B#0,3X,B#1,19X
  63    DBLROT: DEF 8X,B#1,3X,B#0,19X
  64    ARITH:  DEF 8X,B#1,3X,B#1,19X
  65    ;
  66    ; NEXT MICROINSTRUCTION ADDRESS SELECT
  67    ;
  68    BRFNO:      EQU H#0 ;BRANCH REGISTER IF F NOT EQUAL TO ZERO
  69    BR:         EQU H#1 ;BRANCH REGISTER
  70    CONT:       EQU H#2 ;CONTINUE
  71    BM:         EQU H#3 ;BRANCH MAP
  72    JSRFNO:     EQU H#4 ;JUMP TO SUBROUTINE IF F NOT EQUAL TO ZERO
  73    JSR:        EQU H#5 ;JUMP TO SUBROUTINE
  74    RTS:        EQU H#6 ;RETURN FROM SUBROUTINE
  75    STKREF:     EQU H#7 ;FILE REFERENCE
  76    LOOPFNO:    EQU H#8 ;END LOOP AND POP IF F=0
  77    PUSH:       EQU H#9 ;PUSH AND CONTINUE
  78    POP:        EQU H#A ;POP AND CONTINUE
  79    LOOPCOUT:   EQU H#B ;END LOOP AND POP IF CN+4
  80    BRFEQ0:     EQU H#C ;BRANCH REGISTER IF F=0
  81    BRF3:       EQU H#D ;BRANCH REGISTER IF F3
  82    BROVR:      EQU H#E ;BRANCH REGISTER IF OVR
  83    BRCOUT:     EQU H#F ;BRANCH REGISTER IF CN+4
  84    ;
  85    ; OTHER STUFF
  86    ;
  87    CN0:    EQU B#0
  88    CN1:    EQU B#1
  89    LOW:    EQU B#0
  90    HIGH:   EQU B#1
  91    ZERO:   EQU B#0
  92    ONE:    EQU B#1
  93    ;
  94    AM2901: DEF 9X,3VQ#1,1X,3VX,1VX,3VX,4VX,4VX,4X
  95    AM2909: DEF 4VX,4VH#2,24X
  96    DIN:    DEF 28X,4VH#
  97    DIN1:    DEF  28X,4VH#5
  98    ;
  99    ; DEFINE MACROS
 100    ;
 101    TABLE5:  MACRO     X,Y,Z
 102             LOCAL     LAB1
 103    Z::      DATA      H#'X                ;CONCATINATION
 104             DATA      NARG                ;NUMBER OF MACRO ARGUMENTS
 105    LAB1:    DATA      LAB1+5
 106             IF        H#'X_NE_'Y
 107             DATA      Z
 108             ELSE
 109             DATA      Y
 110             ENDIF
 111             ENDM
 112    ;
 113    MOVEB:   MACRO     X,Y,Z
 114             AM2909 & AM2901  X,Y,,OR,,RO  & DIN H#F
 115             AM2909  A14,JSRFNO
 116    ;        EXIT MACRO IF THIRD PARAMETER IS NULL
 117             IFC       Z,
 118             EXITM
 119             ELSE
 120             AM2909  &  AM2901  X,DZ,,OR,,Z
 121             ROTATE
 122             ENDIF
 123             ENDM
 124    ;
 125    END

 TOTAL DEFINITION ERRORS =    0

 CROSS REFERENCE TABLE (see sample in TMA Cross Reference table)
```

MACRO TMA

CONCLUDED

```
LINE    ADDR   META ASSEMBLER TEST PROGRAM

  1             TITLE    META ASSEMBLER TEST PROGRAM
  2             LIST     B                          ;LIST OBJECT MODULE IN BLOCK MODE
  3             NOLIST   L                          ;DO NOT LIST IN INTERLEAVED MODE
  4             MAP      0,16                       ;GENERATE ENTRY POINT MAP
  5             LIST     X,Q                        ;LIST CROSS REFERENCE TABLE
  6                                                 ;LIST ADDRESSES IN OCTAL
  7             ;
  8             ; THE FOLLOWING GROUP OF STATEMENTS FORM THE EXAMPLE IN
  9             ; THE AMDASM/80 MANUAL.
 10             ;
 11  000000     A0::   AM2909 & AM2901 RAMF,DZ,,OR,,R0 & DIN H#F
 12  000001     A1::   AM2909 & AM2901 RAMF,DZ,,OR,,R1 & DIN 9
 13  000002     A2:    AM2909 & AM2901 RAMF,DZ,,OR,,R2 & DIN 0
 14  000003     A3:    AM2909 & AM2901 RAMF,DZ,,OR,,R4 & DIN 4
 15  000004     A4:    AM2909 & AM2901 RAMF,ZB,,AND,,R3
 16  000005     A5::   AM2909 & AM2901 ,DA,,AND,R0,R0 & DIN 1
 17  000006     A6:    AM2909 A14,JSRFNO & AM2901 RAMD,ZB,,OR,,R0
 18  000007     A7:    AM2909 & AM2901 ,DA,,AND,R1,R1 & DIN 1
 19  000010     A8::   AM2909 A14,JSRFNO & AM2901 RAMD,ZB,,OR,,R1
 20  000011     A9:    AM2909 & AM2901 ,DA,,AND,R2,R2 & DIN 1
 21  000012     A10:: AM2909 A14,JSRFNO & AM2901 RAMD,ZB,,OR,,R2
 22  000013     A11:  AM2909 & AM2901 RAMF,ZB,CN0,SUBR,,R4
 23             ; NOTE THE % SIGN AFTER A5.  THE EXAMPLE IN THE AMDASM/80 MANUAL
 24             ; DOES NOT SHOW THE % SIGN, AND IS IN ERROR.  WITHOUT THE
 25             ; % SIGN, AN ERROR WOULD RESULT FROM PLACING A LABEL WHOSE LENGTH
 26             ; IS 3 BITS INTO A 4 BIT FIELD.
 27  000014     A12:  AM2909 A5%,BRFNO & AM2901
 28  000015     A13:  AM2909 A15,BR & AM2901
 29  000016     A14:: AM2909 ,RTS & AM2901 RAMF,ZB,CN1,ADD,,R3
 30  000017     A15:: AM2909 A15, BR & AM2901 ,ZB,,OR,,R3
 31  000020     DATA  LAB1_AND_H#F_SHL_2           ;BOOLEAN OPERATORS
 32             TST4:    EQU       A1_OR_A15_AND_H#9
 33             ;
 34             ;
 35             ; SAMPLE DIRECTIVES
 36             ;
 37  000400     ORG H#100
 38             LAB1: EQU 50
 39             LAB3: SET LAB1
 40             LAB4: SET 5+LAB1
 41             LAB6: EQU LAB1*2/4+12
 42             TST2: EQU 20H#1%
 43             TST3: EQU 20H#1-%
 44  000400     DATA H#FFFFF
 45             LAB7: EQU 20(A5*2)*
 46  000401     DATA  20(A15+10)*
 47             ; A 'SPACE 5' DIRECTIVE FOLLOWS, LEAVING 5 SPACES ON LISTING

 49             DUP 5                              ;DUPLICATE DIRECTIVE
 50  000402     DATA H#FFFF*
 50  000403     DATA H#FFFF*
 50  000404     DATA H#FFFF*
 50  000405     DATA H#FFFF*
 50  000406     DATA H#FFFF*
 51  000407     DATA     $                         ;LOCATION COUNTER SYMBOL
 52             XLABT: SET $
 53  000410     ALIGN 4                            ;ALIGN PROGRAM COUNTER
 54  000410     RES 10                             ;RESERVE STORAGE
 55  000422     ENTRY1:: RES       1
 56  000423     FF 12X,20H#12345                   ;FREE FORMAT DIRECTIVE
 57  000424              FF        32X
 58             ; EXAMPLE OF CONDITIONAL ASSEMBLY
 59                      IF        TST2
 60  000425     BA5:     DATA      Q#20
 61  000426              AM2909
 62                      ELSE
 65                      ENDIF
 66                      IF        LAB1_GT_60
 68                      ELSE
 69  000427              DATA      LAB1-5
 70                      ENDIF
 71                      IF        LAB1_EQ_50
 72  000430              DATA      LAB1+LAB1
 73                      ENDIF
 74             ;
 75             ; TEST MACRO CAPABILITY
 76             ;
 77             ; DEFINE A NEW MACRO THAT CALLS A MACRO DEFINED AT DEFINITION TIME
 78             MOVEA:   MACRO     X,Y,Z
 79                      MOVEB     ,Y,Z
 80                      AM2909  X,BR  &  AM2901
 81                      ENDM
 82             ;
 83             ;
 84             ; CALL SOME MACROS
 85             ;
 86                      MOVEB     RAMF,ZB
 86  000431  +           AM2909 & AM2901  RAMF,ZB,,OR,,R0  & DIN H#F
 86  000432  +           AM2909  A14,JSRFNO
 86          + ;         EXIT MACRO IF THIRD PARAMETER IS NULL
 86          +           IFC       ,
```

```
LINE    ADDR   META ASSEMBLER TEST PROGRAM

 87             ;
 88                      MOVEB     Q#1,DZ,R5
 88  000433  +           AM2909 & AM2901  Q#1,DZ,,OR,,R0  & DIN H#F
 88  000434  +           AM2909  A14,JSRFNO
 88          + ;         EXIT MACRO IF THIRD PARAMETER IS NULL
 88          +           IFC       R5,
 88          +           ELSE
 88  000435  +           AM2909  &  AM2901  Q#1,DZ,,OR,,R5
 88  000436  +           ROTATE
 88          +           ENDIF
 89             ;
 90                      TABLE5    2E,46,ENTRY2
 90  000437  + ENTRY2::       DATA      H#2E              ;CONCATINATION

 90  000440  +           DATA      NARG               ;NUMBER OF MACRO ARGUMENTS
 90  000441  + ..0000:     DATA      ..0000+5
 90          +           IF        H#2E_NE_46
 90          +           ELSE
 90  000442  +           DATA      46
 90          +           ENDIF
 91             ;
 92                      MOVEA     A8,H#55:,R6
 92          +           MOVEB     ,H#55:,R6
 92  000443  +           AM2909 & AM2901  ,H#55:,,OR,,R0  & DIN H#F
 92  000444  +           AM2909  A14,JSRFNO
 92          + ;         EXIT MACRO IF THIRD PARAMETER IS NULL
 92          +           IFC       R6,
 92          +           ELSE
 92  000445  +           AM2909  &  AM2901  ,DZ,,OR,,R6
 92  000446  +           ROTATE
 92          +           ENDIF
 92  000447  +           AM2909  A8,BR  &  AM2901
 93             ;
 94             ; EXAMPLES OF LINE CONTINUATION
 95             A18:: AM2909 & AM2901 RAMD,DZ,,OR,,R0 &
 96                    / DIN H#F
 97             A19:  AM2909 & AM2901 RAMF,DZ,,OR,,R0
 98                    /  & DIN H#F
 99             ; DO NOT LIST NEXT 3 LINES AND THEN EJECT PAGE
104                      LIST

106             ; DEMONSTRATE OVERLAY ERROR OVERRIDE ATTRIBUTE
107  000453             DIN1  &  DIN  9               ;OVERLAY ERROR
      ***OVERLAY ERROR (25)
108  000454             DIN1  &  DIN  9@              ;OVERRIDE ERROR
109             ;
110             ; SAMPLE ERRORS
111             ;
112  000455             DATA      H#100000            ;CONSTANT TOO LARGE
      ***VALUE TOO LARGE (27)
113                      EQU       H#100              ;MISSING LABEL
      ***MISSING LABEL
114                      ORG       100                ;CANNOT HAVE BACKWARDS ORIGIN
      ***ILLEGAL VALUE (22)
115             TSTX:    SET       -1                 ;NEGATIVE VALUES ARE ILLEGAL
      ***ILLEGAL VALUE (21)
116                      LIST      J                  ;ARGUMENT ERROR
      ***ARGUMENT ERROR (19)
117  000456             FF        LABX,10X           ;UNDEFINED SYMBOL
      ***UNDEFINED SYMBOL (23)
118  000457             DATA      B#101*-            ;CONSTANT MODIFIER ERRORS
      ***ATTRIBUTE ERROR (26)
119  000460             FF        BA5,5X$,B#101      ;X FIELD CANNOT HAVE ANY MODIFIERS
      ***ARGUMENT ERROR (26)
120                                                 ;DUPLICATE LABEL
121  000461    A13:  AM2909 A15,BR # AM2901          ;ILLEGAL CHARACTER
      ***DUPLICATE LABEL
      ***ARGUMENT ERROR (21)
122                                                 ;MISSING LABEL
123  000462          AM2909 A5,BRFNO & AM2901       ;FIELD LENGTH CONFLICT
      ***FIELD LENGTH CONFLICT (15)
124  000463          ROTATE  &  SHIFT               ;FORMAT OVERLAP
      ***OVERLAY ERROR (38)
125  000464    LABX     EQU       8                 ;ILLEGAL DIRECTIVE, FORGOT :
      ***ILLEGAL DIRECTIVE ( 1)
126             END


TOTAL ASSEMBLY ERRORS =   14
```

ENTRY POINT MAP

0000000	A0	0000000
0000001	A1	0000001
0000002	A5	0000005
0000003	A8	0000010
0000004	A10	0000012
0000005	A14	0000016
0000006	A15	0000017
0000007	ENTRY1	0000422
0000010	ENTRY2	0000437
0000011	A18	0000450

STEP-3

SPECIFICATIONS

MEM 32
MEM 128

SPECIFICATIONS

STEP-3 Instrument

ELECTRICAL

Power Supply	100–130 Vac @ 47–440 Hz or 200–260 Vac @ 47–440
Fuse	4.0 Amp Slo-Blo

MECHANICAL (Table top or rack mounting)

Height	7.0 inches
Width	17.65 inches
Depth	27.5 inches

ENVIRONMENAL

Operating	10 to 45°C; 0 to 90% relative humidity
Storage	-40 to 85°C; 0 to 95% relative humidity

CRT

Dimensions	5 inches measured diagonally
Viewing Area	13 square inches
Display	8 lines by 32 characters/line
Character Size	0.25 × 0.12 inches

KEYBOARD

Dimensions	14.5 inches by 3.75 inches	
Keys	Hex Keypad	16
	Control	11
	Standard	47
		74 Total

SPECIAL INTERFACES

Baud Rate	Individually programmable with data rates of 2400, 1200, 300, 150 or 110 baud, For faster baud rate, consult factory.
Stop Bits	1 or 2, individually programmable.
Parity	0, 1, EVEN, ODD
Number	One 20ma current loop, two EIA RS232 compatible, one with modem controls.
Serial Mode	Full or half duplex.

CARD CAGE

Eight-slot card cage with three slots omitted for instrument functions and Self Test. Five slots available for Writable Control Store such as MEM 32, and Options such as Trace.

CONTROLS

ON-OFF, RESET, WRITE PROTECT.

CONNECTOR TYPES

READ WRITE — BNC Connector

BREAKPOINT — BNC Connector

ADDRESS [G] — P10 26-conductor edge connector, 0.1" conductor spacing. Mating part 3M#3462-0001 or equivalent.

MEMORY OUTPUTS [G] — P11, P12 Two 40-conductor edge connectors, 0.1" conductor spacing. Mating part 3M#3464-0001 or equivalent.

MEM 32 MEMORY ORGANIZATION (D0 IS LSB)

1K × 32	D0 through D7: Least Significant Byte D24 through D31: Most Significant Byte
2K × 16	D0 through D7: 0-1K Least Significant Byte D8 through D15: 1K-2K Least Significant Byte D16 through D23: 0-1K Most Significant Byte D24 through D31: 1K-2K Most Significant Byte
4K × 8	D1 through D7: 0-1K D8 through D15: 1K-2K D16 through D23: 2K-3K D24 through D31: 3K-4K

MEM 128 MEMORY ORGANIZATION (D0 IS LSB)

4K × 32	D0 through D7: Least Significant Byte D24 through D31: Most Significant Byte
8K × 16	D0 through D7: 0-4 Least Significant Byte D8 through D15: 4K-8K Least Significant Byte D16 through D23: 0-4K Most Significant Byte D24 through D31: 4K-8K Most Significant Byte

PINOUT A OF MEM-32, MEM-128 BOARD EDGE

Conductor #	P10 [B,C]	P12 [D,E,F]	P11 [D,E,F]
1	A0	D0	D16
3	A1	D1	D17
5	A2	D2	D18
7	A3	D3	D19
9	A4	D4	D20
11	A5	D5	D21
13	A6	D6	D22
15	A7	D7	D23
17	A8	E00	E02
19	A9	E10	E12
21	A10	D8	D24
23	A11	D9	D25
25	UL	D10	D26
27	—	D11	D27
29	—	D12	D28
31	—	D13	D29
33	—	D14	D30
35	—	D15	D31
37	—	E01	E03
39	—	E11	E13

Notes: A. Even-Numbered Pins: GND
B. UL = User Latch Input (Breakpoint Qualifier)
C. Ax = Address Input
D. Dx = Data Output
} 0 = LS Bit
E. Elx = Enable Input (8 bits of data)
F. EOx= Enable Output (from STEP-3)
} 0 = LS Byte
G. Standard terminations are 3M#3399 (Address) and two 3M#3421 (Data)

MEM 32, 128

SPECIFICATIONS

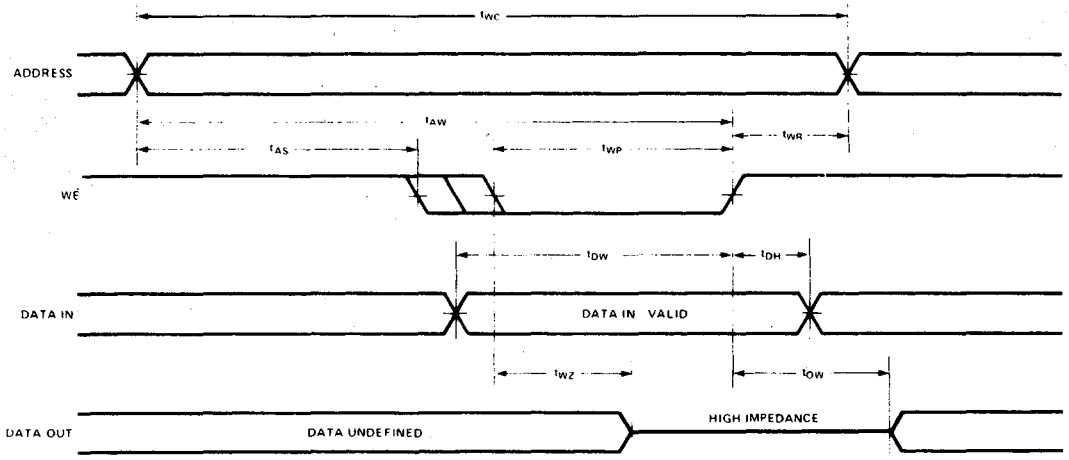
DC CHARACTERISTICS (TA = 0 to 45° C)

Parameter	Test Conditions	INT-1 Min	INT-1 Max	INT-2 Min	INT-2 Max	INT-3,4,5 Min	INT-3,4,5 Max	Units
ADDRESS & ENABLE LINES								
"0" Input Current	V_{IN} = 0.45 V		−400		−400		−400	μA
"1" Input Current	V_{IN} = 2.7 V		50		50		50	μA
"0" Input Voltage			0.8		0.8		0.8	V
"1" Input Voltage		2		2		2		V
Input Hysteresis		0.2		0.2		0.2		V
Input Clamp Voltage	I_{IN} = 18 mA		−1.5		−1.2		−1.2	V
DATA LINES								
"0" Output Voltage	I_{OUT} = 20 mA[D]		0.5		0.5		0.5	V
"1" Output Voltage	I_{OUT} = −6.5 mA[D]	2.4		2.4		2.4		V
Output Short Circuit Current[B]	V_{OUT} = 0 V		−30	−40	−225		−100	mA
Output Leakage Current	Tristate				+10		±50	μA
					−200			

Notes: A. Positive current defined as into terminal referenced.
B. No more than one output should be grounded at a time.
C. Manufacturer reserves the right to make design and process changes and improvements.
D. 1 mA for INT-1 interface, 3 mA for INT-2 interface.

AC CHARACTERISTICS

WRITE CYCLE



WRITE CYCLE (Assumes Interface INT-1, Resistive Termination)

Symbol	Parameter	MEM-32F Min	MEM-32F Max	MEM-32A Min	MEM-32A Max	MEM-128F Min	MEM-128F Max	MEM-128A Min	MEM-128A Max	MEM-128B Min	MEM-128B Max	Unit
t_{WC}	Write Cycle Time	65		75		75		90		180		ns
T_{AW}	Address Valid To End of Write	55		65		40		50		155		ns
t_{AS}	Address Setup Time	10		10		10		10		20		ns
t_{WP}	Write Pulse Width	45		55		55		70		150		ns
t_{WR}	Write Recovery Time	15		20		10		20		15		ns
t_{DW}	Data Valid to End of Write	35		35		30		30		60		ns
t_{DH}	Data Hold Time	20		20		20		20		15		ns
t_{WZ}	Write Enabled to Output in High Z	0	35	20	35	0	30	0	40	10	85	ns
t_{OW}	Output Active from End of Write	20	40	25	40	5		5		5		ns

MEM 32-128

CONCLUDED

AC Characteristics (cont'd)

BREAKPOINT

	Min	Typ	Max	Unit
Address Input to Breakpoint Output		60	70	ns
Max Address Skew for "Glitchless Output"	4	6		ns

MEMORY READ MEM 32

Symbol	Parameter	MEM TYPE	INT-1 Max	INT-2 Max	INT-3[C] Min	INT-3[C] Max	INT-4[D] Min	INT-4[D] Max	INT-5 Max	Unit
T_{PHL}, T_{PLH}	Address Access Time[A]	F	36	48		58		54	49	ns
T_{PHL}, T_{PLH}	Address Access Time[A]	A	45	57		67		63	58	ns
T_{ZL}, T_{ZH}	Enable to Output Delay	all		40		25		25	25	ns
T_{HZ}, T_{LZ}	Output Disable Time	all		25		20		20		ns
T_W	Latch Clock Width	all			10		10			ns
T_S	Data Setup Time[B]	all			5↑		0↓			ns
T_H	Data Hold Time[B]	all			2↑		10↓			ns

MEMORY READ MEM 128

Symbol	Parameter	MEM TYPE	INT-1 Max	INT-2 Max	INT-3[C] Min	INT-3[C] Max	INT-4[D] Min	INT-4[D] Max	INT-5 Max	Unit
T_{PHL}, T_{PLH}	Address Access Time[A]	F	50	62		72		68	63	ns
T_{PHL}, T_{PLH}	Address Access Time[A]	A	70	82		92		88	83	ns
T_{PHL}, T_{PLH}	Address Access Time[A]	B	180	195		205		199	195	ns
T_{ZL}, T_{ZH}	Enable to Output Delay	all		40		25		25	25	ns
T_{HZ}, T_{LZ}	Output Disable Time	all		25		20		20		ns
T_W	Latch Clock Width	all			10		10			ns
T_S	Data Setup Time[B]	all			5↑		0↓			ns
T_H	Data Hold Time[B]	all			2↑		10↓			ns

Notes:

A. Worst case address to data transition utilizing a galloping pattern (GALPAT).

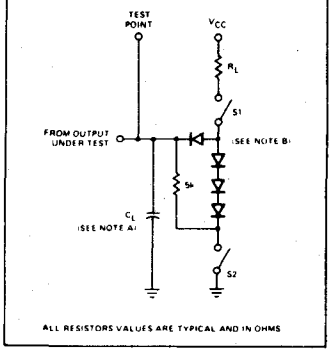
B. Arrow indicates transition of latch input used for reference:
↑ for the low-to-high transition.
↓ for the high-to-low transition.

C. Access time includes data setups on register.

D. Worst case access: clock goes low after data sets up.

PARAMETER MEASUREMENT INFORMATION

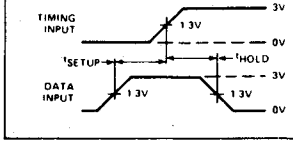
TEST LOAD CIRCUIT



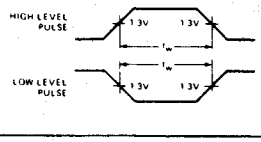
	INT-1	INT-2	INT-3,4,5
C_L	5	50	15
R_L	1K	90	280

VOLTAGE WAVEFORMS

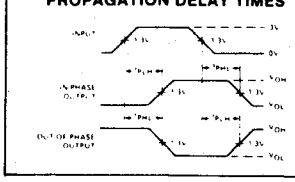
SETUP AND HOLD TIMES



PULSE WIDTHS



PROPAGATION DELAY TIMES

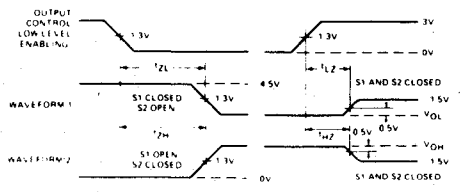


NOTES

A. C_L includes probe and jig capacitance in pF.

B. All diodes are 1N916 or 1N3064.

ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



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Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Input Voltage	-1 to 5.5V	Stresses above, and extended time at, absolute maximum rating may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.
Output Current	150ma	
Storage Temp.	-45° to 75°C	

ROM 4/8

SPECIFICATIONS

D.C. CHARACTISTICS Ta-0 to 45°C[F]; 4.75V≤ V_{CC} ≤5.25V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
"0" Input Current (CS only)	Vin = .50V			2	ma
"0" Input Current	Vin = .50V			-400	μa
"1" Input Current	Vin = 2.7V			50	μa
"0" Input Voltage		.85			V
"1" Input Voltage				2.0	V
"0" Output Voltage	1out = 40 ma	.5			V
Output Short Circuit Current[B]	Vout = OV			-30	ma
"1" Output Voltage	Iout = -6.5ma	2.4			V
Output Leakage Current				±50	μa
Input Clamp Voltage	Iin = 5.0ma			-1.0	V
Input Impedance (Address lines)			100		Ohms
Input Capacitance[G]	Vin = 2.0V		35		pf
Output Capacitance[D,E]	Vin = 2.0V		40		pf
Power Supply Current				200	ma

AC CHARACTISTICS

Calculation of Worst Case Access Time, WCAT, at the Memory Socket:

WCAT = TAA + 3.5ns × L + TD

where TAA = Worst Case memory access time from the data sheet

L = Length of cable + 1.5 feet

TD = Delay through ROM simulation module

SYMBOL	PARAMETER	MAX VALUE TS	L	R	UNIT
TD	Delay through ROM Simulation module	15	20	20	ns
TZL, TZH	Enable to Output Delay	25	25	25	ns
TLZ, THZ	Output Disable Time	20	20	20	ns
TW	Latch Clock Width	--	20	20	ns
TS	Data Setup Time	--	0	5	ns
TH	Data Hold Time	--	10	2	ns

TS = Tristate; L = Latching; R = Register

* For voltage waveforms, see page 20

NOTES:
A. Positive current is defined as into the terminal referenced.
B. no more than one output should be grounded at the same time.
C. Manufacturer reserves the right to make design and process changes and improvements.
D. All characteristics include the effect of the 12" cable between the buffer card and test signal.
E. Power off.
F. For high temperature operation to 125°C consult factory.
G. Input capacitance on slave address lines: 5pf typical.

TRACE

SPECIFICATIONS

TRACE OUTPUTS

(Available on BNC connectors at board edge)

TRACE TRIGGERED TG — A positive true signal available 3 to 5 processor cycles (depending on trigger mode), plus 25ns after a valid trigger condition has occured. The signal state is indicated on the CRT. TG can be used to trigger an external logic analyzer, or halt the target processor.

TRACE DONE TD — A positive true signal available 3 to 5 processor cycles (depending on trigger mode) plus 25ns after a Trace has been completed. The signal state is indicated on the CRT. TD can be used to halt the target procesor.

TRACE INPUTS

SIGNAL NAME	INPUT FROM	SIGNAL DEFINITION
A1 thru A9	Master ROM Buffer assembly	Least significant address inputs
(A10, A11)[6]		
(A10, A11)[6]	Address Probe	Address input
A12 thru A15	Address Probe	Most significant address input
UAC[1]	Address Probe	User address clock
EE[2]	Address Probe	External enable to trace operation
TQ1[2,3,5]TQ2[2,3,5]	Address Probe	External Trigger inputs
D0 thru D7	Data Probe 1[5]	Least significant external data inputs.
UDC[1]	Data Probe 1[5]	User data clock
UCTL1	Data Probe 1[5]	User display input for XSTATE™
D8 thru D15	Data Probe 2[5]	Most significant external data inputs.
UDC[1,4]	Data Probe 2[5]	User data clock
UCT2	Data Probe 2[5]	User done input for XSTATE™
D16 thru D63[7]	Data Probe 3-8[5]	Data Inputs[8]

NOTES:
1. Clock edge used to latch data, positive or negative, is individually switch programmable.
2. Logical true input level is individually switch programmable, positive or negative.
3. Clock input, UAC or UDC, used to strobe signal is individually selectable.
4. Used only to synchronously latch data; not used for internal timing.
5. Use of this input is optional; to run, Trace needs only UAC and the least significant addresses.
6. A10, A11 input can be obtained from either the Master ROM assembly or Address Probe. Jumpers on the Trace Board select the source.
7. Only available on Trace Expander Board.
8. Each group of 8 input bits has its own clock input and latch circuitry.

AC SPECIFICATIONS

Setup time (TSU) and hold time (THD) from active clock edge.

	SWITCH-SELECTABLE CLOCK EDGE (POS OR NEG)				WIRED POSITIVE CLOCK EDGE			
	TSU		THD		TSU		THD	
	TYP	MAX	TYP	MAX	TY	MAX	TYP	MAS
ADDRESS	-12*	-4*	15	25	-4*	2	8	25
DATA	-4*	2	8	12.5	3	5	1	2
EE	30	45			-	-	-	-

*data may arrive after the clock

Minimum clock width (high or low): 25ns

Trace Cycle Time: 90ns guaranteed, 80ns typical.

EXPANSION CHASSIS

SPECIFICATIONS

SPECIFICATIONS— STEP-3E EXPANSION CHASSIS

ELECTRICAL

Power Supply	100-130 Vac @ 47-440 Hz or 200-260 Vac @ 47-440 Hz
Fuse	2.5 amp Slo-Blo

MECHANICAL

Height	5.25 inches
Width	17.65 inches
Depth	20.0 inches

ENVIRONMENAL

Operating	1 to 45°C; 0 to 90% relative humidity
Storage	-40 to 85°C; 0 to 95% relative humidity

CARD CAGE

Six-slot, card cage with one slot committed for interconnect. Five slots available for Writable Control Stores such as MEM 32, and Options.

CONTROLS

ON-OFF, RESET, WRITE PROTECT.

INTERCONNECT

Two (2) fifty (50) conductor ribbon cables approximately 6 inches in length.

SELF TEST

SPECIFICATIONS

ACCESS TIME:	2-254ns in 2ns increments
ACCURACY:	± 3ns or 5% whichever is greater
OUTPUT:	12 Address lines, 4 enable lines BRK, Write, 32 data lines
INPUT:	32 Data lines, 4 enable lines, 1 BREAKPOINT
CARDSLOT:	Uses 1 of the 3 dedicated instrument card slots.

STEP-3

ORDERING INFORMATION

STEP-3, MEM-32, MEM-128

Step-3, MEM-32, and MEM-128 are ordered and priced as a system

Part No.	Description
Step-3/ nMEM-abc/ nMEM-abc	Step-3 Firmware Integration and Test Station with n MEMabc Writable Control Stores and m MEMa Writable Control Stores

MEM-32, MEM-128

Part No.	Description
n MEM-a b c	High speed Writable Control Store, WCS, for use in Step-2 and Step-3. Example: MEM-128F3.

- c — WCS, interface option per chart below. If no interface is specified, interface 1 is assumed.
- b — WCS, speed designator per chart below.
- a — Memory type: 32 or 128.
- n — quantity of memory boards being ordered.

WCS SPEED DESIGNATOR CHART

	F	A	B
MEM-32	36ns	45ns	—
MEM-128	50ns	70ns	180ns

WCS INTERFACE CHART

INT-1 Unbuffered output with 51-ohm series terminations for cable driving. The output should not be connected to more than one TTL load and cannot be wire-ORed. Used with ROM EMULATOR OUTPUTS to plug directly into system ROM sockets.. (INT-1 is supplied as standard.)

INT-2 Bidirectional buffered tristate output with outputs capable of wire-ORed configuration. Each group of eight bits has its own enable input. IC used: 74LS245. This is a special-order option.

INT-3 Buffered tristate output with edge-triggered latches for direct use in pipeline organizations. IC used: 74S374.

INT-4 Buffered tristate output with transparent latch. Outputs are capable of wire-ORed operation. IC used: 74S373.

INT-5 Buffered tristate output without latch. Outputs are capable of wire-ORed operation. IC used: 74S373.

Example: Step-3/ 2 MEM-32F/ 1 MEM-128A

- Step-3 — Specifies Step-3
- 2 MEM-32F — Specifies 2 WCS type MEM-32F, interface 1
- 1 MEM-128A — specifies an additional WCS type MEM-128A, interface 1

SELF TEST

Part No.	Description
Step-3S	Self Test module for WCS and ROM Simulation test and access time measurement. Includes PG board.

TRACE

Part No.	Description
Step-3T	Trace option, 32 bits, 11 MHz, with probes.
Step-3TE	Trace expansion option, 48 bits, 11 MHz, with probes, Must be used with Step-3T above.

EXPANSION CHASSIS

Part No.	Description
Step-3E	Step-3 six slot Expansion Chassis with integral power supply.

TMA

TMA-M-STD	TMA, for all mini and maxi computers. Fortran IV version, supplied on magnetic tape. Tape is unblocked, 80 character records. —Specify ASCII or EBCDIC, 800 or 1600 BPI
TMA-F-RT11	TMA, for use with PDP-11/LSI-11 computers utilizing RT11 operating system with Fortran IV. Supplied on RX01 compatible floppy diskette.
TMA-D-RT11	TMA, RT11 version for DEC computers or RK05 disk pack.
TMA-M-DOS	TMA, DOS format for PDP-11 computers with magnetic tape drives. —Specify 800 or 1600 BPI.
TMA-M-RSX11M	TMA, source and object code directly compatible with PDP-11 computers utilizing RSX11M operating system. Supplied on magnetic tape. —Specify 800 or 1600 BPI.
TMA-D-RSX11M	TMA, object and source code for DEC computers running RSX11M operating system. Furnished on RK05 disk pack.
TMA-F-RSX11M	TMA, source and object code directly compatible with PDP-11 computers utilizing RXS11M operating system. Supplied on RX01 compatible floppy diskette.

MACRO-TMA

MACRO-TMA-M-STD	MACRO-TMA for all mini and maxi computers, Fortran IV version, supplied on magnetic tape. Tape is unblocked, 80 character records. —Specify ASCII or EBCDIC, 800 or 1600 BPI.
MACRO-TMA-M-RSX11M	MACRO-TMA, source and object code directly compatible with PDP-11 computers. Utilizing RSX11M operating system. Supplied on magnetic tape. —Specify 800 or 1600 BPI.
MACRO-TMA-F-RT11	MACRO-TMA, for use with PDP-11/LSI-11 computers utilizing RT11 operating system with Fortran IV. Supplied on RX01 compatible floppy diskette.

ROM SIMULATION

A ROM module order should contain the following information:

1. Part Number; Example: ROM 8G/48
   - 48 — Number of memory bits being simulated rounded up to the nearest multiple of 16.
   - G — ROM type per chart. If the proper Rom type is unknown at order entry time use "X".
   - 8 — ROM organization, 4 or 8 bits.
2. Manufacturer's part number for actual ROM or PROM, if known.
3. Total memory size, example 1k × 48.
4. Type of memory board: MEM-32 or MEM-128.
5. Cable length if different than 3 feet (standard).

If additional ROM modules need to be ordered to supplement an existing set, append an "S" (for slave) to the part number. Example: ROM 8G/16S specifies an additional 16 bits of ROM simulation. A ROM 8G/48 plus a ROM 8G/16S is equivalent to a ROM 8G/64.

All ROM simulation orders except those with an "S" suffix are shipped with spare master.

APPENDIX B

MEMORY ORGANIZATIONS

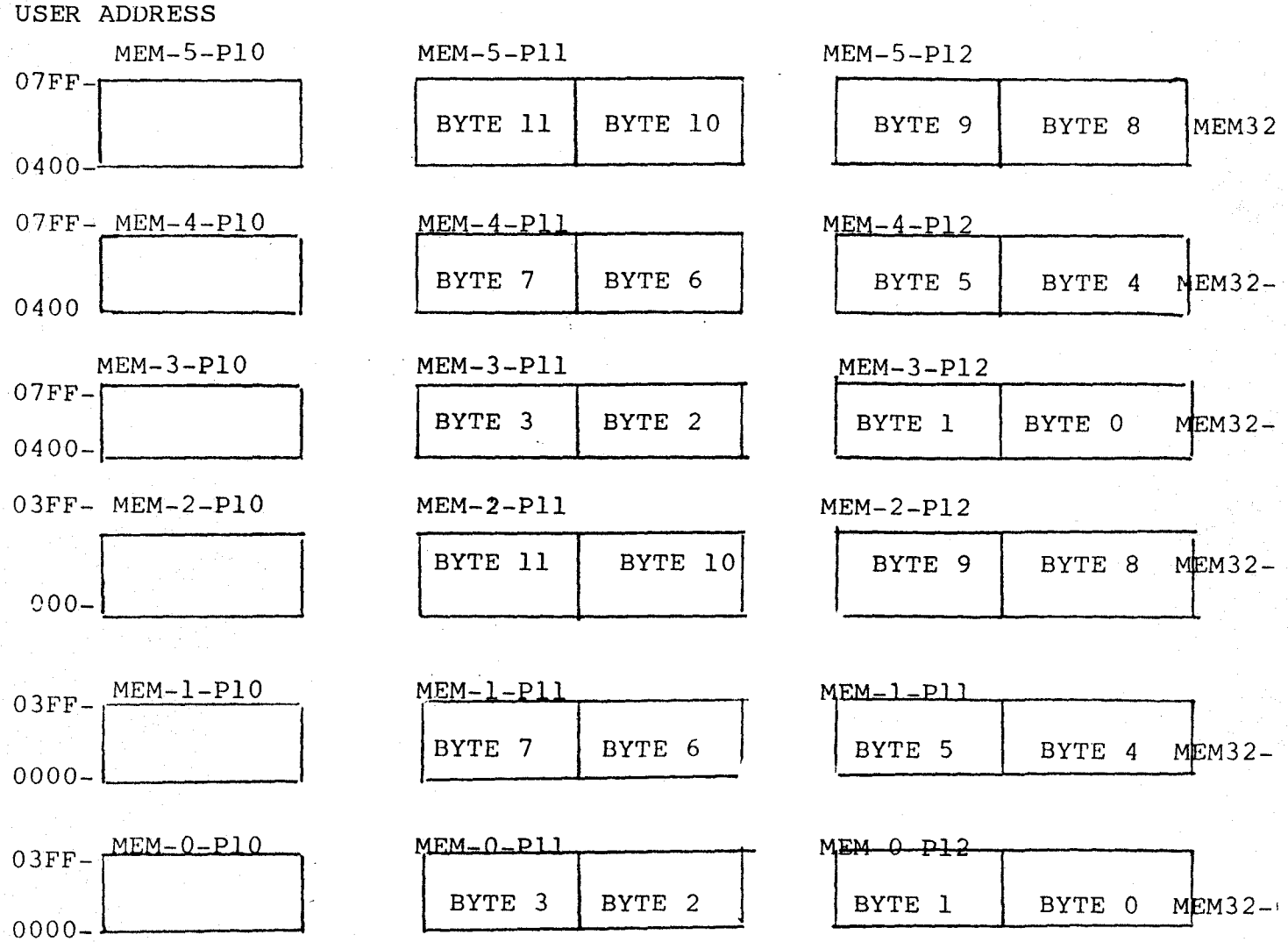


TABLE B-1 User Interface Data Mapping for MEM32

32 bit org. switches

Max organization 2kx(68-96) bits/word

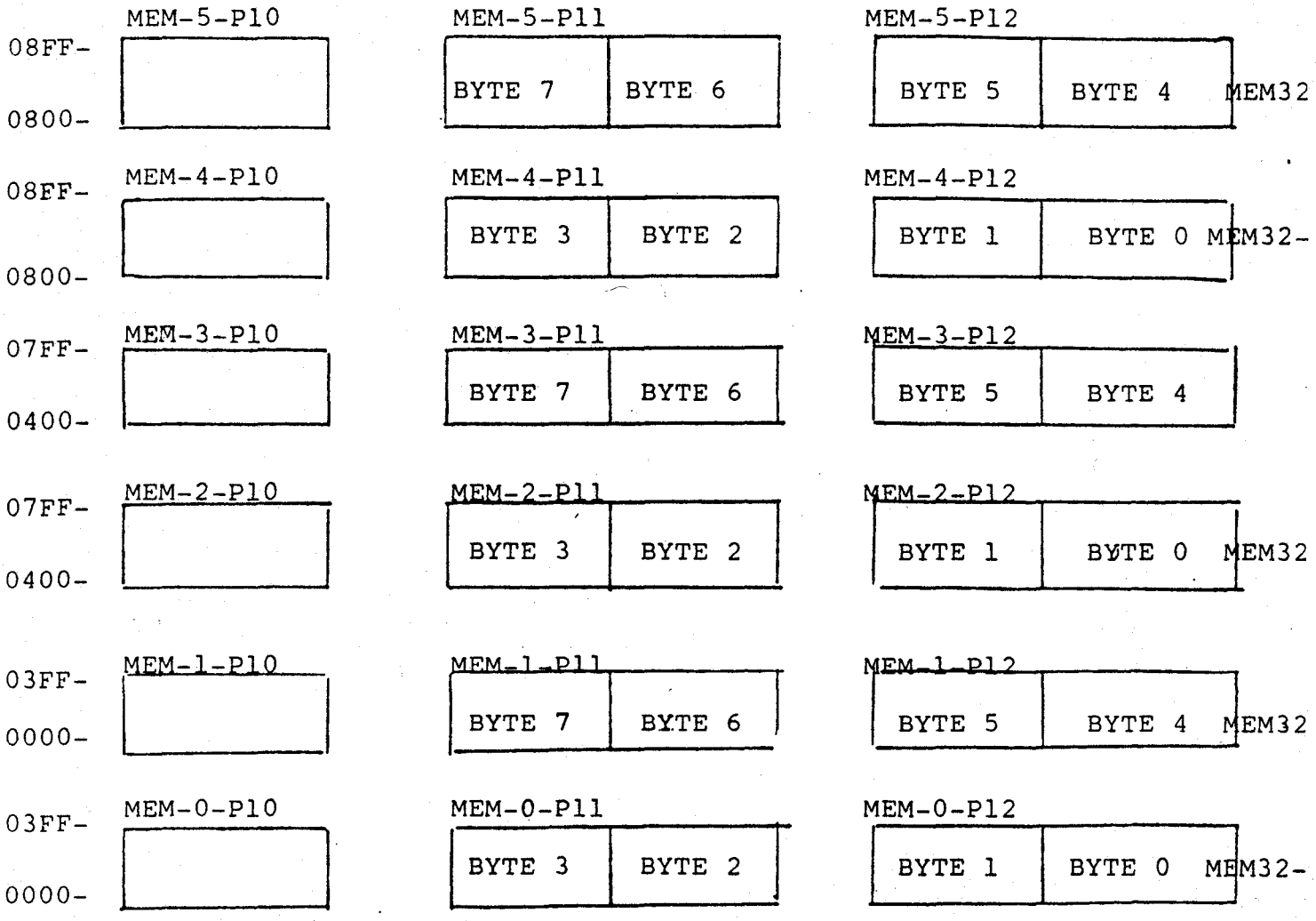


TABLE B-2 User Interface Data Mapping for MEM32
32 bit org. switches
Max organization 3kx (36-64) bits/word

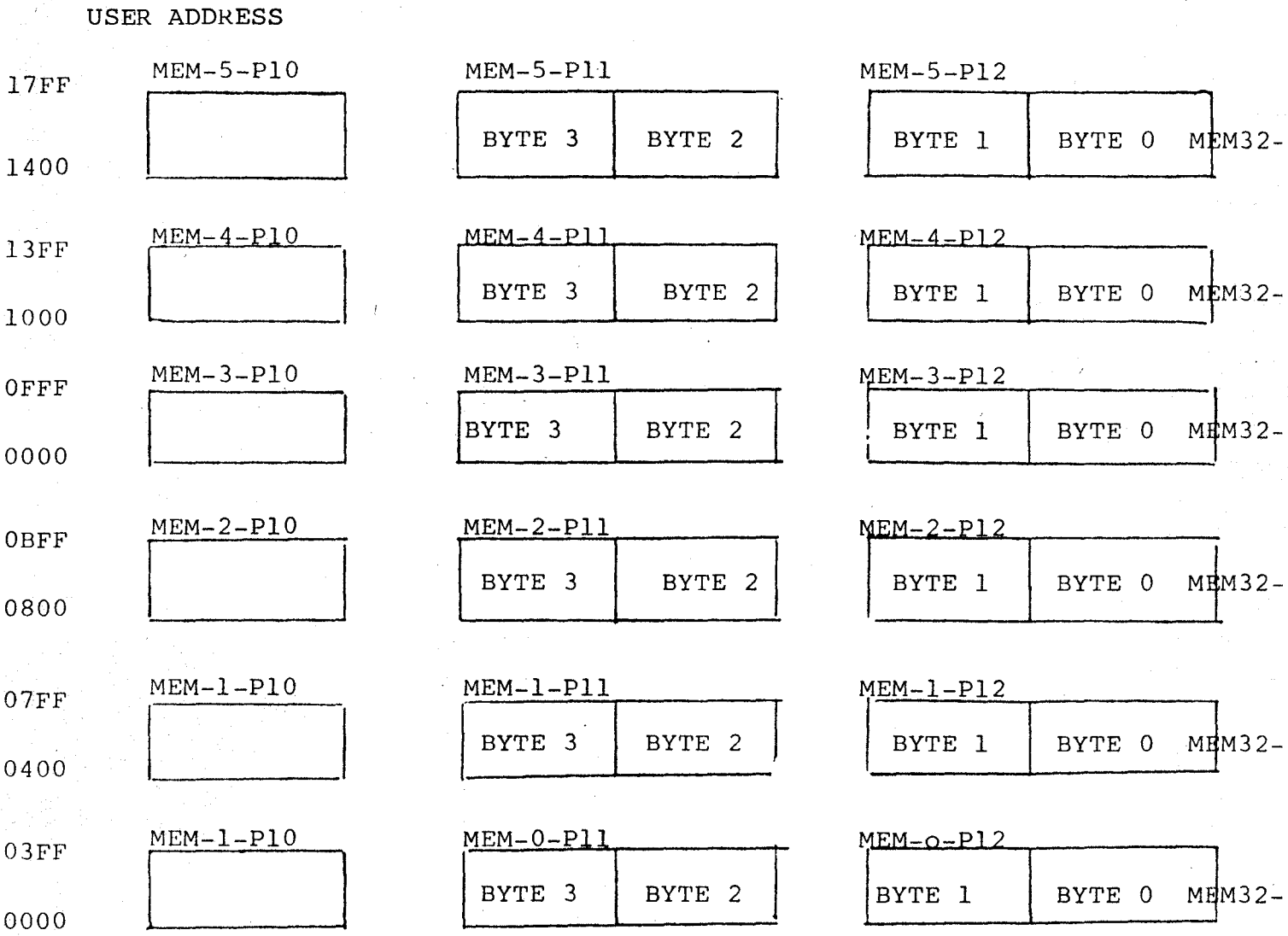


TABLE B-3 User Interface Data Mapping for MEM32

32 bit org switches

max organization 6kx (8-32) bits/word

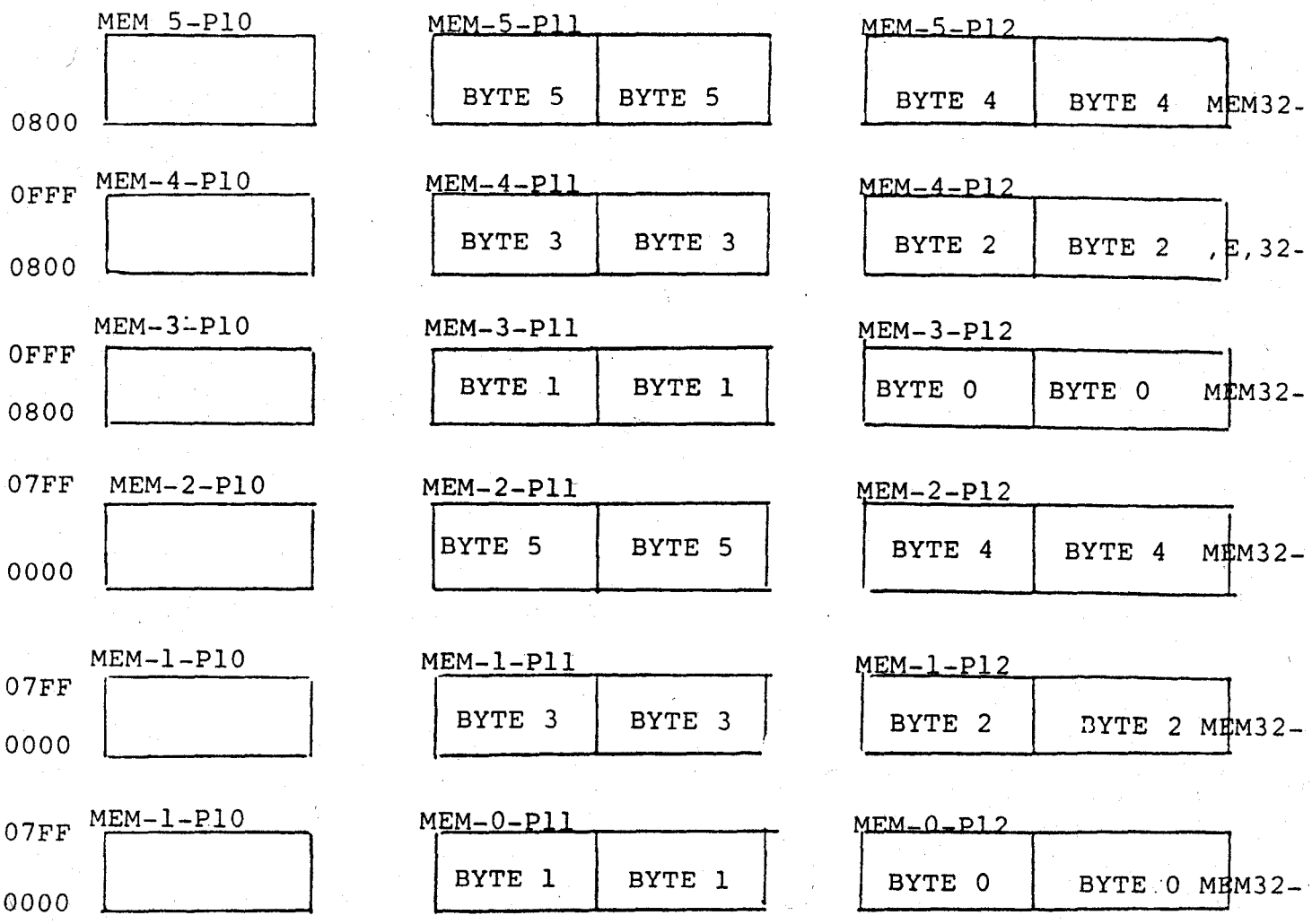


TABLE B-4 User Interface Data Mapping for MEM 32
16 bit org switches

max organization 4kx (36-48) bits/word

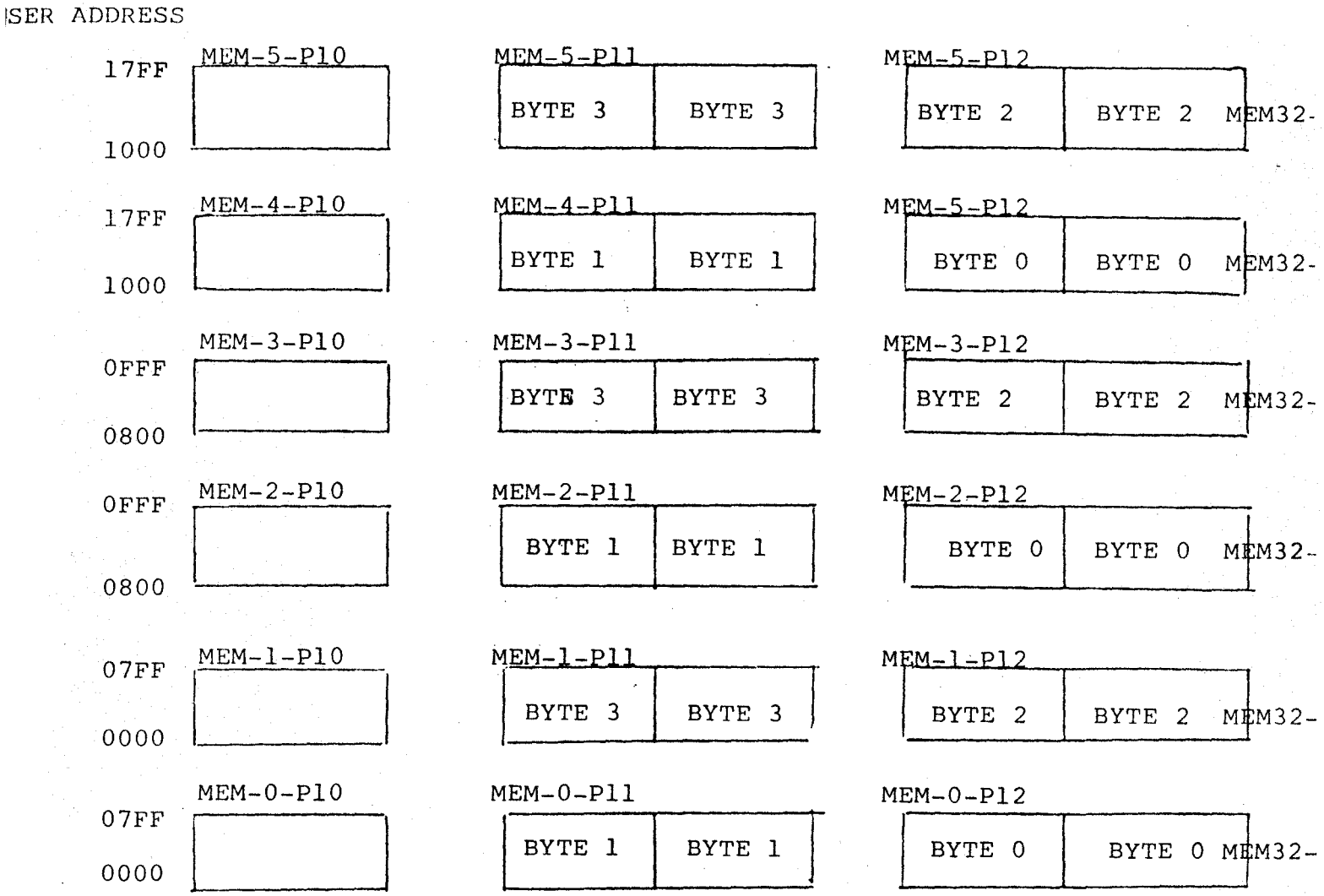


TABLE B-5 User Interface Data Mapping for MEM 32

16 bit switches

Max Organization 6kx (20-32) bits/word

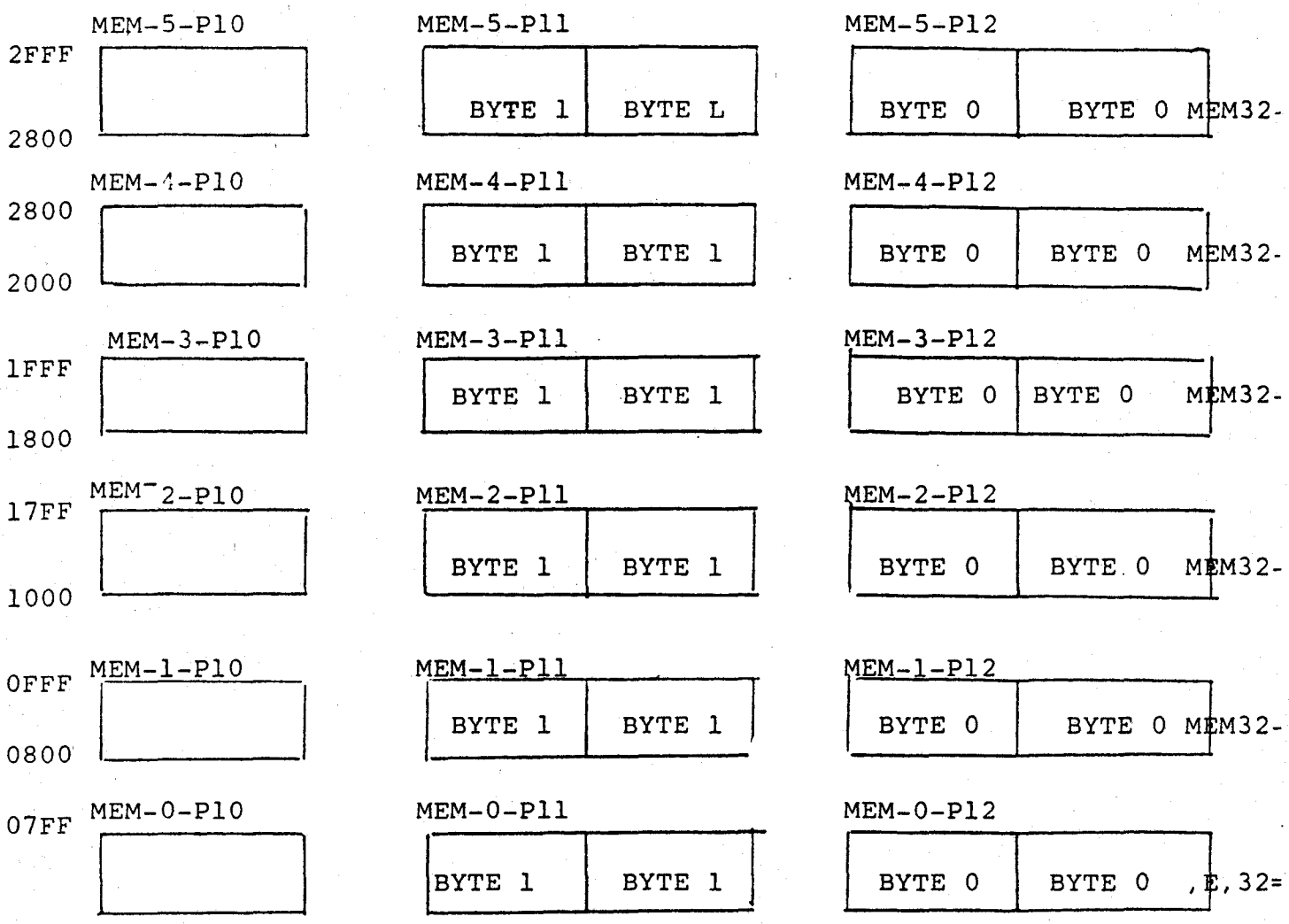


TABLE B-6 User Interface Data Mapping for MEM 32

16 bit org. switehces

Max Organization 12kx (8-16) bits/word

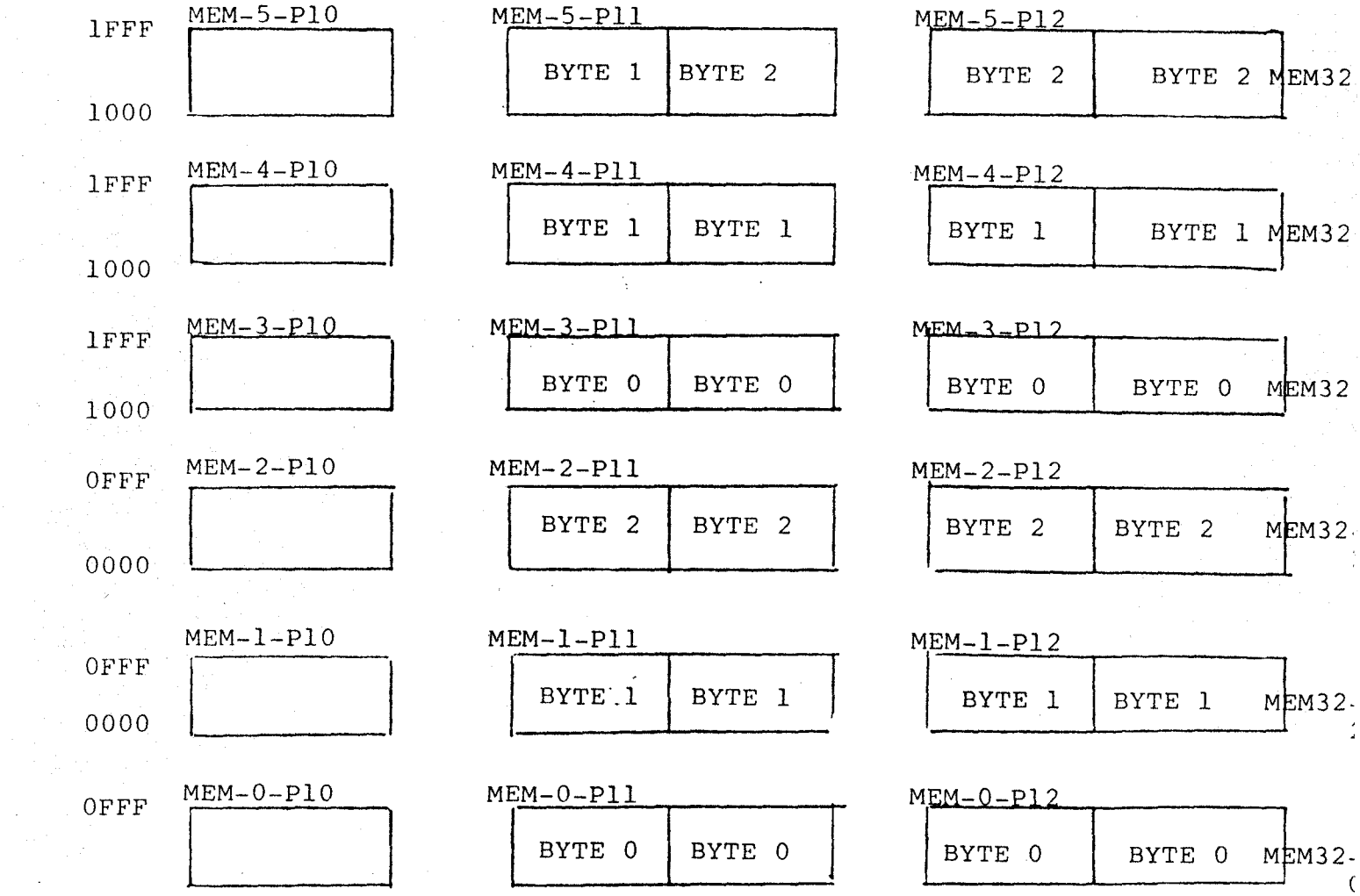


TABLE B-7 User Interface Data Mapping for MEM32

8 Bit org Switches

Max Organization 8kx (20-24) bits/word

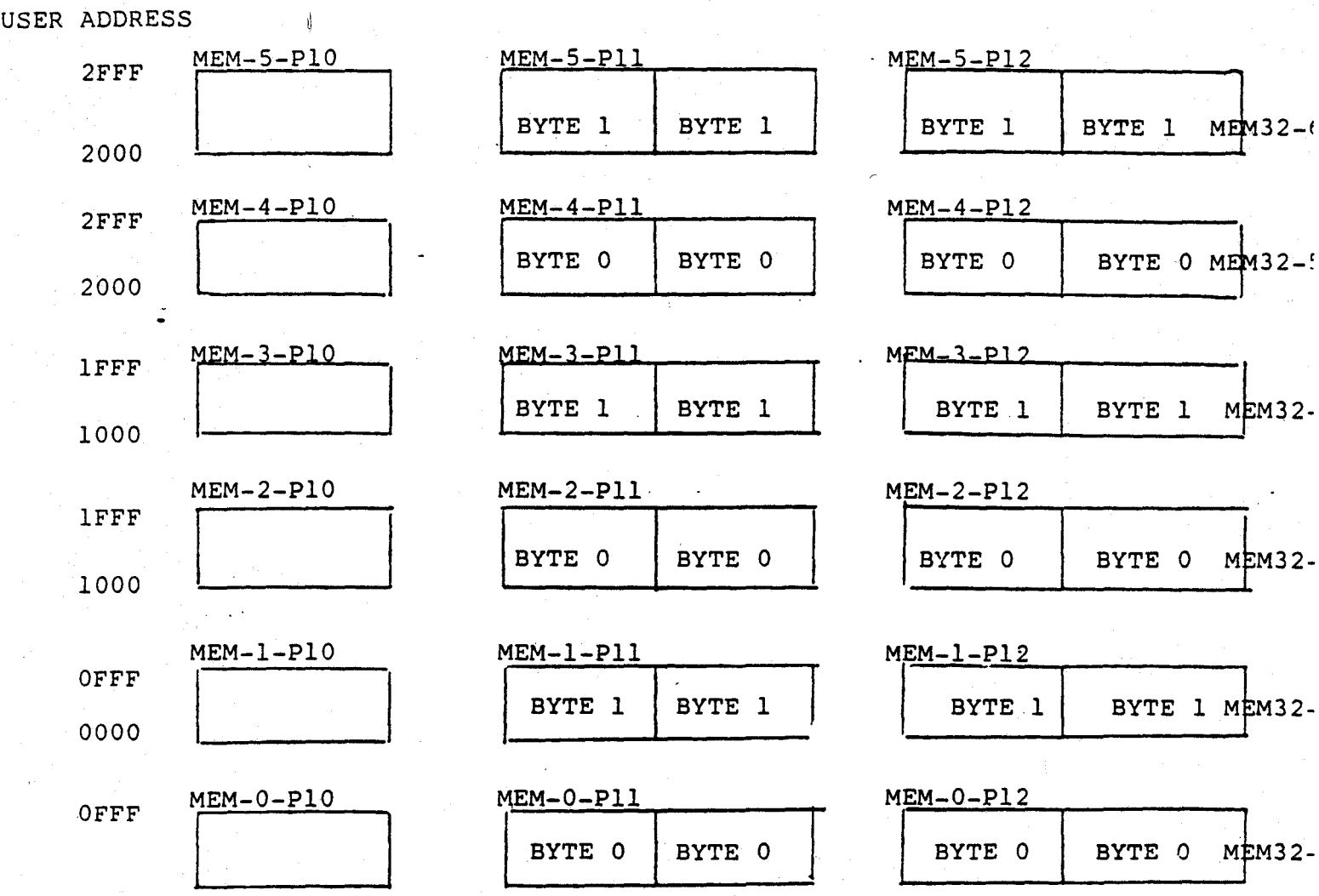


TABLE B-8 User Interface Data Mapping for MEM32

8 Bit Org Switches

Max Organization 12kx (12-16) bits/word

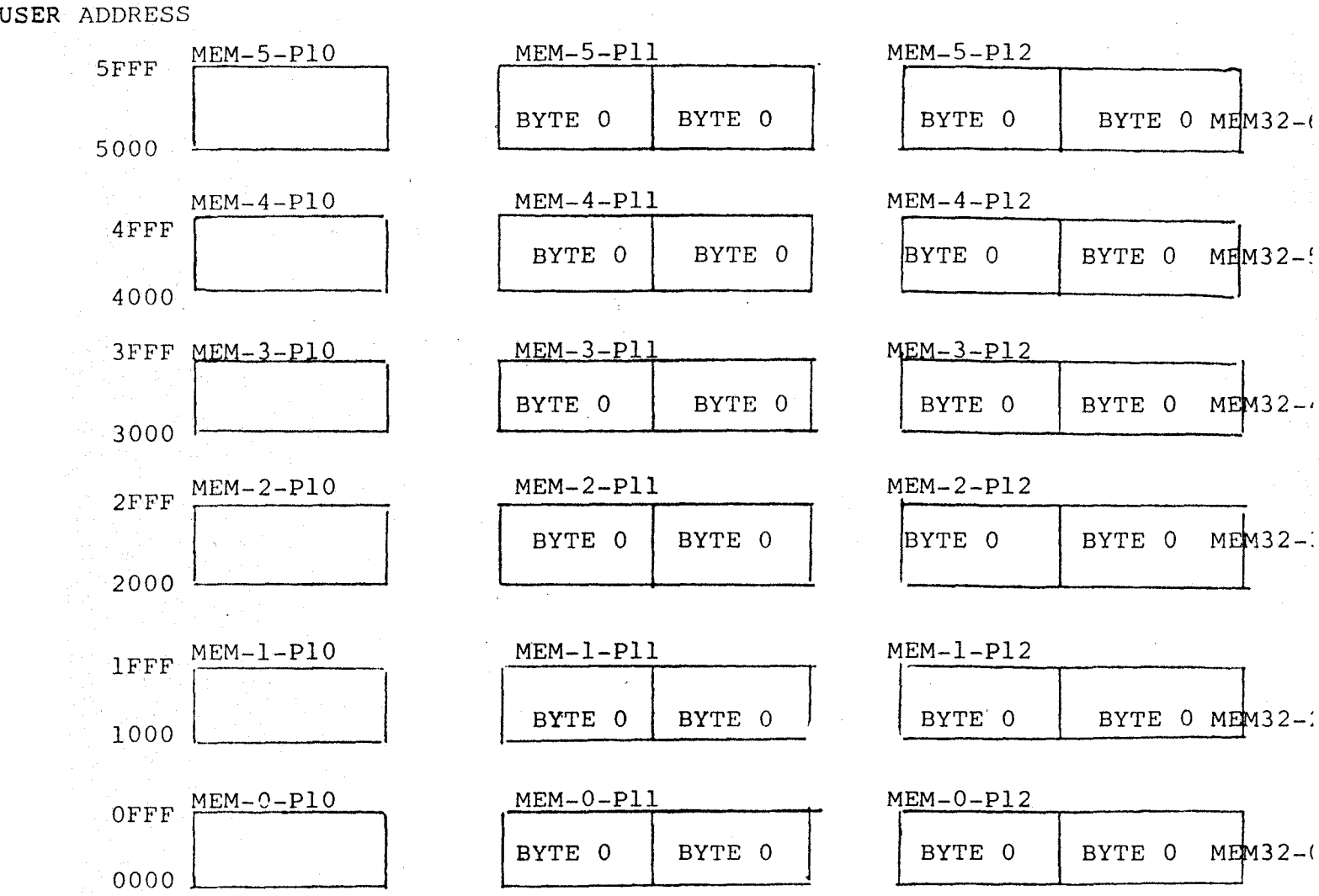


TABLE B-9 User Interface Data Mapping for MME 32

8 Bit Org Switches

Max Organization 24k x 8 Bits/word

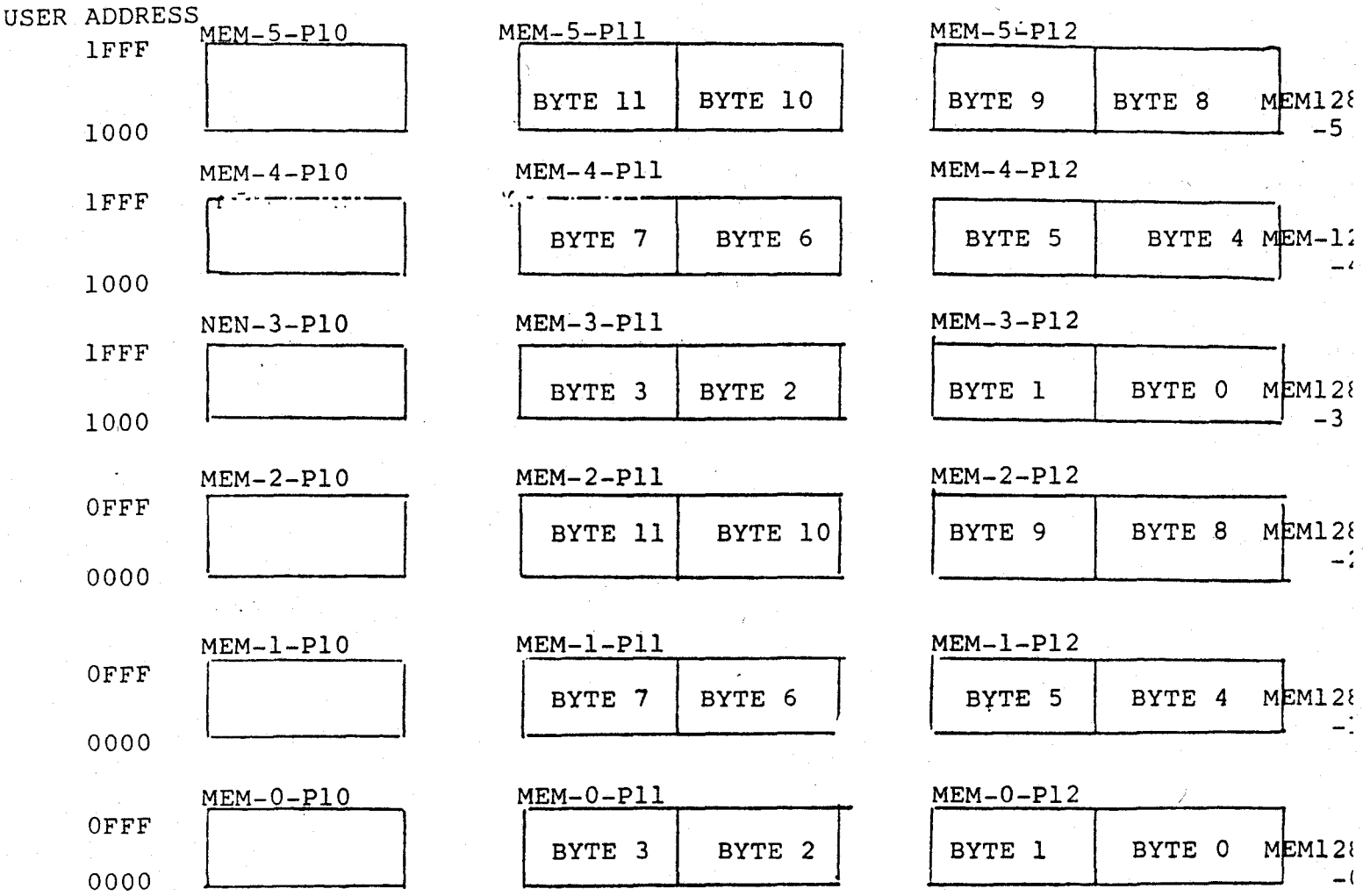


TABLE B-10 User Interface Data Mapping MEM 128
32 Bit Switches

Max Organization 8KX(68-96) bits/word

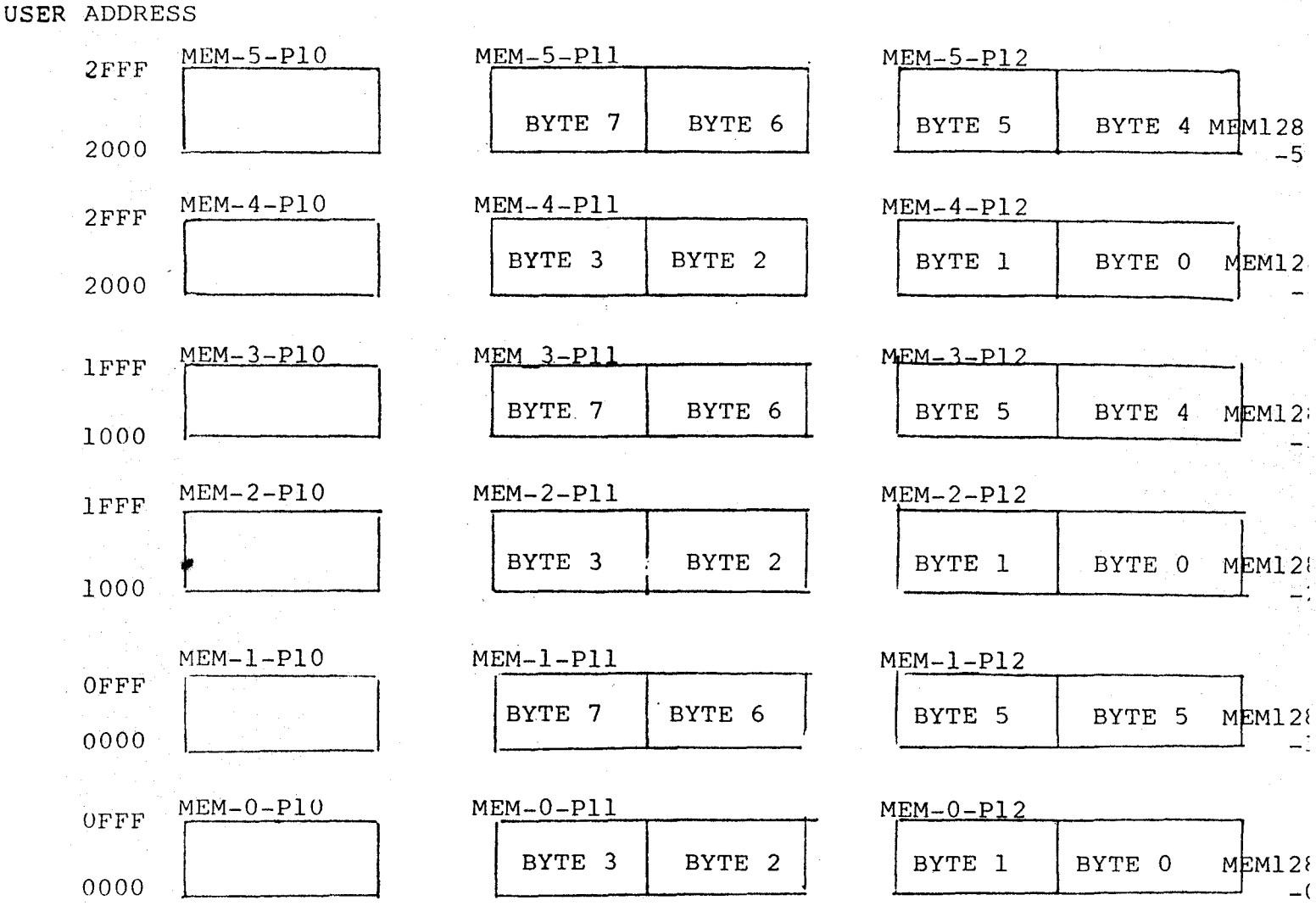


TABLE B-11 User Interface Data Mapping MEM128
32 bit Org Switches
Max Organization 12kx(36-64) bits/word

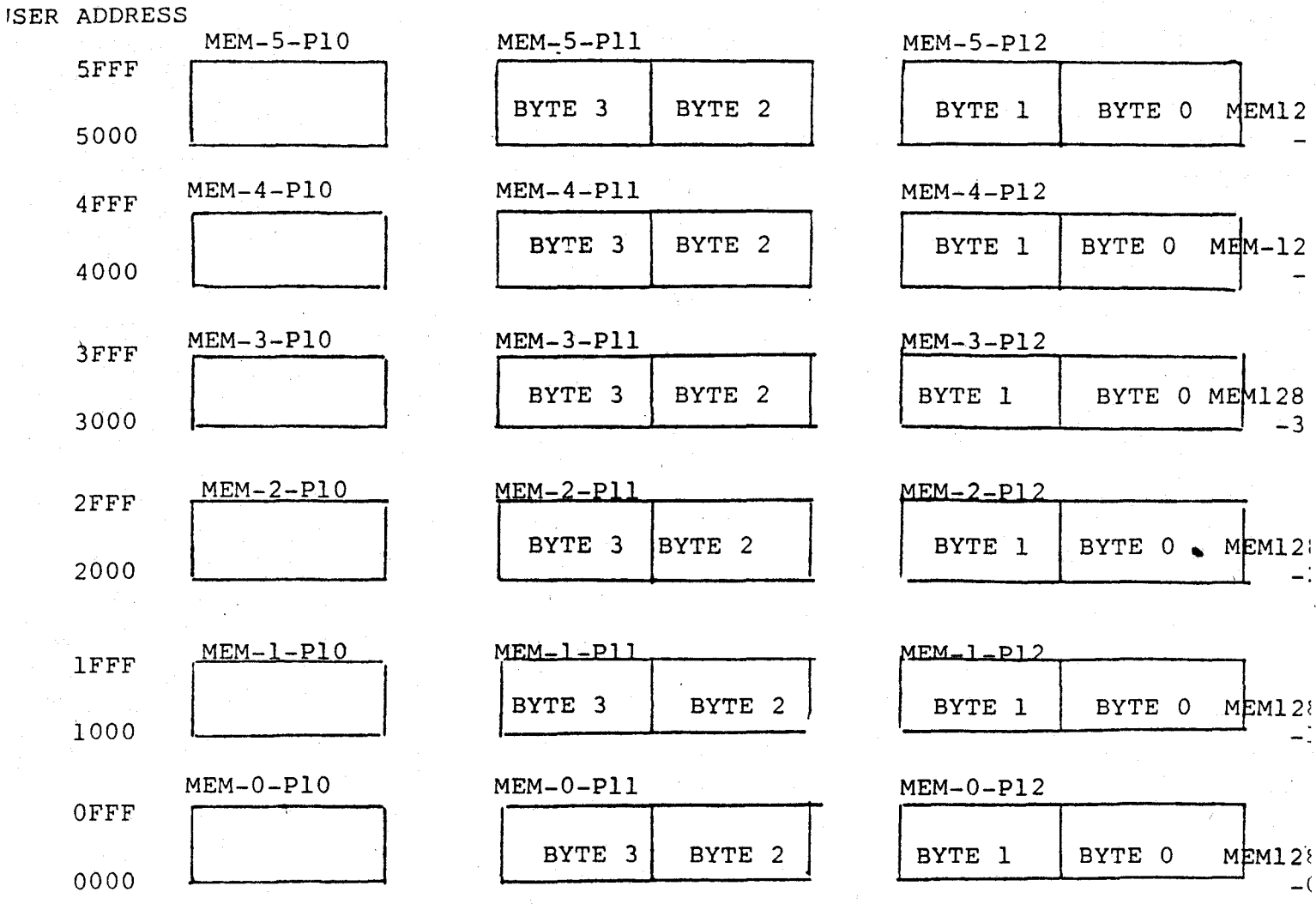


TABLE B-12 User Interface Data Mapping MEM128
32 Bit Org Switches

Max Organization 24kx (8-32) bits/word

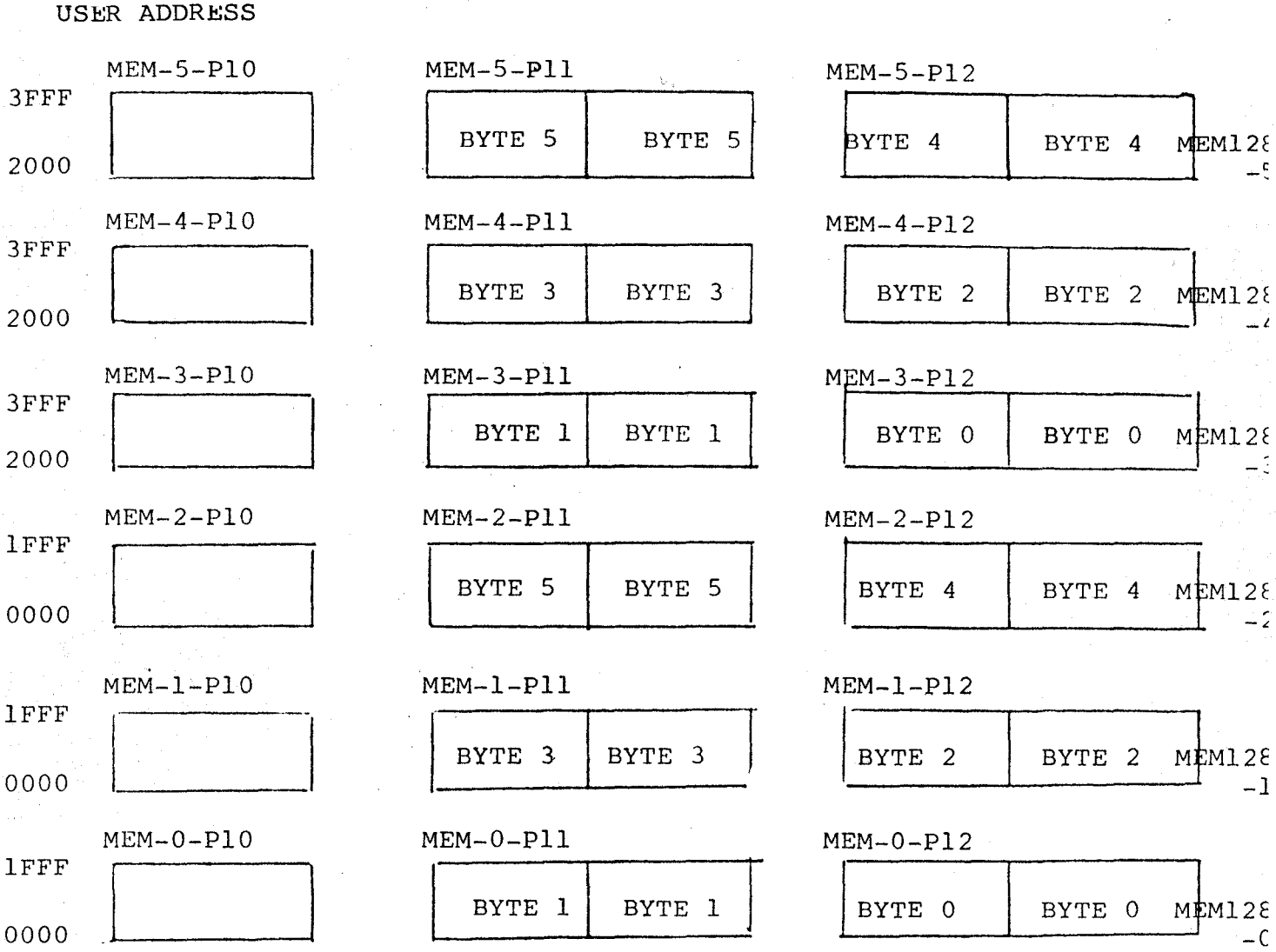


TABLE B-13 User Interface Data Mapping MEM128
16 Bit Org Switches

Max Organization 16kx (36-48) bits/word

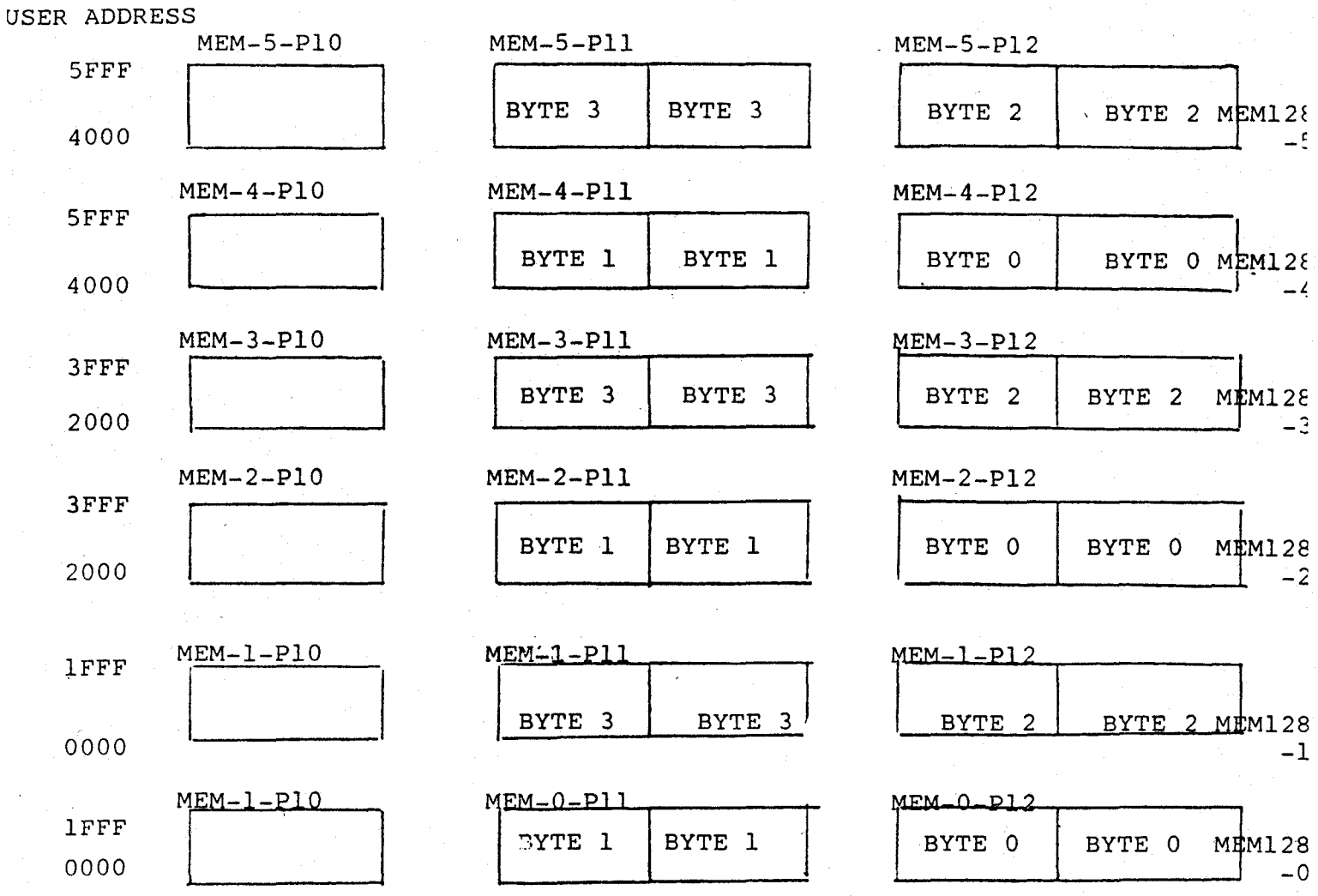


TABLE B-14 User Interface Data Mapping MEM128
16 Bit Org Switches
Max Organization 24kx(20-32) bits/word

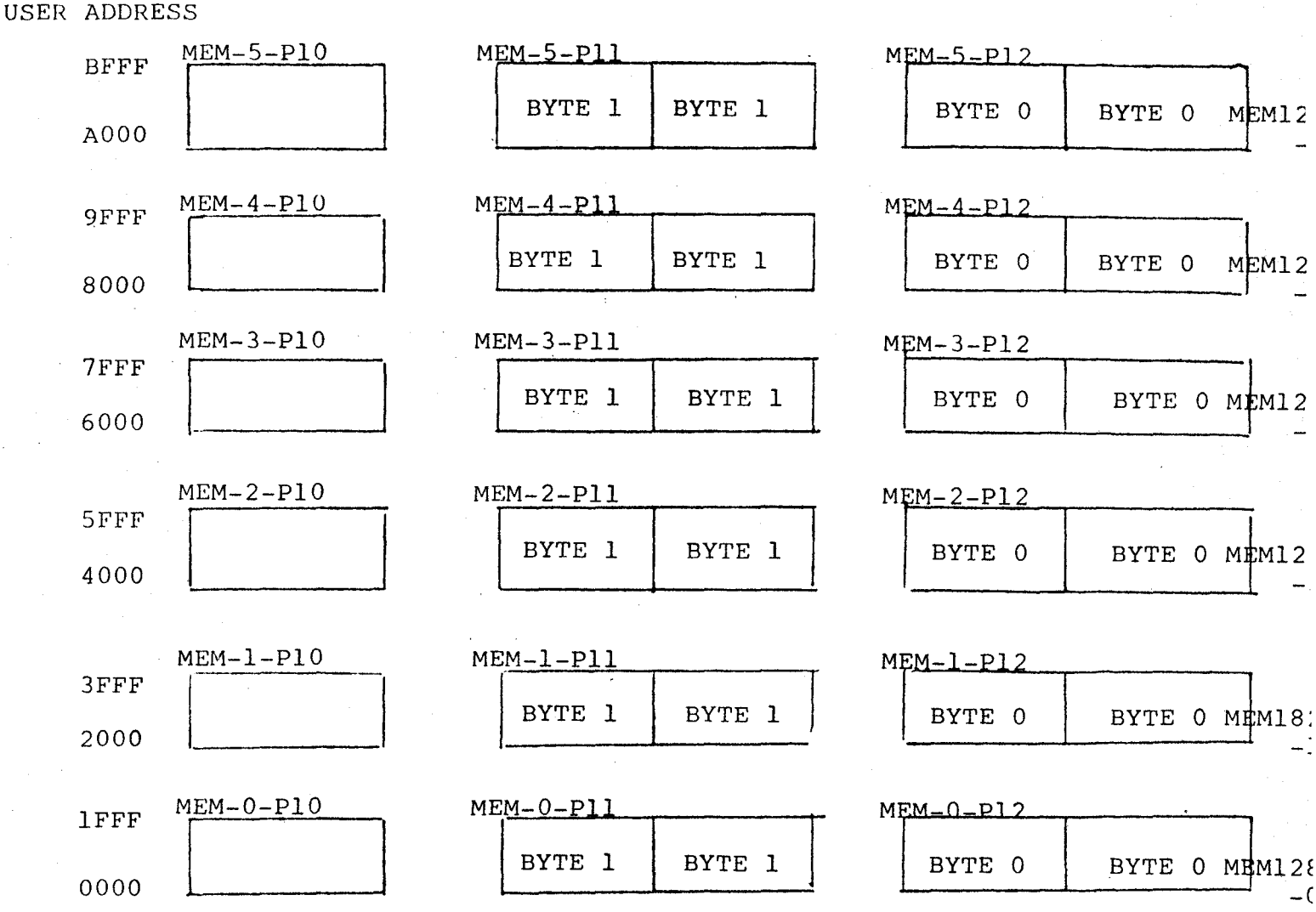


TABLE B-15 User Interface Data Mapping MEM128
16 Bit Org Switches
Max Organization 48kx (8-16) bits/word

APPENDIX C

ERROR MESSAGES

APPENDIX C STEP ERROR MESSAGES

ADDRESS OUT OF RANGE - 1) Address in a data stream being loaded in microword format + the bias address specified in the start address exceeds the available hardware limits.

2) The values specified for I/O exceed the current hardware address limit.

CHR TYPE ERROR LAST ADD= During data transfers, STEP-N checks that data is valid HEX character and reports a character type error when a non-HEX character is detected in the data stream. Where feasible the last address successfully transferred is reported.

CARD SWITCHES DO NOT AGREE - Message appears when WCS memory modules assigned to a single array to not have the same organization switch setting.

CHECKSUM ERROR LAST ADD= - When loading data in Microword™ format the checksum calculated does not agree with the checksum continued in the data stream. When feasible the last address successfully transferred is repeated.

COMPARE ERROR AT ADDRESS Message reports the address at which a compare error is detected during I/O compare operations.

COMM ERROR= OR, FE LAST ADD= - Communication error reported resulting from an OVERUN or FRAMING ERROR on the communication port. Where feasible the last address is reported. An overun condition occurs when a new character is received prior to a previous character being processed. A framing error indicates that either one or both stop bits were in error. When this error is encountered, the following conditions should be checked.

COMM ERROR= OR, FE
LAST ADD= (CONTINUED)

1) Number of STOP bits in the received data.

2) Band Rate.

3) Data polarity from the peripheral

4) Receipt of a break character will generate an overrun.

5) A short or open circut on the port.

COMM FAILURE - DCD, DSR - This message reports a communication failure on Port 1. When operating in TEXT, this message indicates loss of the Data Carrier Detect or Data Set Ready from the modem device attached to Port 1.

FMT OPTION NOT INCLUDED - Check that the format specified is valid for the function, i.e. BNPF is not loaded by STEP-N.

DATA TOO WIDE FOR MEM CONFIGURATION - Data width specified is too wide for the memory organization requested. For example, MSG appears if 32 bit data width is requested on a Writable Control Store module with 16 bit organization switches.

ILLEGAL ADDRESS SPECIFIED

1) Message appears when an address specified in conjunction with a memory manipulation command is out of range for the available hardware.

2) Also, when an address is specified in an incorrect machine data format, i.e. a HEX address with octal data format.

3) Also, a breakpoint address specified out of range will result in this error message.

ILLEGAL BAUDRATE - An illegal Baudrate has been specified. Legal Baudrates are 110, 150, 300, 1200, 2400, 4800, 9600.

ILLEGAL CHARACTER - Indicates an illegal character type or the value of parameter is out of range in the current machine context.

ILLEGAL DEVICE - Illegal Device code specified for current machine limits. (See I/O command section.)

ILLEGAL FORMAT - Illegal I/O Format code specified for current machine limits. (See I/O command section.)

ILLEGAL POSITION - Signals the operator a PROM position outside the width range of the current memory array has been requested.

LGTH NOT EQ WIDTH LAST ADD= - 3720. During data transfers in Microword ™ format the record length is checked against the STEP-N word width of the selected array. Where feasible the last address successfully transferred is reported.

MEMORY R W ERROR LAST ADD= - During load operation in Microword™ format a read after write is performed to check data loaded into memory. A read-WRITE ERROR is generated on error and where feasible the last address successfully transferred is reported.

NOT UNIQUE COMMAND - Insufficient characters were specified in the command to make up a unique command, i.e. conflicts with some other instruction.

ONLY ONE ARRAY - Message appears when the array command is invoiced to change to array = 2 and STEP-N is configured for only one array.

OUT OF RANGE - # Location specified in an I/O command results in exceeding the machine setup limits.

STARTING ADDRESS TOO LARGE - Max starting address allowed is 7FFFH.

TIMEOUT ON LINK LAST ADD= - When leading data, STEP-N will timeout after approximated 130 sec of dead time on the port in which no characters of any kind have been received. Where feasible, the last address successfully loaded is reported.

TOO MANY CHARACTERS - Too many characters specified in a command to be valid. Max = 6 or too many characters specified in a parameter field. Max = 6.

TOO MANY CARDS REQUIRED - Memory organization requested requires more WCS memory modules than the machine hardware configuration currently contain - and is available for the users current array.

TX ABORTED - Transmission aborted message appears when an I/O operation is aborted by a light at the keyboard.

VALUE OUT OF RANGE - 1) A command utilizing an address parameter will result in an address outside the range of the available hardware for the current machine organization.

2) A breakpoint is requested that is outside of the range of the available hardware for the current machine organization.

3) Width of the data word specified is too wide for available hardware or the width specified is not on a 4 bit boundary.

WAITINF FOR CTS=O - When operating on Port 1 for I/O operations, STEP-N will not proceed with I/O until the CLEAR TO SEND signal is true on the port. This provides a convenient wait for the operator to dial up time share system when operating over a modem.

ADDITIONAL ERROR MESSAGES WITH STEP-3 OPTIONS

BOARD ID ERROR - Message appears when a slot specified during a test command does not contain a board of the type (MEM-32 or MEM-128_ specified in the test.

CTS DOES NOT = RTS - During TEST 3 the RTS output is connected via the jumper connector supplied to the CTS input. Message indicates CTS is not received.

DATA COMMS ERROR BAUD= - During TEST 3, data transmitted is not identical to data transmitted. BAUD= reports the baud rate at which the error occurred.

NO RECEIVED DATA BAUD= - During TEST 3, no data is being received by the UART.

ILLEGAL CMND WHILE RUNNING - Message indicates a command has been entered from MON RUN or RUNNING which is restricted to entry from MON HLT only. Examples are FORCE™, JAM, and XSTATE™.

TRACE NOT INSTALLED - Indicates a command which requires trace in the system has been attempted.

TSETUP ERROR - Message appears when a Trace has been setup which utilizes a breakpoint and no proper breakpoint value has been set for the assigned breakpoint.

SPEED-TEST ERROR MESSAGES + SELF TEST ERROR MESSAGES See section 4.4 and section 2.2.4.

APPENDIX D

ASCII TABLE

APPENDIX D

ASCII TABLE

Graphic or Control	ASCII (Hexadecimal)	What to Type
NULL	ØØ	CNTl @
SOM (SOM)	Ø1	CNTl A
EOA (STX)	Ø2	CNTl B
EOM (ETX)	Ø3	CNTl C
EOT	Ø4	CNTl D
WRU (ENQ)	Ø5	CNTl E
RU (ACK)	Ø6	CNTl F
BELL	Ø7	CNTl G
FE (BS)	Ø8	CNTl H or ←
H. TAB	Ø9	CNTl I
LINE FEED	ØA	CNTl J
V. TAB	ØB	CNTl K
FORM (FF)	ØC	CNTl L
RETURN	ØD	CNTl M or Returr
SO	ØE	CNTl N
SI	ØF	CNTl O
DCO (DEL)	1Ø	CNTL P
X-ON (DC1)	11	CNTl Q
TAPE AUX. ON (DC2)	12	CNTL R
X-OFF (DC3)	13	CNTL S
TAPE AUX. OFF (DC4)	14	CNTL T
ERROR (NAK)	15	CNTL U or →
SYNC (ETB)	16	CNTL V
LEM	17	CNTL W

Graphic or Control	ASCII (Hexadecimal)	What to Type
SØ.(CAN)	18	Contl X
S1.(EM)	19	Contl Y
S2.(SUB)	1A	Contl Z
S3.(ESCAPE)	1B	ESC
S4.(FS)	1C	Contl [
S5.(GS)	1D	Contl ^
S6.(RS)	1E	Contl -
S7.(US)	1F	
ACK.	7C	
ALT. MODE.	7D	
RUBOUT.	7F	
SPACE	20	
!.	21	
".	22	
#.	23	
$.	24	
%.	25	
&.	26	
'.	27	
(.	28	
).	29	
*.	2A	
+.	2B	
=.	2C	
-.	2D	
.	2E	
/.	2F	
:.	3A	
;.	3B	
<.	3C	
=.	3D	
>.	3E	
?.	3F	

Graphic or Control	ASCII (Hexadecimal)
[	5B
\	5C
]	5D
↑	5E
←	5F
@	4Ø
BLANK	2Ø
Ø	3Ø
1	31
2	32
3	33
4	34
5	35
6	36
7	37
8	37
9	39
A	41
B	42
C	43
D	44
E	45
F	46
G	47
H	48
I	49
J	4A
K	4B
L	4C
M	4D
N	4E
O	4F

Graphic or Control	ASCII (Hexadecimal)
P	5Ø
Q	51
R	52
S	53
T	54
U	55
V	56
W	57
X	58
Y	59
Z	5A

APPENDIX E

TECHTRAN 950 USAGE

TO USE TECHTRAN 950 WITH STEP-N

1) Set Techtran switches as follows:

   a. Front Panel Switch to OFF LINE (down)
   b. Real Panel Rate switch 240 (2400 baud)
   c. Real Panel selector switch to BIN CTRL ON (up)
   d. Full/Half duplex switch to FULL (up)

2) Connect Step RS 232 cable from Port 1 (modum port on STEP-2) to Techtran Terminal port. Ground Pin 20 of RS 232 connector or insert S1 as described in "Adjustments".

3) Turn Techtran on (switch up) using PWR switch on Rear Panel

4) Insert Diskette with label up, reading backwards (head access slot first in). Close door.

5) Enter DUMP command on STEP-2 and set following parameters:

```
FORMAT = 0
START ADDRESS = 0
NUMBER OF LOCATIONS = 1
DEVICE = 1

BAUD (CR) = 2400
STOP (CR) = 1
QUIT
```

STEP-N is now ready to talk to the Techtran

TO FORMAT A DISKETTE = Shift B

TO WRITE TO THE DISKETTE

1) Enter DUMP(CR)

```
FORMAT = 0 (CR)
START ADDRESS = 0 (CR)
NUMBER OF LOCATIONS = MAX CODE DEPTH IN DECIMAL
DEVICE = 1 (CR)
```

2) Enter TEXT (CR)

3) Type "(C&H).W(SP)xxxxx(CR)" where xxxxx is the file name. If a mistake is made on file name spelling, type "(SP)" in place of "(CR)" and re-enter name.

   If diskette is full, the Read Write and Ready lights will flash. I/O IN PROGRESS will be displayed on the STEP-2 CRT.

4) When ENTER COMMAND appears on STEP-2 CRT, enter TEXT(CR) and type SHIFT(DEL), a number 3 on the STEP-2 keyboard. This corresponds to a control S which terminates the Techtran write.

TO READ INFO FROM DISKETTE

1) Enter TEXT (CR) from STEP-N

2) To Read diskette directory enter the following command:

.D(SP)R(CR)

3) To Read a diskette file use the following command:

.R(SP)xxxxx(CR) where xxxxx is the file name

4) To terminate a read, use SHIFT(DEL), a number 3 on keyboard which corresponds to a control S.

5) Use SHIFT V (0) to EXIT TEXT on STEP-2. Use shift Ø on Alphanumeric keyboard on STEP-3.

TO LOAD INFORMATION FROM DISKETTE

(assumes data previously written from STEP-2)

1) Enter LOAD (CR) from STEP-2 keyboard

FORMAT = 0 (CR)
START ADDRESS = 0 (CR)
NUMBER OF LOCATIONS = maximum permitted
DEVICE = 1 (CR)

2) Enter TEXT (CR)

3) Type "(C&H) .R(SP) xxxxx (CR) "where xxxxx is the file name. Note if the file name is misspelled, use (SP) in place of (CR) and re-enter the correct name.

TO COMPARE A TECHTRAN FILE TO THE CONTENTS OF STEP-2 MEMORY:

follow LOAD proceedure but use "COMPARE" command in place of load.

TO DELETE THE DIRECTORY:
Enter TEXT(CR) and type ".D(SP)D(CR)

(SHIFT BLANK =) ESCAPE
STEP-2 OR "B" STEP-3
KEY

CROSS REFERENCE TABLE

TECHTRAN CODE		STEP-2 KEYBOARD UPPER CASE	STEP-2 GENERATE USING:	STEP-3 GENERATE USING CONTROL:
CONTROL	R	2	SHIFT:	R
CONTROL	X	8	(CLEAR)	X
CONTROL	S	3	S	S
CONTROL	T	4	(DEL)	T
CONTROL	Q	1	Z	Q
CONTROL	Z	9	(C&H) D	Z

TO FORMAT A NEW DISKETTE

1) Insert Diskette
2) Enter TEXT (CR)
3) On STEP-2, press "SHIFT" and while pressing "SHIFT", key "B".
   On STEP-3, press "ESC".

APPENDIX F

OLD MEM 32 OPERATION

MEM 32 OPERATION

1. General

The original MEM32 assembly differs in a number of ways from the MEM32 A & B boards:

1) It is composed of two boards, a memory board and an interface board
2) There is no read/write operation
3) The address display function works in a slightly different fashion.
4) The address compare circuitry is different.
5) The switches are configuted differently.

2. Switch Settings

Memory operation is controlled through the four switches located between BNC1 and BNC2. There switches have the following functions:

SWITCH	POSITION		FUNCTION
S1	On		Address for CRT display is sampled from using edge of signal placed on BNC labled "SMPL".
	Off		Address for CRT display is sampled asynchronously by STEP-2 CPU.
S2	--		Not used
S3	S3	S4	Organization select
S4	On	On	Memory board width 32 bits
	On	Off	Memory board width 16 bits
	Off	On	Memory board width 8 bits
	Off	Off	Signal organization

3. Memory Access

The MEM32 board operates similarly to MEM 32A. The memory is accessed by the target processor when in "MONITOR" mode. There is no switch which bypasses Step-2 control of memory access.

4. Read/Write Operation

There is no Write mode, the MEM 32 memory board is Read Only from the target processor.

5. Address Input and Display

P10 is used for address input. The pin assignments are the same as the MEM 32A board. The UL is used as the clock input on the Int 3 &Int 4 boards and is also ANDed with the address compare circuitry. A positive true signal enables the address compare function. This is necessary to distinguish between a next address obtained by a "Jump" type command or an "Increment" type command where timing may be different and an invalid address increment occurs before the "JUMP".

The address is latched either asynchronously with respect to the target processor clock (S1=OFF) or synchronously with respect to the positive edge of the signal placed on the SMPL signal of first memory board (S1=ON). When sampled asynchronously an invalid address may be displayed. In either case the CRT display is updated twice a second.

6. Trigger Output

The trigger output is generated the same way as on MEM 32A board.

7. Data Output

Refer to MEM 32 A writeup.

8. Data Output Configuration

The MEM 32 board comes with one of four plug in interface boards: INT-1, INT-2, INT-3, INT-4.

INT-1 Unbuffered output with 100 ohm series terminations for cable driving. The output should not be connected to more than one TTL load and cannot be wired-0 Red. Used with ROM emulator outputs to plug directly into system ROM sockets.

INT-2 Buffered output with outputs capable of 0 Red configuration. Each group of eight bits has its own enable input.

INT-4 Buffered output with "shine thru" latch. Outputs are capable of wired 0 Red operation.

ROM 4,8 Seventeen, different, field-upgradable, plug-in ROM simulator outputs which emulate over 200 bipolar ROMs and PROMs: See ROM data sheet.

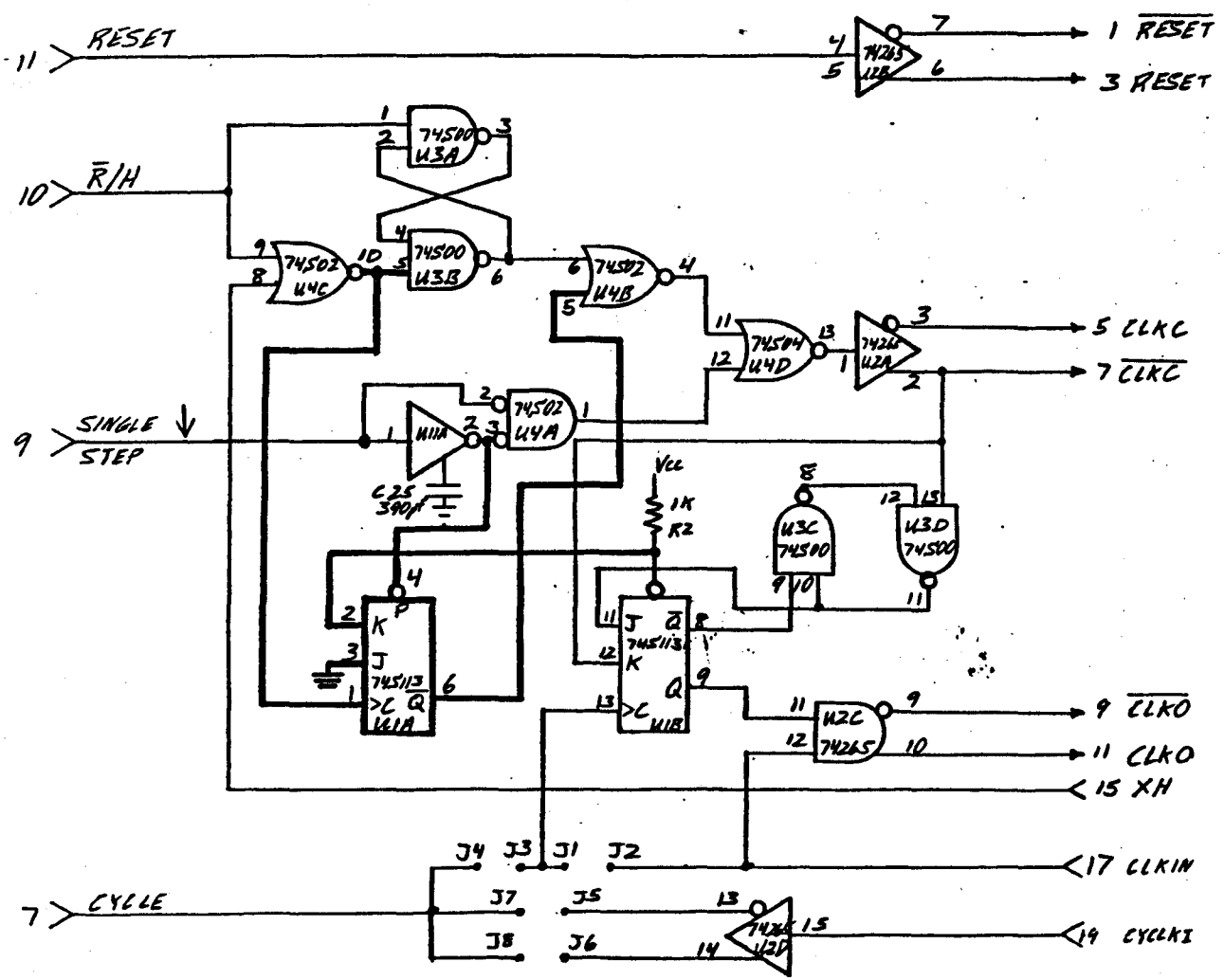
9. Direct Memory Interconnection

Refer to MEM 32 A & B writeup.

APPENDIX G

I/O CLOCK BOARD MODIFICATION

I/O & CLOCK BD MOD FOR PIPELINE SYSTEMS (SEE DWG 0001053 SHT 1)



MODIFICATION INSTRUCTIONS

A) CUT TRACE BETWEEN U4B PINS 5 AND 6

B) DISCONNECT PIN 1 U1A FROM R2 & U1 PIN 10

C) INSTALL WIRE FROM U4B PIN 5 TO U1A PIN 6

D) INSTALL WIRE FROM U4A PIN 3 TO U1A PIN 4

E) INSTALL WIRE FROM U1B PIN 10 TO U1A PIN 2

F) INSTALL WIRE FROM U3B PIN 5 TO U1A PIN 1

G) INSTALL WIRE FROM U1A PIN 3 TO U1A PIN 7(GNI

OPERATION

A) ATTACH BRKPT OUTPUT FROM MEM BD TO XHLT BN(INPUT

B) SET A BRKPT IN MON HLT

C) GO TO "RUNNING" BY PRESSING "R" (CR)

D) WHEN THE ADDR=XXXX READOUT STOPS CHANGING AND THE BRKPT HAS REVERSE VIDEO, THE TARGI PROCESSOR IS HALTED. NOTE: DUE TO TIMING CONSTRAINTS, THIS MAY BE THE ADDRESS AFTER THE BRKPT SETTING.

E) TO RESTART: 1) HOLD DOWN THE "H" KEY TO GO INTO "MON HLT" MODE.
2) PRESS "S" KEY, SINGLE STEP, TO CLEAR THE HALT STATE.

LTR	DESCRIPTION	BY	APP	DATE
B	CORR ERROR	VAB		
A	DOC RLSE # 35	VAB		

REVISIONS

STEP ENGINEERING

NEXT ASSY | USED ON

TITLE MOD 7451 I/O & CLK BOARD

B 0001151 V1

NOTES:

757 Pastoria Avenue Sunnyvale, California 94086
(408) SEE STEP (733-7837)